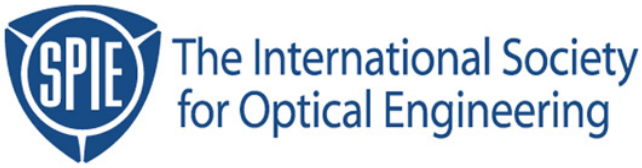

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The New, New Limits of Optical Lithography

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ABSTRACT

The end of optical lithography has been so often predicted (incorrectly) that such predictions are now a running joke among lithographers. Yet optical lithography does have real, physical limitations and even more real economic limits, and an accurate estimation of these limits is essential for planning potential next generation lithography (NGL) efforts. This paper will review the two types of resolution limits in optical lithography: the pitch resolution, governed by the amount of spatial frequency information that can pass through an imaging lens, and the feature size resolution, limited by our ability to control feature size. Projecting the trends in these resolution limits, the capabilities of 193nm immersion lithography will be explored.

Keywords: Resolution Enhancement, Resolution Limits, Optical Lithography

1. Introduction

Optical lithography has been the mainstay of semiconductor patterning since the early days of integrated circuit production. The continual reduction of the dimensions of the features used to construct transistors has allowed these transistors to become ever smaller, faster, lower power-consuming, and cheaper. Historically, the smallest features on a wafer have been reduced in size by about 30% every two to three years. As a result, chips with features less than 100nm across are in production today. Many technological barriers confront us when simultaneously shrinking transistor size and increasing the number of transistors on a chip. Ultimately, however, chip manufacturing has always been limited by our ability to print small features cost-effectively. As a result, the resolution limits of optical lithography tend to dictate the manufacturing capabilities of our industry. This paper will begin with a discussion of the factors that affect lithographic quality, leading to a definition and description of lithographic resolution. Using this foundation, the resolution limits of optical lithography will be explored, including the common approaches to extending this resolution.

2. Lithographic Quality

Improving quality in manufacturing is a continual process. Like reducing costs and improving productivity or throughput, quality improvements benefit everyone from the customer to the manufacturer. How can lithographic quality be improved? One of the foundational tenets of quality management is this: before quality can be systematically improved, it must be numerically measured. Just looking at an SEM picture of a photoresist profile and saying "yes, the quality has improved" is not good enough. Numerical metrics of quality must be defined, directly related to customer benefits, and then measured before they can be used to systematically improve your lithography.

So how is lithographic quality defined? This simple question has a surprisingly complex answer. Lithography is such a large component of the total manufacturing cost of a chip and has such a large impact on final device performance that virtually all aspects of the lithography process must be carefully considered.

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Although somewhat arbitrary, I have divided lithographic quality into four basic categories: photoresist profile control, overlay, down-stream compatibility, and manufacturability.

Photoresist Profile Control is a superset of the common critical dimension (CD) control metric that is universally thought to be the most important aspect of high resolution lithography processes. For many lithographic steps the ability to print features at the correct dimensions has a direct and dramatic influence on device performance. It is typically measured as a mean to target CD difference for one or more specific device features, as well as a distribution metric such as the standard deviation. Spatial variations across the chip, field, wafer or lot are also important and can be characterized together or individually. In addition, the sensitivity of CD to process variations is often characterized and optimized as a method to improve CD control. Metrics such as resolution, depth of focus, and process latitude are expressions of CD control. For example, resolution can be defined as the smallest feature of a certain type that provides adequate CD control for a given process.

Profile control, however, recognizes that the printed resist patterns are three-dimensional in nature and a single CD value may not be sufficient to characterize their lithographic quality. Extension of CD control to profile control means taking into account other dimensions. In the "z direction" from the top to the bottom of the photoresist, the resist profile shape is usually characterized by a sidewall angle and a final resist height. In the "x-y direction" patterns more complex than a line or space require a shape characterization that can include metrics such as corner rounding, line-end shortening, area fidelity, line edge roughness, or the critical shape difference.

Overlay is the ability to properly position one lithographic level with respect to a previously printed level. In one sense, lithography can be thought of as an effort to position photoresist edges properly on the wafer. But rather than characterize each edge individually, it is more convenient to correlate two neighboring edges and measure their distance from each other (CD) and the position of their midpoint (overlay). One simple reason for this division is that, for the most part, errors that affect CD do not influence overlay, and vice versa. (Unfortunately, this convenient assumption is becoming less and less true as the target feature sizes shrink.) Overlay is typically measured using special targets optimized for the task, but actual device structures can be used in some circumstances. Since errors in overlay are conveniently divided into errors influenced by the reticle and its projected image, and those influenced by the wafer, measurements are made within the exposure field and for different fields on the wafer to separate out these components. While historically CD control has gained the most attention as the limiter to feature size shrinks, overlay control may soon be as critical or even more so.

Down Stream Compatibility describes the appropriateness of the lithographic results for subsequent processing steps, in particular etch and ion implantation. Unlike many other processing steps in the manufacture of an integrated circuit, the handiwork of the lithographer rarely finds its way to the final customer. Instead, the true customers of the lithography process are the etch and implant groups, who then strip off those painstakingly prepared photoresist profiles when finished with them. Downstream compatibility is measured with such metrics as etch resistance, thermal stability, adhesion, chemical compatibility, strippability, and pattern collapse.

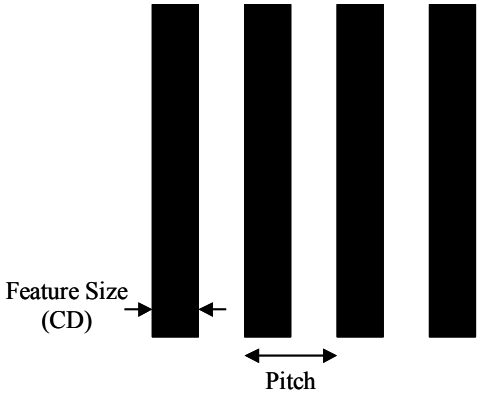
Manufacturability is the final, and ultimate, metric of a lithographic process. The two major components of manufacturability are cost and defectivity. The importance of cost is obvious. What makes this metric so interesting, and difficult to optimize, is the relationship between cost and other metrics of lithographic quality such as CD control. While buying ultra flat wafers or upgrading to the newest stepper platform may provide an easy improvement in CD and overlay performance, their benefit may be negated by the cost increase. It is interesting to note that throughput (or more correctly overall equipment productivity) is one

the major components of lithographic cost for a fab that is at or near capacity due to the normal factory design that places lithography as the fab bottleneck.

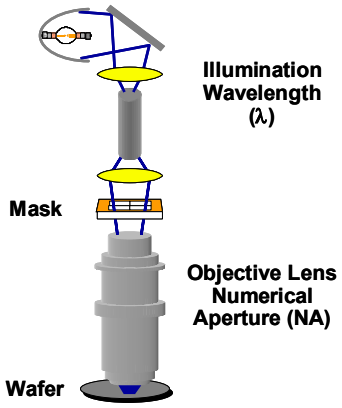
Defectivity in all areas of the fab has been the major contributor to yield loss for most processes throughout the history of our industry, though this is currently changing due to increased parametric yield losses. Because lithographic processes are repeatedly applied to make a chip, any improvements in defectivity in the lithography area is multiplied many times over. Finally, concerns such as safety and environmental impact will always play a role in defining the overall manufacturability of a process.

The outline for defining lithographic quality presented above gives a flavor for the complexity of the task. Literally dozens of quality metrics are required to describe the true value of a lithographic result. However, once these metrics have been defined, their relative value to the customer evaluated, and methods for their measurement established, they become powerful tools for the continuous improvement required to remain competitive in semiconductor manufacturing. One important use of lithographic quality metrics is in the definition of resolution. Quite simply, resolution is defined as the smallest feature that can be printed with acceptable quality for a desired purpose.

3. Resolution



The resolution limit of optical lithography is not a simple function. In fact, resolution limits differ depending on what type of feature you are trying to print. In general, however, there are two types of resolution: the smallest pitch that you can print (the pitch resolution) and the smallest feature that you can print (the feature resolution). While related, these two resolutions are limited differently by the physics of lithography, and have different implications in terms of final device performance. Pitch resolution, the smallest linewidth + spacewidth pair that we can print, determines how closely we can pack transistors together on one chip. This resolution has the greatest impact on cost per function and functions per chip. Feature size resolution determines the characteristics and performance of an individual transistor, and has the greatest impact on chip speed and power consumption. Obviously both are very important.



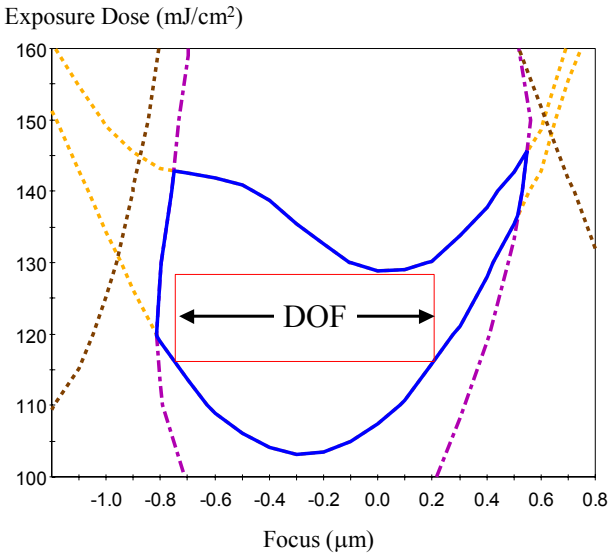
Pitch resolution is the classical resolution discussed in most optics textbooks and courses. It is governed by the wavelength of the light used to form the images and the numerical aperture of the imaging lens. The classical pitch resolution is given by a version of the Rayleigh equation

$$pitch\ resolution = k_{pitch}\frac{\lambda}{NA}$$

where λ is the vacuum wavelength of the lithographic imaging tool, *NA* is the numerical aperture, and k_{pitch} depends on the details of the imaging process [1]. Ultimately, k_{pitch} can be as low as 0.5, but only with tremendous effort (as will be discussed below). Values of 0.8 – 1.0 are more typical today.

While pitch resolution has a hard physical limit given by the Rayleigh equation, feature resolution is limited by our ability to control the critical dimension (CD) of the feature. As features are made smaller, our control of the CD of that feature is worse. There is no hard cut-off, only a continual worsening of CD control as the feature size is reduced. Feature size control is governed by the magnitude of various process errors that inevitably occur in a manufacturing environment (such as focus and exposure errors), and the response of the process to those errors. In order to improve CD control one must simultaneously reduce the sources of process errors and improve process latitude (the response of CD to an error). Interestingly, process latitude is similar to pitch resolution in that it also depends most strongly on the imaging wavelength and numerical aperture, though in more complicated ways.

Process latitude is an exceedingly general concept, but usually the most important process latitudes are the interrelated responses of CD to focus and exposure. Using the process window to characterize these responses [2], we define depth of focus (DOF) as *the range of focus which keeps the resist profile of a given feature within all specifications (linewidth, but also sidewall angle and resist loss) over a specified exposure range* [3]. As any lithographer who has ever struggled with attempts to improve feature resolution knows, one of the most insidious problems of lithography is that small features tend to have smaller depth of focus. In fact, feature resolution can be succinctly defined as *the smallest feature of a given type which can be printed with a specified depth of focus* [4]. The specification for DOF is governed by the magnitude of the process errors present in the manufacturing process, while the DOF itself is used as a proxy for the full range of process latitudes that govern the resulting CD control.

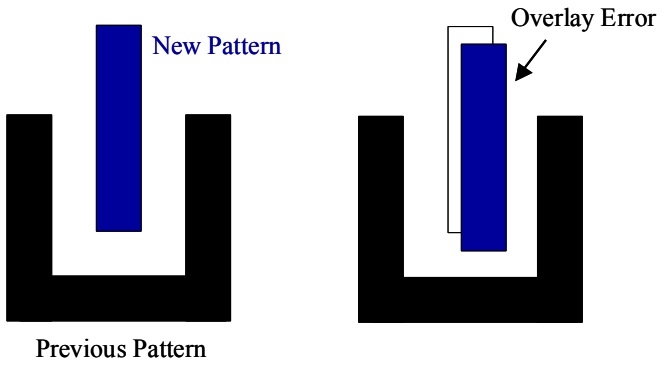


This last point is worth reiterating. Lithographers expend a large amount of effort to characterize and improve the focus-exposure process window for two reasons. First, focus and exposure are two of the most important variables in lithography and their proper control is essential to achieving good lithographic quality. But secondly, and equally importantly, focus and exposure are used to represent all of the possible process errors that can occur in the fab. Process errors fall into two broad categories [5]: those that affect the "set point" of the process (of which exposure is the primary example) and those that affect the "slope" or gradient of the information being printed in the resist (exemplified best by focus). Every process error can be related to one or both of these categories. Thus, characterizing the response of the process to focus and exposure errors can serve as an adequate stand-in for all possible process errors and responses.

4. Overlay – Lithography on Multiple Levels

The above description of resolution in semiconductor lithography ignores one important aspect of chip manufacturing – lithography is not done just once to make one chip, it is repeated many times. An integrated circuit is built up layer by layer to create a complex, three dimensional structure of many different materials. Anywhere from 20 to 30 separate lithography steps are performed on a wafer to create a modern chip. The limits of resolution, as discussed previously, apply to any one of these lithography steps. But there is another

important type of resolution that relates to how one lithography step prints relative to a previous lithography step. When printing a small pattern one must not only get the size of that feature correct, one must place that feature on the wafer at just the right spot so that it can work correctly with the patterns defined by previous lithography steps. Overlay is the measure of how well one pattern is placed on a wafer relative to a previously defined pattern.



Overlay errors have a definite impact on how small we can make the circuit device. Given a certain expected amount overlay error, the chip must be designed with enough room between the various components in order to tolerate these errors without causing device failure. As a result, the transistors are not as small and are not packed as tightly together as they might otherwise be. The biggest impact of adding tolerance for overlay errors is a decrease in packing density and a subsequent increase is chip size. Like pitch resolution, overlay control affects price per function and functions per chip. Continuously improving our ability to control overlay is almost as important as improving our ability to control CD.

5. Improving Resolution

Since both pitch resolution and feature resolution are important, the following approaches are used to improve "resolution" in general:

- Reduce the exposure wavelength
- Increase the imaging lens numerical aperture
- Reduce k_{ptich} by moving from three-beam imaging to two-beam imaging
- Increase the focus-exposure process window size
- Reduce the magnitude of process errors such as focus and exposure errors

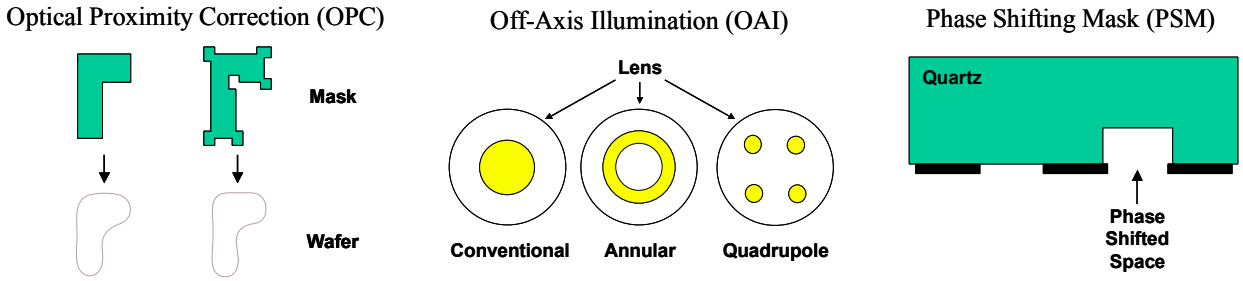
But here's the rub: several of these factors work against each other. For a given feature, there is an optimum numerical aperture that gives the largest process window. Increasing the NA further will reduce the process window, making the feature resolution worse even as the pitch resolution is improved. Reducing wavelength is always good, but as a practical matter it is extraordinarily difficult since we are limited by our ability to engineer materials with the proper optical properties at the lower wavelength. Of course, reducing the magnitude of process errors is a never ending quest with cost being the only possible downside. That leaves two final resolution enhancement approaches: reducing k_{pitch} and increasing the size of the process window.

By far the most effective and popular process window improvement approach has been improvements in the photoresist. Over the years resist capabilities have undergone dramatic progress. While we are still far from being able to ignore the photoresist (meaning that resist properties in no way limit our lithographic capabilities), resist performance today is high enough that even small improvements in optical imaging can be seen in the final patterns.

Attempts to improve the process window by optical means (sometimes called optical "tricks") include:

- Optimization of the mask pattern shape (called optical proximity correction, OPC)

- Optimization of the angles of light illuminating the mask (called off-axis illumination, OAI)
- Adding phase information to the mask in addition to intensity information (called phase shifting masks, PSM)
- Control of the polarization of the illumination (a technique too new to have an acronym yet)



Collectively, these optical approaches are known as resolution enhancement technologies (RETs) [6-8]. While some techniques improve feature resolution at the expense of pitch resolution, many of the RET approaches can improve pitch resolution and increase the process window simultaneously, a seemingly no-compromise path to resolution enhancement. However, the most promising RETs (especially the best PSM techniques) require a revolution in chip layout design that has yet to occur. Ultimately, a k_{pitch} as low as 0.5 is possible, but only for chips designed specifically to take advantage of these RETs.

Overlay, as a type of "resolution", has historically been seen as independent of the other feature size resolutions. Lithographers were divided into CD engineers and overlay engineers, and there was not much need for them to interact. All of the many fine adjustments that the overlay engineers made to the stepper had no discernable impact on critical dimensions. Adjustments made by the CD engineer to the resist process or stepper dose and focus did not impact overlay enough to worry about. But as both CD and overlay requirements push down to the nanometer level we find that many of the same sources of CD errors are also causing overlay errors. Aberrations in the stepper or scanner cause not only CD errors but also pattern placement errors that vary across the field and are different for different pattern types. Even focus and exposure errors can affect overlay results and overlay measurements. And the use of non-perfect phase shift masks combine with all of the above errors in very complex ways to impact pattern placement. In the sub-100nm lithography world control of CD and control of overlay are beginning to merge.

6. The "Limits" of Optical Lithography

Assuming a continuation of the basic trends of Moore's Law and the economically compelling justification for pushing optical lithography to its very limits, what are those limits? Examining the resolution drivers of wavelength, numerical aperture, RETs and process control, some predictions can be made.

Wavelength: Each change in wavelength made by the industry has been progressively more expensive, limited mostly by the initial lack of maturity of the photoresist. The transition to 193nm lithography has been much slower than expected and the switch to 157nm may never occur. It is quite likely that 193nm will be the last wavelength, thanks in part to immersion lithography (discussed more below). Resist for 248nm exposure are very mature and exhibit incredible performance. Especially when considering the feature resolution limited by CD control, early adoption of 193nm lithography may actually mean a loss in resolution. However, 193nm resist are quickly improving in capability and, if past trend continue, will soon surpass 248nm materials in performance.

Numerical Aperture: Dry (conventional) scanners will probably reach numerical apertures of 0.9 this year. However, the cost/benefit trade-off of pushing much past this achievement does not look promising. Immersion lithography is poised to change things dramatically. The high refractive index (1.44) and transparency of pure water at 193nm means that lenses with numerical apertures greater than 1 can be designed and built. It is important to note that immersion fluids do not *make* the numerical aperture higher, they simply *enable* a higher numerical aperture [9]. Pushing the "brick wall" of the highest possible NA from 1.0 to 1.44, however, does allow the exponential rise in cost and complexity that comes with approaching a physical limit to slow a bit. A numerical aperture of 1.2, and possibly up to 1.3, seems likely. And with the use of this immersion fluid comes an improvement in depth of focus of at least the immersion index, and sometimes up to a factor of 2 [9]. It is probably more accurate, though, to say that immersion will slow the shrinking of the process window as feature size is reduced.

Resolution Enhancement Technologies: The use of off-axis illumination has been a tremendous enabler for resolution enhancement. Quadrupole in particular is perfect for improving the resolution and depth of focus for dense features. But quadrupole (and its many variants) can only reduce k_{pitch} to 0.707 (a half-pitch $k_1 = 0.35$) at the most. Since this limit assumes an infinitely small quadrupole radius, the practical limits is more like $k_{pitch} = 0.8$ (a half-pitch $k_1 = 0.4$). To push beyond this limit one must switch to annular or cross-quadrupole source shapes. These sources can conceivably push k_{pitch} to about 0.6, but with a significant loss of process window (especially exposure latitude). Attenuated phase shift masks are commonly used to get some of this exposure latitude back, but lowering k_1 from 0.4 to 0.3 is a tremendous effort. Strong phase shifting masks (such as alternating PSM) or the use of dipole illumination can overcome some of these limitations but only at the expense of a double exposure. Dropping below $k_{pitch} = 0.8$ (and pushing to 0.6) puts even greater emphasis on resist performance and process control.

Process Control: Looking at the historical trends of process window sizes as a function of the minimum pitch used in manufacturing, the depth of focus has tended to be about linearly proportional to the pitch (as a rough rule of thumb, I use DOF ~ 1.5*minimum pitch). Thus, process windows tend to shrink about 30% each process generation, though immersion lithography should bring some relief to this trend (possibly growing DOF to be ~ 2.5*minimum pitch). To live with these smaller process windows, a reduction in the sources of process variations is required. One area that will no doubt receive considerably more attention in the next few years will be better feedback control of best dose and focus to the scanner. There seems to be no inherent stumbling blocks to continuing to live within the confines of these smaller process windows.

As a result of these trends and coming capabilities, future 193nm immersion scanners could achieve 90nm pitch performance with a single exposure (assuming NA = 1.3 and $k_{pitch} = 0.6$). Double exposure opens up the possibility for even further resolution improvements, though the true limits of this approach have yet to be adequately explored. As for feature resolution, CD control limits should push feature sizes to about 30nm, and possibly a bit lower. The ultimate limitation to feature resolution will probably be line edge roughness.

7. Conclusions

So where does all of this leave the future of semiconductor lithography? Lithography is hard and getting harder. There will be no revolution that makes it easier again. The fundamental pitch limits require us to reduce wavelength (though a transition to 157nm will be very expensive), increase numerical aperture (immersion lithography will raise NAs above 1) and use strong RETs. Feature size resolution limits will take

advantage of all of the pitch resolution enhancements, plus use improving photoresists and continuous process control improvements to push individual features to incredibly small sizes. Overlay control requirements will put increasing demands on exposure tool mechanical precision, as well as highly corrected lens aberrations to limit image distortion. However, the full potential of optical lithography will be unlocked only when chip design processes are modified to conform to the constraints of lithography's physical limits (a topic that has been recently dubbed "design for manufacturing"). In the end, our industry will optimize the technical trade-offs of lithography for the lowest cost production of the chips that consumers want.

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