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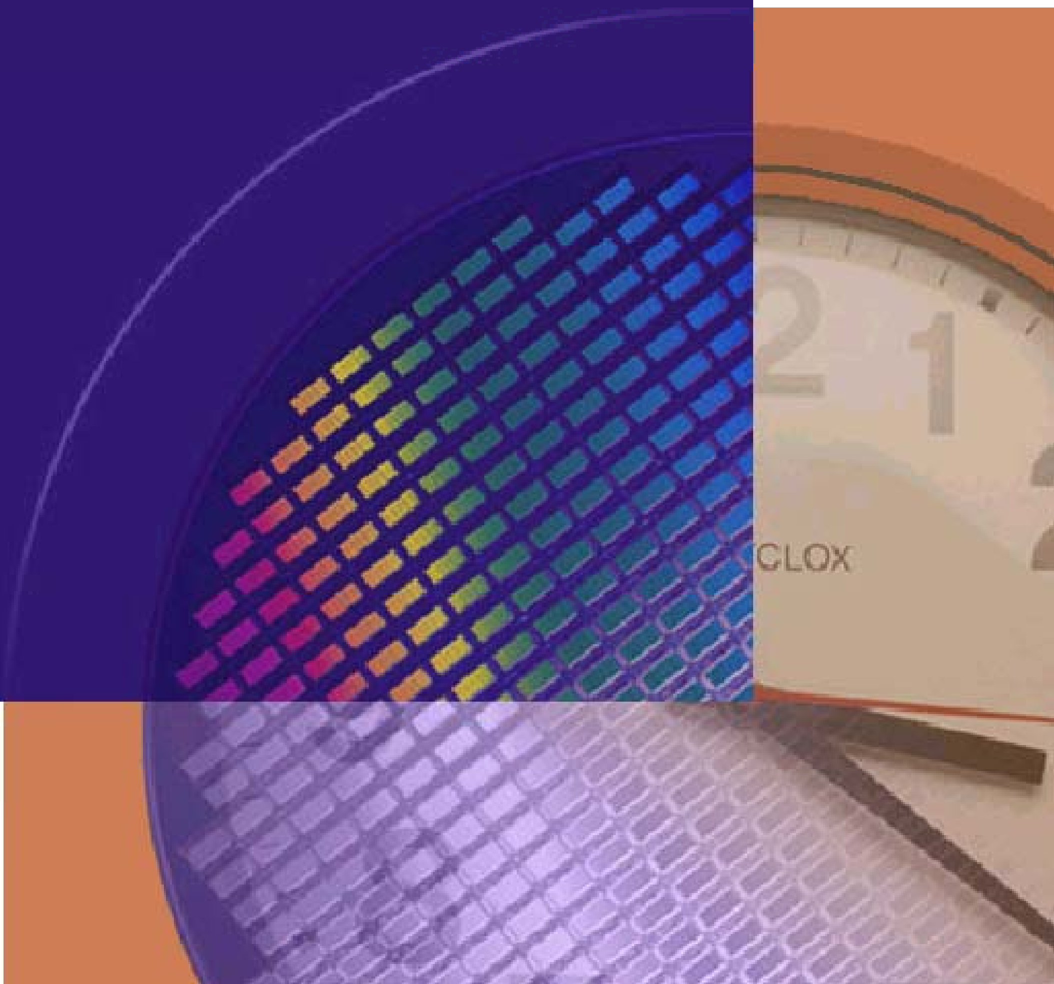
The Yield Management Company

The End of the Semiconductor Industry as We Know It

Chris Mack



Disclaimer

The views presented here are my own and are not meant to be forward-looking statements about the semiconductor industry's financial performance.

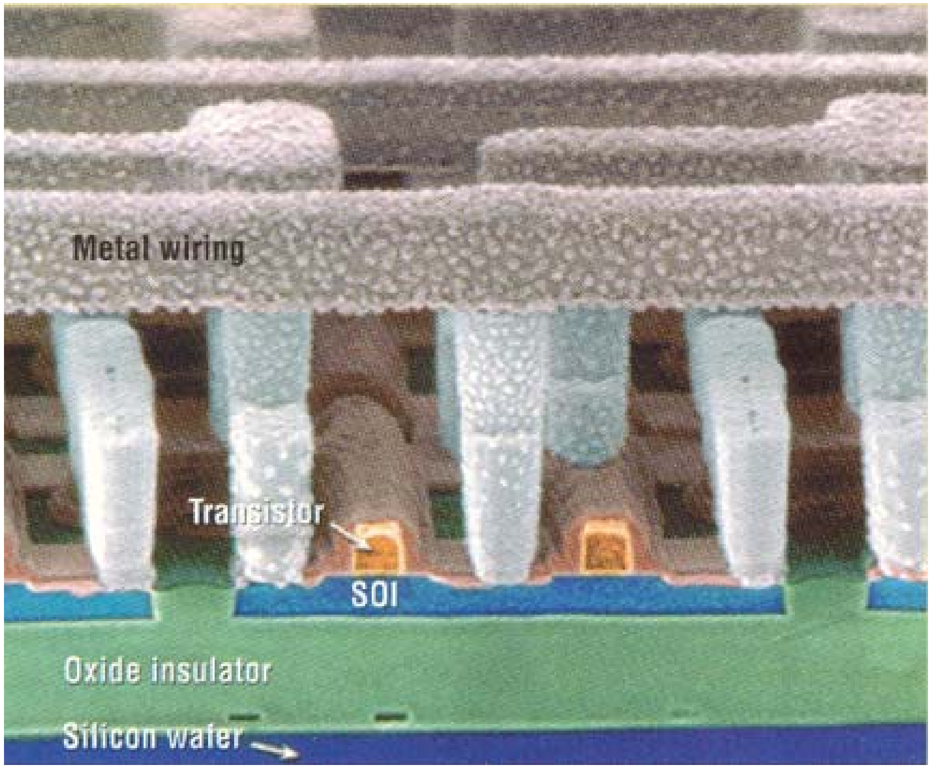
The resemblance of any characters depicted here to any persons, living or dead, is purely coincidental.

Offer not valid in the state of Nevada.

Individual results may vary.

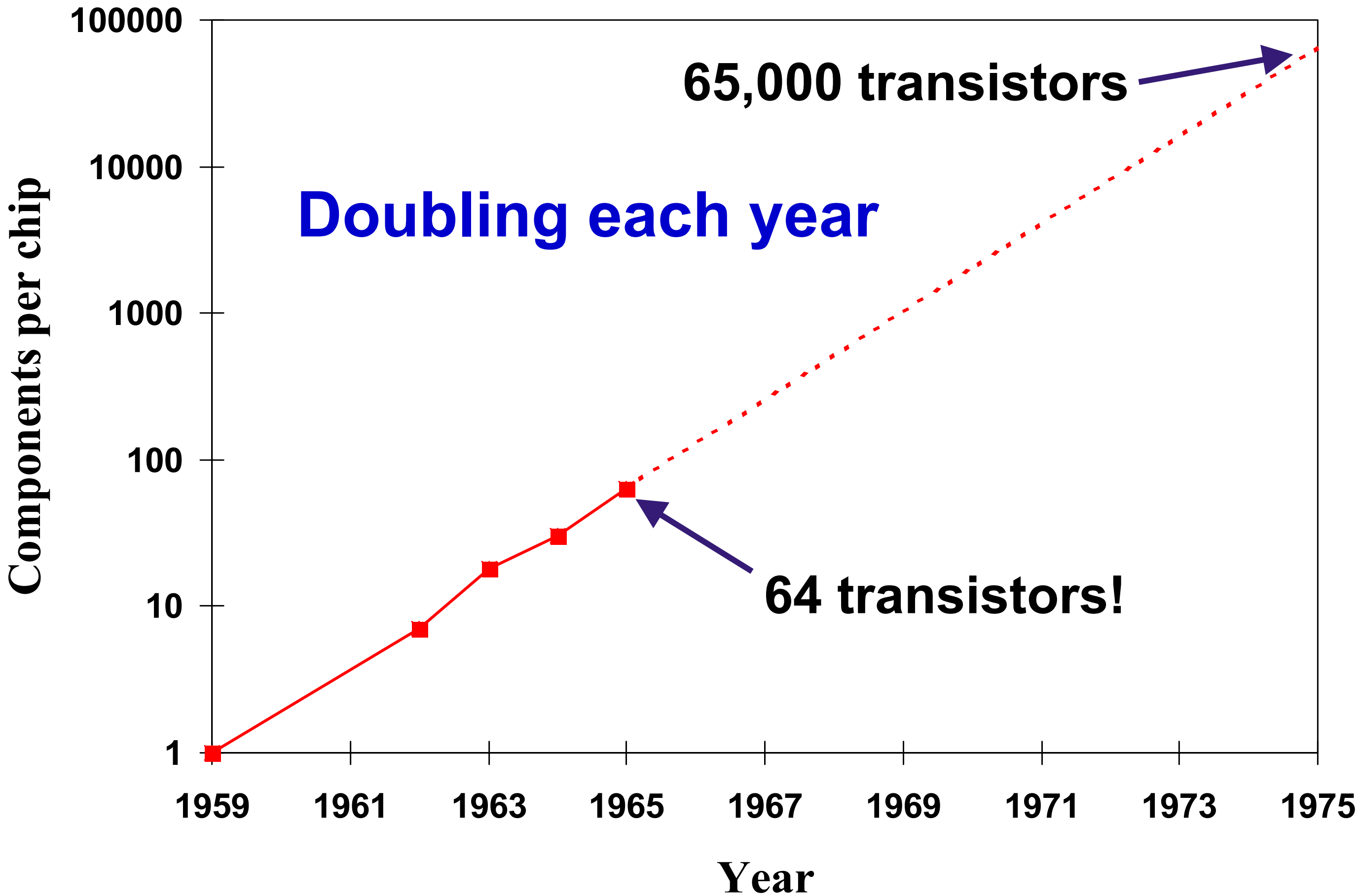
Outline

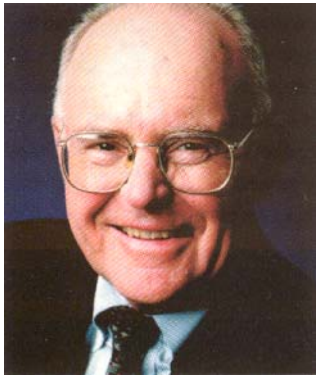
- Moore's Law
  - Past, Present, and Future
- Drivers for Lithography
  - Push vs. Pull
- Semiconductor Industry Economics
- Defining the Challenges



Moore's Law

- 1965: Moore's Observation





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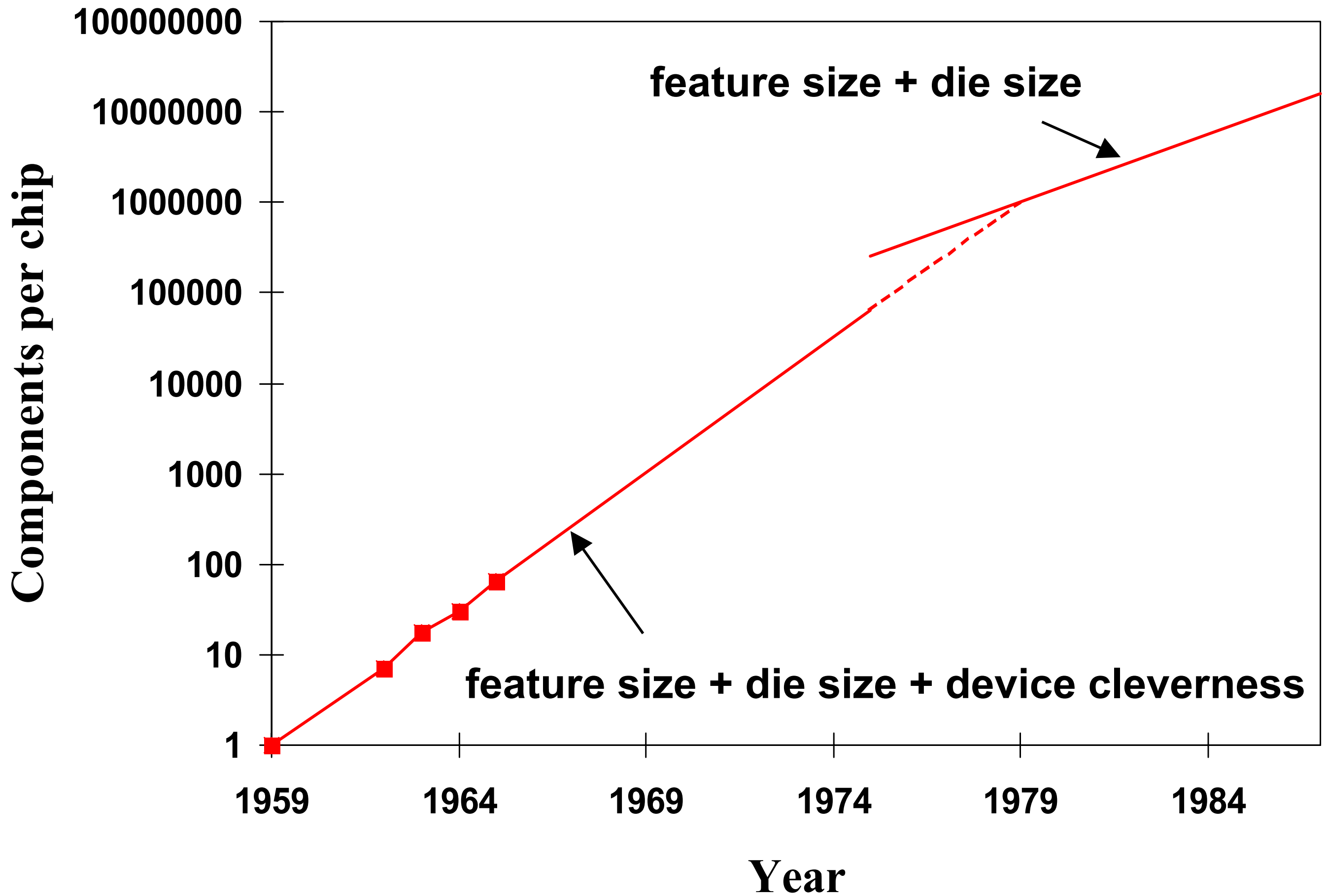
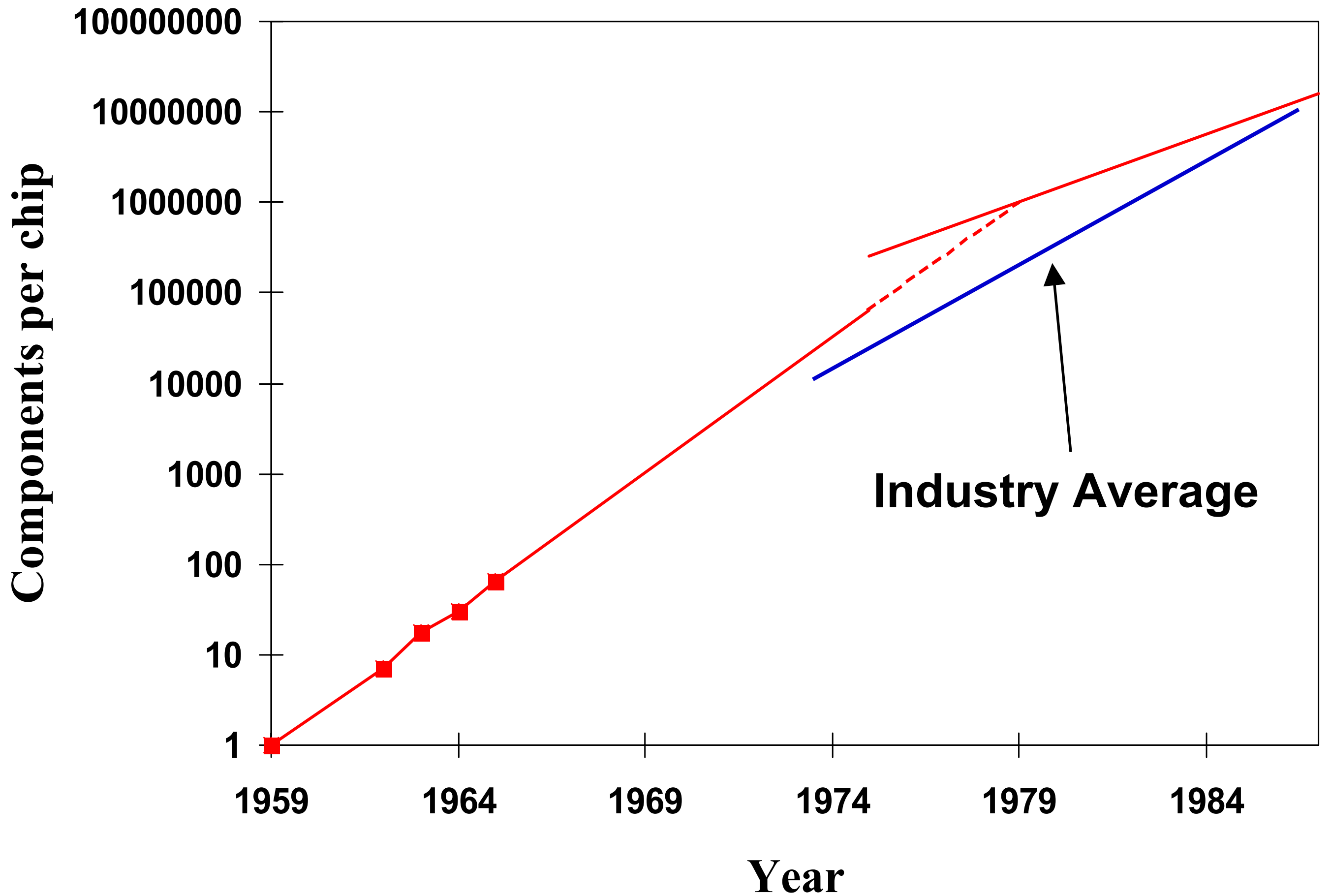
Moore's Law

- 1975: Moore's Next Observation



Moore's Law

- 1980s: Moore's Law



Moore’s Law

- 1990s: Moore’s Self-Fulfilling Prophecy
  - 1994 National Technology Roadmap for Semiconductors
    - Moore’s Law is now the industry’s law
    - No one can afford to fall behind
  - 1997 National Technology Roadmap
    - Moore’s Law is accelerated
    - We have to beat the law to stay competitive
  - 1999 ITRS Roadmap: More Acceleration
    - Dual roadmap: realists versus wishful thinkers?
  - 2001 ITRS Roadmap: Acceleration is here to stay
    - Predictions of a slowdown back to 18 month cycles are always three years out
- There is a sense of inevitability

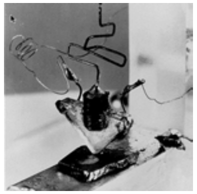
Moore’s Law

- In retrospect, Moore’s Law has been going on for 100 years!

1900	**1 inch**	← **Telegraph wires**
1912	**¼ inch**	← **Electromechanical relays**
1924	**1/16 inch**	
1936	**16 mils**	← **Vacuum tubes**
1948	**4 mils**	← **Miniature vacuum tubes, Solid State Transistors**
1960	**1 mil (25 μm)**	↖ **Current version of Moore’s Law begins**







Moore's Law

- 1995 Prediction (Semiconductor International):
  Mack's Roadmap to Retirement - Life in the Year 2025

Memory Chip:	**64 Tb**	
Feature Size:	**10 nm**	
CD control:	**± 1 nm (± half resist molecule)**	
Chip Area:	**3" X 6"**	← **First casualty**
Wafer Size:	**32"**	← **Second casualty**
Chip Price:	**$1000**	← **No one will pay it**
Fab Cost:	**$1 Trillion**	← **No one can pay it**

Moore's Law

- 2003: A Roadmap to the Roadmaps

1994 Roadmap: 100 nm production in 2007
1997 Roadmap: 100 nm production in 2006
1999 Roadmap: 100 nm production in 2005
2001 Roadmap: 100 nm production in 2004

- Trend Analysis: By the 2003 Roadmap, we'll have finished the 100 nm node before we've even started it!

Moore's Law

- Current Trends
  - Die size has stopped growing (and in fact is shrinking)
  - Feature size must shrink faster to make up the difference!
  - Moore's Law acceleration is for feature size, not number of transistors (just look at DRAM)
- 2003: Moore's Technomantra
  - Build it and they will come
- Moore's Law is not a law – it is an act of will!

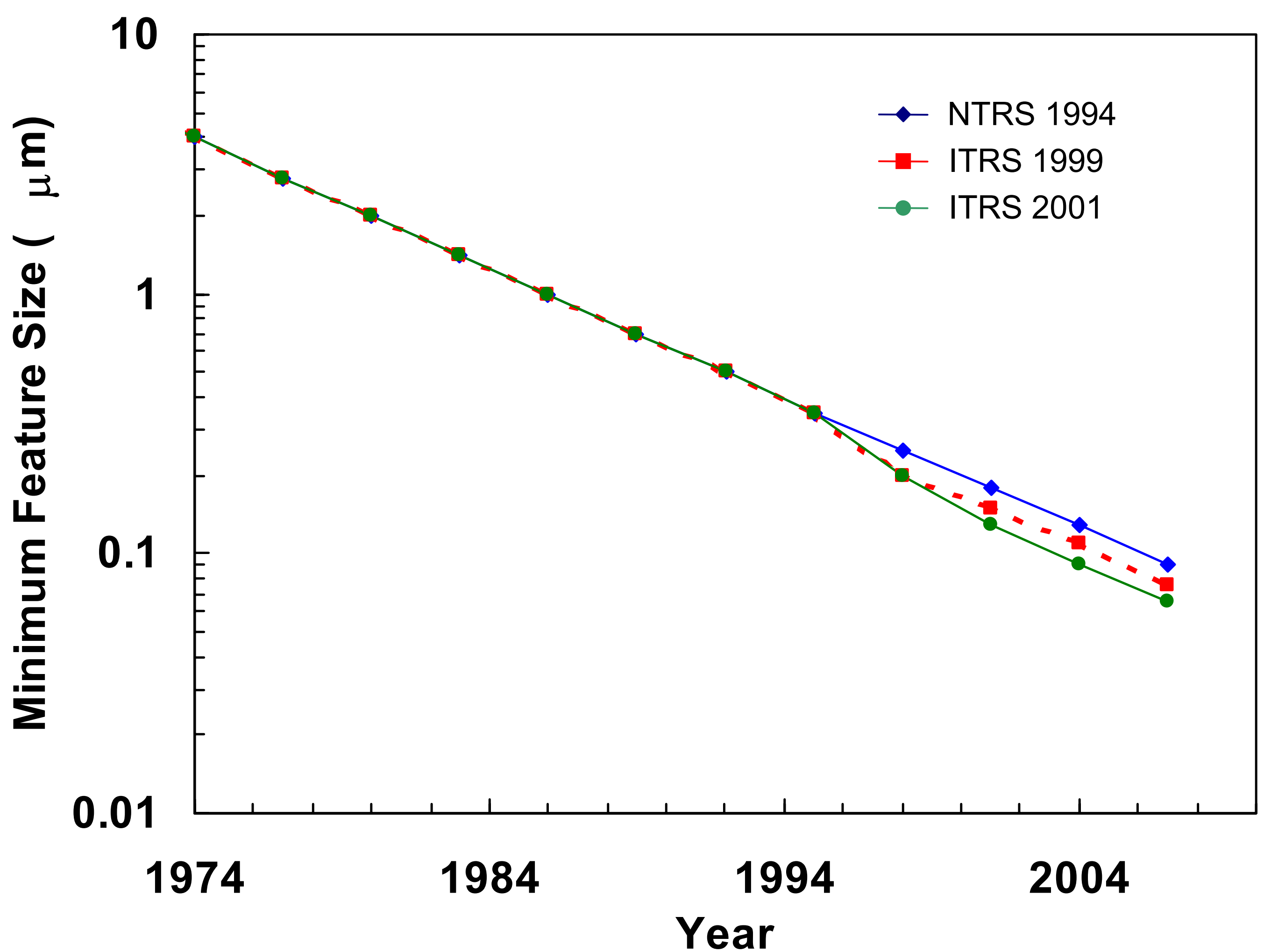
Moore’s Law

- Moore’s Law is not about scaling up, it’s about scaling down!
- We can currently put more transistors on a single chip than the market requires
- The key to Moore’s Law is the shrinking transistor
  - Faster
  - Smaller
  - Lighter
  - Lower Power
  - Cheaper

Why Does Moore's Law Work?

- Moore's Law is a classical learning curve:
  - Cost is reduced (typical values: by 20 - 30%) every time cumulative output doubles
- Our learning curve is no different than any other industry -- except we double output every year!
- Moore's Law is volume driven
  - Learning is driven by the cumulative area of silicon produced

Moore's Law as a Learning Curve



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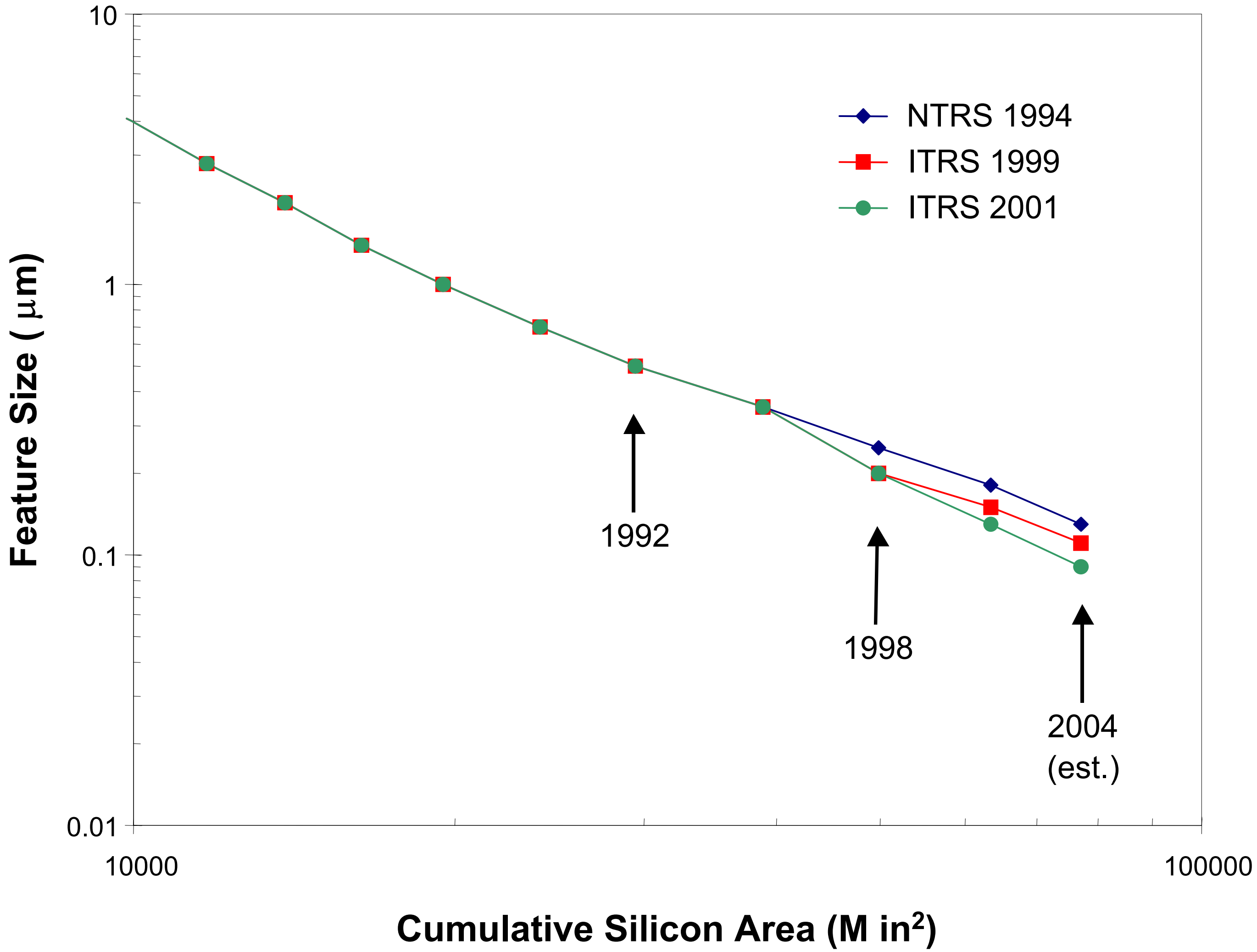
Moore's Law as a Learning Curve



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Why Does Moore's Law Work?

- Industry Drivers: Push vs. Pull
- Push Drivers (technology enablers):
  - Smaller feature sizes
  - Larger chip area
  - Improved designs
- Pull Drivers (volume enablers):
  - Lower cost per function (higher performance per cost)
  - New applications are enabled
  - Higher volumes are needed

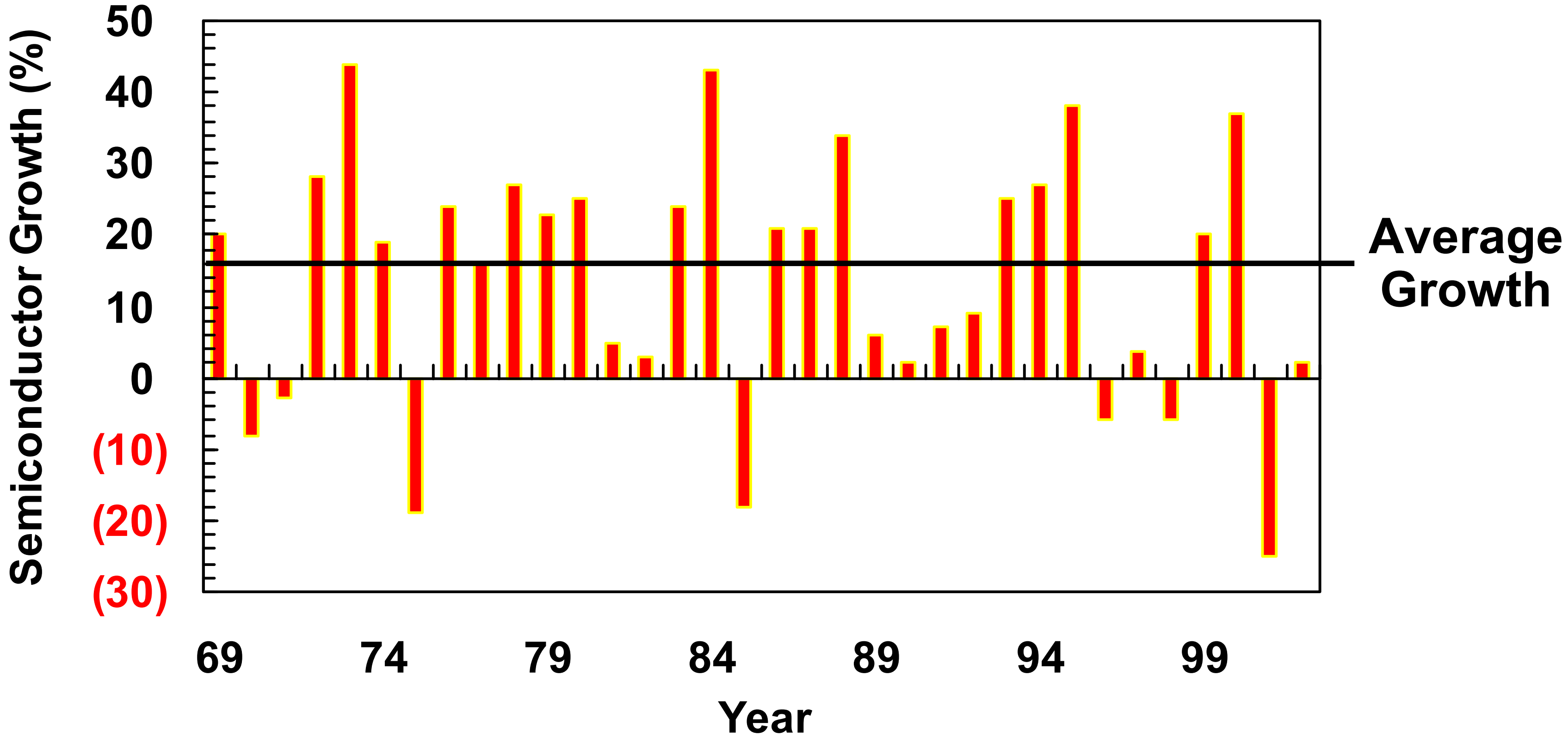
Macroeconomic View

As with all commercial technology, economics has driven and will continue to drive the direction of microlithography.

"…further miniaturization is less likely to be limited by the laws of physics than by the laws of economics."

Robert N. Noyce, 1977

Semiconductor Growth Cycle

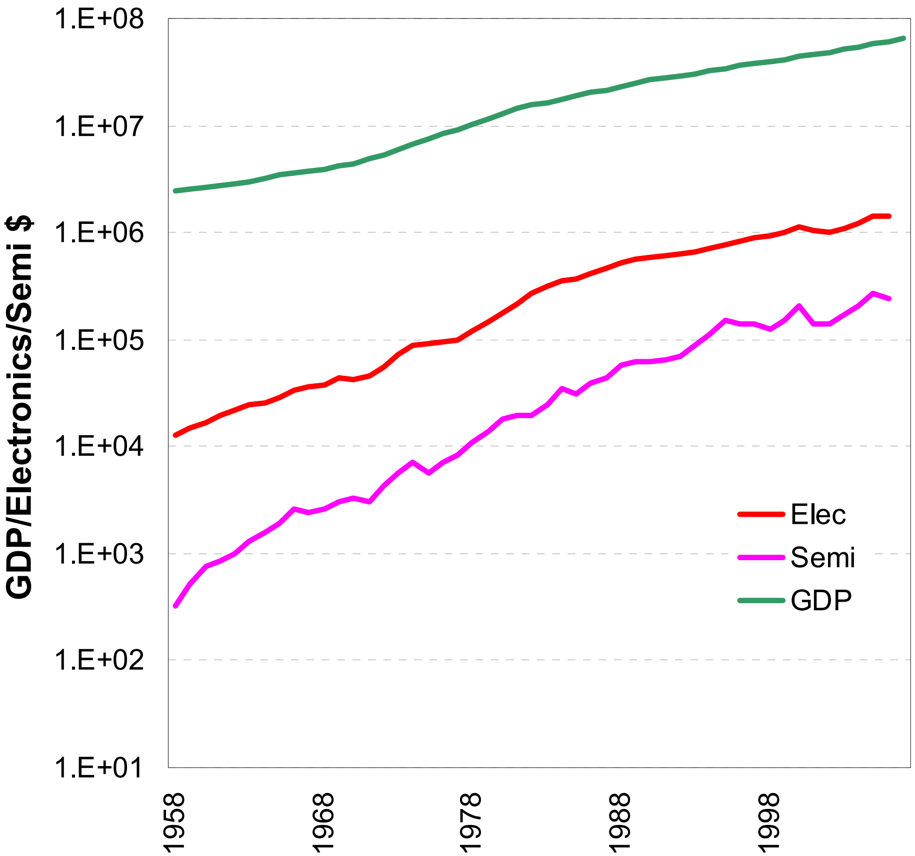


- Demand rise time: 3 - 6 months
- Production rise time: 2 - 3 years

Semiconductor Growth

Average Growth Rates (1961 – 2001)

- Semiconductors
  - 15%
- Electronics
  - 12%
- World GDP
  - 8%
- What drives this disparity?



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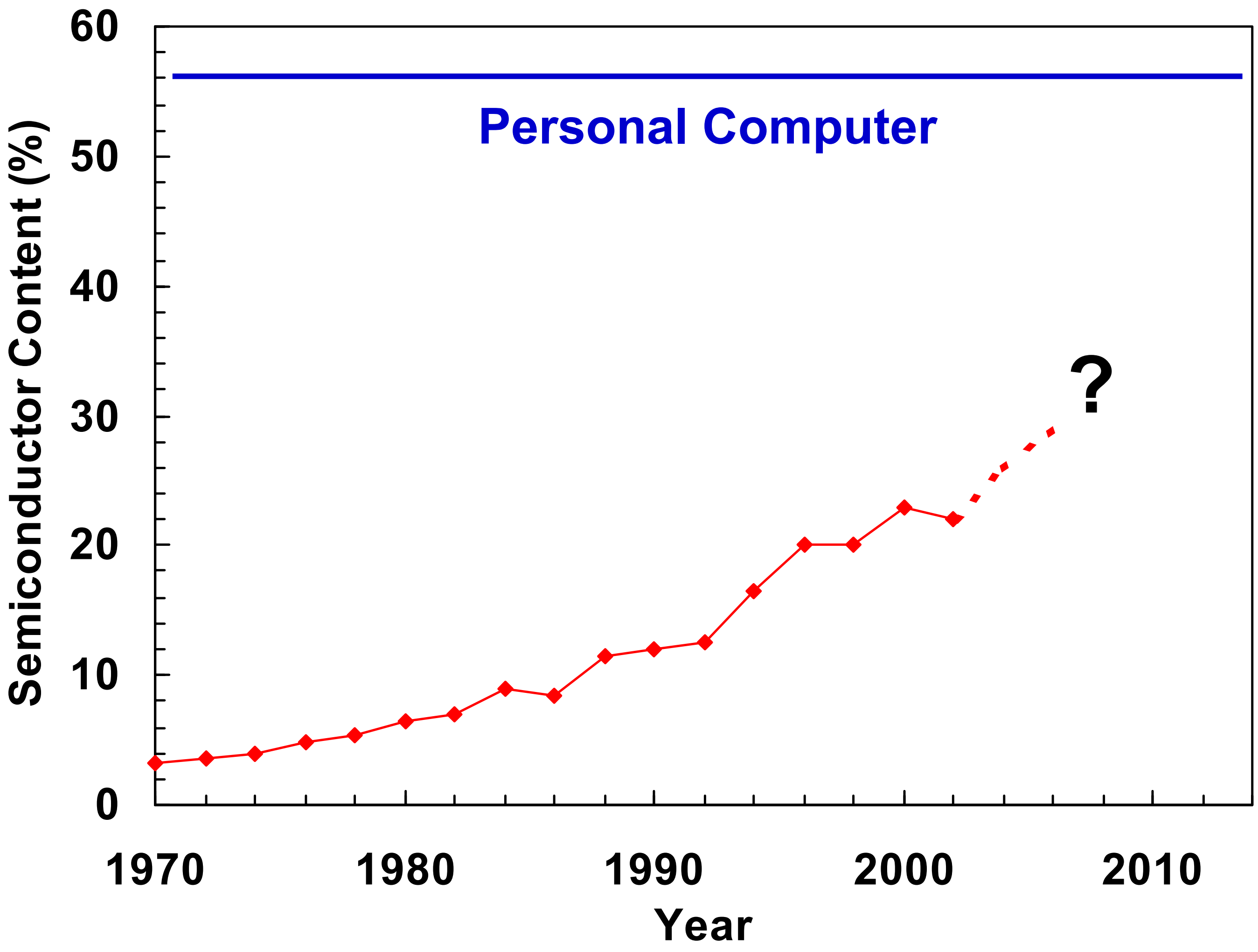
Semiconductor Content of Electronics



Source:

Semiconductor International

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Chip Costs

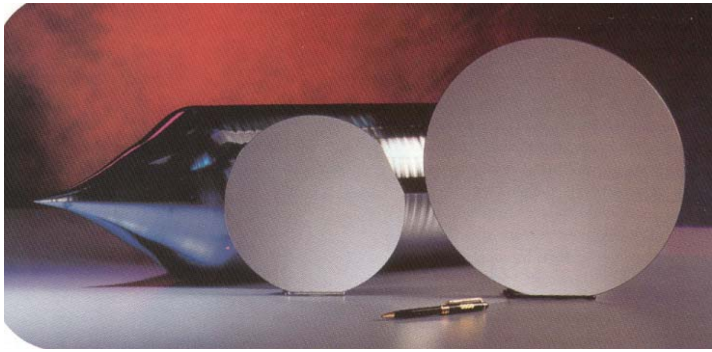
- Despite rising fab, equipment and material costs, and increasing process complexity, the cost/cm^2 of finished silicon has remained about constant over the years. How?

  - increasing wafer sizes
  - increasing yields
  - increasing equipment productivity

Wafer Size Trend

- Wafer size increases every seven to eight years:

Year*	Wafer Diameter
1969	3 inch
1976	4 inch
1984	5,6 inch
1989	8 inch (200mm)
2000	300mm



*first year of major production

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Chip Yield Trend

- 1970s
  - High volume yields of 20 – 40%
- 1980s
  - High volume yields of 40 – 60%
- 1990s
  - High volume yields of 70 – 90%
- 2000s
  - Yields must stay high, even as the technology gets more difficult
  - Ramp time to high yield must be reduced

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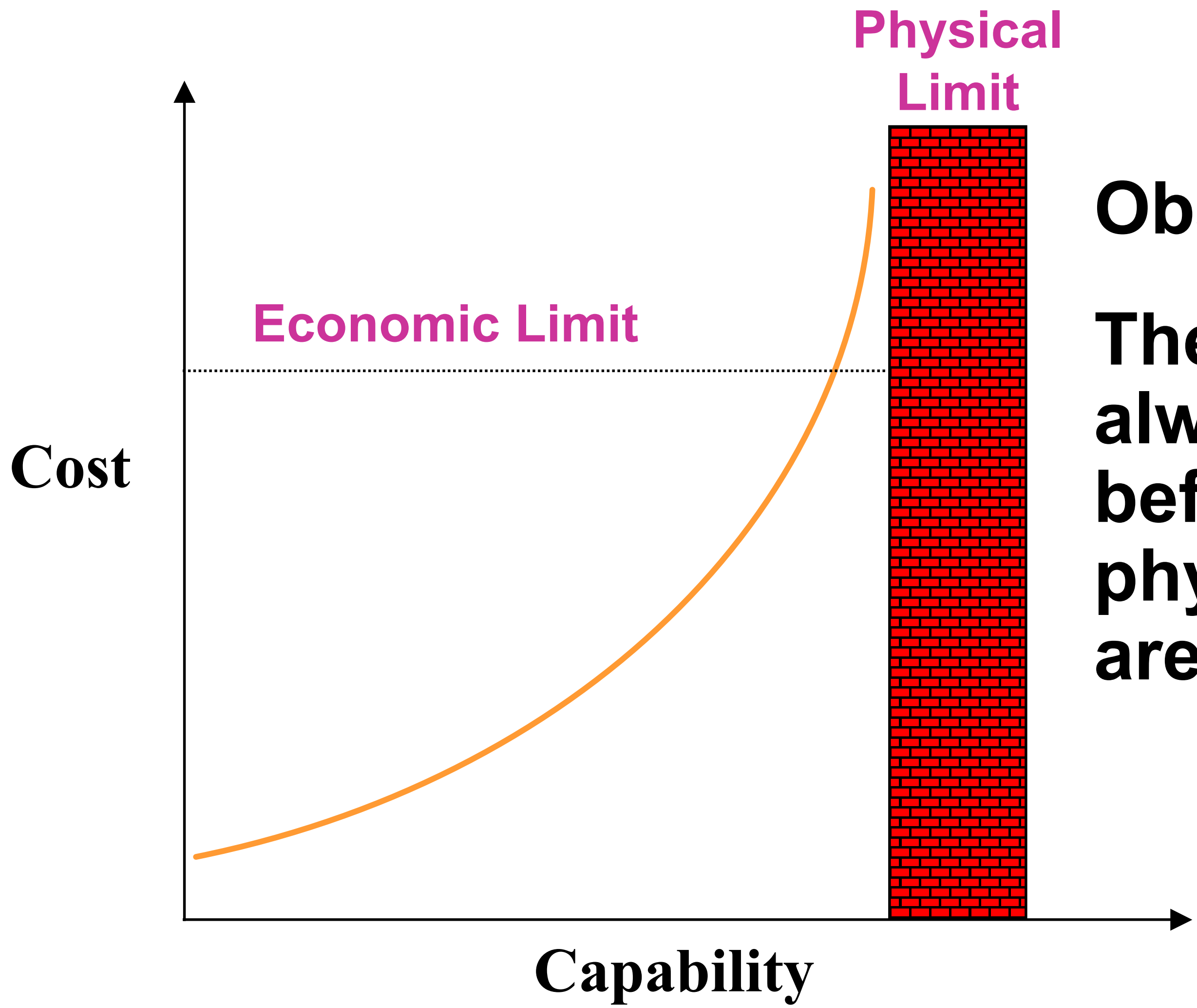
Chip Costs

- The trend to larger wafers is slowing
- Yield must quickly ramp to high yield
- Equipment productivity must keep improving
- Will the cost structure change as we approach the limits of optical lithography?
- Can NGL provide the same cost/cm^2?

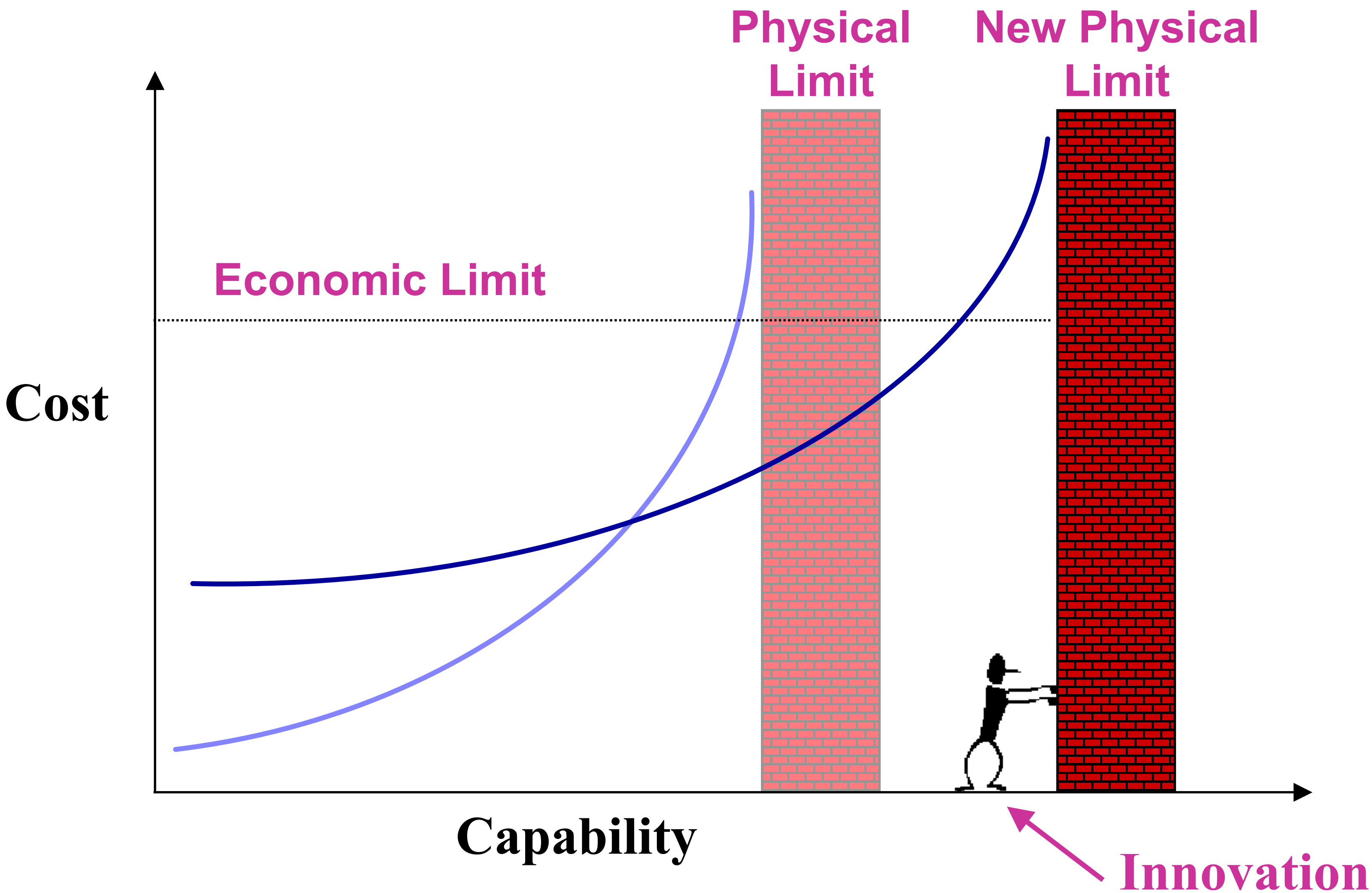
Technology vs. Economics



Observation:

The budget always runs out before the physical limits are reached.

Technology vs. Economics



Innovations in Optical Lithography

- Over the last 15 years numerous innovations have allowed optical lithography to push the limits:
  - Wavelength reduction: 248nm → 193nm → 157nm
  - Increasing numerical apertures
  - Resolution enhancement technologies
  - Improved resist performance
  - Reduced process variations
  - Advanced process control
- Are we done yet? **No.**

Innovations in Optical Lithography

- We have several more innovations in optical lithography yet to come:
  - Immersion lithography vs. 157nm
  - Real equipment productivity remains much less than theoretical
  - Process control will allow us to live with smaller process windows
  - The full advantages of phase shift masks have yet to be realized
  - Polarization control is needed
  - Lithography friendly designs must become the standard

Conclusions and Predictions

- Chip size increases have stopped, putting more pressure on feature size reduction
- 300mm is the largest wafer size, putting more pressure on equipment productivity to keep manufacturing costs down
- Chip designs will become lithography aware to maximize the "yieldable" transistor density
- It is essential that yields achieve the high historical levels for each new technology node
  - Process control will no longer be an option

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Conclusions (cont'd)

- Moore's Law is a volume driven learning curve
  - Volume drives the progress, not time
- Innovations are required to push the economic limits by pushing the technical limits (keep pushing)
- New applications for chips must keep the volume growing (keep pulling)

Acknowledgements

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- Rick Wallace (for stealing the r
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- KLA-Tencor