Lithography in the New Millennium

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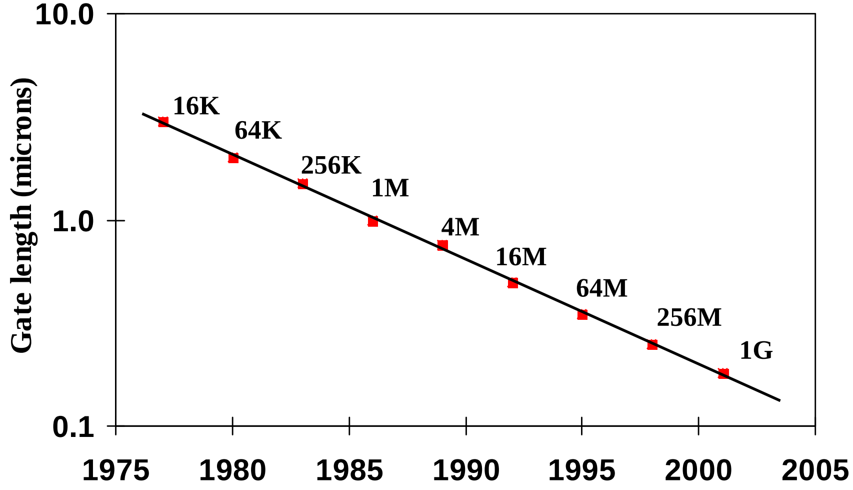
Outline

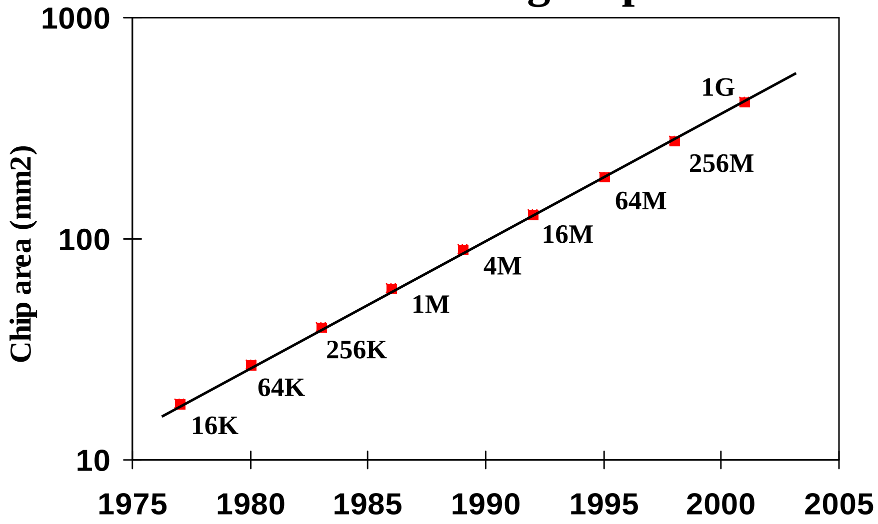
- Moore’s Law
    - Past, Present, and Future
- Drivers for Lithography
    - Push vs. Pull
- Semiconductor Industry Economics
- Future Directions

Moore’s Law

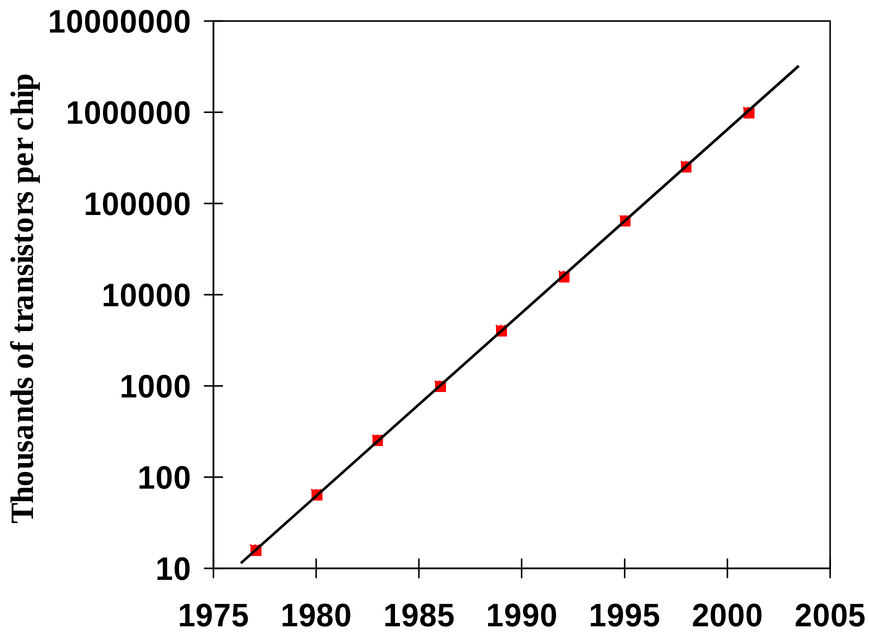
Decreasing transistor size...



...and increasing chip size...

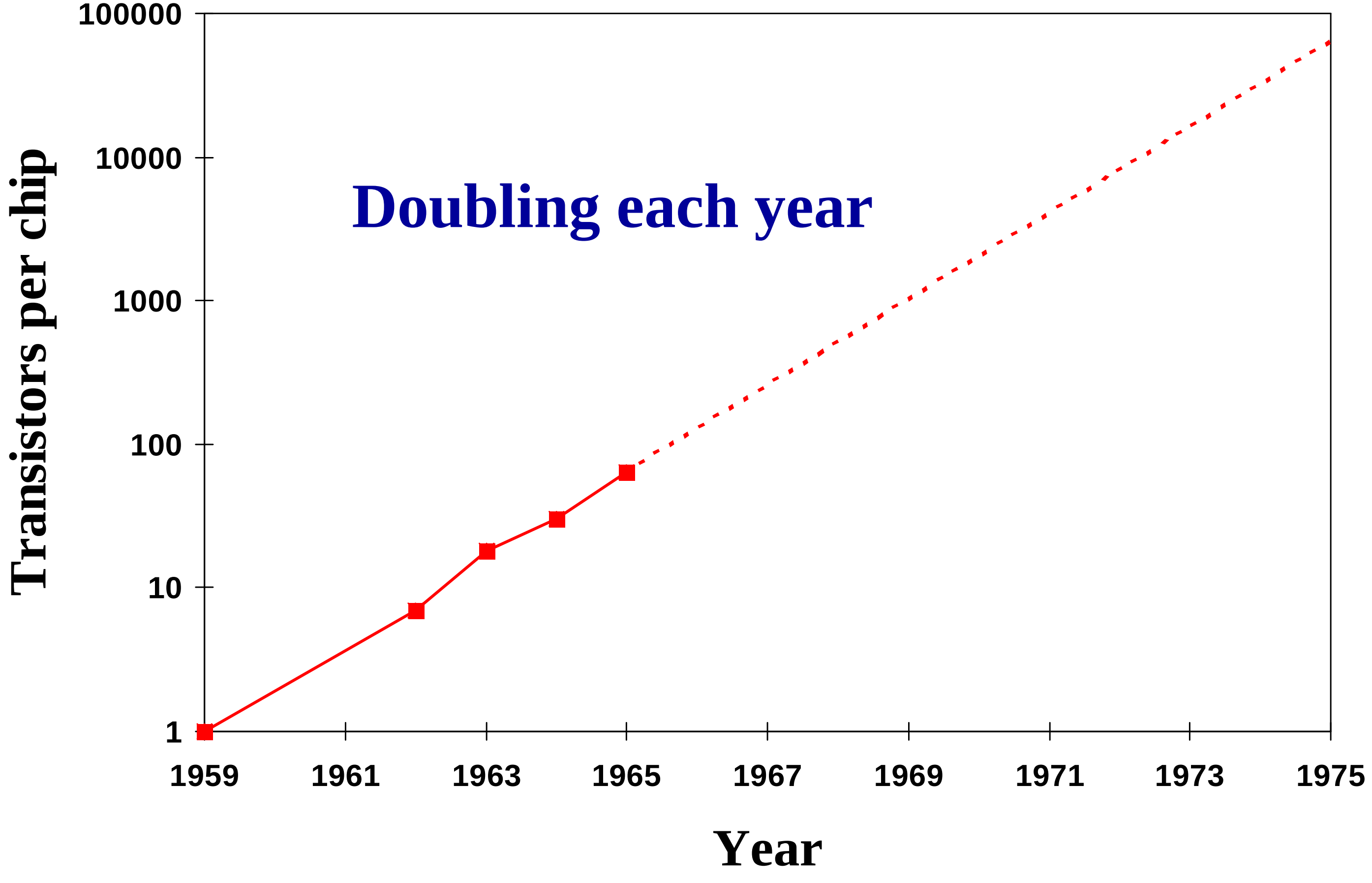


...are resulting in rapid growth in the number of transistors per chip



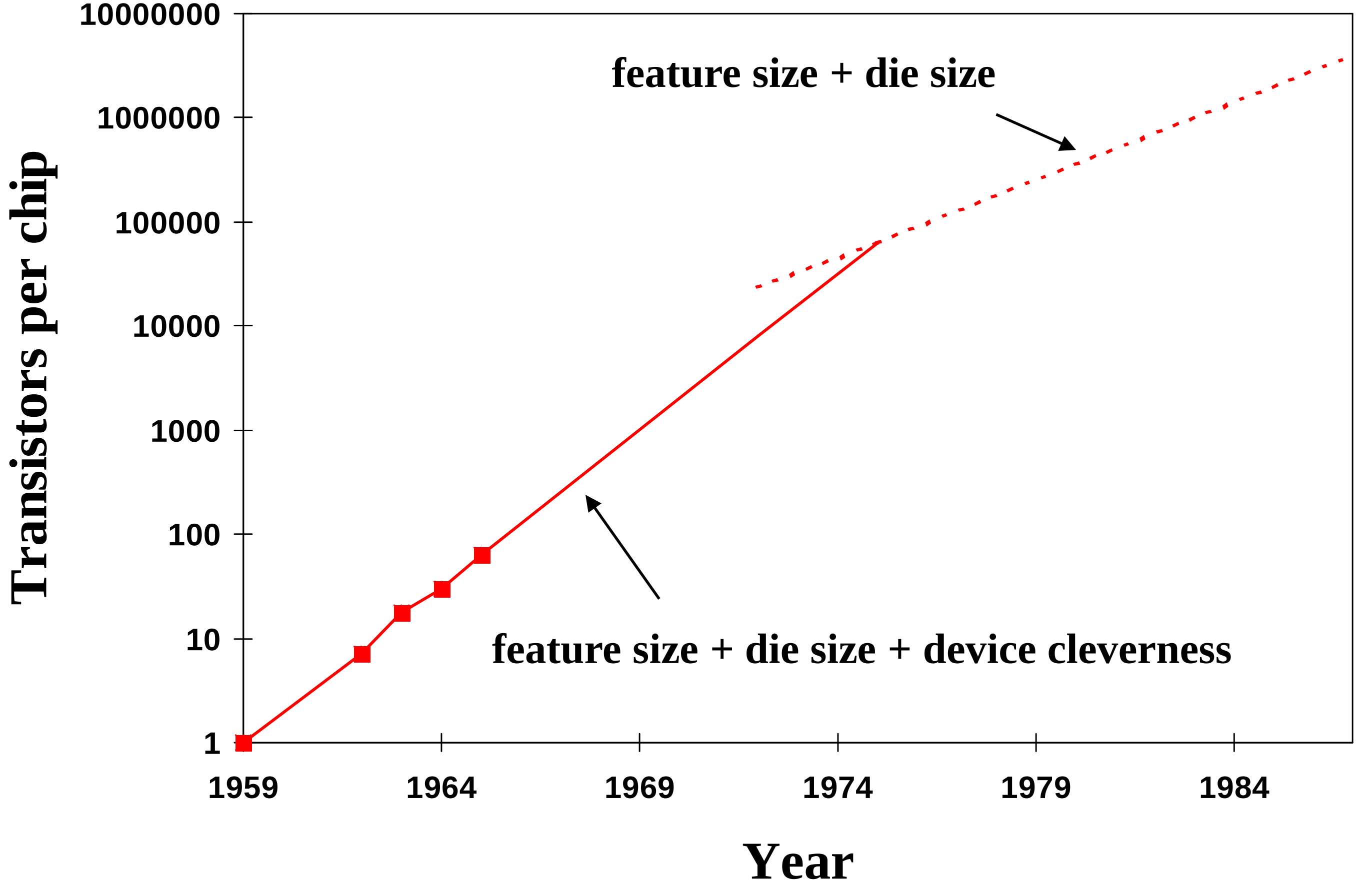
Moore's Law

- **1965: Moore's Observation**



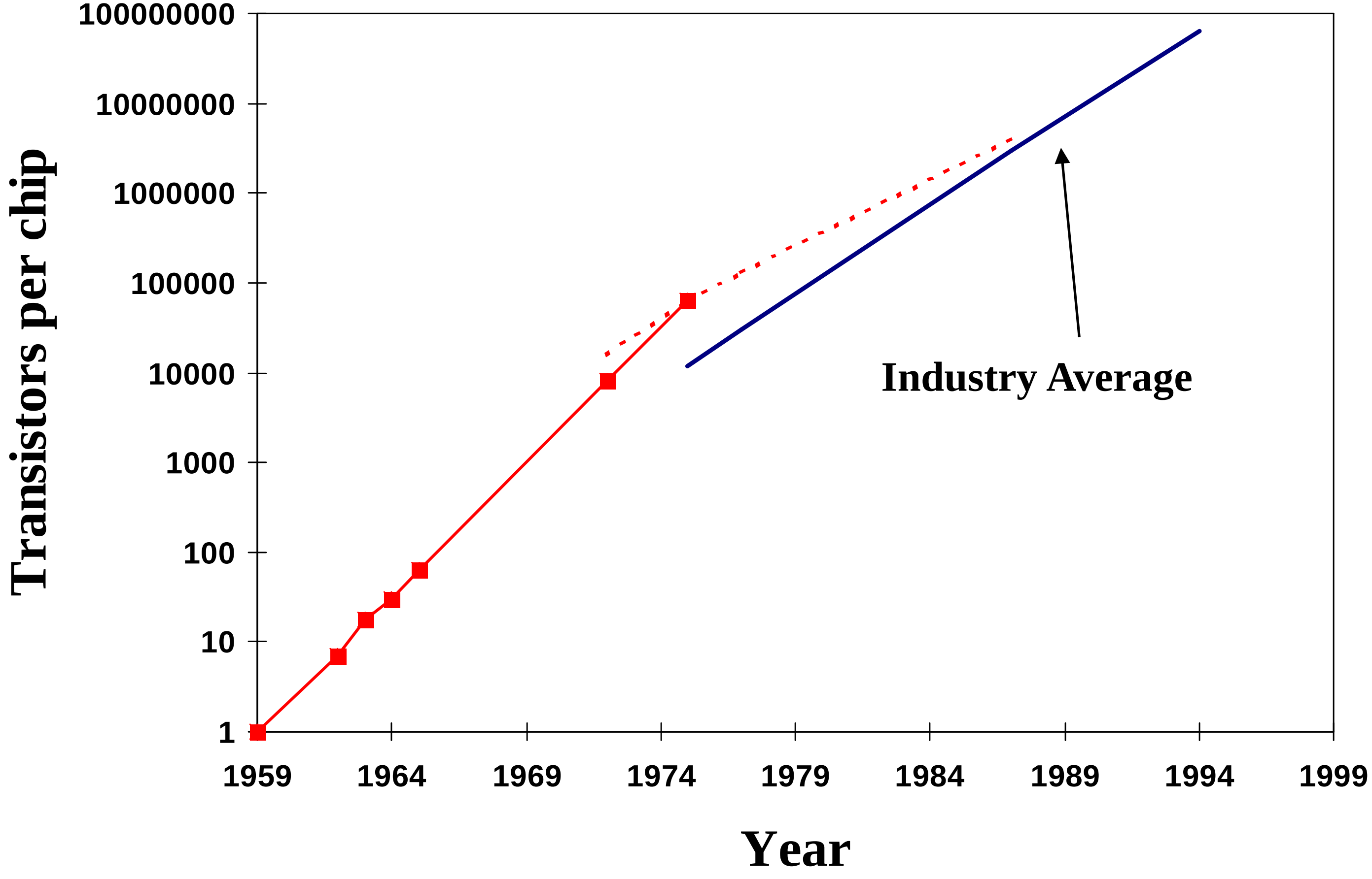
Moore's Law

- **1975: Moore's Next Observation**



Moore’s Law

- **1980s: Moore’s Law**



Moore's Law

- **1990s: Moore's Self-Fulfilling Prophecy**
  - **1994 National Technology Roadmap for Semiconductors**
    - » **Moore's Law is now the industry's law**
    - » **No one can afford to fall behind**
  - **1997 National Technology Roadmap**
    - » **Moore's Law is accelerated**
    - » **We have to beat the law to stay competitive**
  - **1999 Roadmap: More Acceleration?**

Moore's Law

- **2000: Moore's Technomantra**
  - **Build it and they will come**
  - **Rapid change, thought to be inherently unstable, is somehow both stable and predictable**
- **What are the implications of blind faith in Moore's Law?**
- **Our Fear:**
  - **Exponential growth is just the first half of an "S" shaped curve**

Moore’s Law

- **1995: Mack’s Roadmap to Retirement - Life in the Year 2025**

Memory Chip:	**64 Tb**
Feature Size:	**10 nm**
CD control:	**± 1 nm (± half resist molecule)**
Chip Area:	**3” X 6”**
Wafer Size:	**32”**
Chip Price:	**$1000**
Fab Cost:	**$1 Trillion**

Moore's Law

- **1999: Mack's Roadmap to the Roadmaps**

1994 Roadmap:	**100 nm production in 2007**
1997 Roadmap:	**100 nm production in 2006**
1999 Roadmap:	**100 nm production in 2005**
Roadmap Proposal:	**100 nm production in 2003**

- **Trend Analysis: By the 2001 Roadmap, we'll have finished the 100 nm node before we even start it!**

Moore’s Law

- **Moore’s Law is a classical learning curve:**
  - **cost is reduced by 20 - 30% every time cumulative output doubles**
- **Our learning curve is no different than any other industry -- except we double output every year!**
- **Moore’s Law is volume driven**

Moore's Law

- **Industry Drivers: Push vs. Pull**
- **Push:**
  - **Smaller feature sizes**
  - **Larger chip area**
  - **Improved designs**
- **Pull:**
  - **Lower cost per function (higher performance per cost)**
  - **New applications are enabled**
  - **Higher volumes**

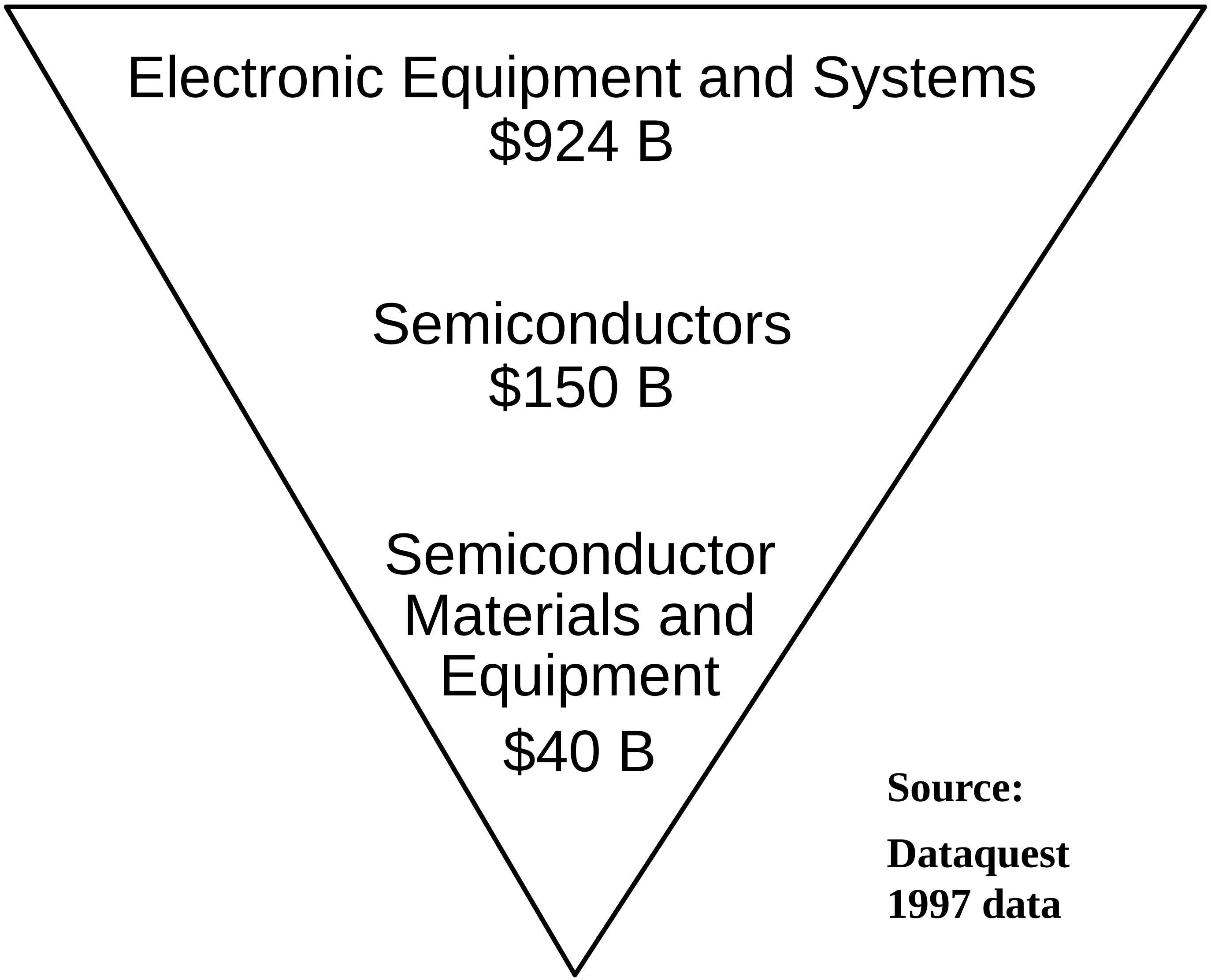
Lithography and the World Economy

As with almost all commercial technology, economics has driven and will continue to drive the direction of microlithography.

"…further miniaturization is less likely to be limited by the laws of physics than by the laws of economics."

Robert N. Noyce, 1977

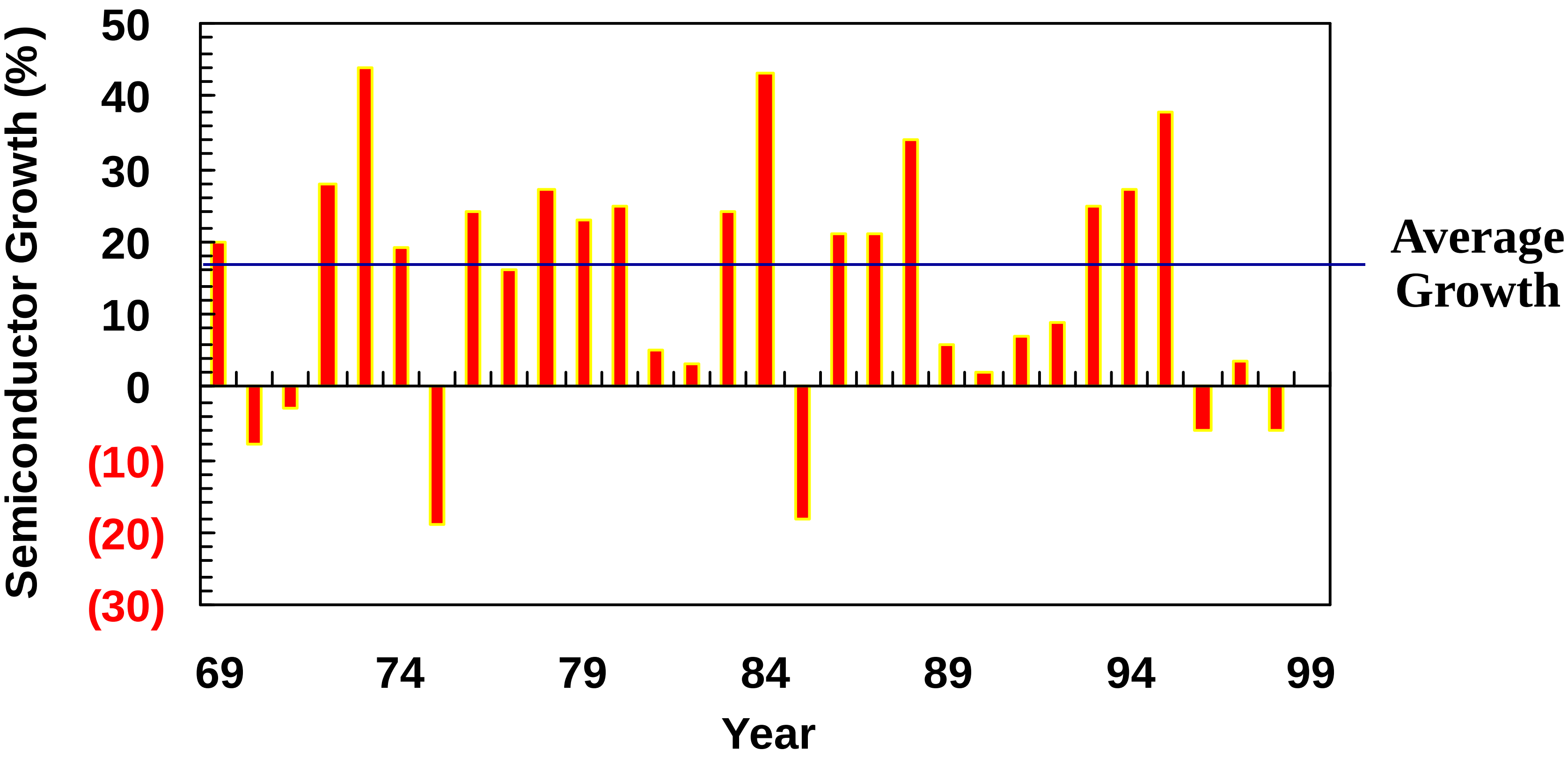
The Electronics “Food Chain”



Source:

Dataquest
1997 data

Semiconductor Growth Cycle



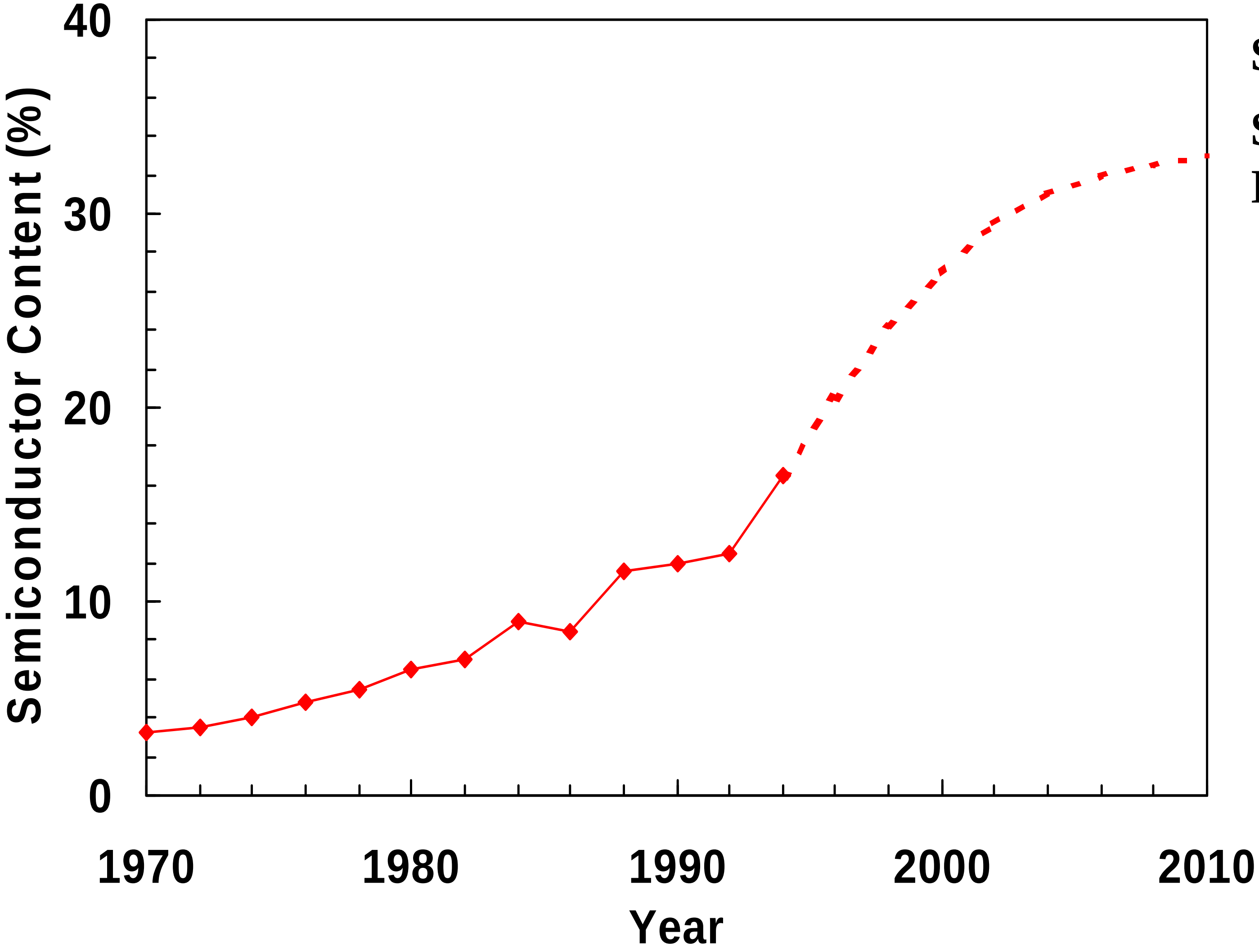
- **Demand rise time: 3 - 6 months**
- **Production rise time: 2 - 3 years**

Semiconductor Growth

- **Average Semiconductor Growth Rate:**
  - **18%**
- **Average Electronics Growth Rate**
  - **9%**

- **How long will this disparity last?**

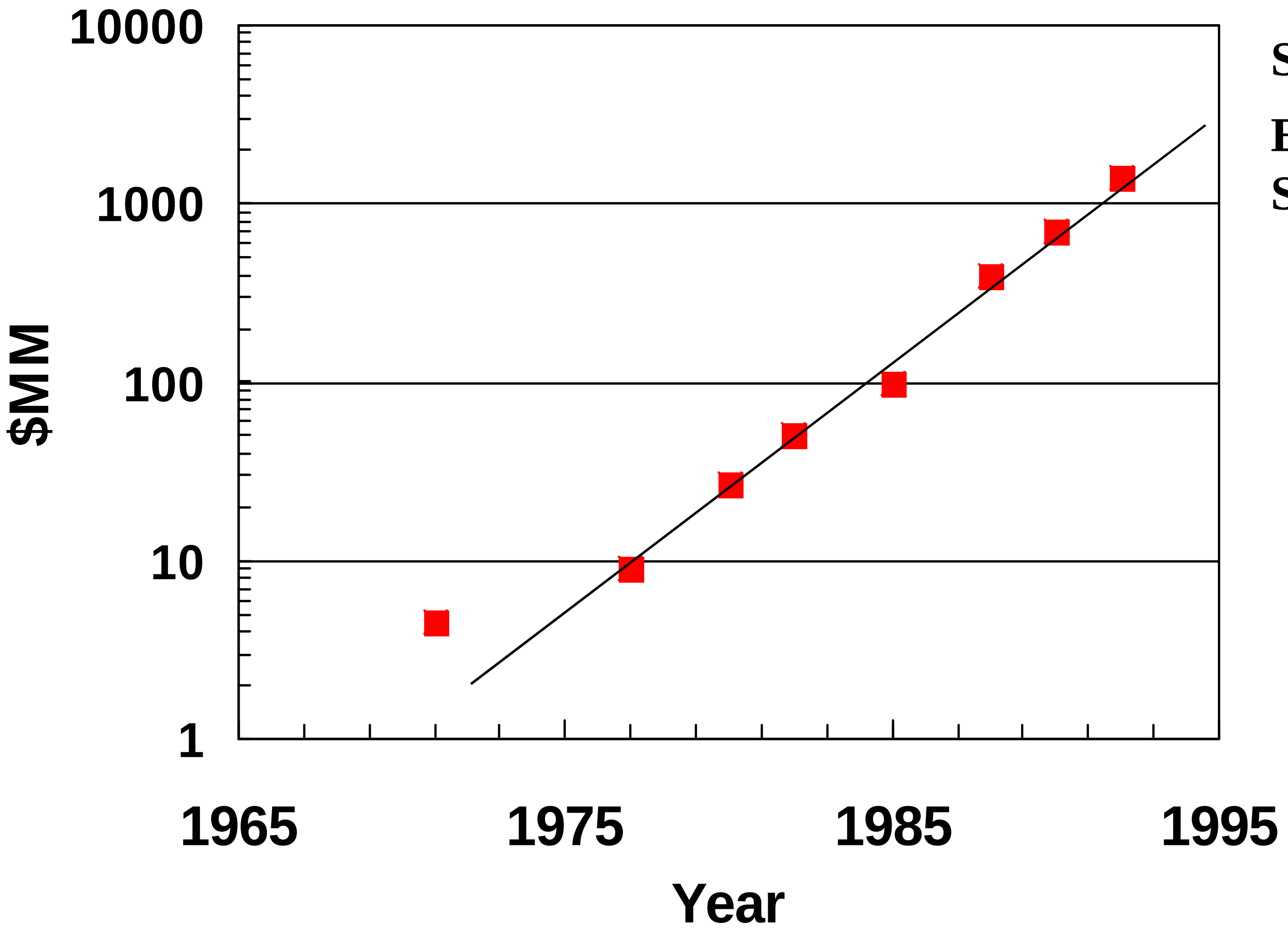
Semiconductor Content of Electronics



Source:

Semiconductor International

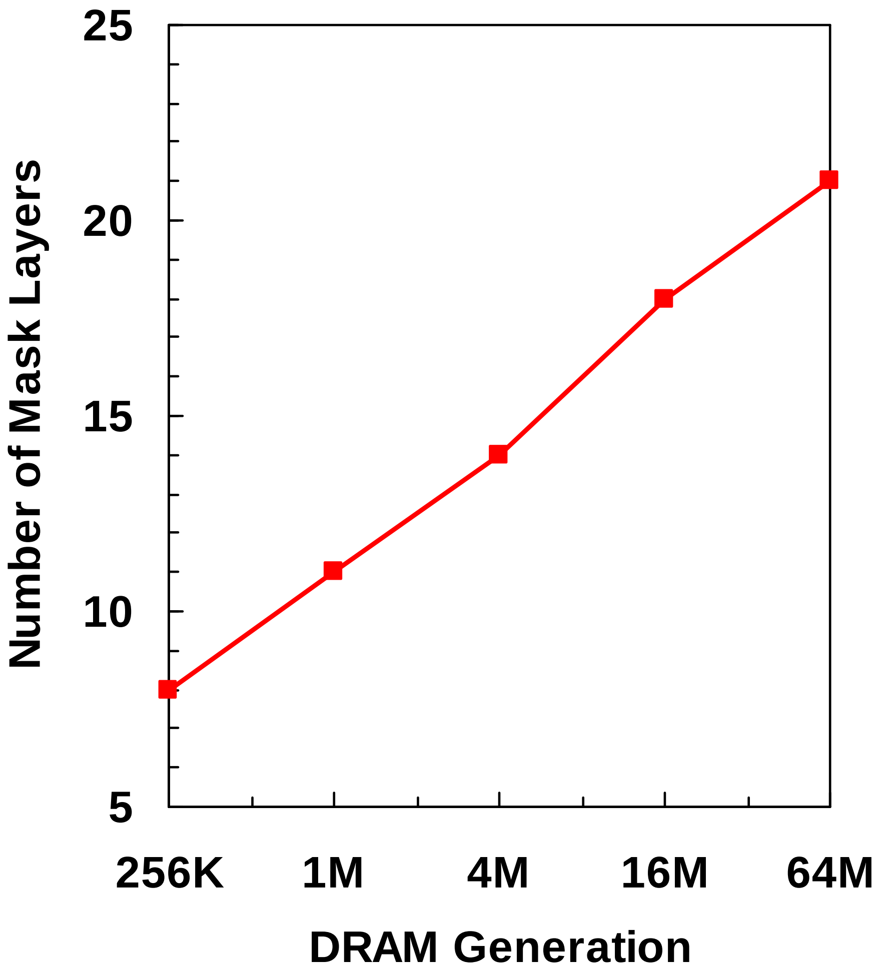
Growing Costs of Wafer Fabs

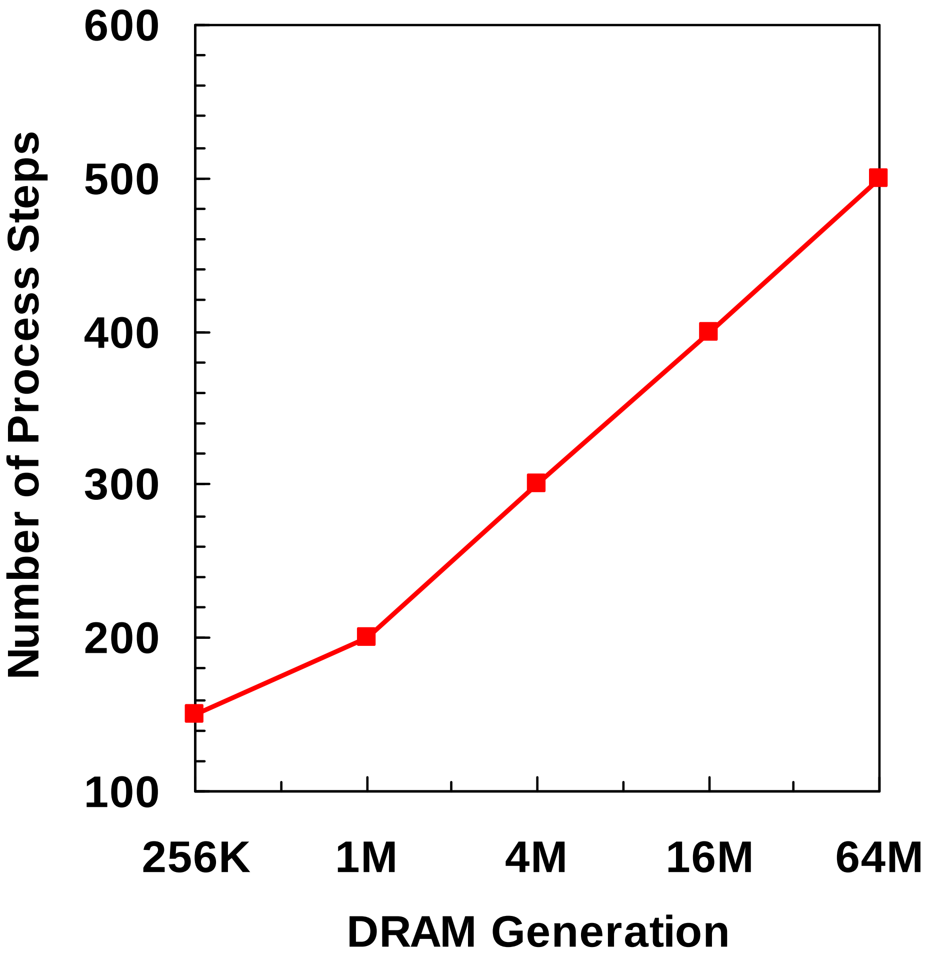


Source:

Electronic News Sept, 1993

Process Complexity Trends





Device Complexity Trends

Device	Year	Transistors per Chip	Chip Area (cm^2)
8086	1978	30K	0.34
80286	1981	120K	0.77
80386	1985	400K	1.0
486	1990	2M	1.8
Pentium	1993	3.5M	2.9
Pentium Pro	1995	5.5M	2.9

Annual Lithography Costs (1998)

Steppers	$3300 M
Tracks	$1600 M
Photoresist	$850 M
Masks	$2000 M
Metrology	$500 M
Total	$8250 M

- Stepper costs double every 5 years
- Mask costs are rising dramatically

Chip Costs

- **Despite rising fab, equipment and material costs, and increasing process complexity, the cost/cm^2 of finished silicon has remained about constant over the years. How?**
  - **increasing wafer sizes**
  - **increasing yields**
  - **increasing throughput (equipment productivity)**

Wafer Size Trend

- **Wafer size increases every seven to eight years:**

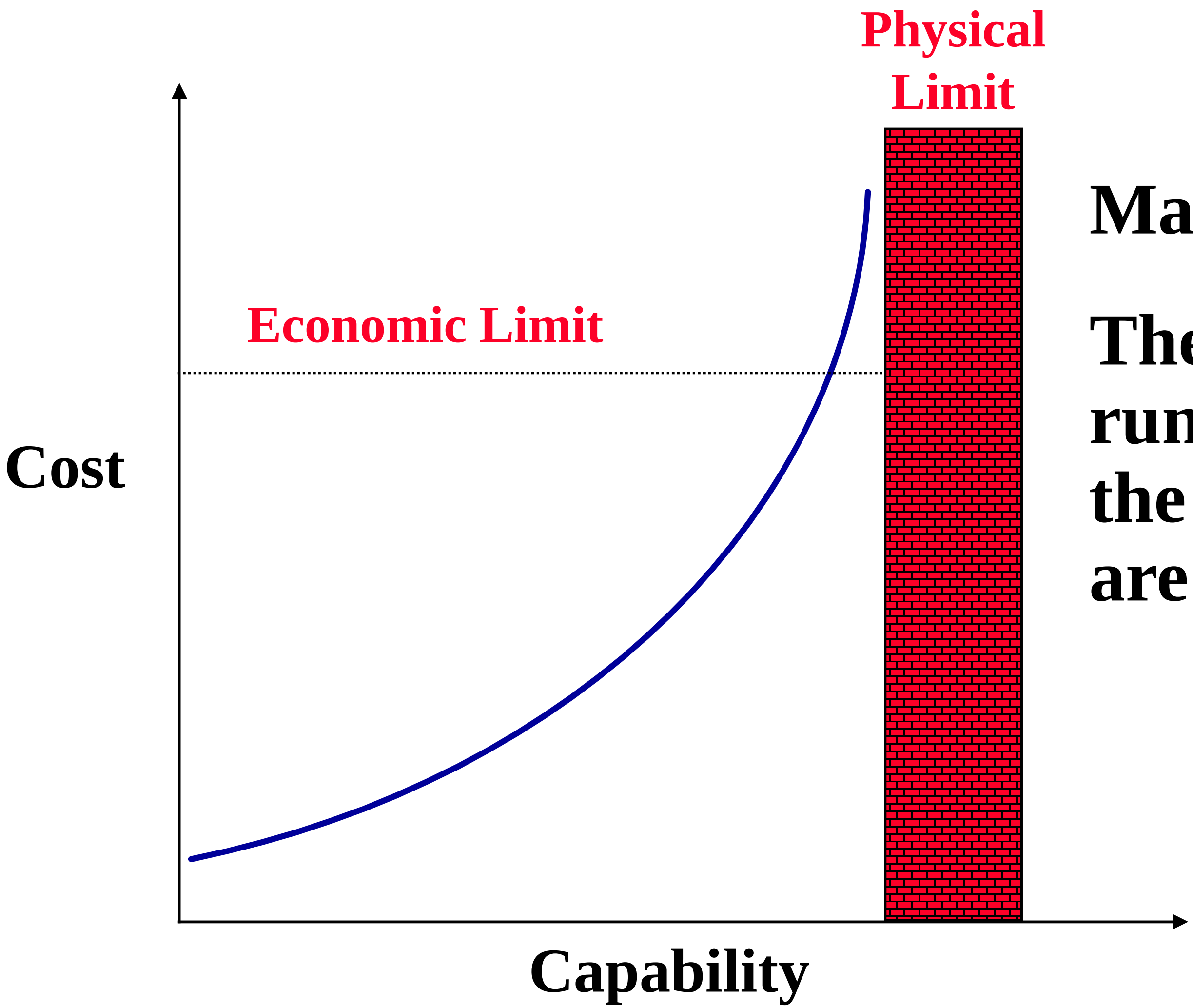
Year*	**Wafer Diameter**
1969	**3 inch**
1976	**4 inch**
1984	**5,6 inch**
1989	**8 inch**
2000?	**12 inch**

***(first year of major production)**

Chip Costs

- The trend to larger wafers may be slowing
- There is no more room for yield improvements
- Can equipment productivity alone keep on the same cost curve?
- How will the cost structure change as we approach the limits of optical lithography?

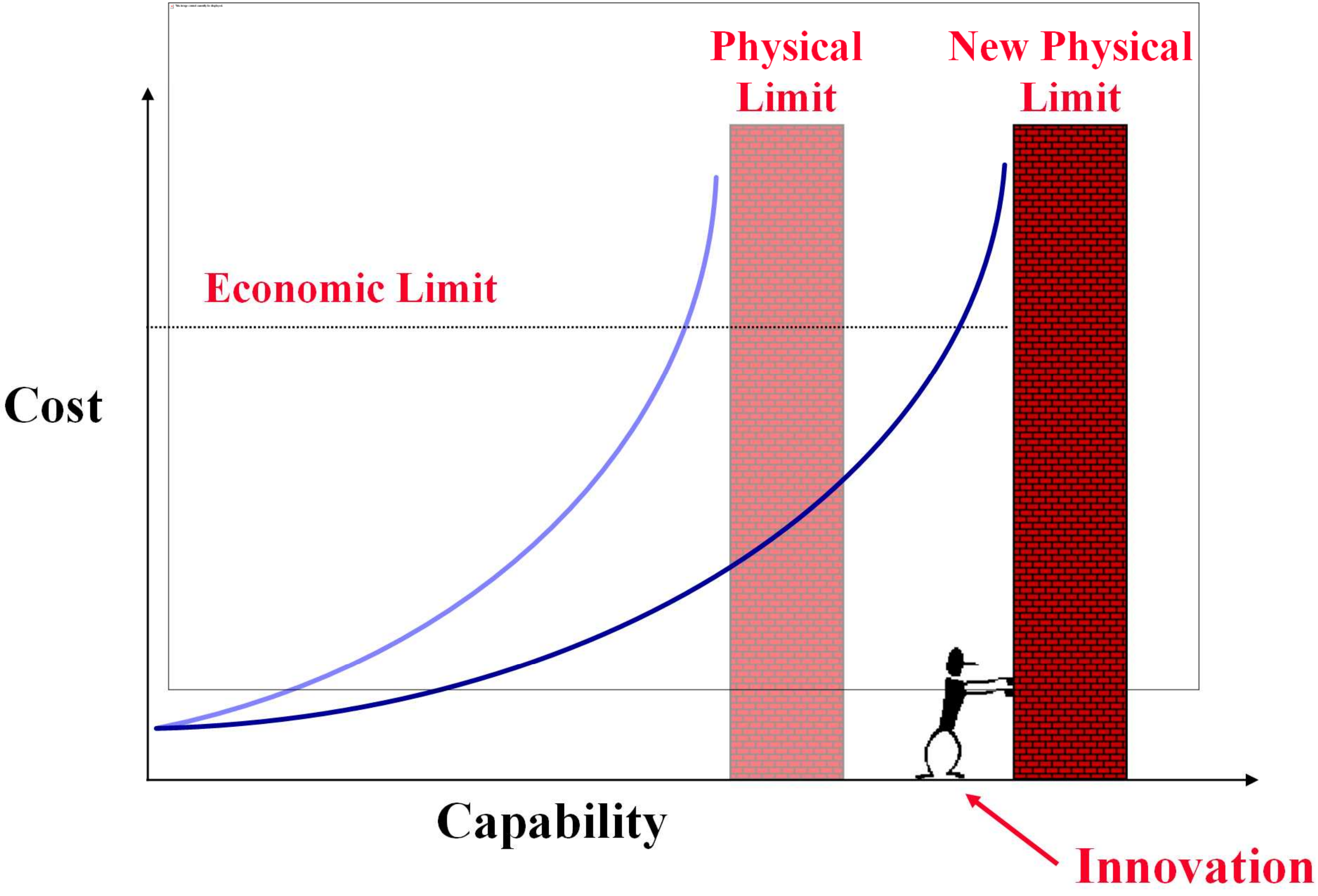
Technology vs. Economics



Mack's Law:

The budget always runs out before the physical limits are reached.

Technology vs. Economics



Future Directions

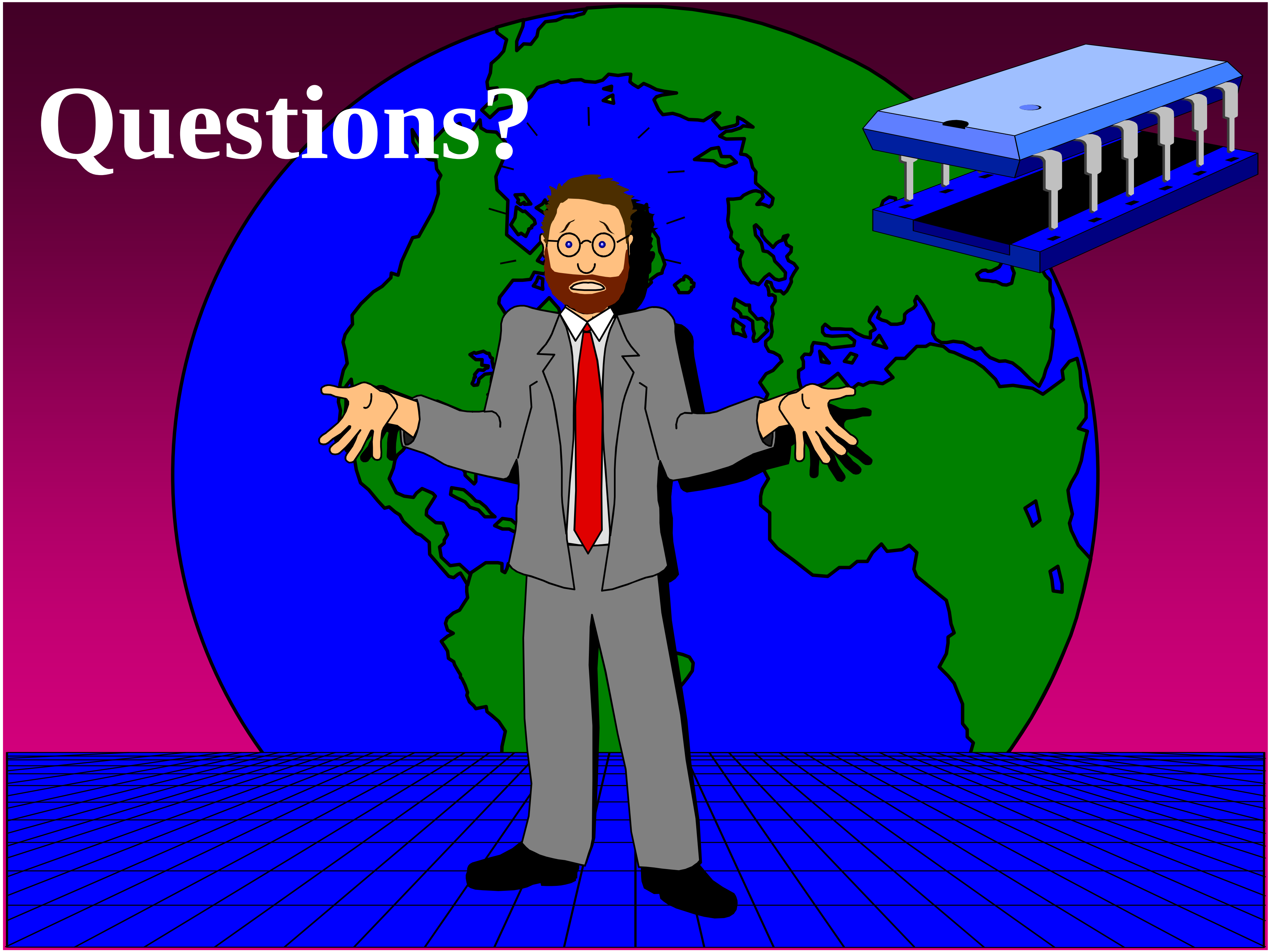
- Cost/cm^2 drives lithographic technology
- Innovation is essential to keeping cost low while improving capability
- Optical lithography is the only technology that has proven itself low cost
- We have several more innovations in optical lithography yet to come

Conclusions

- Moore's Law is dynamic, ever changing
- Chip size trends are slowing, putting more pressure on feature size reduction (push)
- Flat yields and slowing wafer size trends put more pressure on equipment productivity
- If cost/cm^2 goes up, what happens to demand (pull)?
- As semiconductors saturate electronics, semi growth will drop in half

Conclusions (cont'd)

- **Innovations are required to push the economic limits by pushing the technical limits**
- **The convergence of less push and less pull will happen by 2010. Are we ready?**


Questions?