CHE323/CHE384
Chemical Processes for Micro- and Nanofabrication
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Lecture 59 Lithography: Double Patterning

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Hitting the Resolution Limit

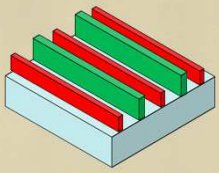
- Wavelength is stuck at 193 nm, the highest NA we have is 1.35, and k_1 is limited to 0.25

$$R = k_1 \frac{\lambda}{NA} \geq 0.25 \frac{193nm}{1.35} = 36nm$$

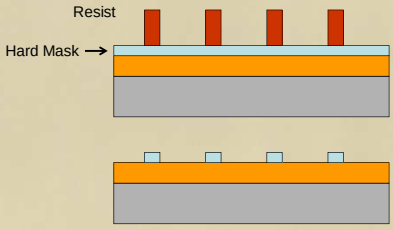
- This resolution limit is technically the smallest "half pitch" that can be printed
  - Practical half-pitch limit is more like 38 – 40 nm
  - Minimum pitch is therefore 75 – 80 nm

Breaking the Resolution Limit

- We can break this resolution limit using double patterning
  - Print twice, several styles are available
  - New limit is about a 40-nm pitch (k_1 = 0.14 or so)



Litho-Etch-Litho-Etch (LELE)



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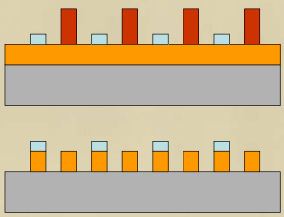
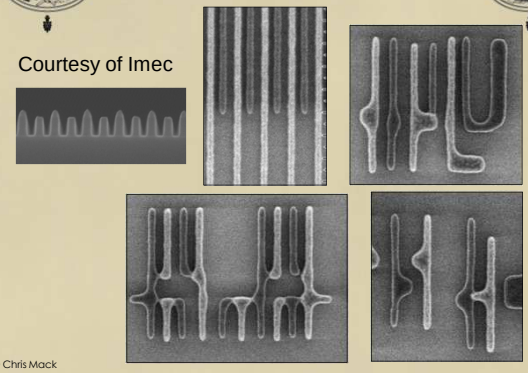


Double Patterning

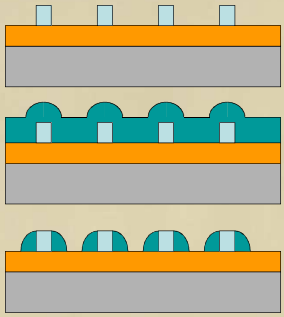
Courtesy of Imec



LELE Problems

- Cost – the cost of LELE is essentially double that of single patterning
- Overlay – overlay errors between the two patterns translates into CD errors (errors in gap width)
  - Requires much tighter overlay control than single patterning
- Pattern decomposition – not every pattern is easily decomposed into two separate patterns (especially random logic)

Self-Aligned Double Patterning (SADP)

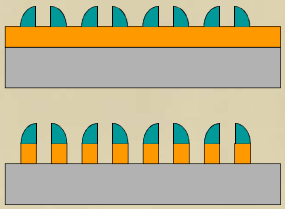


Litho1 + Etch1 (dummy patterns)

Grow Sidewalls (aka spacers)

Etchback

Self-Aligned Double Patterning (SADP)



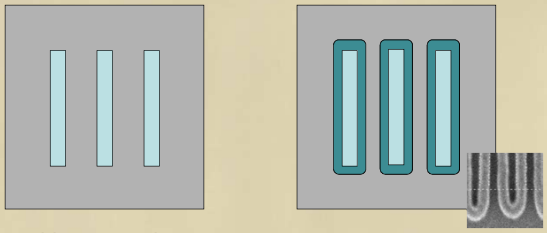
Strip Dummy Pattern

Etch 2

Self-Aligned Double Patterning (SADP)

From Applied Materials

SADP – top down view



Litho1 + Etch1

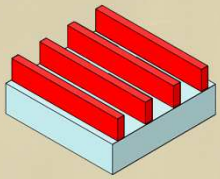
Sidewalls form Loops

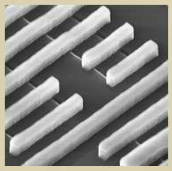
SADP Problems

- Cost – This is cheapest of the double patterning approaches: only one critical lithography step
- Overlay – Not much different from single patterning requirements
- Design – every feature must have the same linewidth (restricted design rules)
- Trim Steps – one or two trim patterning steps are required
- Currently in widespread use, especially Flash

Complimentary Lithography

- Use dipole illumination or alternating PSM to form dense lines/spaces (or SADP for smaller pitch)
- Use second litho-etch step to trim ends of lines and to cut patterns into the lines





Intel 32-nm node (source: Intel)

Lecture 59: What have we Learned?

- What is the current resolution limit of single patterning?
- Name three double-patterning approaches
- What are the main advantages and disadvantages of each double patterning approach?
- Essay question: do you think there is a future for quadruple patterning? Why or why not?