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CHE323/CHE384
Chemical Processes for Micro- and Nanofabrication
www.lithoguru.com/scientist/CHE323

Lecture 31
Copper Dual Damascene

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Reading:
Section 11.2, *Fabrication Engineering at the Micro- and Nanoscale*, 4th edition, Campbell

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The Switch to Copper

- As interconnect become a limiter to chip performance in the 1990s, aluminum was replaced by copper
- Problem: Copper is a fast-diffusing deep-level defect in silicon (a real killer)
  - Solution: Use tungsten as first metal, then apply TiN or Ta barrier layer, then copper after that
- Problem: Copper cannot be easily etched in plasma
  - Solution: Dual Damascene process

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Copper as Contaminant

- Copper must be kept away from the active region of the transistor
  - Tungsten plug makes contact with silicide formed on source/drain

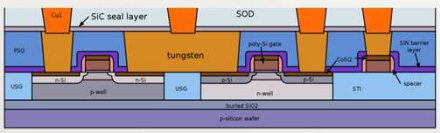

Image from Wikimedia Commons

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Copper Dual Damascene

- Plasma etching doesn't work for copper
  - Reaction products are not volatile
  - Subtractive patterning doesn't work
- Instead, use an additive patterning step
- Damascene process – named for the decorative inlay metal process made famous in Damascus

From http://www.caravanacollection.com

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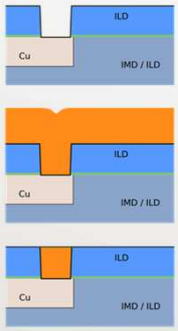
Damascene Process



1. Pattern contact hole in interlayer dielectric (ILD) (IMD = inter metal dielectric)
2. Deposit metal (filling hole)
3. CMP metal, creating plug

(Image from Wikimedia Commons)

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Dual Damascene Process (Via First)

(Image from Wikimedia Commons)

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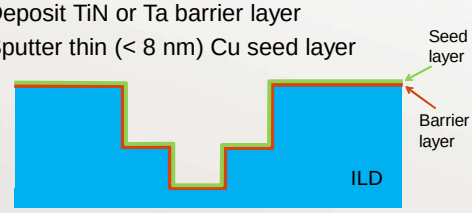
Copper Deposition

- Copper must be deposited via electroplating
  - Deposit TiN or Ta barrier layer
  - Sputter thin (< 8 nm) Cu seed layer



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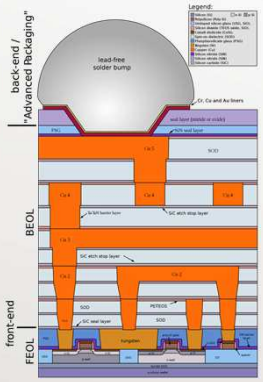

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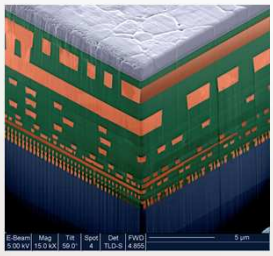

Source: IBM, 2005

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Lecture 31: What have we learned?

- Why must an additive process be used to pattern copper versus the more common subtractive process?
- What are the steps involved in copper deposition?
- Where does the term "damascene" come from?
- Why must copper be kept away from the silicon device?

