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Chemical Processes for Micro- and Nanofabrication
www.lithoguru.com/scientist/CHE323

Lecture 29
Device Interconnect, part 2

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Reading:
Chapter 15, *Fabrication Engineering at the Micro- and Nanoscale*, 4th edition, Campbell

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Interconnect Delay

- The speed of a chip is a function of how fast transistors can be switched on and off, and how fast signals can propagate along the wires connecting them
- Dennard scaling
  - Transistor switching time decreased regularly till the early 2000s
  - Interconnect delay time *increased* during this time, since the length of interconnect wires has remained roughly constant
- Result: Interconnect delay is now equally or more important in determining chip speed as transistor delay

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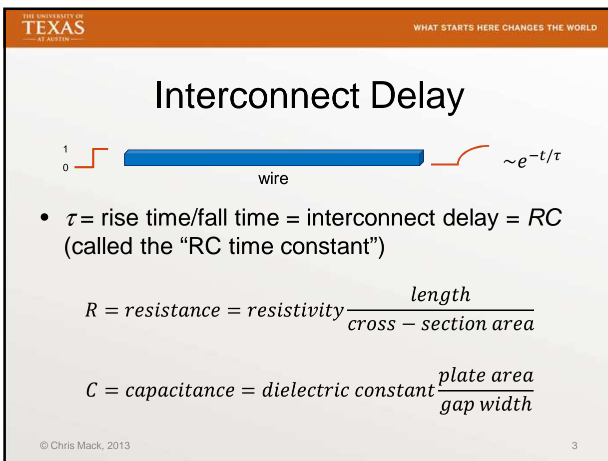

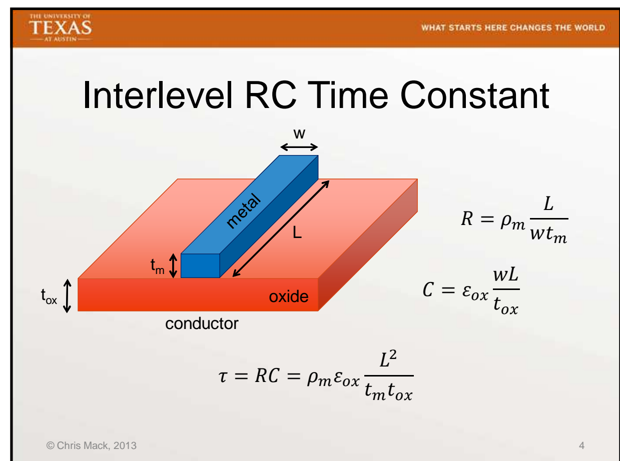

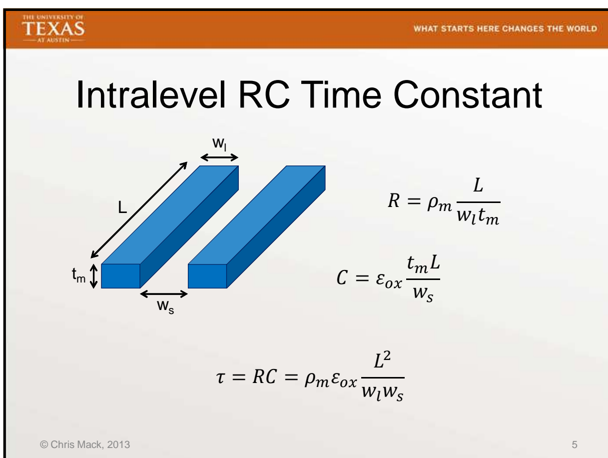

How Can τ Be Reduced?

$$\tau = \rho_m \varepsilon_{ox} \frac{L^2}{w_l w_s}$$

$$\tau = \rho_m \varepsilon_{ox} \frac{L^2}{t_m t_{ox}}$$

1. Reduce metal resistivity
   - ρ_{AL} = 2.8 X 10^{-6} Ω cm
   - ρ_{Cu} = 1.7 X 10^{-6} Ω cm
2. Reduce insulator dielectric constant
   - $\varepsilon_{ox} = K_{ox} \varepsilon_o$, for SiO_2 K_{ox} = 3.9
   - For "low-K" dielectrics, we want K_{ox} ≈ 2 – 2.5
   - Use polymers, fluorinated oxides, porous oxides: this is very hard to do!

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How Can τ Be Reduced?

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$$\tau = \rho_m \varepsilon_{ox} \frac{L^2}{t_m t_{ox}}$$

3. Make t_m, t_{ox} thicker
   - Results in greater topography
   - Limited by metal line aspect ratio
4. Make metal pitch (= $w_l + w_s$) bigger
   - Requires more metal levels
5. Reduce L by using pass transistors
   - Do this when interconnect delay > 2*transistor delay

L
A B

L/2 L/2
A B
Pass transistor

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Interconnect Delay

- We've switched from aluminum to copper, but from here things get exotic (carbon nanotubes, etc.)
- Low-K dielectrics are hard to make and use
  - Low-K usually results in low mechanical strength
- There is a big cost to making metal lines wider and/or thicker
- Pass transistors use up area, and so are costly

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Lecture 29: What have we learned?

- Why is interconnect such a big problem today?
- What gives rise to interconnect delay?
- What are five ways to reduce interconnect delay?

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