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CHE323/CHE384
Chemical Processes for Micro- and Nanofabrication
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# Lecture 28
# Device Interconnect, part 1

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**Reading**:
Chapter 15, *Fabrication Engineering at the Micro- and Nanoscale*, 4th edition, Campbell

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## Device Interconnect

- The CMOS process through transistor formation is called the front-end-of-line (FEOL)
- Connecting all of the transistors together with metal wires (called device interconnect or metallization) is the back-end-of-line (BEOL)
- As the number of transistors grew from thousands to billions, interconnect grew to become extremely difficult – a limitation to cost and performance of the IC

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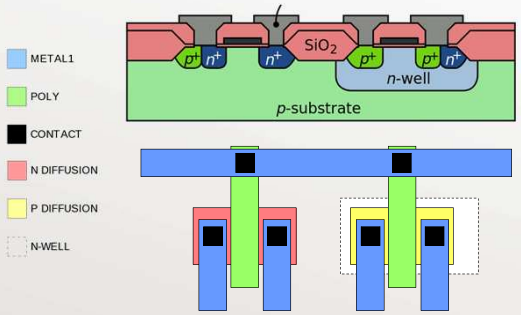
## Single-level Metallization

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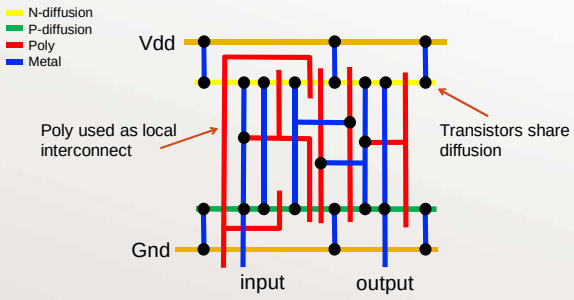
## Stick Diagram

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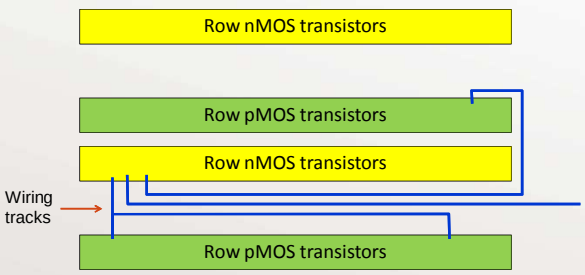
## Metallization in Wiring Tracks

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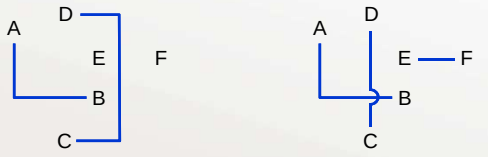
## Topology: Connecting Many Devices




Single level of metal — Multiple levels of metal

Place: where do I place the transistors?
Route: where do I run the metal lines connecting them
Goal: minimize length of wires and area of chip

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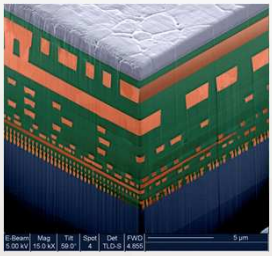
## Mutilevel Metallization

- Adding more levels of metal
  - Each layer adds cost
  - More layers allow for smaller chip area
  - More transistors need more metal layers
  - State-of-the-art today is 10 metal layers



Source: IBM, 2005

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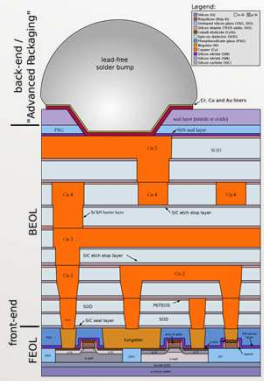


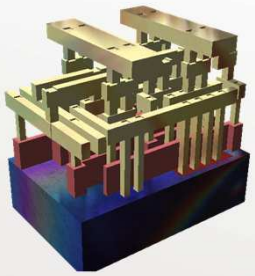

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## Lecture 28: What have we learned?

- Define FEOL and BEOL
- What are the goals of place and route?
- What limits the use of single level metal?
- What are the trade-offs of using more metal levels?

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