CHE323/384 Chemical Processes for Micro- and Nanofabrication
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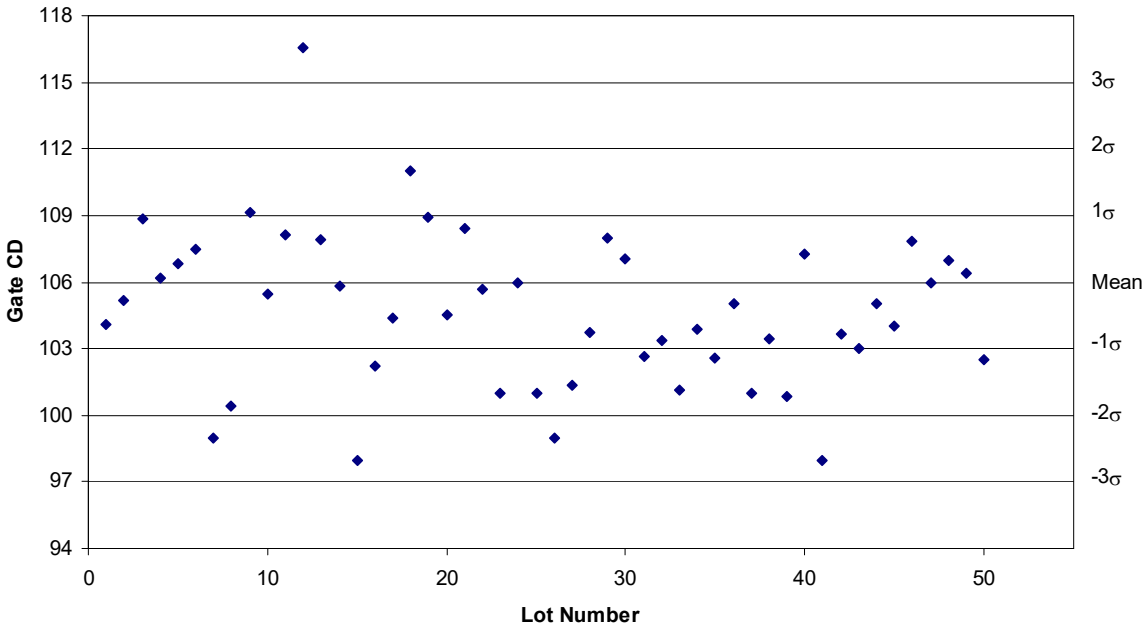
Homework #8

1. Consider an interconnect that exhibits both intralevel and interlevel capacitance using the simple models described in the lectures. Calculate the percentage increase in the interconnect RC delay if the metal and oxide thicknesses remain constant while the metal line and space widths are reduced. Assume that the linewidth and spacewidth are decreased from 0.18 to 0.13 μm and the metal and oxide thicknesses are constant at 0.2 μm. Also assume that the interconnect length L remains constant.

2. Consider the intralevel interconnect delay. Assuming a constant pitch (pitch = linewidth + spacewidth) for the metal lines, what ratio of linewidth to spacewidth will minimize the RC time constant?

3. (a) Identify all violations of the Western Electric rules, explaining which rule has been violated in each case.



(b) For the data in part (a), the mean is 106 nm and the standard deviation is 3 nm. If the target CD is 105 nm and the specification limits are ±10%, what is the Cpk of this process? Is this Cpk bad, marginal, good, or great?

4. An IC manufacturing plant produces 5000 wafers per week. Assume that each wafer contains 140 die, each of which can be sold for $30 if it works. The yield on these chips is currently running at 70%. If the yield can be increased, the incremental income is almost pure profit. How much would the yield have to be increased to produce an annual profit increase of $100,000,000?