CHE323/384 Chemical Processes for Micro- and Nanofabrication
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Homework #2 Solutions

1. A silicon diode is doped on the *n*-side with $N_D = 1 \times 10^{19}$ cm^{-3} and on the *p*-side with $N_A = 2 \times 10^{15}$ cm^{-3}. What is the built-in voltage for the resulting p-n junction? At zero bias, what is the depletion region width? What is the depletion region width when reverse biased by -5 V?

$$V_0 = \frac{kT}{q}\ln\left(\frac{N_A N_D}{n_i^2}\right) = 0.025V\ln\left(\frac{(2\times10^{15})(1\times10^{19})}{(1.5\times10^{10})^2}\right) \quad = \ 0.80 \text{ V (built-in voltage)}$$

$$W = \sqrt{\frac{2\varepsilon_{Si}V_0}{q}\left(\frac{1}{N_A}+\frac{1}{N_D}\right)} = \sqrt{\frac{(2)(11.7)(8.8542\times10^{-14})(0.80)}{1.602\times10^{-19}}\left(\frac{1}{2\times10^{15}}+\frac{1}{1\times10^{19}}\right)} = 7.2 \times 10^{-5} \text{ cm} = 720 \text{ nm}$$

For a reverse bias of -5V, replace V_0 with $V_0 + 5 = 5.80$ V. This increases the depletion width to 1.9 μm.

2. An NMOS transistor has a drain that makes a p-n junction with respect to the substrate with an area of 0.2 μm X 0.2 μm. Calculate the depletion region width and the junction capacitance for this junction when it is reversed biased by -1.5 V. Assume the drain region is very heavily doped (about 1×10^{20} cm^{-3}) and the substrate doping is 2×10^{16} cm^{-3}.

$$V_0 = \frac{kT}{q}\ln\left(\frac{N_A N_D}{n_i^2}\right) = 0.025V\ln\left(\frac{(2\times10^{16})(1\times10^{20})}{(1.5\times10^{10})^2}\right) \quad = \ 0.92 \text{ V (built-in voltage)}$$

$$W = \sqrt{\frac{2\varepsilon_{Si}(V_0 - V)}{q}\left(\frac{1}{N_A}+\frac{1}{N_D}\right)} = \sqrt{\frac{(2)(11.7)(8.8542\times10^{-14})(1.5+0.92)}{1.602\times10^{-19}}\left(\frac{1}{2\times10^{16}}+\frac{1}{1\times10^{20}}\right)} \quad = 396 \text{ nm}$$

$$C_{p-n\ junction} = A\sqrt{\frac{q\varepsilon_{Si}}{2(V_0 - V)}\left(\frac{N_D N_A}{N_D + N_A}\right)} = (2\times10^{-5})^2\sqrt{\frac{(1.602\times10^{-19})(11.7)(8.8542\times10^{-14})}{(2)(1.5+0.92)}\left(\frac{(2\times10^{16})(1\times10^{20})}{2\times10^{16}+1\times10^{20}}\right)}$$

$$C_{p-n\ junction} = \ 1.05 \times 10^{-17} \text{ F}$$

3. To measure the doping level of an n-type wafer, a p^{+}-n junction is formed and its C-V curve is measured. The area of the junction is 100 μm X 100 μm. From the C-V data in the spreadsheet, estimate the wafer doping level. *Hint*: Plot $1/C^2$ vs. V, then extract the slope by finding the best-fit line in the spreadsheet.

$$\frac{1}{C^2} = -\frac{2}{A^2 q \varepsilon_{Si} N_D}(V - V_0)$$, so the slope will be $\left(-\frac{2}{A^2 q \varepsilon_{Si}}\right)\left(\frac{1}{N_D}\right)$ = -1.2 X 10^{39} V $cm^{-3}/F^2\left(\frac{1}{N_D}\right)$

From the best-fit line, the measured slope is -6.152 X 10^{22} V/F^2, giving N_D = 2.0 X 10^{16} cm^{-3}.