CHE323/384 Chemical Processes for Micro- and Nanofabrication
Chris Mack, University of Texas at Austin

Homework #2

1. A silicon diode is doped on the *n*-side with $N_D = 1 \times 10^{19}$ cm^{-3} and on the *p*-side with $N_A = 2 \times 10^{15}$ cm^{-3}. What is the built-in voltage for the resulting p-n junction? At zero bias, what is the depletion region width? What is the depletion region width when reverse biased by -5 V?

2. An NMOS transistor has a drain that makes a p-n junction with respect to the substrate with an area of 0.2 μm × 0.2 μm. Calculate the depletion region width and the junction capacitance for this junction when it is reversed biased by -1.5 V. Assume the drain region is very heavily doped (about 1×10^{20} cm^{-3}) and the substrate doping is 2×10^{16} cm^{-3}.

3. To measure the doping level of an n-type wafer, a p^+-n junction is formed and its C-V curve is measured. From the C-V data in the spreadsheet, estimate the wafer doping level. *Hint*: Plot $1/C^2$ vs. V, then extract the slope by finding the best-fit line in the spreadsheet.