Name: _____

CHE323/384 Chemical Engineering for Micro- and Nanofabrication
Fall, 2013, Chris A. Mack

Practice Exam #2

closed book, closed notes, one formula sheet, calculators allowed

Definitions: Please provide short (one to two sentence) definitions of the following terms. DO NOT use any equations. Make all definitions in words. (2 pt each)

1) Place and Route

2) CMP dishing

3) Sputter yield

4) Epitaxial silicon

Questions: Please provide short (one to two sentence) answers to the following questions. DO NOT use any equations. Make all answers in words. (6 pts each)

1) What is the basic concept behind the Western Electric Rules used in SPC?

2) What commonly causes stress in deposited films, and how is this stress measured?

Problems: Show all work. State all assumptions clearly.

1. (30 pts) For CVD deposition of a film, it is found that the mass transfer coefficient at atmospheric conditions is approximately independent of temperature with a value $h_G = 9.0$ cm/sec. The surface reaction rate coefficient is given by $k_S = 8 \times 10^7 \exp(-1.92 \text{ eV}/kT)$ cm/sec.

a) At what temperature does the transition from reaction-controlled to diffusion-controlled deposition occur?

b) If the pressure is dropped to 1 torr, the value of h_G increases by a factor of 80. For this LPCVD, what is now the transition temperature between reaction-controlled and diffusion-controlled deposition?

2. (20 points) Consider an isotropic etch with infinite selectivity. The film being etched has a nominal thickness d, but this thickness varies by ±20% due to topography. If a 40% overetch is used (that is, the etch time is set to be 40% longer than that required to just etch through the nominal film thickness) in order to ensure complete etching, what is the worst-case undercut distance?

3. (30 points) Consider an interconnect that exhibits only intralevel (within one level of metal) capacitance using the simple model described in the lectures. Calculate the percentage increase in the interconnect RC delay if the metal and oxide thicknesses remain constant while the metal line and space widths are reduced. Assume that the linewidth and spacewidth are decreased from 0.10 to 0.07 μm and the metal and oxide thicknesses are constant at 0.15 μm. Also assume that the interconnect length L remains constant. What can be done to bring this RC delay back down?