WAFER SELECTION GUIDE	
ADVANCED TECHNOLOGY FOR RESEARCH & INDUSTRY	KNOWLEDGE BASE FACT SHEET

- SCOPE: What the parameters in the nomenclature chart mean

This document is a companion to the nomenclature charts used to indicate the naming conventions and parameters we use to keep track of and classify wafers. Most of the terms are common throughout the world of wafers and across the different wafer types.

Silicon Wafers:

Silicon wafers are a thin slice of semiconducting material that is widely used in the production of electronic and micromechanical devices. They are characterised by a number of parameters, which affect their suitability and performance for a chosen task.

1. *Wafer Diameter*

Diameter of the wafer listed in mm. Typically wafers are talked about in inches; typical sizes are 2”,3”,4”,5”,6”,8” & 12” - with 4”,6” and 8” the most commonly used in industry and academia.

2. *Type*

Type refers to the electrical behaviour of the wafer. Intrinsic (I), behaves as pure silicon. N-type, dominant charge carriers are electrons. P-type, dominant charge carriers are holes. Whether a wafer is P-type or N-type will affect the electrical response of any device manufactured.

3. *Crystallographic Orientation*

Wafers are grown as single crystals that have an ordered, regular and repeating structure. When they are sliced from the ingot the flat surface is aligned along one of several relative directions, known as the orientation. The orientation is classified by Miller indices, typical indices being (100), (110) and (111). Orientation affects the physical properties of the silicon wafer – how it is etched, ion implantation and how it integrates with other materials.

4. *Dopant*

The dopant is a material that has been deliberately implanted in the silicon to change the TYPE of the silicon. TYPE and DOPANT are linked.
Typical N-type dopants are Phosphorus, Arsenic, and Antimony. These all provide an extra electron to the silicon which is then free to carry current.
Typical P-type dopants are Boron & Gallium. These have one less electron and so leave a ‘hole’ in the silicon lattice which is free to carry current.

5. *Growth Method*

The growth method refers to the process by which the silicon ingot is grown. There are two main techniques: Czochralski Zone (CZ) and Float Zone (FZ).
CZ: This is the dominant method used to grow commercial silicon wafers due to the better resistance to thermal stress, speed of production and low cost. CZ involves the heating a crucible of polycrystalline silicon until it melts; then dipping a seed of single crystal silicon in and withdrawing slowly to produce an ingot of crystalline silicon.
FZ: This is a high purity alternative to the CZ method. A polycrystalline rod of silicon and a single crystal seed are held face to face and rotated. The rod is then heated by a thin ring and the seed brought in to contact with the tip. The molten silicon orders itself into the single crystal and the heating zone is slowly moved up to extend the ingot of silicon. FZ produces higher purity and higher resistivity Si than is typically possible in CZ processes.

6. *Grade*

Grade refers to the variety in the quality of the wafers. Typically these are PRIME, TEST and RECLAIMED.

- Prime are the highest quality and produced to the highest tolerances on flatness, cleanliness and polish
- Test are similar to prime, except with less rigorous specifications to flatness and cleanliness.
- Reclaimed are wafers that have been stripped and polished of any previous patterning or processing.

There are sometimes other grades of Si wafer mentioned but these are either synonyms of the above or have a specific tolerance on a certain parameter.

7. *Material*
The material is the bulk material of the wafer, typically silicon, but this may vary – some transparent substrates such as glass or quartz are needed for optical devices, and more exotic compound materials such as GaAs or InP for specific band gaps.

8. *Resistivity*
Resistivity is the measure of the resistance to current flow and the movement of the charge carriers (either holes or electrons) through the silicon. Resistivity is measured in Ohm-cm. The dopant level can be adjusted to reach target resistivities, with higher doping lowering the resistivity.

9. *Thickness*
The thickness of the silicon wafer affects the mechanical properties and is typically expressed in µm (microns) and with a tolerance (± 20 µm), The tolerance is measured through a total thickness variation (TTV).

10. *Polish*
Wafer polishing is the final step in the manufacture of silicon wafers, which allows the production of a smooth, super-flat mirrored surface. There are two options for polishing: single side polish (SSP) and double side polish (DSP)
SSP: Only one face is polished, the second (the backside) is etched.
DSP: Both faces are polished, giving a high flatness to the wafer.

11. *Alignment Fiducial*
Alignment fiducial refers to the flats or notches used to identify the wafer. Originally flats were used to identify TYPE as well as ORIENTATION, but now there is less convention about what the flats mean, and notches are quite common on 8" (200mm) wafers.

12. *Other*
At Inseto, we use Other to indicate if the wafers are laser marked with a unique identifier or if they have been stacked in a particular manner.

Coated Wafers
Coated wafers are a subset of silicon wafers where either one or both surfaces have been coated with an additional material. In the Inseto naming convention they are characterised by COATING – the material the wafer is coated with; and COATING THICKNESS – the thickness of that coating, typically µm, nm or Å.

a. Oxide Wafers
One typical coating requested is an Oxide coating. This can be a thermal oxide coating (ATOx) which always coats both sides of the wafer. ATOx stands for atmospheric thermal oxide. Other oxide coating methods include:
Dry Oxide – which produces a thinner oxide layer but with a higher uniformity film.
PECVD Oxide – produces a coating on a single side of the wafer

b. Nitride Wafers
A second typical coating requested is a Nitride coating. Silicon Nitride (SiN) offers different mechanical and chemical properties to oxide layers. The nitride can be deposited by PECVD, LPCVD or low stress LPCVD. These variants are changes in the method of deposition and alter the final physical and mechanical properties of the film.

Glass Wafers:
Glass wafers are generally used where the substrate is required to be transparent. At Inseto we separate out these from silicon and coated silicon wafers as they have some distinct parameters which inform your selection.

1. *Wafer Diameter*
As with Silicon wafers, the diameter is typically listed in mm but may be referred to in inches.

2. *Material*
This lists the material the glass is made from, typical options include Borosilicate, Fused Quartz, Fused Silica and Crystal Quartz. Some people use these terms interchangeably or will drop the 'fused' and 'crystal' terms

3. *Crystallographic Orientation*
Fused Quartz and Fused Silica have no orientation as they are not crystalline materials. Crystal quartz however does and can be X-Cut, Y-Cut, AT-Cut and ST-Cut depending on how the wafer is removed from

the larger crystal.

4. ***Grade***
   The grade of the glass wafer listed here refers to the manufacturers specifications. Each has its own specific chemical, mechanical and optical properties.

5. ***Thickness***
   As with Silicon wafers this refers to the thickness and tolerance of the wafer, typically listed in µm.

6. ***Polish***
   As with Silicon wafers this refers to the finish on the surface of the glass and can be either SSP or DSP. Alongside this there is a rating X/Y, where both X and Y are numbers. X refers to the width of a scratch in µm and Y the diameter of a dig, pit or bubble in hundredths of a mm.

7. ***Edge Shape***
   This denotes how the edge of the glass wafer has been shaped. Most commonly a C shape, but chamfered and square cut are also options.

8. ***Alignment Fiducial, Coating Type, Coating Thickness***
   The final 3 parameters we list are alignment fiducial, coating type and coating thickness and contain the same information as in the Silicon wafers.

SOI wafers:

Another wafer type we separate out is SOI (Silicon on Insulator). SOI wafers make use of a silicon – insulator – silicon substrate and are used for specific applications in microelectronics where reducing parasitic capacitance in the device is crucial. Many photonics devices are also made using SOI wafers to fabricate thin Si optical channels, integrated heaters and other optical devices. They are also used in MEMS production where the thin Si layer is patterned and etched and the underlying insulator layer removed by selective etching to leave a free standing feature. These applications include strain gauges, resonant cantilevers for AFM and molecular scale manipulators as well as microfluidic devices. The choice of insulator within the silicon sandwich is highly specific to the application, but silicon dioxide and sapphire are typical choices for microelectronics and radio frequency applications respectively. The top layer of silicon is referred to as the 'device', the bottom layer the 'handle'.
There are some standard parameters listed as with silicon wafers - these are Diameter, Type and Crystallographic Orientation. We then list the parameters specific to SOI wafers.

1. ***Device Thickness***
   This is the thickness of the top layer of silicon, typically in µm.

2. ***Growth Method***
   This is listed twice in an SOI wafer. First is the growth method of the device layer and can be CZ or FZ.

3. ***Device Resistivity***
   Measured as with a standard silicon wafer, this is the resistivity of the top layer of silicon in Ohm-cm.

4. ***BOx***
   This is the thickness of the insulator layer or 'buried oxide' layer, hence BOx. As with all thicknesses typically µm but can be nm or Å.

5. ***Handle Thickness***
   The thickness of the bottom layer of silicon, typically in µm.

6. ***Growth Method***
   This second listing of growth method relates to the handle layer of silicon.

7. ***Handle Resistivity***
   Measured as with a standard silicon wafer, this is the resistivity of the bottom layer of silicon in Ohm-cm

8. ***Backside***
   This relates to how the backside of the handle layer has been treated and can be a variety of finishes including: Polished, etched, oxide, no oxide and laser marked.

SOS Wafers:

Another type of wafer is SOS (Silicon on Sapphire). SOS wafers make use of a silicon layer grown on a sapphire substrate and are a specific subset of SOI wafers, where the insulator is sapphire. SOS wafers are used in applications where the excellent electrical insulation properties of sapphire are required, such as shielding other circuits from stray currents induced by radiation. As these devices are usually fabricated on Undoped FZ-grown Si to utilise the high minority carrier lifetime properties, these wafers are usually made with undoped EPI-grown Si offering similar properties.

At Inseto we use the parameters below to identify the SOS wafers. These are a hybrid of the SOI parameters and the silicon wafer parameters.

1. ***Diameter***
   As with the other wafer types this is the diameter of the SOS wafers in mm.

2. ***Material***
   This specifies the type of wafer, in the case of all SOS wafers this is SOS.

3. ***Upper Material***
   The upper material of the SOS wafer, usually this is silicon.

4. ***Upper Thickness***
   The thickness of the upper material in microns (μm)

5. ***Resistivity***
   The resistivity of the upper material. This is often critical for SOS-based devices as they are used as the basis of the fabrication for CMOS devices and circuits.

6. ***Dopant***
   This indicates if the upper material has been doped and what material has been doped into it. As with Silicon, the dopant is a material that has been deliberately implanted in the silicon to change the type of the silicon.
   Typical N-type dopants are Phosphorus, Arsenic, and Antimony. These all provide an extra electron to the silicon which is then free to carry current.
   Typical P-type dopants are Boron & Gallium. These have one less electron and so leave a 'hole' in the silicon lattice which is free to carry current.

7. ***Lower Material***
   The lower material of the SOS wafer, usually this is sapphire.

8. ***Cut of Lower Material***
   The cut of the lower material (sapphire wafer) from the original crystal, most common is R- plane as the position of Oxygen atoms in the Sapphire lattice is a good match for (100) Si and the resulting interface is free of defects such as stacking faults and dislocations.

9. ***Orientation of Plane***
   This is an additional metric for describing the plane of the lower material (sapphire wafer). For R-plane this is (1102).

10. ***Lower Material Thickness***
    The thickness of the lower material in microns (μm).

11. ***Polish***
    As with Silicon wafers this refers to the finish on the surface of the glass and can be either SSP or DSP.

12. ***-***

13. ***Alignment, Coating Type, Coating Thickness and Other***
    The final 4 parameters we listed are alignment fiducial, coating type, coating thickness and other contain the same information as in the Silicon wafers.

Sapphire Wafers:

Sapphire wafers are a thin slice of single crystal sapphire that is widely used in the production of electronic and optical devices. They are characterised by a number of parameters, which affect their suitability and performance for a chosen task.

1. ***Wafer Diameter***
   Diameter of the wafer listed in mm. Typically wafers are talked about in inches; typical sizes are 2”,3”,4”,5”,6”,8” & 12” - with 2”,3” and 4” the most commonly used in industry and academia.

2. ***Growth Method***
   The growth method refers to the process by which the ingot of single crystal sapphire is produced. For most sapphire wafers this is the Kyropoulos method (abbreviated to Ky or Kr). The Kyropoulos method is a continuation of the Czochralski method (CZ) which is used in the manufacture of silicon wafers. The Kr method allows for the production of very large ingots of single crystal sapphire that can then be processed into wafers.

3. ***Crystallographic Orientation***
   Wafers are grown as single crystals that have an ordered, regular and repeating structure. When they are sliced from the ingot the flat surface is aligned along one of several relative directions, known as the orientation. The orientation is classified by Miller indices as with silicon wafers but more commonly these are referred to by specific planes.

   Typical cuts of sapphire are R-plane (1102), C-Plane (0001), A-plane (1120), M-plane (1010) and N-plane (1123). Orientation affects the physical properties of the sapphire wafers – and in particular how it integrates and lattice matches with other materials.

4. ***Thickness***
   The thickness of the sapphire wafer affects the mechanical properties and is typically expressed in µm (microns) and with a tolerance (± 20 µm). The tolerance is measured through a total thickness variation (TTV).

5. ***Polish***
   Wafer polishing is the final step in the manufacture of silicon wafers, which allows the production of a smooth, super-flat mirrored surface. There are two options for polishing: single side polish (SSP) and double side polish (DSP).
   SSP: Only one face is polished, the second (the backside) is etched.
   DSP: Both faces are polished, giving a high flatness to the wafer.

6. ***Alignment Fiducial***
   Alignment fiducial refers to the flats or notches used to identify the wafer. Originally flats were used to identify TYPE and well as ORIENTATION, but now there is less convention about what the flats mean and notches are quite common on 8” (200mm) wafers.

7. ***Other***
   At Inseto, we use Other to indicate if the wafers are laser marked with a unique identifier or if they have been stacked in a particular manner.