REV	DESCRIPTION	DATE	APPROVED
-	ORIGINATED		

THIN FILM CIRCUITS

DESIGN RULES

REVISION	-	-	-	-	-	-	-	-																			
SHEET NO.	1	2	3	4	5	6	7	8																			

DRAWN BY		
DOC CONTROL		
ENGINEERING		
DEPT MANAGER		
Q.A.		

ATP APPLIED THIN-FILM PRODUCTS

SIZE	CAGE CODE	DRAWING NUMBER	REV
A	04ZMO	50020	-

SCALE		SHEET 1 OF 2

1.0 PURPOSE/SCOPE

1.1 This document defines the design rules for the thin film circuits.

1.2 This policy applies to all thin film circuits manufactured by Applied Thin-Film Products.

1.3 This document is divided into two sections:

1. Fundamental design rules that must be followed in order for the product to be compatible with ATP's processing techniques.
2. Mask (tooling) requirements.

2.0 FUNDAMENTAL DESIGN RULES

2.1 Standard processing requires that circuits be square or rectangular. Custom shapes require special processing considerations and ATP engineering approval.

2.2 All circuit features must consist of straight lines, arcs, or combinations thereof. Freehand curves are not acceptable.

2.3 Substrate material type, thickness and surface finish must be specified.

2.4 Metalization requirements must be specified. This includes metal types, thickness and tolerances for both sides of the substrate.

2.5 Minimum nominal conductor line width is 0.0008" (20 microns) if the gold thickness is 160 microinches (4 microns) or less.

2.6 Minimum nominal conductor gap width is 0.0004" (10 microns) if the gold thickness is 160 microinches (4 microns) or less. This applies to plate up processes only. Please contact us for minimum gaps for etch back processes.

2.7 Critical dimensions have a standard minimum tolerance of $\pm$0.0001" ($\pm$2.54 microns) from nominal if the gold thickness is 160 microinches (4 microns) or less.

2.8 The standard tolerance for Au thickness is $\pm$20%.

2.9 Minimum nominal resistor width and length is 0.0025" (63.5 microns).

2.10 The tantalum nitride resistor has a stabilized sheet resistance of either 50, 75 or 100 ohms per square. Other values may be available if required.

2.11 Standard resistor tolerance is +-10%. Tighter tolerances are available using laser trimming methods at a higher cost (for further information, please refer to the “Laser Resistor Trim Guidelines” Document #50025.

2.12 All circuits containing thin film resistors should have an isolated 50 ohm test resistor. This is especially important for designs incorporating non-measurable resistors (e.g. Wilkinson style dividers, etc.).

2.13 All conductor and resistor geometries should be a minimum of 0.002" (50 microns) from the edge of the circuit (*see figure 1*).

2.14 The dicing mark should be located on the conductor layer. The preferred dicing mark is a .006”x.030” (152x762 microns) cross (*see figure 2*).

2.15 The standard dicing tolerance (final circuit size) is +-0.002" (50 microns).

2.16 All circuits should have an identifying notation of the conductor layer.

2.17 The optimum aspect ratio* for plated thru (via) hole is 1.0 (e.g. a 0.015" hole in a 0.0015" thick substrate). A minimum ratio of 0.6 is acceptable for 0.015”-0.025” thick substrates. A minimum ratio of 0.8 is acceptable for 0.010” thick substrates Less than this requires ATP engineering approval (*see figure 3*)

*Aspect ratio is defined as: D_v / T_s
where: D_v = diameter of the via (thru hole)
T_s = Thickness of the substrate

2.18 Spacing between holes must be a minimum of one hole diameter (*see figure 3*)

2.19 The minimum distance from the edge of the conductor pad surrounding the thru (via) hole and the hole's edge is 0.0025" (63.5 microns) (*see figure 3*)

3.0 MASK (TOOLING) REQUIREMENTS

3.1 PLATE-UP PROCESS (*conductor mask*)

3.1.1 The conductor geometry is light and the field is dark (negative).

3.1.2 The conductor pattern and the part number are right reading with the emulsion/chrome side down.

3.1.3 A notched (island method) resistor is treated as a void (clear) (*see figure 4*)

3.1.4 A flush (etch back method) resistor is treated as a solid conductor line (*see figure 5)*

3.1.5 All critical dimensions for the plate up process must have an exposure factor built in. Gaps must be biased on the mask 0.00015" (3.81 microns) wider than the nominal dimension. Line widths must be biased on the mask 0.00015" (3.81 microns) narrower than the nominal dimension. (The exposure factor is required due to the combination of light diffraction during exposure and the use of a thick photoresist (>5 micron).

3.2 ETCH BACK PROCESS (*conductor mask*)

3.2.1 The conductor geometry is light and the field is dark (negative).

3.2.2 The conductor pattern and the part number are right reading with the emulsion/chrome side down.

3.2.3 A notched (island method) resistor is treated as a void (clear) (*see figure 4*).

3.2.4 A flush (etch back method) resistor is treated as a solid conductor line (*see figure 5*).

3.2.5 All critical dimensions for the etch back process must have an etch factor built in. Gaps must be biased on the mask 0.0001" (2.54 microns) per 40 microinches (1 micron) of Au narrower than the nominal dimension (e.g. If the Au thickness is 120 microinches (3 microns) bias the

gap 0.0003" narrower). Line widths must be biased on the mask 0.0001" per 40 microinches of Au wider than the nominal dimension. (The etch factor is required due to the undercutting of the Au layer by the etchant during the conductor patterning process).

3.3 NOTCHED RESISTOR PROCESS (*resistor mask*)

3.3.1 The resistor geometry is dark and the field is light (positive).

3.3.2 The resistor pattern is right reading with the emulsion/chrome side down.

3.3.3 All resistors must be notched (*see figure 4*). The notch indent must be a minimum of 0.001" on both sides. Resistor edges should not be flush with the conductor geometry.

3.3.4 Resistors must be dimensioned with a minimum of 0.002" (50 micron) to a maximum of .005" (127 micron) overlap onto the conductor line. Etch and/or exposure factors are not required with the notched resistor process (*see figure 4*).

3.4 FLUSH RESISTOR PROCESS (*resistor mask*)

3.4.1 The resistor geometry is dark and the field is light (positive).

3.4.2 The resistor pattern is right reading with the emulsion/chrome side down.

3.4.3 Resistors must be dimensioned with a minimum of 0.002" (50 micron) to a maximum of .005" (127 micron) overlap wider than the conductor line. Resistor lengths must be biased on the mask 0.0001" (2.54 microns) per 40 microinches (1 micron) of Au shorter than the nominal length of the resistor (e.g. If the Au thickness is 120 microinches (3 microns), bias the resistor length 0.0003" shorter) (*see figure 5).*

3.5 ARRAY

3.5.1 The mask array directly determines the substrate that can be used. The size of the substrate used to fabricate your parts heavily influences the final cost of the circuit. The array size required depends on the circuit size and the quantity ordered. If ATP is fabricating the mask, the optimum array size will automatically be determined for you. If you are providing the masks, please contact us to determine the optimum array size. Standard array sizes are 1"x1", 2"x2", 2.25"x2.25", 3"x3", 3.25”x3.25”, and 4”x4”.

3.5.2 The standard border size between the edge of the array and the edge of the substrate if 0.050" (1270 microns).

3.5.3 The standard dicing kerf (saw street width) is 0.010" (254 microns). 0.008” (203.2 microns), 0.006" (152.4 microns), and 0.005” (127 micron) dicing kerfs are also available. Other sizes can be accommodated. Please contact us for additional information.

3.5.4 The stepping distance of the circuits in the array is determined by adding the dicing kerf to the circuit size. The dicing alignment mark (section 2.15) will be centered at each intersection.

3.6 SUBSTRATE MATERIALS

3.6.1 The following is a list of the standard materials processed by ATP.

MATERIAL / THICKNESS

Alumina (Al_20_3)Asfired surface finish
0.005"
0.010"
0.015"
0.020"
0.025"

Alumina (Al_20_3)Polished surface finish
0.005"
0.010"
0.015"
0.020"
0.025"

Beryllium Oxide (BeO)
0.010"
0.015"
0.025"

Other materials are also available. These include:

Aluminum Nitride
Quartz/Fused Silica
Sapphire
Barium Titanates

Please contact us if you require information on other types of materials or for specifications for any of the above listed materials.

Minimum Conductor to Circuit Edge Spacing: 0.002”(50 microns)

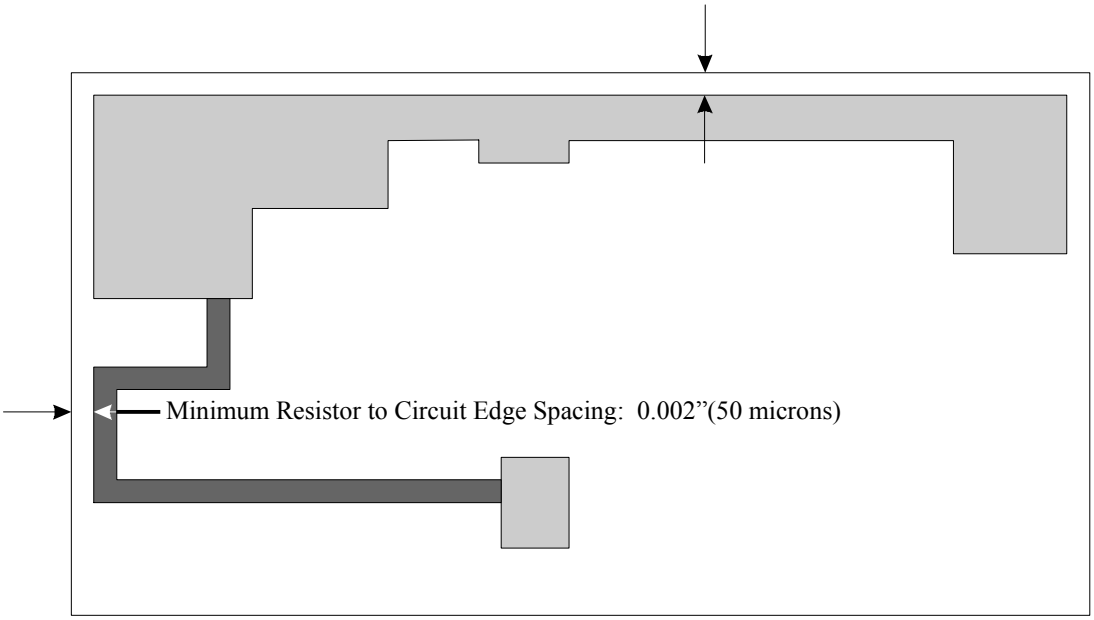


FIGURE #1

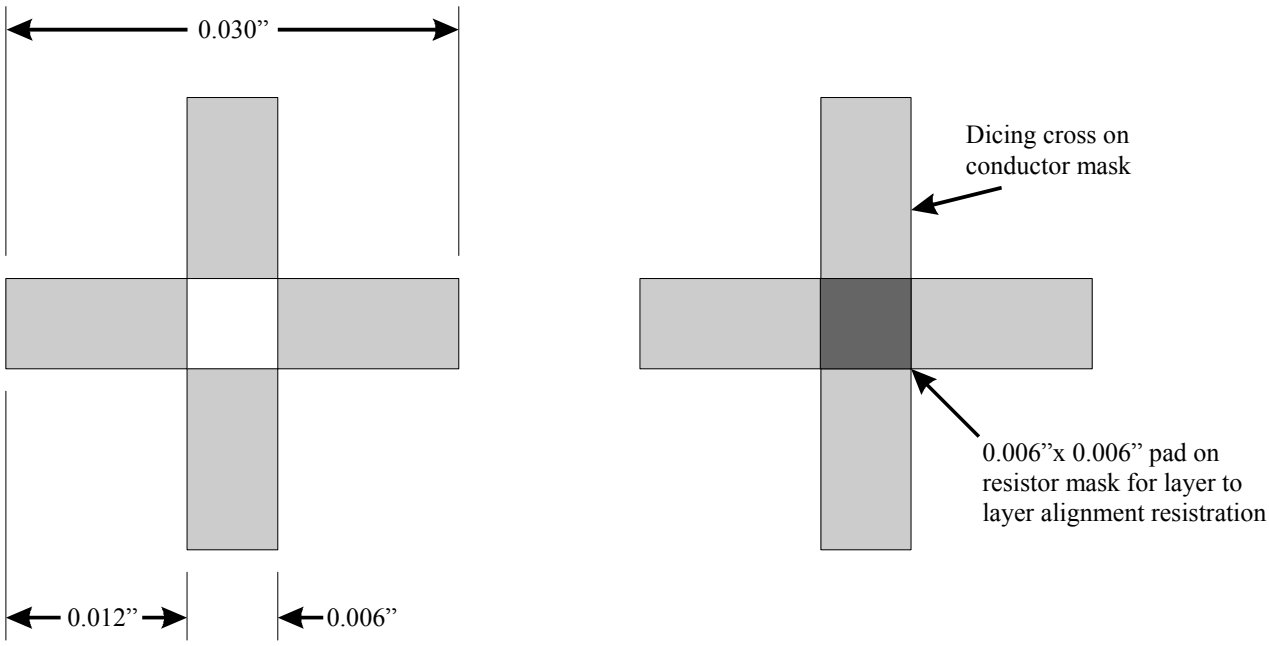


FIGURE #2

APPLIED THIN-FILM PRODUCTS	SIZE	CAGE CODE	DRAWING NUMBER	REV
	A	04ZMO	50020	-
	SCALE			SHEET 6 OF 6

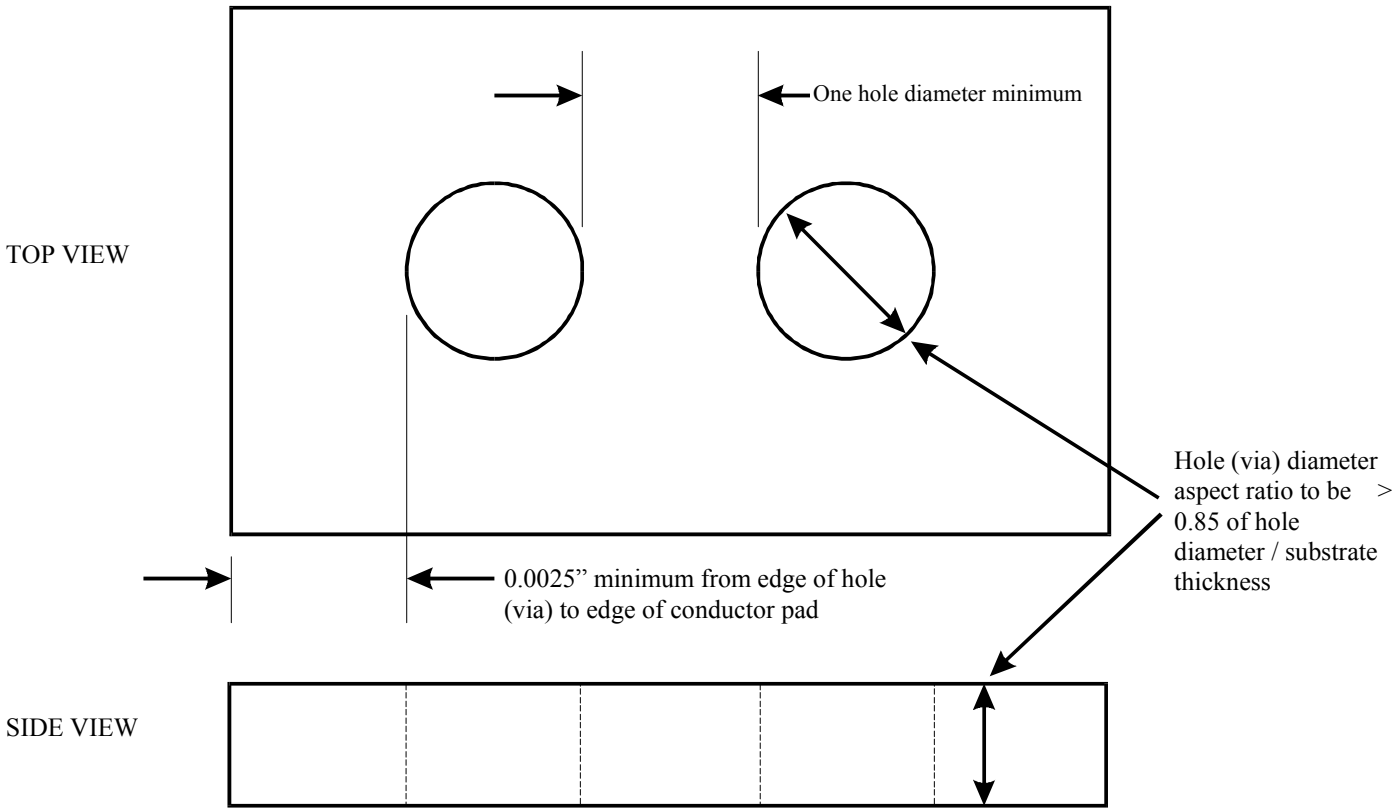
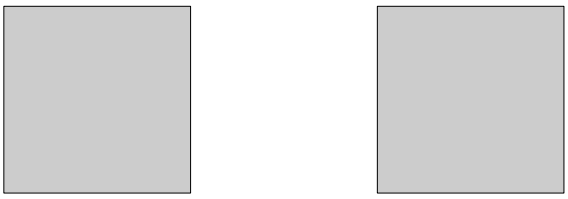


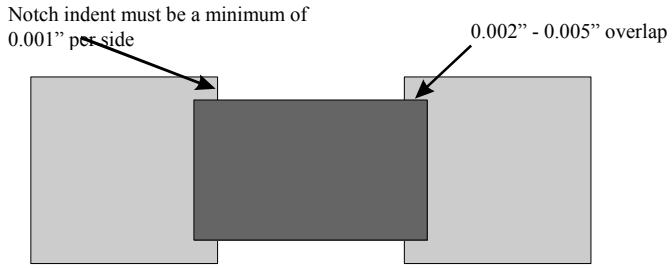
FIGURE #3

	SIZE	CAGE CODE	DRAWING NUMBER	REV
ATP APPLIED THIN-FILM PRODUCTS	A	04ZMO	50020	-
	SCALE			SHEET 7 OF 7

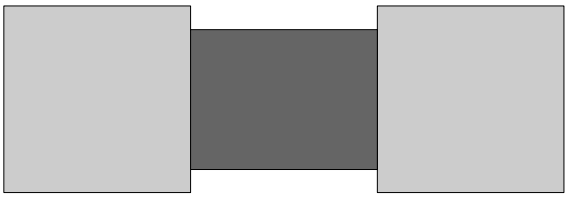
NOTCHED RESISTOR PROCESS
(ISLAND METHOD)



Conductor Mask:
Resistor is treated as a void (clear)



Resistor Mask:
Resistors must be dimensioned
with a 0.002"- 0.005" overlap
onto the conductor line

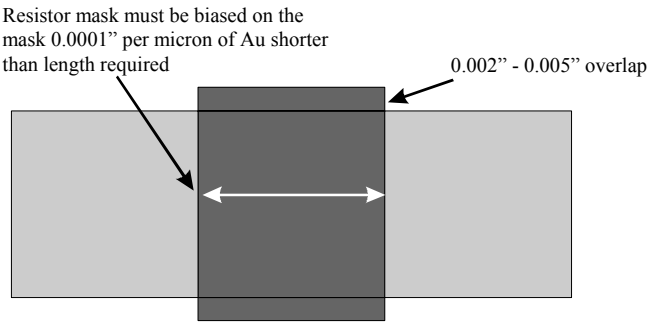


Final Circuit

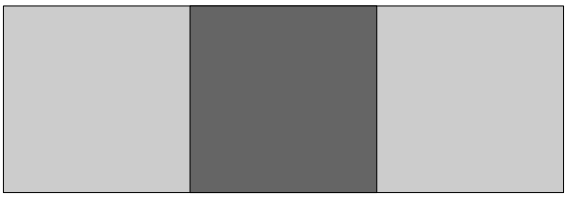
FIGURE #4

FLUSH RESISTOR PROCESS
(ETCH-BACK METHOD)

Conductor Mask:
Resistor is treated as a solid line



Resistor Mask:
Resistors must be dimensioned
with a 0.002"- 0.005" overlap
wider than the conductor line



Final Circuit

FIGURE #5

	SIZE	CAGE CODE	DRAWING NUMBER	REV
ATP APPLIED THIN-FILM PRODUCTS	A	04ZMO	50020	-
	SCALE			SHEET 8 OF 8