

# SNx5C116x Dual Differential Drivers and Receivers

## 1 Features

- Meet or exceed standards TIA/EIA-422-B and ITU recommendation V.11
- BiCMOS process technology
- Low supply-current requirements: 9mA maximum
- Low pulse skew
- Receiver input impedance: 17kΩ typical
- Receiver input sensitivity: ±200mV
- Receiver common-mode input voltage range of -7V to 7 V
- Operate from single 5V power supply
- Glitch-free power-up and power-down protection
- Receiver 3-state outputs active-low enable for SN65C1167 and SN75C1167 only
- Improved replacements for the MC34050 and MC34051

## 2 Applications

- [Motor Drives](#)
- [Factory Automation](#)
- [Building Automation](#)

## 3 Description

The SN65C1167, SN75C1167, SN65C1168, and SN75C1168 dual drivers and receivers are integrated circuits designed for balanced transmission lines. The devices meet TIA/EIA-422-B and ITU recommendation V.11.

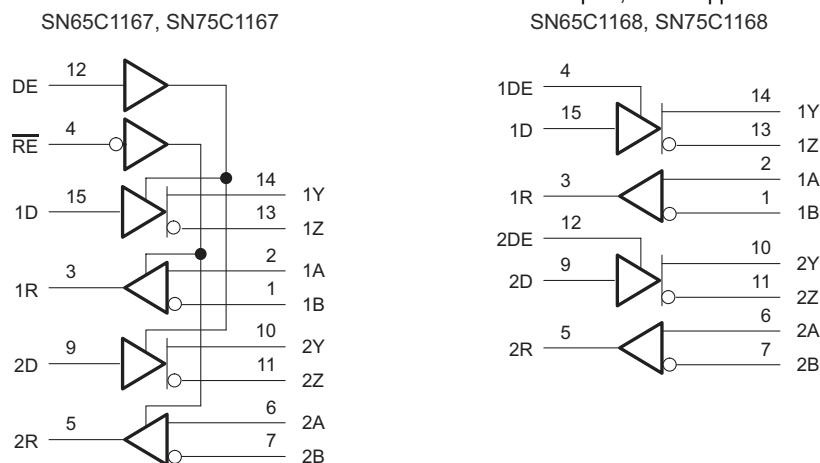
The SN65C1167 and SN75C1167 combine dual 3-state differential line drivers and 3-state differential line receivers, both of which operate from a single 5V power supply. The driver and receiver have active-high and active-low enables, respectively, which can be connected together externally to function as direction control. The SN65C1168 and SN75C1168 drivers have individual active-high enables.

### Package Information

PART NUMBER	PACKAGE <sup>(1)</sup>	PACKAGE SIZE <sup>(2)</sup>
SN65C1167	DB (SSOP)	6.2mm x 5.30mm
	NS (SOP)	10.3mm x 5.30mm
SN75C1167	DB (SSOP)	6.2mm x 5.30mm
	N (PDIP)	19.3mm x 6.35mm
	NS (SOP)	10.3mm x 5.30mm
SN65C1168	N (PDIP)	19.3mm x 6.35mm
	NS (SOP)	10.3mm x 5.30mm
	PW (TSSOP)	5mm x 4.40mm
SN75C1168	DB (SSOP)	6.2mm x 5.30mm
	N (PDIP)	19.3mm x 6.35mm
	NS (SOP)	10.3mm x 5.30mm
	PW (TSSOP)	5mm x 4.4mm

(1) For more information, see [Section 10](#).

(2) The package size (length × width) is a nominal value and includes pins, where applicable.



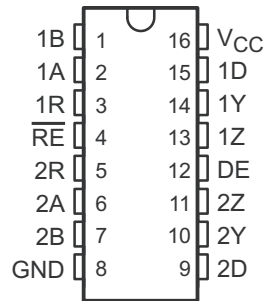
Logic Diagram (Positive Logic)



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## 4 Pin Configuration and Functions

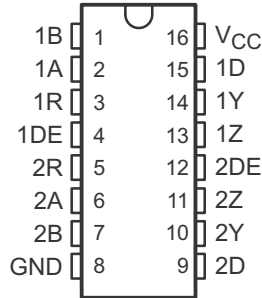


**Figure 4-1. SN65C1167: DB or NS Package  
SN75C1167: DB, N, or NS Package  
(Top View)**

**Table 4-1. Pin Functions, SNx5C1167**

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
1B	1	I	Inverting Input of Channel 1 Differential Receiver
1A	2	I	Non-Inverting Input of Channel 1 Differential Receiver
1R	3	O	Single Ended Receiver Output for Channel 1
$\overline{RE}$	4	I	Receiver Active Low Enable Input for Channel 1 and 2
2R	5	O	Single Ended Receiver Output for Channel 2
2A	6	I	Non-Inverting Input of Channel 1 Differential Receiver
2B	7	I	Inverting Input of Channel 2 Differential Receiver
GND	8	G	Device Ground
2D	9	I	Single Ended Driver Input for Channel 2
2Y	10	O	Non-Inverting Output of Channel 2 Differential Driver
2Z	11	O	Inverting Output of Channel 2 Differential Driver
DE	12	I	Driver Active High Enable Input for Channel 1 and 2
1Z	13	O	Inverting Output of Channel 1 Differential Driver
1Y	14	O	Non-Inverting Output of Channel 1 Differential Driver
1D	15	I	Single Ended Driver Input for Channel 1
V <sub>CC</sub>	16	P	Device VCC, connect 4.5V to 5.5V Source between this Pin and Device Ground

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.



**Figure 4-2. SN65C1168: N, NS, or PW Package  
 SN75C1168: DB, N, NS, or PW Package  
 (Top View)**

**Table 4-2. Pin Functions, SNx5C1168**

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
1B	1	I	Inverting Input of Channel 1 Differential Receiver
1A	2	I	Non-Inverting Input of Channel 1 Differential Receiver
1R	3	O	Single Ended Receiver Output for Channel 1
1DE	4	I	Driver Active High Enable Input for Channel 1
2R	5	O	Single Ended Receiver Output for Channel 2
2A	6	I	Non-Inverting Input of Channel 1 Differential Receiver
2B	7	I	Inverting Input of Channel 2 Differential Receiver
GND	8	G	Device Ground
2D	9	I	Single Ended Driver Input for Channel 2
2Y	10	O	Non-Inverting Output of Channel 2 Differential Driver
2Z	11	O	Inverting Output of Channel 2 Differential Driver
2DE	12	I	Driver Active High Enable Input for Channel 2
1Z	13	O	Inverting Output of Channel 1 Differential Driver
1Y	14	O	Non-Inverting Output of Channel 1 Differential Driver
1D	15	I	Single Ended Driver Input for Channel 1
V <sub>CC</sub>	16	P	Device VCC, connect 4.5V to 5.5V Source between this Pin and Device Ground

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT	
V <sub>CC</sub>	Supply voltage range <sup>(2)</sup>	-0.5	7	V	
V <sub>I</sub>	Input voltage range	Driver	-0.5	V <sub>CC</sub> + 0.5	V
		A or B, Receiver	-11	14	
V <sub>ID</sub>	Differential input voltage range <sup>(3)</sup>	-14	14	V	
V <sub>O</sub>	Output voltage range	-0.5	7	V	
I <sub>IK</sub> or I <sub>OK</sub>	Clamp current range		±20	mA	
I <sub>O</sub>	Output current range	Driver	±150	mA	
		Receiver	±25		
I <sub>CC</sub>	Supply current		200	mA	
	GND current		-200		
T <sub>J</sub>	Operating virtual junction temperature		150	°C	
T <sub>stg</sub>	Storage temperature range	-65	150	°C	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages values except differential input voltage are with respect to the network GND.
- (3) Differential input voltage is measured at the noninverting terminal with respect to the inverting terminal.

### 5.2 ESD Ratings

		VALUE	UNIT	
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±8kV	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1kV	

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

### 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	V
V <sub>IC</sub>	Common-mode input voltage <sup>(1)</sup>			±7	V
V <sub>ID</sub>	Differential input voltage			±7	V
V <sub>IH</sub>	High-level input voltage	2			V
V <sub>IL</sub>	Low-level input voltage			0.8	V
I <sub>OH</sub>	High-level output current	Receiver		-6	mA
		Driver		-20	
I <sub>OL</sub>	Low-level output current	Receiver		6	mA
		Driver		20	

### 5.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT	
T <sub>A</sub>	Operating free-air temperature	SN75C1167, SN75C1168		0	70	°C
		SN65C1167, SN65C1168		-40	85	

(1) Refer to TIA/EIA-422-B for exact conditions.

### 5.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		DB (SSOP)	N (PDIP)	NS (SOP)	PW (TSSOP)	UNIT
		16 PINS	16 PINS	16 PINS	16 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	102.6	60.6	88.5	107.5	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	48.7	48.1	46.2	38.4	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	54.3	40.6	50.7	53.7	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	11.8	27.5	13.5	3.2	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	53.5	40.3	50.3	53.1	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics application report](#).

### 5.5 Electrical Characteristics, Driver Section<sup>(2)</sup>

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP <sup>(1)</sup>	MAX	UNIT	
V <sub>IK</sub>	Input clamp voltage	I <sub>I</sub> = -18mA				-1.5	V	
V <sub>OH</sub>	High-level output voltage	V <sub>IH</sub> = 2V, V <sub>IL</sub> = 0.8V, I <sub>OH</sub> = -20mA		2.4	3.4		V	
V <sub>OL</sub>	Low-level output voltage	V <sub>IH</sub> = 2V, V <sub>IL</sub> = 0.8V, I <sub>OL</sub> = 20mA			0.2	0.4	V	
V <sub>OD1</sub>	Differential output voltage	I <sub>O</sub> = 0mA		2		6	V	
V <sub>OD2</sub>	Differential output voltage <sup>(2)</sup>	R <sub>L</sub> = 100Ω, See <a href="#">Figure 6-1</a>		2	3.1		V	
Δ V <sub>OD</sub>	Change in magnitude of differential output voltage						±0.4	V
V <sub>OC</sub>	Common-mode output voltage						±3	V
Δ V <sub>OCL</sub>	Change in magnitude of common-mode output voltage						±0.4	V
I <sub>O(OFF)</sub>	Output current with power off	V <sub>CC</sub> = 0V	V <sub>O</sub> = 6V V <sub>O</sub> = -0.25V			100 -100	μA	
I <sub>OZ</sub>	High-impedance-state output current	V <sub>O</sub> = 2.5 V <sub>O</sub> = 5				20 -20	μA	
I <sub>IH</sub>	High-level input current	V <sub>I</sub> = V <sub>CC</sub> or V <sub>IH</sub>				1	μA	
I <sub>IL</sub>	Low-level input current	V <sub>I</sub> = GND or V <sub>IL</sub>				-1	μA	
I <sub>OS</sub>	Short-circuit output current <sup>(3)</sup>	V <sub>O</sub> = V <sub>CC</sub> or GND,		-30		-150	mA	
I <sub>CC</sub>	Supply current (total package) <sup>(4)</sup>	No load, Enabled	V <sub>I</sub> = V <sub>CC</sub> or GND		4	6	mA	
			V <sub>I</sub> = 2.4 or 0.5V		5	9		
C <sub>i</sub>	Input capacitance				6		pF	

(1) All typical values are at V<sub>CC</sub> = 5V, and T<sub>A</sub> = 25°C.

(2) Refer to TIA/EIA-422-B for exact conditions.

(3) Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

(4) This parameter is measured per input, while the other inputs are at V<sub>CC</sub> or GND.

## 5.6 Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP <sup>(1)</sup>	MAX	UNIT
$t_{PHL}$	Propagation delay time, high- to low-level output	R1 = R2 = 50 $\Omega$ , C1 = C2 = C3 = 40pF, See Figure 6-2	R3 = 500 $\Omega$ , S1 is open,		7	12	ns
$t_{PLH}$	Propagation delay time, low- to high-level output				7	12	ns
$t_{sk(p)}$	Pulse skew				0.5	4	ns
$t_r$	Rise time	R1 = R2 = 50 $\Omega$ , C1 = C2 = C3 = 40pF, See Figure 6-3	R3 = 500 $\Omega$ , S1 is open,		5	10	ns
$t_f$	Fall time				5	10	ns
$t_{PZH}$	Output enable time to high level	R1 = R2 = 50 $\Omega$ , C1 = C2 = C3 = 40pF, See Figure 6-4	R3 = 500 $\Omega$ , S1 is closed,		10	19	ns
$t_{PZL}$	Output enable time to low level				10	19	ns
$t_{PHZ}$	Output disable time from low level	R1 = R2 = 50 $\Omega$ , C1 = C2 = C3 = 40pF, See Figure 6-4	R3 = 500 $\Omega$ , S1 is closed,		7	16	ns
$t_{PLZ}$	Output disable time from high level				7	16	ns

(1) All typical values are at  $V_{CC} = 5V$ , and  $T_A = 25^\circ C$ .

## 5.7 Electrical Characteristics, Receiver Section

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP <sup>(1)</sup>	MAX	UNIT
$V_{IT+}$	Positive-going input threshold voltage, differential input					0.2	V
$V_{IT-}$	Negative-going input threshold voltage, differential input			-0.2 <sup>(2)</sup>			V
$V_{hys}$	Input hysteresis ( $V_{IT+} - V_{IT-}$ )				60		mV
$V_{IK}$	Input clamp voltage, $\overline{RE}$	SN75C1167	$I_I = -18$ mA			-1.5	V
$V_{OH}$	High-level output voltage		$V_{ID} = 200$ mV, $I_{OH} = -6$ mA	3.8	4.2		V
$V_{OL}$	Low-level output voltage		$V_{ID} = -200$ mV, $I_{OL} = 6$ mA		0.1	0.3	V
$I_{OZ}$	High-impedance-state output current	SN75C1167	$V_O = V_{CC}$ or GND		$\pm 0.5$	$\pm 5$	$\mu A$
$I_I$	Line input current		Other input at 0 V			1.5	mA
						-2.5	
$I_I$	Enable input current, $\overline{RE}$	SN75C1167	$V_I = V_{CC}$ or GND			$\pm 1$	$\mu A$
$r_i$	Input resistance		$V_{IC} = -7$ V to 7 V, Other input at 0 V	4	17		k $\Omega$
$I_{CC}$	Supply current (total package)		No load, Enabled			4	mA
						5	

(1) All typical values are at  $V_{CC} = 5V$  and  $T_A = 25^\circ C$ .

(2) The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.

(3) Refer to TIA/EIA-422-B for exact conditions.

## 5.8 Switching Characteristics

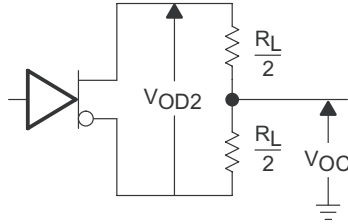
over operating free-air temperature range (unless otherwise noted) <sup>(2)</sup>

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
t <sub>PLH</sub>	Propagation delay time, low- to high-level output	See <a href="#">Figure 6-5</a>	9	17	27	ns
t <sub>PHL</sub>	Propagation delay time, high- to low-level output		9	17	27	ns
t <sub>TLH</sub>	Transition time, low- to high-level output	V <sub>IC</sub> = 0V, See <a href="#">Figure 6-5</a>		4	9	ns
t <sub>THL</sub>	Transition time, high- to low-level output			4	9	ns
t <sub>PZH</sub>	Output enable time to high level	R <sub>L</sub> = 1kW, See <a href="#">Figure 6-6</a>		13	22	ns
t <sub>PZL</sub>	Output enable time to low level			13	22	ns
t <sub>PHZ</sub>	Output disable time from high level			13	22	ns
t <sub>PLZ</sub>	Output disable time from low level			13	22	ns

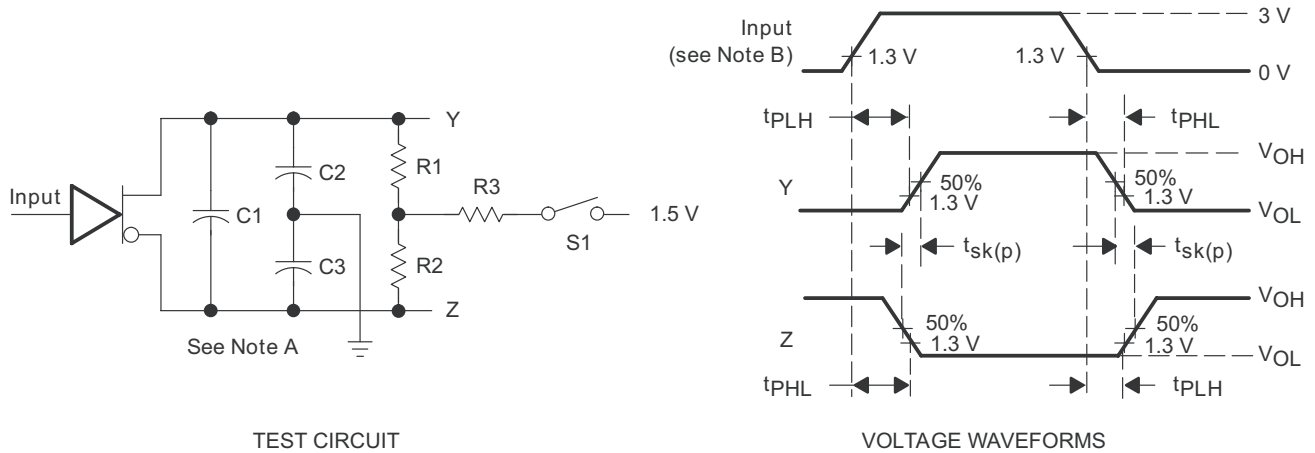
- (1) All typical values are at V<sub>CC</sub> = 5V and T<sub>A</sub> = 25°C.  
 (2) Measured per input while the other inputs are at V<sub>CC</sub> or GND



## 6 Parameter Measurement Information

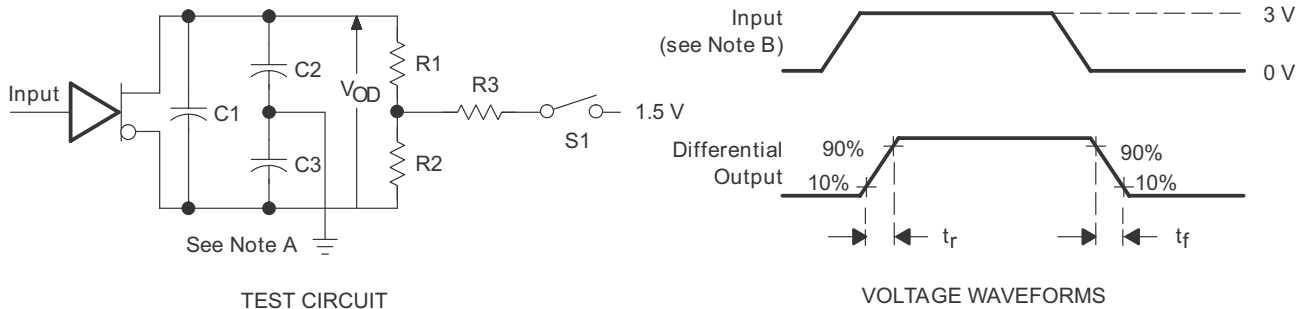


**Figure 6-1. Driver Test Circuit,  $V_{OD}$  and  $V_{OC}$**



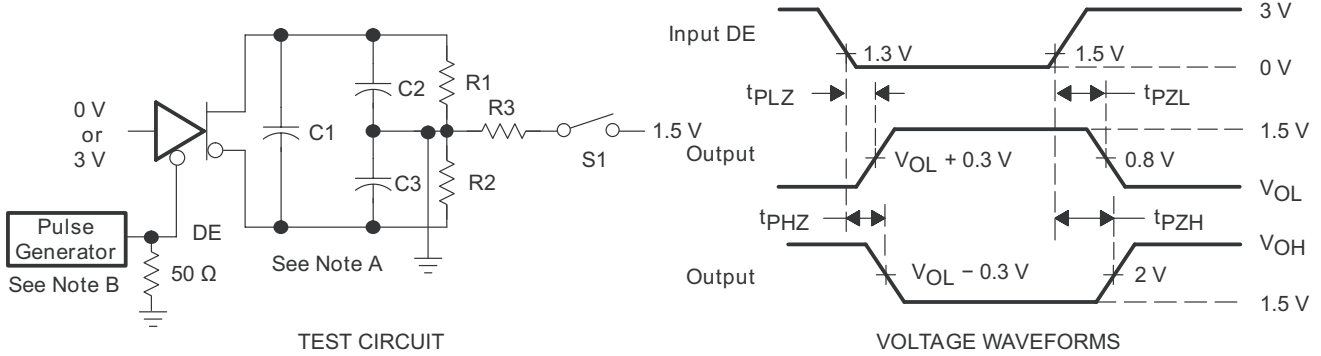
- A. C1, C2, and C3 include probe and jig capacitance.  
B. The input pulse is supplied by a generator having the following characteristics: PRR = 1MHz, 50% duty cycle,  $t_r = t_f \leq 6$ ns.

**Figure 6-2. Driver Test Circuit and Voltage Waveforms**



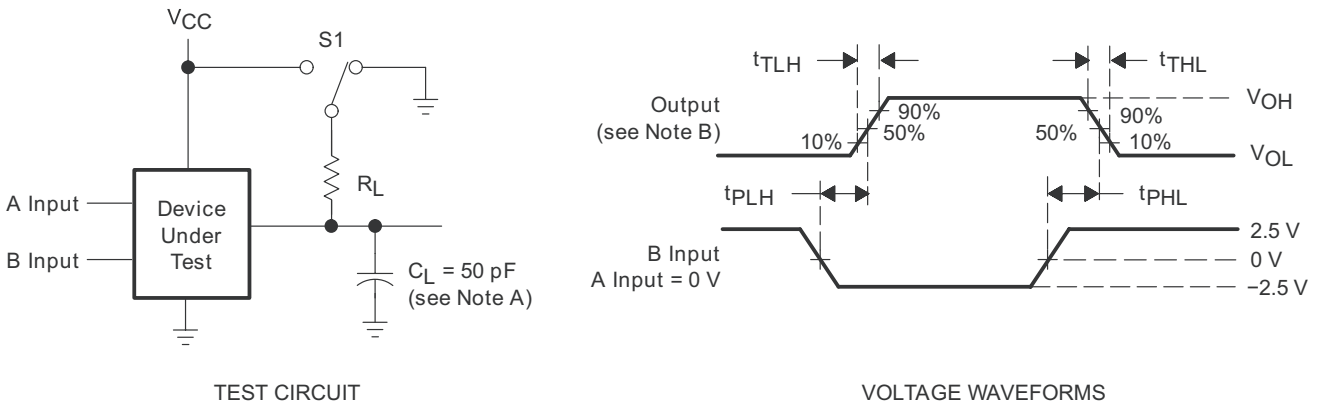
- A. C1, C2, and C3 include probe and jig capacitance.  
B. The input pulse is supplied by a generator having the following characteristics: PRR = 1MHz, 50% duty cycle,  $t_r = t_f \leq 6$ ns.

**Figure 6-3. Driver Test Circuit and Voltage Waveforms**



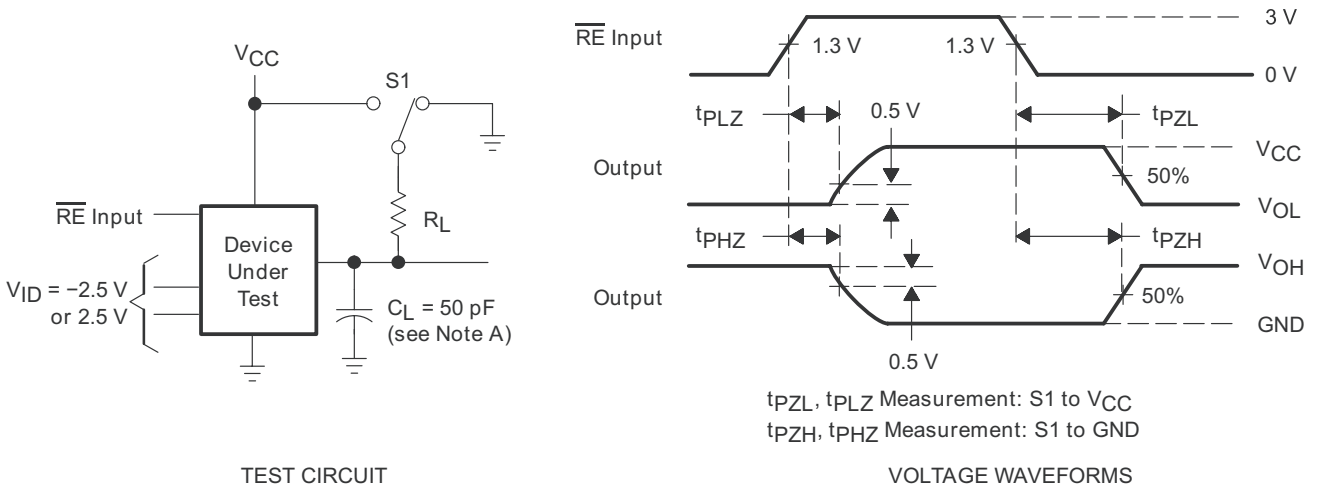
- A. C1, C2, and C3 include probe and jig capacitance.
- B. The input pulse is supplied by a generator having the following characteristics: PRR = 1MHz, 50% duty cycle,  $t_r = t_f \leq 6\text{ns}$ .

**Figure 6-4. Driver Test Circuit and Voltage Waveforms**



- A.  $C_L$  includes probe and jig capacitance.
- B. The input pulse is supplied by a generator having the following characteristics: PRR = 1MHz, 50% duty cycle,  $t_r = t_f \leq 6\text{ns}$ .

**Figure 6-5. Receiver Test Circuit and Voltage Waveforms**

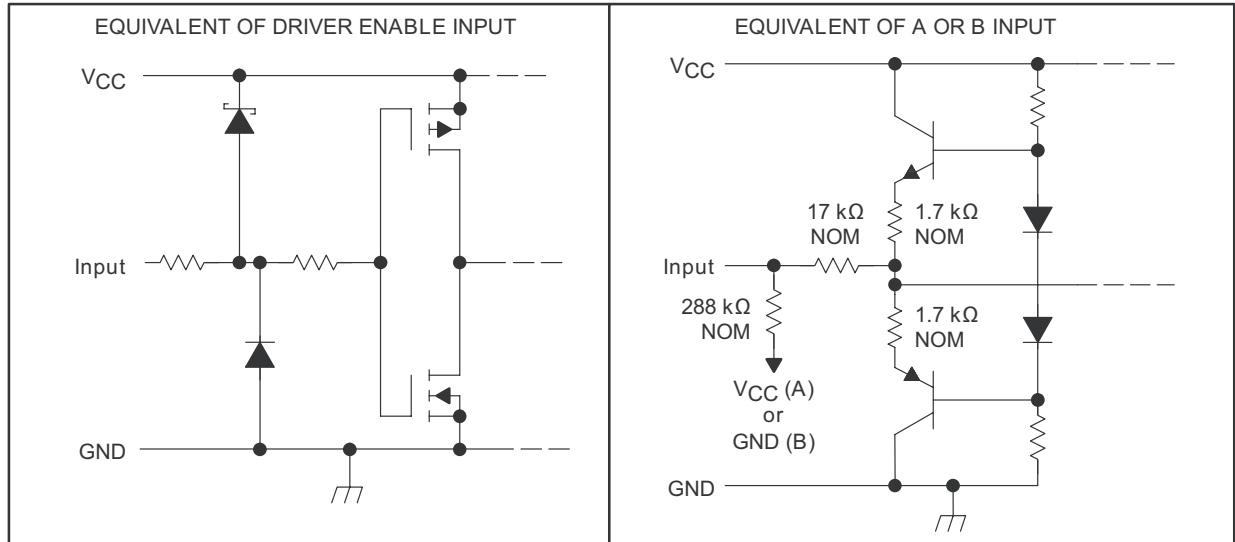


- A.  $C_L$  includes probe and jig capacitance.
- B. The input pulse is supplied by a generator having the following characteristics: PRR = 1MHz, 50% duty cycle,  $t_r = t_f \leq 6\text{ns}$ .

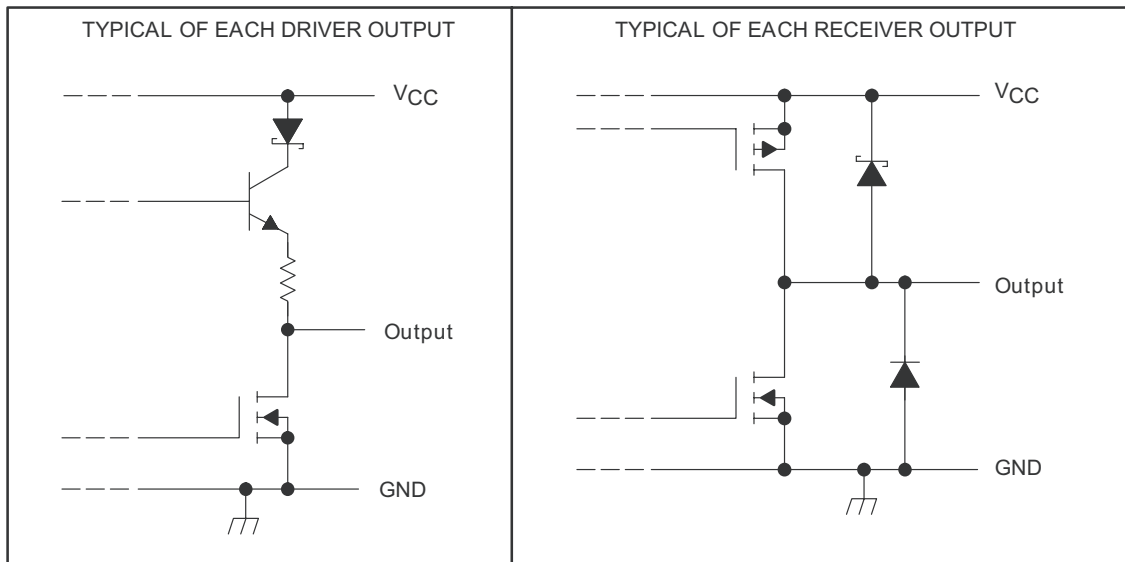
**Figure 6-6. Receiver Test Circuit and Voltage Waveforms**

## 7 Detailed Description

### 7.1 Functional Block Diagram



**Figure 7-1. Schematic of Inputs**



**Figure 7-2. Schematic of Outputs**

## 7.2 Device Functional Modes

### 7.2.1 Functions Table

**Table 7-1. Each Driver<sup>(1)</sup>**

INPUT D	ENABLE DE	OUTPUTS	
		Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

(1) H = high level, L = low level, X = irrelevant, Z = high impedance

**Table 7-2. Each Receiver<sup>(1)</sup>**

DIFFERENTIAL INPUTS A – B	ENABLE RE	OUTPUT R
$V_{ID} \geq 0.2\text{ V}$	L	H
$-0.2\text{ V} < V_{ID} < 0.2\text{ V}$	L	?
$V_{ID} \leq -0.2\text{ V}$	L	L
X	H	Z
Open	L	H

(1) H = high level, L = low level, ? = indeterminate, X = irrelevant,  
 Z = high impedance (off), Open = input disconnected or connected driver off

## 8 Device and Documentation Support

### 8.1 Documentation Support

### 8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 8.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.  
All trademarks are the property of their respective owners.

### 8.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 8.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision F (November 2009) to Revision G (February 2024)</b>	<b>Page</b>
• Changed the numbering format for tables, figures, and cross-references throughout the document.....	1
• Changed the I <sub>CC</sub> for V <sub>I</sub> = 2.4 or 0.5V MAX value From: 3mA To: 9mA in the <i>Electrical Characteristics, Driver Section</i> .....	6

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65C1167NSR	LIFEBUY	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C1167	
SN65C1167NSRG4	LIFEBUY	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C1167	
SN65C1168NSR	LIFEBUY	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C1168	
SN65C1168PW	LIFEBUY	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB1168	
SN65C1168PWG4	LIFEBUY	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB1168	
SN65C1168PWR	LIFEBUY	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB1168	
SN75C1167DB	LIFEBUY	SSOP	DB	16	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		CA1167	
SN75C1167DBR	ACTIVE	SSOP	DB	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	CA1167	Samples
SN75C1167NSR	LIFEBUY	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75C1167	
SN75C1167NSRG4	LIFEBUY	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75C1167	
SN75C1168DBR	ACTIVE	SSOP	DB	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	CA1168	Samples
SN75C1168NSR	LIFEBUY	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75C1168	
SN75C1168NSRG4	LIFEBUY	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75C1168	
SN75C1168PW	LIFEBUY	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	CA1168	
SN75C1168PWR	LIFEBUY	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	CA1168	
SN75C1168PWRG4	LIFEBUY	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	CA1168	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

- (3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65C1167NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN65C1168NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN65C1168PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN75C1167DBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN75C1167NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN75C1168DBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN75C1168NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN75C1168PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1



**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65C1167NSR	SO	NS	16	2000	356.0	356.0	35.0
SN65C1168NSR	SO	NS	16	2000	356.0	356.0	35.0
SN65C1168PWR	TSSOP	PW	16	2000	356.0	356.0	35.0
SN75C1167DBR	SSOP	DB	16	2000	356.0	356.0	35.0
SN75C1167NSR	SO	NS	16	2000	356.0	356.0	35.0
SN75C1168DBR	SSOP	DB	16	2000	356.0	356.0	35.0
SN75C1168NSR	SO	NS	16	2000	367.0	367.0	38.0
SN75C1168PWR	TSSOP	PW	16	2000	356.0	356.0	35.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN65C1168PW	PW	TSSOP	16	90	530	10.2	3600	3.5
SN65C1168PWG4	PW	TSSOP	16	90	530	10.2	3600	3.5
SN75C1167DB	DB	SSOP	16	80	530	10.5	4000	4.1
SN75C1168PW	PW	TSSOP	16	90	530	10.2	3600	3.5



# PACKAGE OUTLINE

## NS0016A

### SOP - 2.00 mm max height

SOP



#### NOTES:

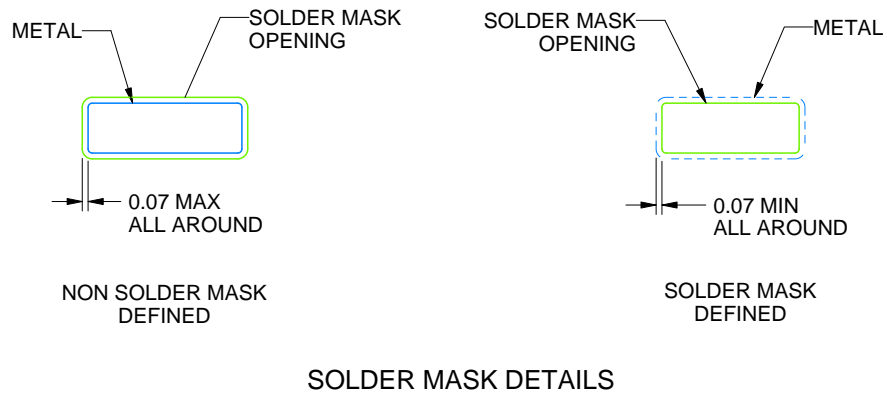
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

# EXAMPLE BOARD LAYOUT

NS0016A

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.



4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



# DB0016A



# PACKAGE OUTLINE

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4220763/A 05/2022

### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220763/A 05/2022

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220763/A 05/2022

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

## MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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