Photonic circuits for on-chip quantum optics

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Introduction

Quantum optics is a rapidly developing field where single photons can be used in applications such as secure communication, simulation of complex quantum systems, and universal quantum computing. So far, experiments in this field have mainly been done using bulk optics, i.e. with optical tables full of lenses, mirrors, and other components. This approach is not very scalable towards more advanced experiments as the alignment, stabilization, and required space of the optical tables become increasingly impractical. However, these problems can be circumvented using integrated optics, and we pursue this on-chip approach with the help of a Raith EBPG5000+ [1,2].

On-chip quantum optics

In the linear quantum optics approach, quantum information is encoded on single photons that act as qubits [3]. On a chip, the most natural way of doing this is by using "dual-rail encoding". Imagine two optical waveguides: when a single photon travels through the first, it represents the logical "0" state, whereas a single photon in the other waveguide is "1". Interestingly, by using a Y-splitter there is an equal chance of detecting the photon in either of the two output waveguides, and thus a superposition of 0 and 1 is created. In general, any unitary quantum operation on a single qubit can be implemented by sending the photons through well-designed photonic circuits consisting of directional couplers and segments with relative length differences. Two-qubit operations can also be performed, but in linear optics quantum computing these are non-deterministic processes. By detecting the photons, a post-selection of the outcomes of the experiment can be made; this implements an effective interaction between pairs of photons. This is at the heart of the famous "KLM scheme" [4]. Photon detection should happen at the highest possible efficiency. Hence, to prevent interconnect loss it is imperative to integrate the detectors on the same chip as the photonic circuits. Detectors with the best quantum efficiency are made out of very narrow superconducting wires [5]. These devices momentarily switch to the normal state upon absorbing a photon, resulting in a measurable voltage pulse. Whenever superconductors are used, the chip has to be cooled to very low temperatures. To keep the chip cold, the amount of heat dissipated on it must be limited. For this reason we use electrostatically controlled phase shifters to make our quantum circuits programmable.

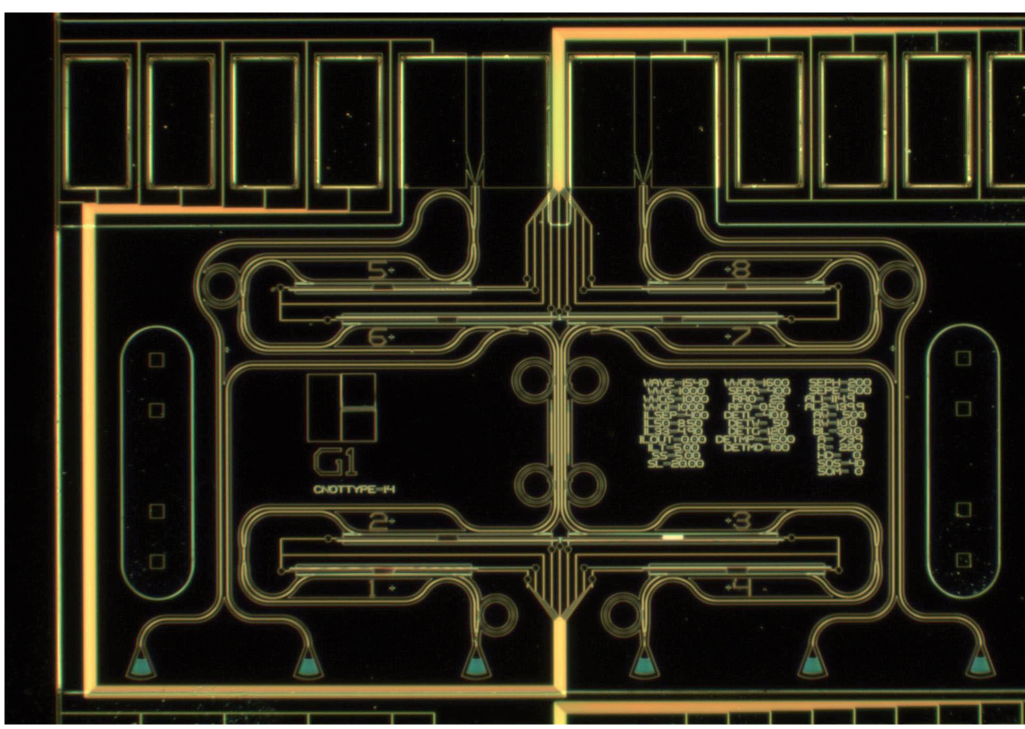

Figure 1: Dark field micrograph of a device for a controlled NOT quantum operation. Grating couplers (blue triangles) are used to get single photons on the chip. The quantum operation is implemented using photonic circuits with directional couplers. Each individual device, such as the one shown here, measures 1.5 by 1 mm.

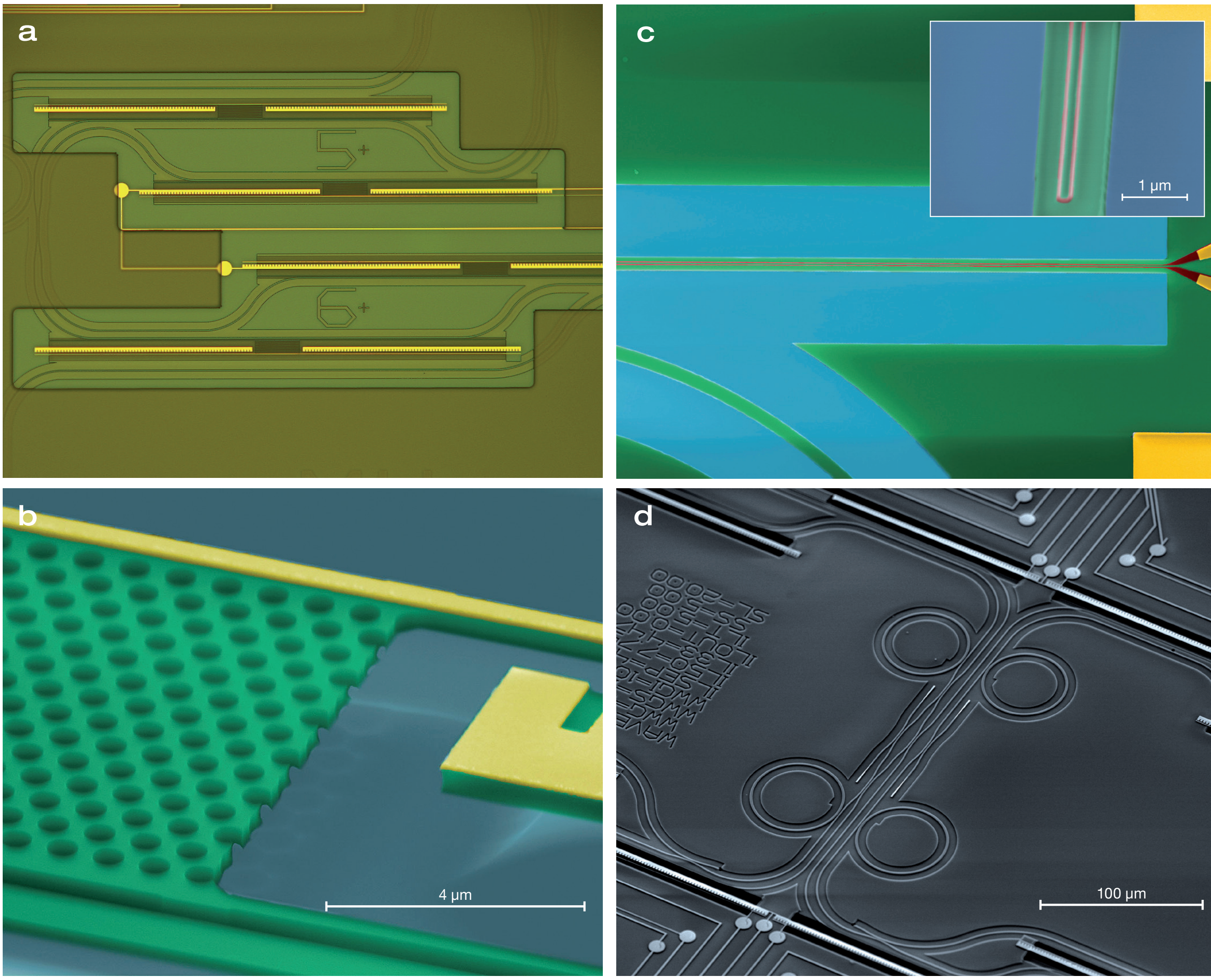

Figure 2: Details of our integrated quantum optical devices. (a) Etch windows for releasing the optoelectromechanical phase shifters. The photoresist protects the superconducting single-photon detectors from the etchant. (b) Zoom of an "H" phase shifter. The electrodes are yellow, the released device and waveguide are green, and the silicon oxide (as well as a very thin layer of SiN) is indicated in blue. (c) Optical waveguide with an SSPD (red) on top. The inset shows the apex and alignment on the waveguide. (d) Bird's eye view oft he CNOT circuit. The rings are used to determine the relative optical phases in the as-fabricated circuits [7]. Four of the eight phase shifters are partly visible.

These MEMS devices do not dissipate any heat and work well at cryogenic temperatures [6]. Figure 1 shows an overview of a finished chip with various elements highlighted in Figure 2.

Fabrication process

Given the many different technologies that are combined when making the chips (i.e. photonics, superconductors, MEMS), more than six lithography steps are needed. Two of these use standard photolithography, whereas the others are done with electron-beam lithography. For this, a Raith EBPG5000+ was used. The starting point is an Si wafer with thermally grown SiO_2 and an LPCVD Si_3N_4 layer. The former serves as a cladding, with the optical circuits and movable parts implemented in the silicon nitride. This material has excellent optical and mechanical properties. A few nm of NbTiN are sputtered on top of the material; these thin films become superconducting around 11 K. In the first step, electrodes and alignment markers are defined. Then the superconducting detectors are written and etched. In the next two steps, the SiN is patterned using reactive-ion etching. A thin layer of SiN remains in the first step, while the second etches all the way into the underlying oxide. Now the mechanical structures are released by immersing the chip in buffered hydrofluoric acid, followed by critical point drying.

Lithography challenges

Writing these complex circuits raises many challenges in e-beam lithography, which can be met with state-of-the-art equipment such as the EBPG5000+.

Proximity effect correction

The metal layer is the first to be written on the chip, and since both large (190x90 µm) contact pads and fine features such as the narrow (as little as 125 nm) gap between the fixed and movable electrodes are involved, different beam currents are used. The exposure is optimized using proximity effect correction to prevent overexposure (Figure 3).

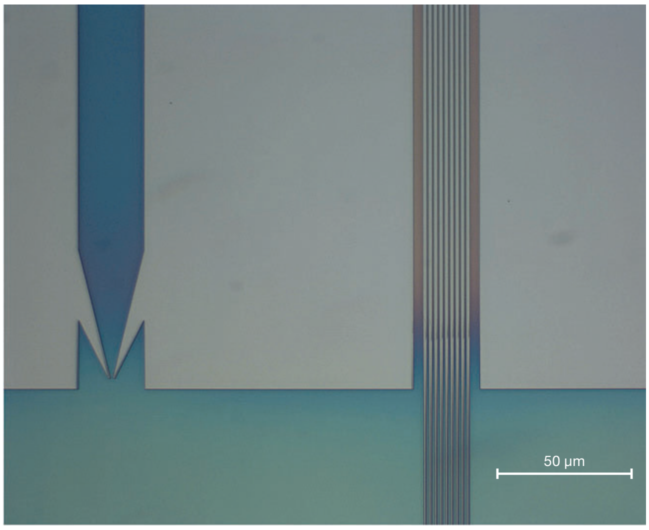

Figure 3: Micrograph of developed PMMA, which was written without proximity effect correction. The nine narrow electrodes required to actuate the phase shifters are overexposed in the region between the large contact pads.

Stitching

The size of the individual devices exceeds the largest write field of the EBPG5000+, meaning that stitching is inevitable. Even at the largest field sizes, EBPG stitching artefacts can be minimized or even completely removed by using built-in techniques and/or data processing.

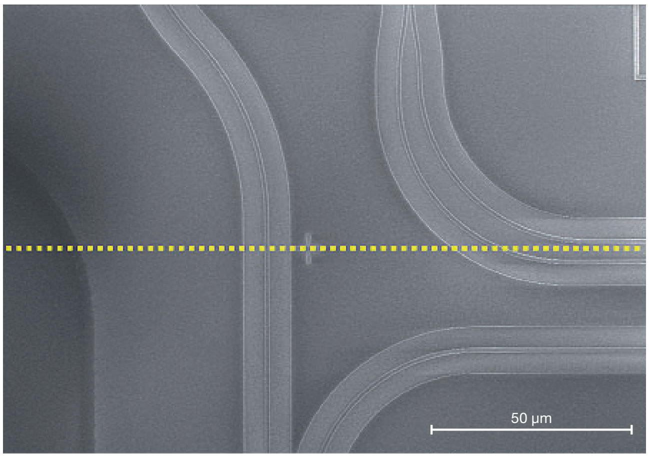

Figure 4: Micrograph of a waveguide that crosses the boundary between two write fields (indicated by the dotted line). The EBPG shows excellent stitching, which is specified as < 15 nm.

Overlay

Another important aspect is the relative placement of all the different layers. The metallic markers are essential. As illustrated in Fig. 5, we protect these with a cover of SU-8 which is patterned using photolithography. This protection is essential to achieve accurate overlay of the different layers.

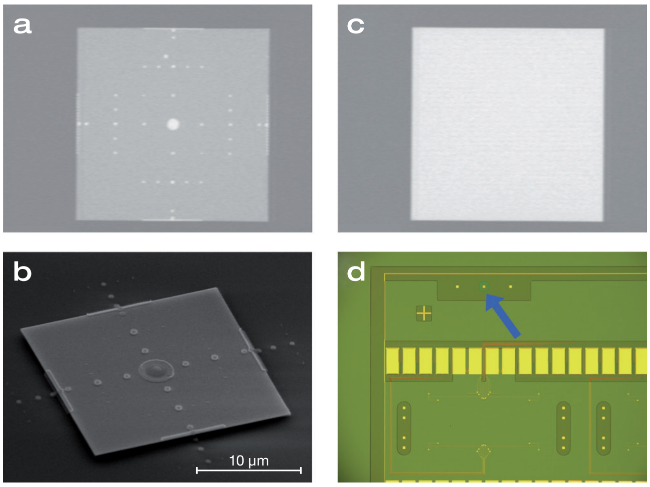

Figure 5: Markers after etching through the SiN. The top row shows the images as acquired using the integrated BSE detector of the EBPG5000+. The left two panels are markers without protection. Redeposited gold (b) creates regions with high electron scattering [bright spots in (a)] that prevent accurate marker recognition. With SU-8 protection (c, d), the marker remains unaffected (c), resulting in good overlay. The optical micrograph in (d) shows the markers underneath the SU-8 protection; the marker indicated by the arrow was exposed.

High resolution for SSPDs

Another lithography challenge is writing the single-photon detectors. When a photon is absorbed in U-shaped nanowire made out of patterned NbTiN [see Figure 2(d)], it momentarily breaks the super-conductivity. This is only possible when the wire is very thin and narrow. The thickness is set by the film deposition and is typically 4-8 nm. The width, however, is set by the lithography. Nanowires as narrow as 30 nm were successfully fabricated using high-resolution HSQ resist and small beam step size. Moreover, the flexibility of e-beam lithography allows the effects of the detector geometry on aspects such as its quantum efficiency to be studied.

Smooth waveguides

Finally, small beam step sizes result in smooth waveguides. With relatively little effort, we obtained propagation losses of 1.5 dB/cm [2]. This can be improved by using even smaller resolutions, or by reflowing the ZEP 520A e-beam resist after developing it. Both will result in smoother waveguides with even lower scattering loss.

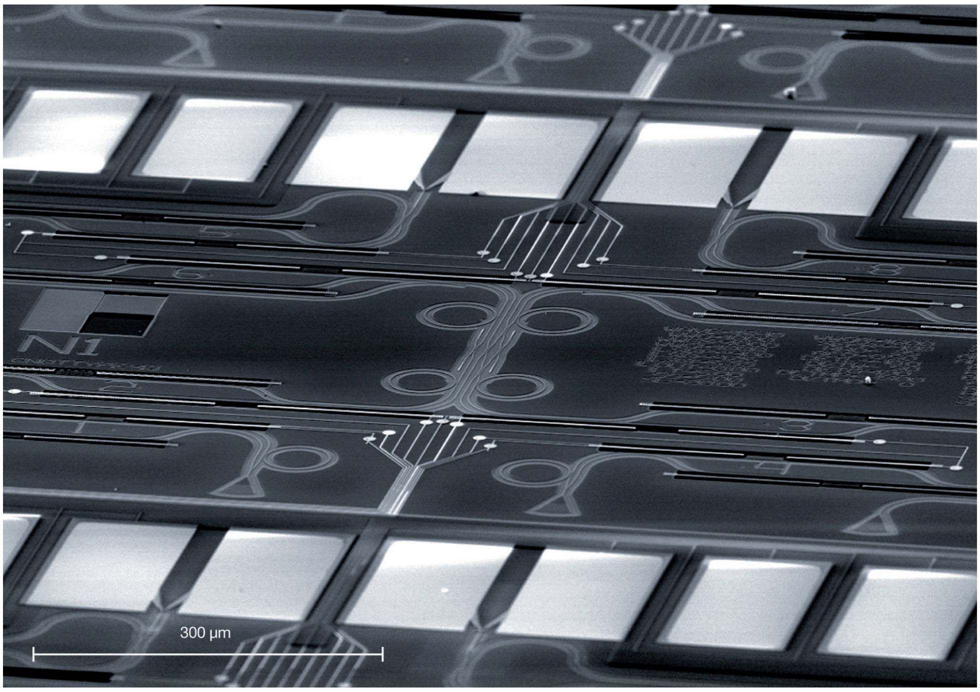

Figure 6: Overview of an integrated optical quantum device after the final fabrication step

Conclusion and outlook

The Raith EBPG5000+ is an indispensable tool for the nanofabrication of our integrated photonic circuits. Its good overlay using automated marker search and alignment allows accurate placement of the different lithography steps. Flexible writing strategies are enabled by the ease of switching resolutions and beam currents, as well as the support of PEC. This is done intuitively with the help of the graphical Cjob and Cview utilities that are supplied with the EBPG. Currently, we are working on further optimization of all the individual components made on the chips and their characterization at cryogenic temperature. The next step will be to send non-classical light such as single photons into these exciting devices, and to design and produce more complex optical quantum circuits.

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