

## DS3662

### Quad High Speed Trapezoidal™ Bus Transceiver

#### General Description

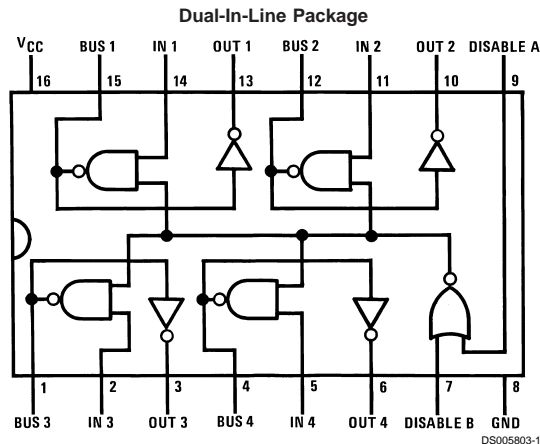
The DS3662 is a quad high speed Schottky bus transceiver intended for use with terminated 120Ω impedance lines. It is specifically designed to reduce noise in unbalanced transmission systems. The open collector drivers generate precise trapezoidal waveforms with rise and fall times of 15 ns (typical), which are relatively independent of capacitive loading conditions on the outputs. This reduces noise coupling to the adjacent lines without any appreciable impact on the maximum data rate obtainable with high speed bus transceivers. In addition, the receivers use a low pass filter in conjunction with a high speed comparator, to further enhance the noise immunity. Tightly controlled threshold levels on the receiver provide equal rejection to both negative and positive going noise pulses on the bus.

The external termination is intended to be a 180Ω resistor from the bus to 5V logic supply, together with a 390Ω resistor from the bus to ground. The bus can be terminated at one or both ends. A two input NOR gate is provided to disable all drivers in a package simultaneously.

#### Features

- Pin to pin functional replacement for DS8641
- Guaranteed AC specifications on noise immunity and propagation delay over the specified temperature and supply voltage range
- Temperature insensitive receiver thresholds track bus logic level
- Trapezoidal bus waveforms reduce noise coupling to adjacent lines
- Precision receiver thresholds provide maximum noise immunity and symmetrical response to positive and negative going pulses
- Open collector driver output allows wire-OR connection
- High speed Schottky technology
- 15 μA typical bus termination current with normal  $V_{CC}$  or with  $V_{CC} = 0V$
- Glitch free power up/down protection on the driver output
- TTL compatible driver and disable inputs, and receiver outputs

#### Block and Connection Diagram



Top View

Order Number DS3662J, DS3662N or DS3662WM  
See NS Package Number J16A, N16A or M16B

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## Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input and Output Voltage	5.5V
Storage Temperature Range	-65°C to +150°C
Maximum Power Dissipation (Note 1) at 25°C	
Cavity Package	1509 mW
Molded Package	1476 mW

Lead Temperature (Soldering, 4 sec.)

260°C

## Recommended Operating Conditions

	Min	Max	Units
Supply Voltage ( $V_{CC}$ )	4.75	5.25	V
Temperature Range ( $T_A$ )	0	70	°C

**Note 1:** Derate cavity package 10.1 mW/°C above 25°C; derate molded package 11.8 mW/°C above 25°C.

## Electrical Characteristics (Notes 3, 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>DRIVER AND DISABLE INPUTS</b>						
$V_{IH}$	Logical "1" Input Voltage		2.0			V
$V_{IL}$	Logical "0" Input Voltage				0.8	V
$I_I$	Logical "1" Input Current	$V_{IN} = 5.5V$			1	mA
$I_{IH}$	Logical "1" Input Current	$V_{IN} = 2.4V$			40	µA
$I_{IL}$	Logical "0" Input Current	$V_{IN} = 0.4V$		-1	-1.6	mA
$V_{CL}$	Input Diode Clamp Voltage	$I_{CLAMP} = -12\text{ mA}$		-0.8	-1.5	V
<b>DRIVER OUTPUT/RECEIVER INPUT</b>						
$V_{OLB}$	Low Level Bus Voltage	$V_{DIS} = 0.8V, V_{IN} = 2V, I_{BUS} = 100\text{ mA}$		0.6	0.9	V
$I_{IHB}$	Maximum Bus Current	$V_{IN} = 0.8V, V_{BUS} = 4V, V_{CC} = 5.25V$		10	100	µA
$I_{ILB}$	Maximum Bus Current	$V_{IN} = 0.8V, V_{BUS} = 4V, V_{CC} = 0V$			100	µA
$V_{IH}$	High Level Receiver Threshold	$V_{IN} = 0.8V, V_{OL} = 16\text{ mA}$	1.90	1.70		V
$V_{IL}$	Low Level Receiver Threshold	$V_{IN} = 0.8V, I_{OH} = -400\text{ µA}$		1.70	1.50	V
<b>RECEIVER OUTPUT</b>						
$V_{OH}$	Logical "1" Output Voltage	$V_{IN} = 0.8V, V_{BUS} = 0.5V, I_{OH} = -400\text{ µA}$	2.4	3.2		V
$V_{OL}$	Logical "0" Output Voltage	$V_{IN} = 0.8V, V_{BUS} = 4V, I_{OL} = 16\text{ mA}$		0.35	0.5	V
$I_{OS}$	Output Short Circuit Current	$V_{DIS} = 0.8V, V_{IN} = 0.8V, V_{BUS} = 0.5V, V_{OS} = 0V, V_{CC} = 5.25V, (\text{Note } 5)$	-40	-70	-100	mA
$I_{CC}$	Supply Current	$V_{DIS} = 0V, V_{IN} = 2V$		50	90	mA

## Switching Characteristics (Notes 3, 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>PROPAGATION DELAYS</b>						
$t_{PLHD}$	Disable to Bus "1"	Figure 1		25	35	ns
$t_{PHLD}$	Disable to Bus "0"			25	35	ns
$t_{PLHB}$	Driver Input to Bus "1"	Figure 2		20	30	ns
$t_{PHLB}$	Driver Input to Bus "0"			20	30	ns
$t_{PLHR}$	Bus to Logical "1" Receiver Output	Figure 3		25	40	ns
$t_{PHLR}$	Bus to Logical "0" Receiver Output			25	40	ns
<b>NOISE IMMUNITY</b>						
$t_{rB}, t_{fB}$	Rise and Fall Times (10%–90%) of the Driver Output	Figure 2	10	15	20	ns
$t_{nR}$	Receiver Noise Rejection Pulse Width	No Response at Receiver Output as per Figure 4		20	10	ns

**Note 2:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" and "Recommended Operating Conditions" provide conditions for actual device operation.

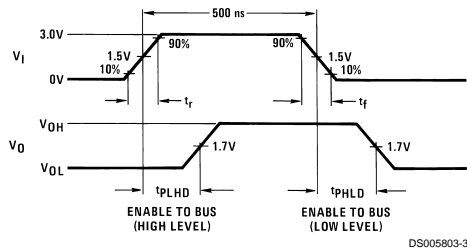
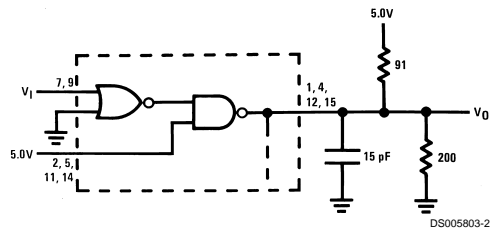
**Note 3:** Unless otherwise specified min/max limits apply across the supply and temperature range listed in the table of "Recommended Operating Conditions". All typical values are for  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 5V$ .

**Note 4:** All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

## Switching Characteristics (Notes 3, 4) (Continued)

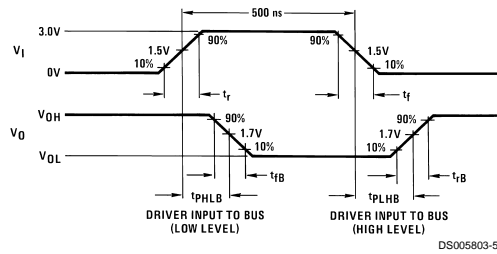
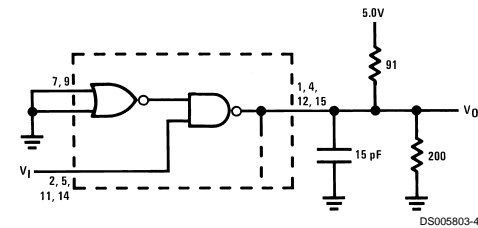
**Note 5:** Only one output at a time should be shorted.

### AC Test Circuits and Switching Waveforms



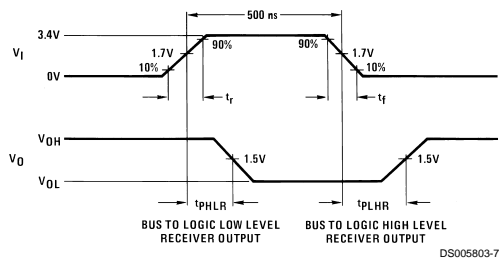
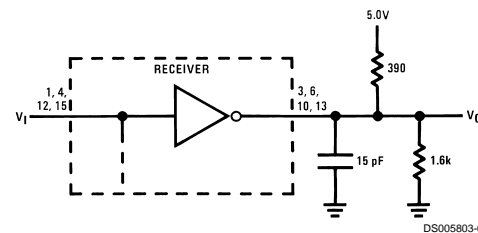
**Note:**  $t_r = t_f = 2.5$  ns. Pulse width = 500 ns measured between 1.5V levels.  $f = 1$  MHz.

**FIGURE 1. Disable Delays**



**Note:**  $t_r = t_f = 2.5$  ns. Pulse width = 500 ns measured between 1.5V levels.  $f = 1$  MHz.

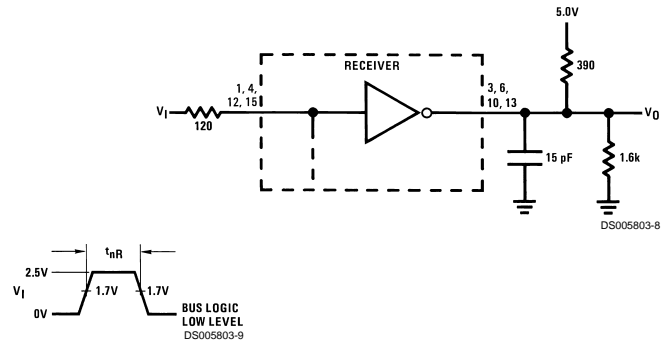
**FIGURE 2. Driver Propagation Delays**



**Note:**  $t_r = t_f = 15$  ns. Pulse width = 500 ns measured between 1.7V levels.  $f = 1$  MHz.

**FIGURE 3. Receiver Propagation Delays**

## AC Test Circuits and Switching Waveforms (Continued)



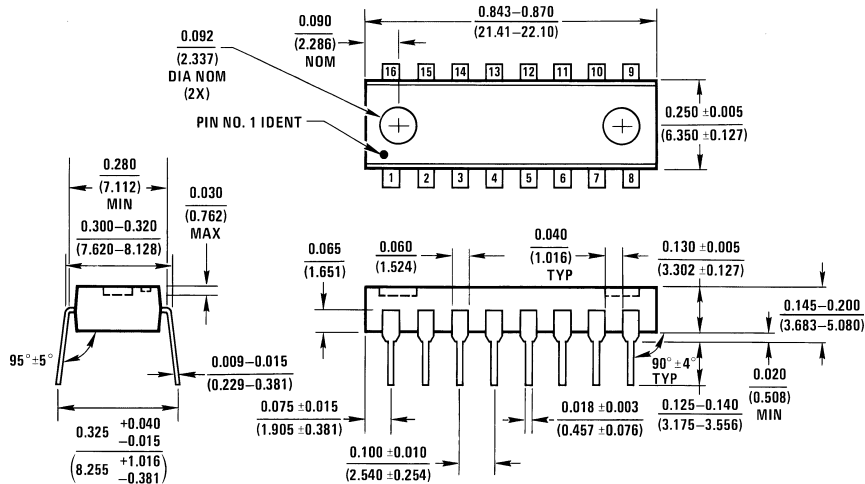
$$t_r = t_f = 2.5 \text{ ns}$$

(a) Receiver Output ( $V_O$ )

## Typical Application



**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



N16A (REV E)

**Molded Dual-In-Line Package (N)**  
**Order Number DS3662N**  
**NS Package Number N16A**

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



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