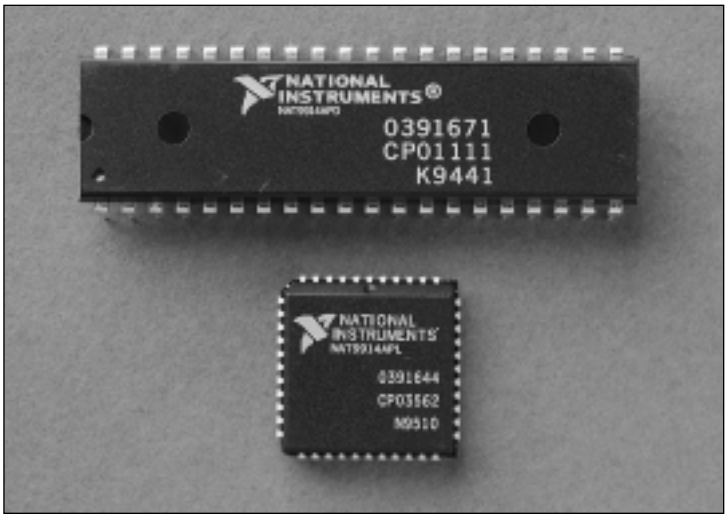
IEEE 488.2 Controller Chip
Drop-In Replacement for TI TMS9914A

NAT9914APD
NAT9914APL

Features

- Pin compatible with TI TMS9914A
- Software compatible with NEC µPD7210 or TI TMS9914A controller chips
- Low power consumption
- Meets all IEEE 488.2 requirements
  - – Bus line monitoring
  - – Preferred implementation of requesting service
  - – Will not send messages when there are no Listeners
- Performs all IEEE 488.1 interface functions
- Programmable data transfer rate (T1 delays of 350 ns, 500 ns, 1.1 µs, and 2 µs)
- Automatic EOS and/or NL message detection
- Direct memory access (DMA)
- Automatically processes IEEE 488 commands and reads undefined commands
- TTL-compatible CMOS device
- Programmable clock rate up to 20 MHz
- Reduces driver overhead
  - – Does not lose a data byte if ATN is asserted while transmitting data



NAT9914

Description

The NAT9914 IEEE 488.2 controller chip can perform all the interface functions defined by that the IEEE Standard 488.1-1987, and also meets the additional requirements and recommendations of the IEEE Standard 488.2-1987. Connected between the processor and the IEEE 488 bus, the NAT9914 provides high-level management of the IEEE 488 bus, significantly increases the throughput of driver software, and simplifies both the hardware and software design. The NAT9914 performs complete IEEE 488 Talker, Listener, and Controller functions. In addition to its numerous improvements, the NAT9914 is also completely pin compatible with the TI TMS 9914A and software compatible with the NEC µPD7210 and TI TMS9914A controller chips.

IEEE 488.2 Overview

The IEEE 488.2 standard removes the ambiguities of IEEE 488.1 by standardizing the way instruments and controllers operate. It defines data formats, status reporting, error handling, and common configuration commands to which all IEEE 488.2 instruments must respond in a precise manner. It also defines a set of controller requirements. The benefits of IEEE 488.2 for the test system developer are reduced development time and cost, because systems are more compatible and reliable. The NAT9914 brings the full power of IEEE 488.2 to the design engineer along with numerous other design and performance benefits, while retaining the 40-pin and 44-pin hardware configurations of the TI TMS 9914A.

General

The NAT9914 manages the IEEE 488 bus. You program the IEEE 488 bus by writing control words into the appropriate registers. CPU-readable status registers supply operational feedback. The NAT9914 mode determines the function of these registers. On power up or reset, the NAT9914 registers resemble the TMS9914A register set with additional registers that supply extra functionality and IEEE 488.2 compatibility. In this mode, the NAT9914 is completely pin compatible with the TI TMS9914A. If you enable the 7210 mode, the registers resemble the NEC µPD7210 register set with additional registers that supply extra functionality and IEEE 488.2 compatibility. This mode is not pin compatible with the NECµPD7210. Figure 2 shows the key components of the NAT9914.

Note: For more details about the NAT9914 see the NAT9914 Reference Manual, Part Number 320775-01.

NATIONAL INSTRUMENTS®
The Software is the Instrument®

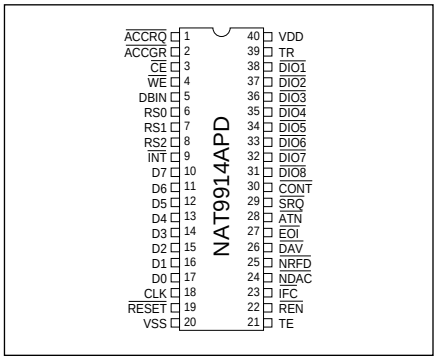


Figure 1. NAT9914APD Pin Configuration

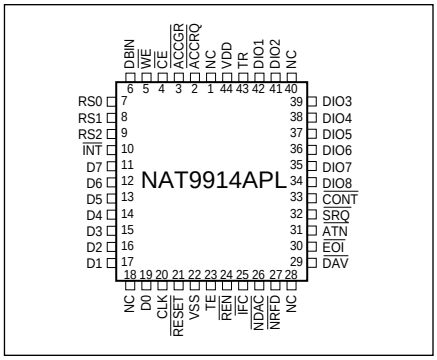


Figure 2. NAT9914APL Pin Configuration

Pin Identification

Pin No.		Mnemonic	Type	Description
PLCC	**DIP**			
11, 12, 13, 14, 15, 16, 17, 19	10, 11, 12, 13, 14, 15, 16, 17	D(7-0)	I/O†	Bidirectional 3-state data bus transfers commands, data, and status between the NAT9914 and the CPU. D0 is the most significant bit.
4	3	CE*	I	Chip Enable gives access to the register selected by a read or write operation, and the register selects RS(2-0)
6	5	DBIN	I†	With the Data Bus Input, you can place the contents of the register selected by RS(2-0) and CE* onto the data bus D(7-0). The polarity of DBIN is reversed for DMA operation.
5	4	WE*	I†	The Write input latches the contents of the data bus D(7-0) into the register selected by RS(2-0)
3	2	ACCGR*	I†	The Access Grant signal selects the DIR or CDOR for the current read or write cycle
2	1	ACCRQ*	O	The Access Request output asserts to request a DMA Acknowledge cycle
20	18	CLK	I†	The CLK input can be up to 20 MHz
21	19	RESET*	I†	Asserting the RESET* input places the NAT9914 in an initial, idle state
10	9	INT*	0 (0C)	The Interrupt output asserts when one of the unmasked interrupt conditions is true. The NAT9914 does not drive INT* high. The INT* pin must be pulled up by an external resistor.
9, 8, 7	8, 7, 6	RS(2-0)	I†	The Register Selects determine which register to access during a read or write operation
25	23	IFC*	I/O†,†† (OC)	Bidirectional control line initializes the IEEE 488 interface functions
24	22	REN*	I/O† (OC)	Bidirectional control line selects either remote or local control of devices
31	28	ATN*	I/O†	Bidirectional control line indicates whether data on the DIO lines is an interface or device-dependent message
32	29	SRQ*	I/O†	Bidirectional control line requests service from the controller
34, 35, 36, 37, 38, 39, 41, 42	31, 32, 33, 34, 35, 36 37, 38	DIO(8-1)*	I/O†	8-bit bidirectional IEEE 488 data bus
29	26	DAV*	I/O†	Handshake line indicates that the data on the DIO(8-1)* lines is valid
27	25	NRFD*	I/O†	Handshake line indicates that the device is ready for data
26	24	NDAC*	I/O†	Handshake line indicates the completion of a message reception
30	27	EOI*	I/O†	Bidirectional control line indicates the last byte of a data message or executes a parallel poll
23	21	TE	O†	Talk Enable controls the direction of the IEEE 488 data transceiver

Pin No.		Mnemonic	Type	Description
PLCC	DIP			
43	39	TR	O†	Trigger asserts when one of the trigger conditions is satisfied
33	30	CONT*	O†	Controller asserts when the NAT9914 is Controller-In-Charge
44	40	VDD	–	Power pin – +5 V (±5%)
22	20	VSS	–	Ground pin – 0 V
1, 18, 28, 40	–	NC	–	No connect

OC= Open collector.
† The pin contains an internal pull-up resistor of 25 kΩ to 100 kΩ.
* Active low.
†† In controller applications where the CLK signal frequency is > 8 MHz, IFC* should be pulled up with a 4.7 kΩ resistor.

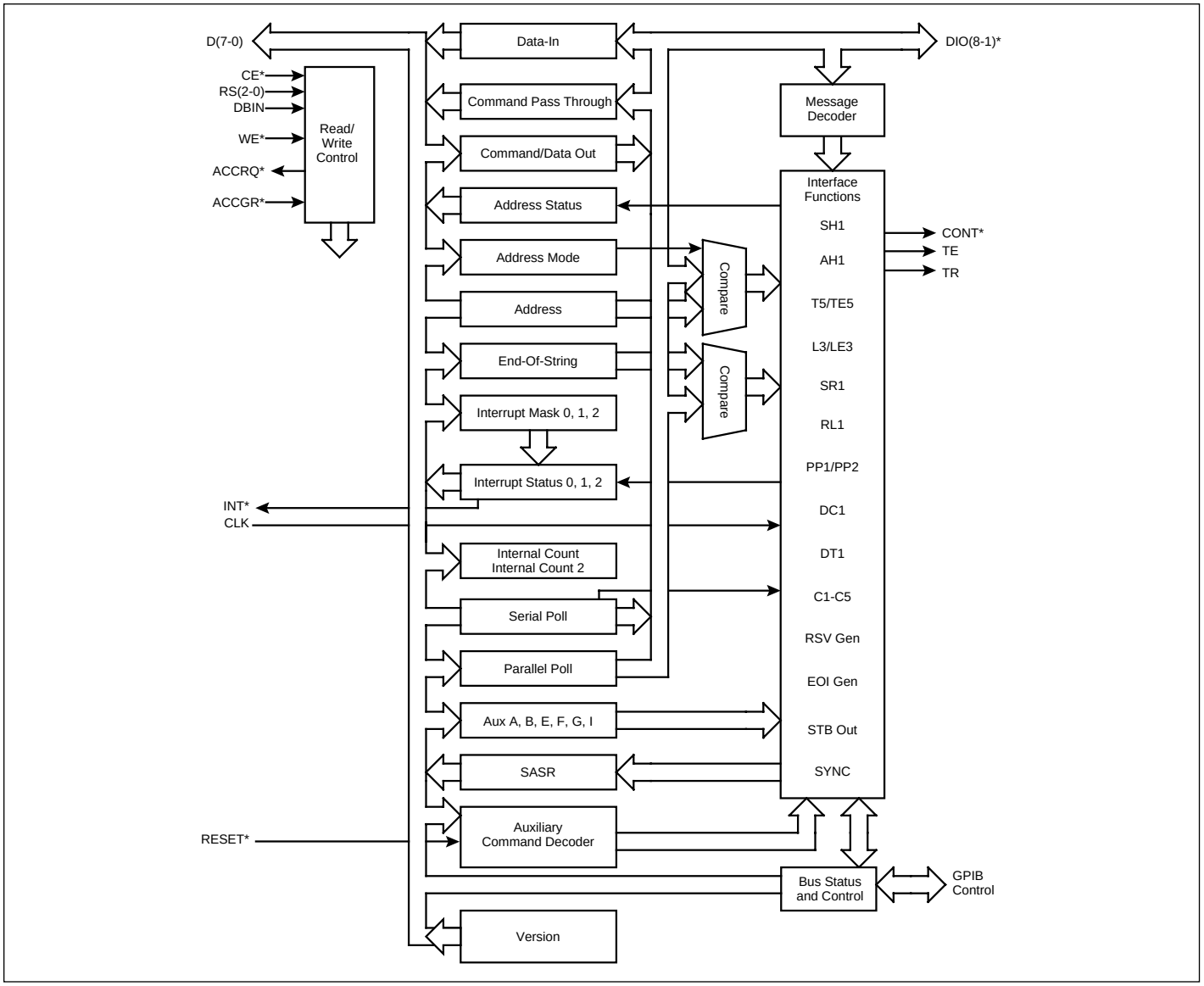


Figure 3. NAT9914 Block Diagram

9914 Mode Registers

In 9914 mode, the NAT9914 registers consist of all the TI TMS9914A registers and two types of additional registers – newly defined registers and paged-in registers. The NAT9914 maps the newly defined registers into the unused portion of the 9914 address space. Each paged-in register appears at offset 2 immediately after you issue an auxiliary page-in command, and it remains there until you page another register into the same space or you issue a reset. The table below lists all the registers in the 9914 register set.

9914 Register Set

Register	Page In	RS(2-0)	WE*	DBIN	CE*	ACCGR*
Interrupt Status 0	U	0 0 0	1	1	0	1
Interrupt Mask 0	U	0 0 0	0	0	0	1
Interrupt Status 1	U	0 0 1	1	1	0	1
Interrupt Mask 1	U	0 0 1	0	0	0	1
Address Status	U	0 1 0	1	1	0	1
Interrupt Mask 2†	P	0 1 0	0	0	0	1
End-of-String†	P	0 1 0	0	0	0	1
Bus Control†	P	0 1 0	0	0	0	1
Accessory†	P	0 1 0	0	0	0	1
Bus Status	U	0 1 1	1	1	0	1
Auxiliary Command	U	0 1 1	0	0	0	1
Interrupt Status 2†	P	1 0 0	1	1	0	1
Address	U	1 0 0	0	0	0	1
Serial Poll Status†	P	1 0 1	1	1	0	1
Serial Poll Mode	U	1 0 1	0	0	0	1
Command Pass Thru	U	1 1 0	1	1	0	1
Parallel Poll	U	1 1 0	0	0	0	1
Data-In	U	1 1 1	1	1	0	1
Data-In	U	X X X	X	0	X	0
Command/Data Out	U	1 1 1	0	0	0	1
Command/Data Out	U	X X X	0	1	X	0

The '†' symbol denotes features (such as registers and auxiliary commands) that are not available in the TMS9914A.

Notes for the PAGE-IN column

U = Page-in auxiliary commands do not affect the register offset.
P = The register offset is valid only after a page-in auxiliary command.

Data Registers

Data In Register (DIR)

DI08	DI07	DI06	DI05	DI04	DI03	DI02	DI01

Command/Data Out Register (CDOR)

DI08	DI07	DI06	DI05	DI04	DI03	DI02	DI01

The data registers transfer data and commands between the IEEE 488 bus and the CPU. The Data In Register (DIR) holds data sent from the GPIB to the CPU, and the CDOR holds information to transfer onto the IEEE 488 bus.

Interrupt Registers

Interrupt Status Register 0 (ISR0)

INT0	INT1	BI	BO	END	SPAS	RLC	MAC

Interrupt Status Register 1 (ISR1)

GET	ERR	UNC	APT	DCAS	MA	SRQ	IFC

Interrupt Status Register 2 (ISR2)†

nba	STBO	NL	EOS	LLOC	ATNI	X	CIC

Interrupt Mask Register 0 (IMR0)

DMAO†	DMAI†	BI IE	BO IE	END IE	SPAS IE	RLC IE	MAC IE

Interrupt Mask Register 1 (IMR1)

GET IE	ERR IE	UNC IE	APT IE	DCAS IE	MA IE	SRQ IE	IFC IE

Interrupt Mask Register 2 (IMR2)†

GLINT	STBO IE	NLEN	0	LLOC IE	ATNI IE	0	CIC IE

The interrupt registers consist of interrupt status bits, interrupt mask bits, and some noninterrupt-related bits. Several conditions can cause an interrupt. The interrupt status sets if its condition is true and an interrupt is generated if you set the corresponding mask bit. Most interrupt status bits are cleared when read. The following tables list the individual bits in the interrupt registers, along with descriptions.

Interrupt Status and/or Mask Register Bits

Bits	Description
INT0	OR of all unmasked ISR0 bits
INT1	OR of all unmasked ISR1 bits
BI	Byte In
BO	Byte Out
END	END (EOI or EOS message received)
SPAS	SPAS (Serial Poll Active State)
RLC	Remote/Local Change
MAC	My Address Change
GET	Group Execute Trigger
ERR	Data Transmission Error
UNC	Unrecognized Command
APT	Address Pass Through
DCAS	Device Clear Active State
MA	My Address
SRQ	Service Request (SRQ) asserted
IFC	Interface Clear (IFC) asserted
STBO†	Status Byte Out Request
LLOC†	Lockout State Change
ATNI†	Attention (ATN) asserted
CIC†	Controller-In-Charge
GLINT†	Global Interrupt Enable

Noninterrupt-Related, Readable Bits

Bits	Description
nba†	Command or Data Byte Available
NL†	New Line Received
EOS†	End-Of-String

Noninterrupt-Related, Writable Bits

Bits	Description
NLEN†	New Line character enabled for EOS
DMAO†	Enable/Disable DMA Out
DMAI†	Enable/Disable DMA In

Poll Registers

Serial Poll Status Register (SPSR)†

S8	PEND	S6	S5	S4	S3	S2	S1

Serial Poll Mode Register (SPMR)

S8	rsv/RQS	S6	S5	S4	S3	S2	S1

The Serial Poll Mode Register holds the STB (status byte: S8, S6 through S1) that transmits over the GPIB when you serial poll the NAT9914, and also holds the local rsv message (request service). The STB automatically transmits when you serial poll the NAT9914 if STBO IE=0. If STBO IE=1, the STB does not transmit during serial polls until you write to the SMPR. You can read the SPMR through the SPSR. The PEND bit sets when rsv sets and clears when the NAT9914 enters the Negative Poll Response State.

Parallel Poll Register (PPR)

PP8	PP7	PP6	PP5	PP4	PP3	PP2	PP1

The PPR contains the value that the NAT9914 outputs on the GPIB when the Controller-In-Charge conducts a parallel poll. To participate in a parallel poll, the bit corresponding to the desired parallel poll response is set to 1. The parallel poll register is double buffered. Therefore, if it is written during a parallel poll, the register updates with the new value at the end of the parallel poll.

Address Registers

The NAT9914 contains several registers that control the GPIB address mode, store the GPIB address, and monitor the GPIB address status.

Address Status Register (ADSR)

REM	LLO	ATN	LPAS	TPAS	LA	TA	ULPA

The Address Status Register monitors the NAT9914 address state. The following table lists the ADSR bits, along with a description of each bit.

Address Status Bits

Bit	Description
REM	The NAT9914 is in a Remote state
LLO	The NAT9914 is in a Lockout state
ATN	GPIB ATN signal
LPAS	Listener Primary Addressed State
TPAS	Talker Primary Addressed State
LA	Listener Addressed
TA	Talker Addressed
ULPA	Stores the LSB of the last address recognized by the NAT9914

Address Register (ADR)

EDPA	DAL	DAT	A5	A4	A3	A2	A1

The NAT9914 can automatically detect the address in ADR as its MTA or MLA. The following table describes the function of each bit.

Address Register Bits

Bit	Description
EDPA	Enables Dual Addressing mode, in which the least significant address bit is ignored, giving the NAT9914 two consecutive GPIB addresses
DAL	Prohibits the Listen address from being detected
DAT	Prohibits the Talk address from being detected
A5-0	GPIB primary address

Other Registers

Command Pass Through Register (CPTR)

CPT7	CPT6	CPT5	CPT4	CPT3	CPT2	CPT1	CPT0

With the Command Pass Through Register (CPTR), the CPU can read the GPIB DIO(8-1) lines in the cases of undefined commands, secondary addresses, or parallel poll responses.

End-Of-String Register† (EOSR)

EOS7	EOS6	EOS5	EOS4	EOS3	EOS2	EOS1	EOS0

The EOS Register holds either the seven or eight-bit EOS message byte that the GPIB system uses to detect the end of a data block.

Auxiliary Command Register

C/S	0	0	F4	F3	F2	F1	F0

A write to this register generates one of the following operations according to the C/S and F (4-0) values.

Auxiliary Commands

Hex values	Command	Operation
00/80	swrst	Clear/Set software reset
01/81	dacr	Invalid/valid DAC release Holdoff
02	rhdf	Release RFD Holdoff
03/83	hdfa	Clear/Set Holdoff on All Data
04/84	hdfe	Clear/Set Holdoff on END only
05	nbaf	New Byte Available False
06/86	fget	Clear/Set Force Group Execute Trigger
07/87	rtl	Clear/Set Return to Local

(continued)

Hex values	Command	Operation
08	feoi	Send EOI with next byte
09/89	lon	Clear/Set Listen Only
0A/8A	ton	Clear/Set Talk Only
OB	gts	Go To Standby
OC	tca	Take Control Asynchronously
OD	tcs	Take Control Synchronously
OE/8E	rpp	Clear/Set Request Parallel Poll
0F/8F	sic	Clear/Set Send Interface Clear
10/90	sre	Clear/Set Send Remote Enable
11	rqc	Request Control
12	rlc	Release Control
13/93	dai	Clear/Set Disable All Interrupts
14	pts	Pass Through Next Secondary
15/95	stdl	Clear/Set Short T1 settling time
16/96	shdw	Clear/Set Shadow Handshake
17/97	vstdl	Clear/Set Very Short T1 delay
18/98	rsv2	Clear/Set Request Service Bit 2
99	sw7210	Switch to µPD7210 Mode
1A	reqf	Send Reqf
9A	reqt	Send Reqt
1C	ch_rst	Chip Reset
9C	clrpi	Clear Page-In Registers
1D/9D	ist	Clear/Set Parallel Poll Flag
1E	piimr2	Page-In Interrupt Mask 2 Register
9E	pieosr	Page-In End-Of-String Register
1F	pibcr	Page-In Board Control Register
9F	piaccr	Page-In Accessory Register

Accessory Register† (ACCR)

ACC7	ACC6	ACC5	ACC4	ACC3	ACC2	ACC1	ACC0

The ACCR is a multipurpose register. A write to this register generates one of the following operations according to the ACC values.

Auxiliary Mode Operations

ACC 7	6	5	4	3	2	1	0	Operation
0	0	1	0	x	x	x	x	Writes to the Internal Counter Register†
1	0	0	x	x	x	0	0	Writes to the Accessory Register A
1	0	1	x	x	x	x	x	Writes to the Accessory Register B
1	1	0	0	x	x	0	0	Writes to the Accessory Register E
1	1	0	1	x	x	x	x	Writes to the Accessory Register F
1	1	0	0	x	x	x	x	Writes to the Accessory Register I

Internal Counter Register† (ICR)

0	0	1	0	T3	T2	T1	T0

The Internal Counter Register tells the internal circuitry in the NAT9914 the clock frequency supplied to the CLK input.

For proper operation, set T(3-0) and MICR as follows:

Clock Frequency	MICR	T(3-0)
1	0	0001
2	0	0010
3	0	0011
4	0	0100
5Δ	0	0101
6	0	0110
7	0	0111
8	0	1000
10	1	0101
16	1	1000
20	1	1010

ΔOn a hardware reset, T (3-0) and MICR are set to 5 MHz.
Note: MICR may be set by switching to the µPD7210 mode and writing to the ICR2 Register.

Accessory Register A† (ACCRA)

1	0	0	BIN	XEOS	REOS	0	0

Accessory Register A controls the usage of the EOS message, as listed in the table below.

EOS Message

Bit		Function
REOS	0 Prohibit 1 Permit	Permits (prohibits) setting END bit when receiving the EOS message
XEOS	0 Prohibit 1 Permit	Permits (prohibits) automatic transmission of END message simultaneously with EOS message transmission while in TACS
BIN	0 7-bit 1 8-bit	Selects 7 or 8 bits as the valid EOS message length

Accessory Registers B† (ACCRB)

1	0	1	ISS	INV	LWC	SPEOI	ATCT

Accessory Register B controls special NAT9914 operating features, as listed in the table below.

Special Features

Bit		Function
ATCT	0 Prohibit 1 Permit	Permits (prohibits) the NAT9914 to automatically take control of the GPIB when control is passed to it (TCT)
SPEOI	0 Prohibit 1 Permit	Permits (prohibits) END message transmission when in Serial Poll Active State (SPAS)
LWC	0 Prohibit 1 Permit	Permits (prohibits) the NAT9914 to accept and respond to the GPIB commands that it sources
INV	0 low 1 high	Specifies the INT* pin active level. The NAT9914 does not drive in INT* high. The INT* pin must be pulled up with an external resistor.
ISS	1 SRQS 0 Parallel Poll Flag	Determines if the ist local message value is equal to SRQS or the Parallel Poll Flag

Accessory Register E† (ACCRE)

1	1	0	0	DHADT	DHADC	0	0

Accessory Register F† (ACCRF)

1	1	0	1	DHATA	DHALA	DHUNTL	DHALL

AUXRE and AUXRF control DAC holdoff modes, as listed in the table below.

Special Features

Bit	Function
DHADC	DAC Holdoff on DCL or SDC
DHADT	DAC Holdoff on GET
DHALL	DAC Holdoff on all commands
DHUNTL	DAC Holdoff on UNL and UNT
DHALA	DAC Holdoff on all Listener addresses
DHATA	DAC Holdoff on all Talker addresses

Accessory Register I† (ACCRI)

1	1	1	0	USTD	PP1	0	DMAE

AUXRI controls special NAT9914 operational features, as listed in the table below.

Special Features

Bit	Function
DMAE=0	ACCRQ* is asserted if either a Byte In (BI) or Byte Out (BO) condition occurs
DMAE=1	ACCRQ* is asserted if the BI and DMAI bits are set or the BO and the DMAO bits are set
PP1	When set, the NAT9914 responds to remote GPIB parallel poll configure commands and automatically responds to parallel polls
USTD	Enables 350 ns T1 delays

GPIB Control/Status Registers† (BCR/BSR)

ATN	DAV	NDAC	NRFD	EOI	SRQ	IFC	REN

The CPU can monitor the GPIB by reading the Bus Status Register. You can assert (drive low) GPIB signals by setting the corresponding bit in the GPIB Control Register to 1.

7210 Mode Registers

The NAT9914 registers include all the NEC µPD7210 registers plus two types of additional registers – extra auxiliary registers and paged-in registers. You write the extra auxiliary registers the same as standard µPD7210 auxiliary registers. Upon issuing an auxiliary page-in command, the paged-in registers appear at the same offsets as existing µPD7210 registers. At the end of the next CPU access, the chip pages out the paged-in registers. The following table lists all the registers in the 7210 mode register set along with their associated addressing information. See the NAT7210 data sheet (National Instruments part number 340488-01) for more information about 7210 mode registers.

7210 Register Set

Register	PAGE-IN	A(2-0)	WE*	DBIN	CE*	ACCGR*
Data-In	U	0 0 0	1	1	0	1
Data-In	X	X X X	X	0	X	0
Command/Data Out	U	0 0 0	0	0	0	1
Command/Data Out	X	X X X	0	1	X	0
Interrupt Status 1	U	0 0 1	1	1	0	1
Interrupt Mask 1	U	0 0 1	0	0	0	1
Interrupt Status 2	U	0 1 0	1	1	0	1
Interrupt Mask 2	U	0 1 0	0	0	0	1
Serial Poll Status	N	0 1 1	1	1	0	1
Serial Poll Mode	N	0 1 1	0	0	0	1
Version	P	0 1 1	1	1	0	1
Internal Counter 2	P	0 1 1	0	0	0	1
Address Status	U	1 0 0	1	1	0	1
Address Mode	U	1 0 0	0	0	0	1
Command Pass Through	N	1 0 1	1	1	0	1
Auxiliary Mode	U	1 0 1	0	0	0	1
Source/Acceptor Status†	P	1 0 1	1	1	0	1
Address 0	N	1 1 0	1	1	0	1
Address	N	1 1 0	0	0	0	1
Interrupt Status 0†	P	1 1 0	1	1	0	1
Interrupt Mask 0†	P	1 1 0	0	0	0	1
Address 1	N	1 1 1	1	1	0	1
End-Of-String	N	1 1 1	0	0	0	1
Bus Status†	P	1 1 1	1	1	0	1
Bus Control†	P	1 1 1	0	0	0	1

Notes for the PAGE-IN Column

U = The page-in auxiliary command does not affect the register.
N = The register offset is alway valid except for immediately after a page-in auxiliary command.
P = The register is valid only immediately after a page-in auxiliary command.

Preliminary DC Characteristics

T_A 0 to 70° C; V_{CC} = 5 V ±5%

		Limits			Test
Parameter	**Symbol**	**Min**	**Max**	**Unit**	**Condition**
Voltage input low	V_{IL}	-0.5	+0.8	V	
Voltage input high	V_{IH}	+2.0	V_{CC}	V	
Voltage output low	V_{OL}	0	0.4	V	
Voltage output high	V_{OH}	+2.4	VCC	V	
Input/output leakage current		-10	+10	µA	without internal pull-up
Input/output leakage current		-200	+200	µA	with internal pull-up
Supply current			45	mA	
Output current low					
All pins except ACCRQ	I_{OL}	2		mA	0.4 V @ I_{OL}
ACCRQ	I_{OL}	4		mA	0.4 V @ I_{OL}
Input current low	I_{IL}		- 0.5	mA	
Supply voltage	V_{DD}	4.75	5.25	V	

Capacitance

T_A 0 to 70° C; V_{CC} = 5 V ±5%

		Limits			Test
Parameter	**Symbol**	**Min**	**Max**	**Unit**	**Condition**
Input capacitance	C_{IN}		10	pF	
Output capacitance	C_{OUT}		10	pF	
I/O capacitance	$C_{I/O}$		10	pF	

Absolute Maximum Ratings

Property	**Range**
Supply voltage, V_{DD}	-0.5 to +7.0 V
Input voltage, V_I	-0.5 to V_{DD} +0.5 V
Operating temperature, T_{OPR}	0 to +70° C
Storage temperature, T_{STG}	-40 to +125° C

Comment: Exposing the device to stresses above those listed could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

AC Characteristics

T_A 0 to 70° C; V_{CC} = 5 V ±5%

		Limits			Test
Parameter	**Symbol**	**Min**	**Max**	**Unit**	**Condition**
Address hold from $\overline{CE}$, $\overline{WE}$,and DBIN	t_{AH}	0		ns	
Address setup to $\overline{CE}$, $\overline{WE}$, and DBIN	t_{AS}	0		ns	
Data float from $\overline{CE}$ or DBIN	t_{DF}		20	ns	
Data delay from DBIN↓,	t_{DR}		75	ns	$\overline{ACCGR}$=0
$\overline{ACCRQ}$ unassertion	t_{DU}		20	ns	
Data delay from $\overline{CE}$↓	t_{RD}		80	ns	$\overline{ACCGR}$=1
$\overline{CE}$ recovery width	t_{RR}	80		ns	
$\overline{CE}$ pulse width	t_{RW}	80		ns	
Data hold from $\overline{WE}$↑	t_{WH}	0		ns	
Data setup to $\overline{WE}$↑	t_{WS}	60		ns	

Timing Waveforms

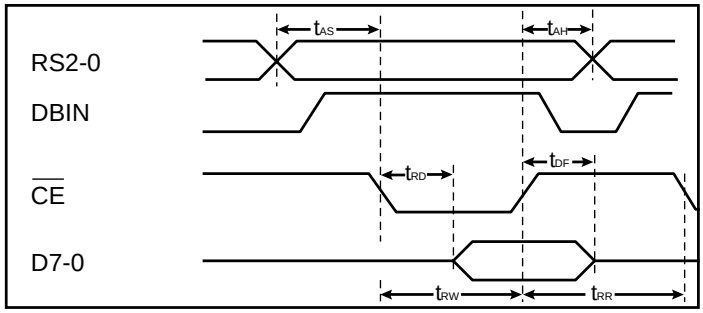


Figure 4. CPU Read

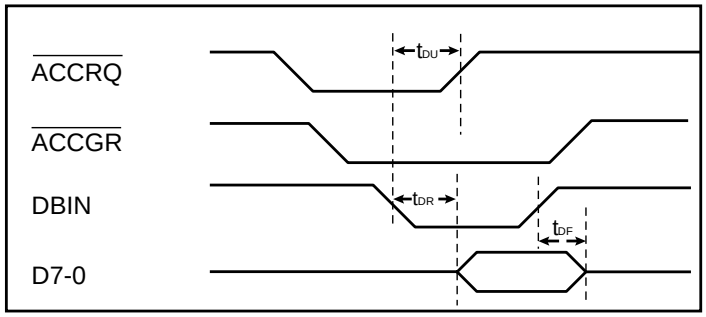


Figure 5. DMA Read

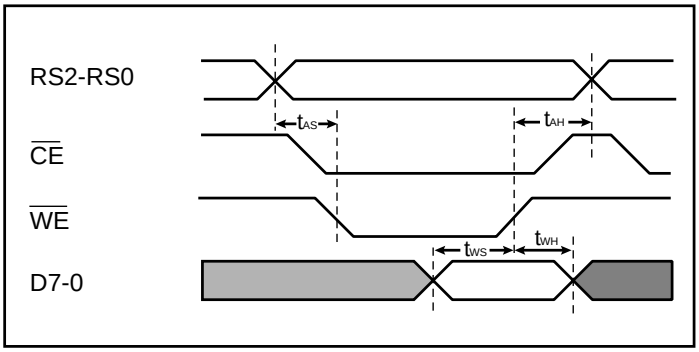


Figure 6. CPU Write

Notes:

- t_{AS} is the setup time to $\overline{CE}$↓ or $\overline{WE}$↓ whichever is later.
- t_{AH} is the hold time from $\overline{WE}$↑ or $\overline{CE}$↑ whichever is earlier.

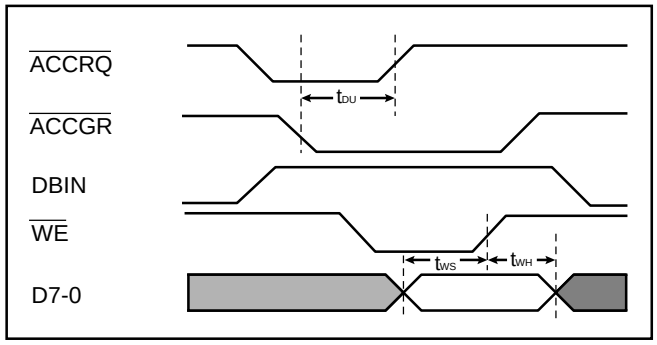


Figure 7. DMA Write

Source Handshake

Parameter	Symbol	Limits (ns) Min	Max	Test Condition
NDAC↑ to DAV↑	t_{ND}		40	
NDAC↑ to INT↓or ACCRQ↓	t_{NI}		40	INT(DOIE Bit=1) ACCGR (DMAO Bit=1)
WE↑ to DAV↓	t_{WD}	2000	2180	2 µs T1, 5MHz
WE↑ to DAV↓	t_{WD}	1200	1380	1.1 µs T1, 5MHz
WE↑ to DAV↓	t_{WD}	600	780	500 ns T1, 5MHz
WE↑ to DAV↓	t_{WD}	400	580	350 ns T1, 5MHz

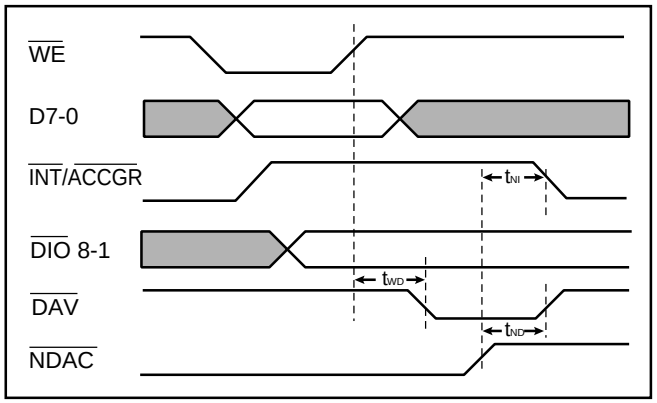


Figure 8. Source Handshake Timing

Acceptor Handshake

Parameter	Symbol	Limits (ns) Min	Max	Test Condition
DAV↓to NDAC↑	t_{DD}		35+3T	
DAV↑ to NDAC↓	t_{DF}		25	
DAV↓to INT↓or ACCRQ↓	t_{DI}		50+2T	INT(DIIE Bit=1), ACCGR (DMAI Bit=1)
DAV↓to NRFD↓	t_{DR}		20	
DBIN↑ to NRFD↑	t_{NR}		35	Read of DIR, not in Holdoff state

Note: T=one clock period

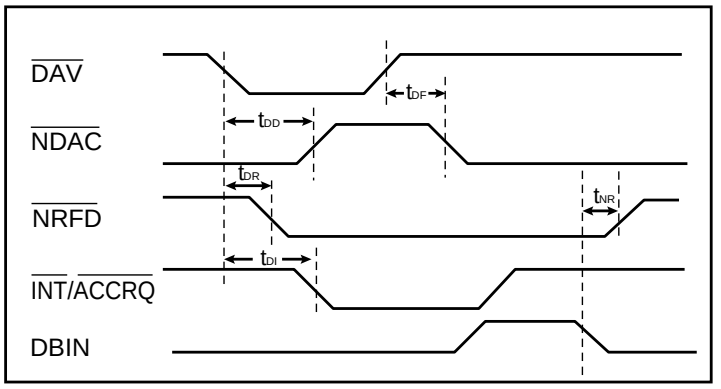


Figure 9. Acceptor Handshake Timing

Response to ATN

Parameter	Symbol	Limits (ns) Min	Max	Test Condition
ATN↑ to NRFD↓	t_{AF}		35	Acceptor handshake holdoff
ATN↓to NDAC↓	t_{AN}		35	AIDS → ANRS
ATN↓to TE↓	t_{AT}		30	TACS → TADS

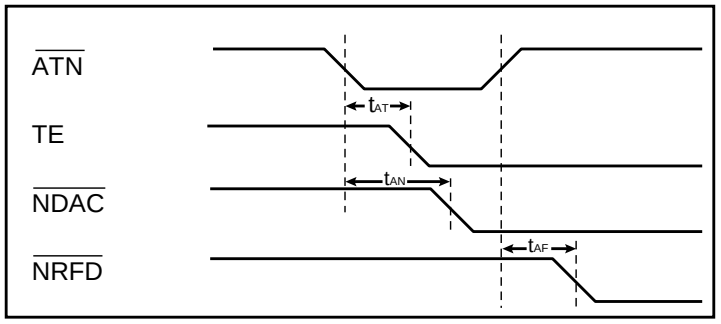


Figure 10. ATN Response Timing

Parallel Poll

Parameter	Symbol	Limits (ns) Min	Max	Test Condition
EOI ↓to DIO↓ valid	t_{ED}		90	PPSS → PPAS
EOI↓to TE ↑	t_{ET}		30	PPSS → PPAS
EOI ↑ to TE ↓	t_{TE}		30	PPAS → PPSS

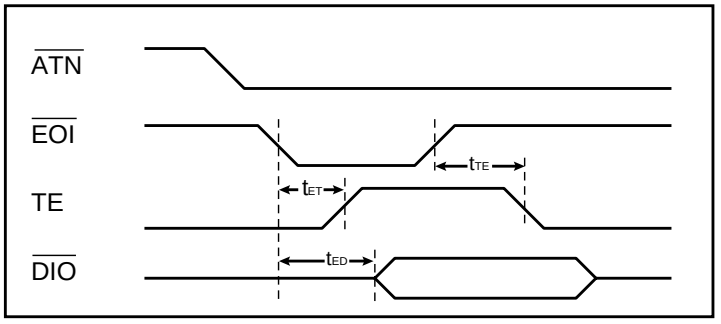


Figure 11. Parallel Poll Response Timing

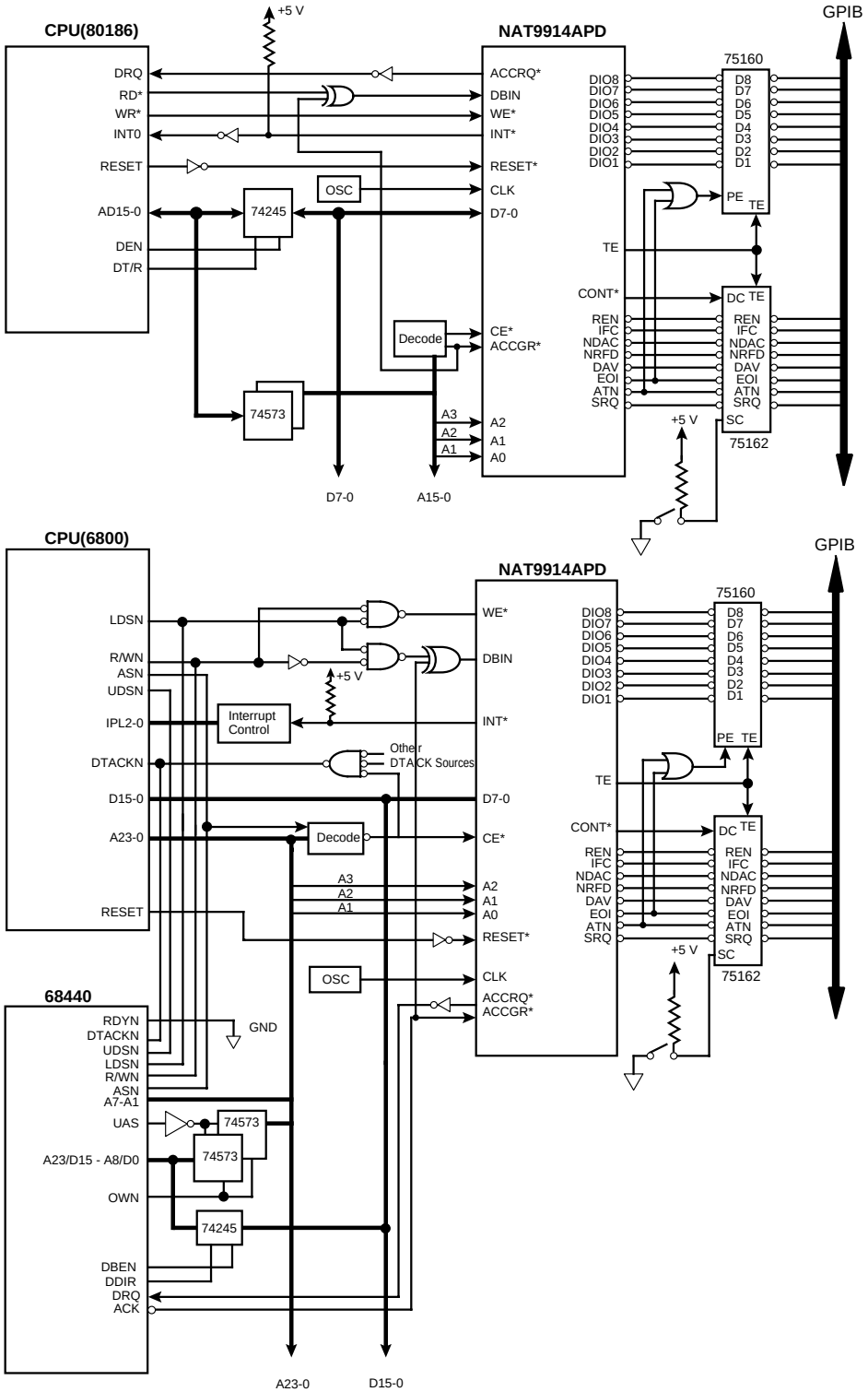


Figure 12. Typical CPU Systems with NAT9914 APD

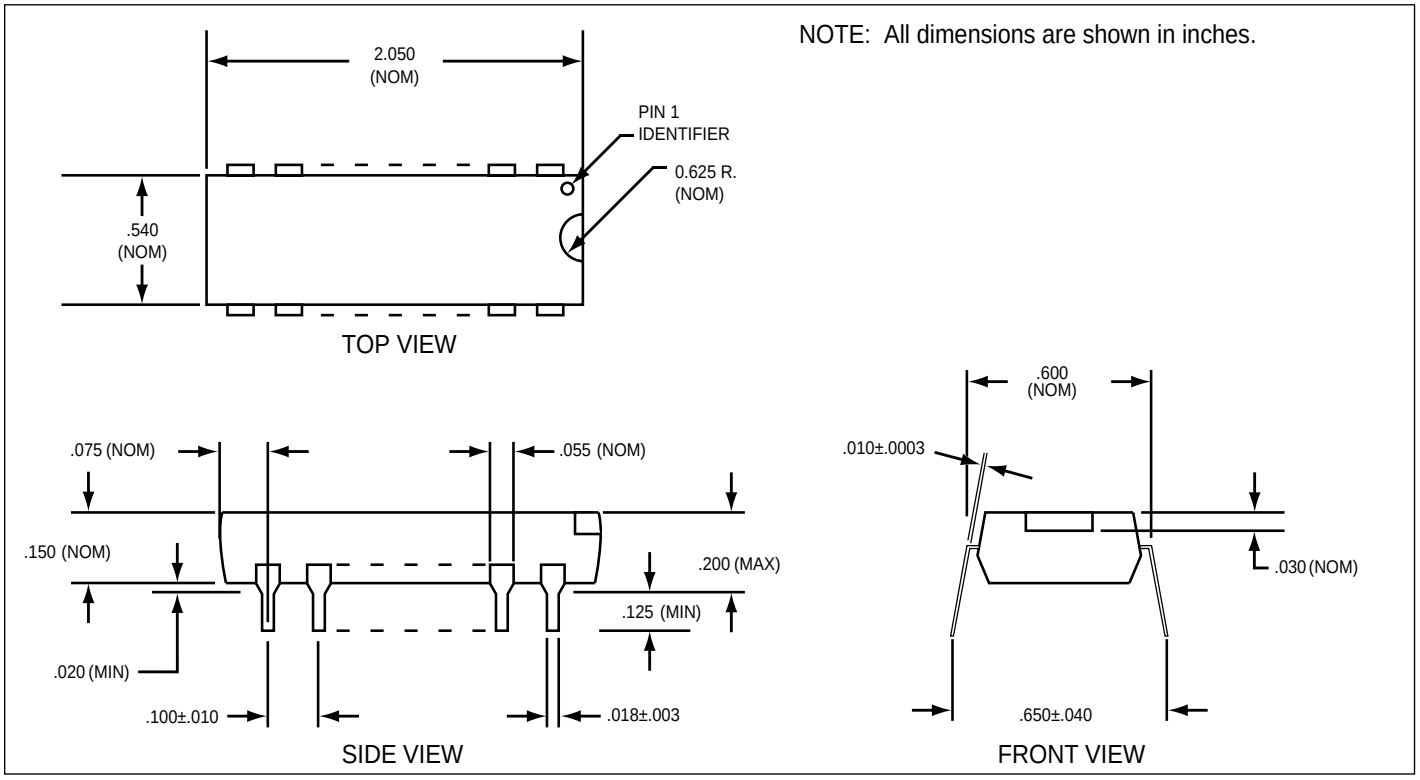


Figure 13. Mechanical Data 40-Pin Plastic DIP

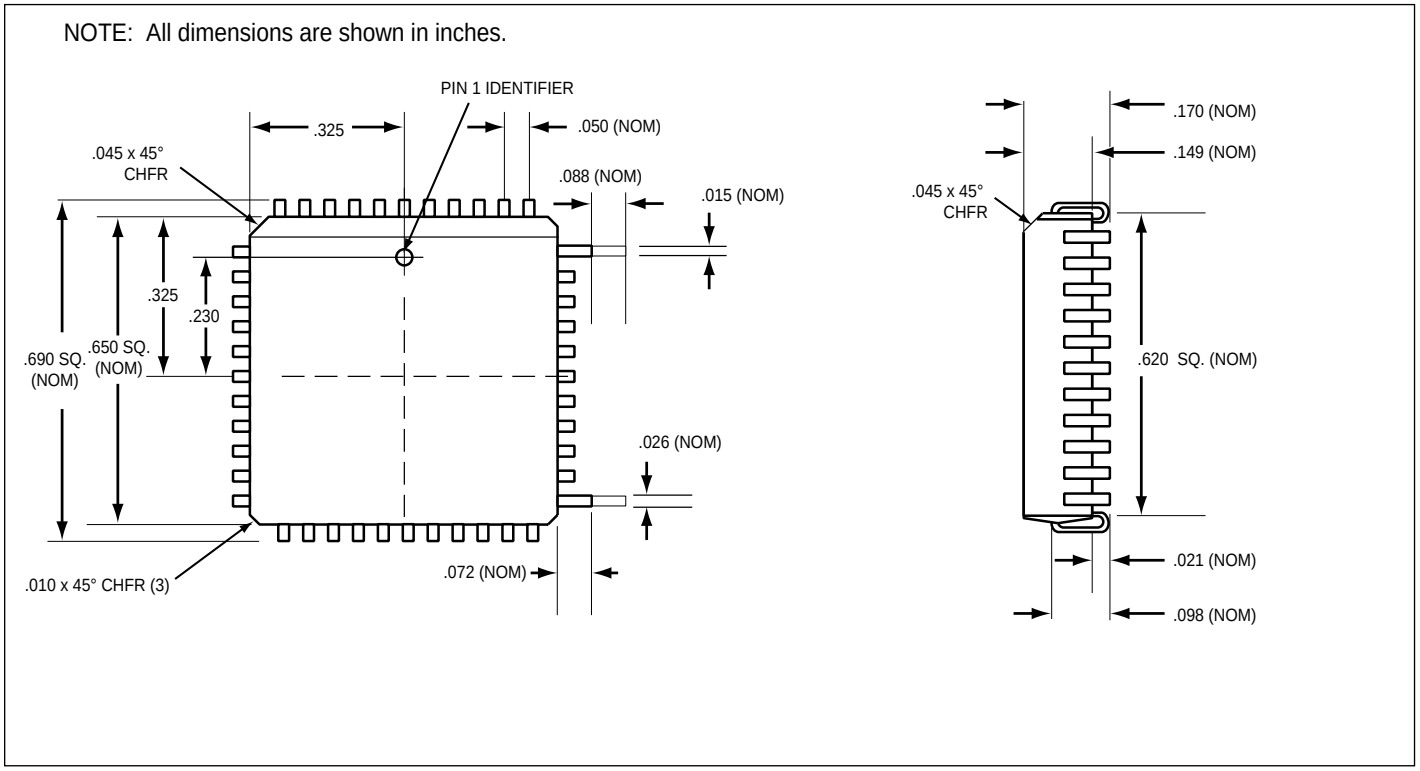


Figure 14. Mechanical Data 44-Pin PLCC

NAT9914APD
NAT9914APL

Part Numbers

NAT9914APD
NAT9914APL

Part Number Legend

a	b	c	d	e
NAT	9914	A	P	D

a. Family name – NAT = 8-bit GPIB Talker/Listener/Controller interface

b. Device number – 9914 = TI TMS9914A pin-compatible part

c. Revision

d. Package material – P = plastic

e. Package type – D = Dual Inline Package (DIP)
L = Plastic Leaded Chip Carrier (PLCC)

NAT9914 Programmer Reference Manual.....320775-01

Seminars / Training

Free and fee-paid seminars are presented several times a year in cities around the world. Comprehensive, fee-paid training courses are available at National Instruments offices, or at customer sites. Call for training schedules.

Support

National Instruments provides comprehensive technical assistance around the world. In the U.S. and Canada, applications engineers are available Monday through Friday from 8:00 a.m. to 6:00 p.m. (central time), at (512) 795-8248. In other countries, contact the nearest branch office. You can fax questions to corporate headquarters any time at (512) 794-5678.

National Instruments sponsors a wide variety of user group activities, such as user group meetings at trade shows and at large industrial sites. Our users also receive our quarterly *Instrumentation Newsletter*™ with the latest information on new products, product updates, application tips, and current events.

Warranty

All National Instruments GPIB hardware products are covered by a two-year warranty from the date of shipment. GPIB chip-level products, DAQ boards and VXIbus and MXIbus products are covered by a one-year warranty. The warranty covers board failures, components, cables, connectors, and switches, but does not cover faults caused by misuse. The owner may return a failed assembly to National Instruments for repair during the warranty period. Extended warranties are available at an additional charge.

Information furnished by National Instruments is believed to be accurate and reliable. National Instruments reserves the right to change product specifications without notice.

NATIONAL INSTRUMENTS®
The Software is the Instrument®

Ordering Information: Corporate Headquarters • 6504 Bridge Point Parkway • Austin, TX 78730-5039 USA • Tel: (512) 794-0100 • Fax: (512) 794-8411
E-mail: info@natinst.com • WWW: http://www.natinst.com

Branch Offices: Australia 03 9 879 5166 • Austria 0662 45 79 90 0 • Belgium 02 757 00 20 • Canada 905 785 0085 • Denmark 45 76 26 00 • Finland 90 527 2321 • France 01 48 14 24 24 • Germany 089 741 31 30
Hong Kong 2645 3186 • Israel 03 5734815 • Italy 02 413091 • Japan 03 5472 2970 • Korea 02 596 7456 • Mexico 95 800 010 0793 • Netherlands 0348 433466 • Norway 32 84 84 00 • Singapore 2265886
Spain 91 640 0085 • Sweden 08 730 49 70 • Switzerland 056 200 51 51 • Taiwan 02 377 1200 • U.K. 01635 523545