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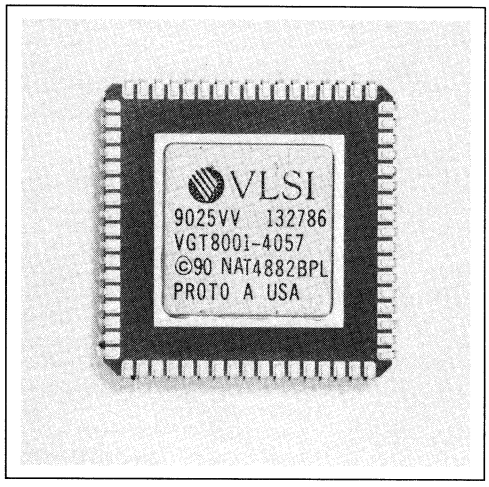
IEEE 488.2 Controller

NAT4882BPL



NAT4882BPL

Features

- Performs all IEEE 488.1 interface functions
  - Source Handshake (SH1)
  - Acceptor Handshake (AH1)
  - Talker or Extended Talker (T5 or TE5)
  - Listener or Extended Listener (L3 or LE3)
  - Service Request (SR1)
  - Remote/Local (RL1)
  - Parallel Poll
    remote configuration (PP1)
    local configuration (PP2)
  - Device Clear (DC1)
  - Device Trigger (DT1)
  - Controller, all capabilities (C1, 2, 3, 4, 5)
- Meets all IEEE 488.2 requirements
  - Bus line monitoring
  - Preferred implementation of requesting service
  - Will not send messages when there are no Listeners
- Uses 6 primary and secondary addressing modes
  - Automatic single or dual primary addressing detection
  - Automatic single primary with single secondary address detection
  - Single or dual primary with multiple secondary addressing
  - Multiple primary addressing
- Software compatible with NEC µPD7210 or TI TMS9914A controller chips
- Automatic EOS and/or NL message detection
- Direct Memory Access (DMA)
- Programmable data transfer rate (T1 delays of 350 nsec, 500 nsec, and 2 µsec)
- Automatically processes IEEE 488 commands and reads undefined commands
- Programmably compatible with bus transceivers (TI, National Semiconductor, Motorola, and Intel)
- TTL-compatible CMOS device
- 20 MHz clock rate
- Reduces driver overhead
  - Does not lose a data byte if ATN is asserted while transmitting data
  - Static interrupt status bits that do not clear when read
  - Internal timer interrupt
  - Automatically transmits END or performs an RFD holdoff on last byte of DMA transfer
- Device status indicator pins (CIC, TA, LA, REM, LOK, TRIG, MA)

Description

The NAT4882™ is an IEEE 488.2 controller chip that performs all the interface functions defined in the IEEE Standard 488.1-1987 and meets the additional requirements and recommendations of the IEEE Standard 488.2-1987. Connected between the processor and the IEEE 488 bus, the NAT4882 provides high-level management of the IEEE 488 bus, significantly increases the throughput of driver software, and simplifies both the hardware and software design. The NAT4882 performs complete IEEE 488 Talker, Listener, and Controller functions. In addition to its numerous improvements, the NAT4882 is also completely software compatible with the NEC µPD7210 and TI TMS9914A controller chips, and thus is compatible with software from existing designs.

IEEE 488.2 Overview

In 1987, the IEEE 488.2 standard removed the ambiguities of IEEE 488.1 by standardizing the way instruments and controllers operate. The standard defines data formats, status reporting, error handling, and common configuration commands to which all IEEE 488.2 instruments must respond in a precise manner, along with a set of controller requirements. The benefits of IEEE 488.2 for the test system developer are reduced development time and cost, because systems are more compatible and reliable. The future of GPIB is based on IEEE 488.2. The NAT4882 brings the full power of IEEE 488.2 as well as numerous other design and performance benefits to the design engineer.

NAT4882 PIN CONFIGURATION

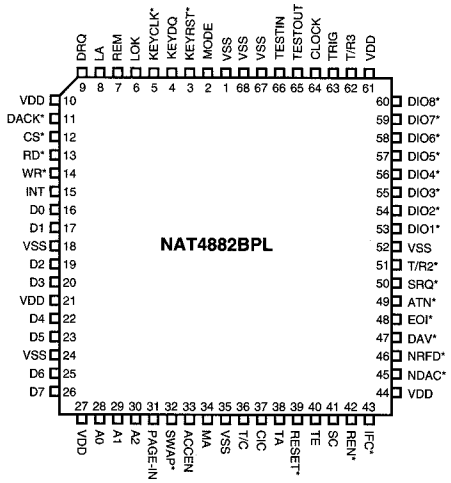


Figure 1.

PIN Identification

Mnemonic	Type	Description
D(7-0)	I/O¥	Bidirectional 3-state data bus transfers commands, data, and status between the NAT4882 and the CPU.
CS*	I¥	The chip select enables access to the register selected by a read or write operation – the register selects A(2-0).
RD*	I¥	The read input enables the contents of the register selected by A(2-0) and CS* and places them onto the data bus D(7-0).
WR*	I¥	The write input latches the contents of the data bus D(7-0) into the register selected by A(2-0).
DACK*	I¥	The DMA Acknowledge signal selects the DIR or CDOR for the current read or write cycle.
DRQ	O	The DMA Request output asserts to request a DMA Acknowledge cycle.
CLOCK	I¥	The CLOCK input can go up to 20 MHz.
RESET*	I¥	Asserting the RESET input places the NAT4882 in an initial, idle state.
INT	O	The interrupt output asserts when one of the unmask interrupt conditions is true.
A(2-0)	I¥	The register selects determine which register to access during a read or write operation.
MODE	I¥	The MODE pin selects the mode in which the NAT4882 will be after a reset – 7210 (high) or 9914A (low).
SWAP*	I¥	The SWAP* pin rearranges the order of the registers when asserted and in 9914A mode (for use with the Turbo488®).
ACCEN	O	The Access Enable pin asserts when one of the paged-in registers is paged while in 9914A mode.
PAGE-IN	I¥	The PAGE-IN pin asserts pages in the paged-in registers while in 7210 mode.
IFC*	I/O¥	Bidirectional control line initializes the IEEE 488 interface functions.
REN*	I/O¥	Bidirectional control line selects either remote or local control of devices.
ATN*	I/O¥	Bidirectional control line indicates whether data on the DIO lines is an interface or device-dependent message.
SRQ*	I/O¥	Bidirectional control line requests service from the controller.
DIO(8-1)*	I/O¥	8-bit bidirectional IEEE 488 data bus.
DAV*	I/O¥	Handshake line indicates the data on the DIO(8-1)* lines is valid.
NRFD*	I/O¥	Handshake line indicates that the device is ready for data.
NDAC*	I/O¥	Handshake line indicates the completion of a message reception.
EOI*	I/O¥	Bidirectional control line indicates the last byte of a data message or to execute a parallel poll.
TE	O	Talk Enable controls the direction of the IEEE 488 data transceiver.
T/R(3) T/R(2)*	O	These pins are the input/output control for the IEEE 488 transceivers.
SC	O	The SC pin asserts when the NAT4882 is the IEEE 488 System Controller (rsc).
CIC	O	CIC asserts when the NAT4882 is the IEEE 488 Controller-In-Charge.
TA	O	TA asserts when the NAT4882 is an active or addressed IEEE 488 Talker.
LA	O	LA asserts when the NAT4882 is an active or addressed IEEE 488 Listener.
REM	O	REM asserts when the NAT4882 is in a remote state (REMS or RWLS).
LOK	O	LOK asserts when the NAT4882 is in a lockout state (LWLS or RWLS).
TRIG	O	TRIG asserts when in DTAS or the auxiliary trigger command is issued.
MA	O	My Address pulses when the NAT4882 receives its IEEE 488 address.
T/C	I¥	T/C indicates the last byte of a DMA transfer.
KEYCLK*	O	KEYCLK* reflects the status of the KEYCLK* bit in the Key Register.
KEYRST*	O	KEYRST* reflects the status of the KEYRST* bit in the Key Register.
KEYDQ	I/O¥	KEYDQ reflects the status of the KEYDQ bit in the Key Control Register when KEYDATEN is set and you can read its status in the key status register.
TESTIN	I	Test pin – should always be grounded.
TESTOUT	O	Test pin – should not be connected.
VDD	-	Power pins – +5 V (±5%).
VSS	-	Ground pins – 0 V.

¥ Pin contains an internal pull-up resistor of 30 kΩ to 150 kΩ.
*Indicates active low signals.

General

The NAT4882 manages the IEEE 488 bus. You program the IEEE 488 bus by writing control words into the appropriate registers. CPU-readable status registers supply operational feedback. The function of these registers is determined by the mode of the NAT4882. When in 7210 mode, the registers resemble the µPD7210 register set with additional registers to supply extra functionality and supply IEEE 488.2 compatibility. When in 9914A mode, the registers resemble the TMS9914A register set with additional registers that supply extra functionality and supply IEEE 488.2 compatibility. The block diagram below shows the key components of the NAT4882.

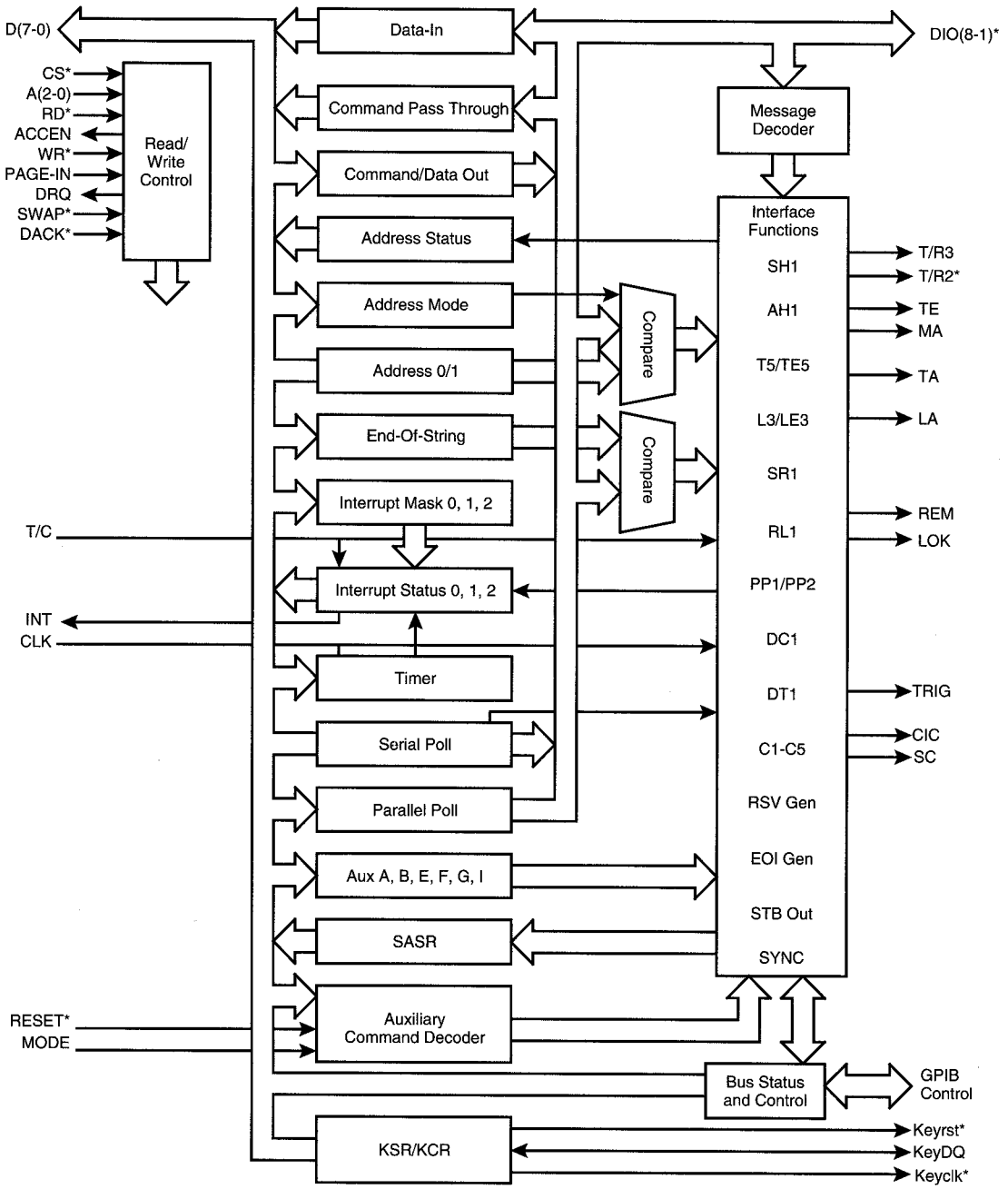


Figure 2.
NAT4882 Block Diagram

7210 Mode Registers

In 7210 mode, the NAT4882 registers include all the NEC µPD7210 registers, plus two types of additional registers – extra auxiliary registers and paged-in registers. The extra auxiliary registers are written the same as standard µPD7210 auxiliary registers. The paged-in registers appear at the same offsets as existing µPD7210 registers immediately after an auxiliary page-in command is issued. Paged-in registers are paged out at the end of the next CPU access. The following table lists all the registers in the 7210 mode register set with their associated addressing information. Features (such as registers and auxiliary commands) that are not available in the µPD7210 or TMS9914A are denoted by the '†' symbol.

7210 Register Set

Register	PAGE-IN	A(2-0)	WR*	RD*	CS*	DACK*
Data In	U	0 0 0	1	0	0	1
Data In	X	X X X	1	0	X	0
Command/Data Out	U	0 0 0	0	1	0	1
Command/Data Out	X	X X X	0	1	X	0
Interrupt Status 1	U	0 0 1	1	0	0	1
Interrupt Mask 1	U	0 0 1	0	1	0	1
Interrupt Status 2	U	0 1 0	1	0	0	1
Interrupt Mask 2	U	0 1 0	0	1	0	1
Serial Poll Status	N	0 1 1	1	0	0	1
Serial Poll Mode	N	0 1 1	0	1	0	1
Key Status†	P	0 1 1	1	0	0	1
Key Control†	P	0 1 1	0	1	0	1
Address Status	U	1 0 0	1	0	0	1
Address Mode	U	1 0 0	0	1	0	1
Command Pass Through	N	1 0 1	1	0	0	1
Auxiliary Mode	U	1 0 1	0	1	0	1
Source/Acceptor Status†	P	1 0 1	1	0	0	1
Address 0	N	1 1 0	1	0	0	1
Address	N	1 1 0	0	1	0	1
Interrupt Status 0†	P	1 1 0	1	0	0	1
Interrupt Mask 0†	P	1 1 0	0	1	0	1
Address 1	N	1 1 1	1	0	0	1
End-Of-String	N	1 1 1	0	1	0	1
Bus Status†	P	1 1 1	1	0	0	1
Bus Control†	P	1 1 1	0	1	0	1

Notes for the PAGE-IN Column

U = The register is unaffected by the page-in auxiliary command or the PAGE-IN pin.

N = The register offset is always valid except for immediately after a page-in auxiliary command or if the PAGE-IN pin is asserted.

P = The register is valid only immediately after a page-in auxiliary command or if the PAGE-IN pin is asserted.

DATA REGISTERS

Data-In Register (DIR)

DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0

Command/Data Out Register (CDOR)

DO7	DO6	DO5	DO4	DO3	DO2	DO1	DO0

You can use the data registers for data and command transfers between the IEEE 488 bus and the CPU. The Data-In Register (DIR) holds data sent from the GPIB to the CPU and the Command/Data-Out Register (CDOR) holds information for transfer onto the IEEE 488 bus.

INTERRUPT REGISTERS

Interrupt Status Register 0 (ISR0) †

CDBA	STBO	NL	EOS	IFCI	ATNI	TO	SYNC

Interrupt Status Register 1 (ISR1)

CPT	APT	DET	END	DEC	ERR	DO	DI

Interrupt Status Register 2 (ISR2)

INT	SRQI	LOK	REM	CO	LOKC	REMC	ADSC

Interrupt Mask Register 0 (IMR0) †

GLINT	STBO	NLEN	BTO	IFCI	ATNI	TO	SYNC

Interrupt Mask Register 1 (IMR1)

CPT	APT	DET	END	DEC	ERR	DO	DI

Interrupt Mask Register 2 (IMR2)

X	SRQI	DMAO	DMAI	CO	LOKC	REMC	ADSC

The interrupt registers consist of interrupt status, interrupt mask, and some non-interrupt-related bits. There are 18 conditions that can cause an interrupt. The interrupt status bit sets if its condition is true and an interrupt is generated if the corresponding interrupt mask bit is set. Most interrupt status bits are cleared upon being read unless the SISB bit in Auxiliary Register I is set, in which case the status bits are cleared by issuing an auxiliary command or taking other action. The following tables list the individual bits in the interrupt registers with a brief description.

Interrupt Status/Mask Register Bits

Bit	Description
INT	OR of all unmasked interrupt status bits
STBO†	Status Byte Out Request
IFCI†	Interface Clear (IFC) asserted
ATNI†	Attention (ATN) asserted
TO†	Time Out
SYNC†	GPIB Handshake Synchronized
CPT	Command Pass Through
APT	Address Pass Through
DET	Device Trigger (DTAS)
END	END (EOI or EOS message received)
DEC	Device Clear (DCAS)
ERR	Data Transmission Error (No Listener)
DO	Data Out (SGNS)
DI	Data In
SRQI	Service Request Input
CO	Command Out
LOKC	Lockout State Change
REMC	Remote State Change
ADSC	Address Status Change
GLINT†	Global Interrupt Enable

Non-Interrupt-Related, Readable Bits

Bit	Description
CDBA†	Command or Data Byte Available
NL†	New Line Received
EOS†	End-Of-String
LOK	Lockout (LWLS or RWLS)
REM	Remote (REMS or RWLS)

Non-Interrupt-Related, Writeable Bits

Bit	Description
NLEN†	New Line character enabled for EOS
BTO†	Enable/Disable Byte Timeouts
DMAO	Enable/Disable DMA Out
DMAI	Enable/Disable DMA In

SERIAL POLL REGISTERS

Serial Poll Status Register (SPSR)

S8	PEND	S6	S5	S4	S3	S2	S1

Serial Poll Mode Register (SPMR)

S8	rsv	S6	S5	S4	S3	S2	S1

The Serial Poll Mode Register holds the STB (status byte – S8, S6 through S1) that will be sent over the GPIB when the NAT4882 is serial polled and also holds the local rsv message (request service). The STB is automatically sourced when the NAT4882 is serial polled and the STBO bit in IMR0 is cleared. When STBO is set (†), the STB is not sourced during serial polls until the SPMR is written. The SPMR is readable through the SPSR. The PEND bit is set when rsv is set. The PEND bit is cleared upon entering Negative Poll Response State (NPRS) and when rsv is cleared.

KEY REGISTERS †

Key Status Register (KSR) †

V3	V2	V1	V0	KEY DQ	Mode	0	0

Key Control Register (KCR) †

0	SWAP	MSTD	0	KEY CLK*	KEY DEN	KEY DAT	KEY RST*

The Key Control Register contains bits you can use to control the Key pins KEYCLK*, KEYRST*, and KEYDQ. Pins KEYCLK* and KEYRST* are driven to the value of the corresponding bit. The KEYDQ pin is driven to the value of the KEYDAT bit when the KEYDEN bit is set. If KEYDEN is cleared, the KEYDQ pin is configured as an input and you can monitor it via the KEYDQ bit in the Key Status Register. You can also monitor the MODE pin via the MODE bit in the KSR. Setting the MSTD bit in the KCR causes the NAT4882 to use a 200 nsec T1 delay when sourcing data bytes. The SWAP bit is set to swap 9914A registers for use with the Turbo488. V(3:0) in the KSR indicates the version of the NAT4882, and should read 0010 for the NAT4882BPL.

ADDRESS REGISTERS

The NAT4882 contains several registers used to control the GPIB address mode, the GPIB address(es), and monitor the GPIB address status.

Address Status Register(ADSR)

CIC	ATN*	SPMS	LPAS	TPAS	LA	TA	MJMN

Address Mode Register (ADMR)

TON	LON	TRM1	TRM0	0	0	ADM1	ADM0

The Address Mode Register selects the address mode of the NAT4882 and controls the mode for the transceiver control outputs, T/R2* and T/R3. T/R2* and T/R3 are controlled by the values of the TRM1 and TRM0 bits, as shown in the following table.

TRM1	TRM0	T/R2*	T/R3
0	0	EOIOE*	TRIG
0	1	CIC*	TRIG
1	0	CIC*	EOIOE
1	1	CIC*	PE

Notes for the T/R2* and T/R3 columns

EOIOE = TACS + SPAS + CIC & ~CSBS
CIC = ~(CIDS + CADS)
PE = CIC + ~PPAS
TRIG = DTAS or trigger auxiliary command issued

The following table lists the different addressing modes of the NAT4882 in 7210 mode.

Address Modes

ton	lon	adm1	adm0	Address Mode	Contents of Registers ADR0	ADR1
1	0	0	0	Talk Only	GPIB address not necessary (no controller)	
0	1	0	0	Listen Only	GPIB address not necessary (no controller)	
0	0	0	1	Address Mode 1	Major address	Minor address
0	0	1	0	Address Mode 2	Primary address	Secondary address
0	0	1	1	Address Mode 3	Primary major address	Primary minor address

Notes for the Address Mode column

Mode 1 The NAT4882 recognizes its MTA/MLA if the received address matches either ADR0 or ADR1; interface function Talker/Listener (T/L).

Mode 2 Address Register 0 = primary address; Address Register 1= secondary addresses; interface function Talker Extended/Listener Extended (TE/LE).

Mode 3 The CPU must read the secondary address through the Command Pass Through Register; interface function Talker Extended/Listener Extended (TE/LE).

Address Status Bits

Bit	Description
ATN*	GPIB ATN signal
LPAS	Listener Primary Addressed State
TPAS	Talker Primary Addressed State
CIC	Controller-In-Charge
LA	Listener Addressed
TA	Talker Addressed
MJMN	Set if minor T/L addressed Clear if major T/L addressed
SPMS	Serial Poll Mode State

Address Register 0 (ADR0)

X	DT0	DL0	AD 5-0	AD 4-0	AD 3-0	AD 2-0	AD 1-0

Address Register 1 (ADR1)

EOI	DT1	DL1	AD 5-1	AD 4-1	AD 3-1	AD 2-1	AD 1-1

Address Register 0/1 (ADR)

ARS	DT	DL	AD5	AD4	AD3	AD2	AD1

The NAT4882 is able to automatically detect two types of addresses in ADR0 and ADR1. The function of each bit is described in the following table.

Address Register 0/1 Bits

Bit	Description
ARS	Selects either address register 0 or 1
DT1-0	Prohibits the talk address from being detected
DL1-0	Prohibits the listen address from being detected
AD5-0	Lower five bits of GPIB address
EOI	Holds the value of EOI line when data is received

COMMAND PASS THROUGH REGISTER (CPTR)

CPT 7	CPT 6	CPT 5	CPT 4	CPT 3	CPT 2	CPT 1	CPT 0

With the Command Pass Through Register, the CPU can read GPIB DIO lines 8 through 1 in the cases of undefined commands, secondary addresses, or parallel poll responses.

END-OF-STRING REGISTER (EOSR)

EOS 7	EOS 6	EOS 5	EOS 4	EOS 3	EOS 2	EOS 1	EOS 0

The End-Of-String Register holds either the 7 or 8-bit EOS message byte used in the GPIB system to detect the end of a data block.

GPIB SOURCE/ACCEPTOR STATUS REGISTER (SASR)

CDBA	AEHS	ANHS1	ANHS2	ADHS	ACRDY	SH1A	SH1B

The CPU can monitor the Source and Acceptor handshake functions via the Source/Acceptor Status Register. The following table lists each bit in the SASR along with a description.

Source/Acceptor Status Bits

Bit	Description
CDBA	Command or Data Byte Available local message
AEHS	Acceptor Holding Off on End State
ANHS1	Acceptor Holding Off on All or End State
ANHS2	Acceptor Holding Off because a Holdoff Handshake Immediate command was issued
ADHS	Acceptor in a DAC Holdoff State
ACRDY	Acceptor in ACRS
SH1(A-B)	Source Handshake Status SH1(A-B)=00 SH1 in SIDS or SGNS SH1(A-B)=1X SH1 in SDYS SH1(A-B)=01 SH1 in STRS

AUXILIARY MODE REGISTER (AUXMR)

CNT 2	CNT 1	CNT 0	COM 4	COM 3	COM 2	COM 1	COM 0

The Auxiliary Mode Register is a multipurpose register. A write to this register generates one of the following operations, according to the values of the CNT bits and COM4. The following table shows bit patterns that must be written to the AUXMR to access the hidden registers.

Auxiliary Mode Operations

CNT 2	CNT 1	CNT 0	COM 4	COM 3	COM 2	COM 1	COM 0	Operation
0	X	0	C4	C3	C2	C1	C0	Issues an auxiliary command specified by C4 to C0
0	1	1	U	S	P3	P2	P1	Writes to the parallel poll register
1	0	0	A4	A3	A2	A1	A0	Writes to the Auxiliary Register A
1	0	1	B4	B3	B2	B1	B0	Writes to the Auxiliary Register B
1	1	0	0	E3†	E2†	E1	E0	Writes to the Auxiliary Register E
1	1	0	1	F3	F2	F1	F0	Writes to the Auxiliary Register F (†)
0	1	0	0	G3	G2	G1	G0	Writes to the Auxiliary Register G (†)
1	1	1	0	I3	I2	I1	I0	Writes to the Auxiliary Register I (†)
1	1	1	1	J3	J2	J1	J0	Writes to the Auxiliary Register J (†)

Auxiliary Commands

CNT 210	COM 43210	Command	Operation
000	00000	pon	Generates the local pon message
000	00010	chrst	Chip reset
000	00011	rhdf	Release RFD holdoff
000	00100	trig	Trigger
000	0x101	rtl	Sets the Return to Local (rtl) message if x =1; clears or pulses rtl if x =0
000	00110	seoi	Send EOI with next byte
000	00111	nvld	Nonvalid (OSA reception); release DAC holdoff
000	01111	vld	Valid (MSA Reception, CPT,DEC,DET); release DAC holdoff
000	01000 †	rqc	Request Control
000	00001	ist=0	Clear parallel poll flag: ist
000	01001	ist=1	Sets parallel poll flag: ist
000	01010 †	rlc	Release Control
000	01011 †	lut	Untalk
000	01100 †	lul	Unlisten
000	01110 †	nbaf	New Byte Available False
000	10000	gts	Go To Standby
000	10001	tca	Take Control Asynchronously
000	10010	tcs	Take Control Synchronously
000	11010	tcse	Take Control Synchronously on End
000	10011	ltn	Listen
000	11011	ltn&cnt	Listen in Continuous Mode
000	11100	lun	Local Unlisten
000	10100	~rsc	Disable System Control
000	10101†	9914	Switch to 9914A Mode
000	11110	sic&rsc	Sets IFC and rsc
000	10110	~sic	Clears IFC
000	11111	sre&rsc	Sets REN and rsc
000	10111	~sre	Clears REN
000	11000 †	reqt	Issue reqt message
000	11001†	reqf	Issue reqf message
000	11101	rpp	Execute a parallel poll
010	10000 †	page	Page in additional registers
010	10001†	hldi	Holdoff handshake immediately
010	1001X	rsvd	Reserved
010	10100 †	clrDET	Clear DET bit in ISR1
010	10101 †	clrEND	Clear END bit in ISR1
010	10110 †	clrDEC	Clear DEC bit in ISR1
010	10111 †	clrERR	Clear ERR bit in ISR1
010	11000 †	clrSRQI	Clear SRQI bit in ISR2
010	11001 †	clrLOKC	Clear LOKC bit in ISR2
010	11010 †	clrREMC	Clear REMC bit in ISR2
010	11011 †	clrADSC	Clear ADSC bit in ISR2
010	11100 †	clrIFCI	Clear IFCI bit in ISR0
010	11101 †	clrATNI	Clear ATNI bit in ISR0
010	11110 †	clrSYNC	Clear SYNC bit in ISR0
010	11111 †	setSYNC	Set SYNC bit in ISR0

PARALLEL POLL RESPONSE REGISTER (PPR)

0	1	1	U	S	P3	P2	P1

The Parallel Poll Response Register determines the parallel poll response of the NAT4882. The following table shows each bit in the register along with the function of each bit.

Parallel Bit	Response Poll	Function
U	0 1	Respond to parallel polls Do not respond to parallel polls
S	0 1	Reverse phase In phase
P3-P1	000-111	Status bit output line DIO1(P3-1= 000) to DIO8(P3-1 = 111)

AUXILIARY REGISTER A (AUXRA)

1	0	0	A4	A3	A2	A1	A0

The five-bit AUXRA register controls the GPIB data receiving mode of the NAT4882, and also controls how the EOS message is used as listed in the following table.

Data Receiving Modes

A1	A0	Data Receiving Mode
0	0	Normal Handshake Mode
0	1	RFD Holdoff on all data Mode
1	0	RFD Holdoff on END Mode
1	1	Continuous Mode

EOS

Bit		Function
A2	**0 Prohibit** 1 Permit	Permits (prohibits) the setting of the END bit by the reception of the EOS message
A3	**0 Prohibit** 1 Permit	Permits (prohibits) automatic transmission of END message simultaneously with the transmission of EOS message while in TACS
A4	**0 7-bit** 1 8-bit	Selects 7 or 8-bits as the valid length of the EOS message

AUXILIARY REGISTER B (AUXRB)

1	0	1	B4	B3	B2	B1	B0

The five-bit AUXRB register controls special operating features of the NAT4882, as listed in the following table.

Special Features

Bit		Function
B0	**0 Prohibit** 1 Permit	Permits (prohibits) the detection of an undefined command by setting the CPT bit on receipt of an undefined command and performing a DAC holdoff
B1	**0 Prohibit** 1 Permit	Permits (prohibits) the transmission of the END message when in Serial Poll Active State (SPAS)
B2	**0 low-speed** 1 high-speed	Permits high-speed T1 (500 to 350 ns) in the source handshake function after transmission of first byte following ATN unasserting. If cleared, prohibits high-speed T1
B3	**0 high** 1 low	Specifies the active level of the INT pin
B4	**1 SRQS** 0 Parallel Poll flag	Determines if the value of the ist local message is equal to SRQS or the parallel poll flag

AUXILIARY REGISTER E (AUXRE)

1	1	0	0	E3	E2	E1	E0

The four-bit AUXRE register controls DAC holdoff modes, as listed in the following table.

Special Features

Bit	Name	Function
E0	DHDC	DAC Holdoff on DCAS
E1	DHDT	DAC Holdoff on DTAS
E2 †	DHADC	DAC Holdoff on DCL or SDC
E3 †	DHADT	DAC Holdoff on GET

AUXILIARY REGISTER F † (AUXRF)

1	1	0	1	F3	F2	F1	F0

The four-bit AUXRF register controls DAC Holdoff modes, as listed in the following table.

Special Features

Bit	Name	Function
F0	DHALL	DAC Holdoff on all UCG, ACG, and SCG commands
F1	DHUNLT	DAC Holdoff on UNL and UNT
F2	DHALA	DAC Holdoff on all Listener addresses
F3	DHATA	DAC Holdoff on all Talker addresses

AUXILIARY REGISTER G † (AUXRG)

0	1	0	0	G3	G2	G1	G0

The four-bit AUXRG register controls special operational features of the NAT4882, as listed in the following table.

Special Features

Bit	Name	Function
G0	CHES	Enables the clearing of the END detector circuitry on the reception of a data byte without END
G1	DISTCT	When set, this bit disables the ability of NAT4882 to take control when control is passed to it
G2	RPP2	Request parallel poll local message
G3	NTNL	Setting this bit prevents the NAT4882 from sourcing a data or command byte when there are no Listeners on the GPIB

AUXILIARY REGISTER I † (AUXRI)

1	1	1	0	I3	I2	I1	I0

The four-bit AUXRI register controls special operational features of the NAT4882. These features are listed in the following table.

Special Features

Bit	Name	Function
I0	SISB=0	Interrupt status bits are cleared by reads of the Interrupt Status registers
	SISB=1	Interrupt status bits are cleared by issuing the appropriate auxiliary command or the conditions listed below only
I1	ACC	Enables the EOI to be sent with a data byte if the TC pin is asserted during a DMA write cycle to the NAT4882; or, performs a RFD Holdoff on a data byte if the TC pin is asserted during a DMA read cycle
I2	PP2	When set, the NAT4882 ignores remote GPIB parallel poll configure commands
I3	USTD	The USTD bit and AUXRB bit B2 control the T1 delay used when sourcing command and data bytes (see chart below)

The following table lists the different T1 delays handled by the NAT4882.

AUX B2 Bit	AUX I3 Bit	T1 for first data and all commands	T1 for the second and remaining data
0	0	2 µsec	2 µsec
0	1	1.1 µsec	1.1 µsec
1	0	2 µsec	500 nsec
1	1	1.1 µsec	350 nsec

The following table lists the clear conditions of each interrupt status bit when SISB is set.

Bit	Clear Condition when SISB=1
CPT	pon + read CPTR
APT	pon + valid + non-valid
DET	pon + Clear DET
END	pon + Clear END
DEC	pon + Clear DEC
ERR	pon + Clear ERR
DO	pon + ~TACS + ~SGNS + nba
DI	pon + (finish handshake) * (Holdoff mode) + read DIR
SRQI	pon + clear SRQI
CO	pon + ~CACS + ~SGNS + nba
LOKC	pon + clear LOKC
REMC	pon + clear REMC
ADSC	pon + clear ADSC + ton + lon
IFCI	pon + clear IFCI
ATNI	pon + clear ATNI

AUXILIARY REGISTER J † (AUXRJ)

1	1	1	1	J3	J2	J1	J0

You use the four-bit AUSRJ register to set the timeout value of the timer interrupt. You can set the timeout value between the range of 15 µsec to 125 sec when the NAT4882 is clocked at 20 MHz. The timer starts when the AUXRJ is written with a non-zero value and sets the TO bit in the ISR0 when the timeout value has expired. The following chart lists the approximate timeout values handled by Auxiliary Register J at 20 MHz. If you use another clock frequency for the NAT4882, the timeout value may be computed with the formula – time = $(2^{factor} * 5)$/frequency.

J3-0	Timeout Value (> or =)	Factor
0000	Disabled	-
0001	15 µsec	6
0010	30 µsec	7
0011	125 µsec	9
0100	250 µsec	10
0101	1 msec	12
0110	4 msec	14
0111	15 msec	16
1000	30 msec	17
1001	125 msec	19
1010	250 msec	20
1011	1 sec	22
1100	4 sec	24
1101	15 sec	26
1110	30 sec	27
1111	125 sec	29

The timer handles different types of timeouts, depending on the value of the BTO bit. If BTO is cleared, the timer operates in global mode. In this mode, the timer is started upon writing a non-zero value to the AUXRJ and continues counting until the timeout value is reached, which sets the TO bit. If BTO is set, the timer operates in byte timeout mode. In this mode, you start the timer upon writing a non-zero value to the AUXRJ, and it continues counting until the timeout value is reached. However, DIR reads or CDOR writes will clear the timer and force it to start counting again. In Byte Timeout mode, after TO is set, it will remain set until the AUXRJ is written. Further reads of DIR or writes of CDOR will have no effect on TO until the AUXRJ is written.

BUS CONTROL/STATUS REGISTERS † (BCR/BSR)

ATN	DAV	NDAC	NRFD	EOI	SRQ	IFC	REN

The CPU can monitor the GPIB by reading the Bus Status Register. You can assert (drive low) GPIB signals by setting the corresponding bit in the GPIB Control Register to 1.

9914 Mode Registers

In 9914 mode, the NAT4882 registers consist of all the TI TMS9914A registers and two types of additional registers – newly defined registers and paged-in registers. The newly defined registers are mapped into the unused portion of the 9914 address space. Each paged-in register appears at offset 2 immediately after an auxiliary page-in command is issued, and remains there until another register is paged into the same space or a reset is issued. The following table lists all the registers in the 9914 register set.

9914 Register Set

Register	Page In	Not Swapped A(2-0)	WR*	RD*	CS*	DACK*	Swapped A(2-0)
Interrupt Status 0	U	0 0 0	1	0	0	1	110
Interrupt Mask 0	U	0 0 0	0	1	0	1	110
Interrupt Status 1	U	0 0 1	1	0	0	1	111
Interrupt Mask 1	U	0 0 1	0	1	0	1	111
Address Status	U	0 1 0	1	0	0	1	100
Interrupt Mask 2 †	P	0 1 0	0	1	0	1	100
End-of-String †	P	0 1 0	0	1	0	1	100
Bus Control †	P	0 1 0	0	1	0	1	100
Accessory †	P	0 1 0	0	1	0	1	100
Bus Status	U	0 1 1	1	0	0	1	101
Auxiliary Command	U	0 1 1	0	1	0	1	101
Interrupt Status 2 †	P	1 0 0	1	0	0	1	011
Address	U	1 0 0	0	1	0	1	011
Serial Poll Status †	P	1 0 1	1	0	0	1	010
Serial Poll Mode	U	1 0 1	0	1	0	1	010
Command Pass Thru	U	1 1 0	1	0	0	1	001
Parallel Poll	U	1 1 0	0	1	0	1	001
Data-In	U	1 1 1	1	0	0	1	000
Data-In	U	X X X	1	0	X	0	XXX
Command/Data Out	U	1 1 1	0	1	0	1	000
Command/Data Out	U	X X X	0	1	X	0	XXX

Notes for the PAGE-IN column

U = The register offset is unaffected by page-in auxiliary commands.

P = The register offset is valid only after a page-in auxiliary command.

The Not Swapped column for A(2-0) is valid when the SWAP pin is unasserted (high) and the SWAP bit is cleared (see 7210 MODE Key Registers). The Swapped column for A(2-0) is valid when the SWAP pin is asserted (low) or the SWAP bit is set.

DATA REGISTERS

Data-In Register (DIR)

DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0

Command/Data Out Register (CDOR)

DO7	DO6	DO5	DO4	DO3	DO2	DO1	DO0

You use the data registers for data and command transfers between the IEEE 488 and the CPU. The DIR holds data sent from the GPIB to the computer and the CDOR holds information written into it for transfer to the IEEE 488.

INTERRUPT REGISTERS

Interrupt Status Register 0 (ISR0)

INT0	INT1	BI	BO	END	SPAS	RLC	MAC

Interrupt Status Register 1 (ISR1)

GET	ERR	UNC	APT	DCAS	MA	SRQ	IFC

Interrupt Status Register 2 (ISR2) †

CDBA	STBO	NL	EOS	LLOC	ATN	TO	CIC

Interrupt Mask Register 0 (IMR0)

DMAO	DMAI	BI IE	BO IE	END IE	SPAS IE	RLC IE	MAC IE

Interrupt Mask Register 1 (IMR1)

GET IE	ERR IE	UNC IE	APT IE	DCAS IE	MA IE	SRQ IE	IFC IE

Interrupt Mask Register 2 (IMR2) †

GL INT	STBO IE	NL EN	BTO	LLOC IE	ATN IE	TO IE	CIC IE

The interrupt registers consist of interrupt status bits, interrupt mask bits, and some non-interrupt related bits. There are 19 conditions that can cause an interrupt. The interrupt status bit will set if its condition is true. An interrupt will be generated if the corresponding mask bit is set. Most interrupt status bits are cleared upon being read. The following tables list the individual bits in the interrupt registers along with a description.

Interrupt Status and/or Mask Register Bits

Bits	Description
INT0	OR of all unmasked ISR0 bits
INT1	OR of all unmasked ISR1 bits
BI	Byte In
BO	Byte Out
END	END (EOI or EOS message received)
SPAS	SPAS (Serial Poll Active State)
RLC	Remote/Local Change
MAC	My Address Change
GET	Group Execute Trigger
ERR	Data Transmition Error
UNC	Unrecognized Command
APT	Address Pass Through
DCAS	Device Clear Active State
MA	My Address
SRQ	Service Request (SRQ)
IFC	Interface Clear (IFC) asserted
STBO †	Status Byte Out Request
LLOC †	Lockout State Change
ATN †	Attention (ATN) asserted
TO †	Time Out
CIC †	Controller-In-Charge
GLINT †	Global Interrupt Enable

Noninterrupt Related, Readable Bits

Bits	Description
CDBA †	Command or Data Byte Available
NL †	New Line Received
EOS †	End-Of-String

Noninterrupt Related, Writeable Bits

Bits	Description
NLEN †	New Line character enabled for EOS
BTO †	Enable/Disable Byte Timeouts
DMAO †	Enable/Disable DMA Out
DMAI †	Enable/Disable DMA In

SERIAL POLL REGISTERS

Serial Poll Status Register (SPSR) †

S8	PEND	S6	S5	S4	S3	S2	S1

Serial Poll Mode Register (SPMR)

S8	rsv	S6	S5	S4	S3	S2	S1

The Serial Poll Mode Register holds the STB (status byte – S8, S6 through S1) that will be sent over the GPIB when the NAT4882 is serial polled and the local rsv message (request service). The STB is automatically sourced when the NAT4882 is serial polled when STBO IE is cleared. When the STBO IE bit in IMR2 is set (†), the STB is not sourced during serial polls until the SMPR is written. The SPMR is readable through the SPSR. SPSR is only accessable if a register has been paged into offset 2. The PEND bit is set when rsv is set and cleared by Negative Poll Response State when rsv is cleared.

ADDRESS REGISTERS

The NAT4882 contains two registers used to control the GPIB address mode, store the GPIB address, and monitor the GPIB address status.

ADDRESS STATUS REGISTER (ADSR)

REM	LLO	ATN	LPAS	TPAS	LA	TA	ULPA

You use the address status register to monitor the address state of the NAT4882. The following table lists the ADSR bits along with a description of each bit.

Address Status Bits

Bit	Description
REM	The NAT4882 is in the Remote state
LLO	The NAT4882 is in the Local Lockout state
ATN	GPIB ATN signal
LPAS	Listener Primary Addressed State
TPAS	Talker Primary Addressed State
LA	Listener Addressed
TA	Talker Addressed
ULPA	Stores the LSB of the last address recognized by the NAT4882

ADDRESS REGISTER (ADR)

EDPA	DAL	DAT	A5	A4	A3	A2	A1

The NAT4882 can automatically detect the address in ADR as its MTA or MLA. The function of each bit is described in the following chart.

Address Register Bits

Bit	Description
EDPA	Enables dual addressing mode, in which the least significant address bit is ignored, giving the NAT4882 two consecutive GPIB addresses
DAL	Prohibits the Listen address from being detected
DAT	Prohibits the Talk address from being detected
A5-0	GPIB primary address

COMMAND PASS THROUGH REGISTER (CPTR)

CPT 7	CPT 6	CPT 5	CPT 4	CPT 3	CPT 2	CPT 1	CPT 0

With the Command Pass Through Register (CPTR), the CPU reads the GPIB DIO (8-1) lines in the cases of undefined commands, secondary addresses, or parallel poll responses.

PARALLEL POLL REGISTER (PPR)

PP8	PP7	PP6	PP5	PP4	PP3	PP2	PP1

The PPR contains the value that the NAT4882 outputs on the GPIB when a parallel poll is conducted by the Controller-In-Charge. If you desire to participate in a parallel poll, then you should set the bit corresponding to the desired parallel poll response to 1. The parallel poll register is double buffered. Therefore, if it is written during a parallel poll, the register will be updated with the new value at the end of the parallel poll.

END-OF-STRING REGISTER † (EOSR)

EOS 7	EOS 6	EOS 5	EOS 4	EOS 3	EOS 2	EOS 1	EOS 0

The EOSR holds either the 7 or 8-bit EOS message byte used in the GPIB system to detect the end of a data block.

AUXILIARY COMMAND REGISTER

C/S	X	X	F4	F3	F2	F1	F0

A write to this register generates one of the following operations according to the values of the C/S and F (4-0).

Auxiliary Commands

C/S	F 43210	Command	Operation
0/1	00000	swrst	Clear/Set software reset
0	00001	dacr	Non-Valid DAC release Holdoff
1	00001	dacr	Valid DAC release Holdoff
X	00010	rhdf	Release RFD Holdoff
0/1	00011	hlda	Clear/Set Holdoff on All Data

(continues)

(continued)

C/S	F 43210	Command	Operation
0/1	00100	hlde	Clear/Set Holdoff on END only
X	00101	nbaf	New Byte Available False
0/1	00110	fget	Clear/Set Force Group Execute Trigger
0/1	00111	rtl	Clear/Set Return to Local
X	01000	seoi	Send EOI with next byte
0/1	01001	lon	Clear/Set Listen Only
0/1	01010	ton	Clear/Set Talk Only
X	01011	gts	Go To Standby
X	01100	tca	Take Control Asynchronously
X	01101	tcs	Take Control Synchronously
0/1	01110	rpp	Clear/Set Request Parallel Poll
0/1	01111	sic	Clear/Set Send Interface Clear
0/1	10000	sre	Clear/Set Send Remote Enable
X	10001	rqc	Request Control
X	10010	rlc	Release Control
0/1	10011	dai	Clear/Set Disable All Interrupts
X	10100	pts	Pass Through Next Secondary
0/1	10101	stdl	Clear/Set Short T1 settling time
0/1	10110	shdw	Clear/Set Shadow Handshake
0/1	10111	vstdl	Clear/Set Very Short T1 delay
0/1	11000	rsv2	Clear/Set Request Service Bit 2
0	11001	rsvd	Reserved
1	11001 †	sw7210	Switch to µPD7210 Mode
0	11010 †	reqf	Send Reqf
1	11010 †	reqt	Send Reqt
X	11011	rsvd	Reserved
0	11100 †	chrst	Chip Reset
1	11100 †	clrpi	Clear Page in Registers
0/1	11101 †	ist	Clear/Set Parallel Poll Flag
0	11110 †	piimr2	Page-In Interrupt Mask 2 Register
1	11110 †	pieosr	Page-In End-Of-String Register
0	11111 †	pibcr	Page-In Board Control Register
1	11111 †	piaccr	Page-In Accessory Register

ACCESSORY REGISTER † (ACCR)

CNT 2	CNT 1	CNT 0	COM 4	COM 3	COM 2	COM 1	COM 0

The ACCR is a multipurpose register. A write to this register generates one of the following operations according to the values of the CNT bits and COM4.

Auxiliary Mode Operations

CNT			COM					Operation
2	1	0	4	3	2	1	0	
1	0	0	A4	A3	A2	0	0	Writes to the Auxiliary Register A
1	0	1	B4	B3	B2	B1	B0	Writes to the Auxiliary Register B
1	1	0	0	E3	E2	E1	E0	Writes to the Auxiliary Register E
1	1	0	1	F3	F2	F1	F0	Writes to the Auxiliary Register F
1	1	1	0	I3	I2	I1	I0	Writes to the Auxiliary Register I
1	1	1	1	J3	J2	J1	J0	Writes to the Auxiliary Register J

AUXILIARY REGISTER A † (AUXRA)

1	0	0	A4	A3	A2	0	0

The three-bit AUXRA register controls how the EOS message is used, as shown in the following table.

EOS Message

Bit		Function
A2	**0 Prohibit** 1 Permit	Permits (prohibits) the setting of the End bit by the reception of the EOS message
A3	**0 Prohibit** 1 Permit	Permits (prohibits) automatic transmission of END message simultaneously with the transmission of EOS message while in TACS
A4	**0 7-bit** 1 8-bit	Selects 7 or 8 bits as the valid length of the EOS message

AUXILIARY REGISTER B † (AUXRB)

1	0	1	B4	B3	B2	B1	B0

The five-bit AUXRB register controls special operating features of the NAT4882, as shown in the following table.

Special Features

Bit		Function
B0	**0 Prohibit** 1 Permit	Permits the NAT4882 to automatically take control of the GPIB when control is passed to it (TCT)
B1	**0 Prohibit** 1 Permit	Permits (prohibit) the transmission of the END message when in Serial Poll Active State (SPAS)
B2	**0 Prohibit** 1 Permit	Permits the NAT4882 to accept and respond to the GPIB commands it sources
B3	**0 high** 1 low	Specifies the active level of the INT pin
B4	**1 SRQS** 0 Parallel poll flag	Determines if the value of the ist local message is equal to SRQS (B4=1) or the parallel poll flag (B4=0)

AUXILIARY REGISTER E † (AUXRE)

1	1	0	0	E3	E2	E1	E0

The four-bit AUXRE register controls DAC holdoff modes, as explained in the following table.

Special Features

Bit	Name	Function
E0	DHDC	DAC Holdoff on DCAS
E1	DHDT	DAC Holdoff on DTAS
E2	DHADC	DAC Holdoff on DCL or SDC
E3	DHADT	DAC Holdoff on GET

AUXILIARY REGISTER F † (AUXRF)

1	1	0	1	F3	F2	F1	F0

The four-bit AUXRF register controls DAC holdoff modes.

Special Features

Bit	Name	Function
F0	DHALL	DAC Holdoff on all UCG, ACG, and SCG commands
F1	DHUNLT	DAC Holdoff on UNL and UNT
F2	DHALA	DAC Holdoff on all Listener addresses
F3	DHATA	DAC Holdoff on all Talker addresses

AUXILIARY REGISTER I † (AUXRI)

1	1	1	0	I3	I2	I1	I0

This four-bit register controls special operational features of the NAT4882 as shown in the following table.

Special Features

Bit	Name	Function
I0	DMAEN=0 DMAEN=1	DRQ is asserted if either a Byte In (BI) or Byte Out (BO) condition occurs DRQ is asserted if the BI and DMAI bits are set or the BO and the DMAO bits are set
I1	ACC	When set, EOI is sent with a data byte if the TC pin is asserted during a DMA write cycle to the NAT4882 or a RFD holdoff is performed on a data byte if the TC pin is asserted during a DMA read cycle
I2	PP1	When set, the NAT4882 responds to remote GPIB parallel poll configure commands and automatically responds to parallel polls
I3	USTD	Enables 350 nsec (T1) delays

AUXILIARY REGISTER J † (AUXRJ)

1	1	1	1	J3	J2	J1	J0

You use the four-bit AUXRI register to set the timeout value of the timer interrupt. You can set the timeout value between the range of 15 µsec to 125 sec. You start the timer when the AUXRJ is written with a non-zero value, and AUXRJ sets the TO bit in the ISR0 when the timeout value has expired. The following chart lists the approximate timeout values handled by AUXRJ at 20 MHz. If you use another clock frequency for the NAT4882, you can compute the timeout value with the following formula - time = $(2^{factor} * 5)$/frequency.

J3-0	Timeout Value (> or =)	Factor
0000	Disabled	-
0001	15 µsec	6
0010	30 µsec	7
0011	125 µsec	9
0100	250 µsec	10
0101	1 msec	12
0110	4 msec	14
0111	15 msec	16
1000	30 msec	17
1001	125 msec	19
1010	250 msec	20
1011	1 sec	22
1100	4 sec	24
1101	15 sec	26
1110	30 sec	27
1111	125 sec	29

The timer handles two different types of timeouts, depending on the value of the BTO bit. If BTO is cleared, the timer operates in global mode. In global mode, you start the timer upon writing a non-zero value to the AUXRJ. The AUXRJ continues counting until it reads the timeout value, which sets the TO bit. If BTO is set, the timer operates in byte timeout mode. In this mode, you start the timer upon writing a non-zero value to the AUXRJ, and the AUXRJ continues counting until it reaches the timeout value. However, DIR reads or CDOR writes will clear the timer and force it to start counting again. In byte timeout mode, after TO is set, it will remain set until the AUXRJ is written. Further reads of DIR or writes of CDOR will have no effect on TO until the AUXRJ is written.

BUS CONTROL/STATUS REGISTERS † (BCR/BSR)

ATN	DAV	NDAC	NRFD	EOI	SRQ	IFC	REN

The CPU can monitor the GPIB by reading the Bus Status register. You can assert GPIB signals (driven low) by setting the bit corresponding to the GPIB signal in the GPIB Control Register to 1.

DC Characteristics

T_A 0 to 70°C; V_{CC} = 5 V ± 5%

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Condition
Voltage input low	V_{IL}	-0.5	+0.8	V	
Voltage input high	V_{IH}	+2.0	V_{CC}	V	
Voltage output low	V_{OL}	0	0.4	V	
Voltage output high	V_{OH}	+2.4	VCC	V	
Input/output leakage current		-10	+10	µA	without internal pull-up
Input/output leakage current		-190	+190	µA	with internal pull-up
Supply current			90	mA	
Output current low D [7:0]	I_{OL}		24 mA		0.4 V @ I_{OL}
INT, DRQ	I_{OL}		8 mA		0.4 V @ I_{OL}
LA, REM, LOK, KEYCLK, KEYDQ, KEYRST, TRIG, TE, CIC, TA, MA, ACCEN	I_{OL}		4 mA		0.4 V @ I_{OL}
KEYRD*, T/R3, DIO [8-1], T/R2, SRQ*, ATN*, EOI*, DAV*, NRFD*, NDAC*, IFC*, REN*, SC	I_{OL}		2 mA		0.4 V @ I_{OL}
Output current high D [7:0]	I_{OH}		24 mA		2.4 V @ I_{OH}
INT, DRQ	I_{OH}		8 mA		2.4 V @ I_{OH}
LA, REM, LOK, KEYCLK, KEYDQ, KEYRST, TRIG, TE, CIC, TA, MA, ACCEN	I_{OH}		4 mA		2.4 V @ I_{OH}
KEYRD*, T/R3, DIO [8-1], T/R2, SRQ*, ATN*, EOI*, DAV*, NRFD*, NDAC*, IFC*, REN*, SC	I_{OH}		2 mA		2.4 V @ I_O
Input current low/high	I_{IL}/I_{IT}	-20 µA+20 µA -400 µA+400 µA			without pull-up with pull-up

Capacitance

T_A 0 to 70°C; V_{CC} = 5 V ± 5%

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Condition
Input capacitance	C_{IN}		8	pF	
Output capacitance	C_{OUT}		8	pF	
I/O capacitance	$C_{I/O}$		8	pF	

Absolute Maximum Ratings

Property	Range
Supply voltage, V_{CC}	-0.5 to +6.0 V
Input voltage, V_I	-0.5 to V_{CC} +0.5
Operating temperature, T_{OPR}	0 to +70° C
Storage temperature, T_{STG}	-40 to +125° C

Comment – Exposing the device to stresses above those listed could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Timing Waveforms

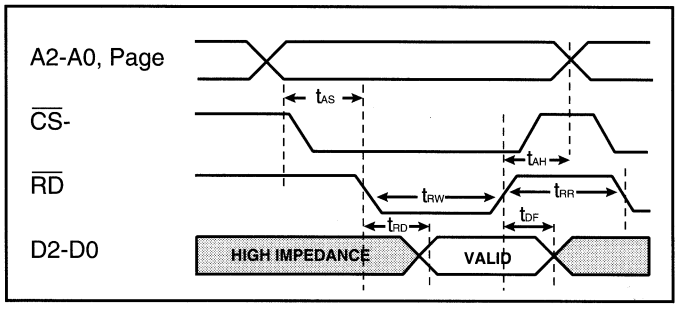


Figure 3.
CPU Read

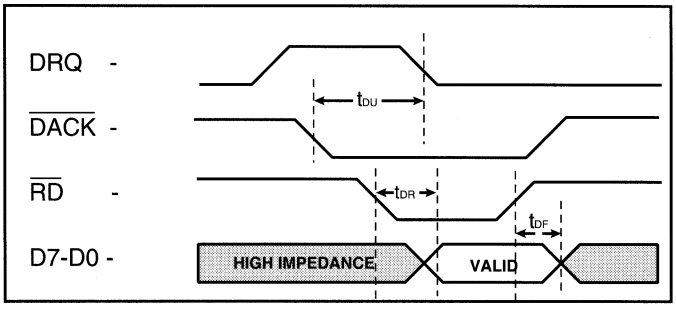


Figure 4.
DMA Read

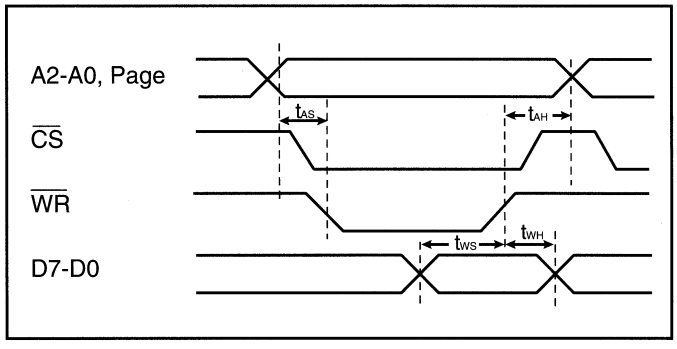


Figure 5.
CPU Write

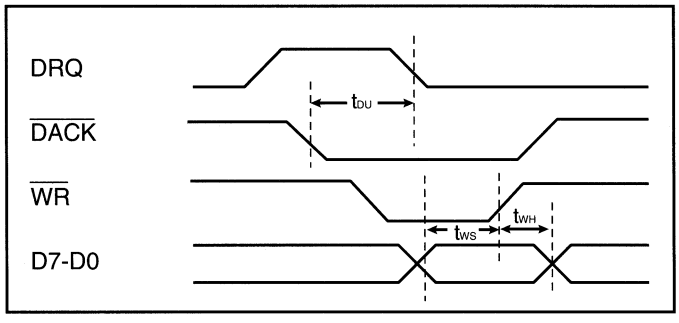


Figure 6.
DMA Write

AC Characteristics

T_A 0 to 70°C; V_{CC} = 5 V ± 5%

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Condition
Address setup to $\overline{RD}\downarrow$, $\overline{WR}\downarrow$	t_{AS}	9		nsec	
Data delay from $\overline{RD}\downarrow$, $\overline{CS}$=0	t_{RD}		45	nsec	
Data float from $\overline{RD}\uparrow$	t_{DF}		26	nsec	
$\overline{RD}$ pulse width	t_{RW}	45		nsec	
$\overline{RD}$ recovery width	t_{RR}	15		nsec	
Address hold from $\overline{RD}\uparrow$, $\overline{WR}\uparrow$	t_{AH}	0		nsec	
DRQ unassertion	t_{DU}		31	nsec	
Data dalay from $\overline{RD}\downarrow$, $\overline{DACK}$=0	t_{DR}		38	nsec	
Data setup to $\overline{WR}\uparrow$	t_{WS}	7		nsec	
Data hold from $\overline{WR}\uparrow$	t_{WH}	10		nsec	

Timing Waveforms

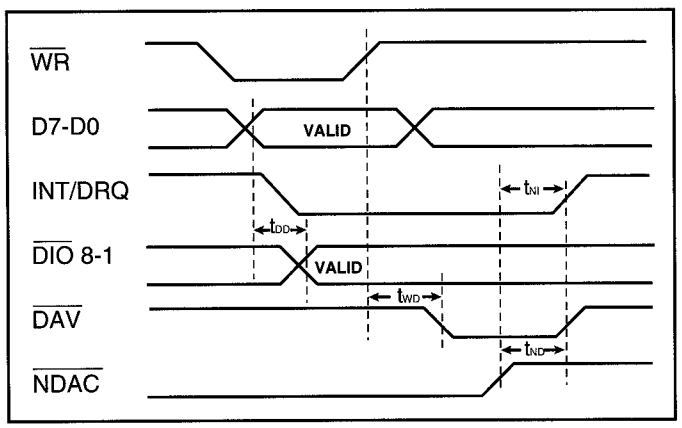


Figure 7.
Source Handshake

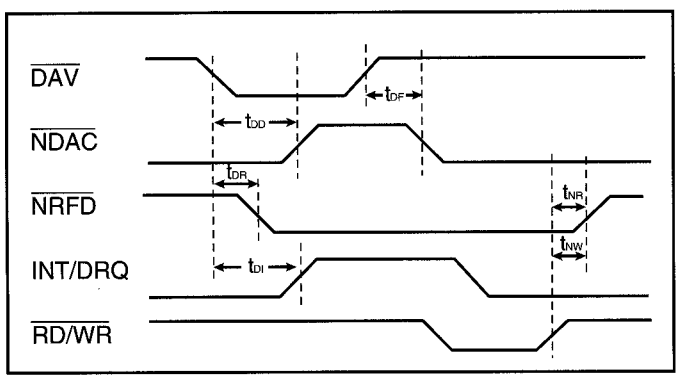


Figure 8.
Acceptor Handshake

Response to ATN

Parameter	Symbol	Limits (nsec) Min	Limits (nsec) Max	Test Condition
$\overline{EOI}\downarrow$ to $\overline{DIO}$ valid			51	PPSS ↔ PPAS, $\overline{ATN}$ = TRUE
$\overline{EOI}\downarrow$ to TE↑			48	PPSS ↔ PPAS, $\overline{ATN}$ = TRUE
$\overline{EOI}\uparrow$ to TE↓			30	PPSS ↔ PPAS, $\overline{ATN}$ = TRUE
$\overline{ATN}\downarrow$ to $\overline{NDAC}\downarrow$			46	AIDS → ANRS
$\overline{ATN}\uparrow$ to $\overline{NRFD}\downarrow$			50	Acceptor handshake holdoff
$\overline{ATN}\downarrow$ to TE↓			32	TACS → TADS

Source Handshake

Parameter	Symbol	Limits (nsec) Min	Limits (nsec) Max	Test Condition
Delay of $\overline{DIO}$ valid from D valid	t_{DD}		55	
Delay of $\overline{DAV}\downarrow$ from $\overline{WR}\uparrow$	t_{WD}		41Ø+68	2 µsec T1
Delay of $\overline{DAV}\downarrow$ from $\overline{WR}\uparrow$	t_{WD}		21Ø+73	1.1 µsec T1
Delay of $\overline{DAV}\downarrow$ from $\overline{WR}\uparrow$	t_{WD}		11Ø+75	500 nsec T1
Delay of $\overline{DAV}\downarrow$ from $\overline{WR}\uparrow$	t_{WD}		8Ø+71	350 nsec T1
Delay of $\overline{DAV}\downarrow$ from $\overline{WR}\uparrow$	t_{WD}		5Ø+71	200 nsec T1
Delay of $\overline{DAV}\uparrow$ from $\overline{NDAC}\uparrow$	t_{ND}		56	
Delay of INT↑ or DRQ↑ from $\overline{NDAC}\uparrow$	t_{NI}		41	INT(DOIE Bit=1) DRQ(DMAO Bit=1)

ø = a rising edge on CLK

Acceptor Handshake

Parameter	Symbol	Limits (nsec) Min	Limits (nsec) Max	Test Condition
Delay of $\overline{NDAC}\uparrow$ from $\overline{DAV}\downarrow$	t_{DD}		3Ø+65	
Delay of $\overline{NRFD}\downarrow$ from $\overline{DAV}\downarrow$	t_{DR}		70	
Delay of INT↑ or DRQ↑ from $\overline{DAV}\downarrow$	t_{DI}		2Ø+43	INT(DIIE Bit=1), DRQ (DMAI Bit=1)
Delay of $\overline{NDAC}\downarrow$ from $\overline{DAV}\uparrow$	t_{DF}		60	
Delay of $\overline{NRFD}\uparrow$ from $\overline{RD}\uparrow$	t_{NR}		69	Read of DIR, not in holdoff state
Delay of $\overline{NRFD}\uparrow$ from $\overline{WR}\uparrow$	t_{NW}		3Ø+75	In holdoff state, issuing finish handshake auxiliary command

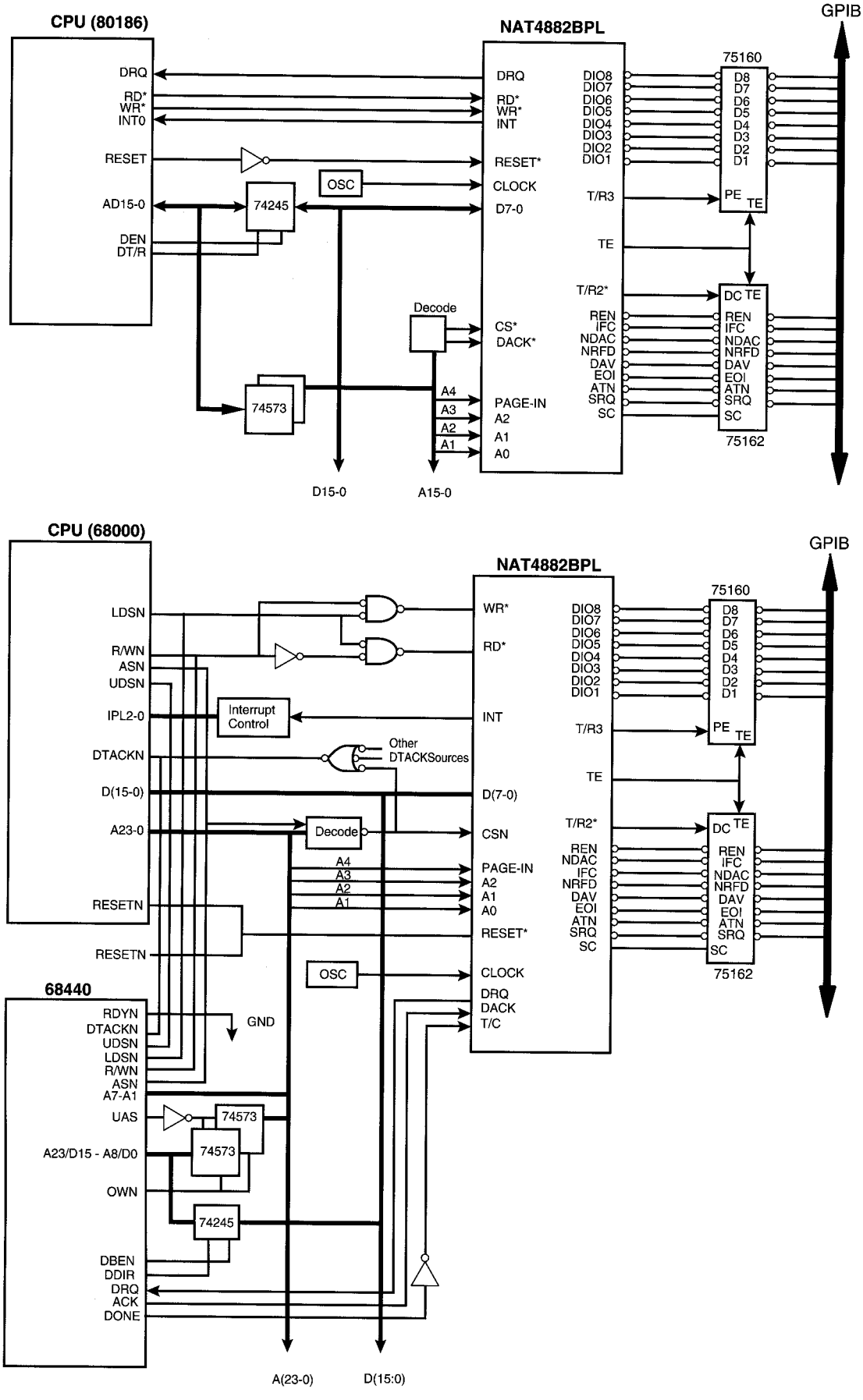
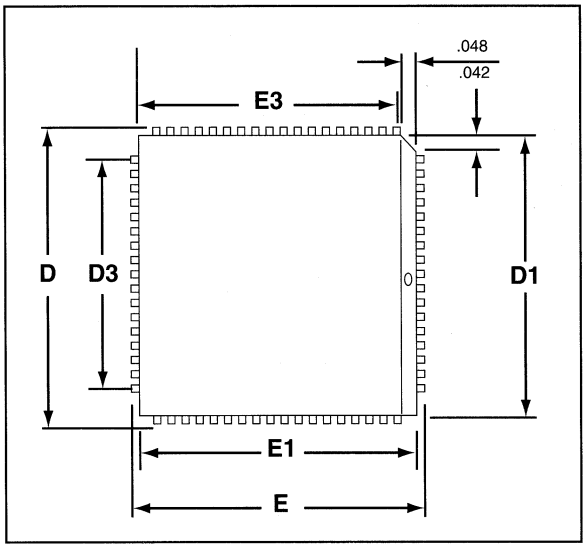
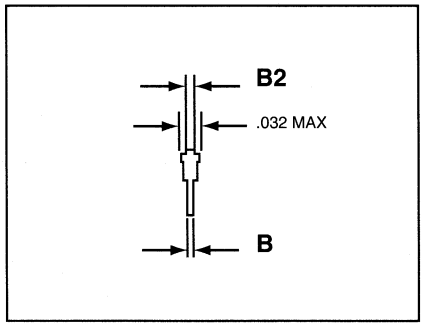


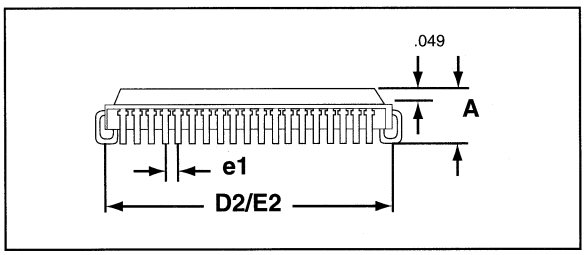
Figure 9.
Typical CPU Systems with NAT4882 BPL



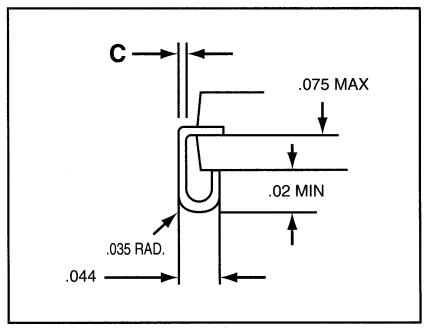
Top View



Pin
Front View



Side View



Pin
Side View

Dimensions

	A	B	B2	C	D	D1	D2	D3	E	E1	E2	E3	e1
MIN	.165 (4,19)	.013 (,330)	.026 (,660)	.008 (,203)	.985 (25,02)	.950 (24,13)	.890 (22,61)	.800 (20,32) REF	.985 (25,02)	.950 (24,13)	.890 (22,61)	.800 (20,32) REF	.050 (1, 27) TYP
MAX	.185 (5,08)	.021 (,533)	.032 (,813)	.011 (,254)	.995 (25,27)	.956 (24,33)	.930 (23,62)		.995 (25,27)	.956 (24,33)	.930 (23,62)		

Notes:

1. All dimensions are in inches.
2. Lead frame material – Copper.
3. Lead finish – Matte tin or Sn/Pb solder dip.

Figure 10.
Mechanical Data 68-Pin PLCC

Ordering Information

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