DATA SHEET

PCF7961XTT

Security Transponder, Micro-RISC Kernel and Radio Transmitter (SMART)

Product Specification

2011 Nov 17

Confidential

CONTENTS

1 FEATURES

- Single chip Security Transponder and Keyless Entry solution with on-chip UHF Transmitter
- Up to seven keyless Entry command buttons
- RISC programmable device features
- 512 Byte EEPROM for extended data storage
- 32 bit quasi unique device and product type identification
- Device supply may be derived from LF Field
- Single Lithium cell operation, 2.1V to 3.6V
- 20-Pin TSSO package

Calculation Unit

- Hardwired security algorithm
- HT2 48 bit Secret Key
- HT3 96 bit Secret Key

Security Transponder Emulation

- HT3 compatible Transponder operation
- 96 bit secret key authentication
- Up to 460 Byte User EEPROM size
- Fast mutual authentication, 53ms (96 bit Secret Key)
- HT2 compatible basic command set and coding
- Versatile EEPROM access and protection capabilities
- Improved Transponder Command error handling
- Excellent sensitivity in read and write mode

RISC Controller

- 8 Bit RISC Architecture (MRK II)
- 16 kByte E-ROM or 4/8 kByte ROM (application)
- 4 kByte ROM (device firmware and library functions)
- 192 Byte User RAM
- 7 general purpose I/O
- Two 8 Bit Timer/Counter
- Watchdog
- Single level interrupt architecture
- On-chip RC Oscillator (< ±8%)
- Short instruction execution time (as fast as 0.5μs)
- Low power consumption
  RUN: 300μA, IDLE: 20μA, PD: 100nA
- Programmable battery low detection

UHF Transmitter

- Highly integrated PLL stabilized design
- Carrier frequency 315MHz or 434MHz
- Programmable reference crystal load capacitance
- Programmable ASK and FSK modulation properties
- Up to 20 kbps modulation data rate (Manchester)
- Programmable and stabilized output power
- Low power consumption
  TRANSMIT: 9.8mA; 9dBm @ 434MHz
  LOCKED: 1.5mA

2 GENERAL DESCRIPTION

The PCF7961X is a single chip solution for applications combining vehicle Immobilization and Keyless Entry functions (Combi Key) that require the transponder to offer extended data storage capabilities.

To serve the function of a Security Transponder, an external coil has to be connected to the device. Providing contactless communication with the base station as well as to derive the device power supply from the magnetic field, generated by a corresponding base station. No additional battery supply is needed. The basic transponder operation is emulated by the RISC and is functional compatible with the transponder PCF7938XA and features versatile EEPROM access and protection capabilities. The Security Transponder features secure contactless authentication, employing a Secret Key and a random number in order to cipher any communication between the device and the base station. The PCF7961X features a factory programmed quasi unique serial number that also serves as product type identification.

When serving Keyless Entry functions, the device is powered from an external battery. The application program and the hardwired Calculation Unit may accomplish rolling code generation. The Calculation Unit may operate in standard HT2 (48 bit Secret Key) or HT3 mode (96 bit Secret Key). A number of general purpose I/Os are provided for command buttons, LED, IR or other optional external circuitry. The on-chip UHF Transmitter requires no external components to operate at 315MHz or 434MHz except for the reference crystal and the loop antenna matching circuitry.

Device operation is controlled by an E-ROM (FLASH like features) based RISC Controller, powered by NXP's low power 8-Bit MICRO RISC KERNEL (MRK II). The RISC employs a 2-stage pipeline architecture in order to execute an instruction in a single clock cycle. Device timing is derived from an on-chip low tolerance RC Oscillator that provides a programmable system clock, with a frequency up to 2 MHz. The system clock may also be derived from the transponder interface, e.g. LF Field clock or the PLL reference clock, if desired.

The PCF7961X incorporates an advanced power management that supports voltage measurement for battery low detection. For increased battery lifetime, the device features an extremely low quiescent current in POWER-OFF state, achieved by disconnecting the battery from most of the internal circuitry.The device comes in a 20 pin TSSO Package.

The device is available as E-ROM product (FLASH like features) supporting in-circuit program download and debugging. The device is fully RoHS compliant and Dark Green (DG). DG means use of flame retardants free of halogen and antimony.

3 ORDERING INFORMATION

EXTENDED TYPE NUMBER	DESCRIPTION MEMORY TYPE	PACKAGE NAME	PACKAGE OUTLINE VERSION	TEMPERATURE RANGE (°C)
PCF7961XTT/C1AErrff	16 KB EROM	TSSOP20	SOT360-1	-40°C to +85°C
PCF7961XTT/C1AE0915	16 KB EROM	TSSOP20	SOT360-1	-40°C to +85°C
PCF7961XTT/C1AC0915	8 KB EROM	TSSOP20	SOT360-1	-40°C to +85°C
PCF7961XTT/C1ACrrff	8 KB EROM	TSSOP20	SOT360-1	-40°C to +85°C

Note

1. PCF7961XTT/C1AE0915 and PCF7961XTT/C1AC0915 represent the E-ROM product for development and applications with low quantities. E-ROM programming shall be performed by the customer. The Monitor and Download Interface (MSDA/MSCL) supports E-ROM download and ERASE/WRITE as fast as 700ms for 4 kByte.
2. PCF7961XTT/C1AErrff and PCF7961XTT/C1ACrrff represent a customized product. The ROM Library is specified by a 2 digit code at location marked „rr“. Under certain conditions, NXP may perform E-ROM programming with customer application code and customer EEPROM pattern. The customer E-ROM and EEPROM FabKey is specified by a 2 digit code at location marked „ff“.

4 TYPICAL APPLICATION

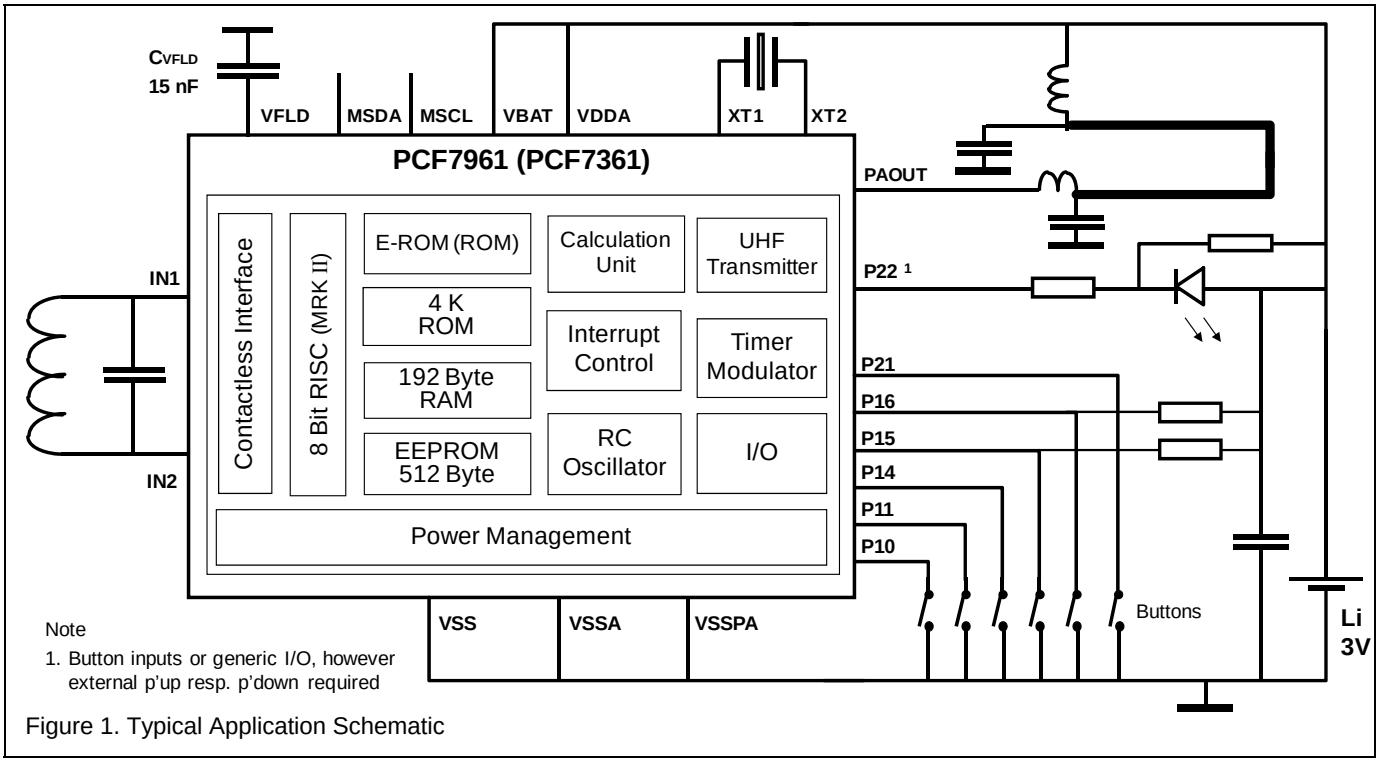


Figure 1. Typical Application Schematic

Note

1. Since most of the device ports do not feature an on-chip pull-up or pull-down, corresponding application measures are required to avoid a floating port, when operating as input (e.g. during POWER-OFF mode). This is applicable for ports P15, P16 and P22.
2. The value of C_{VFLD} need to be selected, according to the system properties, see section 22.1.

5 BLOCK DIAGRAM

The PCF7961X features a high level of integration and requires few external components only, to operate as Security Transponder and/or Keyless Entry Solution. The device incorporates the following circuitry, see Figure 2.

Contactless Interface

Rectifier and Voltage Limiter
Modulator
Clock Recovery
Demodulator
LF Field Detection

Power Management

Supply Switch
Supply Switch Logic
Power On Reset
Port Up Sense

Calculation Unit

Test/Debug Logic

RISC Controller

8 Bit RISC (MRK II family)
ROM, System Code Memory
E-ROM (ROM), Application Code Memory
RAM
EEPROM
Interrupt Control
Timers / Counters
I/O Ports
Programmable Voltage Comparator
System Clock (including on-chip RC oscillator)
Watchdog Timer

UHF Transmitter

XTAL Oscillator
Phase Locked Loop (PLL)
Power Amplifier
Control Logic

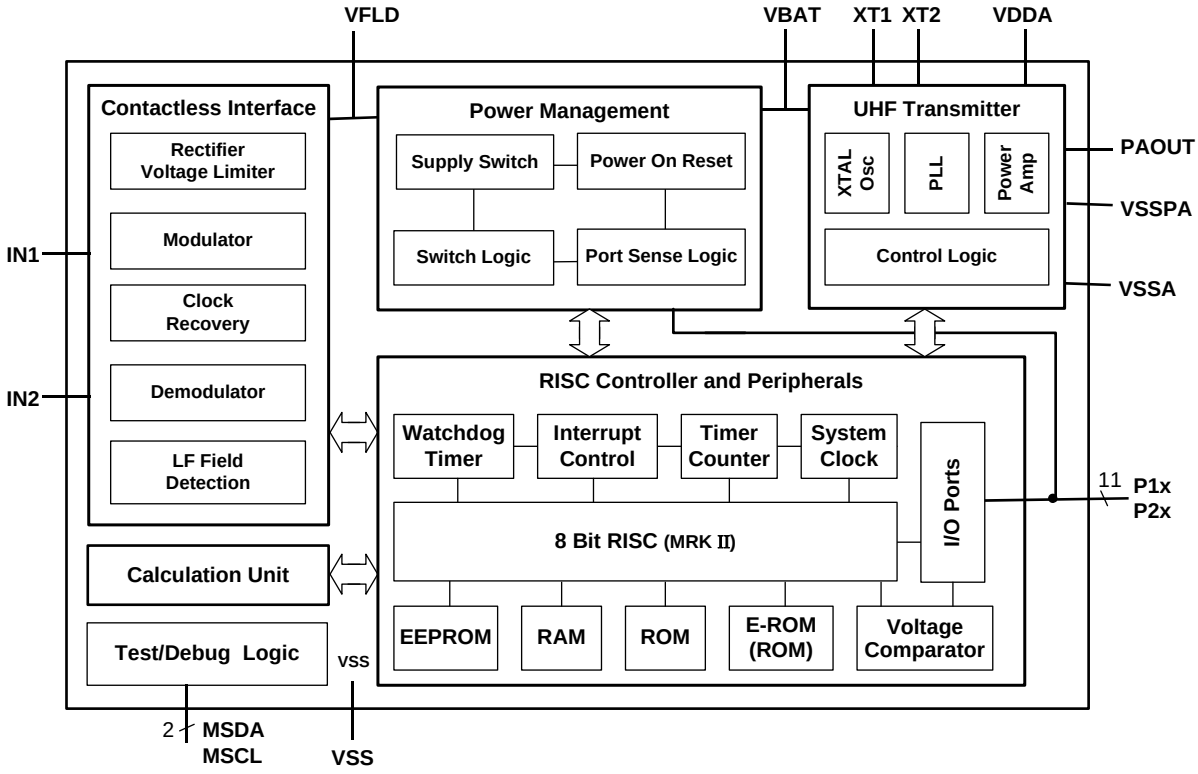


Figure 2. Block Diagram

6 QUICK REFERENCE DATA

Transponder Emulation

PARAMETER		VALUE	UNIT
Carrier frequency		125	kHz
Data rate	READ	4.0	kbit/s
	WRITE (typ)	5.2	kbit/s
Data coding	READ	Manchester or Bi-Phase	
	WRITE	Binary Pulse Length Modulation (BPLM)	
Data transmission mode		Half-Duplex	
Modulation		Amplitude Shift Keying (ASK)	
Identifier (serial number and product type ID)		32	bit
Secret Key		96	bit
Authentication time (typ)		53	ms
Special Features, Note 1	• Ciphered mutual authentication and data transmission, according to HT2 Security Algorithm • Functional compatible with Security Transponder PCF7938XA.		

Note

1. Custom features may be implemented by a corresponding user application code.

RISC Operation

PARAMETER	VALUE	UNIT
Operating supply voltage (RISC)	2.1 – 3.6	V
Power-down current	100	nA
ROM (System Code Memory)	4 K	Byte
E-ROM (Application Code Memory)	16 K (E-ROM)	Byte
RAM (user)	192	Byte
EEPROM	512	Byte
General purpose I/O	7 (TSSOP20)	
Operating speed, as derived from on-chip RC oscillator	0.125 – 2	MHz

Special Features	• EEPROM Erase/Write over full operating voltage range (2.1 to 3.6 V) • Capable to derive power supply from Contactless LF Interface • Full control over Contactless LF Interface • Programmable voltage comparator for battery voltage monitoring • PWM generation • Watchdog timer • Up to seven dedicated button inputs • 32 bit serial number and product type identifier
Calculation Unit	• Supports Standard HT2 or HT3 security algorithm (Secret Key 48 or 96 bit) • Supports Pseudo Random Number generation (Rolling Code) • Compatible with product family e.g. PCF7938XA, PCF7x41XTT, PCF7952XTT, PCF7953XTT

UHF Transmitter

PARAMETER		VALUE	UNIT
Operating supply voltage		2.1 – 3.6	V
Supply current (434 MHz)			
TRANSMIT mode		9.8	mA
LOCKED mode		1.5	mA
Carrier frequency		315 or 434	MHz
Output power (434 MHz)		9	dBm
Special Features	• Programmable XTAL load capacitance • Programmable FSK modulation characteristics • Programmable output amplitude • Programmable ASK modulation characteristics		

7 PINNING

FUNCTION	DESCRIPTION	PIN TSSOP20	NOTE
IN1	Input, Transponder Interface (Coil)	1	
IN2	Input, Transponder Interface (Coil)	2	
P14	General purpose I/O with switch able internal pull-up and Wake Up sense	3	
VBAT	Battery Supply Voltage (Battery pos. Terminal)	4	
P11	General purpose I/O with internal pull-up and Wake Up sense	5	
P22	General purpose I/O, Wake Up sense and Timer 1 compare output (PWM)	6	
P21	General purpose I/O, with switch able internal pull-up, Wake Up sense and Timer/Counter 1 Capture input / Interrupt input	7	
MSCL	ROM Monitor Serial Clock Output	8	1
MSDA	ROM Monitor Serial Data with internal pull-up	9	1
XT2	XTAL Oscillator	10	
XT1	XTAL Oscillator	11	
VSSA	Transmitter analogue ground	12	
VDDA	Transmitter analogue supply voltage	13	
VSSPA	Transmitter power amplifier ground	14	
PAOUT	Transmitter power amplifier output	15	
P10	General purpose I/O with internal pull-up and Wake Up sense	16	
P15	General purpose I/O, external clock input and Wake Up sense	17	
P16	General purpose I/O, Voltage comparator input and Wake Up sense	18	
VSS	Common Ground (Battery neg. Terminal)	19	
VFLD	Rectified LF Field Supply Voltage	20	

Note

1. MSCL is an open drain output in PUSH configuration and must be left unconnected in the application. During in-circuit flashing or debugging an external pull down resistor is required for proper operation. MSDA features an on-chip pull-up to VBAT. MSDA may be left open or terminated to VBAT, as desired. For field use, the device shall be configured for PROTECTED mode, after the application code has been flashed, see section 12.

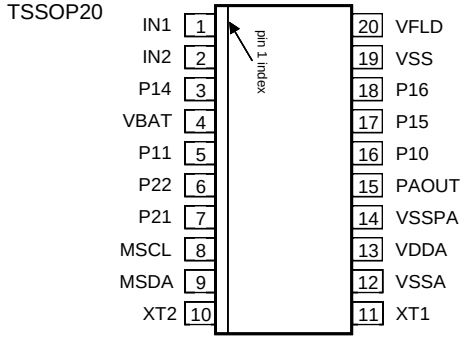


Figure 3. Pin Configuration

8 POWER MANAGEMENT DESCRIPTION

The PCF7961X features a versatile Power Management enabling the device to derive its power supply from either the external battery or the LF Field, as selected by the on-chip Supply Switch, Figure 4. The UHF Transmitter is operational only, if the device supply is derived from the battery. However, the XTAL Oscillator is operational in any case, see also section 21.1.

Determining the appropriate supply configuration and hence Supply Switch state, is accomplished by means of the Supply Switch Logic and the ROM implemented device BOOT sequence. During device power-up the Supply Switch Logic will evaluate the supply condition and set the Supply Switch accordingly. Subsequently, the RISC Controller will commence program execution, starting with the BOOT sequence, which under certain conditions will change the Supply Switch state, hence change the supply configuration, before the application program is executed finally. Such condition may apply, in case an LF Field and button press is detected at the same time.

Each supply configuration corresponds to a certain device operating mode, referred to as BATTERY, TRANSPONDER or POWER-OFF Mode. The device is supplied either from an external battery (BATTERY Mode) or from the LF Field (TRANSPONDER MODE) or virtually consumes no power at all (POWER-OFF Mode).

In case the device is supplied from the rectified LF Field (pin VFLD), an on-chip low dropout voltage regulator is operational, adjusting the voltage to fit the internal chip supply voltage specification (V_{DD}).

The Power Management features a set of control bits and flags to influence the supply condition and program execution as desired.

In any case, a Power On Reset circuitry monitors the device supply voltage (V_{DD}), forcing the device into the reset state (MRST), in case the chip supply voltage drops below the Power On Reset threshold voltage. The Power On Reset circuitry is able to detect voltage dips as short as 10 us and features a hysteresis of typical 80 mV. Once triggered, the Power On Reset will be prolonged ($t_{POR-HLD}$) by a corresponding mono-flop, to ensure proper device start-up. A device reset is also generated in case an LF Field Detect is detected (LF-RST), provided the LF Field Detect circuitry is configured accordingly, see also section 9.4. Moreover, a device reset may be forced upon instruction, by triggering the control bit RST

After battery power-up, the device enters either POWER-OFF or BATTERY Mode. Thus, the application program cannot detect, that the battery has been changed or has been inserted, see also section 22.9.

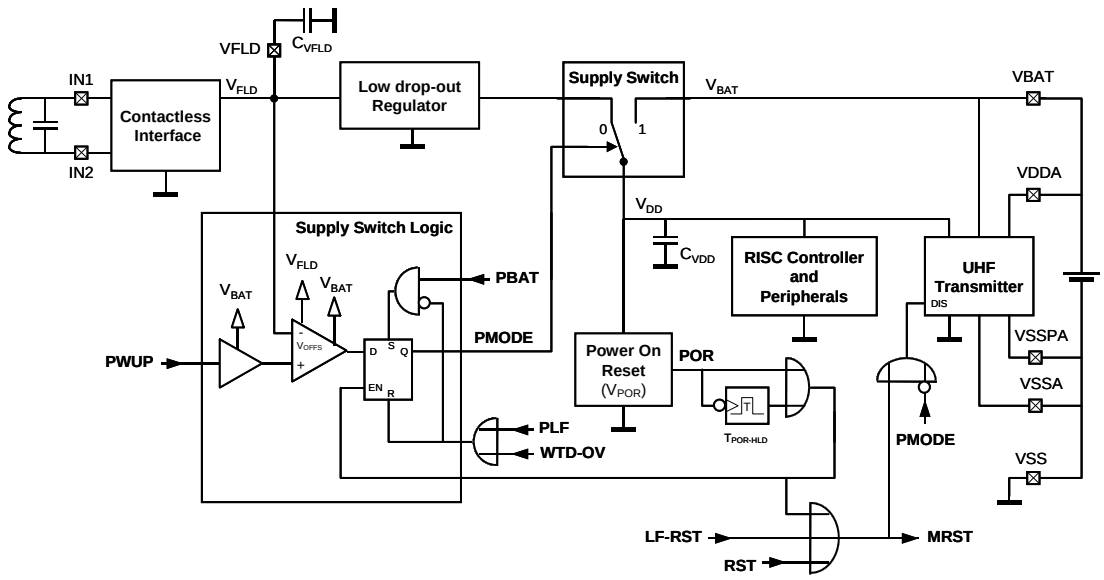


Figure 4. Power Management

Note

1. For information only, the on-chip capacitor C_{VDD} yields 2nF

8.1 Supply Switch Logic

The Supply Logic selects the appropriate Supply Switch state during device power-up. It evaluates the supply condition and responds to a Port Wake-Up (PWUP) event or LF Wake-Up event, see Figure 4.

The Supply Switch is controlled by a flip-flop that is forced into transparent state, whenever the device supply voltage (V_{DD}) stays below the Power On Reset threshold. By default the device is configured for LF Field supply (PMODE = 0), even if no LF Field is present, meaning that the voltage at pin VFLD is zero. This is achieved by means of a small offset voltage introduced at the negative comparator input.

Regardless of the supply condition, once the supply voltage (V_{DD}) exceeds the Power On Reset threshold voltage ($V_{POR,BAT}$ respectively $V_{POR,FLD}$), POR becomes low. After a short delay ($t_{POR,HLD}$), the flip-flop is forced into latch state freezing the supply switch state and the RISC Controller becomes operational. Program execution commences starting with the BOOT Routine, before the application Program or Transponder Emulation is being invoked (see Figure 5 and section 14).

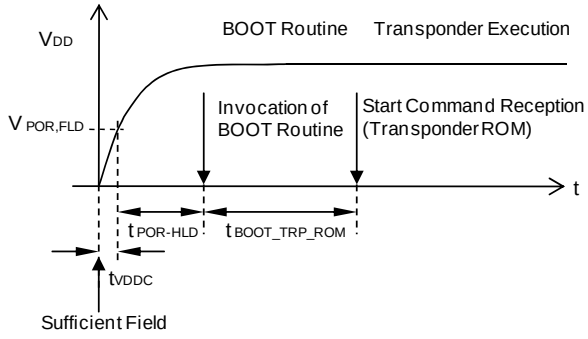


Figure 5. Power up timing Transponder Emulation

Altering the supply condition, hence state of the supply switch, during RISC operation is feasible upon instruction only. Latter one may be desired under certain conditions, e.g. when an LF Field is being detected, while battery supply has been utilized so far. To alter the supply condition, the flip-flop state may be changed by triggering the control bits PBAT and PLF.
If the Watchdog Timer is allowed to overflow in BATTERY mode, the Supply Switch will be forced to LF Field supply, typical causing a device reset, see also section 11.6.

Presence of LF Field

In case the LF Interface is fed by a corresponding input signal, due to the presence of an LF Field, it is rectified and charges the capacitor C_{VFLD}. As the voltage develops at pin VFLD (V_{FLD}), the low dropout voltage regulator becomes operational. As soon as the chip supply voltage (V_{DD}) exceeds the Power On Reset threshold voltage ($V_{POR,FLD}$), the signal POR becomes low. After a short delay ($t_{POR,HLD}$), the flip-flop is forced into latch state freezing the supply switch state (PMODE = 0). Hence, the device is supplied from the LF Field, regardless of any subsequent Port Wake Up events (button press) and unless changed by the application program.

Port Wake Up (button press)

In case no LF Field is present and a Port Wake Up condition is applicable, e.g. one of the button input is forced low, the comparator forces the flip-flop into high state (PMODE = 1). Consequently, the device is connected to the battery. As soon as the chip supply voltage (V_{DD}) exceeds the Power On Reset threshold voltage ($V_{POR,BAT}$), the signal POR becomes low. After a short delay ($t_{POR,HLD}$), the flip-flop is forced into latch state freezing the state of the supply switch. Hence, the device is supplied from the battery, regardless the voltage that may develop at pin VFLD subsequently.

However, since it is desired to give LF Field supply, hence transponder operation, priority over battery supply, the device will respond to an LF Field detected, by overwriting the flip-flop state and changing the supply condition according to section 9.4.

Presence of LF Field and Port Wake Up (button press)

In case an LF Field and a Port Wake Up condition, e.g. button press, are present at the same time, LF Field supply is forced by default, since the voltage at VFLD exceeds the battery voltage (V_{BAT}) typically. Consequently, the comparator forces the flip-flop into low state. Anyhow, in case of a weak LF Field and higher battery voltage the supply switch may be set for battery supply initially, which subsequently would be changed to LF Field supply by the BOOT routine, provided the LF Field triggered the LF Field Detection circuitry, thus is detected to exceed the LF Field Detect threshold voltage ($V_{THR,FD}$ respectively $V_{THR,FD-VIN}$). In the latter case, the LF Field can be expected being sufficiently strong to support device operation, see also section 9.4.

8.2 Device Operating Modes

The device resides in one of three modes, POWER-OFF, BATTERY or TRANSPONDER Mode, see Figure 6.

Each mode corresponds to a certain device supply configuration. Hence the device is supplied either from an external battery (BATTERY Mode) or from the LF Field (TRANSPONDER Mode) or virtually consumes no power from the battery at all (POWER-OFF Mode).

The device resides in POWER-OFF Mode any time a Power On Reset condition is applicable, either because of a weak supply condition or forced by the application program. The POWER-OFF Mode is terminated, upon a Wake Up event, e.g. presence of an LF Field or Port Wake Up (button press). Once the Supply Switch Logic evaluated the supply condition during device power-up and the BOOT sequence completed, the device will commence execution of the application program in either BATTERY mode or TRANSPONDER mode.

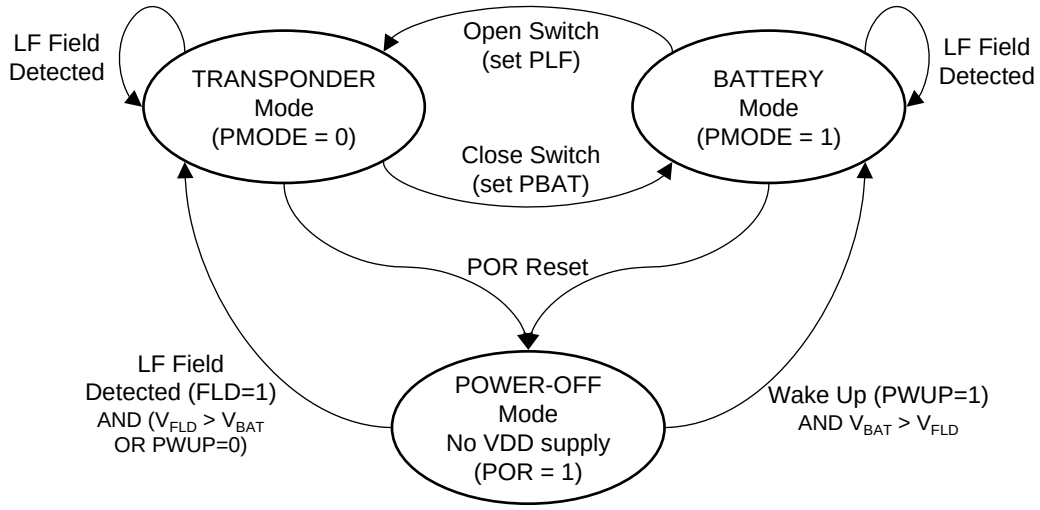


Figure 6 Device Operating Modes

8.2.1 POWER-OFF Mode

In POWER-OFF Mode, the internal Supply Switch disconnects the device from the battery (PMODE = 0), making the device to drain virtually no current from the battery. The internal device supply voltage (V_{DD}) stays below the power on reset threshold voltage ($V_{POR,FLD}$) and device operation is halted. Only a minimum of circuitry remains operational, like the Power Management and I/O Port circuitry, however, latter one is configured for input mode in any case.

The POWER-OFF Mode is terminated and BATTERY Mode entered, upon a Port Wake Up (WUP = 1), in case one of the button inputs has been forced low at least (see also section 8.3). Considering an LF Field is present in the same moment, the BOOT sequence will terminate the BATTERY Mode and interrogates the TRANSPONDER Mode instead, provided the LF Field is strong enough and triggered the LF Field Detect circuitry (FLD = 1). Latter one is the case, when the LF Field applied exceeds the LF Field Detect threshold voltage ($V_{THR,FD}$ resp. $V_{THR,FD-IN}$) (see also section 9.4).

The POWER-OFF Mode is terminated and TRANSPONDER Mode entered, whenever a proper LF Field supply condition is applicable, as evaluated by the Supply Switch Logic, see also section 8.1.

8.2.2 BATTERY Mode

In BATTERY Mode, the internal Supply Switch connects the battery with the device supply (PMODE = 1) and powers the device from the external battery.

Device operation is controlled by the RISC and the corresponding program code. Program execution starts with the BOOT sequence before control is passed to the corresponding WARM BOOT vector enabling the application code to be executed (see also section 14).

In case no LF Field is detected while executing the BOOT sequence, control is passed to the WARM BOOT vector BATTERY (0000_H) finally. Otherwise, in case the LF Field Detect circuitry is detected being triggered (FLD = 1), the BOOT sequence will terminate the BATTERY Mode and interrogate the TRANSPONDER Mode. This would disconnect the device from the battery and force an LF Field supply condition. Depending on the device configuration, the BOOT sequence immediately invokes the corresponding transponder emulation or directly branches to the WARM BOOT vector TRANSPONDER (0010_H) (see also section 11.1.1.2).

Once control has been passed to the corresponding WARM BOOT vector, the application code is responsible to handle and respond to any subsequent events appropriately, e.g. LF Field detected, including transponder invocation.

Upon instruction, the application code may terminate the BATTERY Mode at any time, by clearing the latch PMODE. This is accomplished, by triggering the control bit PLF. As a result, the device supply will be derived from the LF Interface and the subsequent device behavior depends on the supply and Wake Up condition.

In case no LF Field is present, and the device supply drops below the Power On Reset threshold, the device enters POWER-OFF Mode. However, the effects of residual charge at pin VFLD need to be taken into account, in order avoid undesired device operation, see section 22.5. In the moment the device enters POWER-OFF Mode, the Supply Switch Logic will take over device control.

In case an LF Field is present, device operation continues in TRANSPONDER Mode, however, the BOOT sequence is not being executed by default and the application code responsible to take the necessary actions, e.g. transponder invocation.

8.2.3 TRANSPONDER Mode

In TRANSPONDER Mode, the internal Supply Switch disconnects the battery from the device supply (PMODE = 0), instead, the internal device supply is derived from the LF Interface, hence the rectified LF Field (V_{FLD}).

The device operation is controlled by the RISC and the corresponding program code. Program execution starts with the BOOT sequence before control is possibly passed to the corresponding WARM BOOT vector (TRANSPONDER, 0010H) enabling the application code to be executed (see also section 14). Depending on the device configuration, the BOOT sequence will immediately invoke the corresponding transponder emulation or branch to the WARM BOOT vector directly (see also section 11.1.1.2).

Once control has been passed to the WARM BOOT vector, the application code is responsible to handle and respond to any subsequent events appropriately, e.g. LF Field detected, including transponder invocation.

Upon instruction, the application code may terminate the TRANSPONDER Mode at any time, hence setting the latch PMODE, by triggering the control bit PBAT. Consequently, the device supply would be derived from the battery subsequently. In case the battery supply does not exceed the Power On Reset threshold, a Power On Reset condition applies. Consequently, the Supply Switch Logic takes device control and forcing the device to resume LF Field supply and eventually to start over again.

The POWER-OFF Mode cannot be entered upon instruction, instead POWER-OFF Mode will be entered as soon as the supply voltage drops below the Power On Reset threshold. However, the effects of residual charge at pin VFLD need to be taken into account, in order avoid undesired operation, see also section 22.5. In the moment the device enters POWER-OFF Mode, the Supply Switch Logic will take over device control.

8.3 Port Sense Logic

The Port Sense Logic provides means to wake up the device from POWER-OFF mode or to trigger a corresponding interrupt during program execution, by designated I/O ports (button inputs), according to Figure 7.

Upon a high-to-low transition the corresponding port mono-flop is triggered and remains set for the specified time (T_{PSMF}), regardless of the subsequent port state. The mono-flop is triggered again upon a high-to-low transition only. Provided the corresponding port is configured for input mode and is not being used in a different context, Port Trigger occurs and a corresponding interrupt request is generated.

When the device resides in POWER-OFF Mode, hence POR (Power On Reset) being high, Port Trigger will set a flip-flop, signaling a Port Wake-Up event. As the RISC Controller resides in Power On Reset state, the Port Interrupt is not being detected. The Supply Switch Logic monitors the state of this flip-flop and will respond to the Port Wake-Up event accordingly, see section 8.1.

The Port Wake Up flip-flop is cleared in the moment the device Power On Reset (POR) vanishes, e.g. as soon as the power-on reset circuitry detects a valid operating voltage, causing the device to commence program execution. Subsequent Port Trigger events, e.g. possibly caused by button bouncing, will be handled as Port Interrupts and the application program shall respond as desired.

In any case, Port Trigger is supported only, if the designated ports are configured for input mode, hence the corresponding port direction control bit is cleared (IOxx), see section 11.7. Further, the ports must not be used in a different context, possibly overruling the port direction control bit. E.g. P15 as external Timer Counter clock input, see section 11.4 respectively section 11.5; P16 as external Voltage Comparator input, see section 11.9, P21 as Timer 1 Capture input respectively P22 as Timer 1 Pulse Width Modulator output, see section 11.5.

While the device resides in POWER-OFF mode, any of the above mentioned ports generates a Port Wake Up event, because the I/O port are in any case forced into input mode and the Wake Up feature cannot be disabled. In order to avoid unintended device Wake Up, special care is required, when using one of the above ports as an ordinary I/O, see section 22.7.

In any case, it is necessary to establish static non-floating conditions in port input mode, in order to avoid an undesired quiescent current to be drawn from the battery. As the ports are falling edge sensitive, both, pull-up or pull-down measures are allowed to define the static level. Please note that P10 and P11 already feature an on-chip pull-up and Port P14 and P21 an on-chip pull-up that is active only, when the port operates in input mode.

After battery power-up, the device either enters POWER-OFF or BATTERY Mode. Thus, the application program cannot detect, that the battery has been changed or has been inserted, see also section 22.9.

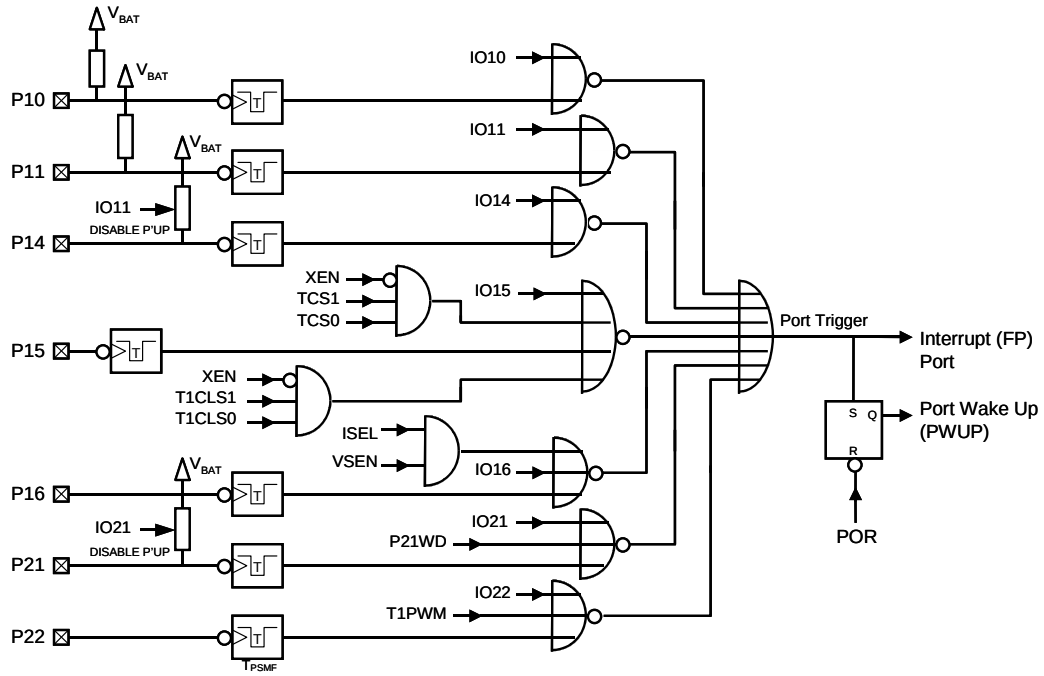


Figure 7. Port Sense Logic

8.4 Power Management Control Register

The Power Management features a set of control bits and flags to influence device operation, arranged in the Power Control register, PCON, that is located in the SFR space of the data memory, see Table 1.

Table 1 Power Control Register, PCON

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
NMI	X	FLD	PMODE	RST	PBAT	PLF	IDLE
R/W	W0	R	R	R0/W1	R0/W1	R0/W1	R0/W

Note Address = 26H

1. Bits marked ‘X’ are not connected and reserved for future use. Any read operation yields an undefined result. For future compatibility, any write operation should assign a ‘0’.
2. RST, PBAT, PLF and IDLE provide a trigger signal for the corresponding circuitry. Any read operation yields zero as result.
3. PBAT and PLF must not be set to ‘1’ simultaneously.
4. RST must not be set to ‘1’ simultaneously with PBAT or PLF.

FLD, Field Detected

The flag FLD signals the presence of an LF Field by monitoring the rectified LF Field supply. If latter one exceeds the LF Field Detect threshold voltage ($V_{THR,FD}$ respectively $V_{THR,FD-IN}$) FLD is set, otherwise it is cleared, see also section 9.4.

PMODE, Power Mode

The flag PMODE signals the current state of the Supply Switch, hence, applicable supply condition, according to Table 2.

Table 2 Power Modes

PMODE	Supply Condition	Note
0	LF Field supply	
1	Battery supply	

The state of PMODE cannot be altered directly. Instead, indirect control is provided by the control bits PBAT and PLF.

PBAT, Power from Battery

The control bit PBAT provides means to force device supply from battery. Any access that writes a ‘1’ to PBAT will set the Supply Switch accordingly (PMODE = 1). However, PLF must not be set in the same moment.

In any case, when changing the supply condition, the application program shall ensure that the new supply condition is sufficient to supply the device and shall force the device operating current to a minimum during the transition. Otherwise, must be aware of an unexpected Power On Reset event.

PLF, Power from LF Field

The control bit PLF provides means to force device supply from the LF Field. Any access that writes a ‘1’ to PLF will set the Supply Switch accordingly (PMODE = 0).

In any case, when changing the supply condition, the application program shall ensure that the new supply condition is sufficient to supply the device and shall force the device operating current to a minimum during the transition. Otherwise, must be aware of an unexpected Power On Reset event. It is recommended to use the corresponding ROM library function (PM_ENABLE_LF), see section 23.

RST, RESET device

The control bit RST provides means to immediately reset the entire device, causing the device to initialize all Special Function Register to their corresponding reset value and to invoke the boot sequence. The Supply Switch, hence supply condition (PMODE), is not affected directly by the reset, however, will eventually be modified during the boot sequence (see section 14).

This feature is of convenient use, in case an LF Field is being detected, in order to invoke the transponder emulation via the BOOT sequence.

NMI, Non Maskable Interrupt control

The control bit NMI provides means to configure the device behavior upon detection of an LF Field (FLD = 1), according to Table 3.

Table 3 NMI Control

NMI	Low to High transition of FLD	Note
0	Trigger device reset	
1	Trigger NMI (Non Maskable Interrupt, INT0)	

In case NMI is cleared, a low to high transition of FLD will reset the entire device, causing the device to initialize all SFR to their corresponding reset value and to invoke the boot sequence. The Supply Switch, hence supply condition (PMODE), is not affected directly by the reset, however, will eventually be modified during the boot sequence (see section 14).

In case NMI is set, the Non Maskable Interrupt, NMI, will be triggered and the corresponding interrupt service routine will be invoked. This feature allows to protect “critical” sections of the application program from being terminated by a reset due to the detection of an LF Field, see also section 22.8.

After a device Power On Reset, the NMI bit is cleared, and resets will be generated upon each LOW-to-HIGH transition of FLD.

IDLE, IDLE Mode

The control bit IDLE, provides means to force the RISC Controller into IDLE mode. Any access that writes a '1' to IDLE will cause the device to halt program execution after completion of the corresponding instruction, by inhibiting the CPU clock. However, the system clock and all peripherals stay operational. The IDLE mode terminates and program execution is resumed upon a corresponding event, see Interrupt System and IDLE Control, section 11.2.5.

9 CONTACTLESS INTERFACE DESCRIPTION

The Contactless Interface provides the means to utilize the PCF7961X as a contactless transponder, capable to derive its power supply and system clock by inductive coupling to an LF Field generated by a corresponding base station. Further, to utilize the same LF Field to receive data from and transmit data to the base station under control of the RISC Controller. An external LC resonant circuit needs to be connected to the coil inputs (IN1 and IN2) of the Contactless Interface, see Figure 8.

Independent from the device operating mode, the Contactless Interface is capable to detect the presence of an LF Field and provides a corresponding signal to Wake Up the device from POWER-OFF mode or to interrupt device operation.

The PCF7961X features build-in means to emulate the NXP transponder family PCF 7938XA, that may be extended by user programmed functions. Please consult the corresponding ROM Library description (see section 23).

The Contactless Interface comprises an LF Rectifier, Voltage Limiter, LF Field Detection, Modulator, Demodulator and Clock Recovery circuitry, see Figure 8.

9.1 LF Rectifier and Voltage Limiter

The LF Rectifier operates in full-bridge configuration, charging an external capacitor connected to pin VFLD. A shunt Voltage Limiter is provided to ensure that the voltage at pin VFLD does not exceed the specification. In any case, the interface input current must not exceed the specified limits. The rectifier characteristics are shown in Figure 9b.

The data communication with the device employs Amplitude Shift Keying (ASK) of the LF Field. The modulation duration and LF Field strength must be chosen such that the rectified supply voltage stays above the Power On Reset threshold during the LF Field low condition, see Figure 10.

In case the LF Field is low for a certain duration or switched off, the device will generate a Power On Reset after the specified time ($t_{RESET,SETUP}$), which is desired, in order to provide means to force a device reset during contactless operation, see Figure 10.

9.2 Modulator

The Contactless Interface utilizes absorption modulation of the LF Field to send data to the base station. The modulation timing is fully determined by the RISC Controller operating the node LFMOD accordingly.

Absorption modulation is accomplished by applying an additional load (S2 closed) across the coil inputs. The absorption modulation characteristics depend on the source impedance of the external resonance circuit, the modulation load impedance ($R_{1\text{-}LIN}$, $R_{1\text{-}NLIN}$ and $R_{2\text{-}LIN}$), the Voltage Limiter and the internal power consumption of the device. The applied load (S2) is different for each of the two half waves of the carrier, due to clock recovery reasons. The typical modulation characteristics are shown in Figure 9a.

A dedicated Digital Modulator circuit is provided to easily implement Manchester coding, see section 11.8.

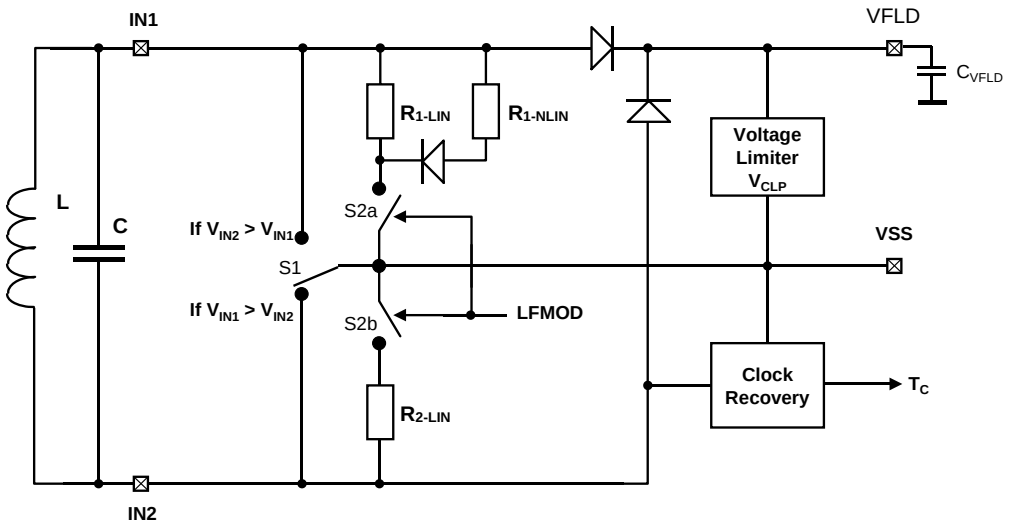


Figure 8. Contactless Interface Rectifier, Voltage Limiter and Modulator circuitry

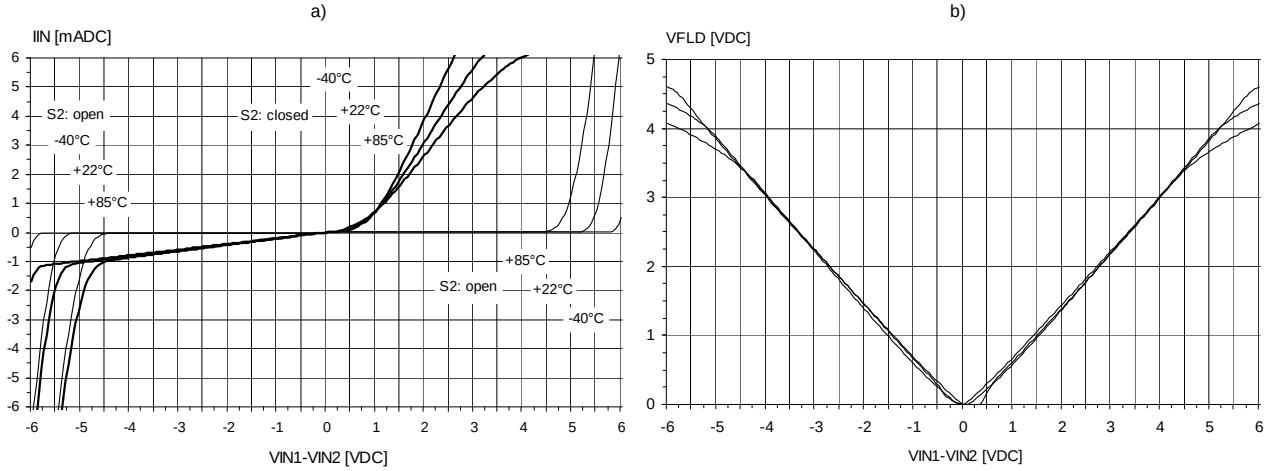


Figure 9. Typical modulation (a) and LF Rectifier (b) characteristics

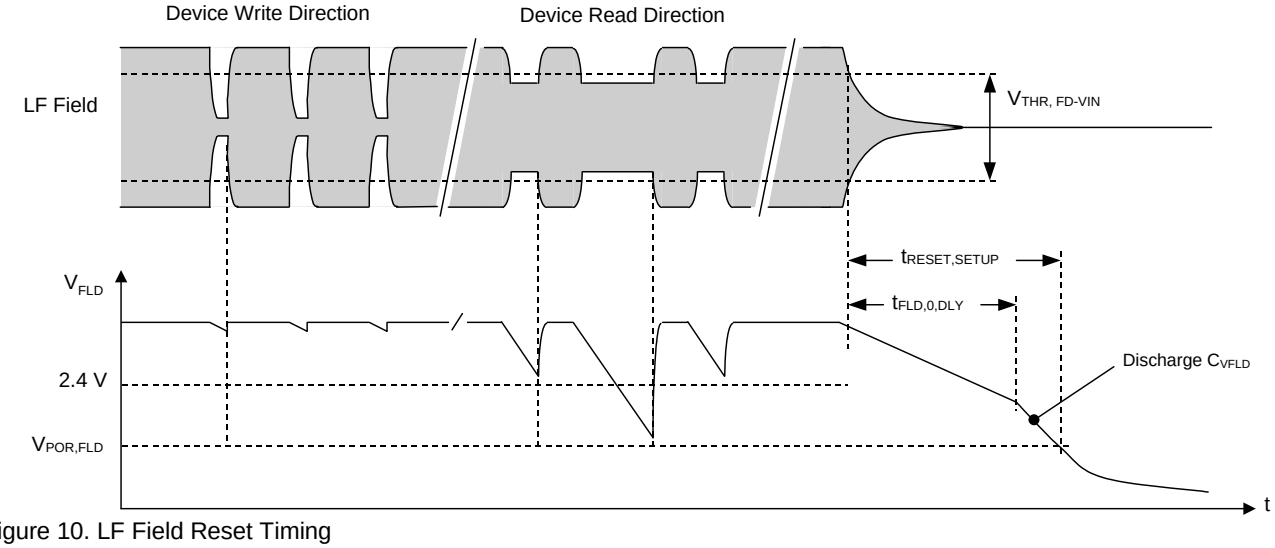


Figure 10. LF Field Reset Timing

9.3 Demodulator

The Contactless Interface utilizes On-Off-Keying (OOK) of the LF Field to receive data from the base station. The demodulator circuitry has been designed to fit the modulation characteristics as implemented by the NXP Transponder PCF7938XA. The Demodulator senses the differential voltage across the coil inputs (pin IN1 and IN2) and signals a corresponding LF Field LOW condition by means of the control bit LFD, see Figure 11 and Figure 12.

Once enabled by the control bit LFEN, the demodulator freezes the internal demodulator threshold and is operational after a short settling time (t_{ADLY}). The demodulator is designed for temporary operation only and provides its specified operation for a certain duration (t_{IDLE}) only. After that, its characteristics are undefined and it needs to be disabled for a certain time (t_{DSETUP}) before it is enabled again, in order to refresh the demodulator threshold. Hence, data reception as a string is limited accordingly. In any case, the Demodulator signals the LF Field LOW condition only, and the RISC Controller needs to decode the data string bit by bit subsequently. For this reasons, the control bit LFD is also routed to the Timer/Counter 1 Capture Logic, in order to support timer based decoding of the serial data string, see also 11.5.

The demodulator output (LFD) may bounce during the LF Field LOW to HIGH transition, and it is recommended to trigger the Timer/Counter 1 Capture Logic by the rising edge of the demodulator output (LFD).

The Demodulator control bits are arranged in the Demodulator Control register, DEMCON, that is located in the SFR space of the data memory, see Table 4.

Table 4 LF Demodulator Register, DEMCON

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
LFD	X	X	X	X	X	X	LFEN
R	W0	W0	W0	W0	W0	W0	R/W

Note Address = 1CH

1. Bits marked ‘X’ are not connected and reserved for future use. Any read operation yields an undefined result. For future compatibility, any write operation should assign a ‘0’.

LFEN, LF Demodulator Enable

When the control bit LFEN is set, the Demodulator is enabled, otherwise disabled. In the moment the Demodulator is forced from disabled to enabled state, it will set and freeze its demodulator threshold and be operational for the specified time (t_{IDLE}). After that time, its operation is not specified. During a LF Field modulation phase the demodulator shall be disabled

LFD, LF Demodulator Data

When the demodulator detects a LF Field LOW modulation, LFD is set, otherwise it is cleared, provided the Demodulator is enabled and the IDLE time did not elapse (t_{IDLE}). While the demodulator is disabled, the LFD bit yields a one.

During Demodulator settling (t_{ADLY}) LFD is undefined and may change randomly, which needs to be taken into account, e.g. by disabling the Timer/Counter 1.

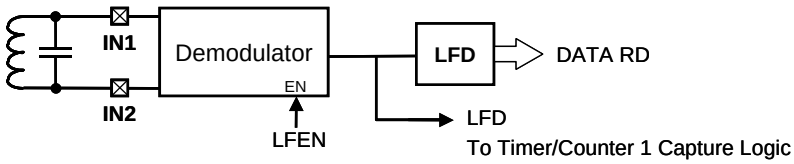


Figure 11. Demodulator Block Diagram

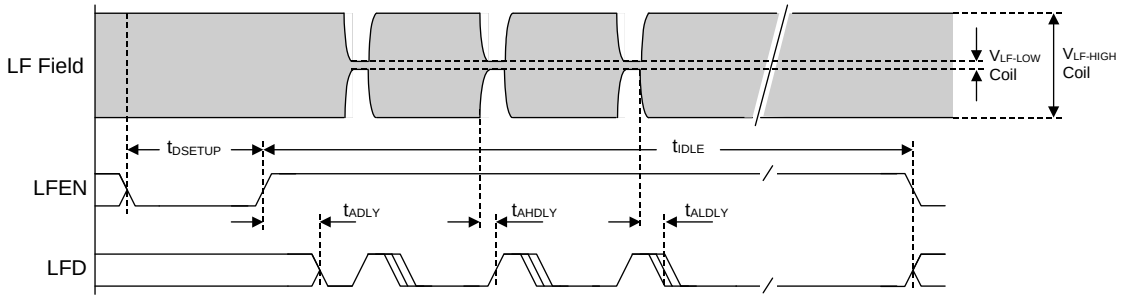


Figure 12. Demodulator Timing

9.4 LF Field Detection

Independent of the actual device operating state, the Contactless Interface is capable to detect the presence of an LF Field, in order to Wake Up the device from POWER-OFF mode or to interrupt device operation, see Figure 13 and Figure 14.

The circuit comprises of an independent envelope detector that senses the differential voltage across the coil inputs (pin IN1 and IN2) followed by a comparator. The LF Field envelope is compared with a certain threshold, which by design is greater than the power-on reset threshold ($V_{POR,FLD}$), forming the Field Detect flag, FLD. Latter one turns high, when the LF Field exceeds the Field Detect threshold ($V_{THR,FD-VIN}$) and it may be tested by the RISC Controller when desired.

The envelope detector integration constant is chosen such that the data transmission write pulse (T_{WRP}), during transponder data reception, does not toggle the Field Detect flag. Instead the LF Field needs to be off for a certain time ($t_{FLD,0-DLY}$) before FLD becomes low, see Figure 14.

Whenever FLD turns low, certain device circuitry will be activated (e.g. RC Oscillator), in order to consume the charge stored in the external capacitor at pin VFLD and as a result, to safely generate a device reset, satisfying the LF Field Power On Reset setup time specification ($t_{RESET,SETUP}$), see also section 9.1. In addition, ensures that the voltage at pin VFLD is low enough ($V_{FLD} < V_{BAT}$), to allow a Port Wake-Up to interrogate the BATTERY Mode.

Depending of the Power Management configuration, a low-to-high transition of Field Detect (FLD) causes either a device reset (LF-RST) or the invocation of the non maskable interrupt (LF Field).

In case NMI is cleared, a low to high transition of FLD will reset the entire device, causing the device to initialize all SFR to their corresponding reset value and to invoke the boot sequence. Otherwise, in case NMI is set, the Non Maskable Interrupt, NMI, will be triggered and the corresponding interrupt service routine will be invoked. This feature allows to protect “critical” sections of the application program from being terminated by a reset due to the detection of an LF Field, see also section 22.8.

In case invocation of the non maskable interrupt is selected and considered operating from battery supply (BATTERY Mode) it is up to the application program, whether to force a LF Field supply condition (TRANSPONDER Mode) or not. However, FLD being set is no guarantee that the available LF Field is sufficient to power the device. A device Power On Reset may eventually occur in case of a weak LF Field, which needs to be taken into account once the LF Field supply condition is forced.

FLD, Field Detected

The flag FLD signals the presence of an LF Field, by monitoring the rectified LF Field supply. In case it exceeds the LF Field Detect threshold voltage ($V_{THR,FD}$ resp. $V_{THR,FD-IN}$) FLD is set, otherwise it is cleared, The Field Detect flag is located in the Power Management Control register, PCON, see section 8.3.

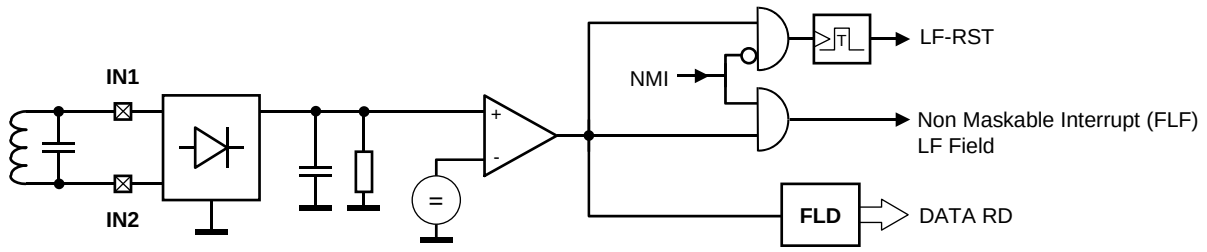


Figure 13. LF Field Detection circuitry

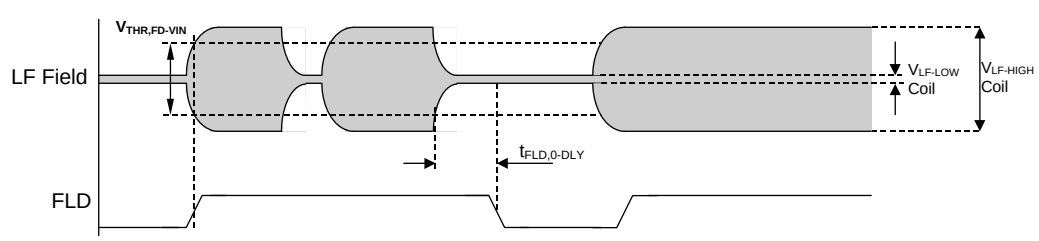


Figure 14. LF Field Detection timing

10 RISC CONTROLLER DESCRIPTION

The PCF7961X is powered by NXP's 2nd generation low power 8-Bit MICRO RISC KERNEL (MRK II) to control device operation in BATTERY and TRANSPONDER Mode.

The MRK II utilizes a Harvard architecture featuring an 8 bit ALU and 16 bit instruction width. Due to the two stage pipeline concept, instructions virtually execute in a single clock cycle, resulting in an ultra low power consumption. The applicable instruction set is downward compatible to the MRK I Family of products, featuring a number of extended addressing modes and architectural enhancements. For a general description of the MRK II core, please refer to the specification MRK II Family, Architecture and Instruction Set, see section 23. However, the PCF7961X specific implementation of the MRK II core is described below.

10.1 Application Code Memory

The PCF7961 provides 16 kByte of Application Code, Each instruction consists of 16 bit and thus occupies two bytes, see Figure 15.

After a device reset, program execution starts with the BOOT routine and subsequently continues with the Application Code, commencing at the corresponding WARM BOOT vector (see section 14). In BATTERY Mode, execution starts from location 0000H, in TRANSPONDER Mode from location 0010H, provided the Transponder Emulation is disabled (TEN = 0, see section 11.1.1.2)..

Transponder Sub Command handling and unresolved SYS calls feature dedicated vectors that are accessed in the corresponding event.

The PCF7961X features 5 interrupt vectors. Each vector is assigned to a fixed location in the memory. INT 5 and INT 6 are reserved for future use.

Interrupt vectors INT 1 to INT 4 can independently be enabled or disabled. If an interrupt is enabled, it causes the RISC controller to perform a CALL operation to the corresponding location, where execution of the Interrupt Service Routine, ISR, commences. E.g. in case of an INT 2 interrupt (Timer 0 Overflow) program execution would commence at memory location 0006H. A JMP instruction needs to be placed at the corresponding location, in order to redirect program execution to the final location of the ISR (interrupt service routine). It is recommended to place a RETI instruction at all interrupt vectors not used.

Interrupt vector INT0 is not maskable (NMI, not maskable interrupt). It is always executed immediately if a request is generated. The behavior of INT0 can be configured according to section 9.4.

In the case of simultaneous interrupts, the interrupt with the lowest vector address is executed first.

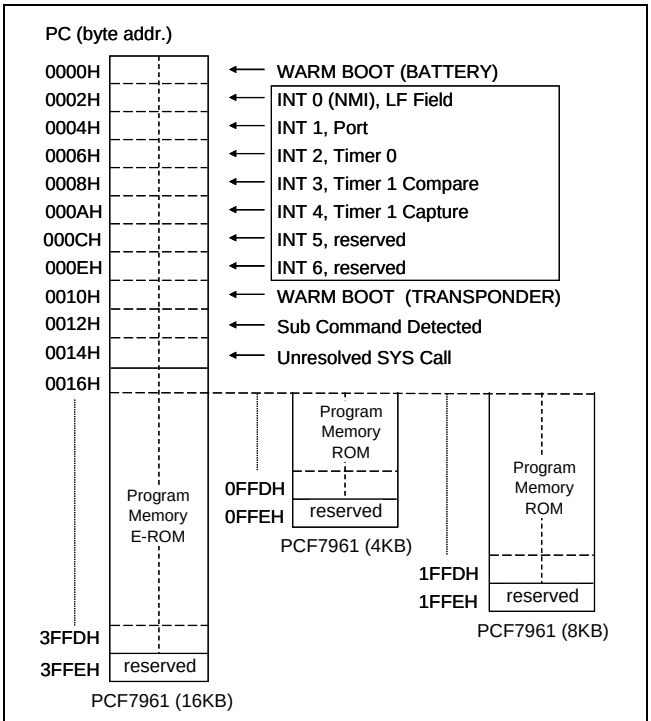


Figure 15. Application Code Memory

Note

1. The upper two bytes are reserved for device configuration purposes in any case and are not available to the application.

10.2 System Code Memory

The PCF7961X features 8 kByte of System Code Memory that holds a predefined NXP implemented ROM Library featuring a set of library functions, the Transponder Emulation, the device Boot routine and controls the in-circuit Monitor and Download Interface. The System Code Memory is not visible to the application. The ROM Library functions and Transponder Emulation are invoked by a System Call (SYS instruction) that passes control back to the application program, when completed.

The Interrupt System is disabled during execution of system code, including the NMI. Thus, any interrupt request is latched only and execution delayed until control is returned to the application code.

For a detailed description of the ROM Library, please refer to specification PCF7x61X ROM Library, Implementation and Description, see also section 23.

Boot Routine

The BOOT routine is invoked immediately after a device reset. The BOOT routine configures the device, e.g. determines the supply condition, evaluates device protection flags, invokes transponder emulation modes according to the EEPROM configuration and passes control to the Application Code accordingly, see section 14.

ROM Library

The ROM library features a set of functions to emulate the NXP HT3 transponder, as well as a set of generic functions. The corresponding functions are invoked from the application program by a System Call (SYS instruction). For more detailed usage, please refer to the specification HT3-Transponder-ROM, Implementation and Description (see also section 23).

In-Circuit Monitor and Download Routine

The in-circuit Monitor and Download Interface provides means for E-ROM and EEPROM initialization and to monitor and manipulate the embedded peripherals in the context of system debugging, employing communication via a two-wire serial interface (MSDA / MSCL), see section 15.

10.3 Data Memory

The PCF7961X Data Memory address space is split into a Register File (R0 to R7), reserved space, Special Function Registers (SFR) and 192 byte User RAM, see Figure 16.

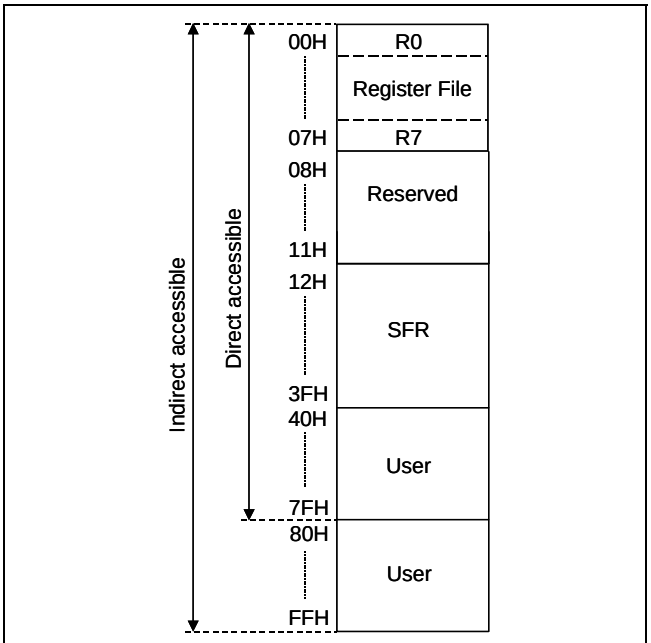


Figure 16. Data Memory, RAM

The application program may not address the reserved address space from 08H to 11H in order to prevent unintended results.

The SFR space enables I/O from/to the peripherals, the transponder interface and EEPROM as well as control of the interrupt system. The User segment provides RAM for volatile application data and Stack storage. RAM space up to address $7F_H$ supports direct and indirect addressing, while RAM space beyond $7F_H$ supports indirect addressing only. For details, refer to the specification MRK II Family, Architecture and Instruction Set, see section 23.

11 PERIPHERIAL DESCRIPTION

In order to enable access to the peripherals like the Contactless Interface, the EEPROM as well as to control operation of the Interrupt System Power Management and UHF Transmitter, a set of Special Function Register, SFR, is provided. Table 5 provides a comprehensive overview of the SFR organization and their corresponding values after a device reset.

Table 5 Special Function Register Summary

NAME	DESCRIPTION	ADDR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	RESET VALUE
PSW	Program Status Word	12_H	C	H	OV	X	C‘	H‘	OV‘	X’	
SP	Stack Pointer	13_H	SP7	SP6	SP5	SP4	SP3	SP2	SP1		$0000000X_B$
SBIT	Indirect Bit Address	14_H	MAP					SBIT2	SBIT1	SBIT0	
SPTR	Indirect Byte Address	15_H	SPTR7	SPTR6	SPTR5	SPTR4	SPTR3	SPTR2	SPTR1	SPTR0	
IE	Interrupt Enable	16_H	EA		EE	ET1A	ET1O	ET0	EP		$0X00000X_B$
IFF	Interrupt Flag	17_H			FE	FT1A	FT1O	FT0	FP		$XX00000X_B$
T0	Timer/Counter 0	18_H									
TR0	Timer/Counter 0 Reload	19_H									
TCON	Timer/Counter 0 Control	$1A_H$		TPS2	TPS1	TPS0	TCS1	TCS0		TRS0	$X00000X0_B$
WTCON	Watchdog Timer Control	$1B_H$		WPS2	WPS1	WPS0				WCLR	$X000XXXX_B$
DEMCON	Demodulator Control	$1C_H$	LFD							LFEN	$XXXXXXX0_B$
MODCON	Modulator Control	$1D_H$	MDB	EFM	EAM	TSEL	SCEN	EP17	EP20	ETP	$X00X0000_B$
CRYP1	Calculation Unit I/O	$1E_H$	CRIO								
CRYP2	Calculation Unit Control	$1F_H$						CRM2	CRM1	CRM0	
P1OUT	Port 1 Output	20_H	P17	P16	P15	P14	P13	P12	P11	P10	
P1INS	Port 1 Input sense	21_H	P17S	P16S	P15S	P14S	P13S	P12S	P11S	P10S	
P1DIR	Port 1 Direction	22_H	IO17	IO16	IO15	IO14	IO13	IO12	IO11	IO10	00000000_B
P2OUT	Port 2 Output	23_H		P26		P24	P23	P22	P21	P20	$X0X00000_B$
P2INS	Port 2 Input sense	24_H		P26S		P24S	P23S	P22S	P21S	P20S	
P2DIR	Port 2 Direction / Control	25_H	P21WD	P2CIS		IO24	IO23	IO22	IO21	IO20	$00X00000_B$
PCON	Power Control	26_H	NMI		FLD	PMODE	RST	PBAT	PLF	IDLE	$0XXX0000_B$
SCSL	System Clock Select	27_H						CSL2	CSL1	CSL0	$XXXXX000_B$
T1CON1	Timer/Counter 1 Control 1	28_H	T1RUN	T1RES	T1RC	T1OTC	T1CF	T1CR	T1CSS	T1CM	$0XXXXX00_B$
T1CON2	Timer/Counter 1 Control 2	29_H	T1PWM	T1RCAP	T1RCMP	T1S2	T1S1	T1S0	T1CLS1	T1CLS0	$00XXXX00_B$
T1CAP	Timer/Counter 1 Capture	$2A_H$									
T1CMP	Timer/Counter 1 Compare	$2B_H$									
EEDAT	EEPROM Data	$2C_H$	EEIO								
EECON	EEPROM Control	$2D_H$	BUSY	PERR	WR	POEE	PG6	PG5	PG4	PG3	$0000XXXX_B$
EEADR	EEPROM Address	$2E_H$	PG2	PG1	PG0	BYTE1	BYTE0	BIT2	BIT1	BIT0	
VCON	Voltage Comp. Control	$2F_H$	VCMP	VSEN	ISEL		VST3	VST2	VST1	VST0	$X0XXXXXX_B$
XFCON	XTAL Frequency Control	30_H			XFC5	XFC4	XFC3	XFC2	XFC1	XFC0	$XX000000_B$
PACON	Power Amplifier Control	31_H	AMH3	AMH2	AMH1	AMH0	AML3	AML2	AML1	AML0	$XXXX0000_B$
TXCON1	Transmitter Control 1	32_H			XCD	XFCS	TM	OG1	OG0	XEN	$XX001000_B$
TXCON2	Transmitter Control 2	33_H			FBSL		VOSL	PAM1	PAM0	TXON	00000000_B

Note

1. Address locations not specified are reserved for future use and shall not be accessed.

11.1 EEPROM

The PCF7961X incorporates 512 byte of non-volatile memory (EEPROM). Reading and writing of EEPROM data is supported in sequential order, bit wise addressing with auto increment is implemented for the read operation, while an ERASE/WRITE operation does always affect a complete byte. Up to four bytes may be subject to a ERASE/WRITE operation at the same time.

11.1.1 Organisation

The 512 byte of non-volatile memory (EEPROM) are organized as 128 pages, each page assembled by four byte with a total of 32 bit per page, see Figure 17.

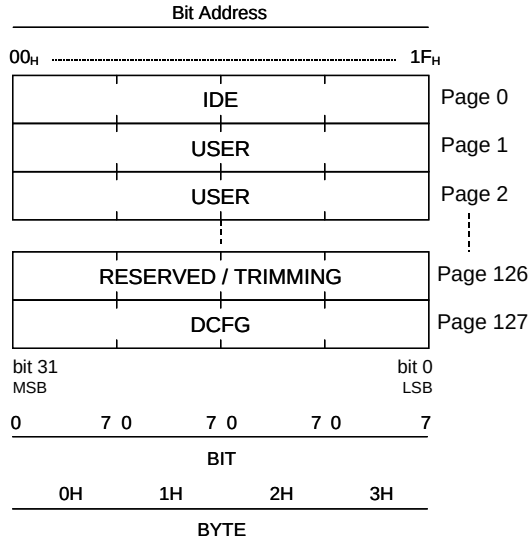


Figure 17. EEPROM Memory Organization

Page 0 holds the device Identifier, IDE, page 126 is reserved in the EROM version (PCF7961) for storage of trimming information in a ROM version (not planned) and page 127 holds device configuration data (DCFG). All are programmed during device manufacturing and locked against overwriting, according to section 16. Pages 1 to 125 are available for user data storage.

The Bit Address referred to is assembled by the BYTE and related BIT address, as specified by the corresponding control register, see below. The logical bit designators (e.g. bit31, MSB and bit0, LSB) are provided in addition.

11.1.1.1 Identifier, IDE

The Identifier, IDE, is a factory programmed quasi unique 32 bit pattern that serves the function of a device serial number (SN) and product type identification (PI) and cannot be altered. The Identifier is located page 0 and only supports reading, see Figure 18.

The product type identification is located in the bits 4 to 7 and factory programmed for all PCF7961X devices to 4_H.

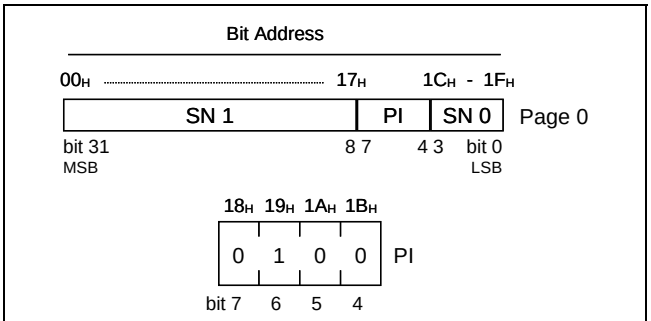


Figure 18. Identifier Organization, IDE

The Identifier is typically employed in the process of device authentication in Transponder mode as well as during rolling code or challenge response generation for keyless entry applications.

11.1.1.2 Device Configuration Page, DCFG

Figure 19 shows the DCFG page, which is located in physical page 127 of the EEPROM. Bit addresses 00h to 0Fh contain device configuration information, which are locked against overwriting.

Bit addresses 10h to 1Fh contain the transponder mode configuration (TMODE). These bits are evaluated at each device reset, after the boot program has detected that an LF field is present (see section 14). TMODE can be initialized via the Monitor and Download Interface only.

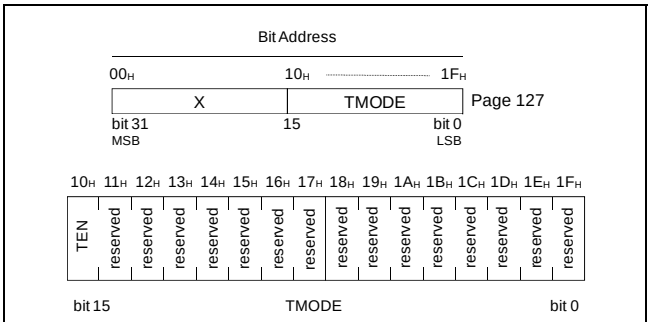


Figure 19. Device Configuration Page, DCFG

Note

1. Bits marked ‘X’ or reserved are for device internal use. They are initialized and locked against overwriting during device manufacturing and are not available for data storage. Any read operation yields an undefined bit value. The reserved bits of TMODE should be set to “0” in order to keep compatibility in case of future extensions.

TEN, Transponder Emulation Enable

TEN enables emulation of the HT3 transponder. If set, the monolithic emulation of the HT3 transponder is started after each device reset and after an LF Field has been detected. If cleared, the Boot Sequence does not invoke the Transponder Emulation at all. Instead control is passed to the application program, starting at the TRANSPONDER WARM BOOT vector (location 0010h).

11.1.2 High-Level EEPROM Access

A set of firmware functions for EEPROM ERASE/WRITE access are readily available, in order to ease development of the application software. For details refer to the specification HT3 Family ROM library (MRKII), Implementation and Description, see section 23.

In case the EEPROM is accessed through one of the ROM Library functions, memory access restrictions are implemented according to Table 6.

Table 6 EEPROM Access Rights via ROM Library

Page	Bit	ROM Library	Note
0	All	Read Only	
1 to 125	All	Read/Write	
126 to 127	All	Read Only	

The application program may restrict the EEPROM access further as required and desired, in order to virtually protect more memory locations against alteration or access.

In addition, the EEPROM can be accessed via the Monitor and Download Interface, in order to customize the EEPROM content during device personalization. In case the EEPROM is accessed through the Monitor and Download Interface, memory access restrictions depend on the Device Mode (INIT respectively PROTECTED, see also section 12) and are implemented according to Table 7.

Table 7 EEPROM Access Rights via Monitor Interface

Page	Bit	INIT	PROTECTED	Note
0	All	Read Only	No Access	
1 to 125	All	Read/Write	No Access	
126	All	Read Only	No Access	
127	00_H to $0F_H$	Read Only	No Access	
127	10_H to $1F_H$	Read/Write	No Access	

11.1.3 Low-Level EEPROM Access

Although the application program will typically utilize the high-level EEPORM access only, the low-level access scheme is described below for the sake of completeness. Because of the access restriction desired by the application, the low-level EEPROM access is restricted according to Table 8.

Table 8 Low-Level EEPROM Access Rights

Page	System Code	Application Code	Note
0	Read/Write	Read Only	
1 to 125	Read/Write	Read/Write	
126 to 127	Read/Write	Read Only	

Any application code can access the EEPROM in accordance with the access restriction only, whereas the system code (e.g. Boot routine, ROM Library, Monitor and Download Routine) supports unlimited reading and writing. However, the system code is factory programmed and cannot be altered by the user.

Read/write access to the EEPROM utilizes a set of control registers, in order to specify the designated EEPROM location, the type of operation to be performed and provides status information. The control registers are located in the Special Function Register range and comprise the Control/Status register EECON, see Table 9, the address register EEADR, see Table 10 and the data register EEDAT, see Table 11.

Table 9 EEPROM control register, EECON

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
BUSY	PERR	WR	POEE	PG6	PG5	PG4	PG3
R	R/W1	R/W	R/W	R/W	R/W	R/W	R/W

Address = 2DH

Table 10 EEPROM address register, EEADR

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
PG2	PG1	PG0	BYTE1	BYTE0	BIT2	BIT1	BIT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address = 2EH

Table 11 EEPROM data register, EEDAT

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
EEIO	X	X	X	X	X	X	X
R/W0	W0	W0	W0	W0	W0	W0	W0

Note Address = 2CH

1. Bits marked ‘X’ are not connected and reserved for future use. Any read operation yields an undefined result. For future compatibility any write operation should assign a ‘0’.

Read Operation

Reading of EEPROM data is supported in sequential order, featuring bit wise addressing with auto increment.

Due to the given EEPROM access delay ($t_{EE,DLY}$), repeated reading from the EEPROM requires to introduce a corresponding delay in between to consecutive read operations, in accordance with the CPU clock rate selected, see Table 12.

Table 12 EEPROM Read Delay

CPU clock	Number of instructions between two consecutive EEPROM read operations
125 kHz	0
250 kHz	1
500 kHz	1
1 MHz	3
2 MHz	6

It is recommended to use the according NXP-ROM-library functions for Read- and Write-Operations.

Write Operation

Writing of EEPROM data is supported page wise in sequential order, featuring bit wise addressing with auto increment. The device supports ERASE/WRITE of a single byte within a page, without stressing the unaffected bytes of that page. Anyhow, four byte (one page) may be altered at one time, thus during the same EARSE/WRITE cycle.

Before actually altering the EEPROM array, write operations target the 32 bit (4 byte) EEPROM write buffer that is required to be initialized prior to each EEPROM write operation. Once the buffer content is set as desired, an EEPROM ERASE/WRITE operation has to be requested, in order to change the EEPROM array according to the buffer content finally. Latter one, when requested from the application code, has to be interrogated by a system call (EE_BURN), in order to verify the write request against the access restriction eventually in place and return an error in such a case. Please refer to the ROM Library description for details regarding EE_BURN, see section 23.

However, the EEPROM ERASE/WRITE sequencer will only alter bytes of the selected EEPROM page that have been previously accessed in the buffer, either a single bit of it or the complete byte. In case that a byte has been accessed only partly, all remaining bits of that byte are set to “1” by default. Hence, writing a single bit to the buffer will cause the corresponding byte of the EEPROM page being altered, erasing seven bits (“1”) and setting the designated bit as intended. The remaining bytes of the page will not be affected nor subject to an ERASE/WRITE operation.

Once the EEPROM write buffer is initialized, either partly or all 32 bit of it, only the page address is of significance during the final ERASE/WRITE operation and the bit and byte address are not regarded.

The EEPROM ERASE/WRITE operation takes a certain time (t_{ERWR}), independent of the number of bytes (one to four) that are being altered within the designated page. Some readily available EEPROM functions of the ROM Library may perform multiple ERASE/WRITE operations, e.g. WRITE_SYNC command, as well as add execution time. As a result, the calling application program will recognize a different timing, see also section 23

The EEPROM cell ERASE operation corresponds to a logic one (“1”), while the WRITE operation affects cells that shall be set to logic zero. (For information only, the physical EEPROM cell always yields a state inverse to the logical one, ensuring compatibility with the existing product family and the corresponding LOCK bit features).

It is recommended to use the according NXP-ROM-library functions for Read- and Write-Operations.

POEE, Power On EEPROM

The EEPROM circuitry is enabled for reading or writing by setting the control bit POEE. As a result the sense amplifier and other EEPROM circuitry will be biased and need to settle (t_{EEPU}) before any read or write access is feasible. In addition, the write buffer needs to be initialized before a write operation shall be performed, for details refer to the control PERR.

For power consumption reasons, POEE shall be cleared, whenever EEPROM access is not required.

PG[6…0], Page Address

The seven bit control word PG[6…0] provides means to specify the EEPROM page designated for access. When changing the page address, the EEPROM access delay ($t_{EE,DLY}$) must timeout, prior to any EEPROM read/write access via the control bit EEIO, see below.

The control bits are partly located in the control register EECON (PG6 to PG3) and partly in EEADR (PG2 to PG0).

BYTE[1…0], Byte Address

The two bit control word BYTE[1…0] provides means to specify the byte within a EEPROM page designated for access. When changing the byte address, the EEPROM access delay ($t_{EE,DLY}$) must timeout, prior to any EEPROM read/write access via the control bit EEIO, see below

BIT[2…0], Bit Address

The three bit control word BIT[2…0] provides means to specify the bit location within a EEPROM byte designated for access. When changing the bit address, the EEPROM access delay ($t_{EE,DLY}$) must timeout prior to any EEPROM read/write access via the control bit EEIO, see below

WR, Select Write/Read

The control bit WR specifies the access direction. If cleared, the EEPROM is accessed for read. If set, it is accessed for write.

Please note that any write attempt, when requested from the application code, needs to be interrogated by a system call (EE_BURN, please refer to the ROM Library description for details, see section 23), in order to verify the write request against the access restriction eventually in place.

The control bit WR must not be cleared, while an EEPROM ERASE/WRITE operation is in progress, hence while the status bit BUSY is set.

EEIO, EEPROM Data I/O

The control bit EEIO provides means to read a single data bit from the EEPROM array or to write to the EEPROM write buffer, in accordance with the access direction as specified by the control bit WR.

In case EEPROM read operation is selected (WR = 0), repeated reading from EEIO will automatically and modulo increment the address pointer, comprising of the bit (BIT[2…0]), byte (BYTE[1…0]) and page (PG[6…0]) address, after any EEIO read operation (post-increment). Consequently, the address pointer sequentially steps through the entire EEPROM space, bit by bit. Thus requires to set the start address only. Writing to EEIO is not allowed in this mode, in order to avoid that the EEPROM address is unintentionally incremented.

Due to the given EEPROM access delay (t_{EEDLY}), repeated reading from the EEPROM by EEIO requires to introduce a corresponding delay in between two consecutive read operations, see Table 12.

In case EEPROM write operation is selected (WR = 1), repeated writing to EEIO will automatically and modulo increment part of the address pointer, affecting the bit (BIT[2…0]) and byte (BYTE[1…0]) only. The address pointer increments after any EEIO write operation (post-increment). However, the page address is not altered.

As writing to EEIO only targets the EEPROM write buffer, an EEPROM ERASE/WRITE operation has to be requested finally, in order to change the EEPROM array according to the buffer content. Latter one, when requested from the application code, has to be interrogated by a system call (EE_BURN), in order to verify the write request against the access restriction eventually in place and return an error in such a case. Please refer to the ROM Library description for details regarding the function EE_BURN, see section 23.

Since the EEPROM write buffer is set to all “1” by default, EEIO supports clearing of the corresponding bit only. Once cleared, the corresponding bit cannot be set to one again, except the write buffer is initialized again, using the control bit PERR. However, the application program needs to write a “1” and “0” to the buffer as desired, in order to signal to the ERASE/WRITE sequencer, which of the EEPROM bytes shall be subject to an ERASE/WRITE operation.

BUSY, Busy

The status bit BUSY provides means to detect completion of the EEPROM erase/write operation. When set the EEPROM erase/write operation is in progress. Otherwise, when cleared, has completed.

The high-low transition of BUSY triggers an interrupt flip-flop signaling that the EEPROM ERASE/WRITE operation finished and provides means to release the device from IDLE mode. A dedicated interrupt is not provided, see also section 11.2. In addition, the high-low transition initializes the ERASE/WRITE sequencer and sets the write buffer to its default value, all “1”.

While BUSY is set, any write operation to the control registers EECON, EEADR and EDAT does have no effect and reading the control register EEDAT yields an undefined result.

PERR, Programming Error

The status bit PERR provides means to verify, if the EEPROM on-chip charge-pump is within specification in the moment the ERASE/WRITE sequence has been started.

In case the status bit PERR is found set, after the EARSE/WRITE sequence completed, the designated EEPROM location may be corrupted and its content is undefined.

If PERR is cleared, the EEPROM ERASE/WRITE sequence completed as desired. However, any supply voltage dip during the ERASE/WRITE sequence may cause a device reset and corrupt the designated EEPROM location leaving its content undefined. By circuit design, it is granted that no other EEPROM page is affected in this condition, because the page address is not reset and the on-chip charge-pump is discharged, while the supply voltage is below the power on reset threshold.

The status bit stays set until the next programming is started. PERR my be cleared by writing a one to itself, which in addition will reset the ERASE/WRITE sequencer and sets the EEPROM write buffer to its default value, hence all “1”. Latter one shall be performed, before any EEPROM write operation is intended. Clearing PERR has no effect.

11.2 Interrupt System and IDLE Control

The PCF7961X employs a single level interrupt architecture with four independently maskable interrupt sources (INT1 to INT4), see Figure 20. Interrupt masking is accomplished by the Interrupt Enable register, IE. The Interrupt Flag register, IFF, signals interrupt requests pending that were generated by the corresponding peripheral.

The lowest interrupt (INT0) cannot be disabled ("non-maskable" interrupt, NMI). It is always serviced immediately after occurrence, disregarding whether another interrupt is already being serviced at that time. However, during execution of system code the interrupt system is disabled, including the NMI.

The interrupt sources operate at a common priority level, meaning that any interrupt service cannot be interrupted by subsequent interrupt requests until it is terminated by a RETI instruction. However, a multi-level interrupt structure can be constructed in software by setting the EA flag during interrupt service.

In the case of simultaneous interrupts (e.g. occurred during the execution of an interrupt service), the interrupt with the lowest vector address will be serviced next. However, at least one instruction of the main program is executed between successive interrupts.

Interrupt INT5 is not assigned to any interrupt vector, however the corresponding bits in the Interrupt Enable (IE) and Interrupt Flag (IFF) registers are used in conjunction with the IDLE mode.

Interrupt vectors INT0 to INT4 are assigned to fixed locations in the Program Memory, see section 10.1.

All interrupts are initially disabled after a device Reset.

Interrupt service, including NMI, is not supported at all while executing from the ROM Library, thus from System Code Memory.

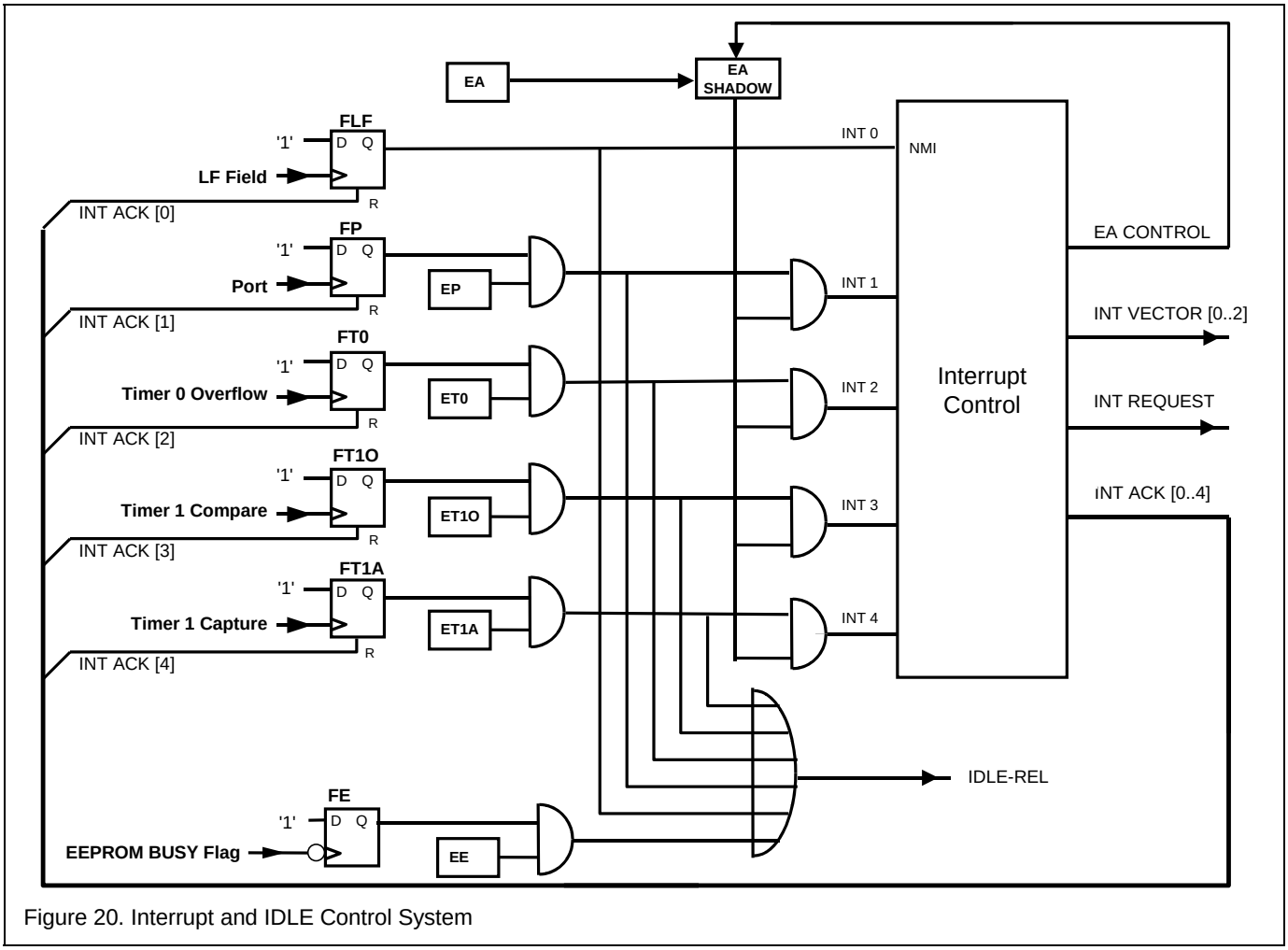


Figure 20. Interrupt and IDLE Control System

11.2.1 Interrupt Enable Register

The Interrupt Enable register, IE, is located in the SFR address space and contains several bits that control the interrupt system to feature interrupt masking, see Table 13.

The control bit EA enables or disables all interrupts. Interrupts will not be serviced while EA is cleared. If EA is set, interrupts are serviced according to the setting of the corresponding interrupt enable bit. In any case, interrupts will be latched until vectored and may alternatively serve to terminate the IDLE mode, if enabled by the corresponding bit, see also section 11.2.5.

Table 13 Interrupt Enable Register, IE

bit 7							bit 0
EA	X	EE	ET1A	ET1O	ET0	EP	X
R/W	W0	R/W	R/W	R/W	R/W	R/W	W0

Note Address = 16H

1. Bits marked ‘X’ are not connected and reserved for future use. Any read operation yields an undefined result. For future compatibility, a write operation should assign a ‘0’.
2. Interrupt service is not available for events assigned to bit EE (INT 5), since this interrupt event is not assigned a vector address.

11.2.2 Interrupt Request Flags

Interrupt requests are latched in corresponding flags of the Interrupt Flag register, IFF, see Table 14.

Table 14 Interrupt Flag Register, IFF

bit 7							bit 0
X	X	FE	FT1A	FT1O	FT0	FP	FLF
W1	W1	R/0	R/0	R/0	R/0	R/0	R/0

Note Address = 17H

1 Bits marked ‘X’ are not connected and reserved for future use. For future compatibility, a write operation should assign a ‘1’.
2. Bits marked ‘R/0’ may be cleared only by a corresponding instruction (INTA) Any set operation does not affect the bit at all.

The corresponding interrupt request flip-flop is cleared automatically when the interrupt is serviced, except for the interrupt flag FE, which serves a dedicated function in the context of IDLE mode release.

11.2.3 Interrupt Source Assignment

The interrupt vectors, located in the Program Memory, are assigned to the sources as listed in Table 15. Since each interrupt vector leaves space for not more than a single instruction, the application program should place a JMP instruction to the address of the actual interrupt service routine. A RETI instruction should be placed instead at all unused vector addresses.

Table 15 Interrupt Source Assignment

Vector	Address	Source	Note
INT 0	0002H	LF Field	1
INT 1	0004H	Port	
INT 2	0006H	Timer 0	
INT 3	0008H	Timer 1 Compare	
INT 4	000AH	Timer 1 Capture	
INT 5	000CH	Reserved	
INT 6	000EH	Reserved	

Note

1. Non Maskable Interrupt (NMI)

11.2.4 Interrupt Service

Interrupt service is executed as follows. When an interrupt request is detected, the Interrupt Control logic clears the EA SHADOW flag rather than the EA bit itself, to prevent subsequent interrupt requests from being serviced. However, the subsequent interrupt is latched.

The interrupt in service is acknowledged automatically by the Interrupt Control logic, by clearing the corresponding bit in the IFF register. Subsequently, the RISC is forced to perform a CALL instruction to the corresponding vector address. The CALL instruction saves the processor status (Program Counter, PC and Program Status Word, PSW) on the Call Stack.

The Interrupt Service Routine has to terminate, after the request has been processed, by executing a RETI instruction. The RETI instruction restores the program status (PC and PSW), in order to resume program execution at the corresponding location. Subsequently, the Interrupt Logic sets the EA SHADOW flag to enable pending or new interrupts to be serviced.

To enable interrupt nesting, the application program may set the EA flag, during an interrupt service, causing the EA SHADOW flag to be set again, enabling interrupt nesting and service for pending or future interrupts.

11.2.5 IDLE mode

Via the IDLE mode, the device provides additional means for the application program to synchronize with internal or external events. The IDLE mode is entered upon instruction, by setting the control bit IDLE, located in Power Control Register, PCON, see also section 8.4.

Any interrupts that are enabled by setting their corresponding bit in the IE register will terminate IDLE

mode and force the device to resume program execution, see Figure 20.

The IDLE mode is typically used alternatively and mutually exclusive to interrupt services. Thus the Global Interrupt Enable bit EA is cleared in this case and no interrupts are invoked. However, if the control bit EA is set, thus general interrupt service is enabled, the corresponding interrupt will be serviced after termination of the IDLE mode.

However, in any case the device executes the instruction following the one that forced the device into IDLE mode first, before the corresponding interrupt is serviced.

The IDLE mode will not be entered, if the corresponding interrupt flag (IFF) is already set for an interrupt that is enabled, while EA is cleared. Thus the corresponding bits in the IFF register should be acknowledged prior to IDLE mode invocation. The Interrupt Control logic does not perform this step, because interrupts are not serviced while EA is cleared.

IDLE invocation

The involved steps before and after using the IDLE mode are as follows:

1. The application programs the IE register by clearing the EA bit and setting the corresponding bits of all interrupt sources that shall be able to release the IDLE mode. The same bits in the IFF register should be cleared, in case they are set by unintended interrupt requests that occurred in the past.
2. The application program sets the IDLE bit and enters the IDLE mode.
3. The IDLE control logic detects an enabled interrupt request and clears the IDLE bit, terminating the IDLE mode (wakeup).
4. The application program continues with the instruction that follows the one, which had set the IDLE bit before. If more than one interrupt source was enabled in step 1, the IFF register should be read to determine the source which has caused the wakeup. In any case, the application program is obliged to clear the corresponding bit in the IFF register to acknowledge the interrupt request. Note that the Interrupt Control logic does not perform this step, because the interrupt has not been processed and vectored in this case (see section 11.2.4).

Clearing of any interrupt request bits should be accomplished by the INTA instruction, while masking all bits with “1” that shall not be affected. The interrupt request bits do not support setting by instruction. A Read-Modify-Write instruction (such as bit manipulation) should not be used, in order to avoid unintentional clearing of interrupt request bits and potential loss of an interrupt event, when latter one occurs after the Read but before the Write phase of the instruction.

11.3 System Clock Generation

The PCF7961X features a versatile system clock generation scheme, for timing purposes and to derive the RISC clock, see Figure 21.

Due to the synchronization ability of the clock generation circuitry, the application program may change the clock configuration at any time “on-the-fly”.

The System Clock Control register is located in the Special Function Register SCSL see Table 16.

Table 16 System Clock Select Register, SCSL

bit 7					bit 2		bit 0
X	X	X	X	X	CSL2	CSL1	CSL0
W0	W0	W0	W0	W0	R/W	R/W	R/W

Note Address = 27H

1. Bits marked ‘X’ are not connected and reserved for future use. Any read operation yields an undefined result. For future compatibility, any write operation should assign a ‘0’.

Initially after reset, the SCSL register is cleared and the lowest RC Oscillator clock is selected.

CSL[2...0], Clock Select

Typically the RISC clock is derived from an on-chip RC Oscillator (T_{OSC}), which operates at a nominal frequency of 4 MHz and is divided by two, prior to usage for duty cycle reasons. The resulting clock ($T_{OSC,D}$) is fed to a programmable divider, in order to enable clock rate selection for the RISC (T_{CPU}) and its peripherals (T_{SYS}) according to the speed and power consumption requirements of the application program.

The Clock Select control bits, CSL, determine the final system clock, TSYS, according to Table 17.

Table 17 Clock Select, CSL

CSL2	CSL1	CSL0	T_{SYS}	T_{SYS} (typ)	Note
0	0	X	T_{OSC} * 32	8 µs	1
0	1	0	T_{OSC} * 16	4 µs	
0	1	1	T_{OSC} * 8	2 µs	
1	0	0	T_{OSC} * 4	1 µs	
1	0	1	T_{OSC} * 2	0.5 µs	
1	1	0	Reserved	Reserved	2
1	1	1	Reserved	Reserved	2

Note

1. If the device executes from the System Code Memory, CSL0 determines the system clock source. CSL0=0 yields LF Field clock, while CSL0=1 yields RC Oscillator clock. A customer application code cannot utilize this option.
2. Reserved for device test purposes.

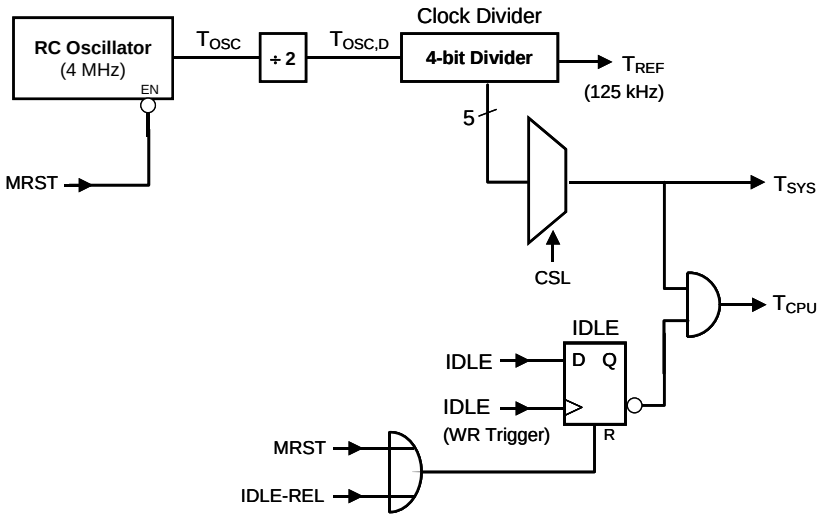


Figure 21. System Clock Generation

IDLE Mode

In IDLE mode the RISC clock (T_{CPU}) is inhibited as long as the control signal IDLE is high, while the clock for peripherals (T_{SYS}) is not affected.

T_{REF}, Reference Clock

For system timing purposes, especially for use with the EEPROM, in order to generate appropriate programming timings, a 125 kHz (TYP) clock reference is derived from the clock source. Anyhow, the reference clock is also available for other peripherals.

11.4 Timer/Counter 0

Timer/Counter 0 features an asynchronous 8-bit architecture with auto reload and a 6-bit prescaler, Figure 22.

The Timer/Counter 0 control bits are located in the Special Function Register TCON, Table 18.

Table 18 Timer/counter 0 Control Register, TCON

bit 7	bit 6	bit 5	Bit 4	bit 3	bit 2	bit 1	bit 0
X	TPS2	TPS1	TPS0	TCS1	TCS0	X	TRS0
W0	R/W	R/W	R/W	R/W	R/W	W0	R/W

Note Address = 1AH

1. Bits marked ‘X’ are not connected and reserved for future use. Any read operation yields an undefined result. For future compatibility, a write operation should assign a ‘0’.

The timer/counter 0 control register is initially cleared after reset and the timer is stopped.

TCS[1…0], Timer/Counter 0 Clock Source

Timer/Counter 0 can operate as timer or as event counter, depending on the clock source selected by the corresponding control bits TCS, Table 19.

TPS[2…0], Timer/Counter 0 Prescaler

Timer/Counter 0 features a programmable 6-bit prescaler that provides prescaler values of 2^N for N = 0 to 6, selected by TPS, see Table 20. Writing to and reading from the prescaler is not supported at all.

Table 19 Timer/Counter 0 Clock Source Select, TCS

TCS1	TCS0	Clock Source	Note
0	0	Reference clock, T_{REF}	1
0	1	System clock, T_{SYS}	1
1	0	LF Field carrier clock, T_C	2
1	1	External clock source XEN = 0: External clock/event at Port P15, $P15_{CLK}$ XEN = 1: XTAL Oscillator divided clock, T_{XDCLK}	3

Note

1. The clock is derived from the on-chip RC Oscillator (Battery Mode) or the Contactless Interface clock recovery circuitry (Transponder Mode), see also section 9.
2. The clock is derived from the Contactless Interface clock recovery circuitry, see also section 9.
3. The clock source has to fit the requirements as specified by T_{SYS} respectively $P15_{CLK}$.

Table 20 Timer/counter 0 Prescaler Select, TPS

TPS2	TPS1	TPS0	Prescaler Value	Note
0	0	0	1	
0	0	1	2	
0	1	0	4	
0	1	1	8	
1	0	0	16	
1	0	1	32	
1	1	0	64	
1	1	1	reserved	

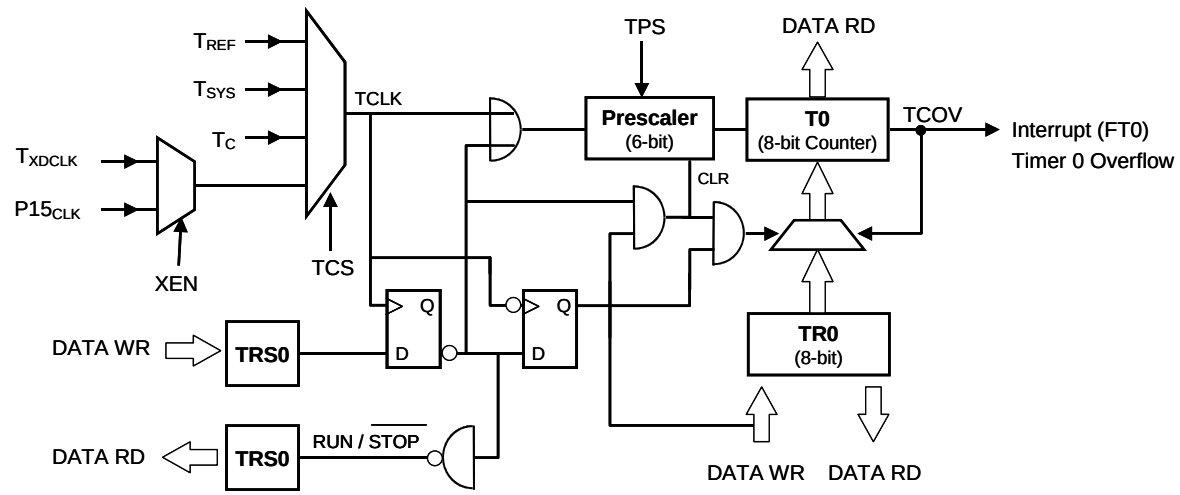


Figure 22. Timer/Counter 0 Block Diagram

TRS0, Timer/Counter 0 Run/Stop

The Run/Stop control bit TRS0 controls the operation of timer/counter 0. A Run/Stop request is synchronized with the clock source (TCLK) and the timer/counter is incremented in response to a rising edge of the clock (TCLK), according to Figure 23.

To force timer/counter 0 into Run mode, a '1' has to be written to the TRS0 flip-flop. To force the Stop mode, a '0' has to be written. The corresponding request is latched upon the next rising edge of the clock signal TCLK and signaled by the Run/Stop mode flip-flop. Subsequent clocks will be recognized respectively ignored by the timer/counter. Please note that the prescaler does not recognize the clock, which acknowledges the RUN mode, while it does recognize the clock, which acknowledges the STOP mode, Figure 23.

Anyhow, the counter and prescaler states are not changed in Stop mode. Reading the control bit TRS0 signals, if timer/counter 0 is running or stopped.

Upon overflow of the Timer/Counter register T0, the Timer/Counter 0 interrupt request flag FT0 is set. At the same time, the timer/counter register is overwritten with the value stored in the timer/counter reload register TR0.

TR0, Timer/Counter 0 Reload

The Timer/Counter reload register, TR0, is located in the SFR address range and available for reading and writing.

In case Timer/Counter 0 is stopped (TRS0 = 0), writing to TR0 will clear the prescaler and affect register T0, since T0 does receive a copy of the value loaded into TR0.

If the Timer/Counter is running (TRS0 =1), writing to TR0 has no effect.

T0, Timer/Counter 0 Counter Register

The timer/counter register, T0, is located in the SFR address range and available for reading only. A write operation has no effect. The timer/counter register, T0, may be initialized via the reload register TR0 only.

It is important to notice that the system clock (instruction clock) and timer/counter 0 clock may be asynchronous to each other, depending on the selected clock sources. Thus reading from T0 by software may happen at the exact moment in which the timer/counter is incremented. In such a case, the read value may be undefined. Thus the timer/counter should be stopped before reading T0. Alternatively, successive readings of T0 should be performed in order to verify the read results against each other.

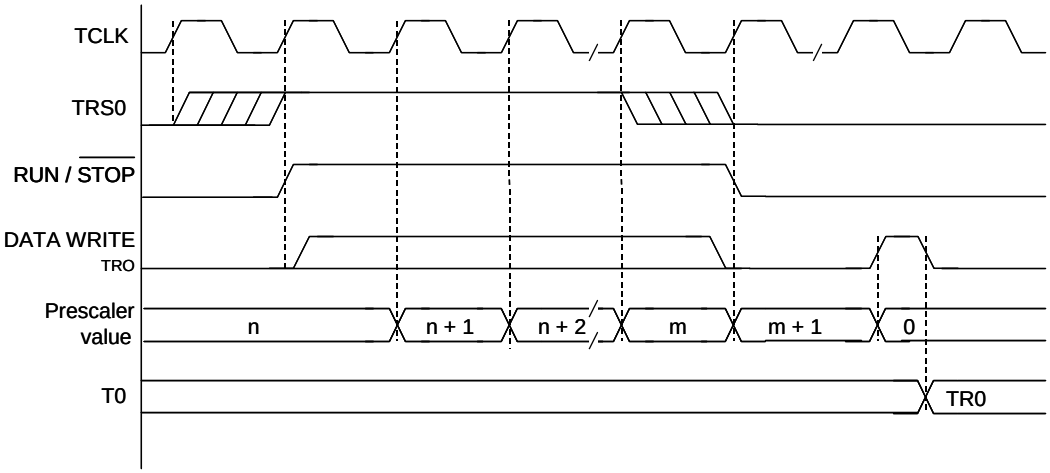


Figure 23. Timer/Counter 0 Timing

11.5 Timer/Counter 1

Timer/Counter 1 features an 8-bit architecture with 7-bit prescaler, Capture/Compare, Auto-Reset and Pulse Width Modulation circuitry, Figure 24 and Figure 28.

The timer/counter 1 control bits are located in the Special Function Register T1CON1 and T1CON2, Table 21 and Table 22.

Table 21 Timer/counter 1 Control Register, T1CON1

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
T1RUN	T1RES	T1RC	T1OTC	T1CF	T1CR	T1CSS	T1CM
R/W	R0/W1	R0/W1	R/W	R/W	R/W	R/W	R/W

Address = 28H

Table 22 Timer/counter 1 Control Register, T1CON2

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
T1PWM	T1RCAP	T1RCMP	T1S2	T1S1	T1S0	T1CLS1	T1CLS0
R/W	R0/W	R/W	R/W	R/W	R/W	R/W	R/W

Address = 29_H

Notice that the prescaler and Timer 1 register cannot be accessed directly, instead, may be cleared upon instruction only. However, the Timer 1 register value may be captured upon instruction, any time desired.

T1CLS[1,0], Timer/Counter 1 Clock Source

Timer/counter 1 can operate as timer or as event counter, depending on the clock source selected by the corresponding control bits T1CLS, see Table 23.

T1S[2…0], Timer/Counter 1 Prescaler Select

Timer/counter 1 features a programmable 7-bit prescaler that provides prescaler values of 2^N for N = 0 to 7, selected by T1S, see Table 24. Writing to and reading from the prescaler counter is not supported at all.

Table 23 Timer/Counter 1 Clock Source Select, T1CLS

T1CLS1	T1CLS0	Clock Source	Note
0	0	Reference clock, T_{REF}	
0	1	4MHz RC Oscillator clock, T_{OSC}	
1	0	LF Field carrier clock, T_C	1
1	1	External clock source XEN = 0: External clock/event at Port P15, $P15_{CLK}$ XEN = 1: XTAL Oscillator divided clock, T_{XDCLK}	2

Note

1. The clock is derived from the Contactless Interface clock recovery circuitry, see also section 9.
2. The clock source has to fit the requirements as specified by T_{SYS} respectively $P15_{CLK}$.

Table 24 Timer/counter 1 Prescaler Select, T1S

T1S2	T1S1	T1S0	Prescaler Value	Note
0	0	0	1	
0	0	1	2	
0	1	0	4	
0	1	1	8	
1	0	0	16	
1	0	1	32	
1	1	0	64	
1	1	1	128	

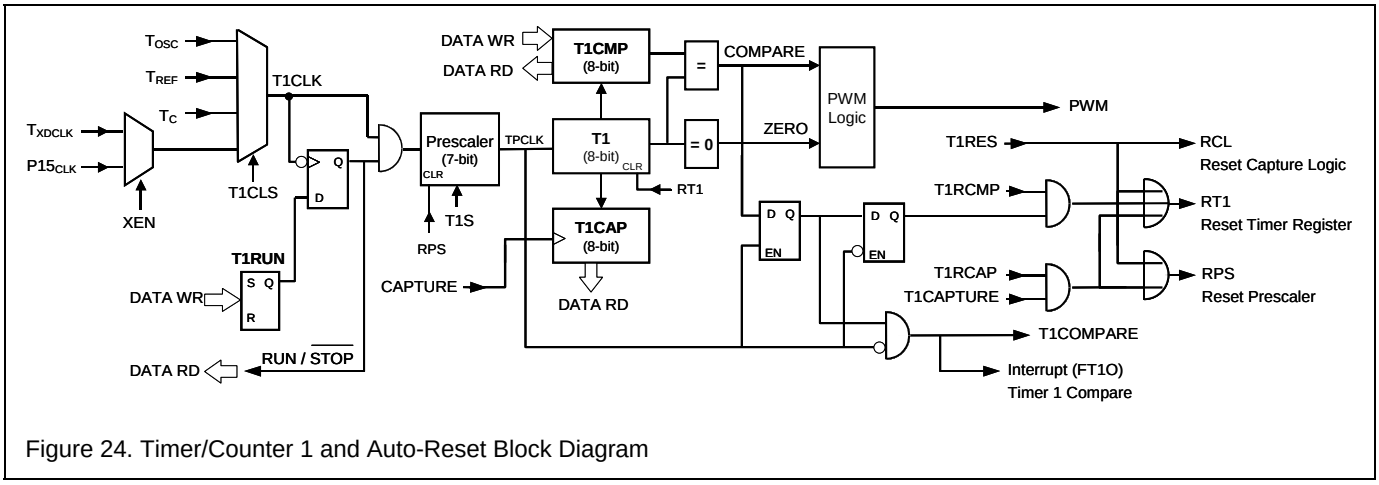


Figure 24. Timer/Counter 1 and Auto-Reset Block Diagram

T1RUN, Timer/Counter 1 Run/Stop

The Run/Stop control bit T1RUN controls the operation of timer/counter 1. A Run/Stop request is synchronized with the clock source (T1CLK) and the timer/counter is incremented in response to a rising edge of the clock (T1CLK), according to Figure 25.

To force timer/counter 1 into Run mode, a '1' has to be written to the T1RUN flip-flop. To force the Stop mode, a '0' has to be written. With the next falling edge of the clock signal T1CLK, the timer/counter will enter the requested mode, which is signaled by the Run/Stop mode flip-flop. Subsequent clocks will be recognized respectively ignored by the timer/counter. Anyhow, the counter and prescaler state are not changed in Stop mode. Reading the control bit T1RUN signals, if timer/counter 1 is running or stopped.

T1CMP, Timer/Counter 1 Compare Register

The value stored in the Timer/counter 1 Compare register, T1CMP, is continuously compared against the Timer/Counter 1 value, T1. If equal a "COMPARE" signal is generated to trigger the interrupt request Timer 1 Compare (FT1O), as well as to serve as input for the Pulse Width Modulation, PWM, and Auto-Reset Logic. According to Figure 26, the interrupt is triggered upon the falling edge of the Timer/Counter clock (T1CLK).

Similarly the Timer/Counter 1 value is continuously compared against "ZERO" and a corresponding signal generated for use with the Pulse Width Modulation, PWM, Logic.

The Timer/counter 1 Compare register, T1CMP, is located in the SFR address range and available for reading and writing.

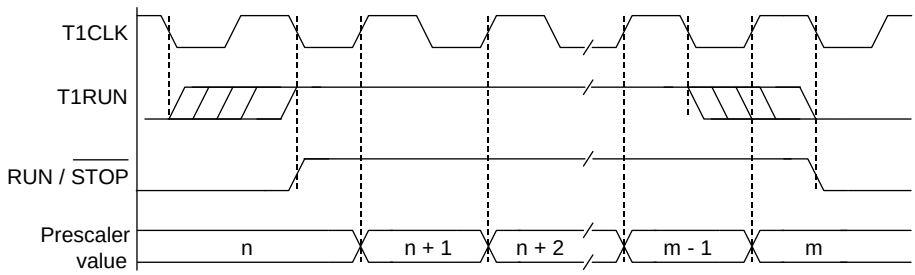


Figure 25. Timer/Counter 1 Timing

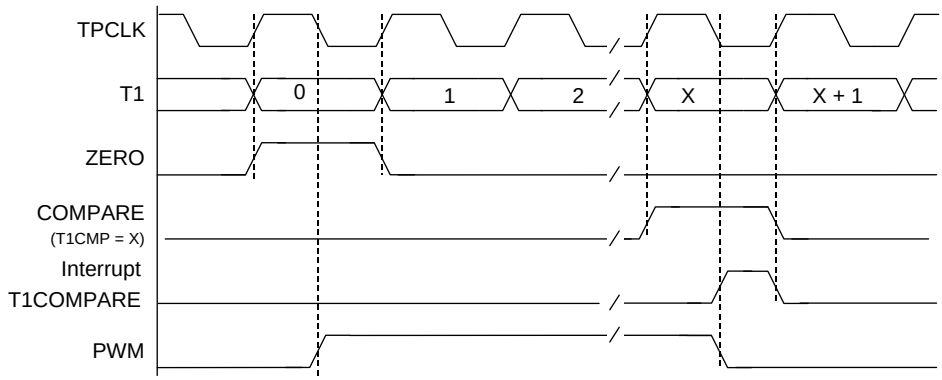


Figure 26. Timer/Counter 1 Compare and PWM timing

T1PWM, Timer/Counter 1 Pulse Width Modulation Control

Setting the control bit T1PWM enables the PWM Logic and causes the direction flip-flop of port P22 to be overruled, forcing the port P22 to be configured for output mode, see Figure 27.

The state of P22 is defined by the XOR function of the output bit of P22 (P22) and the logical level of the PWM signal. The PWM signal is set upon “ZERO” and cleared upon “COMPARE”. Latter one is assigned priority; in case “ZERO” also is applicable in that moment, see Figure 26.

Hence, the pulse width is determined according to the value of T1CMP, featuring a range of 0/256 to 255/256. Consequently, when T1CMP is set to 00h, PWM yields always ‘0’.

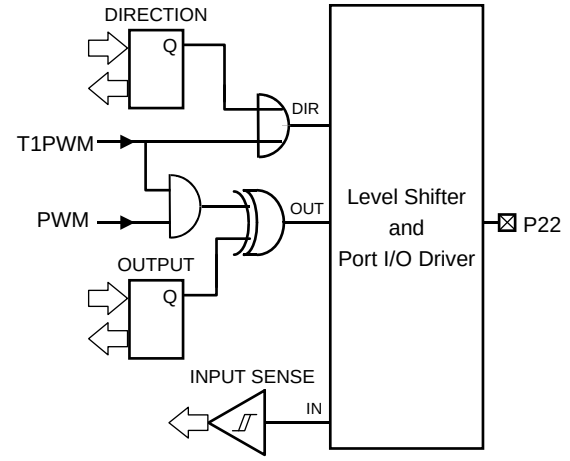


Figure 27. PWM Control

T1CAP, Timer/Counter 1 Capture Register

Timer/counter 1 features an 8-bit capture register, T1CAP, able to capture the current Timer/Counter value in response to a capture request (CAPTURE) as generated by the Timer/Counter 1 Capture Logic, see Figure 28.

The capture trigger (CAPTRG) can be derived from a number of sources and events, and in such an event, the interrupt request Timer 1 Capture (FT1A) is triggered. However, forcing a Manual Capture by instruction, will not trigger the interrupt, see Figure 29

The Timer/counter 1 capture register, T1CAP, is located in the SFR address range and available for reading only.

T1CSS, Timer/Counter 1 Capture Source Select

The capture event may be derived from the LF Demodulator output (LFD) or the port P2, as selected by the control bit T1CSS, see Table 25

Table 25 Timer/Counter 1 Capture Source Select, T1CSS

T1CSS	Capture Source	Note
0	LF Demodulator (LFD)	2
1	Port P2 (P21 respectively P26I)	3

Note

1. Writing to T1CSS, while the timer is running (T1RUN reads '1'), is not recommended, because it may generate a malicious capture event.
2. The LF Demodulator should be enabled before selecting it as capture source, in order avoid unwanted capture events.
3. As a function of the control bit P2CIS, either P21 or P26I is used as Capture Source input, see section 46. Please note that P26I is not available in TSSOP20 package.

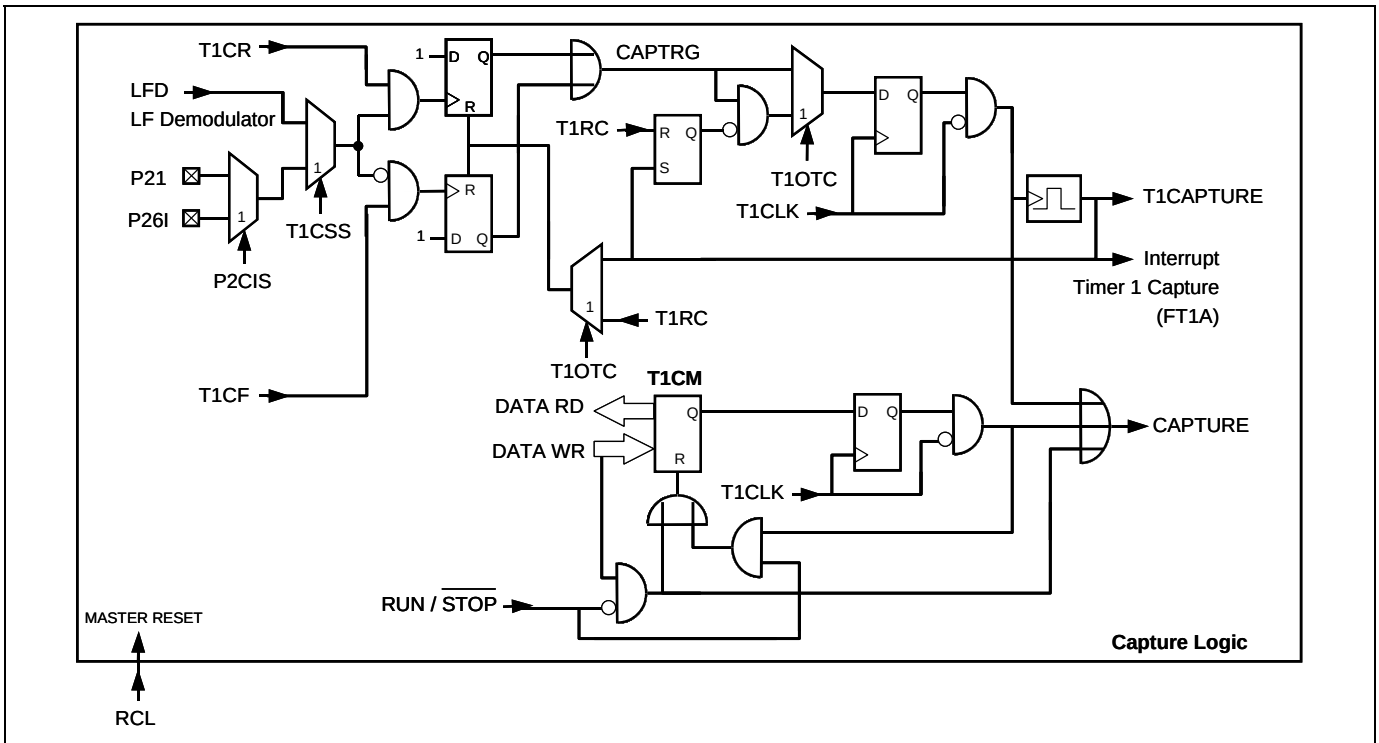


Figure 28. Timer/Counter 1 Capture Logic

T1CR and T1CF, Timer/Counter 1 Capture Configuration

The capture event may be configured to occur on the rising and/or falling edge of the capture source, as selected by the control bit T1CR and T1CF, see Table 26.

If both control bits are set, a capture trigger will be generated upon any change of the input signal.

Due to synchronization of the capture input signals with the timer clock (T1CLK), the repetition rate of the capture events is limited accordingly.

Table 26 Timer/Counter 1 Capture Enable

	Capture Event Configuration	Note
T1CR	Capture on rising edge ('0' -> '1')	1
T1CF	Capture on falling edge ('1' -> '0')	1

Note

1. Writing a ‘1’ to T1CR or T1CF while the timer is running (T1RUN reads ‘1’) is not recommended, and may generate a malicious capture event.

T1CM, Timer/Counter 1 Capture Manual

A capture operation may be requested manually at any time as desired, by writing a ‘1’ to the control bit T1CM, in order to read the current value of the Timer/Counter 1 register, T1, in RUN or STOP mode. As direct reading of the Timer/Counter 1 register is not supported, Capture Manual is the only means to read the Timer/Counter 1 register.

Once set by the application, T1CM will stay '1' until the capture request has been executed, causing the control bit to be cleared. Thus, T1CM can be polled by the application to verify, if the capture request has been carried out. However, T1CM may be cleared any time, by writing a ‘0’ to it, see Figure 29.

Note that operating the control bit T1CM does not trigger a Timer/Counter Reset Upon Capture nor the Timer 1 Capture interrupt.

T1OTC, Timer/Counter 1 One Time Capture

The Timer/counter 1 Capture feature supports 'Single-Shot’ operation, which is enabled by setting the control bit T1OTC. In this case, the capture logic can be triggered “One-Time” only and locks itself, ignoring subsequent events. The capture logic may be unlocked any time, by writing a '1' to the control bit T1RC, see Figure 29.

The 'Single-Shot’ operation is useful to ensure that a capture event is processed properly, e.g. the correct reading is taken from the capture register. In continuous capture mode, a second capture event may cause a new capture value to be stored in the T1CAP register, before the first value has been read out.

T1RC, Timer/Counter 1 Reset Capture

In case the capture logic has been trigged, when operating in Single-Shot mode (T1OTC = 1), the capture logic may be unlocked at any time, by writing a '1' to the control bit T1RC. Writing a '0' to bit T1RC has no effect. T1RC is not latched internally, thus reading from it always yields ‘0’.

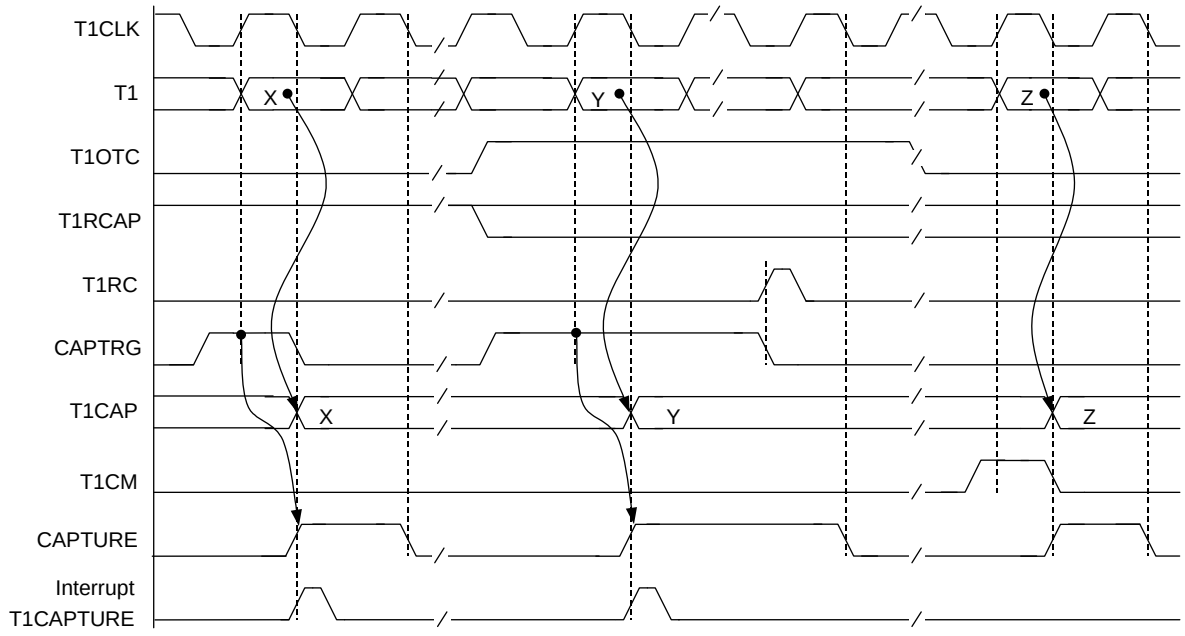


Figure 29. Timer/Counter 1 Capture Logic Timing

T1RES, Timer/Counter 1 Reset

The control bit T1RES provides means to manually reset the Timer/Counter 1 at any time as desired. As the timer/counter RUN/STOP logic is not affected, this feature must not be triggered, as long as the Timer/Counter 1 is in RUN mode. Otherwise, the Timer/Counter registers may hold an undefined value afterwards, because this feature is not synchronized with the Timer/Counter clock. Thus, the Timer/Counter 1 shall be forced into STOP mode, before triggering the control bit T1RES.

Writing a '1' to the control bit T1RES clears the register Timer/Counter 1 (T1), the prescaler and resets the Capture Logic. However, the output state of the PWM circuitry (PWM) will depend on the actual compare register value (T1CMP), see T1PWM, Timer/Counter 1 Pulse Width Modulation . Writing a '0' to bit T1RES has no effect. T1RES is not latched internally; reading from it always yields ‘0’.

T1RCMP, Timer/Counter 1 Reset Upon Compare

Setting the control bit T1RCMP to '1' enables the "Reset Upon Compare" feature. When set, the Timer/Counter register (T1) is cleared, whenever a compare match is detected. Latter one applies, when the Timer/Counter register (T1) equals the Compare Register (T1CMP).

The clear operation is synchronized with the clock that is provided by the prescaler (TPCLK), see Figure 30.

Consequently, the Timer/Counter 1 features a compare match repetition rate equal to [T1CMP + 1] clocks.

T1RCAP, Timer/Counter 1 Reset Upon Capture

Setting the control bit T1RCAP to '1' enables the "Reset Upon Capture" feature. When set, the Timer/Counter register (T1) and the prescaler are cleared, whenever a capture event is detected, see Figure 31.

However, the capture operation will not be affected and completed properly, before the Timer/Counter register (T1) is cleared. Writing a '0' to bit T1RCAP has no effect.

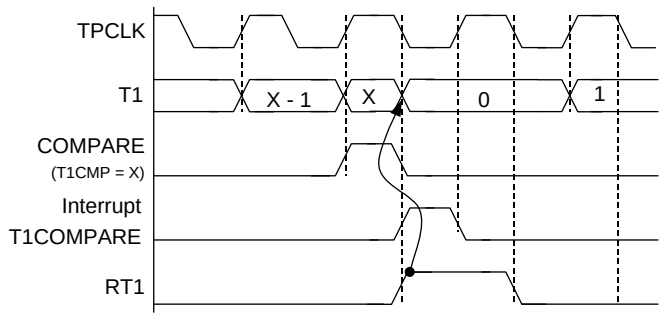


Figure 30. Timer/Counter 1 Reset Upon Compare Timing

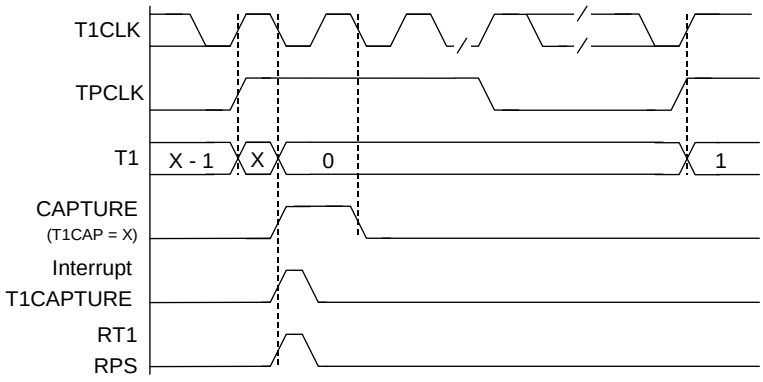


Figure 31. Timer/Counter 1 Reset Upon Capture Timing

11.6 Watchdog Timer, WT

The device incorporates a watchdog timer, WT, to recover the system from situations, in which the application program has run into a deadlock situation. This avoids that the connected battery is drained unnecessarily.

The watchdog timer consists of a programmable 8-bit prescaler and 8-bit main timer, WT, clocked from the reference clock (T_{ref}, see section 11.2), according to Figure 32.

The watchdog timer is always active when the device is supplied from the battery (PMODE = 1). On the other hand, it is always disabled, when the device is supplied from the LF Field (PMODE = 0).

When the watchdog is not continuously restarted and allowed to timeout, it will force the Supply Switch logic to set the Supply Switch to LF Field supply (PMODE = 0), see also section 8.1 (Figure 4). Consequently, the device supply is no longer derived from the battery and the further system behavior depends on the LF Field supply condition and the voltage at pin VFLD. A device reset will be generated subsequently, if the LF Field supply (hence, the voltage at pin VLFD) drops below the power-on reset threshold ($V_{POR.FLD}$). Otherwise, the device may continue program execution, as long as the LF Field supply is sufficient.

However, due to the supply switch implementation, a device reset may be generated, when changing from battery to LF Field supply, even if the LF Field supply is sufficient. Latter one is likely, when the device consumes a high operating current.

The watchdog timer control bits are located in the Special Function Register WTCON, Table 27.

Table 27 Watchdog Timer Control Register, WTCON

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
X	WPS2	WPS1	WPS0	X	X	X	WCLR
W0	R/W	R/W	R/W	W0	W0	W0	R0/W1

Note Address = 1BH

1. Bits marked ‘X’ are not connected and reserved for future use. Any read operation yields an undefined result. For future compatibility, a write operation should assign a ‘0’.
2. Reading of the bit WCLR yields a ‘0’.

Initially after reset, the WTCON register is cleared, which configures the longest possible timeout period.

WPS[2…0], Watchdog Prescaler Select

The Watchdog main counter is clocked by a tap taken from the prescaler, according to Table 28.

Table 28 Watchdog Prescaler Select, WPS

WPS2	WPS1	WPS0	Prescaler Ratio	Note
0	0	0	256	
0	0	1	128	
0	1	0	64	
0	1	1	32	
1	0	0	16	
1	0	1	8	
1	1	0	4	
1	1	1	2	

WCLR, Watchdog Clear

To prevent the Watchdog Timer from overflowing, a ‘1’ has to be written periodically to the control bit WCLR by the application program. Writing a ‘0’ to WCLR has no effect. WCLR is not latched internally and reading from it always yields ‘0’.

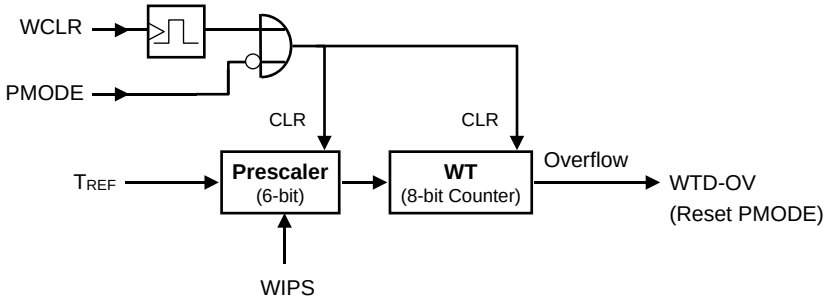


Figure 32. Watchdog Timer Block Diagram

11.7 I/O Ports

The device incorporates two quasi-identical I/O port structures, Port 1 and Port 2, with in total 15 port lines. The ports serve as button inputs (device Wake Up), control external peripherals and partly provide extended functions. In case of the package version TSSOP20 only seven of the 15 I/O ports are available externally.

Port 1 consists of eight independently configurable bi-directional ports. According to Figure 33, the port lines are configured in “push-pull” fashion, when used in output mode. Port P10, P11, P14, P15 and P16 may serve as button input (device Wake Up) and partly feature on-chip pull-up resistors, see also section 8.3.

Port 2 consists of seven I/O lines, featuring five independently configurable bi-directional port lines (P20 to P24). According to Figure 33a, the port lines are configured in “push-pull” fashion, when used in output mode. Port P21 and P22 may serve as button input (device Wake Up). Port P20, P21, P23 and P24 features on-chip switch able pull-up resistors, which are only active, if the corresponding port line operates in input mode.

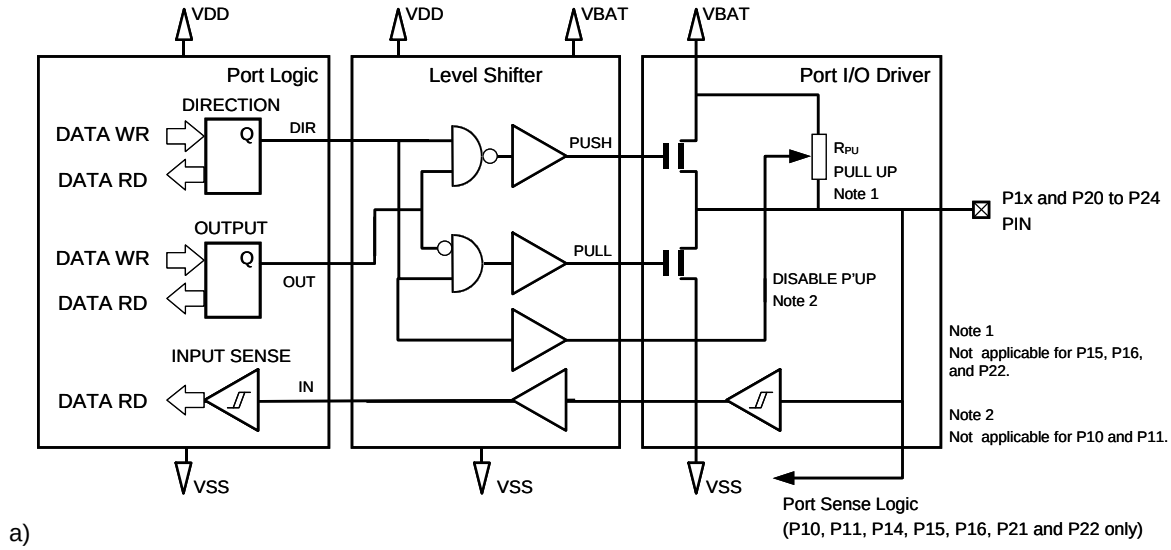


Figure 33. Port 1 and Port 2 Configurations

Configuration of and access to the I/O Ports is provided by means of a Direction, Output and Input Sense Register located in the Special Function Register range, see below.
When configured for input mode, floating port terminals must be avoided and external pull-up or pull-down means eventually need to be provided accordingly. During device Reset and POWER-OFF mode, the port direction and output flip-flops are cleared, automatically configuring all port lines for input. In this situation, ports P15, P16 and P22 must feature external pull-down or pull-up measures to VSS or VBAT. The remaining ports feature on-chip measures. However, pull-down measures for P15, P16 and P22 must be considered carefully, as an undesired device wake up may occur when the device is about to enter POWER-OFF mode, see section 22.7.
Although of generic nature and fully controlled by the application program, some I/O lines feature extended control functions according to Table 29.

P10, P11, P14 to P16, P21 and P22, Wake-Up Sense and Port Interrupt

The port lines P10, P11, P14 to P16, P21 and P22 are connected to the Port Sense Logic and may serve as button inputs for device wake-up. Thus, provide means to release the device from POWER-OFF mode, in response to a high-to-low transition, see section 8.3.

Apart from the device wake up function, these ports may also be used to trigger a port interrupt during program execution. Subsequent port polling might be required to distinguish between button activation and port interrupt.

P15, External Clock Input

Port line P15 may serve as an external clock input in combination with Timer/Counter 0 and Timer/Counter 1, see section 11.4 respectively section 11.5. If used for this purpose, P15 should be operated in input mode only, to avoid unintentional short circuit conditions. The Port Interrupt feature (Port Sense Logic) will be disabled accordingly, see section 8.3.

P16, Voltage Comparator Input

Port line P16 may serve as analog input for the on-chip voltage comparator. If used for this purpose, the port I/O driver, input sense control will be overruled and the Port Interrupt feature (Port Sense Logic) will be disabled accordingly, see section 11.9 and 8.3.

P17, P20, Digital Modulator Output

The port lines P17 and P20 may be controlled from the on-chip digital modulator circuitry that supports signal train generation, e.g. Manchester/Bi-Phase, etc.. If used for this purpose, the port direction control will be overruled accordingly, see section 11.8.

P21, Timer 1 Capture Trigger Input

Port line P21 may serve as external Capture trigger input in combination with Timer/Counter 1, or alternatively as external interrupt input utilizing the Capture Interrupt vector, see section 11.5.

In this case, Port P21 should be operated in input mode only, to avoid unintentional short circuit conditions. The Port Interrupt feature (Port Sense Logic) may be disabled by the control bit P21WD as desired, see section 11.7.1.

P22, Timer 1 PWM Output

Port line P22 may serve as Pulse Width Modulator (PWM) output in combination with Timer/Counter 1. If used for this purpose, the port direction control will be overruled and the Port Interrupt feature (Port Sense Logic) will be disabled accordingly, see section 11.5 and 8.3.

Table 29 Port configuration and function assignment

Port Feature	Port 1								Port 2							Note
	10	11	12	13	14	15	16	17	20	21	22	23	24	26I	26ON	
Internal Pull Up (Down)	•	•												**(•)**		
Internal switch able Pull Up			•	•	•			•	•	•		•	•			1
Wake Up Sense / Port Interrupt	•	•			•	•	•			•	•					
Voltage Comparator Input							•									
Digital Modulator Output								•	•							
Timer 1 Capture Trigger External Interrupt										•						
Timer 1 PWM Output											•					
External Clock Input						•										

Note

1. Active only, if the port line operates in input mode.

11.7.1 PxDIR, Port Direction Control

All port lines may be configured independently for input or output as defined by the Special Function Register Port Direction, see Table 30 and Table 31.

Table 30 P1 Direction Register, P1DIR

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
IO17	IO16	IO15	IO14	IO13	IO12	IO11	IO10
R/W	R/W	R/W	R/W	R/w	R/W	R/W	R/W

Address = 22H

Table 31 P2 Direction Register, P2DIR

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
P21WD	P2CIS	X	IO24	IO23	IO22	IO21	IO20
R/W	R/W	W0	R/W	R/W	R/W	R/W	R/W

Note Address = 25H

1 Bits marked ‘X’ are not connected and reserved for future use. Any read operation yields an undefined result. For future compatibility, a write operation should assign a ‘0’.

IO2x, Port Direction Control

If the corresponding direction bit is set, the port line is configured for output and the corresponding port I/O driver forces the port line high or low, depending on the state of the output flip-flop. If the corresponding direction bit is cleared, the I/O port driver is configured for input and the corresponding PUSH-PULL stage is forced into tri-state.

As mentioned above, the port direction control bit is overruled by other peripherals under certain condition, see section 11.7.

P21WD, Port 21 Wake Up Disable

When set to ‘1’, the control bit P21WD provides means to inhibit Port Interrupt generation for Port 21, during device operation, see also section 8.3. This feature is useful, in case Port 21 serves as trigger input for the Timer/Counter 1 Capture function, see also section 11.5.

However, P21WD is cleared, while the device resides in POWER-OFF mode. Thus, Port 21 supports device Wake Up in any case. The control bit P21WD is located in the Port 2 Direction register, P2DIR.

P2CIS, Port 2 Capture Input Source

The control bit P2SCI serves the function to select the port line that is used as Capture Source input for Timer/Counter 1, in case the Capture event shall be derived from Port 2 (T1CSS = 1, see section 11.5).

When P2CIS is set to ‘1’ Port 26I is selected, otherwise P21. Please note that P26I is not available in TSSOP20 package,

11.7.2 PxOUT, Port Output Control

The port output flip-flop controls the state of the corresponding port line, if latter one is configured for output mode. Any read operation from the port output flip-flop will be executed by sampling the state of the flip-flop rather than the state of the port line.

The port output register are located in the Special Function Register range, see Table 32and Table 33.

Table 32 P1 Output Register, P1OUT

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
P17	P16	P15	P14	P13	P12	P11	P10
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address = 20H

Table 33 P2 Output Register, P2OUT

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
X	P26	X	P24	P23	P22	P21	P20
W0	R/W	W0	R/W	R/W	R/W	R/W	R/W

Note Address = 23H

1 Bits marked ‘X’ are not connected and reserved for future use. Any read operation yields an undefined result. For future compatibility, a write operation should assign a ‘0’.

11.7.3 PxINS, Port Input Sense

Reading from the port lines is accomplished by means of the Special Function Register Port Input Sense, see Table 34 and Table 35.

Table 34 P1 Input Sense Register, P1INS

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
P17S	P16S	P15S	P14S	P13S	P12S	P11S	P10S
R	R	R	R	R	R	R	R

Address = 21H

Table 35 P2 Input Sense Register, P2INS

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
X	P26S	X	P24S	P23S	P22S	P21S	P20S
	R		R	R	R	R	R

Note Address = 24H

1. Bits marked ‘X’ are not connected and reserved for future use.

P1INS and P2INS directly sense the port pin and return the corresponding states of the I/O lines, see Figure 33.

11.8 Digital Modulator

The device features an on-chip digital modulator circuitry for use with the port lines P17 and P20 or the Contactless Interface or the UHF Transmitter in the context of FSK and ASK modulation of the UHF carrier, see Figure 34.

The digital modulator supports signal train generation, e.g. with Manchester/BiPhase or Pulse Width coding, provides a bit buffer and features a sub-carrier mode. Operation is configured by the control bits located in the Special Function Register MODCON, Table 36.

Table 36 Modulator Control Register, MODCON

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
MDB	EFM	EAM	TSEL	SCEN	EP17	EP20	ETP
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address = 1DH

Initially after reset, the Modulator Control register, MODCON, is cleared, disabling the modulator by default.

EP17, Enable P17

Setting the control bit EP17 will force the Port P17 into output mode. The port output state is determined by the XOR function of the modulator output and the port data output flip-flop, establishing the desired port state before and after modulator operation.

EP20, Enable P20

Setting the control bit EP20 will force the Port P20 into output mode. The port output state is determined by the XOR function of the modulator output and the port data output flip-flop, establishing the desired port state before and after modulator operation.

ETP, Enable Transponder

Setting the control bit ETP provide means to control the contactless interface modulator circuitry for transponder operation, see also section 9.2. A ‘one’ bit will introduce a corresponding LF Field load modulation. The LF field load modulation is under direct control of the application program in terms of data rate and data coding.

EAM, Enable Amplitude Modulation

Setting the control bit EAM provide means for ASK modulation of the UHF Transmitter, in accordance with the control signal AMOUT, see also 12.4.3.

EFM, Enable Frequency Modulation

Setting the control bit EFM provide means for FSK modulation of the UHF Transmitter, in accordance with the control signal FMOUT, see also section 12.4.2.

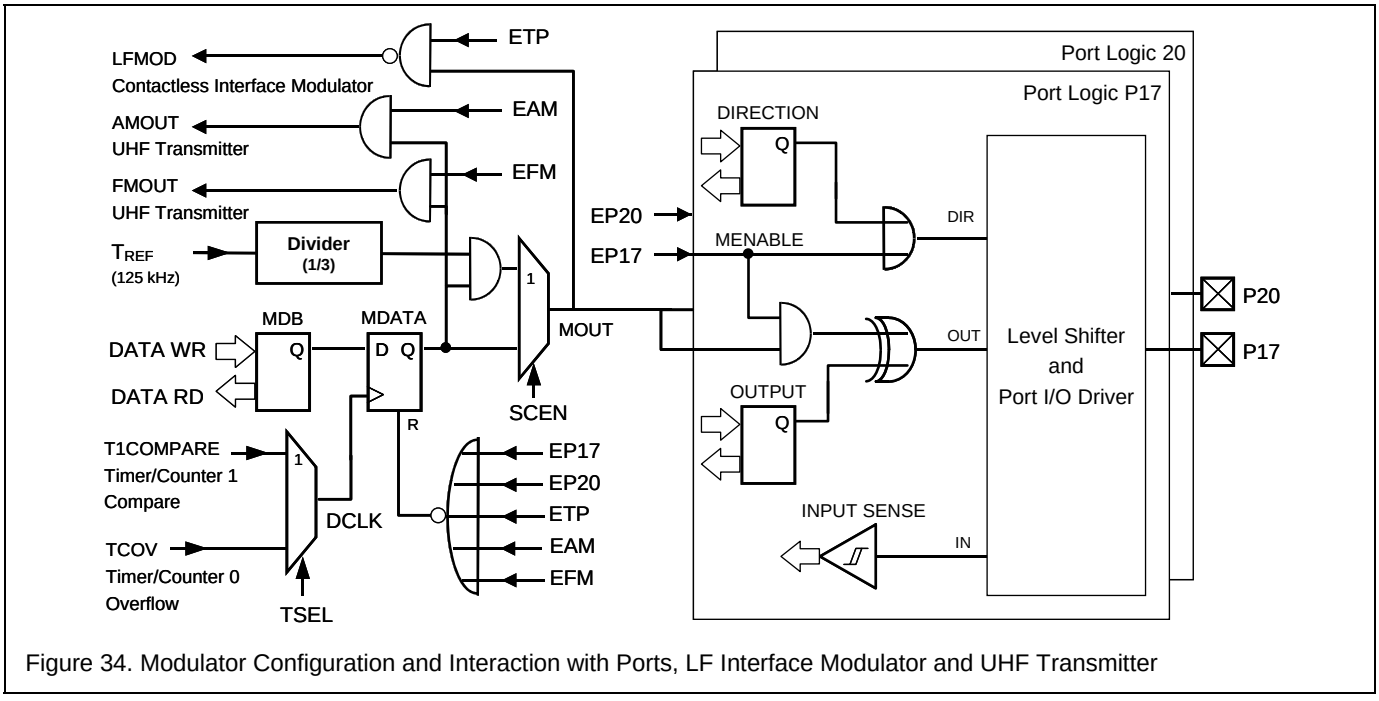


Figure 34. Modulator Configuration and Interaction with Ports, LF Interface Modulator and UHF Transmitter

TSEL, Timer Select

The digital modulator data clock (DCLK) is derived from either the Timer/Counter 0 overflow event (see section 11.4) or from the Timer/Counter 1 Compare match (see section 11.5). The corresponding clock source is selected by TSEL, according to Table 37.

Table 37 Modulator Timer Select, TSEL

TSEL	Used clock	Note
0	Timer/Counter 0 Overflow	
1	Timer/Counter 1 Compare match	

MDB, Modulator Data Bit

The modulator data flip-flop is clocked by the data clock (DCLK) as selected, and in response to a rising edge it latches the data stored in the Modulator Data Buffer, MDB. Subsequently, the corresponding Timer/Counter interrupt service routine shall serve the Modulator Data Buffer with the bit value designated to be output upon the next clock cycle, see Figure 35.

In case Manchester coding shall be implemented, the Timer/Counter consequently need to be operated at twice the desired bit rate.

The data flip-flop MDATA is cleared, in case neither port P17 (EP17) nor P20 (EP20) nor the contactless interface (ETP) nor the UHF Transmitter (EAM, EFM) are being controlled by the modulator.

SCEN, Sub-Carrier Enable

The modulator circuitry features a sub-carrier mode, that can be applied for the signal train generated at port P17 or P20, e.g. for use with Infra-Red transmissions. The sub-carrier is enabled, if the control bit SCEN is set. The sub-carrier is derived from the reference clock by division by three and features a duty cycle of 33%. However, is not synchronized with the bit clock (DCLK), see Figure 36.

The SCEN bit should be cleared while the modulator is not used, in order to minimize power consumption.

Setting of the control bit ETP enables LF Field load modulation. For compatibility reasons, sub-carrier modulation should not be applied for the LF Field, thus the configuration bit SCEN should be cleared in this case.

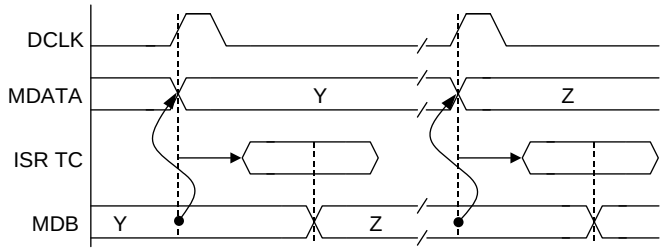


Figure 35. Port Modulator Timing

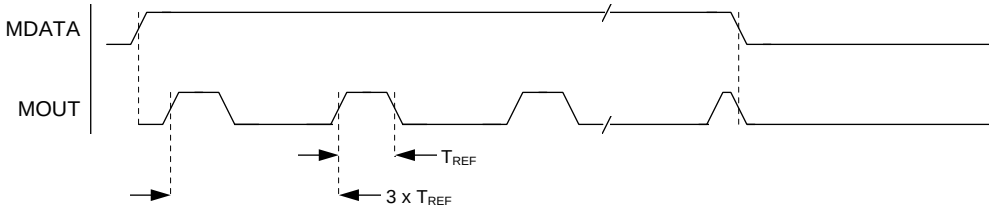


Figure 36. Sub-carrier Timing

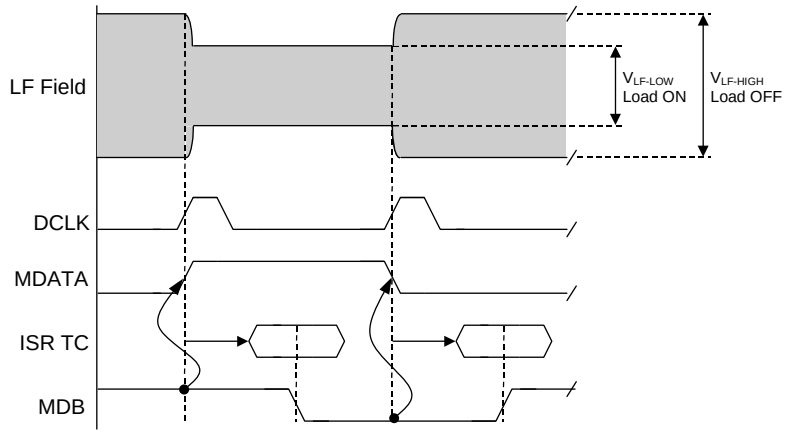


Figure 37. Contactless Interface Modulator Timing

11.9 Voltage Comparator

The device features a voltage comparator with programmable and temperature stabilized reference voltage that is able to monitor the battery supply voltage or a voltage from an external source applied to port P16, see Figure 39.

Utilizing the scheme of a programmable reference voltage and subsequent comparator, an A/D conversion employing the method of successive approximation can be implemented. Latter one is readily available as a library function provided by firmware ROM, see section 23.

The voltage comparator is controlled via the Special Function Register VCON, Table 38.

Table 38 Voltage Comparator Control, VCON

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
VCMP	VSEN	ISEL	X	VST3	VST2	VST1	VST0
R	R/W	R/W	W0	R/W	R/W	R/W	R/W

Note Address = 2FH

1. Bits marked ‘X’ are not connected and reserved for future use. Any read operation yields an undefined result. For future compatibility, a write operation should assign a ‘0’.

VSEN, Voltage Comparator Enable

The voltage comparator is enabled by setting the control bit VSEN. The circuitry needs to settle (t_{RSET}), before the status bit VCMP provides a valid result, see Figure 40.

For power consumption reasons, VSEN should be cleared while operation of the voltage comparator is not required.

ISEL, Input Select

The control bit ISEL provides means to either monitor the battery voltage or a voltage from an external source applied to port P16, see Table 39.

Table 39 Voltage Comparator Input Select, ISEL

ISEL	Source	Note
0	VBAT pin	
1	Port P16	

After changing the voltage source, the circuitry needs to settle (t_{CSET}), before the status bit VCMP provides a valid result, Figure 40.

In case the battery voltage is monitored, a weak resistive divider loads the battery, adjusting the comparator input voltage to a convenient measurement range.

In case an external voltage source is monitored, meaning that the control bit VSEN and ISEL are set at the same time, the direction flip-flop of port P16 is being overruled. Consequently, the corresponding input gate is disabled, forcing port P16 into tri-state, allowing analog operation for P16, see Figure 38.

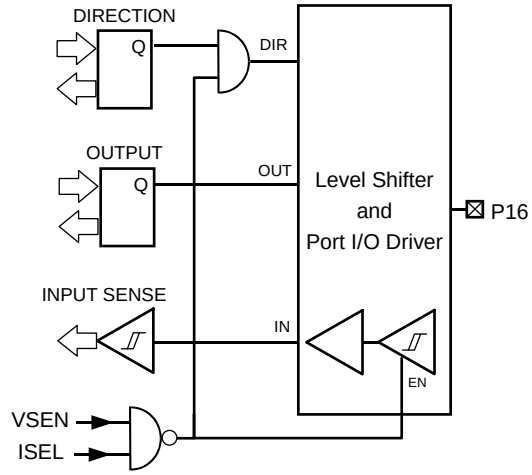


Figure 38. Interaction with Port P16

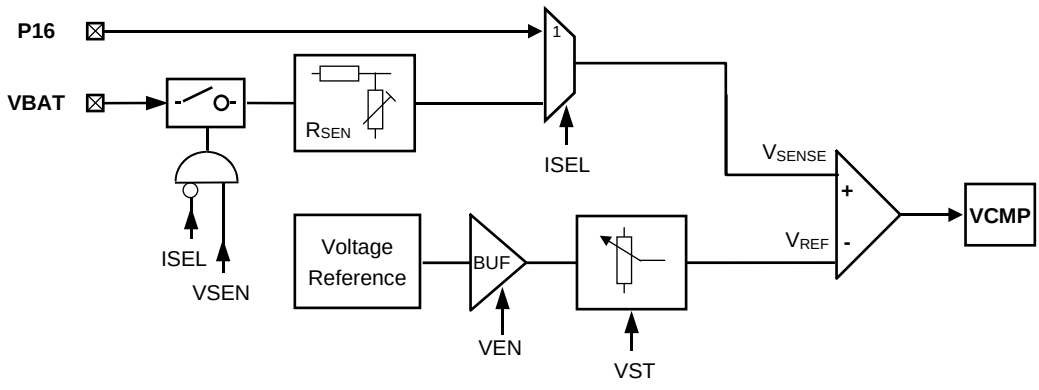


Figure 39. Programmable Voltage Comparator

VCMP, Voltage Compare

The comparator continuously compares the voltage sensed from the selected source (V_{SENSE}) against the programmable reference voltage (V_{REF}). If the sense voltage exceeds the reference voltage, the status bit VCMP is set, otherwise it is cleared.

VST, Reference Voltage Set

The programmable reference voltage can be set to the values as given in Table 40.

The available voltage range and accuracy is different for the two sources (VBAT and P16), as selected by ISEL.

After changing the reference voltage, the circuitry needs to settle (t_{CSET}), before the status bit VCMP provides a valid result, Figure 40.

Table 40 Comparator Reference Voltage Control, VST

VST3	VST2	VST1	VST0	V_{BAT} [V] (typ)	V_{REF} [V] (typ)
0	0	0	0	1.90	0.59
0	0	0	1	1.99	0.62
0	0	1	0	2.08	0.65
0	0	1	1	2.17	0.68
0	1	0	0	2.26	0.71
0	1	0	1	2.35	0.73
0	1	1	0	2.44	0.76
0	1	1	1	2.53	0.79
1	0	0	0	2.62	0.82
1	0	0	1	2.71	0.85
1	0	1	0	2.80	0.88
1	0	1	1	2.89	0.90
1	1	0	0	2.98	0.93
1	1	0	1	3.07	0.96
1	1	1	0	3.16	0.99
1	1	1	1	3.25	1.02

ISEL	0	1

Note

1. The listed voltages indicate the voltage levels that must typically be applied to VBAT respectively to P16, in order to match the internal reference voltage.

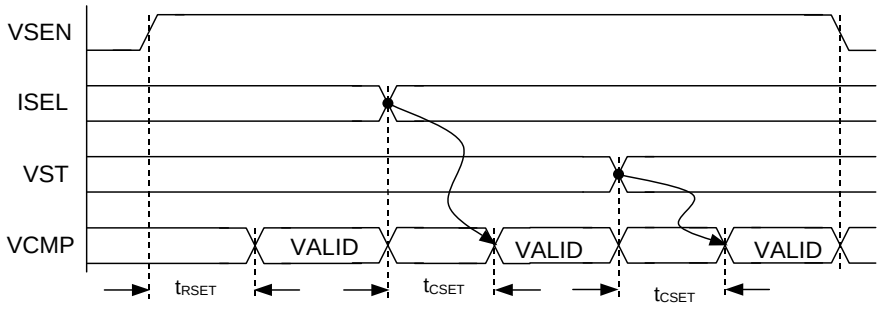


Figure 40. Voltage Comparator Timing

11.10 Calculation Unit

The PCF7961 employs a calculation unit for hardware accelerated device authentication, message encryption and rolling code generation, e.g. in the context of keyless entry functions.

Details concerning the security algorithm implementation are specified in a separate Application Note. Please contact your local NXP representative for more information.

The application program may operate the Calculation Unit in HT2 mode or in HT3 mode. Operating the Calculation Unit in HT2 mode involves a 32 bit Identifier, a 48 bit Secret Key and a 32 bit Random Number. The algorithm operates on a 48 bit Shift Register. The HT3 mode involves a 96 bit Secret Key, a 64 bit Random Number, and a 64 bit Shift Register. In both modes, all values are fully determined by the application program.

The Calculation unit consists of a 64 bit shift register with linear feedback (LF) and nonlinear feedback (OWF, One Way Function) capabilities that feature different characteristics for HT2 and HT3 mode, see Figure 41.

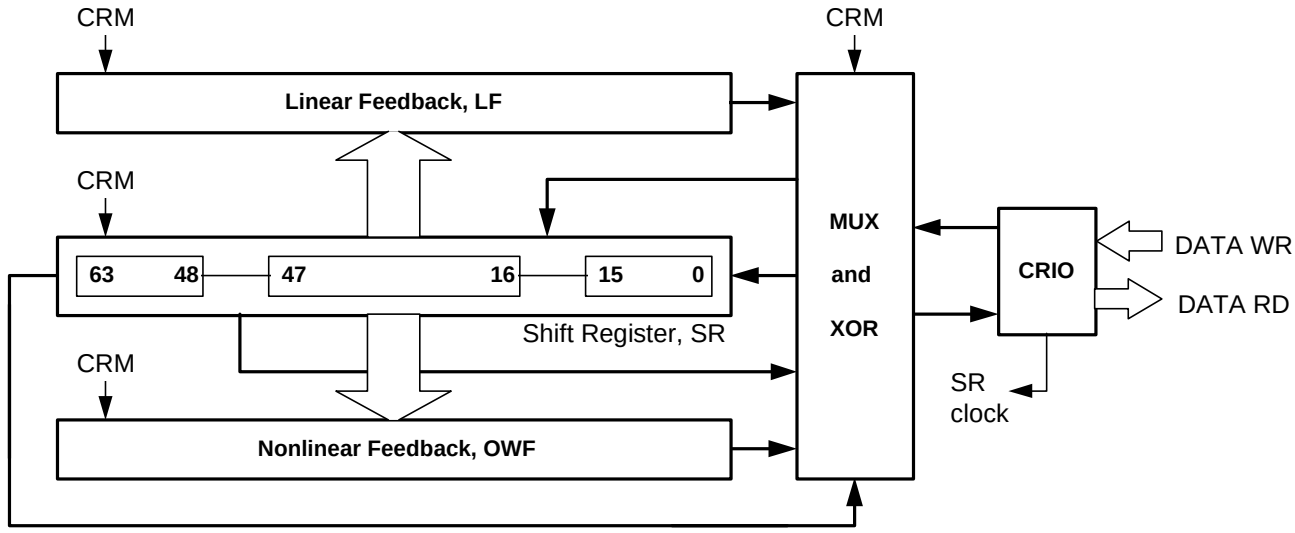


Figure 41. Calculation Unit Block Diagram

Operation of the Calculation Unit is managed by a set of Special Function Registers, CRYP1 and CRYP2, see Table 41.

The Identifier, Random Number, Secret Key and data processed are fed into the Calculation Unit and executed bit by bit under application program control. Their origin is not determined by the circuit design at all. Reading from and writing to the Calculation Unit is provided via the control bit CRIO. Upon each read, write or read-modify-write operation applied to CRYP1, the Calculation Unit Shift Register (SR) is clocked once, causing the Calculation Unit to convey its current value to the new value. This process is completed within one RISC instruction cycle.

The Calculation Unit initialization and operation is managed by a number of functions selected by the control bits CRM, as listed in Table 42.

Switching between the functions does not clock the Calculation Unit at all. However, it may change the value of CRIO, depending on the output value of the linear (LF) or nonlinear feedback (OWF), see the description of functions in the following.

Table 41 Calculation Unit I/O and Control Register

CRYP1, Calculation Unit I/O

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CRIO	X	X	X	X	X	X	X
R/W	W0	W0	W0	W0	W0	W0	W0

Address = 1EH

CRYP2, Calculation Unit Control

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
X	X	X	X	X	CRM2	CRM1	CRM0
W0	W0	W0	W0	W0	R/W	R/W	R/W

Note Address = 1FH

1. Bits marked ‘X’ are not connected and reserved for future use. Any read operation yields an undefined result. For future compatibility, a write operation should assign a ‘0’.

Table 42 Crypt Mode, CRM

CRM2	CRM1	CRM0	Function/Mode	Note
0	0	0	Load 16-HITAG2	
0	0	1	Load 16-Enhanced (HT3)	
0	1	0	Load 0-HITAG2	
0	1	1	Load 0-Enhanced (HT3)	
1	0	0	LF- HITAG2	
1	0	1	LF-Enhanced (HT3)	
1	1	0	OWF- HITAG2	
1	1	1	OWF-Enhanced (HT3)	

Function 0, Load 16-HITAG2

Function 0 is typically used, when the Calculation Unit is operated in HT2 mode, in order to initialize the Shift Register bit by bit. The Shift Register (SR) is operated in 48 bit fashion, bit 48 to bit 63 are not applicable and their values are undefined. The following course of events is triggered with each clock applied to the Calculation Unit:

$(SR_N^+) \leftarrow (SR_{N-1})$; N = 15 - 1

$(SR_0^+) \leftarrow (SR_{47})$

$(SR_N^+) \leftarrow (SR_{N-1})$; N = 47 - 17

$(SR_{16}^+) \leftarrow (CRIO)$

$(CRIO^+) \leftarrow OWF_{HITAG2}(SR^+)$

Note

1. Read operations on CRIO are not allowed and may cause undefined results that are fed into the shift register (Bit 16).

Function 1, Load 16-Enhanced

Function 1 is typically used, when the Calculation Unit is operated in HT3 mode, in order to initialize the Shift Register bit by bit. The Shift Register (SR) is operated in 64 bit fashion. The following course of events is triggered with each clock applied to the Calculation Unit:

$(SR_N^+) \leftarrow (SR_{N-1})$; N = 15 - 1

$(SR_0^+) \leftarrow (SR_{63})$

$(SR_N^+) \leftarrow (SR_{N-1})$; N = 63 - 17

$(SR_{16}^+) \leftarrow (CRIO)$

$(CRIO^+) \leftarrow OWF_{ENHANCED}(SR^+)$

Note

1. Read operations on CRIO are not allowed and may cause undefined results that are fed into the shift register (Bit 16).

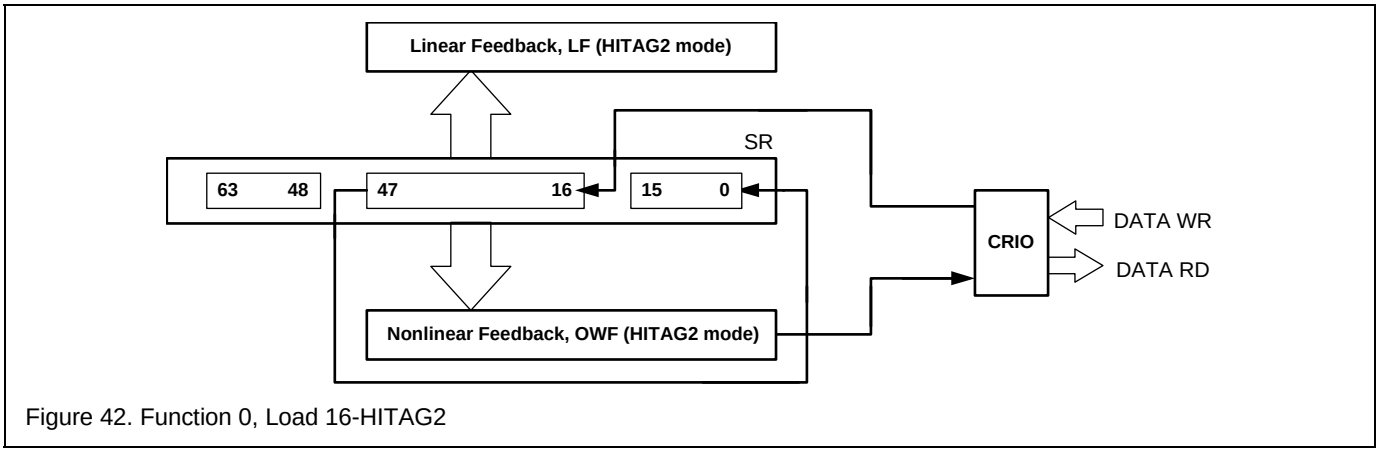


Figure 42. Function 0, Load 16-HITAG2

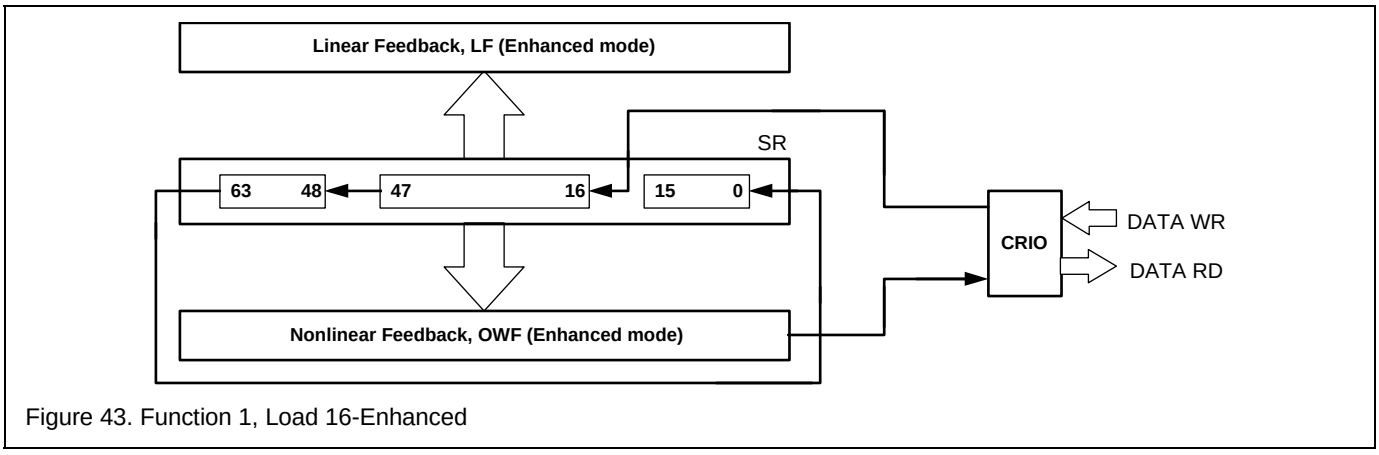


Figure 43. Function 1, Load 16-Enhanced

Function 2, Load 0-HITAG2

Function 2 is typically used, when the Calculation Unit operates in HITAG2 mode, in order to initialize the Shift Register (SR) bit by bit. The Shift Register (SR) is operated in 48 bit fashion, bit 48 to bit 63 are not applicable and their value is undefined. The following course of events is triggered with each clock applied to the Calculation Unit:

$(SR_N^+) \leftarrow (SR_{N-1})$; N = 47 - 1

$(SR_0^+) \leftarrow$ (CRIO)

$(CRIO^+) \leftarrow OWF_{HITAG2}(SR^+)$

Note

1. Read operations on CRIO are not allowed and may cause undefined results that are fed into the shift register (Bit 0).

Function 3, Load 0-Enhanced

Function 3 is typically used, when the Calculation Unit operates in HT3 mode, in order to initialize the Shift Register (SR) bit by bit. The following course of events is triggered with each clock applied to the Calculation Unit:

$(SR_N^+) \leftarrow (SR_{N-1})$; N = 63 - 1

$(SR_0^+) \leftarrow$ (CRIO)

$(CRIO^+) \leftarrow OWF_{ENHANCED}(SR^+)$

Note

1. Read operations on CRIO are not allowed and may cause undefined results that are fed into the shift register (Bit 0).

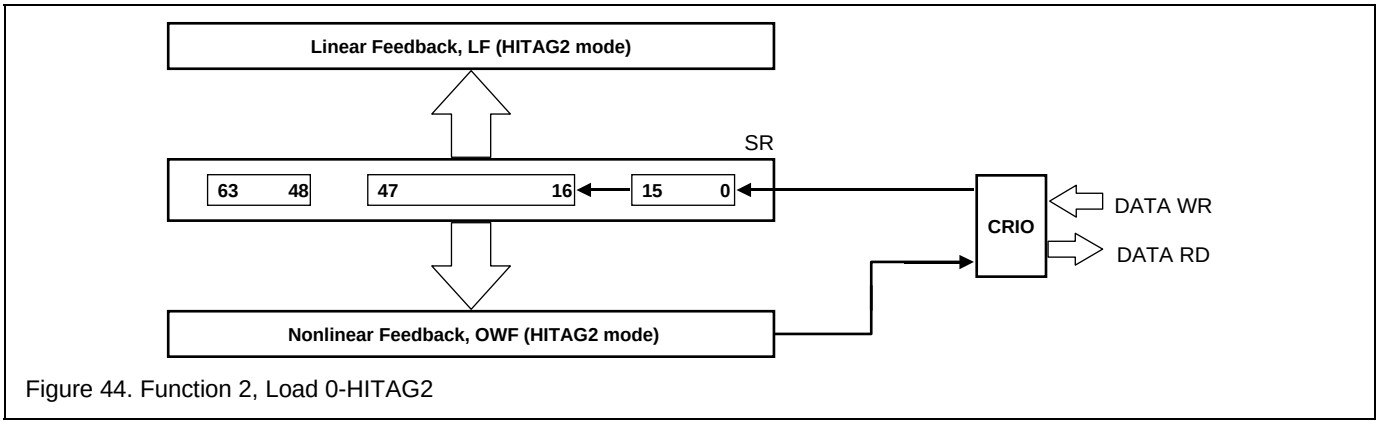


Figure 44. Function 2, Load 0-HITAG2

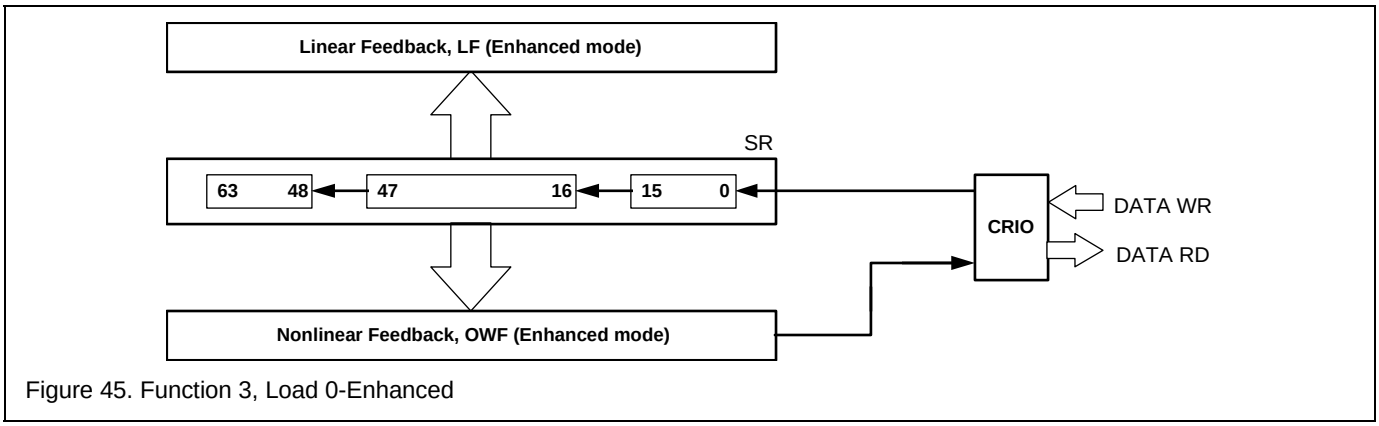


Figure 45. Function 3, Load 0-Enhanced

Function 4, LF-HITAG2

Function 4 is typically used, when the Calculation Unit is operated in HT2 mode, in order to convey the Shift Register (SR) bit by bit involving the linear feedback, which operates in HT2 mode. The Shift Register (SR) is operated in 48 bit fashion, bit 48 to bit 63 are not applicable and their value is undefined.. The following course of events is triggered with each clock applied to the Calculation Unit:

$(SR_N^+) \leftarrow (SR_{N-1}); \quad N = 47 - 1$

$(SR_0^+) \leftarrow LF_{HITAG2}(SR)$

$(CRIO^+) \leftarrow OWF_{HITAG2}(SR^+)$

Note

1. In case a write operation is executed for CRIO, the value written is discarded and finally replaced by new output value of the nonlinear feedback, OWF_{HITAG2} (SR+), after the clock cycle completed.

Function 5, LF-Enhanced

Function 5 is typically used, when the Calculation Unit is operated in HT3 mode, in order to convey the Shift Register bit by bit involving the linear feedback, which operates in HT3 mode. The Shift Register (SR) is operated in 64 bit fashion. The following course of events is triggered with each clock applied to the Calculation Unit:

$(SR_N^+) \leftarrow (SR_{N-1}); \quad N = 63 - 1$

$(SR_0^+) \leftarrow LF_{ENHANCED}(SR)$

$(CRIO^+) \leftarrow OWF_{ENHANCED}(SR^+)$

Note

1. In case a write operation is executed for CRIO, the value written is discarded and finally replaced by new output value of the nonlinear feedback, $OWF_{ENHANCED}$ (SR^+), after the clock cycle completed.

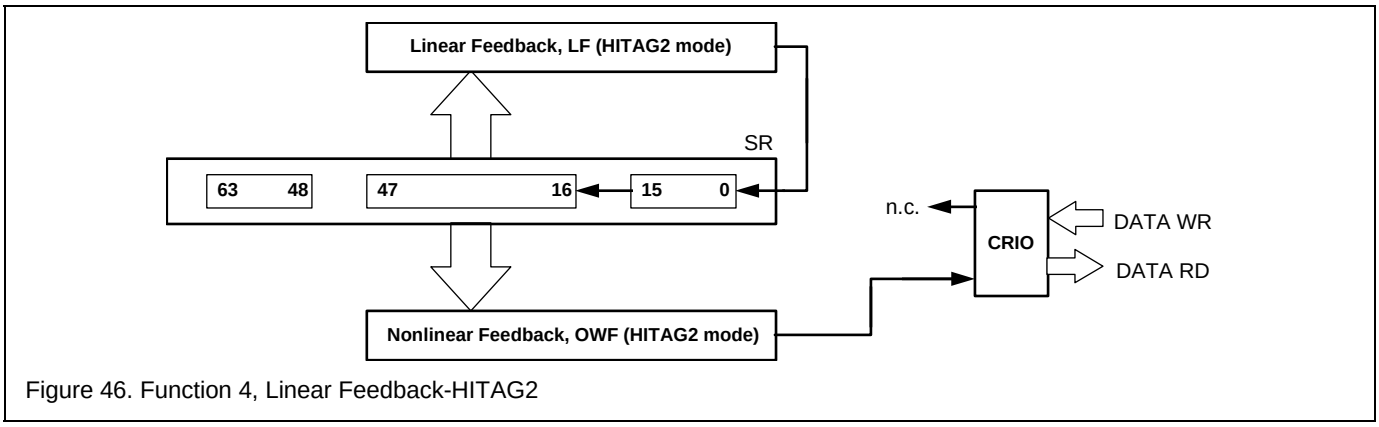


Figure 46. Function 4, Linear Feedback-HITAG2

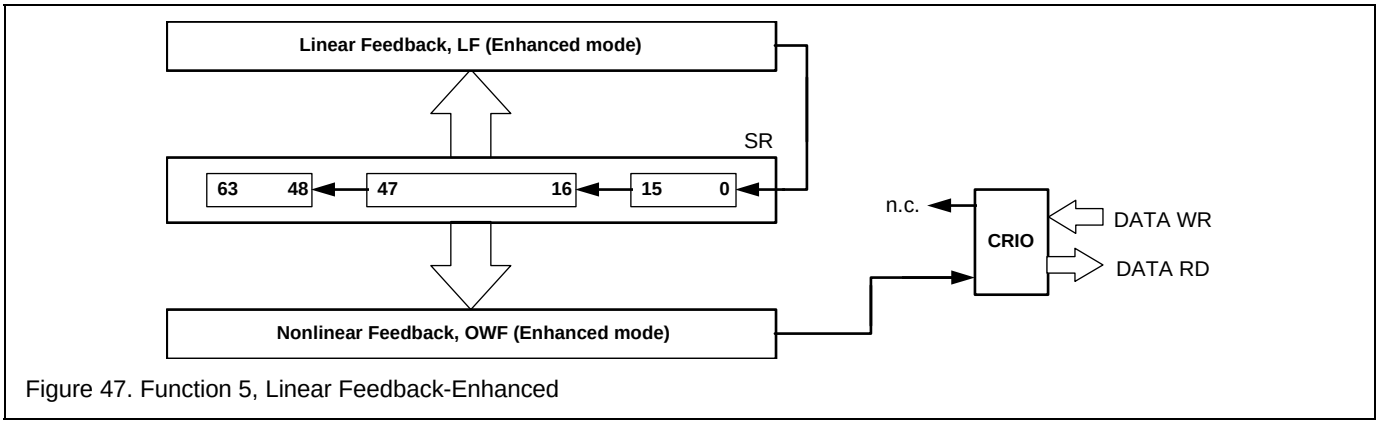


Figure 47. Function 5, Linear Feedback-Enhanced

Function 6, OWF-HITAG2

Function 6 is typically used, when the Calculation Unit is operated in HT2 mode, in order to convey the Shift Register bit by bit involving the nonlinear feedback, which operates in HT2 mode. The Shift Register (SR) is operated in 48 bit fashion, bit 48 to bit 63 are not applicable and their value is undefined. The following course of events is triggered with each clock applied to the Calculation Unit:

$(SR_N^+) \leftarrow (SR_{N-1})$; N = 47 - 1

$(SR_0^+) \leftarrow (CRIO) \oplus OWF_{HITAG2}(SR)$

$(CRIO^+) \leftarrow OWF_{HITAG2}(SR^+)$

Note

1. Read operations on CRIO are not allowed and may cause undefined results that are fed into the shift register (Bit 0).

Function 7, OWF-Enhanced

Function 7 is typically used, when the Calculation Unit is operated in HT3 mode, in order to convey the Shift Register bit by bit involving the nonlinear feedback, which operates in HT3 mode. The Shift Register (SR) is operated in 64 bit fashion. The following course of events is triggered with each clock applied to the Calculation Unit:

$(SR_N^+) \leftarrow (SR_{N-1})$; N = 63 - 1

$(SR_0^+) \leftarrow (CRIO) \oplus (SR_{63}) \oplus OWF_{ENHANCED}(SR)$

$(CRIO^+) \leftarrow OWF_{ENHANCED}(SR^+)$

Note

1. Read operations on CRIO are not allowed and may cause undefined results that are fed into the shift register (Bit 0).

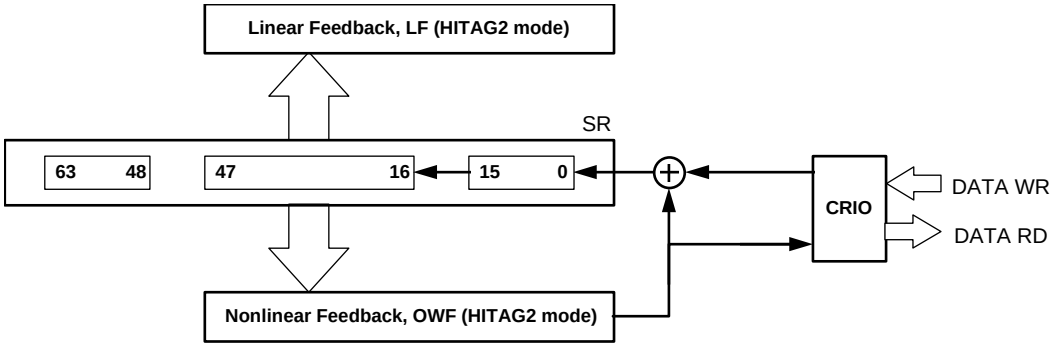


Figure 48. Function 6, Nonlinear Feedback-HITAG2

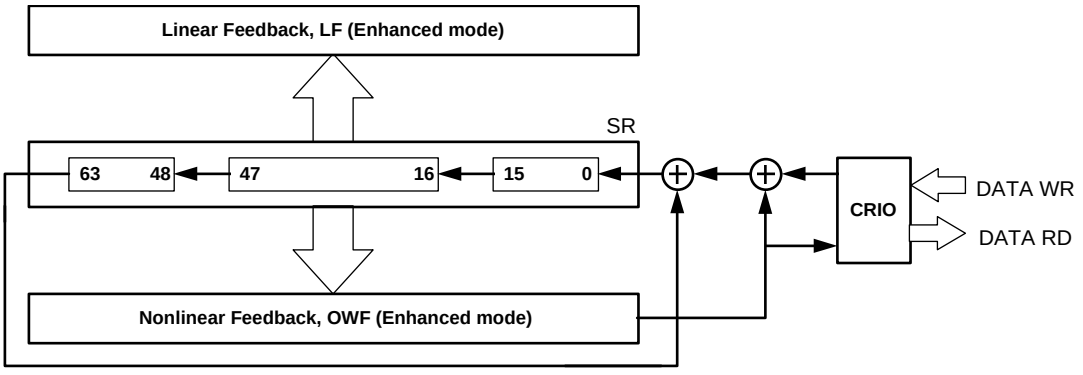


Figure 49. Function 7, Nonlinear Feedback-HT3

12 UHF TRANSMITTER DECRIPTION

The PCF7961X features a sophisticated on-chip ASK/FSK UHF Transmitter designed for use in the ISM frequency range 315 MHz or 434MHz. The UHF Transmitter incorporates an XTAL Oscillator, fully integrated PLL Synthesizer and a Power Amplifier to drive an external antenna, see Figure 50.

The UHF Transmitter allows fine-tuning of the XTAL Oscillator by means of a programmable on-chip XTAL load capacitance, in order to compensate manufacturing tolerances of the crystal. Except for the XTAL itself, no additional external components are required. The Power Amplifier provides means to adjust and stabilize the output power, making it almost independent from battery voltage and temperature changes. It operates in singled-ended configuration and only few external components are needed to match the external antenna.

The UHF Transmitter can be used for both ASK and FSK modulation with data rates up to 20 kbps (Manchester).

The UHF Transmitter is operational only, if the device supply is derived from the battery (BATTERY Mode). It is disabled while the device operates as transponder (TRANSPONDER Mode). However, the XTAL Oscillator is operational in BATTERY and TRANSPONDER Mode, see also section 8.

The UHF Transmitter is controlled by a set of control registers located in the Control Logic and mapped into the Special Function Register range of the RISC Controller.

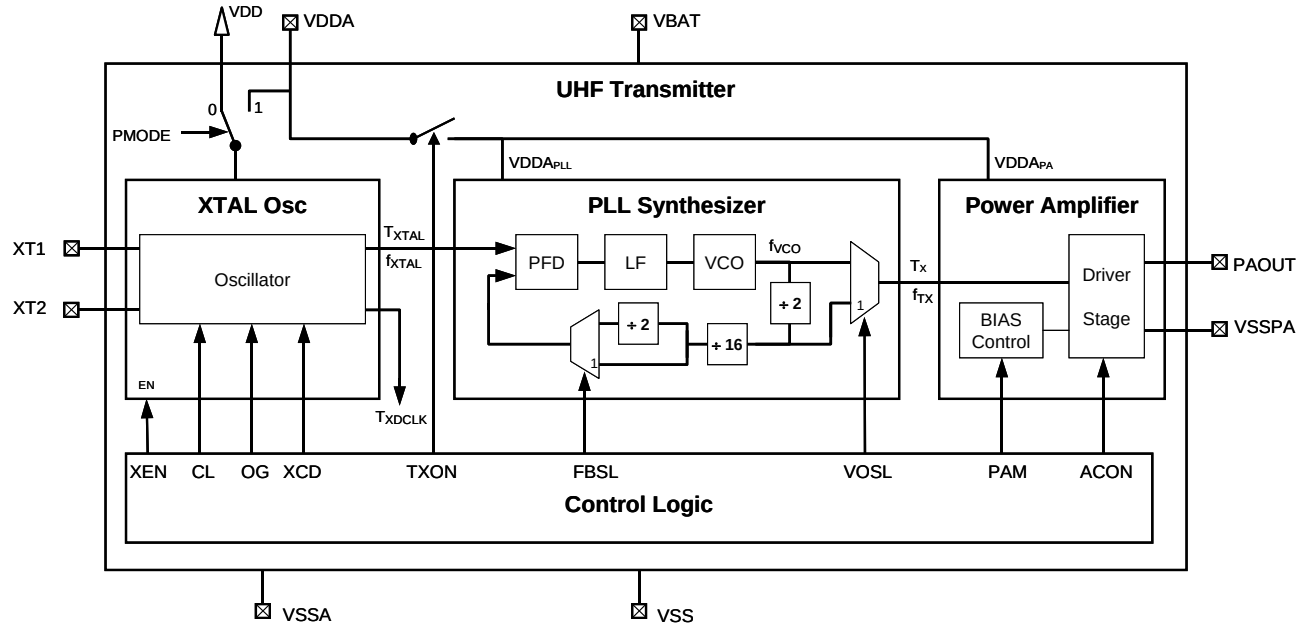


Figure 50. UHF Transmitter Block Diagram

12.1 XTAL Oscillator

The XTAL Oscillator provides the reference clock for the PLL synthesizer and if desired may be used for system timing purposes. Except for the XTAL itself, the XTAL Oscillator does not require any additional external components. The oscillator implementation selected features a programmable on-chip load capacitance for the XTAL, Figure 51.

The programmable load capacitance (CL) allows to fine tune the XTAL frequency, in order to compensate the initial frequency tolerances of the XTAL and for FSK modulation means. The load capacitance is determined via the control register XFCON, see section 12.4 for details. During XTAL start up it is recommended to set the internal load capacitance to its maximum (FCON = 0).

The actual oscillator signal at pin XT1 passes a buffer stage, before it is made available to other device circuitry (T_{XTAL}). The reference clock (T_{XREF}) for the PLL Synthesizer equals the XTAL frequency.

The Timer/Counter clock can be derived from the XTAL Oscillator. Depending on the control bit XCD the XTAL frequency is divided by 3 or 4 prior to use (T_{XDCLK}), in order to satisfy the device maximum clock frequency specification.

The XTAL Oscillator provides gain control (OG) means; in order to determine the XTAL Oscillator start-up and operation conditions, see section 12.4.1 and 22.10.

For proper XTAL oscillator operation it is mandatory to establish proper bias conditions for the XTAL Oscillator circuitry, as determined by NXP during device manufacturing and stored in a reserved EROM location. This task has to be accomplished by the user application program by calling (SYSCALL) the library function PLL_XO_INIT once, prior to enabling the XTAL Oscillator circuitry. The XTAL Oscillator circuitry maintains its initialization condition until a device reset occurs.

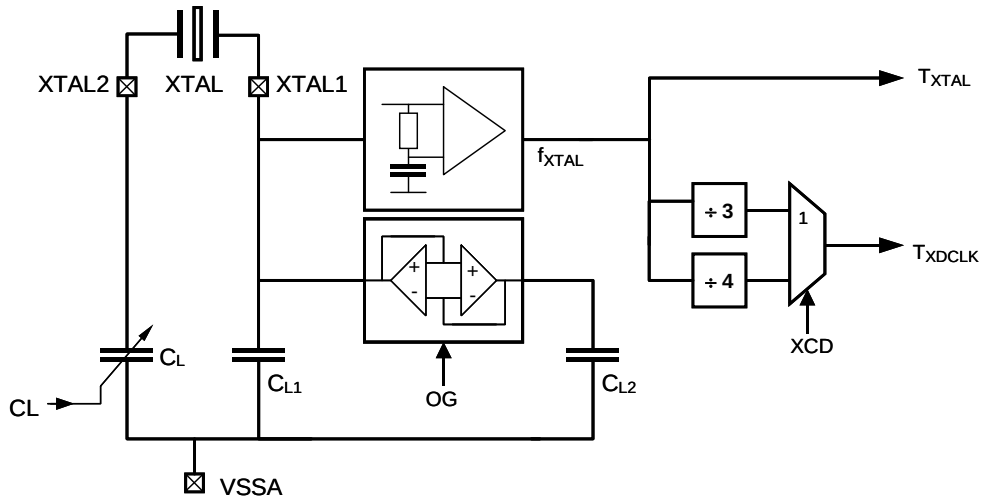


Figure 51. XTAL Oscillator Implementation

12.2 PLL Synthesizer

According to Figure 52 the PLL Synthesizer consist of a fully integrated VCO, Loop Filter (LF), Phase-Frequency Detector (PFD) and a divider chain providing a programmable division ratio of 32 or 64.

The reference clock (T_{XREF}) is derived from the XTAL Oscillator and feeds the Phase-Frequency Detector. The Power Amplifier is driven by the VCO output frequency directly or is divided by two prior to use, depending on the desired carrier frequency.

The divider control bits are located in the control register TXCON2, see section 12.4 for details.

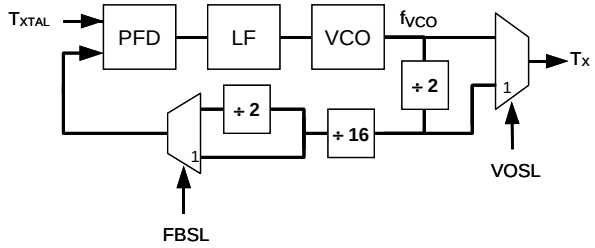


Figure 52. PLL Synthesizer

12.3 Power Amplifier

The Power Amplifier is driven from the PLL Synthesizer and operates in single ended fashion, according to Figure 53.

The Power Amplifier consists of four binary weighted output stages, which are connected in parallel and are operational according to the amplifier control signal ACON, see section 12.4 for details.

The Power Amplifier features three regulated and one unregulated high power output Power Mode, as selected by the control bit PAM. When operating in regulated mode, the output stage drive voltage is controlled by a BIAS circuitry. Each of the three regulated Power Modes delivers a certain output power that is stabilized against supply voltage and temperature variations to a large degree. The lowest Power Mode provides the best regulation characteristics. Hence, select the lowest Power Mode acceptable for the application and eventually control the exact output power by means of the control signal ACON. Further, the available output power is a function of the actual VCO frequency. The higher the VCO frequency, hence its supply voltage (VDD_{VCO}) is, the higher the output power becomes. To select a low VCO frequency is desirable for Japan, due to the limitation in place regarding the radiated output power.

The Power Mode control bits are located in the control register TXCON2, see section 12.4 for details.

The Power Amplifier output (pin PAOUT) does require an external DC path to pin VBAT, established by the antenna loop or a dedicated bias coil. A dedicated ground pin (VSSPA) is provided to improve the RF properties of the circuitry. Pin VSSPA must be connected with pin VSS. Best performance is achieved, if the output voltage swing at pin PAOUT yields one volt less than two times the supply voltage: $V_{PAOUT\ PP} = 2\ (V_{VDDA} - 0.5V)$.

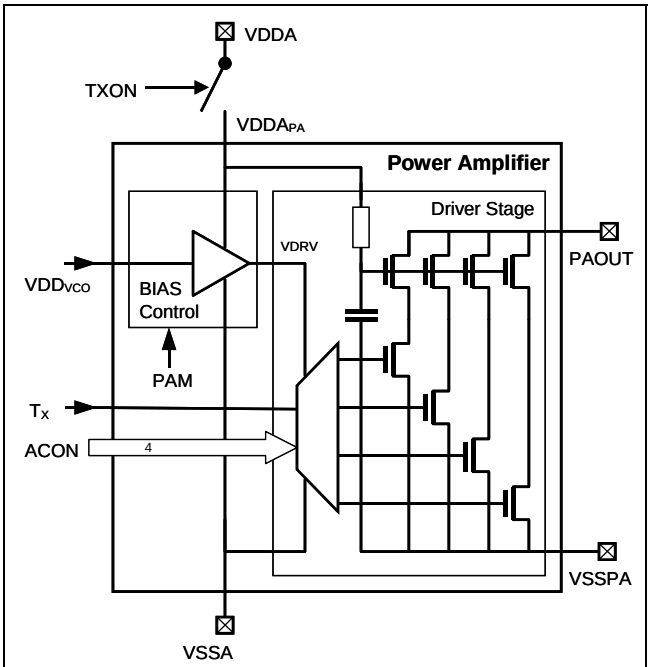


Figure 53. Power Amplifier Implementation

12.4 Control Logic

The Control Logic provides means to configure, tune and control the carrier and modulation of the UHF Transmitter utilizing a set of control register. The control registers are located in the Special Function Register range for access by the RISC Controller, Table 43 to Table 46.

Table 43 XTAL Oscillator Frequency Control, XFCON

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
X	X	XFC5	XFC4	XFC3	XFC2	XFC1	XFC0
W0	W0	R/W	R/W	R/W	R/W	R/W	R/W

Address = 30H

The control register XFCON controls the XTAL Oscillator frequency, for either frequency fine-tuning or FSK modulation means, see section 12.4.2.

Table 44 Power Amplifier Control, PACON

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
AMH3	AMH2	AMH1	AMH0	AML3	AML2	AML1	AML0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address = 31H

The control register PACON controls the Power Amplifier driver stage, for either amplitude fine-tuning or ASK modulation means, see section 12.4.1.

Table 45 Transmitter Control 1, TXCON1

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
X	X	XCD	XFCS	TM	OG1	OG0	XEN
W0	W0	R/W	R/W	R/W	R/W	R/W	R/W

Address = 32H

The control register TXCON1 holds several control bits that enable and control the XTAL Oscillator and XTAL load capacitance.

Table 46 Transmitter Control 2, TXCON2

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
X	X	FBSL	X	VOSL	PAM1	PAM0	TXON
W0	W0	R/W	W0	R/W	R/W	R/W	R/W

Address = 33H

The control register TXCON2 holds more control bits that enable and control the PLL Synthesizer, select the output frequency range and control the Power Amplifier.

12.4.1 Transmitter Set-Up and General Control

Before being operational the UHF Transmitter need to be configured for the desired carrier frequency and operating mode.

The UHF Transmitter may be operated in the 315 MHz or 434 MHz range, with a division ratio of 32 applicable between the desired carrier frequency (f_{TX}) and actual PLL reference frequency (f_{XREF}). Table 47 shows the recommended settings for common XTAL frequencies.

Table 47 UHF Transmitter configuration

FBSL	VOSL	f_{VCO}	f_{TX}	f_{XTAL}
1	0	315 MHz	315 MHz	9.8433 MHz
1	0	434 MHz	434 MHz	13.56 MHz

Note

1. Other settings of FBSL and VOSL are not supported.

The corresponding configuration bits are located in the control register TXCON2.

FBSL, PLL Feedback Select

For proper device operation, the configuration bit FBSL has to be set (FBSL = 1). In this case the VCO frequency is divided by 32 prior to comparison with the PLL reference.

VOSL, VCO Output Select

The configuration bit VOSL determines if the nominal (VOSL = 0) or the divided (VSOL = 1) VCO frequency is fed to the Power Amplifier. Depending on the desired carrier frequency, a certain setting of VOSL is mandatory see above.

OG, XTAL Oscillator Gain Control

The configuration bits OG provide means to influence the gain control of the XTAL Oscillator. According to Table 48 a high gain setting shall be chosen during XTAL start-up, while during ASK or FSK operation a low gain is desirable. The applicable configuration depends on the actual XTAL specification, hence feasible oscillation margin and allowed XTAL drive level. In case an additional series resistor shall be introduced, in order to limit the XTAL drive level, this resistor need to be inserted between the XTAL and pin XTAL1.

Table 48 Typical XTAL Oscillator Gain, OG, settings

OG1	OG0	Gain	Usage	Note
0	0	High	XTAL start-up f_{XTAL} = 13.56 MHz	
0	1	Medium High	XTAL start-up f_{XTAL} = 9.84 MHz	
1	0	Medium Low	FSK or ASK operation f_{XTAL} = 13.56 MHz	
1	1	Low	FSK or ASK operation f_{XTAL} = 9.84 MHz	

XCD, XTAL Clock Divider

A set of clock dividers are available, to cope with a variety of XTAL clock frequencies, in case the XTAL is used as Timer/Counter clock. If the control bit XCD is set the XTAL clock is divided by 3. Otherwise, if cleared, is divided by four prior to further use.

XEN, XTAL Oscillator Enable

The control bit XEN provides means to enable (XEN = 1) the XTAL Oscillator any time desired. The XTAL Oscillator provides the reference clock for the PLL Synthesizer. In addition, the XTAL Oscillator clock (T_{XTAL}) is available to the Timer/Counters and may be used for timing purposes. If XEN is zero, the XTAL Oscillator is disabled and consumes virtually no current.

The XTAL Oscillator start-up characteristics and final frequency is controlled by dedicated control bits see section 12.4.2.

TXON, Transmitter Power On

The control bit TXON provides means to power-up (TXON = 1) the PLL Synthesizer and Power Amplifier circuitry. To avoid spurious emission, the Power Amplifier shall be muted (ACON = 0) during power-up and the PLL Synthesizer (VCO) allowed to start-up and lock first. Latter one requires that the XTAL Oscillator is operational (XEN = 1).

If TXON is zero, the PLL Synthesizer and Power Amplifier are shut-off and disconnected from the supply pin (VDDA) not drawing any significant quiescent current.

12.4.2 XTAL Oscillator Control and FSK Modulation

The XTAL Oscillator features an on-chip programmable XTAL load capacitance, capable of to fine-tune the XTAL frequency and to introduce a FSK modulation if desired. A unique feature of the Programmable Load Capacitance is to fine-tune the XTAL to the desired frequency once it is oscillating, see Figure 55.

The Programmable Load Capacitance comprises of 64 weighted capacitors, chosen in a way to provide an almost linear frequency shift of the XTAL frequency versus the control signal FCON, Figure 54. The actual XTAL load capacitance is calculated according to Table 49.

The applicable XTAL load capacitance is determined by the 6bit register FML (Frequency LOW) and FMH (Frequency HIGH).

XFC[5…0], XTAL Oscillator Frequency Control

The control register FML (Frequency LOW) and FMH (Frequency HIGH) cannot be manipulated directly, instead are accessed for reading and writing through the control bits XFC depending on the state of the control bit XFCS.

The control bits XFC are located in the control register XFCON.

XFCS, XTAL Frequency Control Select

Depending on the state of the control bit XFCS either the register FMH (XFCS = 1) or FML (XFSC = 0) can be accessed for reading and writing, utilizing the control register XFC.

The control bits XFCS is located in the Control register, TXCON1.

TM, Transparent Mode

Changing the XTAL Load Capacitance typical employs an Up/Down counter, in order to implement a smooth transition from the present to the new value, step by step. When the control bit TM is set, the Up/Down counter is forced into transparent state, making any change to become effective immediately.

The control bit TM is located in the Control register, TXCON1.

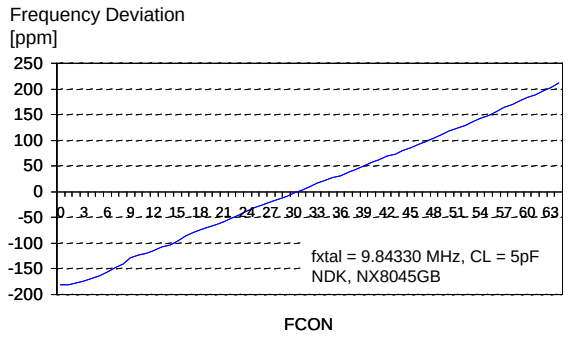


Figure 54. Typical Frequency Deviation

Table 49 XTAL Load Capacitance

FCON	CL [pF]	Note
0_D … 7_D	30.700 pF – FCON * 2.270 pF	
8_D … 15_D	12.540 pF – (FCON – 8D) * 0.700 pF	
16_D … 23_D	6.940 pF – (FCON – 16D) * 0.340 pF	
23_D … 31_D	4.220 pF – (FCON – 24D) * 0.199 pF	
32_D … 39_D	2.628 pF – (FCON – 32D) * 0.128 pF	
40_D … 47_D	1.604 pF – (FCON – 40D) * 0.089 pF	
48_D … 55_D	0.892 pF – (FCON – 48D) * 0.066 pF	
56_D … 63_D	0.364 pF – (FCON – 56D) * 0.052 pF	

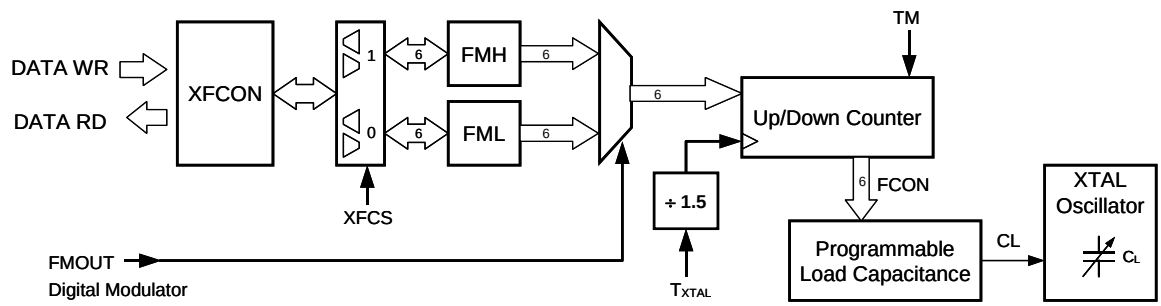


Figure 55. XTAL Load Capacitor Control

Frequency modulation of the carrier is achieved by varying the XTAL frequency. Hence, by switching between the FMH and FML register in accordance to control signal FMOUT, which is derived from the Digital Modulator, Figure 56.

If the Digital Modulator is disabled, the control signal (FMOUT) is low, enabling constant frequency operation with the XTAL frequency determined by the control register FML, see also section 11.8.

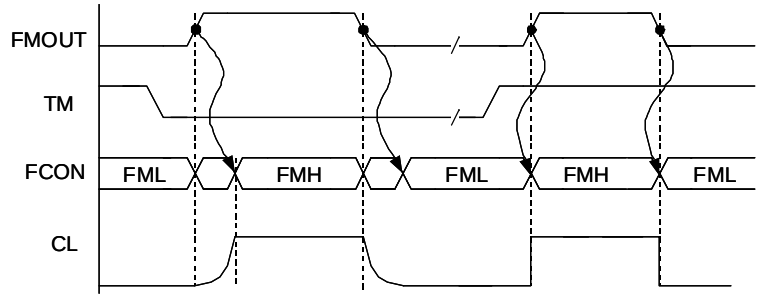


Figure 56. FSK Modulation Timing

12.4.3 Power Amplifier Control and ASK Modulation

The device features several control bits controlling the output amplitude and ASK modulation characteristics of the Power Amplifier see Figure 57.

The control register PACON features two 4bit values that set the HIGH (AMH) and LOW (AML) level during amplitude modulation of the UHF carrier. Amplitude modulation is achieved by switching between the HIGH and LOW level in accordance to control signal AMOUT, which is derived from the Digital Modulator output see section 11.8.

If the Digital Modulator is disabled, the control signal (AMOUT) is low, enabling continuous wave operation with the output amplitude determined by the control bits AML.

AMH[3…0], Amplitude Modulation HIGH

In case the control signal AMOUT is high, the actual value of AMH determines the UHF carrier output amplitude, by controlling (ACON) the four binary weighted Power Amplifier output stages.

The control bits AMH are located in the Power Amplifier Control register, PACON.

AML[3…0], Amplitude Modulation LOW

In case the control signal AMOUT is low, the actual value of AML determines the UHF carrier output amplitude, by controlling (ACON) the four binary weighted Power Amplifier output stages.

The control bits AML are located in the Power Amplifier Control register, PACON.

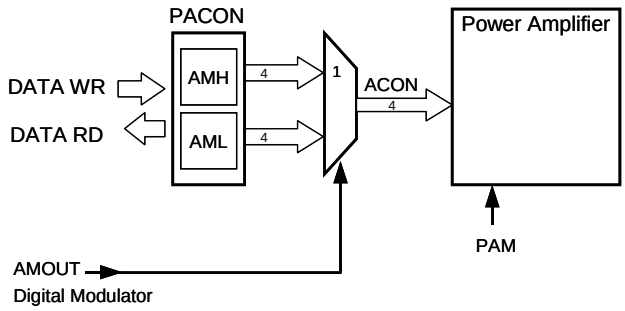


Figure 57. Power Amplifier Control

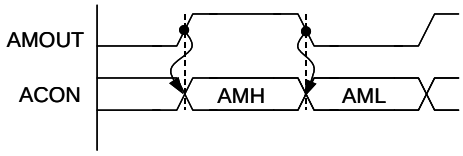


Figure 58. ASK Modulation Timing

PAM[1,0], Power Amplifier Mode

The Power Amplifier feature means to stabilize the output power against battery voltage and ambient temperature variations. If desired, the corresponding circuitry can be disabled, enabling the Power Amplifier to deliver the highest output power available, Table 50

Table 50 Power Amplifier Modes, PAM

PAM1	PAM0	Power Mode	Comment	Note
0	0	I	Low power Highest stability	
0	1	II	Medium power Medium stability	
1	0	III	High power Low stability	
1	1	IV	Maximum power Stabilization OFF	

Note

1. The lower the available output power selected, the better the stability against temperature and battery voltage variations.

The control bits PAM only determine the available output power, the actual output power is set by the Power Amplifier Control bits AMH and AML (PACON register).

The control bits PAM are located in the control register TXCON2.

13 DEVICE MODES

The device features different Device Modes affecting the overall device behavior, the Monitor and Download Interface operation and user ability to access the EEPROM and E-ROM.

The Device Mode is controlled by a set of configuration bytes, which are located in the EEPROM and E-ROM.

The configuration bytes may not be altered by the user directly, instead, requires to utilize the corresponding Monitor and Download command, see section 15.

INIT Mode

When the device is supplied from NXP, it is configured for INIT mode by default, according to section 11.1.

The INIT mode shall be used during software development only. The Monitor and Download Interface is fully operational, enabling the customer to initialize the EEPROM and E-ROM as desired for the application, in accordance with the access restrictions in place by design, see section 25.

To protect the EEPROM and E-ROM from readout and to disable the debug features, the device must be forced into PROTECTED mode finally.

Leaving the device in INIT mode, may cause the device to execute a software break, in case a LOW pulse is detected at pin MSDA. Latter one would terminate execution of the application program and would invoke built-in debug program. In this case, execution of the application program is interrupted until a proper debug command is issued or a device reset is applied, see also section 22.4.

PROTECTED Mode

In the moment the device is set for PROTECTED mode, the EEPROM and E-ROM are protected against altering and readout via the Monitor and Download Interface, and the debug features are disabled. The PROTECTED mode has to be used during system testing and in the application finally.

The device may be forced into INIT mode again, by issuing a corresponding command (C_ER_EROM) via the Monitor and Download Interface. Latter one sets the EEPROM and the E-ROM to a predefined state before the INIT mode is resumed. Hence, discards all application related EEPROM data and the E-ROM based application program. However, in case this sequence does not complete successfully, the device enters TAMPERED mode.

TAMPERED Mode

The TAMPERED mode is entered temporarily during the sequence, which forces the device from PROTECTED mode back into INIT mode. If this sequence does not complete successfully, thus is interrupted, the TAMPERED mode will be entered.

The device may be forced into INIT mode, by again issuing a corresponding command (C_ER_EROM) via the Monitor and Download Interface. Latter one sets the EEPROM and the E-ROM to a predefined state before the INIT mode is resumed. Hence, discards all application related EEPROM data and the E-ROM based application program. However, in case this sequence does not complete successfully, the device remains in TAMPERED mode until a new attempt is made, by issuing the command (C_ER_EROM) again.

VIRGIN Mode

After manufacturing, the device operates in VIRGIN mode, enabling extended device test and device configuration. Finally, NXP forces the device into INIT mode and the VIRGIN mode is irreversibly locked, in order to ensure it cannot be activated again.

14 BOOT ROUTINE

After any device reset, either forced by a Port Wake Up condition or a LF Field Reset or interrogated by the application program, program execution starts with the ROM based BOOT routine. The BOOT routine executes a sequence of instructions that configures the device and evaluates the device mode and transponder configuration. Subsequently, invokes the Transponder Emulation, the Application Program (WARM BOOT) or the Monitor, see Figure 59.

14.1 Functional Description

In the moment the BOOT routine commences, the pin MSCL is set high for test purposes in the context of Debug Monitor Mode activation. Subsequently, the on-chip RC Oscillator and other device circuitry are initialized according to the Device Configuration (DCFG) values stored in the EEPROM.

Next, the present device mode is evaluated. In case the device signals TAMPERED mode, device operation is halted, to render the device useless. Latter one is signaled by a MSCL low-to-high transition. Unless MSDA is detected low, causing the device to interrogate the MONITOR routine. See below.

Next, the device verifies the supply condition, by testing the Supply Switch state (PMODE). Device operation commences in TRANSPONDER Mode, in case PMODE signals an LF Field supply condition (PMODE = 0) or an LF Field is being detected (FLD = 1), even if a battery supply condition is present (PMODE = 1). In the latter case the device will ignore the battery supply and forces an LF Field supply condition (PMODE = 0). In this case, the system clock is derived from the Contactless Interface clock recovery circuitry (LF Field clock).

Subsequently, the device will evaluate the device configuration as stored in EEPROM (DCFG, see also section 11.1.1.2) regarding the Transponder Emulation. In case the Transponder Emulation is disabled (TEN = 0) the device will utilize the WARM BOOT vector TRANSPONDER (0010_H) after completion of the BOOT routine. Otherwise, in case the Transponder Emulation is enabled (TEN = 1), the BOOT routine quits and passes control directly to the Monolithic Transponder Emulation of the PCF7938XA. The detailed device operation during Monolithic Transponder Emulation is described by the HT3 Family ROM library (MRKII) specification, see section 23.

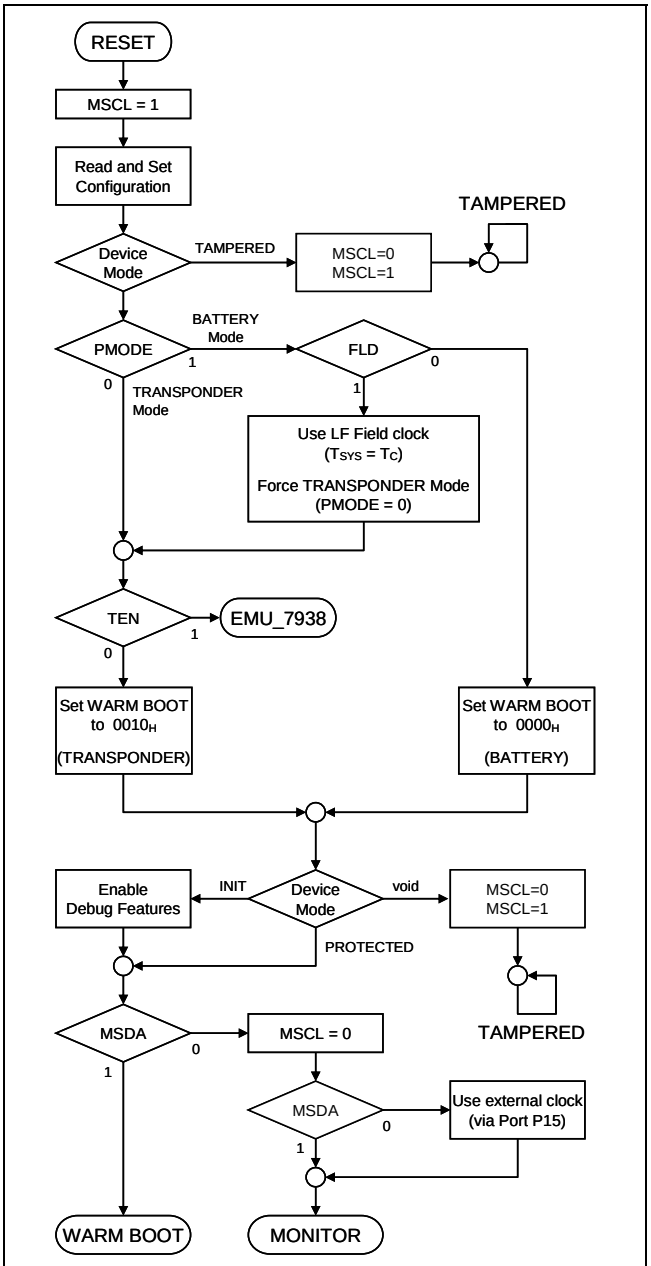


Figure 59. Flow Chart BOOT Routine

Anyhow, when verifying the supply condition, by testing the Supply Switch state (PMODE), the BOOT routine may also detect BATTERY Mode (PMODE = 1) and no LF Field being present (FLD = 0). In this case, the device will utilize the WARM BOOT vector BATTERY (0000H) after completion of the BOOT routine.

Finally, the BOOT routine verifies the Device Mode again to enable the debug features if the device is configured for INIT mode. Otherwise, if the device is set to PROTECTED mode, the debug features are not available. Prior to passing device control to the corresponding WARM BOOT location in the Application Code Memory, the pin MSDA is tested. If MSDA is high, the WARM BOOT is executed. In case MSDA is detected low, the MONITOR routine is interrogated. See below.

Any other coding of the Device Mode configuration bits is not valid and is handled like the device being in TAMPERED Mode, causing to halt device operation, to render the device useless. Latter one is signaled by a MSCL low-to-high transition. Unless MSDA is detected low, causing the device to interrogate the MONITOR routine.

In case the BOOT sequence leads to interrogation of the MONITOR routine, the device either uses an internal or external device clock, according to the timing of MSCL and MSDA. For a detailed description, reference is made to the PCF7961 Monitor and Download Interface specification, see section 23.

It is worth mentioning that in case the MONITOR has been entered accidentally, while the device is set to PROTECTED or TAMPERED Mode, the on-chip Watchdog Timer terminates the Monitor mode again, in case no valid monitor command is received.

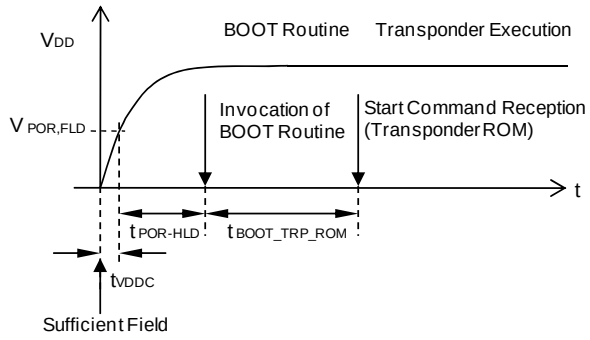


Figure 60. Power up timing for Transponder Emulation (ROM, TEN=1)

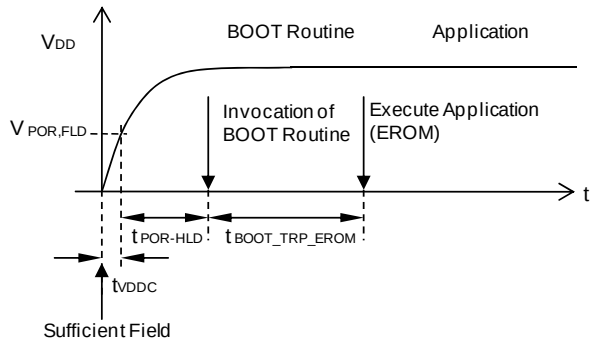


Figure 61. Power up timing for LF powered application (EROM, TEN=0)

14.2 Execution Time

The total execution time of the BOOT routine depends on the device configuration and application conditions. According to Figure 60 and Figure 61 the BOOT routine commences as soon as the power on reset hold delay timeouts ($t_{POR-HLD}$) and terminates with the invocation of the Application Program (WARM BOOT) or Transponder Emulation, see also section 8.1.

Presence of LF Field

In case device start-up is caused by the presence of an LF Field, the BOOT routine execution time is a function of the Transponder Emulation configuration, see 'Power up timing' in Figure 60 and Figure 61. $t_{BOOT\_TRP\ \_ROM}$ is the Device Boot time for Transponder execution in ROM. $t_{BOOT\_TRP\_EROM}$ is the Device Boot time for Application or Transponder execution in E-ROM; additional boot time caused by execution of the program code in the E-ROM is not included. t_{VDDC} is the charge time of the C_{VFLD} capacitor until the POR level is reached and is explained in an application note which is available on request.

Port Wake Up (button press)

In case device start-up is caused by a Port Wake Up (PWUP = 1) and no LF field is present the BOOT routine execution time yields the value t_{BOOT_WUP} (see Figure 62).

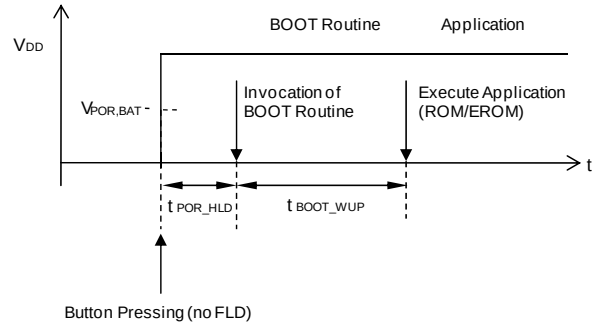


Figure 62: Power up timing for battery supply modes

Presence of LF Field and Port Wake Up (button press)

In case device start-up is caused by a Port Wake Up (PWUP = 1) and an LF Field is present in the same moment (FLD = 1), device start-up occurs in BATTERY Mode (PMODE = 1). However, the BOOT routine forces the device into TRANSPONDER Mode finally (PMODE = 0). The BOOT routine execution time yields the value $t_{BOOT\_WUP\_FLD}$, as shown in Figure 63 (TEN=0) and Figure 64 (TEN=1).

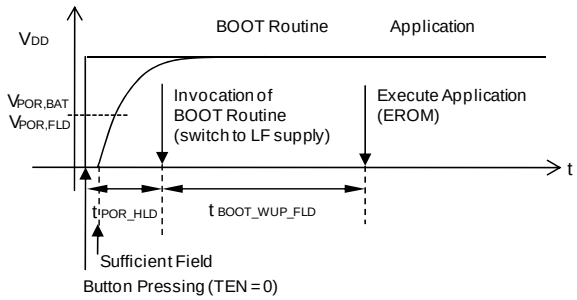


Figure 63: Power up timing for Port wake up and LF field (TEN=0)

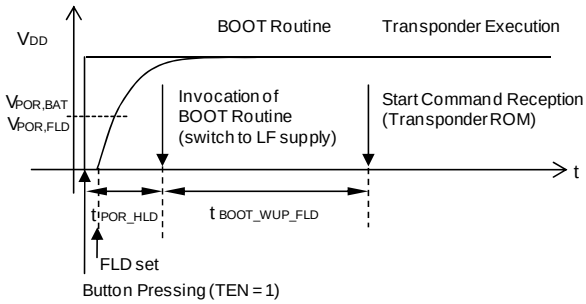


Figure 64. Power up timing for Port wake up and LFfield (TEN=1)

15 MONITOR AND DOWNLOAD INTERFACE

The Monitor and Download Interface is implemented as a serial interface that utilize the MSDA and MSCL pin. This interface provides means to initialize the EEPROM and E-ROM , as well as provides debug features during application program development. The Monitor and Download routine does occupy some Stack space, which needs to be considered during application program design.

The majority of the features provided by the Monitor and Download Interface are available only, if the device is set into INIT mode, which is the factory default setting. When performing system tests and field trials, the device shall be set to PROTECTED mode. Latter one locks the EEPROM and E-ROM content, protecting it against alteration and read out, as well as disables the debug features. The device may be forced back into INIT mode by a dedicated operation (Monitor and Download command C_ER_EROM), which will set the EEPROM and E-ROM to a predefined state, see also section 12.

For more details, reference is made to the PCF7961 Monitor and Download Interface description, see section 23.

For development and prototyping purposes dedicated tools are available that are part of the PCF7961X development tool set, see section 24.

16 EEPROM CONTENT AT DELIVERY

The PCF7961X EEPROM content is initialized during device manufacturing, according to Table 51.

However, the EEPROM content may be changed as desired by the application, except for the page 0 and page 127. Page 0 holds the device Identifier (IDE) and serves the function of a serial number and product type ID, while page 127 holds device configuration data.

Table 51. EEPROM Content Upon Delivery

Content [HEX]	Page	Note
XX XX XX 4X	0	1
11 11 22 22	1	
33 33 44 44	2	
55 55 66 66	3	
00 XX XX XX	4	2
XX XX XX XX	5 to 119	
00 00 00 00	120 to 123	
reserved	124	
XX XX XX XX	125 to 126	
X6 XX 80 00	127	

MSB LSB

Note

1. Bit 7 to 4 of this page (Identifier) serve the function of a product type (application) identifier and are set to ‘0100’ for the PCF7961X. For system compatibility reasons, PCF7x22 (KEECART) uses the same product type Identifier.
2. Initially the device is configured for the standard EQ pattern and all protection flags in the TMCF byte are cleared. The customer may change the configuration as desired for the application.
3. Locations marked ‘X’ are undefined and may hold any pattern.

Consequently, the device is initially configured for PCF7938XA (HT3) transponder emulation and set to INIT mode, providing full support regarding the Monitor and Download Interface, see section 12.

17 LIMITING VALUES

All values are in accordance with Absolute Maximum Rating System (IEC 134).
V_{SS} = 0V; V_{SSA} = 0V; V_{SSPA} = 0V

PARAMETER	MIN	MAX	UNIT
Operating temperature range	-40	+85	°C
Storage temperature range	-55	+125	°C
Voltage at any I/O, V_{BAT} and V_{DDA} pin to V_{SS}, Note 4	-0.5	3.6	V
Voltage at V_{PAOUT} pin to V_{SS}	-0.5	7.2	V
Voltage at any I/O pin to V_{SS}	-0.5	V_{BAT} +0.3	V
Peak input current for pin IN1 and IN2		30	mA
Peak output current LOW (I_{OL}) port P1x and P2x, except P26O, Note 6		15	mA
Peak output current LOW (I_{OL}) port P26O, Note 6		30	mA
Latch-up current, Note 1	100		mA
ESD, human body model, Note 2	2		kV
ESD, human body model for pins V_{BAT} / V_{DDA} and V_{SS} / V_{SSA}, Note 2	3		kV
ESD, machine model, Note 3	200		V
Power dissipation		120	mW

Notes

1. According to JEDEC, JESD 17
2. According to JEDEC, JESD 22-A114
3. According to JEDEC, JESD 22-A115
4. Because of to the device concept and design, pin VFLD, IN1 and IN2 may show a higher voltage during normal device operation, caused by a corresponding input signal applied to IN1 and IN2.
5. Please note P26O is not available in TSSOP20 package

18 ELECTRICAL CHARACTERISTICS

18.1 Operating Conditions

Tamb = -40 to +85°C, V_{SS} = 0V, f_C = 125kHz, $T_O = 1/f_C$ and C_{VFLD}= 10nF.
Unless otherwise specified.

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
TRANSPONDER Mode, (LF Field Supply)						
V_{BAT}	Battery supply voltage	Note 1	-0.2		3.6	V
I_{IN}	Coil input peak current	$\lvert I_{IN} \rvert$			6	mA
f_c	LF field carrier frequency			125		kHz
MI_{WR}	Minimum modulation Index, Write direction	$V_{IN-HIGH}$ = 5Vp,$T_{TMOD} = 8T_0$ Note 8		100	95	%
V_{FLD}	Rectified supply voltage	Note 2	2.4		5.5	V
$V_{THR,FD}$	LF Field Detect threshold voltage	$V_{FLD} – V_{SS}$	2.0		2.4	V
$V_{THR,FD-VIN}$	LF Field Detect threshold voltage (peak)	$\lvert V_{IN1} - V_{IN2} \rvert$	3.0		3.7	V
Device executes from ROM (e.g. Transponder Emulation, SCSL = 0), V_{FLD} = 3.0V, Note 3						
$I_{CC-RFLD}$	Supply current			16	30	µA
Device executes from E-ROM, V_{FLD} = 3.0V, Note 3						
I_{CC-2M} $I_{CC-125k}$ $I_{CC-IDLE}$	RUN mode @ T_{SYS} = 2 MHz RUN mode @ T_{SYS} = 125 kHz IDLE mode	EEPROM disabled, A/D converter disabled		420 60 35	600 100 80	µA µA µA
BATTERY Mode, (Battery Supply), V_{IN} = 0, V_{BAT} = 3.0V						
V_{BAT}	Battery supply voltage	Note 10	2.1	3.0	3.6	V
$I_{QQ,APP}$	POWER-OFF quiescent current in application configuration	V_{BAT} = 3.6V, Note 4, 9 Tamb = -20 to +25°C		0.1	1	µA
$I_{QQ,APP}$	POWER-OFF quiescent current in application configuration	V_{BAT} = 3.6V x; Note 4, 9			3	µA
Device executes from ROM, V_{BAT} = 3.0V, Note 4						
$I_{BAT-R2M}$ $I_{BAT-R125k}$ $I_{BAT-RIDLE}$	RUN mode @ T_{SYS} = 2 MHz RUN mode @ T_{SYS} = 125 kHz IDLE mode	EEPROM disabled, A/D converter disabled		215 35 17	500 80 50	µA µA µA
Device executes from E-ROM, V_{BAT} = 3.0V, Note 4						
I_{BAT-2M} $I_{BAT-125k}$ $I_{BAT-IDLE}$	RUN mode @ T_{SYS} = 2 MHz RUN mode @ T_{SYS} = 125 kHz IDLE mode	EEPROM disabled, A/D converter disabled		450 60 30	600 100 80	µA µA µA
TRANSPONDER Mode or BATTERY Mode, Note 5						
ΔI_{DD-EE}	Supply current EEPROM (ERASE/WRITE)	Note 6		20	50	µA
ΔI_{DD-VC}	Supply Current Voltage Comparator	Note 7		20	35	µA
Power On Reset (POR)						
$V_{POR,FLD}$	Power-On Reset threshold	$V_{FLD} – V_{SS}$	1.8		2.1	V
$V_{POR,BAT}$	Power-On Reset threshold	$V_{BAT} - V_{SS}$	1.8		2.1	V

Notes concerning section Operating Conditions

1. External measures for reverse battery connection must be applied to ensure transponder operation in such case.
2. During transponder operation the rectified supply voltage must not drop below the specified value ($V_{POR,FLD}$) and the input voltage at IN1 and IN2 must not drop below $V_{THR,FD-VIN}$ for more than $t_{FLD,0-DLY}$, otherwise a device reset may occur, see also section 9.1
3. Specifies the internal chip operating current that needs to be supplied from the rectified supply voltage. Input/output current of ports (P1 and P2) zero. Value measured according to Figure 66.
4. No external clock (P15) applied to device and input/output current of ports (P1 and P2) zero.
5. Specifies the additional internal chip operating current caused by the corresponding circuitry, if enabled, which has to be added to the device operating current (I_{CC} respectively I_{BAT}) in order to determine the total device operating current. Value measured according to Figure 67.
6. The specified current applies during the EEPROM ERASE/WRITE cycle only (t_{ERWR}).
7. When the Voltage Comparator is enabled and the VBAT pin selected as source (ISEL = 0), the battery is loaded with the sense resistor (R_{SEN}). The sense current caused needs to be added to load drawn from the battery.
8. The demodulator sensitivity applicable in write direction is defined according to Figure 65 and characterized at a worst-case decay time (T_{DECAY}) according to Figure 68.
9. Represents the quiescent current in a typical application wiring. Value measured according to Figure 67.
10. E-ROM ERASE/WRITE supported at VBAT $\geq$ 2.5 V only.

18.2 AC/DC Characteristics

Tamb = -40 to +85°C, V_{SS} = 0V, f_C = 125kHz and C_{VFLD}= 10nF.
Unless otherwise specified.

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Contactless Interface, V_{FLD} = 3V						
C_{IN}	Input capacitance	Note 1	6	8	10	pF
$R_{1\text{-}LIN}$	Input resistance at IN1, linear	V_{IN1} = 0.5V, V_{IN2} = 0V, Note 2	1.6	2.5	3.0	kΩ
$R_{1\text{-}NLIN}$	Input resistance at IN1, non-linear	V_{IN1} = 1.5V, V_{IN2} = 0V, Note 2	0.48	0.9	1.46	kΩ
$R_{2\text{-}LIN}$	Input resistance at IN2, linear	V_{IN1} = 0V, V_{IN2} = 0.5V, Note 2	3.4	5.2	6.4	kΩ
$V_{CLP\text{-}IN}$	Input limiter clamp voltage, Note 3	I_{IN} = ±6mA			7.2	V
		I_{IN} = ±150µA	4.2			V
$V_{THR,CR}$	Clock Recovery threshold (peak)	Note 4		40	100	mV
P1, P2 (General Purpose I/O), (V_{BAT} = 3V, unless otherwise specified)						
C_I	Pin capacitance	V_{IN} = 0.1V_{RMS}, f = 1MHz		5		pF
$C_{I\text{-}P15}$	Pin capacitance	V_{IN} = 0.1V_{RMS}, f = 1MHz		5	7	pF
V_{IL}	Input low voltage		-0.1		0.2 V_{BAT}	V
V_{IH}	Input high voltage		0.8 V_{BAT}		V_{BAT} + 0.1	V
I_{IL}	Input low current	V_{IL} = 0			0.5	µA
I_{IH}	Input high current	V_{IH} = V_{BAT}			0.5	µA
V_{OL}	Output low voltage	I_O = 4mA			0.4	V
V_{OH}	Output high voltage	I_O = -4mA	V_{BAT} - 0.4			V
I_{PU}	Pull-Up current	V_I = 0V	30	75	150	µA

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Voltage Comparator, VSEN = 1						
R_{SEN}	Sense Load Resistance			150		kΩ
Battery Voltage Sense, ISEL = 0						
$V_{THR,BAT}$	Threshold voltage battery monitor	VST = 00H	1.84	1.90	1.96	V
		VST = 01H	1.93	1.99	2.05	V
		VST = 02H	2.02	2.08	2.14	V
		VST = 03H	2.11	2.17	2.23	V
		VST = 04H	2.20	2.26	2.32	V
		VST = 05H	2.29	2.35	2.41	V
		VST = 06H	2.38	2.44	2.50	V
		VST = 07H	2.47	2.53	2.59	V
		VST = 08H	2.56	2.62	2.68	V
		VST = 09H	2.65	2.71	2.77	V
		VST = 0AH	2.74	2.80	2.86	V
		VST = 0BH	2.83	2.89	2.95	V
		VST = 0CH	2.92	2.98	3.04	V
		VST = 0DH	3.01	3.07	3.13	V
		VST = 0EH	3.10	3.16	3.22	V
		VST = 0FH	3.19	3.25	3.31	V
Port (P16) Voltage Sense, ISEL = 1, Note 5						
$V_{THR,P16}$	Threshold voltage Port P16	VST = 00H		0.59		V
		VST = 01H		0.62		V
		VST = 02H		0.65		V
		VST = 03H		0.68		V
		VST = 04H		0.71		V
		VST = 05H		0.73		V
		VST = 06H		0.76		V
		VST = 07H		0.79		V
		VST = 08H		0.82		V
		VST = 09H		0.85		V
		VST = 0AH		0.88		V
		VST = 0BH		0.90		V
		VST = 0CH		0.93		V
		VST = 0DH		0.96		V
		VST = 0EH		0.99		V
		VST = 0FH		1.02		V

Notes see next page.

Notes concerning section AC/DC Characteristics

1. Input capacitance across IN1 and IN2. Value determined by characterization.
2. Measured in TRANSPONDER Mode while the internal modulator is active, thus the additional load is ON (S2 closed), according to Figure 69.
3. Value measured in TRANSPONDER Mode, according to Figure 70.
4. Value measured according to Figure 66.
5. Due to reference voltage spreads, the accuracy is limited to ± 50mV.

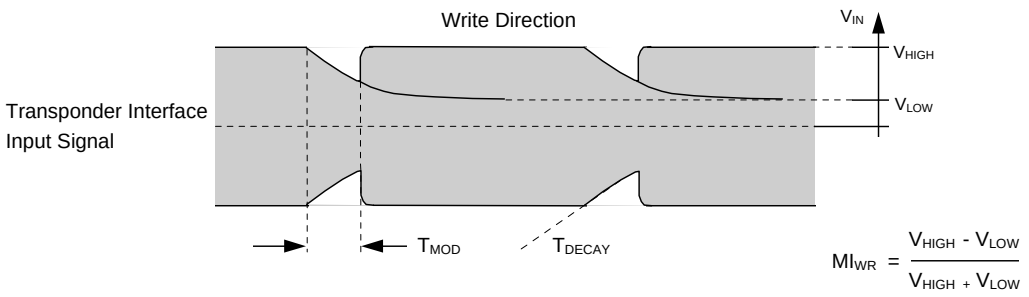


Figure 65. Transponder Demodulator Specification

18.3 UHF Transmitter Operating Conditions

Tamb = -20 to +70°C, $V_{BAT} = V_{DDA}$, V_{SS} = 0V
Unless otherwise specified.

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
V_{DDA}	Supply Voltage		2.1	3.0	3.6	V
$V_{DDA,SU}$	Supply Voltage, XTAL start-up	Note 2	2.2	3.0	3.6	V
I_{DDA-PD}	Supply current in Power-Down mode	XEN = 0, TXON = 0			0.5	µA
$I_{DDA-XTAL}$	Supply current XTAL Oscillator ON	V_{BAT} = 3.0V, XEN = 1, TXON = 0 FCON = 0				
		OG = 3, f_{TXAL} = 9.84 MHz		350	800	µA
		OG = 2, f_{TXAL} = 13.56MHz		400	850	µA
$I_{DDA-VCO}$	Supply current VCO ON	V_{BAT} = 3.0V, XEN = 1, TXON = 1 FCON = 0, ACON = 0				
		OG = 3, f_{TXAL} = 9.84 MHz		1.2	2	mA
		OG = 2, f_{TXAL} = 13.56MHz		1.5	2.3	mA
ΔI_{PA}	Power Amplifier current in Transmit mode f_{TX} = 315 MHz, Note 1	V_{BAT} = 3.0V XEN = 1, TXON = 1, VOSL = 0 FCON = 0, OG = 3, ACON = “1111”				
		PAM = ‘10’, RL ~ 200 Ω		7.3	9.9	mA
		PAM = ‘00’ RL ~ 700 Ω		1.1	2.0	mA
ΔI_{PA}	Power Amplifier current in Transmit mode f_{TX} = 434 MHz, Note 1	V_{BAT} = 3.0V XEN = 1, TXON = 1, VOSL = 0 FCON = 0, OG = 2, ACON = “1111”				
		PAM = ‘10’, RL ~ 200 Ω		8.3	10.9	mA
		PAM = ‘00’ RL ~ 700 Ω		1.5	2.4	mA
$I_{DD,TX}$	Supply current in Transmit mode		$I_{BAT} + I_{DDA-VCO} + \Delta I_{PA}$			
f_{TX}	Carrier frequency range		310		450	MHz
f_{VCO}	VCO Frequency		310		450	MHz
f_{XTAL}	XTAL Oscillator Frequency		9.7		14.1	MHz

Notes

1. Load tank circuit according to Figure 71.
2. During XTAL oscillator start-up the minimum supply voltage must yield the specified value.

18.4 UHF Transmitter AC/DC Conditions

Tamb = -20 to +70°C, $V_{BAT} = V_{DDA} = 3.0V$, $V_{SS} = 0V$
Measured at 50 Ohm reference board, unless otherwise specified.

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
XTAL Oscillator, XEN = 1						
R_{MARGIN}	Oscillation startup margin, Note 3	$V_{BAT} = V_{DDA} = 2.2V$, Tamb = 25°C				
		f_{TXAL} = 9.84 MHz, OG = 1_D	800	1800		Ω
		f_{TXAL} = 13.56 MHz, OG = 0	600	1200		Ω
C_{XT1}	Pin capacitance	Tamb = 25°C, OG = 3_D	14.1	17.4	20.7	pF
		Input resistance –50 Ω				
C_{XT2}	Pin capacitance	Tamb = 25°C, FCON = 0	26.3	32		pF
		Tamb = 25°C, FCON = 63_D		2	2.9	pF
t_{XTSET}	XTAL Oscillator settling time	$V_{BAT} = V_{DDA} = V_{DDA,SU}$, XFC = 0				
		OG = 1, f_{XTAL} = 9.84MHz		0.5	1.5	ms
		OG = 0, f_{XTAL} = 13.56MHz		0.4	1.5	ms
PLL Synthesizer, XEN = 1, TXON = 1						
B_{LOOP}	Loop bandwidth, Note 2	f_{TXAL} = 9.84 MHz		320		kHz
		f_{TXAL} = 13.56 MHz		430		kHz
PN_{PLL}	Phase noise	PAM = “10”, ACON = “1111”				
	Matched into 50 Ω, R_L ~ 200 Ω	10 kHz offset		-86	-66	dBc/Hz
		100 kHz offset		-84	-64	dBc/Hz
		1 MHz offset		-92	-72	dBc/Hz
		10 MHz offset		-115	-95	dBc/Hz
E_{REF}	Reference spurious emissions	ACON = “1111”, PAM = ‘10’		-45	-35	dBc
	$f_{TX} \pm f_{XTAL}$					
t_{ACQ}	PLL Acquisition time	XEN = 1, TXON = 1		0.1	0.5	ms
Power Amplifier, XEN = 1, TXON = 1, Note 1						
P_{OUT}	Output power	ACON = “1111”, PAM = ‘10’				
	f_{TX} = 315 MHz, matched into 50 Ω	RL ~ 200 Ω	5.8	8.5	10.6	dBm
		RL ~ 700 Ω	2.2	4.0	5.5	dBm
		ACON = “1111”, PAM = ‘00’				
		RL ~ 700 Ω	-16	-7	2	dBm
		ACON = “0000”, PAM = ‘10’			-45	dBm
P_{OUT}	Output power	ACON = “1111”, PAM = ‘10’				
	f_{TX} = 434 MHz, matched into 50 Ω	RL ~ 200 Ω	6.5	9.0	11	dBm
		RL ~ 700 Ω	2.2	4.5	6.5	dBm
		ACON = “1111”, PAM = ‘00’				
		RL ~ 700 Ω	-11.5	-4	3	dBm
		ACON = “0000”, PAM = ‘10’			-45	dBm

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Power Amplifier, XEN = 1, TXON = 1 at 25°C, Note 1						
P_{OUT}	Output power f_{TX} = 315 MHz, matched into 50 Ω	ACON = “1111”, PAM = ‘10’ RL ~ 200 Ω RL ~ 700 Ω ACON = “1111”, PAM = ‘00’ RL ~ 700 Ω	 6.8 2.7 -15	 8.5 4.0 -7	 10.2 5.1 1	 dBm dBm dBm
P_{OUT}	Output power f_{TX} = 434 MHz, matched into 50 Ω	ACON = “1111”, PAM = ‘10’ RL ~ 200 Ω RL ~ 700 Ω ACON = “1111”, PAM = ‘00’ RL ~ 700	 7.5 3 -10.5	 9.0 4.5 -4	 10.5 6.0 2.5	 dBm dBm dBm
Modulation						
$f_{MOD,ASK}$	ASK modulation frequency	Duty cycle 50%			20	kHz
$f_{MOD,FSK}$	FSK modulation frequency	Duty cycle 50%			20	kHz
Duty Cycle of modulated signal, Note 4						
$t_{DUTY,FSK}$	Duty cycle of modulated FSK signal	Duty cycle (mod. Signal) 50%, f_{TXAL} = 9.84 MHz, Tamb = 25°C, OG = 3, Modulation: 9.6 kHz FCON = 0 - FCON = 63_D	45		55	%

Notes

1. Load tank circuit according to Figure 71.
2. Derived from chip simulation, not tested.
3. The given R_{MARGIN} (Oscillation margin) is tested and guaranteed only at room temperature (Tamb = 25°C) and a supply voltage of $V_{BAT} = V_{DDA}$ = 2.2V and oscillator gain setting OG = 1 for f_{XTAL} = 9.84 MHz and OG = 0 for f_{XTAL} = 13.56 MHz. To guarantee sufficient oscillation startup margin every reference application board has to be checked individually by the customer.
4. Application advice, the duty cycle is not measured during production test. It is strongly recommended to check every reference application board by the customer individually, since PCB parasitic and the chosen type of XTAL influence the duty-cycle.

19 TIMING CHARACTERISTICS

19.1 General

V_{BAT} = 2.1V to 3.6V, Tamb = -40 to +85°C, f_C = 125 kHz, $T_C = 1/f_C$ and C_{VFLD} = 10nF.
Unless otherwise specified.

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
On-chip RC Oscillator						
T_{OSC}	Clock period	Tamb = -20 to +85°C	0.23	0.25	0.27	µs
T_{OSC}	Clock period		0.225	0.25	0.275	µs
$T\Delta_{OSC}$	Clock jitter	V_{BAT} = 3.0V, Note 2			10	ns
System Clock						
T_{SYS}	System Clock				2.2	MHz
T_{XDCLK}	Divided XTAL Clock				4.4	MHz
Reference Clock						
T_{REF}	Reference Clock	Note 1	87.5	125	137.5	kHz
External Clock via P15 ($P15_{CLK}$)						
f_{XCLK}	External clock frequency				3.5	MHz
t_{XCH}	External clock high time		125			ns
t_{XCL}	External clock low time		125			ns
t_{XCR}	External clock rise time				0.5	µs
t_{XCF}	External clock fall time				0.5	µs

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Power Management						
$t_{POR-HLD}$	Power On Reset Hold wait time				0.48	ms
$t_{BOOT\_TRP\_EROM}$	Wait time for Device Boot, Transponder executed in E-ROM	PMODE = 0, TEN = 0, Notes 3, 9			0.46	ms
$t_{BOOT\_TRP\_ROM}$	Wait time for Device Boot, Transponder executed in ROM	PMODE = 0, TEN = 1, Note 3			8.25	ms
t_{BOOT_WUP}	Wait time for Device Boot, WakeUp event, WakeUp on Battery	PMODE = 1, FLD = 0, Notes 3, 9			0.75	ms
$t_{BOOT\_WUP\_FLD}$	Wait time for Device Boot, WakeUp on Battery, Field on	PMODE = 1(0), FLD = 1, TEN = 0, Notes 3, 4, 9			0.75	ms
$t_{BOOT\_WUP\_FLD}$	Wait time for Device Boot, WakeUp on Battery, Field on, Transponder executed in ROM	PMODE = 1(0), FLD = 1, TEN = 1, Notes 3, 5			8.75	ms
T_{PSMF}	Port Sense mono-flop duration		5		100	µs
Voltage Comparator						
t_{CSET}	Comparator settling time				2	µs
t_{RSET}	Reference Voltage settling time				20	µs
EEPROM						
T_{RET}	Data retention time	Tamb = 50°C	20			years
N_{WR-CYL}	Write endurance EEPROM	Tamb = 25°C, Note 7	200 k			cycles
N_{E-ROM}	Write endurance E-ROM	Tamb = 25°C, Note 8	10 k			cycles
t_{EEPU}	EEPROM Power Up time				8	µs
t_{EEDLY}	EEPROM Access delay				3	µs
t_{ERWR}	ERASE/WRITE time EEPROM	Note 6		384		T_{REF}

Notes concerning section TIMING CHARACTERISTICS General

1. When the device is clocked from the XTAL Oscillator, the corresponding clock divider must be set in a way that the specification for T_{REF} is satisfied.
2. Value represents the maximum deviation from nominal clock period. No supply voltage ripple present.
3. Under normal operation: Timing based on 125kHz LF transponder clock; Monitor and Download Interface disabled (MSDA = 1), see also section 14.1
4. Device start-up occurs with PMODE = 1, however, due to an LF Field present (FLD = 1), the BOOT routine forces the device into Application Mode finally (PMODE = 0), see also section 14.1
5. Device start-up occurs with PMODE = 1, however, due to an LF Field present (FLD = 1), the BOOT routine forces the device into TRANSPONDER Mode finally (PMODE = 0), see also section 14.1
6. Value holds for the EEPROM circuitry ERASE/WRITE time. Some readily available ROM Library functions may perform multiple EARSE/WRITE operation, e.g. WRITE_SYNC command and add execution, see also section 23.
7. Endurance test is performed by a corresponding monitor flow at a product with structural similarity regarding the EEPROM cell design. According to Arhennius' Law, assuming an activation energy of 0.15eV, the number of useful cycles at room temperature is about 2.5 times higher than at 85°C.
8. E-ROM ERASE/WRITE supported at VBAT ≥ 2.5 V only.
9. Value does not include additional application dependant boot time caused by execution of the program code in the E-ROM.

19.2 Contactless Interfaces

Tamb = -40 to +85°C, f_C = 125 kHz (typical) and C_{VFLD}= 10nF.
Unless otherwise specified.

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Demodulator						
t_{ADLY}	Analog output setup delay				40	µs
t_{AHDLY}	Analog output HIGH setup delay		4	20	40	µs
t_{ALDLY}	Analog output LOW setup delay			4	16	µs
t_{DSETUP}	Demodulator setup time				100	µs
t_{IDLE}	Idle time				80	ms
LF Field Power On, Note 2						
t_{VDDC}	Wait time for C_{VFLD} charge	Note 3		2		ms
LF Field Detection (Power On Reset)						
$t_{FLD,0\text{-}DLY}$	LF Field Low detection delay time		0.6		6	ms
$t_{RESET,SETUP}$	Wait time for LF Field Power On Reset setup	Note 4	10			ms

Notes

1. Additional timing characteristics for Command Handling and Data Transmission are specified in the HT3 family data sheet, see reference in section 23.
2. The total start-up time of the transponder consists of t_{VDDC} + $t_{POR\text{-}HLD}$ + $t_{BOOT\_TRP\_ROM,}$ as shown in Figure 60.
3. The time t_{VDDC} is application dependent and mainly determined by the coupling factor and C_{VFLD}.
4. Value holds for a theoretical capacitor value of C_{VFLD} = 20nF and is determined by $t_{FLD,0\text{-}DLY}$ + 0.2ms * C_{VFLD}/1nF, see also section 9.1.

20 TEST SETUP

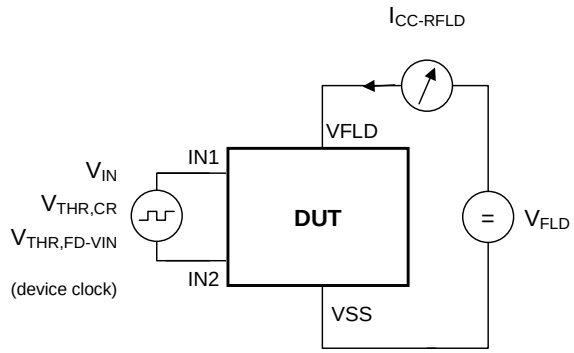


Figure 66. TRANSPONDER Mode measurement setup

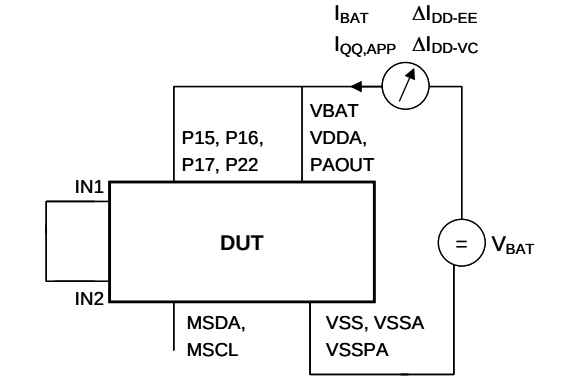


Figure 67. BATTERY Mode measurement setup

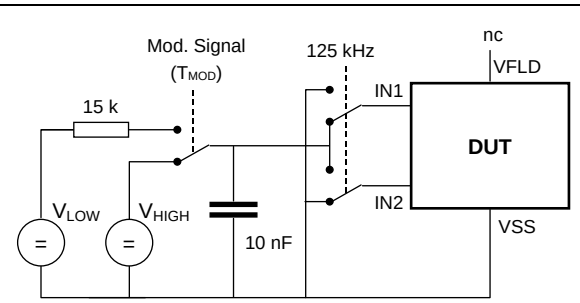


Figure 68. MI_{PROG} measurement setup

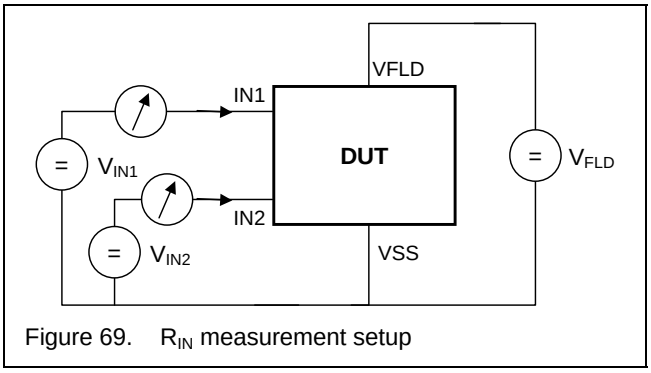


Figure 69. R_{IN} measurement setup

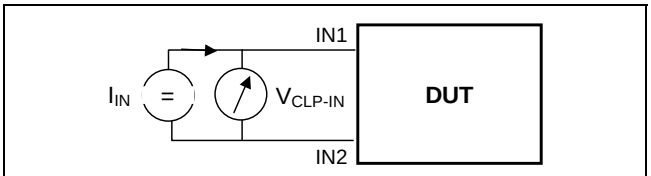
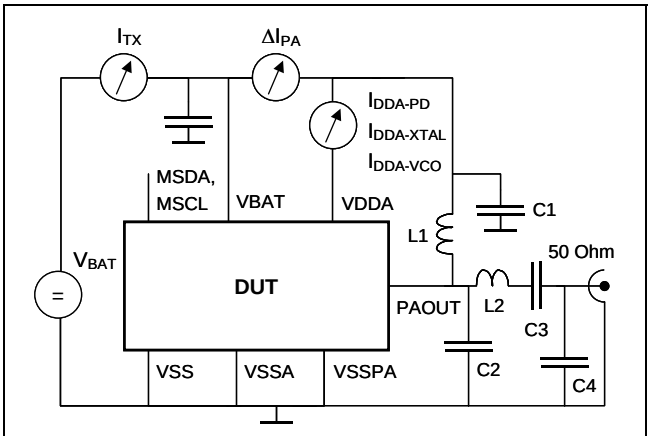


Figure 70. V_{CLP-IN} measurement setup



f_{TX}	315 MHz		434 MHz	
RL	≈ 200 Ω	≈ 700 Ω	≈ 200 Ω	≈ 700 Ω
L1	150n	150n	120n	120n
L2	33n	33n	22n	27n
C1	330p	330p	220p	220p
C2	8p2 + 1p5	6p8 + 1p5	6p8	2p2 + 2p2
C3	56 p	56 p	27p	27p
C4	18p + 1p	39p + 3p3	12p + 3p3	22p + 2p2

Figure 71. Power Amplifier measurement setup

21 ANOMALY NOTES

This section provides additional information concerning known anomalies discovered with the device and reports changes that are subject to implementation with future device versions.

21.1 Reading of UHF Transmitter is not supported with LF Field supply

Although the XTAL Oscillator is operational in TRANSPONDER Mode, hence may be supplied from the LF Field, reading from any of the UHF Transmitter control registers is not feasible. This holds for the registers XFCON, PACON, TXCON1 and TXCON2. However writing to these registers is supported.

Hence, microcontroller Read-Modify-Write commands must not be used to alter the register content, as the result would be undefined.

22 APPLICATION NOTES

This section provides additional information concerning device application and highlights differences in the device operation, when compared with the existing product family.

Additional information's are provided by the application note Software Development for PCF7X41ATS, that may be applied for the PCF7961X also (see section 23).

22.1 Selecting the capacitor C_{VFLD} properly

During transponder operation the rectified supply voltage must not drop below the power on reset threshold, as specified by $V_{POR,FLD}$. The LF Field strength, hence the inductive coupling factor and the value of C_{VFLD} are means to satisfy this condition, considering the device current consumption as specified. A typical system yields a capacitor C_{VFLD} of 15nF. Notice that the capacitor suffers an initial tolerance and a change of value over temperature, etc. Thus, a worst case figure of 10nF for C_{VFLD} has been considered for the electrical characteristics as specified in section 18 and 18.3.

22.2 Avoid leakage current in POWER-OFF mode

Some device ports (P15, P16 and P22) do not feature on-chip pull-up or pull-down and corresponding measures are required externally, when these ports are operated in input mode. Notice that all ports operate in input mode, while the device resides in POWER-OFF mode. Thus, pull-up or pull-down measures are required to avoid floating ports that would result in unwanted leakage currents draining the battery.

However, pull-down measures need to be considered carefully, as an accidental device wake up may occur, when the device is about to enter POWER-OFF mode, see 22.7.

22.3 LED output configuration

In case an LED is desired for visual user acknowledgment, an additional weak shunt resistor must be provided across the LED, in order to avoid unwanted leakage current draining the battery. Please notice the typical application diagram, see section 4.

Due to the given voltage drop across the LED, the LED cannot be considered to serve as a suitable pull-up for the corresponding port, while the port operates in input mode (e.g. during device POWER-OFF mode). A weak shunt resistor across the LED terminates the corresponding port properly.

22.4 Avoid device Lock-Up in INIT

The device INIT mode is the factory supplied default and used while developing software and during device personalization, in order to initialize the EEPROM content.

Consequently, the Monitor and Download Interface is operational in INIT mode and a low pulse on the MSDA pin would be treated as a breakpoint event. Consequently, the part will stop executing the application program, waiting for further debug commands. If no further commands are received, the part will idle forever, which in the user's perspective may be interpreted as a Lock-Up situation.

The device will idle until either a debug command is received or the battery is disconnected and applied again, causing the device to execute a power on reset and to terminate the debug mode.

The low pulse on the MSDA pin may origin from any kind of sources; an ESD pulse, EMC Noise or PCB cross talk.

To avoid unwanted device Lock-Ups during prototyping or in the field, the device shall be put into PROTECTED Mode once the EROM and EEPROM are initialized and device debugging is completed. In PROTECTED Mode the debug and breakpoint feature is disabled and any low pulses on MSDA pin will be ignored, causing the device to execute the application code as desired.

The device may be forced into PROTECTED mode and back into INIT mode again, by dedicated Monitor and Debugs commands, see section 12 and 15.

22.5 Entering POWER-OFF Mode

When entering the POWER-OFF mode, the application program must be aware of residual charge, which causes the device to continue program execution for a short time, before a Power On Reset condition applies and POWER-OFF mode is entered finally.

In order to cope with such situations, a sequence of instructions should be used as follows:

```
;Forces the device into POWER-OFF mode
;
     SETB  PLF
inf: JMP   inf   ;Consumes up residual charge
```

The first instruction clears the PMODE flip-flop and disconnects the battery from the internal supply (V_{DD}). The second instruction will be executed repeatedly, until the internal supply dropped below the power on reset threshold ($V_{POR,FLD}$) and the POWER-OFF mode is entered finally.

Note that a Port Wake Up condition may be present before (port high-to-low transition), but would not be detected and

ignored, until the power on reset condition applies, enabling the Supply Switch Logic again, see also section 8.1.

In case an LF Field is already present, before the sequence is executed, and this LF Field is sufficient to provide a supply voltage (V_{FLD}) that exceeds the power-on threshold ($V_{POR,FLD}$), then the POWER-OFF mode will not be entered at all and the device will idle in the endless loop sketched above (`inf: JMP inf`) as long as this field stays present.

If an LF Field is applied during execution of the endless loop, before the power-on reset condition has been reached, and this LF Field exceeds the LF Field Detect threshold ($V_{THR,FD}$), then an LF Wake Up condition applies. This either triggers a Device Reset or a Non Maskable Interrupt (NMI), as selected by the corresponding configuration bit (NMI), and enables the application program to take the proper action (e.g. invoke the TRANSPONDER emulation), see also section 8.4, 9.4 and 22.6.

Note, that a Port Interrupt is not recognized, unless the Interrupt System is configured accordingly before the endless loop is entered. The following alternate sequence of instructions tries to enter POWER-OFF mode, but accepts a Port Interrupt and generates a Reset in case:

```
;Forces the device into POWER-OFF mode and
;Port Interrupts are enabled
;
     SETB  EP
     SETB  PLF
     SETB  IDLE
     SETB  RST
```

In any case, please also be aware of an accidental device Wake Up, according to section 22.7.

22.6 Entering TRANSPONDER Mode

Entering TRANSPONDER mode from POWER-OFF mode is handled by the BOOT routine, whereas the application program needs to take action, when an LF Field is detected while operating in BATTERY Mode. In the latter case, the application program will be interrupted, as triggered by the LF Field Detection circuitry, see section 9.4.

According to the configuration of NMI, either a Device Reset or a Non Maskable Interrupt (NMI) is triggered. In case the Device Reset has been selected, the BOOT routine will handle invocation of the TRANSPONDER Mode.

In case the Non Maskable Interrupt has been selected, the corresponding interrupt is vectored and a user-defined sequence of instructions is executed, that shall serve to enter the TRANSPONDER Mode. However, note that the NMI will not be vectored as long as the device executes from system code e.g. any of the ROM Library functions. Instead, it is latched and vectored when program control is returned to the application code.

The TRANSPONDER Mode is entered, by triggering the control bit PLF (see also section 8.4), which shall be performed using the appropriate ROM Library functions (see also section 23). The corresponding ROM Library ensures that necessary timing constrains are satisfied.

If further control is not required by the application, setting the RST bit may also enter the TRANSPONDER mode. This triggers a device reset and starts the BOOT sequence, which will handle invocation of the TRANSPONDER Mode.

22.7 Avoid accidental device Wake Up

In case a pull-down like load is connected to any of the three port lines of P15, P16 or P22 and the device drives the corresponding port line HIGH before entering the POWER-OFF mode, an unintended device Wake Up condition may occur. Since the mentioned ports are forced into input mode, when entering POWER-OFF mode, a high-to-low transition will occur (e.g. eventually delayed due to capacitive load) that will trigger the corresponding Port Sense mono-flop. Similar, operating the ports in output mode and forcing a high-to-low transition triggers the mono-flop also. If the mono-flop is still in its "triggered" state, in the moment the Power On Reset condition applies, the device will instantly power-up again (see also section 8.3). Depending on the application program, this may initiate an endless loop.

To prevent the application from such situations, the following sequence of instructions is recommended, before the POWER-OFF mode is entered:

```
;Forces the device into POWER-OFF mode and
;avoids accidentally Wake Up
;
     CLR   P1DIR ;switch all ports to input
     CLR   P2DIR
     CALL  delay ;T = TPSMF + application delay
                 ;
     SETB  PLF   ;Disconnect battery
inf: JMP   inf   ;Wait for power-off
```

The above sequence forces all ports to input mode and waits for a certain time. The delay needs to exceed the Port Sense mono-flop duration (T_{PSMF}) plus the time the external circuitry needs to establish static conditions at the port lines. Finally, the POWER-OFF mode is invoked and an endless loop is entered to consume up remaining stored charge, see also 22.5.

22.8 Usage of control bit NMI

The control bit NMI provides means to either force a device reset or trigger the Non Maskable Interrupt upon detection of an LF Field. In case the control bit NMI is set, the Non Maskable Interrupt (INT 0) will be triggered and the corresponding interrupt service routine will be vectored. This feature is of great use to protect “critical” sections of the application program from being aborted by a device reset due to detection of an LF Field. The following example demonstrates this mechanism:

```
Using NMI to protect “critical” sections of
;the application program from being aborted
;due to the detection of an LF Field
;
int0:            ;INT0 service routine
                 ;Signals LF Field detected
                 ;using the flag fld_detected
     SETB  fld_detected
     RETI

     ;...
encapsulate_critical_section:
     CLRB  fld_detected
     SETB  NMI
     ; - start of critical section –
     ;...
     ; - end of critical section –
     CLRB  NMI
     SBC   fld_detected
     SETB  RST   ;Reset if LF Field detected
     ;...
```

The example postpones the generation of a device reset due to an LF Field Detection until the end of the critical section. The critical section(s) should be kept very short to minimize the transponder start-up delay, as recognized by the base station.

22.9 Device operating mode after battery power-up

In the moment of a battery power-up sequence, the device either enters POWER-OFF or BATTERY Mode. Thus, the application program cannot detect, if the battery has been changed or is inserted.

E.g. during battery power-up, the Port Sense Logic may signal a Port Wake-Up condition, because battery contact noise may trigger the corresponding port mono-flop or because the port input voltage develops slower than the device supply voltage at pin VBAT. Consequently, the Port Wake UP flip-flop is set and BATTERY Mode is entered. Depending on the contact noise duration, even the Port Interrupt may be triggered.

In any case, the application program shall poll the corresponding ports to verify the Wake Up condition and act as required.

22.10 Controlling the XTAL Oscillator Gain properly

For proper XTAL oscillator operation it is mandatory to control the XTAL Oscillator Gain correctly via the control bits OG (Register TXCON1, see section 12.4.1).

Prior to XTAL Oscillator start up it is mandatory to select the highest gain (9.84375Hz: OG = “01”), in order to establish the largest oscillation margin and ensure fast start up.

Once the XTAL Oscillator started, the Oscillator Gain need to be reduced accordingly, in case FSK modulation shall be applied.

22.11 System Test by monitoring internal clock signals

To ease system test the device features means to monitor the clock frequency of various internal signals, e.g. XTAL Clock, RC Oscillator and System Clock.

The mentioned clock signals can be output via Port 14 and P22, by invoking the corresponding ROM Library function (PLL_CLOCK_OUT, function code: 7Ah), see Table 52. The affected Port (P14, P22) must not be driven externally during this system test, in order to avoid a short circuit situation.

Table 52 Clock Monitor Selection

R3	Clock	Port	Comment
00h			Disabled
01h	T_{XTAL}	P22	XTAL clock
02h	T_{XDCLK}	P22	Divided XTAL clock
10h	T_{OSC}	P14	4 MHz RC clock
20h	T_{XDCLK}	P14	Divided XTAL clock
30h	T_{SYS}	P14	System clock

The monitor operation is maintained until it is disabled again or a Power On Reset is applied. The mentioned ROM Library function may be invoked as follows.

```
;Activate the Clock Monitor via Port P14/ P22
;Port Interrupts are enabled
;
     MOV   R4, #7AH
     MOV   R3, Clock_under_Test
     SYS
     ; - start Test
     ;...
     ;...
     ;...
     ; - end Test–
     MOV   R4, #7AH
     MOV   R3, #00H
     SYS
```

Note

1. The system call ADD_CLOCK_OUT (function code: 7AH) uses 4 byte of STACK and executes in 21 cycles. It does configure the Port P14 and P22 as required.

23 RELATED DOCUMENTS

Type	Name / Reference	Description
Data Sheet	MRK II Family	Architecture and Instruction Set
Data Sheet	HT3-Transponder-ROM	Implementation and Description
Data Sheet	HT3 Family ROM library (MRKII)	Implementation and Description
Data Sheet	PCF7961 Monitor and Download Interface	Functional Description
Data Sheet	PCF7938XA	Functional Description
Application Note	AN01034	Software Development for PCF7X41ATS (STARC 2XLite)

24 DEVELOPMENT TOOLS

Reference	Name	Description
OM6710	RIDE	Software development suite
OM6713	Universal Download and Debug Board (U-DDB)	Hardware and software Interface between host PC and target device
OM6714	EWMRKII IDE & C-Compiler	Embedded Workbench for MRKII Integrated Development Environment & C-Compiler
OM6715	2-LINK Debugger	Hardware and software Interface between host PC and target device. For use in combination with OM6714
OM6716	TED-Kit 2	Transponder Evaluation and Development Kit 2

25 REVISION HISTORY

Revision	Page	Description
2009 Nov 17		First release Preliminary Specification
2009 Dec 04		Editorial changes (Figure 19 and other) Correction QUICK REFERENCE DATA
2010 Sept 21		Editorial updates and changes Product Specification
2010 Dec 01		Editorial changes, update Legal Information
2011 Mar 31	7	Editorial changes. Add PCF7961XTT/C1AErrff.
2011 Aug 04	34	Removed misleading sentence.
2011 Sep 14	82	“Power Management “: Corrected MIN and MAX values.
2011 Nov 17	7 90	Updated ORDERING INFORMATION, added 8 k Version. Updated LEGAL INFORMATION.

26 LEGAL INFORMATION

26.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification or product development
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification
Product [short] data sheet	Production	This document contains the product specification

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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