NXP PJF7992 - PEPS low frequency chip introduction

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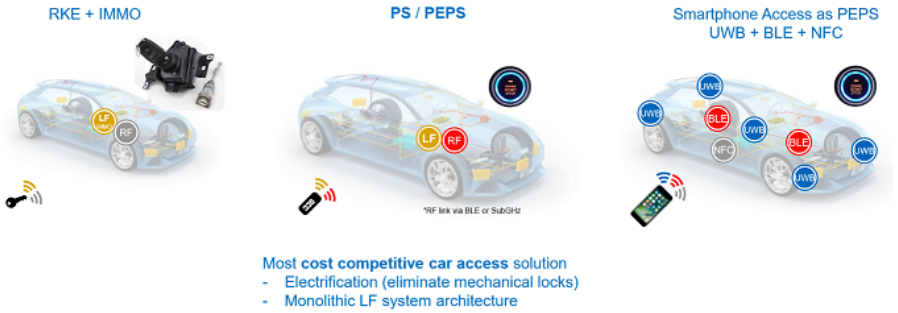
Category: PEPS Article Tags: Embedded Hardware

1. Overview

The PEPS system RF solution uses ultra-high frequency signals in the 434 MHz band combined with low frequencies in the 125 KHz band. Through the response interaction of the PEPS system, it realizes functions such as tire pressure monitoring, remote door locks, and one-button start.



II. Introduction

PJF7992 is a fully integrated base station IC second generation ABIC2 (Advanced Basestation IC 2) from NXP. The IC is designed to provide read and write access to transponders with a high degree of integration and a low number of external components.

The IC can be used with the NXP transponder series HT2, HT2-extended, HT3 and HT-Pro (PCF7xxx) and similar transponder types, operates at 125 kHz and supports FSK frequency modulation and ASK amplitude modulation.

As the second generation, the PJF7992 provides many enhanced features based on the PCF7991 ABIC, such as an on-chip voltage regulator, support for single-wire communication, integrated LIN transceiver and waveform shaping of the antenna drive signal. Specifically, the IC has a wide supply voltage range, allowing it to be supplied directly from the vehicle battery (12V), and does not require an external voltage regulator. An on-chip temperature sensor is provided to protect the device from overheating.

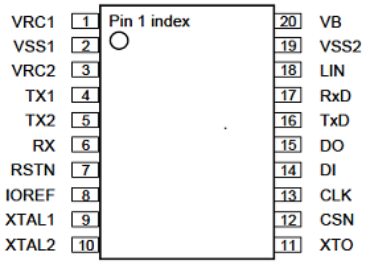
2.1 Features

- Integrated single-chip base station
- Integrated powerful programmable antenna driver/modulator
- Integrated LIN transceiver (physical layer compatible with 0 and SAE J2602, compatible with LIN1.3)
- Support single-line communication
- High-performance adaptive sampling time AM/PM demodulator
- On-chip clock oscillator and divider for external clock reference
- Antenna open and short circuit detection
- Low power consumption and ultra-low power standby mode

2.2 Application

The advancement of semiconductor technology has provided automobile manufacturers with intelligent, safer and more convenient automobile technology. PCF7991 is suitable for read and write operations and has a stable frequency. This chip is used as the RFID front-end circuit to successfully apply RFID electronic tag technology to automotive electronic locks, and electronic identity recognition is achieved through 125kHz wireless communication between the car and the key.

3. Introduction of main function pins



Pin Number	Symbol	Type	Characteristic	Description
1	VRC1	N.A.	Power out	Blocking capacitor for voltage regulator 1
2	VSS1	Ground	Power	Ground analog, antenna driver
3	VRC2	N.A.	Power out	Blocking capacitor for voltage regulator 2
4	TX1	Output	Push/pull or tristate	Antenna driver
5	TX2	Output	Push/pull or tristate	Antenna driver
6	RX	Input	Analog	Receiver
7	RSTN	Output	Open collector	RESET pin
8	IOREF	Supply	Power in	Interface mode switch / Supply for interface pins
9	XTAL1	Input	Analog	Oscillator interface, external clock reference input
10	XTAL2	N.A.	Analog	Oscillator interface
11	XTO	Output	Push/pull	Buffered XTAL clock output
12	CSN	Input	Digital	SPI: Chip-select
13	CLK	Input	Digital	SPI: Data-clock
14	DI	Input	Digital	SPI: Data-in
15	DO	Output	Open drain	SPI: Data-out
16	TxD	Input	Digital	LIN Transceiver Data-in (LOW for dominant, HIGH for recessive)
17	RxD	Output	Push/pull	LIN Transceiver Data-out (LOW when dominant, HIGH when recessive)
18	LIN	In / Out	Analog	LIN Transceiver Bus Line (LOW in dominant state) Capacitor for LIN slave node
19	VSS2	Ground	Power	Ground digital, LIN Transceiver
20	VB	Supply	Power in	Battery connection

4. PJF7992 Communication Introduction

4.1 Communication Mode Overview

PJF7992 can communicate with the device via SPI or single-wire mode, depending on the needs of the application. The device configuration utilizes a set of commands to control and modify the corresponding device registers.

The serial interface is configured as transparent or buffered transponder communication mode through commands, enabling read/write access to the transponder. In transparent mode, the data lines (LIN, DI, DO) are used to provide direct control of the antenna driver and direct access to the demodulated received signal, providing access to the demodulated received signal binary pulse length modulation (BPLM) encoder and Manchester decoder, sending and receiving transponder data in 8-bit blocks.

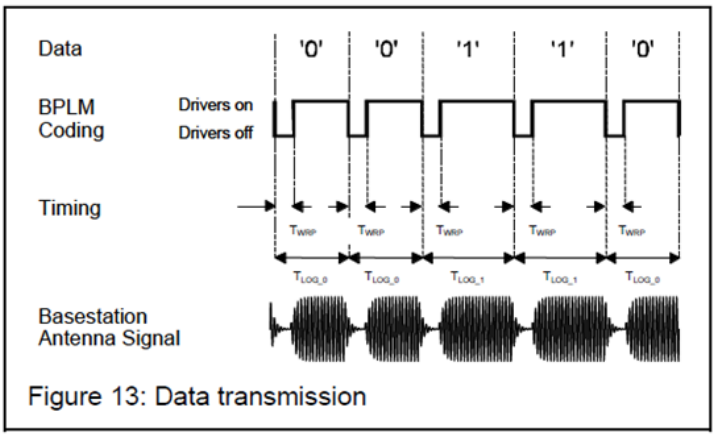


Figure 13: Data transmission

(Image source: "PJF7992A_DataSheet.pdf")

4.2 Communication Mode Selection

For architectures with embedded base stations, SPI operation is most suitable because it provides fast and direct access to the device. For architectures with remote base stations, single-wire mode is advantageous because it requires only three interconnect wires (VBAT, GND, and LIN) and has excellent signal-to-noise ratio characteristics for serial data communication.

Pin IOREF determines the operation mode of the serial interface, selecting SPI operation if the voltage level at IOREF exceeds a certain threshold (VIOREF, IMS). In this case, the voltage level at pin IOREF is also used to match the interface I/O voltage level specification with the power supply provided to the external microcontroller. In this case, the microcontroller and pin IOREF must be provided by an external voltage regulator (VIOREF). Otherwise, if pin IOREF is below a certain threshold (VIOREF, IMS), single-wire operation is selected.

4.2.1 SPI Communication Mode

The SPI communication mode is achieved by setting the value of VIOREF greater than VIOREF. In this mode, the interface operates synchronously during command reception and response, using dedicated data input DI, data output DO and data clock, CLK lines.

Applications with multiple slave devices provide Chip Select to wake up the device from SLEEP mode, while in single-slave applications, the chip select pin CSN cannot be set to ground because additional functions such as wake-up, initialization, and transparent communication control are required.

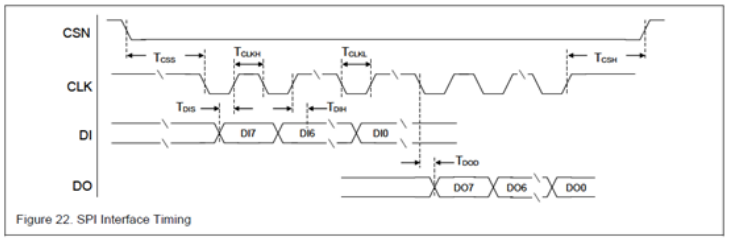


Figure 22. SPI Interface Timing

4.2.2 Single-wire communication mode

By setting VIOREF to less than VIOREF, in this mode, the data input and data output share the same line, the interface operates asynchronously, and a dedicated data clock line is avoided. Instead, the data clock is derived from the system clock.

In the transparent communication process with the transponder, the actual data rate is irrelevant, the timing is determined by the transponder protocol, and the single-wire mode uses the on-chip LIN transceiver to communicate with the device remotely. No external microcontroller is required, the LIN transceiver is controlled by an internal state machine, and the CSN, DI, and CLK pins have no function so they can be grounded.

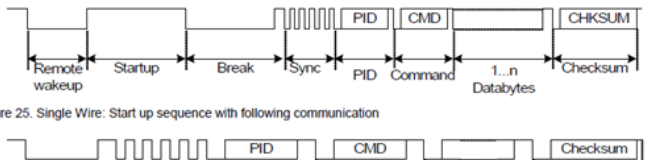


Figure 25. Single Wire: Start up sequence with following communication

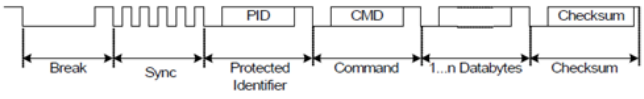


Figure 26. Single Wire: standard communication sequence