NXP PCF7991 - PEPS low frequency chip introduction

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Preface

NXP PCF7991 is a very old chip. It is currently used in farm tags and low-end low-frequency keyless entry PSPS (Passive Entry Passive Start) systems. Next, the communication commands and communication timing between MCU and PCF7991 are introduced.

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1. Basic Introduction

1. Overview

The PCF7991AT is a fully integrated Advanced Basestation IC (ABIC) designed for automotive engine immobilizer systems, providing read and write access to ID transponders. The device is designed to work with transponders operating at 125kHz and using ASK write and AM/PM read operations, and can be optimized according to system and transponder requirements for amplifier gain, filter cutoff frequency, etc.

Italic Style The PCF7991AT is designed for easy integration into the read-write or read-only system of the engine immobilizer, featuring high integration and very few external components. The device integrates a powerful antenna driver/modulator, low noise adaptive sampling time demodulator, programmable filter/ amplifier and digital converter, suitable for base stations that need to design high performance with the transponder . The PCF7991AT can communicate bidirectionally , and the three-wire interface can be configured as a two-wire interface operation by connecting DIN and DOUT.

2. Features and applications

2.1 Features

- Fully integrated single-chip base station
- Integrated powerful programmable antenna driver/modulator
- On-chip clock oscillator and divider for external clock reference
- Antenna open circuit and short circuit detection
- Low power consumption and ultra-low power standby mode
- Few external components and small package

2.2 Application

The advancement of semiconductor technology has provided automobile manufacturers with intelligent, safer and more convenient automobile technology. PCF7991 is suitable for read and write operations and has a stable frequency. This chip is used as the RFID front-end circuit to successfully apply RFID electronic tag technology to automobile electronic locks, and electronic identity recognition is achieved through 125kHz wireless communication between the car and the key.

3. Introduction of main function pins

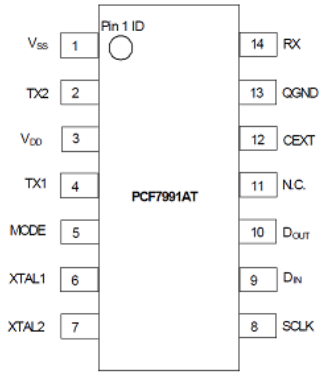
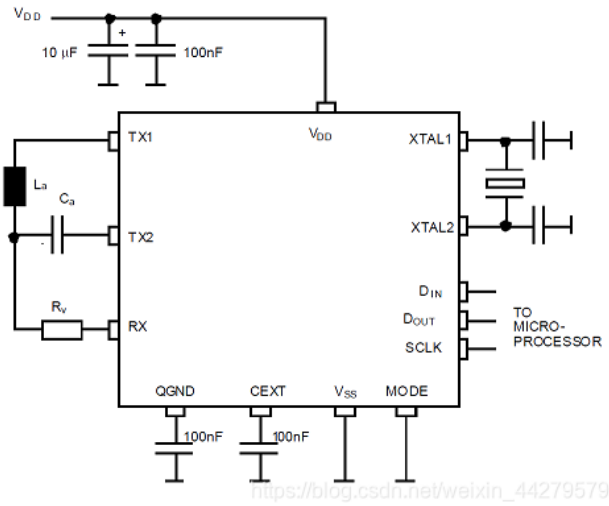


Table 1 Pin Description for PCF7991AT

SYMBOL	PIN	DESCRIPTION
V_{CC}	1	Common ground GND
TX2	2	Antenna driver output
V_{DD}	3	Supply voltage input, stabilized
TX1	4	Antenna driver output
MODE	5	Microcontroller interface mode select
XTAL1	6	Oscillator interface external clock reference input
XTAL2	7	Oscillator interface
SCLK	8	Microcontroller interface: serial clock input
DIN	9	Microcontroller interface: serial data in
DOUT	10	Microcontroller interface: serial data out
NC	11	Not connected
CEXT	12	High pass filter decoupling
QGND	13	Analog ground bias
RX	14	Receiver input

3. Minimum application circuit



The figure shows the minimum application circuit of PCF7991AT. The antenna coil La and capacitor Ca form a series resonant LC circuit (f = 125kHz). The capacitors at QGND and CEXT provide internal bias and decoupling for the device.

2. PCF7991AT Communication

1. PCF7991AT Communication Overview

The communication between PCF7991AT and MCU is done by a three-wire digital interface. This interface is used in transparent mode (READ_TAG, WRITE_TAG / WRITE_TAG_N) to read and write the configuration data of the device.
Before sending commands, the PCF7991AT needs to initialize the serial interface to communicate with the MCU. The initialization condition is: when SCLK is high, the DIN signal needs to jump from low to high.
All commands transmitted to the PCF7991AT serial interface are transmitted starting with the most significant bit. When SCLK is in the high state, DIN is latched and DOUT is valid.
The digital filter samples the SCLK and DIN inputs at a rate of 1/fTX (8 µs typical). DIN input state changes are delayed by 16 to 24 µs until they are recognized by the internal circuitry.

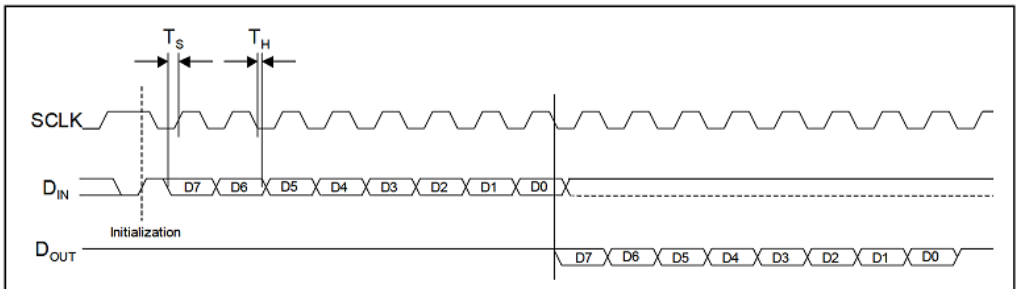


Figure 4. Serial Interface Timing

2. PCF7991AT communication sending command set

9 COMMAND SET

Table 2 Command set summary

COMMAND NAME	MSB				BIT NO.			LSB	RESPONSE
	7	6	5	4	3	2	1	0	
GET_SAMPLING_TIME	0	0	0	0	0	0	1	0	8 bit (0 0 D5-D0)
GET_CONFIG_PAGE	0	0	0	0	0	1	P1	P0	8 bit (X3 X2 X1 X0 D3-D0)
READ_PHASE	0	0	0	0	1	0	0	0	8 bit (0 0 D5 - D0)
READ_TAG	1	1	1	-	-	-	-	-	enter READ_TAG-mode
WRITE_TAG_N	0	0		1	N3	N2	N1	N0	enter WRITE_TAG-mode with pulse width programming
WRITE_TAG	1	1	0	-	-	-	-	-	enter WRITE_TAG-mode
SET_CONFIG_PAGE	0	1	P1	P0	D3	D2	D1	D0	4 bit per config page addressed
SET_SAMPLING_TIME	1	0	D5	D4	D3	D2	D1	D0	8 bit (00 D5 - D0)

2.1 GET_SAMPLING_TIME command

This command is used to read back the setting of sampling time TS.

2.2 GET_CONFIG_PAGE command

This command is used to read back the parameter set configured in PAGE 0, PAGE 1, PAGE 2, PAGE 3, and read back the programmed transmitter pulse width.

2.3 READ_PHASE command

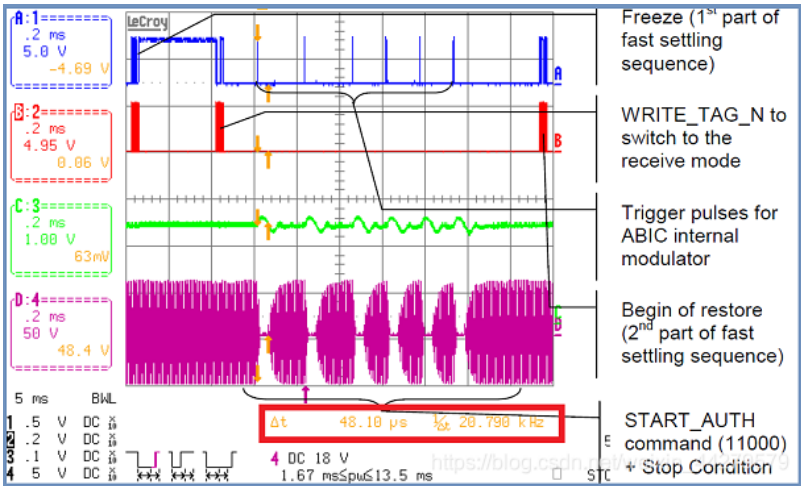
This command is used to read the antenna phase TANT (binary bit0 ~ bit5), which is measured in each carrier cycle.

2.4 READ_PHASE command

This command is used to read the demodulated bit stream from the transponder. After the three command bits are asserted, the PCF7991 immediately switches to READ_TAG mode, which is terminated by a low-to-high transition of SCLK.

2.5 WRITE_TAG_N command

This command is used to write data to the transponder and set the parameters of modulator blanking.
A high level on DIN is equivalent to the antenna driver being turned off, and a low level is equivalent to the antenna driver being turned on.
If N3-N0 is set to 0, the signal on DIN will be switched to the driver in a transparent manner. If N3-N0 is set to 1 to 1111, the time interval for the driver to be turned off is equal to N * T0 (T0 = 8 μs)
The WRITE_TAG mode is terminated by a low-to-high transition of SCLK, so the drivers will restart to their initial state regardless of the activation state of the modulation pulse timer.



2.6 WRITE_TAG Command

This is a simple 3-bit format for the WRITE_TAG_N command. It allows switching to WRITE_TAG mode with minimal communication time.
WRITE_TAG mode is also terminated by a low-to-high transition of SCLK, so the drivers will restart their initial state regardless of the activation state of the modulation pulse timer.

2.7 SET_SAMPLING_TIME command

This command specifies the sampling time TS of the modulator. The sampling time is coded in binary.

2.8 SET_CONFIG_PAGE command

Table 9 SET_CONFIG_PAGE command sequence

BIT NO.	7	6	5	4	3	2	1	0	REMARK
Command	0	1	P1	P0	D3	D2	D1	D0	no response

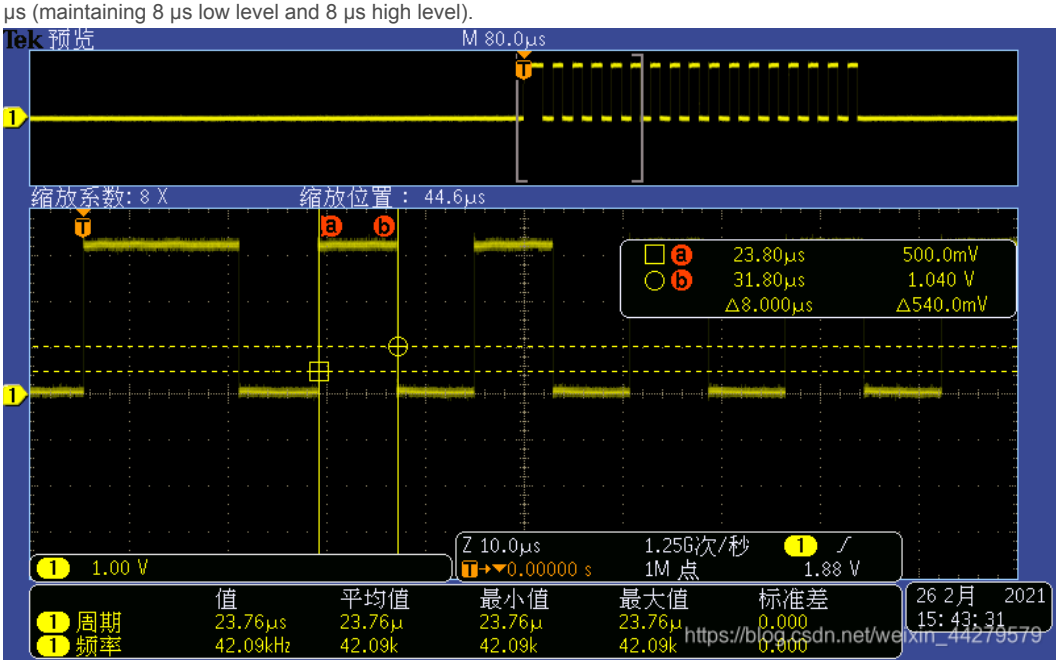
Table 10 SET_CONFIG_PAGE mapping

BIT NO. COMMAND/PAGE NO.	P1	P0	D3	D2	D1	D0
SET_CONFIG_PAGE 0	0	0	GAIN1	GAIN0	FILTERH	FILTERL
SET_CONFIG_PAGE 1	0	1	PD_MODE	PD	HYSTERESIS	TXDIS
SET_CONFIG_PAGE 2	1	0	THRESET	ACQAMP	FREEZE1	FREEZE0
SET_CONFIG_PAGE 3	1	1	DISLP1	DISSMART COMP	FSEL1	FSEL0

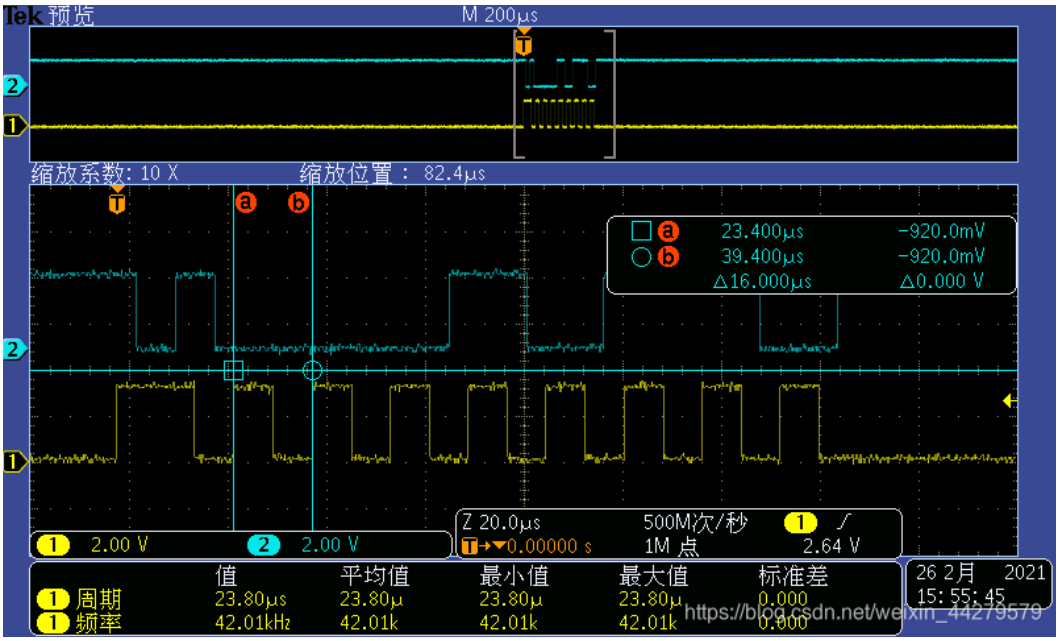
位名称	描述	复位值	参数
FILTERL	带通滤波	0	0: fL = 3 kHz; 1: fL = 6 kHz
FILTERH		0	0: fH = 40 Hz; 1: fH = 160 Hz
GAIN0	增益放大	0	0: gain0 = 16; 1: gain0 = 32
GAIN1		1	0: gain1 = 6.22; 1: gain1 = 31.5
TXDIS	失能天线驱动	0	0: driver active; 1: driver inactive
HYSTERESIS	数据滞后比较器	0	0: hysteresis OFF; 1: hysteresis ON
PD	使能掉电	0	0: device active; 1: Power-down mode
PD_MODE	掉电模式	0	0: Idle mode; 1: Power-down mode
FREEZE0	接收器参数表覆盖	0	为了快速接收，设置放大器和滤波器参数表可以暂时被覆盖
FREEZE1		0	
ACQAMP	存储信号的振幅	0	放大器比较结果
THRESET	数字转化器复位阈值	0	如果 THRESET 被设置，阈值发生器被禁止，并且按接收信号条件初始化。
FSEL0 FSEL1	晶振频率同步硬件	0 0	0 0：4MHz 0 0：8MHz 0 0：12MHz 0 0：16MHz
DISSMARTCOMP	失能智能比较器	0	0: comparator = ON, 1: comparator = OFF
DISLP1	禁止主低通	0	0: low pass = ON, 1: low pass = OFF

3. PCF7991AT communication debugging

1. Serial port communication and timing are simulated through IO port and delay. After the initialization condition SCLK is pulled high and maintained at a high level, DIN is pulled low from a high level and then starts to jump from a low level to a high level. The stable period of SCLK is 16 μs (maintaining 8 μs low level and 8 μs high level).



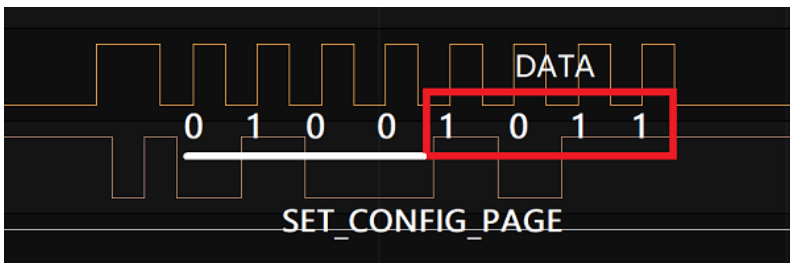
2. SCLK is sampled by the rising edge, and the first edge is held after initialization to maintain the high level. Data is sent by changing the DIN level + a delay + SCLK jumps from low to high level to collect DIN data + a delay + an empty instruction + a delay + SCLK jumps from high to low level + a delay and so on.



3. Reading response also obtains response data by periodically reading the level of DOUT IO port through SCLK. Write data to PAGE 0 through SET_CONFIG_PAGE command, and read the data written to PAGE 0 through GET_CONFIG_PAGE command. Verify the communication is successful through comparison, and write the data to PCF7991.
   SET_CONFIG_PAGE command writes D3 D2 D1 D0:

Table 9 SET_CONFIG_PAGE command sequence

BIT NO.	7	6	5	4	3	2	1	0	REMARK
Command	0	1	P1	P0	D3	D2	D1	D0	no response



GET_CONFIG_PAGE command reads D3 D2 D1 D0:

Table 8 GET_SAMPLING_TIME command sequence

BIT NO.	7	6	5	4	3	2	1	0	REMARK
Command	0	0	0	0	0	0	1	0	
Response	0	0	D5	D4	D3	D2	D1	D0