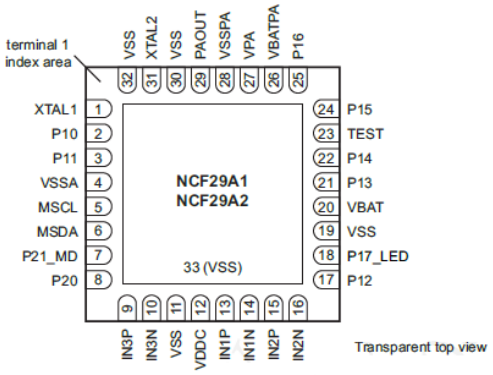
NXP NCF29A1 - PEPS Key Chip Timer Introduction

1. Introduction to NCF29A1

NCF29A1 /NCF29A2 is a very compact single chip solution, ideal for automotive applications, the chip features vehicle IMMO and keyless entry/start. The chip integrates a security transponder, supports multi-channel EEPROM access, and provides up to 2048 bytes of EEPROM for data storage for application-defined access control. The UHF transmitter does not require external components, except for the reference crystal and loop antenna matching circuit. The device operates in the 310-447MHz band. The 868 MHz and 915 MHz bands can be supported upon request. The UHF transmitter is directly controlled by a RISC controller and supports carrier FSK, ASK, OOK modulation with rising data rates. The device has 10 I/O ports, allowing up to 10 command button inputs, and the on-chip hardware calculation unit or any user-defined software based algorithm can be used for data communication.



2. Timer/Counter 0, 1, 2

Timer 0 and Timer 2 are the same, but unlike Timer 0/2, Timer 1 is an 8/16-bit timer with a 12-bit frequency divider. The following description uses Timer 0 as T0 and Timer 2 as T2. T0/T2 is a 16-bit timer with a 12-bit frequency divider. Clock Source RCCLK, 16 MHz RC Main Oscillator Clock The 16 MHz main RC oscillator is the main clock source for high-speed CPU and peripheral operations.

1、Timer/Counter 0，2

T0/T2 is a 16-bit timer with 12-bit frequency division, which can be used as an interval, event counter, digital modulator or clock divider. If timer 0/2 reaches the value of 0, an interrupt will be generated, which can be set and cleared. The output of timer 0/2 can be used to provide a divided clock output at the I/O port. The timer can restart timing by loading the reload value from register TxRLD into register TxREG, and then automatically count down. When the timer register TxREG value is 0, the timer register TxREG is reloaded with the value of the reload register TxRLD, generating an interrupt request and triggering other peripheral functions.

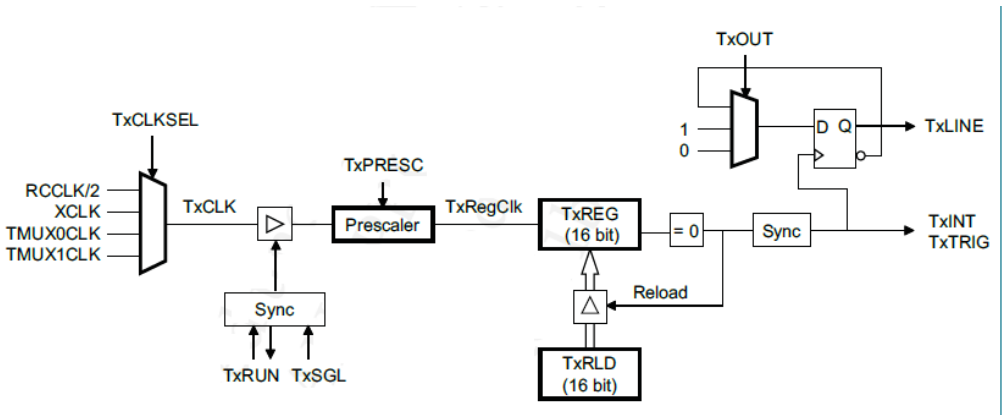


Fig 54. Block diagram of Timer 0/2

2、Timer/Counter 1

Unlike Timer 0/2, Timer 1 is an 8/16-bit timer and 12-bit frequency divider that can be used for general purpose applications or as a time interval and event counter, demodulator or signal generator and modulator.

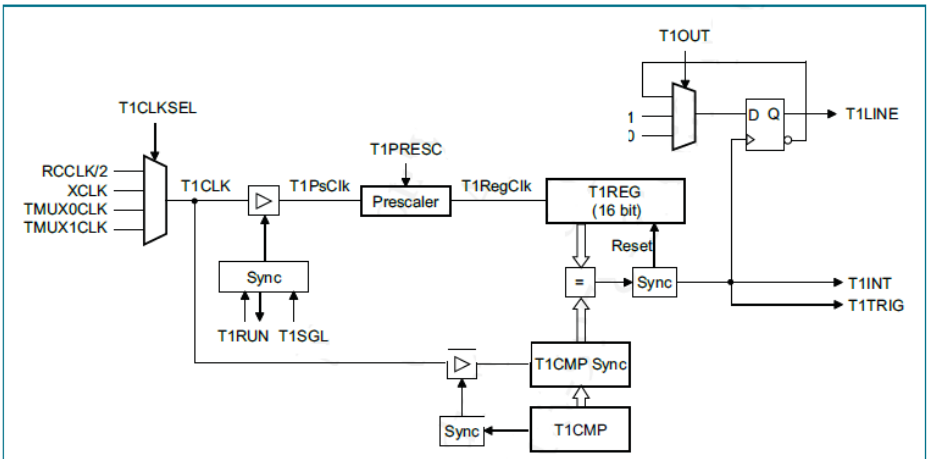


Fig 55. Block diagram of Timer 1 configured in Mode 0 and 1

Timer 1 has four operating modes:

Mode 0:

In Mode 0 Timer 1 is a synchronous 16-bit timer with a 12-bit prescaler, providing a 16-bit compare and 16-bit capture register. The timer is operated continuously in auto-reload mode.

Mode 1:

Mode 1 has the same properties as Mode 0, except that the timer will automatically stop on the first compare match. If the TIRSTCMP bit is set, the timer register is cleared when the timer stops.

Mode 2:

In Mode 2, Timer 1 operates as an 8-bit timer with a 12-bit divider, providing two 8-bit compares and two 8-bit capture resistors. The purpose of Mode 2 is to generate flexible PWM signals.
The 8-bit timer registers T1REGL and T1REGH run in parallel. It is recommended to clear the timer registers before starting to ensure that both timer registers contain the same value.

Mode 3:

As in Mode 2, in Mode 3, Timer 1 operates as an 8-bit timer with a 12-bit prescaler and also provides two 8-bit compare and two 8-bit capture registers.

3. Timer 1 Register

Table 6. Device register set

Peripheral	Register name[1]	Address	Description	Supply domain
Timer 1 [2]	T1REG	009Eh	Timer 1 register	VDD
	T1CON0	009Ah	Timer 1 control register 0	
	T1CON1	009Bh	Timer 1 control register 1	
	T1CON2	009Ch	Timer 1 control register 2	
	T1CMP	00A2h	Timer 1 compare register	
	T1CAP	00A0h	Timer 1 capture register	

T1REG :

Timer 1 supports read access to the timer registers. The contents of the timer registers are not buffered or synchronized, so it is recommended that T1REG be read only when the timer is stopped (T1RUN = 0). Reading T1REG while the timer is running can produce unstable and erroneous values because the timer value is not necessarily determined when read.

T1CON 0 :

Timer 1 Control Register 0 holds the control bits to adjust the timer mode and output lines, and also provides bits to configure reset and run conditions.

T1CON1 :

Timer 1 Control Register 1 stores the selected divider value T1PRESC[3:0] and the clock source used T1CLKSEL[1:0].

T1CON2 :

Timer 1 Control Register 2 holds the control bits to adjust the capture function.

T1CMP :

The compare register T1CMP is used to set the timeout period of Timer 1.

T1CAP :

Timer 1 capture register T1CAP automatically loads the contents of the timer register. It can only be read when the contents are stable. It does not support write operations on T1CAP.