DATA SHEET

PJF7992A

Advanced Basestation IC 2nd Gen. (ABIC 2)

Product Specification

2007 Nov 29

Confidential

CONTENTS

1 FEATURES

- Fully integrated single chip basestation
- High performance adaptive sampling time AM/PM demodulator
- Programmable modulator/demodulator characteristics
- Antenna driver with wave shaping for improved spectral purity
- Adjustable antenna excitation voltage
- Antenna rupture and short circuit diagnostic
- Serial interface feature SPI and single wire operation
- LIN Transceiver (Physical layer compliant with LIN 2.0 and SAE J2602 and compatible with LIN 1.3) for single wire operation
- Limited LIN 2.0 protocol capabilities
- On-chip XTAL oscillator and clock divider in the case of external clock reference
- Buffered XTAL oscillator output
- Power On Reset function
- Programmable Watchdog (timeout 4.1s / 10 ms)
- Low power consumption
- Temperature Sensor and device protection
- Wide supply voltage range from 6V to 27V
- Low external component count
- Heatsink TSSO Package HTSSOP 20

IMPORTANT NOTE:

The on-chip oscillator of the PJF7992A is suitable for ceramic resonators only. Crystals shall not be used.

2 GENERAL DESCRIPTION

The PJF7992A is a fully integrated Advanced Basestation IC 2nd generation, ABIC 2, designed for car immobilizer systems providing read and write access to an identification transponder. The device is intended for use with the NXP transponder family (PCF7xxx) as well as similar transponder types operating at 125 kHz and employing Amplitude Shift Keying, ASK.

The PJF7992A offers a number of enhancements over the PCF7991, like on-chip voltage regulator, single wire communication, integrated LIN Transceiver and wave shaping of the antenna drive signal.

In detail, the device features a wide supply voltage range allowing supply the device directly from a 12V, making an external voltage regulator unnecessary. An on-chip temperature sensor is provided to protect the device from overheating.

Bi-directional communication with the device utilizes a serial interface that operates in SPI or single wire mode, according to the application needs. In case of a single wire operation, a corresponding bi-directional transceiver is provided that features a LIN compliant Physical Layer specification.

An external microcontroller may be added to implement a customer desired protocol layer (like LIN 2.0). The microcontroller supply needs to be provided by further measures, e.g. by an additional voltage regulator.

For improved spectral purity of the antenna drive signal, wave shaping is provided.

Like for the PCF7991, the PJF7992A receiver characteristics (amplifier gain) are programmable according to system and transponder requirements. The device utilizes the proven concept of adaptive sampling time demodulation. Typically, the device timing is derived from a ceramic (crystals not allowed) controlled on-chip oscillator or may be derived from an external source.

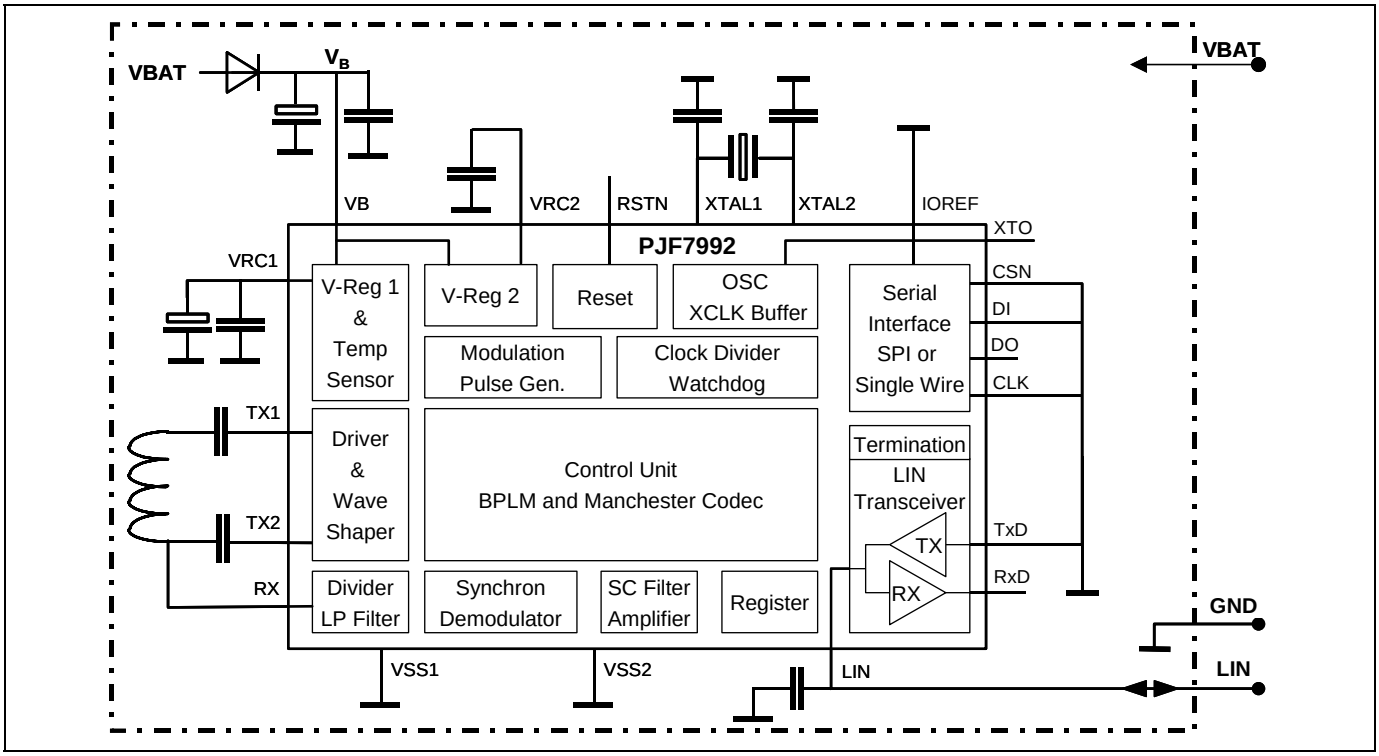
The PJF7992A IC is designed for easy integration into immobilizer read/write and read-only systems featuring a high degree of integration and very low external component count.

3 ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			TEMPERATURE RANGE (°C)
	NAME	DESCRIPTION	OUTLINE VERSION	
PJF7992ATW/B2B	HTSSOP20	Plastic thermal enhanced thin shrink small outline package, 20 pin	SOT527-1	-40°C to +85°C

4 TYPICAL APPLICATION

a) Single wire application with internal implemented protocol



b) SPI or LIN application with microcontroller implemented protocol stack

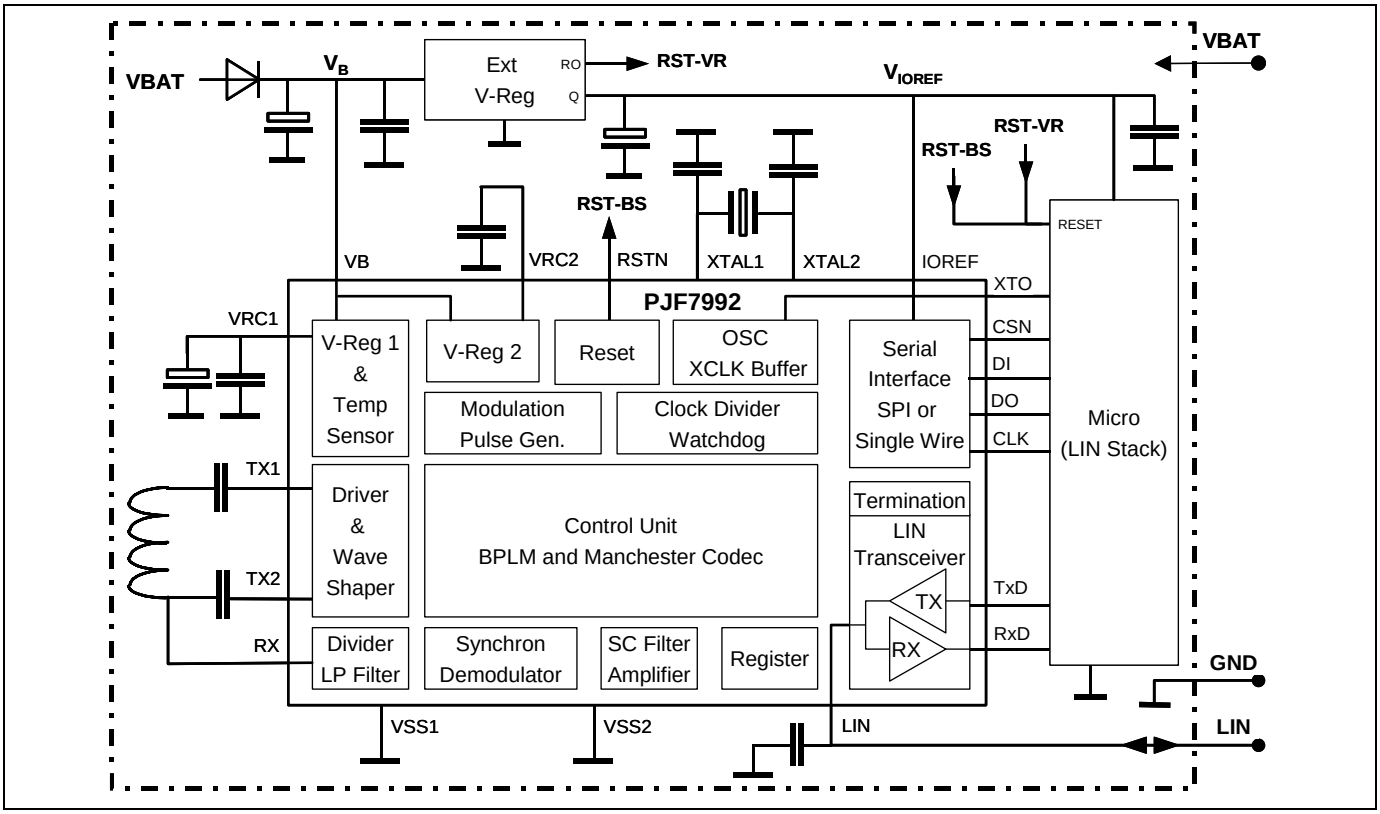


Figure 1. Typical Application

5 PINNING

Table 1 Pin Assignment

Pin Number	Symbol	Type	Description	Note
1	VRC1	N.A.	Blocking capacitor for voltage regulator 1	C typ:22µF || 100nF
2	VSS1	Ground	Ground analog, antenna driver	
3	VRC2	N.A.	Blocking capacitor for voltage regulator 2	C typ:220nF
4	TX1	Output	Antenna driver	
5	TX2	Output	Antenna driver	
6	RX	Input	Receiver	
7	RSTN	Output	RESET pin (open collector)	Note 1
8	IOREF	Supply	Interface mode switch / Supply for interface pins	Note 2
9	XTAL1	Input	Oscillator interface, external clock reference input	
10	XTAL2	Output	Oscillator interface	
11	XTO	Output	Buffered XTAL clock output	Note 1
12	CSN	Input	SPI: Chip-select	Note 3
13	CLK	Input	SPI: Data-clock	Note 3
14	DI	Input	SPI: Data-in	Note 3
15	DO	Output	SPI: Data-out (open drain)	Note 1
16	TxD	Input	LIN Transceiver Data-in (LOW for dominant, HIGH for recessive)	Note 3
17	RxD	Output	LIN Transceiver Data-out (LOW when dominant, HIGH when recessive)	Note 1
18	LIN	In / Out	LIN Transceiver Bus Line (LOW in dominant state) Capacitor for LIN slave node	Note 4 C typ 220 pF
19	VSS2	Ground	Ground digital, LIN Transceiver	
20	VB	Supply	Battery connection	

Note 1: Do not connect in Single-wire mode or if pin is not used (digital output)

Note 2: Connect to GND in Single-wire mode, connect to 5V / 3.3V external supply in SPI-mode, blocking capacitor is recommended

Note 3: Connect to GND in Single-wire mode or if pin is not used (digital input)

Note 4: Do not connect to GND or VBAT in any mode (internal pull-up, wakeup functionality)

The exposed die pad at the bottom of the package allows better dissipation of heat from the PJF7992A via the printed circuit board. The exposed die pad shall be connected to Ground for best EMC performance.

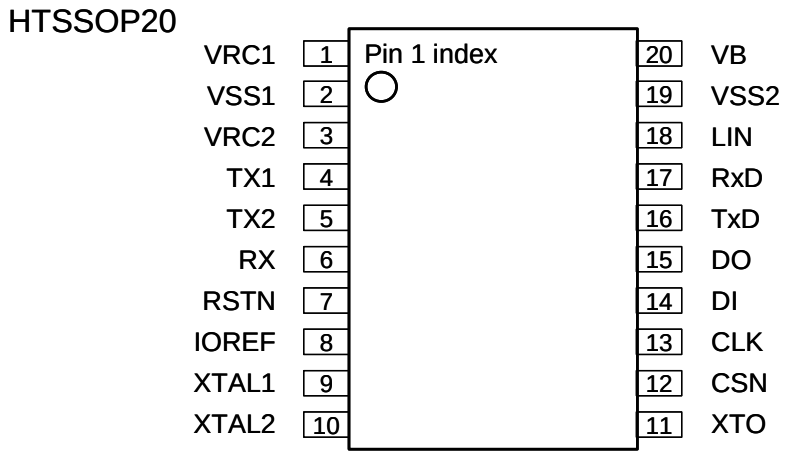


Figure 2. Pin Configuration

6 FUNCTIONAL DESCRIPTION

6.1 Voltage Regulator 1

The V-Reg 1 provides the supply voltage for the antenna driver, featuring low drop-out and a wide input supply voltage range V_B. An external capacitor C_{VRC1} is required for blocking and stability reasons (VRC1). Supply of external circuitry by this voltage regulator is not supported.

The V-Reg 1 features an adjustable (register DRVCON) output voltage V_{VRC1}. The ripple rejection of V-Reg 1 ensures good LF reception characteristics in case of noisy battery supply conditions.

Note: Any noise, ripple and disturbances induced to the VRC1 may decrease system performance and reliability.

6.2 Voltage Regulator 2

The V-Reg 2 provides the supply voltage for the LF receiver block except for the antenna driver, featuring low drop-out and a wide input supply voltage range V_B. An external capacitor C_{VRC2} is required for blocking and stability reasons (VRC2). Supply of external circuitry by this voltage regulator is not supported.

Note: Any noise, ripple and disturbances induced to the VRC2 may decrease system performance and reliability.

6.3 Device Register Set

The Device Register Set comprises of configuration, status and control bits that serve to operate the device and to communicate with a Transponder in range (Table 2).

Table 2 Device Register Set

NAME	DESCRIPTION	ADDR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	RESET VALUE
DCON0	Device Control 0	00_H	RFU	DISXTO	RST	RFU	WDMD	OSCDIS	FSEL_1	FSEL_0	**X000X011B**
DCON1	Device Control 1	01_H	SLP	ACT	POR	TSHUT	WDOV	SWRES	SWFRM	SWCS	**001X0000B**
LINCFG	LIN Transceiver CFG	02_H	RFU	RFU	RFU	RFU	TXON	TXSS	ISLPON	RTON	**XXXX0010B**
RCON0	Receiver Control 0	03_H	RFU	HYST	RNG1	RNG0	GAIN1	GAIN0	RFU	RFU	**00110000B**
RCON1	Receiver Control 1	04_H	RXCHK	RXL	DRX	SWHP2	HPDIS	LPDIS	FRZ1	FRZ0	**00010000B**
PHMEAS	Phase Measurement	05_H	RFU	RFU	MPH_5	MPH_4	MPH_3	MPH_2	MPH_1	MPH_0	**XX111100B**
SMPLC	Sampling Control	06_H	RFU	RFU	ST_5	ST_4	ST_3	ST_2	ST_1	ST_0	**XX000000B**
TXCON	Transmitter Control	07_H	EPD_3	EPD_2	EPD_1	EPD_0	PTX2	TRIS	ETX2	ETX1	**00000111B**
DRVCON	Drive Voltage Control	08_H	THR	FAIL	CHK	RFU	AVR_3	AVR_2	AVR_1	AVR_0	**00001111B**
COMCON	Communication Control 0	09_H	RFU	MDPOL	RFU	MODE	MPW3	MPW2	MPW1	MPW0	**X0X00111B**
STATUS	Status	$0A_H$	STAT	BFP_2	BFP_1	BFP_0	BFLB	BFPR	RDY	DREQ	**00000000B**
BCDAT	Buffered Com. Data	$0B_H$	BCD_7	BCD_6	BCD_5	BCD_4	BCD_3	BCD_2	BCD_1	BCD_0	**00000000B**
CHKSUM	Checksum Result	$0C_H$	CHK_7	CHK_6	CHK_5	CHK_4	CHK_3	CHK_2	CHK_1	CHK_0	**00000000B**
TEST0	Test Register 0	$0D_H$									**XXXXXXXXB**
TEST1	Test Register 1	$0E_H$									**XXXXXXXXB**
TEST2	Test Register 2	$0F_H$									**XXXXXXXXB**

Note

- The specified reset values refer to the different reset conditions of each bit (see bit description in table 3 for further information).
- Write access to registers DCON0, DCON1 and LINCFG is possible by WR_SCFG command only.
- Access to LINCFG bits (TXON, TXSS, ISLPON, RTON) only possible in SPI mode. In single wire mode the bits are controlled by the interface control unit.

RFU: Reserved for future use, these bits have to be set to 0 at any write-access.

Table 3 Bit overview

Register	Bit	Function	Access	Reset Cond.	Reset Value
DCON0	FSEL[1:0]	Clock frequency selection	Random	P	11
	OSCDIS	Disable XTAL oscillator driver	Random	P/S/R	0
	WDMD	Watchdog timeout mode (0/1 = T_{WTD_0} / $T_{SLP,DLY}$)	Random	P/S/R	0
	RST	Software reset (effect see reset conditions)	Random	P	0
	DISXTO	Disable XTO driver	Random	P/S/R	0
DCON1	SWCS	Single wire checksum error.	Read / Clear	P/S/R	0
	SWFRM	Single wire frame error.	Read / Clear	P/S/R	0
	SWRES	Single wire response error.	Read / Clear	P/S/R	0
	TSHUT	Temperature shutdown status flag	Read / Clear	P/S/R	0
	WDOV	Watchdog overflow status bit.	Read / Clear	P	0
	POR	Power on reset status bit (set after a POR)	Read / Clear	P	1
	ACT	Enable device active mode	Random	P/S/R	0
	SLP	Enable device sleep mode	Random	N.A.	0
LINCFG	RTON	LIN transceiver termination switch on/off (1/0)	Random	P/S/R	0
	ISLPON	LIN transceiver low power termination on/off (1/0)	Random	P/S/R	1
	TXSS	LIN transceiver transmitter slope select (For low slope mode the bit has to be set to 0.)	Random	P/S/R	0
	TXON	LIN transceiver transmitter power on/off (1/0)	Random	P/S/R	0
RCON0	GAIN0	Receiver gain setting bit0	Random	P	0
	GAIN1	Receiver gain setting bit1	Random	P	0
	RNG0	Receiver voltage range setting bit0	Random	P	1
	RNG1	Receiver voltage range setting bit1	Random	P	1
	HYST	Enable receiver demodulator hysteresis	Random	P	0
RCON1	FRZ0	Receiver freeze control bit0	Random	P/S/R	0
	FRZ1	Receiver freeze control bit1	Random	P/S/R	0
	LPDIS	Receiver low pass filter disable	Random	P	0
	HPDIS	Receiver high pass filter disable	Random	P	0
	SWHP2	Switch second high pass stage (2 approaches implemented)	Random	P	1
	DRX	Enable antenna short diagnosis	Random	P	0
	RXL	Switch antenna short diagnosis comparator threshold	Random	P	0
	RXCHK	Antenna short diagnosis status flag	Read only	P	0
PHMEAS	MPH[5:0]	Phase measurement result	Read only	P/S/R	111100b[1]
SMPLC	ST[5:0]	Receiver sampling time setting	Random	P	000000b
TXCON	ETX1	Enable TX1 driver	Random	P/S/R	1
	ETX2	Enable TX2 driver	Random	P/S/R	1
	TRIS	TX driver OFF configuration (tristate / ground)	Random	P/S/R	1

Table 3 Bit overview

Register	Bit	Function	Access	Reset Cond.	Reset Value
	PTX2	TX2 phase configuration	Random	P/S/R	0
	EPD[3:0]	Excitation pulse duration setting	Random	P/S/R	0000b
DRVCON	AVR[3:0]	Antenna voltage regulator setting (wave shaping)	Random	P/S/R	1111b
	CHK	Enable automatic check sequence	Random	P/S/R	0
	FAIL	Status bit for trimming and check sequence	Read / Clear	P/S/R	0
	THR	Configure AVR comparator threshold (0 = low threshold; 1 = high threshold)	Random	P/S/R	0
COMCON	MPW[3:0]	Modulation pulse width in transparent and buffered communication	Random	P	0111b
	MODE	Manchester decoder mode (0 : double edge ; 1 :single edge)	Random	P	0
	BDRT	Manchester decoder baudrate	Random	P	0
	MDPOL	Manchester decoder polarity setting	Random	P	0
BCDAT	BCD[7:0]	Buffered communication data register	Random	P/S/R	0x00
STATUS	DREQ	Data request bit for buffered communication	Read / Clear	P/S/R	0
	RDY	Buffered communication ready indication	Read only	P/S/R	0
	BFPR	Bitfail before last byte (inside protocol) indicator	Read only	P/S/R	0
	BFLB	Bitfail in last byte indicator	Read only	P/S/R	0
	BFP[2:0]	Bitfail in last byte position indicator	Read only	P/S/R	000b
	STAT	Buffered communication status information	Read / Clear	P/S/R	0
CHKSUM	CHK[7:0]	Checksum register	Read only	P/S/R	0x00

Note: For detailed information to the function of each bit see the corresponding chapter.

Note 1: Reset value of PHMEAS xx111100b only valid after a reset condition (P/S/R) and bit ACT is not set

Access

Random	Random access (read/write)
Read/Clear	Status bit (read/clear only, clear by write ‘1’)
Read only	Status flag (no write access)

Reset conditions

P	Power On Reset (POR)
S	Sleep mode (watchdog overflow will force the device into sleep mode)
R	Software Reset (RST bit)

6.4 Device Operating Modes

The device resides in one of three operating modes, Figure 3.

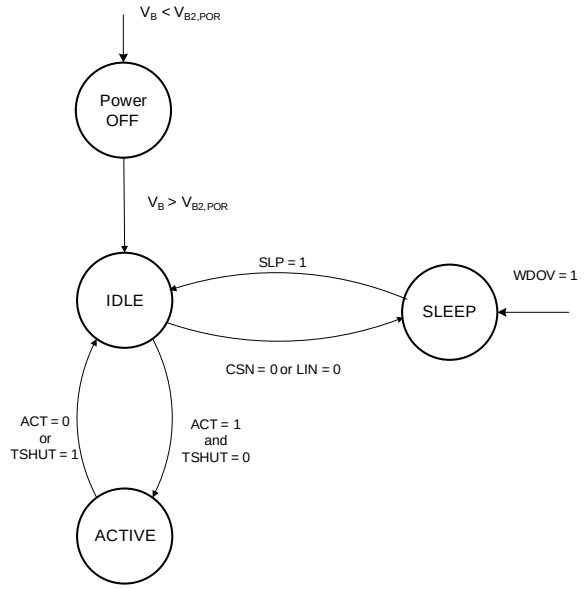


Figure 3. Device Operating Modes

Table 4 Device Circuitry State

Circuitry	SLEEP	IDLE	ACTIVE	Note
Voltage Regulator 1	OFF	OFF	ON	
Voltage Regulator 2	OFF	OFF	ON	
Serial Interface	SLEEP	ON	ON	2
LIN Transceiver	SLEEP	ON	ON	
XTAL Oscillator	OFF	ON	ON	
Watchdog	OFF	ON	ON	
TX1/TX2 Driver	Tri State	Tri State		1
Receiver Path	OFF	OFF	ON	
Temperature Sensor	ON	ON	ON	3
	SLP = 1 ACT = 0	SLP = 0 ACT = 0	SLP = 0 ACT = 1	

Note 1: When the device is ACTIVE, the actual TX1/TX2 Driver state depends on the application (register TXCON)
Note 2: Function of IOREF
Note 3: Default wakeup value, configurable in SFR

Important note:
After a power on reset all register bits are set to its reset condition. Thus the frequency select bits are reset too. This means the frequency selection has to be configured depending on the XTAL frequency before the desired protocol timing can be used. See 6.7 for further information.

6.4.1 SLEEP mode

In SLEEP mode most of the device circuitry is disabled, in order to achieve the lowest power consumption feasible, Table 4. The remote Wake Up detection circuitry (LIN Transceiver) is operational. The Wake Up detection circuitry implemented in the SPI interface is operational if IOREF is connected to an external supply. If IOREF is connected to VSS, only single wire interface mode is possible, the Wake Up from SPI (CSN) is ignored.

In SLEEP mode the antenna Driver Stage is forced into Tri State. The internal LIN slave termination between pins VB and LIN is disabled and instead a weak pull-up is applied in order to minimize power consumption.

The SLEEP mode is entered in case the Watchdog timer is allowed to timeout. Further, the SLEEP mode can be entered immediately by setting the control bit SLP (SLP = 1), See section 6.6. The setting of the control bit SLP (SLP = 1) is possible with the WR_SCFG command only.. This command is not compliant to LIN 2.0. To be tolerant for LIN 2.0 applications entering SLEEP mode via special PID must be chosen. See 6.6.

NOTE: If the pin LIN is in dominant condition the device will get another wakeup immediately after it is set into SLEEP mode and the device will not reside in SLEEP mode.

6.4.2 IDLE mode

In IDLE mode most of the device circuitry is disabled. However, the XTAL Oscillator, the Serial Interface and the LIN Transceiver are turned on (see Table 4). The antenna Driver Stage is forced into Tri State. The internal LIN slave termination between pins VB and LIN is enabled.

The IDLE mode is entered upon detection of a valid wake-up (remote wakeup via LIN or SPI wakeup via CSN depending on the interface mode). Additionally the IDLE mode is the default mode after a power on reset condition.

Further, the device is forced into IDLE mode in case the Temperature Sensor detects the virtual junction temperature exceeding the specified limit (T_{SHD}).

6.4.3 ACTIVE mode

In ACTIVE mode the device is fully operational and all circuitry enabled (see Table 4). Upon command the device is ready to receive and send transponder data.

The ACTIVE mode is entered by setting the control bit ACT (ACT = 1), provided that the Temperature is below T_{SHD}.

6.5 Device wake-Up

In order to terminate the SLEEP mode and to resume device operation by entering IDLE mode, a wake-up has to be applied. In such an event, the control bit SLP is cleared (SLP = 0).

Several wake-up possibilities depending on the serial interface mode are available.

6.5.1 Remote Wake-Up

A Remote Bus Wake-Up condition applies, when the bus line receiver detects a falling edge at pin LIN, followed by a low state for a certain timeout period T_{REM} and finally, a rising edge respectively, see Figure 4.

The remote wake-up is active in single wire mode as well as in SPI mode.

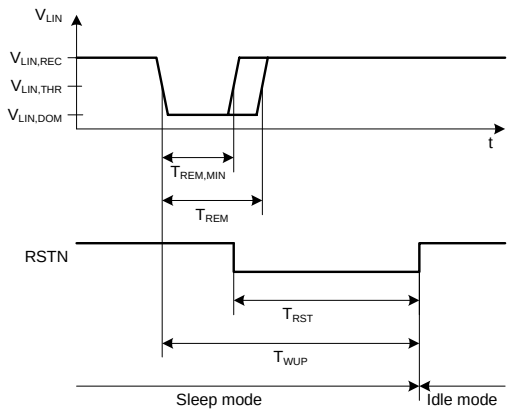


Figure 4. Remote Bus Wake-Up signal timing

For use with an external microcontroller the detection of a remote bus wake-up is indicated at the RSTN pin provided that an external pull-up resistor is connected to $V_{OH,RSTN}$ (e.g. IOREF). The pin RSTN is kept low for a specified time T_{RST} to allow the oscillator clock to start-up and stabilize. Finally the device enters the IDLE Mode and is ready for communication.

6.5.2 SPI Wake-Up

In SPI mode a device wake-up is forced by a falling edge at pin CSN, followed by a low state for a certain period T_{REM} (e.g. to avoid unintended device wake-up due to EMI) and finally a rising edge at pin CSN (Figure 5).

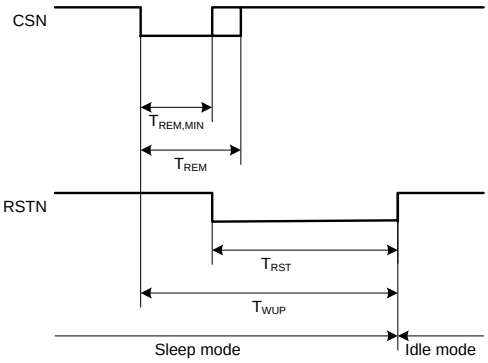


Figure 5. SPI wakeup signal timing

It takes the time T_{RST} to allow the oscillator clock to start-up and stabilize, before finally the device enters the IDLE Mode and is ready for communication. During this time the wake-up sequence is indicated at the pin RSTN that is forced to low. The SPI wakeup is active in SPI mode only.

6.5.3 Wake-up on power on reset

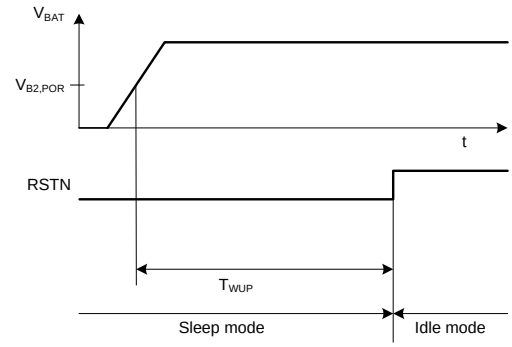


Figure 6. Wake-Up on power on reset timing

The device wakes up autonomously after exceeding the power on reset supply voltage threshold. The XTAL-oscillator is started and the frequency divider is configured in its reset condition. Hence the overall timing will be directly dependent on the selected XTAL frequency. Desired protocol timing is valid after correct setting of the corresponding configuration registers. It is strongly recommended to monitor the ‘POR’ flag inside the ‘DCON1’ register regularly. If ‘POR’ is set, all relevant configuration data has to be re-initialized, Furthermore, after a power-on event, ‘POR’ has to be cleared again by writing a ‘1’. For more information on power on reset see 6.14.

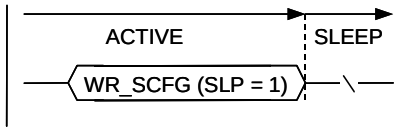
6.6 Enter SLEEP Mode

To enter SLEEP Mode several possibilities are available. The fastest way is to set the bit SLP in DCON1 register by a direct write access. This will cause the device to enter SLEEP mode immediately and is independent of the serial interface mode.

The second way is to use the implemented watchdog timer with 2 different timeout configurations. This will cause the device into sleep mode after the configured watchdog timeout.

For use of the device in multiple slave network applications (in single wire mode) a dedicated LIN 2.0 compliant sequence has been implemented. The sequence starts with a break/sync field followed by a special PID (0x3C) and a data byte (0x00). It reconfigures the watchdog to $T_{SLP,DLY}$ and is available in single wire mode only. After this time the watchdog timer will force the device into SLEEP mode, see Figure 7.

a) SPI and Single Wire Mode



b) Single Wire Mode using special PID

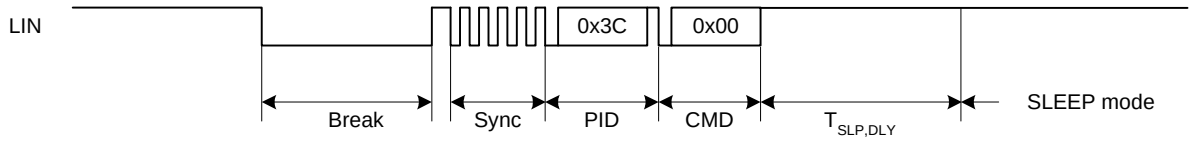


Figure 7. Entering SLEEP Mode

6.7 System Clock Generation

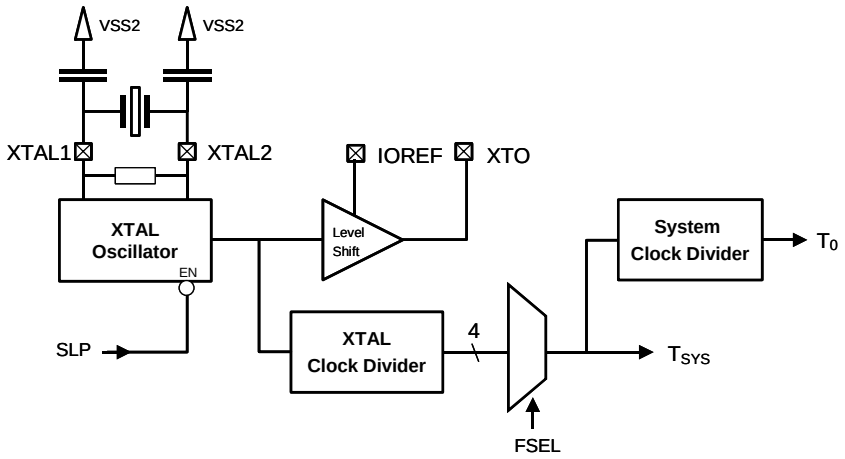


Figure 8. System Clock Generation

The system clock and timing is derived from the on-chip XTAL oscillator or an external clock source. A programmable clock divider allows to utilize clock frequencies of 4, 8 and 16 MHz, Figure 8.

The PJF7992A can be operated with an external clock source. The external source must be applied via AC coupling on XTAL1. The internal feedback resistor connected between XTAL1 and XTAL2 will set the DC

operating voltage. The voltage on XTAL1 shall not exceed the specified $V_{IL,XTAL}$ and $V_{IH,XTAL.}$

The XTAL clock divider has to be configured by the host after each POR to assure a system clock f_{SYS} of 4 MHz.

Note:
Most device internal timings (like serial interface, watchdog, transponder communication…) are related to the system clock.

6.7.1 XTAL Oscillator

The oscillator provides the system clock to the device and external circuitry, if desired, e.g. a microcontroller.

An external ceramic resonator (crystals are not supported) controls the oscillator. Recommended resonator types can be requested from NXP.

For the 16 MHz configuration decreased driving capabilities of the clock output pin XTO has to be taken into account (see electrical characteristics). The oscillator features an on-chip feedback resistance and requires external load capacitors according to the resonator specification.

In SPI mode the device features a buffered output, providing the oscillator clock for use with an external device, e.g. microcontroller. The buffered output features a level shifter, to adopt the clock signal to the actual supply voltage utilized for external circuitry (IOREF).

6.7.2 FSEL, Frequency Select

The control bits FSEL enables the device to accept a clock frequency of 4, 8 or 16 MHz and consequently to derive the proper system timing.

Table 5 Frequency divider control (frequency selection)

Reg	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
DCON0	*RFU*	*DISXTO*	*RST*	*RFU*	*WDMD*	*OSCDIS*	**FSEL_1**	**FSEL_0**

FSEL1	FSEL0	f_{XTAL}	f_{SYS}	Note
1	1	16 MHz	f_{XTAL} / 4	1
0	1	8 MHz	f_{XTAL} / 2	
0	0	4 MHz	f_{XTAL}	

Note 1 After a Power On Reset the control bits FSEL are reset, selecting the highest division ratio.

Note 2: An FSEL setting of (10b) would configure the divider for f_{XTAL} / 3, but this mode shall not be used

Unless the frequency divider is not configured to provide a system frequency of $1/T_{SYS}$ = 4MHz the device internal timings are different from specified values. In this case the serial interface timing (SPI data rate, single wire break length) has to be adapted.

After each change of FSEL bit a LIN synchronization shall be performed.

In single wire mode a change of the FSEL bits will cause the stored baudrate setting to be reset to the 20 kBd value.

6.7.3 XTAL Oscillator Clockfail detection

The XTAL oscillator features a clock fail detection unit. If the XTAL clock fails during operation the clock-fail detection unit switches the device into SLEEP mode.

6.8 Watchdog Timer

Table 6 Watchdog timer control

Reg	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
DCON0	*RFU*	*DISXTO*	*RST*	*RFU*	**WDMD**	*OSCDIS*	*FSEL_1*	*FSEL_0*
DCON1	*SLP*	*ACT*	*POR*	*TSHUT*	**WDOV**	*SWRES*	*SWFRM*	*SWCS*

WDMD	Watchdog timeout timing configuration. 0 … T_{WTD_0} 1 … $T_{SLP,DLY}$
WDOV	Watchdog overflow status bit. Has to be cleared manually by writing ‘1’.

The device features an implemented watchdog timer using the implemented XTAL oscillator, Figure 9.

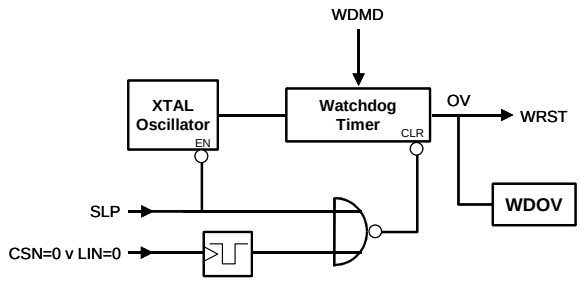


Figure 9. Watchdog Timer

Except in SLEEP mode (SLP = 1) the watchdog timer is active in each device mode. The watchdog timer is cleared at each falling edge on the data input of the serial interface depending on the serial interface mode (LIN in single wire; CSN in SPI mode). In case of a watchdog timer timeout, the WDOV flag is set and the device is set into SLEEP mode by setting the SLP bit. The FSEL setting is not changed but the configured single wire baudrate is set to its default value (20kBd).

Once set, the WDOV flag remains set until it is cleared or a Power On Reset is experienced.

The default watchdog timeout period is T_{WTD_0}. Setting the bit WDMD to ‘1’ sets the watchdog timer to $T_{SLP,DLY}$.

6.9 Transmit Path

The device drives an external antenna operating in resonance, in order to establish an LF Field that can be modulated by On-Off-Keying, OOK, according to the data designated for transmission. In case the device operates in transparent mode, On-Off-Keying is directly controlled via the pins DI (SPI mode) or LIN (single wire mode), resulting in TXMOD, whereas in buffered mode an on-chip BPLM Modulator autonomously transmits the data, see section 7.7.

The transmit carrier clock (T_0) is derived from an on-chip XTAL oscillator and typical yields 125 kHz (f_C). Generation of the antenna drive signal employs Wave Shaping, a Modulation Pulse Timer and versatile Driver stage. Latter one may employ a supply that is controlled in accordance to the carrier level detected at the receiver input, Figure 10. To control the transmitter circuit the register TXCON and COMCON has to be set correspondingly.

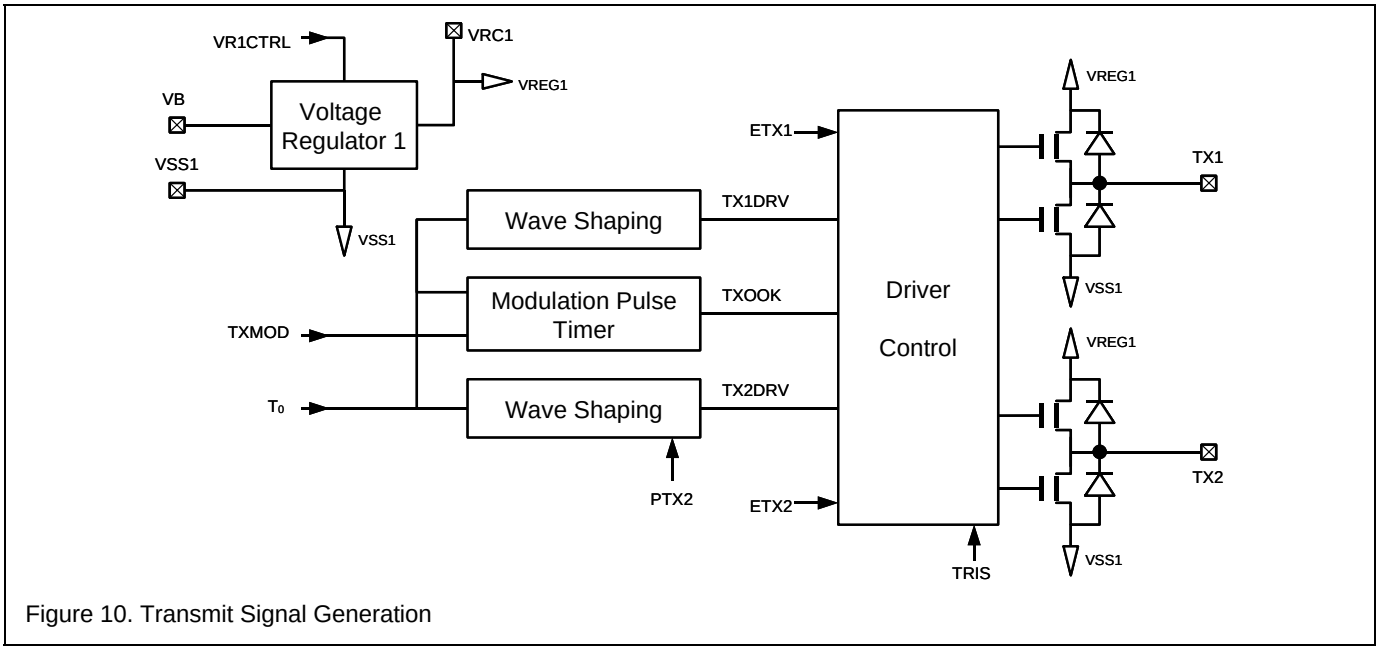


Figure 10. Transmit Signal Generation

6.9.1 Modulation Pulse Timer

On-Off-Keying of the antenna driver may either be executed in accordance to the modulation signal supplied or may employ a pulse timer that is triggered by a low to high transition of the modulation signal (TXMOD) only. The carrier modulation is synchronized with the carrier clock, Figure 11.

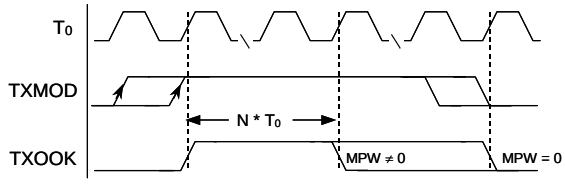


Figure 11. Modulation Pulse Timing

The control bits MPW allow to configure the modulation pulse timer for a LOW duration of 1 to 15 carrier clock periods ($T_0 = 1/f_C$) or to operate in transparent mode, Table 7.

Table 7 Modulation pulse timer control

Reg	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
COMCON	*RFU*	*MDPOL*	*BDRT*	*MODE*	**MPW3**	**MPW2**	**MPW1**	**MPW0**

MPW3	MPW2	MPW1	MPW0	LOW Pulse Duration	Note
0	0	0	0	TRANSPARENT	1
0	0	0	1	T_O	
0	0	1	0	2 T_O	
0	0	1	1	3 T_O	
0	1	0	0	4 T_O	
N				N T_O	
1	1	1	0	14 T_O	
1	1	1	1	15 T_O	

Note 1: Pulse timer disabled and forced into transparent state. Pulse timing is determined by the data timing.

In case of buffered transponder communication, use of the pulse timer is mandatory, as the transmit data is read from a buffer.

6.9.2 Antenna Driver

Table 8 Transmitter control register

Reg	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
TXCON	**EPD_3**	**EPD_2**	**EPD_1**	**EPD_0**	**PTX2**	**TRIS**	**ETX2**	**ETX1**

ETX1	Enable transmitter path TX1
ETX2	Enable transmitter path TX2
TRIS	Switch transmitter to tri-state if no path is driving
PTX2	Invert the phase of transmitter path TX2. This will cause the transmitter path TX1 and TX2 to drive in the same phase.
EPD[3:0]	Wave Shaping configuration bits, see 6.9.3.

The antenna driver is capable to deliver a rectangular shaped drive voltage to the series resonant antenna circuit, featuring a low output impedance. The antenna driver can be configured to operate in full-bridge or half-bridge via the bits ETX1 and ETX2.

In full-bridge operation (ETX1 = ETX2 = 1) both push-pull drivers are operational, enabling complementary drive signals, giving the largest voltage swing across the driver output. In half-bridge operation only one push-pull driver is utilized, while the other is disabled. (ETX1 = 0, respectively ETX2 = 0). The device may be switched from full-bridge into half-bridge operation at any time. The change is synchronized with the system clock and takes effect immediately after the register TXCON has been written.

Complementary drive signals are utilized, if the corresponding control bit for the Wave Shaping is set accordingly (PTX2 = 0). Otherwise (PTX2 = 1), both drivers operate in-phase enabling parallel operation, see section Wave Shaping.

Table 9 Antenna driver control

ETX1 ETX2	TRIS	TXMOD	TX1DRV TX2DRV	TX1 TX2	Note
0	0	X	X	LOW	
0	1	X	X	Tri State	
1	X	0	0	LOW	
1	X	0	1	HIGH	
1	0	1	X	LOW	
1	1	1	X	Tri State	

The available antenna drive current (I_{TX}) is limited by the voltage regulator (V-REG 1) capabilities and power dissipation restrictions. In case of chip overheating ($T_{J,SD}$) the antenna driver will be disabled and forced into Tri-state automatically, see section 6.1.

In device Power Down mode or when disabled while residing in IDLE mode, the antenna driver is forced into Tri-state.

6.9.3 Wave Shaping

The antenna drive signal features a programmable duty cycle, affecting the pulse duration of the excitation signal, Figure 12.

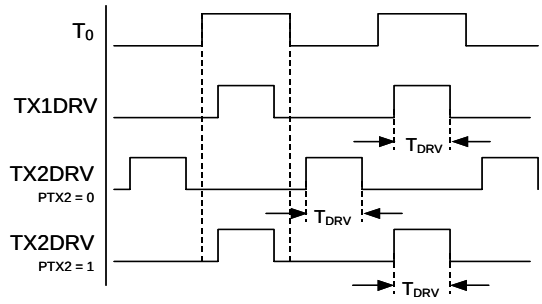


Figure 12. Antenna Driver Pulse Width

This technique provides means for wave shaping for improved system EMI characteristics, mainly targeting the 3th and 5th harmonics. The pulse duration of the excitation signal can be set with a resolution of 125 ns, according to Table 10.

Table 10 Excitation Pulse Duration, EPD

EPD3	EPD2	EPD1	EPD0	Pulse Duration, T_{DRV}	Note
0	0	0	0	4.000 µs	1
0	0	0	1	3.875 µs	
0	0	1	0	3.750 µs	
				(4 – N x 0.125) µs	2
1	1	1	0	2.250 µs	
1	1	1	1	2.125 µs	

Note 1: Represents a pure square wave (50% duty cycle).

Note 2: The binary equivalence of EPD[3:0] determines N. For example, if EPD[3:0] = 0010_b, N = 2.

During the OFF state the driver outputs are forced LOW, unless a modulation is applied, which forces the driver in either LOW (TRIS = 0) or in Tri State (TRIS = 1), see section 6.9.2.

The antenna drive signals are typical complementary (PTX2 = 0), however may be configured being in-phase (PTX2 = 1), in order to support parallel operation in half-bridge configuration, see section 6.9.2.

6.9.4 Drive Voltage Control

Table 11 Antenna driver control register

Reg	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
DRVCON	**THR**	**FAIL**	**CHK**	**RFU**	**AVR_3**	**AVR_2**	**AVR_1**	**AVR_0**

AVR[3:0]	Antenna drive voltage setting, see Table 12
CHK	Control and status bit for the automatic check sequence.
FAIL	Status bit indicating an incorrect trimming or check sequence.
THR	Trimming comparator threshold configuration. 0 … $V_{T,LO}$ 1 … $V_{T,HI}$

When selected by configuration, the V-Reg 1 voltage is controlled (DRVON), hence lowered, in accordance to the carrier level sensed at the receiver input (RX). This measure limits the LF Field that is excited under perfect tuning conditions of the antenna resonance circuit.

Table 12 Antenna Driver Voltage Control

AVR_3	AVR_2	AVR_1	AVR_0	Tx DC Voltage
1	1	1	1	$V_{VRC1,LO}$
1	1	1	0	$V_{VRC1,LO} + V_{VRC1,step}$
1	1	0	1	$V_{VRC1,LO} + 2*V_{VRC1,step}$
X	X	X	X	
0	0	0	1	$V_{VRC1,LO} + 14*V_{VRC1,step}$
0	0	0	0	$V_{VRC1,HI}$

The device features a manual Tx voltage adjustment, which is controlled by register DRVCON.

To get the resulting receiver input voltage to the optimum value a comparator with two thresholds (VT,LO; VT,HI) is implemented. The comparator result is checked and indicated by the FAIL bit in register DRVCON.

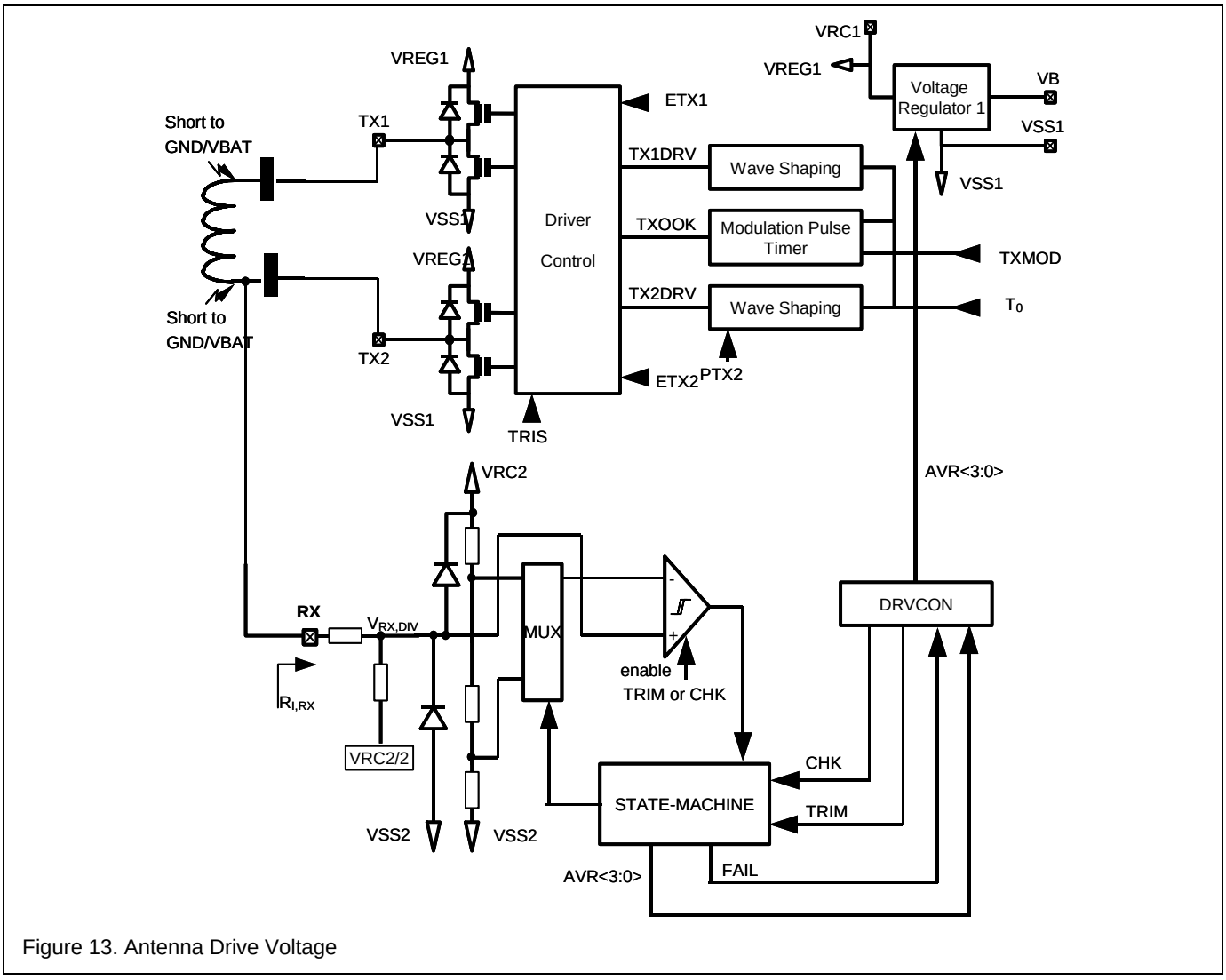


Figure 13. Antenna Drive Voltage

6.9.4.1 Manual Drive Voltage Adjustment

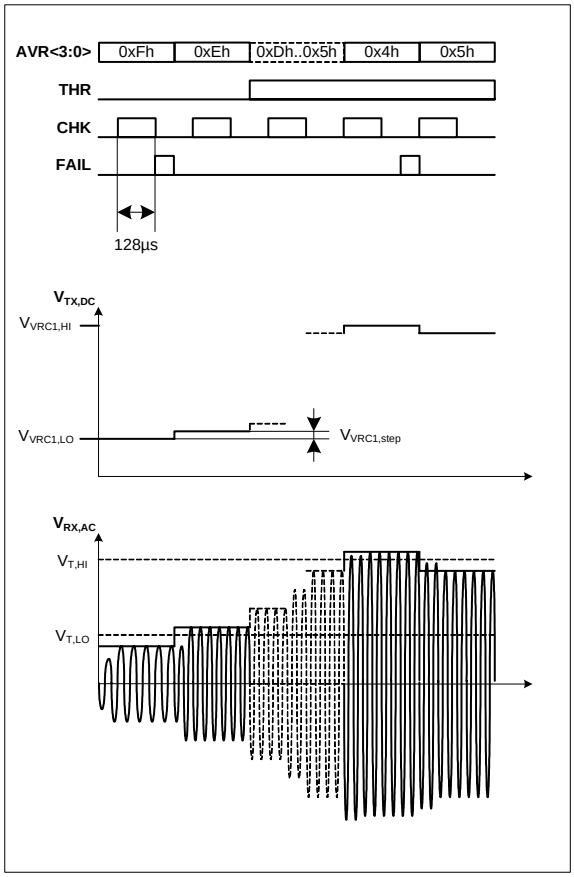


Figure 14. Antenna Drive Voltage manual adjustment

The Tx drive level is configured by the register bits AVR[3:0] in the DRVCON register. The DC voltage $V_{TX,DC}$ on the Tx pins can be adjusted from $V_{VRC1,LO}$ up to $V_{VRC1,HI}$ in steps of $V_{VRC1,step}$. To check the amplitude of the Rx signal (in order to guarantee correct operation the divided Rx amplitude has to be lower than $V_{T,HI}$ referred to VGND) the control bit THR has to be set according to the threshold (lower or higher) to check against. By setting the control bit CHK an automatic check sequence is introduced. According to the setting of the control bit THR a check against the lower (THR=0) or the higher (THR=1) threshold is performed. For checking against the lower threshold ($V_{T,LO}$), a drive voltage below $V_{T,LO}$ is indicated by the status bit FAIL (FAIL=1). For a check against the higher threshold ($V_{T,HI}$), a drive voltage above $V_{T,HI}$ is indicated by the status bit FAIL (FAIL=1). Using this manual check a manual trimming sequence can be performed by increasing the drive voltage and checking against the corresponding threshold values.

Note: If the FAIL bit is set to hi by the state-machine, it must be cleared manually by writing a '1' to the corresponding bit position.

6.10 Receive Path

The device features an improved receiver design, avoiding external capacitors at all or making the device reluctant to leakage currents of up to 0.5µA for external capacitors eventually required.

Table 13 Receiver path control registers

Reg	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
RCON0	**RFU**	**HYST**	**RNG1**	**RNG0**	**GAIN1**	**GAIN0**	**RFU**	**RFU**
RCON1	*RXCHK*	*RXL*	*DRX*	**SWHP2**	**HPDIS**	**LPDIS**	**FRZ1**	**FRZ0**
PHMEAS	*RFU*	*RFU*	**MPH_5**	**MPH_4**	**MPH_3**	**MPH_2**	**MPH_1**	**MPH_0**
SMPLC	*RFU*	*RFU*	**ST_5**	**ST_4**	**ST_3**	**ST_2**	**ST_1**	**ST_0**

GAIN[1:0]	Baseband amplification control, see Table 15
RNG[1:0]	Receiver input voltage range, see Table 14
HYST	Enable hysteresis of demodulator (100mV) and lower sensitivity
FRZ[1:0]	Receiver freeze control, see Table 16
LPDIS	Disable low pass filter
HPDIS	Disable high pass filter
SWHP2	Enable alternative high pass filter for last stage 0 … GmC filter 1 … SC filter (default)
MPH[5:0]	Phase measurement result
ST[5:0]	Sampling time control

6.10.1 Receiver Input and EMI Filter

The receiver input pin offers a large input voltage range, featuring an on-chip matched and programmable voltage divider, in order to scale the resonant circuit tap voltage largely independent of process spreads. An additional external resistor has to be added only, if the tap voltage exceeds the maximum input voltage range.

According to Figure 15, the input signal passes a resistive divider that features a low-pass filter characteristic ($f_{LP,EMI}$), in order to attenuate unwanted input signals for improved device EMI behavior. The configuration bits RNG allow to select four different receiver input voltage ranges, Table 14.

Table 14 Receiver Input voltage range, RNG

RNG1	RNG0	Input Voltage Range	Note
0	0	$0.25 * V_{I,RX}$	
0	1	$0.50 * V_{I,RX}$	
1	0	$0.75 * V_{I,RX}$	
1	1	$V_{I,RX}$	

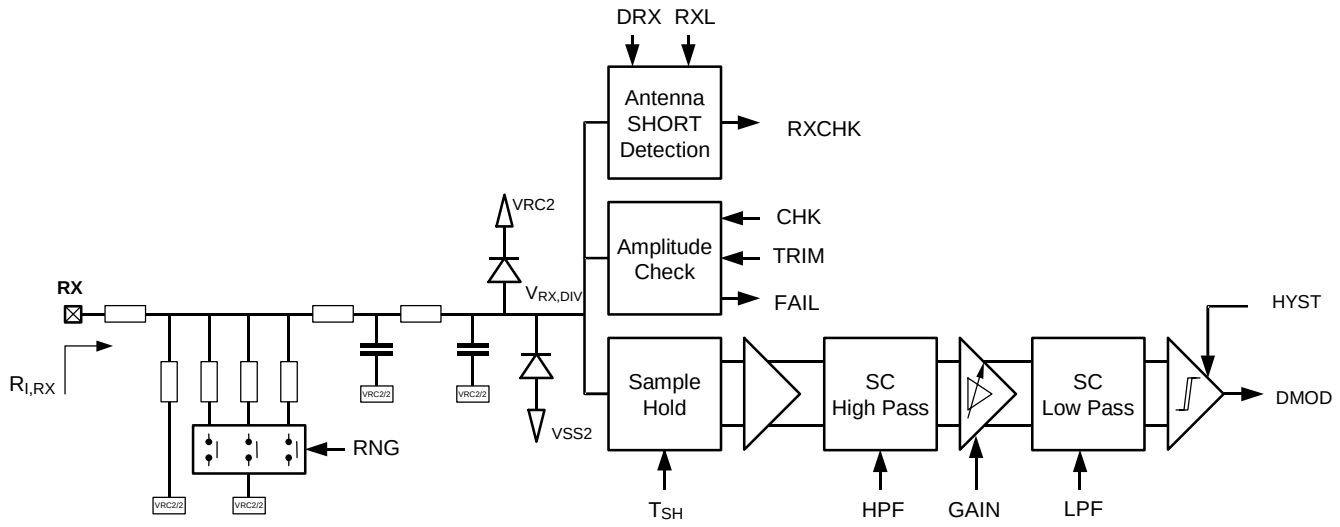


Figure 15. Receiver architecture

6.10.2 Demodulation

Receive signal demodulation is accomplished by NXP's patented Adaptive Sampling Time technique. The scaled receiver input signal is fed to a Sample & Hold circuitry that provides the demodulated and differential output signal, by sampling the signal in-phase and in anti-phase at carrier clock rate. The sampling time is programmable, in order to cope with variations of the antenna resonance frequency.

6.10.3 Base Band Filtering and Amplification

The demodulated receive signal passes a filter and amplifier chain prior to digitalization. The filters are optimized for a data rate of 4kbps for transponder reading.

The base band amplification is programmable, according to Table 15.

Table 15 Base Band Amplification, GAIN

GAIN1	GAIN0	Signal Amplification	Note
0	0	100	
0	1	200	
1	0	500	
1	1	1000	

6.11 Receiver settling

For receiver settling after device power-up, sampling time shift or when switching from transponder write to read mode the digitizer circuit biasing condition can be initialized and restored by configuring the bits FRZ[1:0]. A special sequence is implemented that feature automatic settling of the receiver upon switching from transmit to receive mode (WR_RD_TAG, WR_RD_BUF command).

The effect of the different freeze settings is shown in Table 16.

Table 16 Receiver freeze settings

FRZ[1:0]	Sample & Hold	High pass filter	Low pass filter	Comment
00b	normal	normal	normal	Normal operation
01b	disabled (switches open)	QGND (switches closed)	normal	Used during OOK phase
10b	normal	QGND (switches closed)	normal	Restore sample & hold load
11b	normal	boost mode (fast timing)	normal	Fast settling of high pass filter

6.11.1 Fast settling sequence

For the write/read commands (WR_RD_TAG and WR_RD_BUF) the device features an automatic settling sequence for the receiver path. The fast settling sequence provides fixed timings to get an optimized settling of the receiver circuit. The sequence uses the freeze settings controlled by the FRZ[1:0] bits in register RCON1. For other commands the application is open to control these freeze settings manually and to implement user defined settling timings.

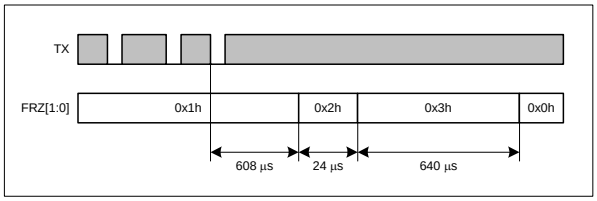


Figure 16. Fast settling sequence timing

Note: Manual start of the fast settling sequence is not supported.

During OOK (On Off Keying) the freeze setting is 0x1h where the S&H stage is frozen and the high pass filter is in QGND condition. At start of the last modulation pulse the freeze settings are controlled automatically.

6.12 Device Diagnostics

The device provides a set of diagnostic features. These are available during normal device operation (ACTIVE mode) and incorporate means to detect an antenna SHORT or OPEN condition. It is not mandatory to distinguish between the failure modes. An Open/Short condition doesn't disable the antenna driver automatically; instead the application is responsible to decide about the appropriate actions. An on-chip temperature sensor protects the device from being damaged due to the failure modes.

6.12.1 Antenna SHORT/OPEN detection

Table 17 Antenna short/open detection

Reg	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
RCON1	**RXCHK**	**RXL**	**DRX**	*SWHP2*	*HPDIS*	*LPDIS*	*FRZ1*	*FRZ0*

DRX	Enable short circuit detection
RXL	Switch short circuit detection threshold 0 … higher threshold 1 … lower threshold
RXCHK	Antenna diagnosis status flag

Antenna SHORT/OPEN detection is accomplished by two techniques, that need to be applied both in order to cover all failure modes.

6.12.1.1 Short Circuit of Antenna Terminals against GND or VBAT

Detection of a short circuit condition of the antenna terminal is feasible only if the driver stage is disabled and the antenna driver outputs (pin TX1 and TX2) reside in Tri State. In addition it is mandatory, that the receiver input (pin RX) feature a DC path to the antenna coil, which typically is the case, Figure 17.

Short circuit detection is accomplished by checking the DC bias condition at the receiver input (pin RX). Latter one typically yields VDD/2 and will be pushed towards GND or VBAT in case one of the terminals suffers a short to GND respectively VBAT.

Setting the control bit (DRX = 1) enables short circuit detection. The Antenna driver must be disabled (ETX1 =ETX2 = 0) and should be forced into Tri State (TRIS = 1). The range setting of the receiver input voltage must be set to 0.25 * $V_{I,RX}$ (RNG[1:0] = 0x00h). After setting, the control bit RXL has to be set to chose the high (short to 5V supply) or the low (short to ground) threshold value. The short circuit detection result is indicated by RXCHK status bit. For setting of RXL and evaluating the RXCHK flag see Table 18.

Table 18 Short circuit detection result evaluation

	RXCHK result	
	RXL = 0	RXL = 1
Antenna OK	0	1
Short to GND	0	0
Short to VDD	1	1

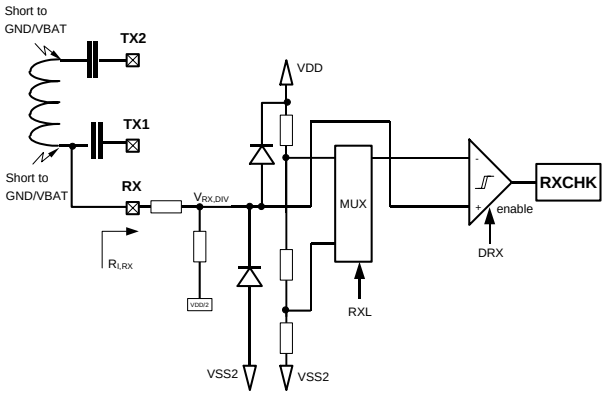


Figure 17. Antenna SHORT Diagnostics

6.12.1.2 Short Circuit of Antenna Terminals against each other or Open condition

Detection of a short circuit or open condition of the antenna terminals itself is feasible by checking the antenna phase and/or carrier level at the receiver input (pin RX).

6.12.2 Temperature Shutdown

In order to protect the device from overheating, an on-chip temperature sensor is provided that monitors the chip temperature. In case the chip temperature exceeds the temperature shutdown threshold T_{SHD}, the device enters IDLE mode, the flag TSHUT is set and the bit ACT is cleared. The TSHUT flag has to be polled by the microcontroller to perform the desired action accordingly.

6.13 LIN Transceiver

For single wire operation, the device incorporates a serial transceiver which physical layer is

- compliant with LIN 2.0
- compliant with SAE J2602
- compatible with LIN 1.3

The transceiver is controlled by register LINCFG (see Table 19).

Table 19 LIN transceiver control

Reg	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
LINCFG	*RFU*	*RFU*	*RFU*	*RFU*	**TXON**	**TXSS**	**ISLPON**	**RTON**

RTON	Enable internal termination resistor R_{PU} (30kOhm)
ISLPON	Enable low power termination (75µA current source for pullup)
TXSS	Switch bandwidth of transceiver circuit 0 … Baudrate < 10.4 kBd 1 … Baudrate > 10.4 kBd
TXON	Enable transmitter driver (tri-state buffer)

In single wire mode an internal state machine controls the LIN transceiver (see 7.3). The implemented single wire protocol is LIN 2.0 Protocol Layer tolerant, since a minimum set of LIN 2.0 messages is supported. Any write access to the configuration bits of the transceiver in single wire mode does not have any effect.

In order to get full LIN 2.0 protocol compliancy, an external microcontroller has to be added.

For manual control of the LIN transceiver the corresponding bits have to be set and the communication is done by applying data to TXD and reading data at RXD. The LIN transceiver converts the data fed to the TXD input into a bus signal with controlled slew rate and wave shaping minimizing EME. The LIN bus output pin is pulled HIGH via an internal termination resistor. Similarly, the receiver circuitry converts the signal applied to the LIN input pin. The converted signal is available at pin RXD.

The LIN Transceiver supports normal slope mode and low slope mode. In single wire mode (see Figure 1a), the slope is selected automatically dependent on the data rate detected on the bus line.

In low slope mode (data rates below 10.4 kbps or bit TXSS = 0 in LINCFG), the slew-rate of the bus signal is lowered to thus further reduce the already low emission in normal slope mode. Otherwise the normal slope mode is used.

6.14 Power On Reset

The device generates an internal power-on reset to initialize the chip after a power-on or power fail condition. The power-on reset senses the supply voltage applied to pin VB. An active low reset signal is generated at pin RSTN for external circuitry and prolonged as specified (T_{RST}).

The output of pin RSTN is configured as Open Collector, allowing to “wire OR” it with other similar reset sources, e.g. from an external Voltage Regulator or Reset Supervisory circuitry. The output does not feature an on-chip pull-up resistor.

For proper system operation the bus master starts bus communication after the PJF7992A Power On reset is settled (T_{RST}).

7 SERIAL INTERFACE

Communication with the device utilizes a serial interface, either operating in SPI or Single Wire mode, depending on the application needs.

The serial interface provides means to configure the device and to communicate with an LF transponder device, present in the LF field. Device configuration utilizes a set of commands to control and modify the corresponding device register.

Upon command the serial interface is set into transparent or buffered transponder communication mode, enabling read/write access to the Transponder. In transparent mode, the data lines (LIN, DI, DO) are utilized to provide direct control over the antenna driver and direct access to the demodulated receive signal. In buffered mode, a Binary Pulse Length Modulation (BPLM) encoder and a Manchester decoder are provided to send and receive transponder data in blocks of 8 bit.

7.1 Operation Modes

The serial interface is capable to be configured for SPI or Single Wire operation. For architectures with embedded base station, the SPI operation is most suitable, as it provides a fast and direct access to the device. For architectures with a remote base station, the single wire mode is advantageous, as it requires only three interconnecting wires (VBAT, GND and LIN) and features excellent signal to noise properties for the serial data communication.

The pin IOREF determines the serial interface mode of operation. SPI operation is selected, if the voltage level at pin IOREF exceeds a certain threshold ($V_{IOREF,IMS}$). In this case, the voltage level at pin IOREF also serves to match the interface I/O voltage level specification with the supply provided for the external microcontroller. The microcontroller and pin IOREF must be supplied from an external voltage regulator (2.7V to 5.5V) in this case.

Otherwise, if pin IOREF is below a certain threshold ($V_{IOREF,IMS}$), Single Wire operation is selected.

7.2 SPI Mode

SPI mode is selected by setting V_{IOREF} to values larger than $V_{IOREF,IMS.}$ In this mode, the interface operates synchronously during command reception and response, employing a dedicated data in, DI, data out, DO, and data clock, CLK, line. A Chip Select line is provided for applications with multiple SPI slaves and to wake up the device from SLEEP mode. In single slave applications the chip select pin CSN must not be set to ground because of additional functionality like wakeup, initialization and control of transparent communication.

During SPI Mode the interface signals (DI, DO, CLK) are subject to oversampling for improved EMI robustness. The SPI signals are sampled every 125ns.

7.2.1 SPI protocol and timing

The protocol layer of the SPI interface operates with MSB first.

Data in (DI) is latched upon the rising edge of the clock line, while data out (DO) is provided with the falling edge of the clock line, see Figure 18.

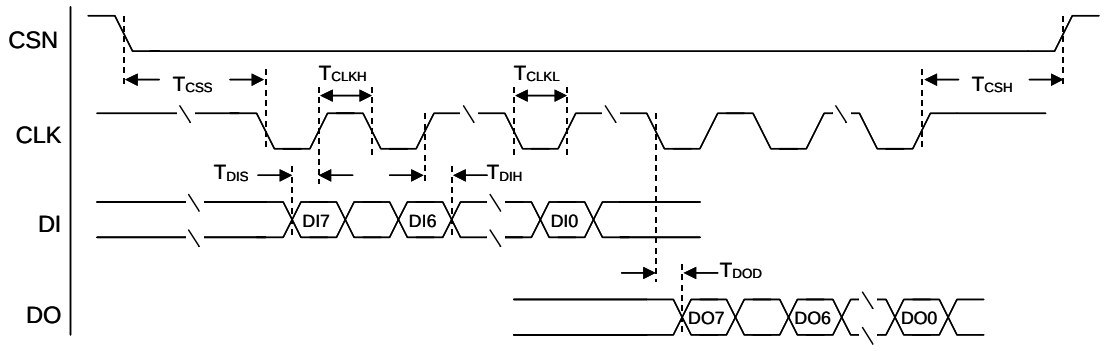


Figure 18. SPI Interface Timing

7.2.2 SPI Command byte

Command bytes consist of 6 bit command code and 2 bit parity to increase data integrity.

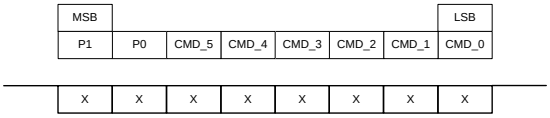


Figure 19. SPI mode command byte

7.2.3 SPI Data byte

Data bytes can consist of any content, dependent on the application.

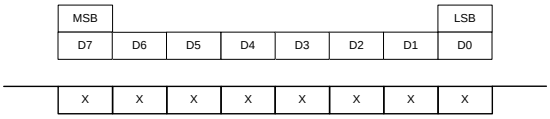


Figure 20. SPI mode data byte

7.3 Single Wire Mode

The single wire mode is selected by setting V_{IOREF} to values smaller than $V_{IOREF,IMS.}$ In this mode, data in and data out share the same wire and the interface operates asynchronously, avoiding a dedicated data clock line. Instead, the data clock is derived from the system clock and adapted to the data rate detected on the communication wire during the device synchronization sequence. Once this sequence is completed, the device is ready to receive and execute commands. The data rate adaptation does operate over a wide range from 8 kbps to 20 kbps. The device wakes up and the synchronization procedure has been designed to be LIN 2.0 Protocol Layer tolerant.

During transparent communication with the transponder, the actual data rate is irrelevant and the timing is determined by the transponder protocol.

The single wire mode utilizes the on-chip LIN Transceiver to communicate remotely with the device. An external microcontroller is not required and the LIN Transceiver is controlled by the internal state machine. The pins CSN, DI and CLK are without function and can be set to ground. Leaving the pins open is possible because of internal input termination when the device works in single wire mode. The pin LIN assembles the single wire bi-directional serial interface, for communication with the device and the transponder.

7.3.1 Single Wire protocol and timing

The protocol layer of the single wire interface operates with LSB first.

If the device and the interface are in power down condition, the communication has always to start with a remote wakeup followed by a synchronization sequence and the protected identifier (PID). After this sequence the interface is awaiting the first command. To wakeup the device the LIN line has to be forced to 0 (dominant) for a certain time T_{REM}. After the device startup time T_{WUP} the interface is awaiting the synchronization sequence.

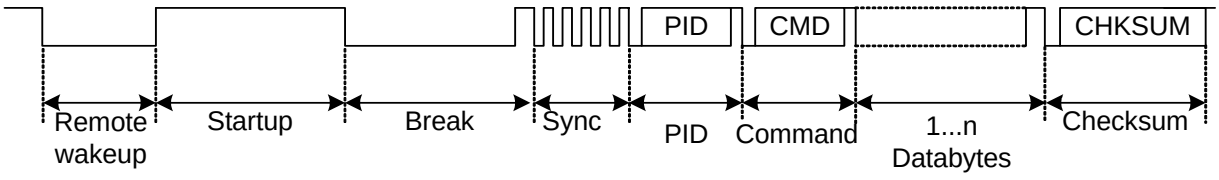


Figure 21. Single Wire: Start up sequence with following communication

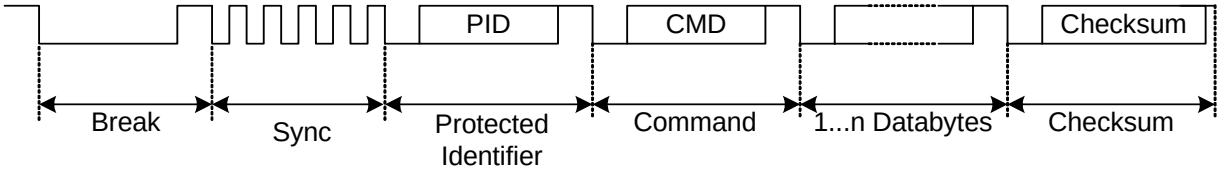


Figure 22. Single Wire: standard communication sequence

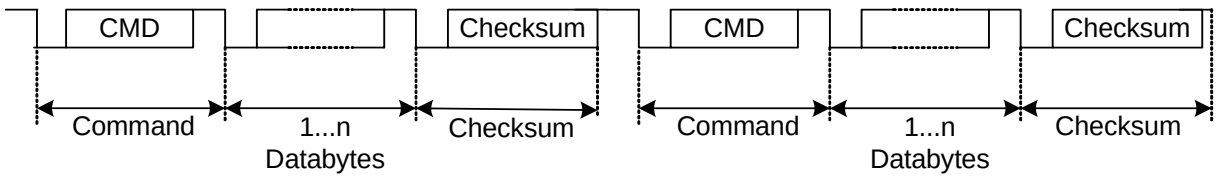


Figure 23. Single Wire communication sequence without new synchronization sequence

The synchronization sequence starts with a 'break field' followed by a synchronization field (sync). The 'sync' field is a data byte with the content 0x55. In this sequence the interface adapts to the current bit rate. The length of the bits in this synchronization sequence is taken as the reference length for the following communication until the next synchronization sequence is performed.

After the command and data bytes have been exchanged a checksum transmission completes the running communication. For all commands except 'WR_SCFG' the checksum is sent by the PJF7992A after the last byte has been exchanged. In case of the 'WR_SCFG' command the correct checksum must always be sent to the PJF7992A, otherwise the command will not be executed.

After the execution of a command the interface awaits the next command without the need of a new synchronization sequence. A new synchronization sequence can be performed by sending a full 'break/sync' sequence. The synchronization sequence is detected by the interface, even if another pattern is expected. After detecting a synchronization sequence, the transfer in progress is aborted and the new frame is processed.

7.3.1.1 Break field

The break field is used to indicate a new synchronization sequence. It is the only field that does not comply with the rest of the bytes. The PJF7992A is able to detect a break sequence with at least 11 bit length followed by a break delimiter. Though the PJF7992A has a break detection threshold of 11 bit the nominal break length should be 13 bit. The break delimiter must be at least one nominal bit time long (see Figure 24).

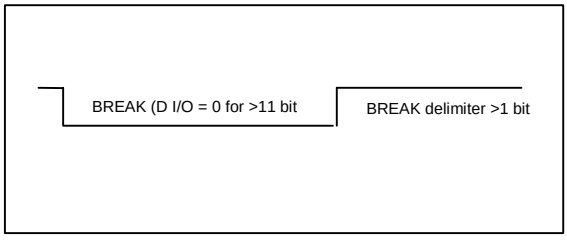


Figure 24. Single Wire break field

The length of the break field always refers to the actual bit length the device is synchronized on. In SLEEP mode or in case of a power on reset the actual bit rate is cleared and set to 20 kBd assuming a system frequency of $1/T_{SYS}$ = 4 MHz.

7.3.1.2 Synchronization field

The synchronization byte is a field with the data value 0x55, as shown in Figure 25. The synchronization field is used by the PJF7992A to adapt to the current bit rate. The PJF7992A measures the length of 8 bit from the first falling edge (start bit) to the last falling edge of the synchronization field (start of data bit 8) and divides this value by 8 to get the bit rate.

To increase synchronization integrity the PJF7992A uses the measured bit length for checking the length of the last synchronization bit (data bit 8). If the synchronization fails the PJF7992A enters a special error mode and awaits a new break/sync sequence. Furthermore the stored baudrate setting will be reset to 20 kBd if a synchronization failure occurs.

Additionally, a change of the FSEL bits will cause the stored baudrate setting to be reset to the 20 kBd value.

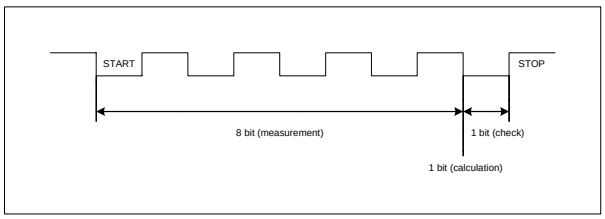


Figure 25. Single Wire Synchronization

7.3.1.3 Protected Identifier field (PID)

The protected identifier byte consists of two sub fields. The identifier (bit 0…5) and the parity(bit 6…7).

The PJF7992A features two different PIDs, one for command execution and one for entering sleep mode.

PID = 0xCF … Command PID

PID = 0x3C … SLEEP PID

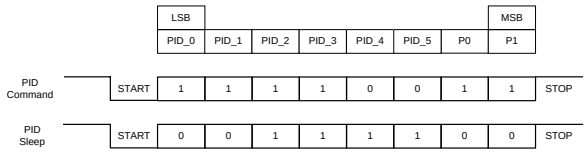


Figure 26. Single wire Protected Identifier byte

7.3.1.4 Command byte

Command bytes consist of 6 bit command code and 2 bit parity to increase data integrity.

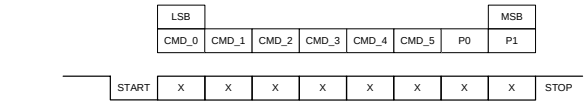


Figure 27. Single wire command byte

7.3.1.5 Data byte

Data bytes can consist of any content, dependent on the application.

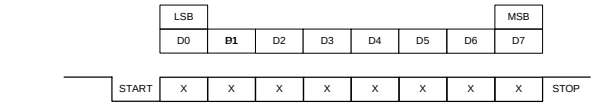


Figure 28. Single wire data byte

7.3.1.6 Checksum byte

Each byte that is exchanged between the PJF7992A and the bus master is part of the checksum calculation. The checksum calculation starts with the protected identifier field and ends with the transmission of the calculated checksum byte at the end of the command. After the transmission the checksum is cleared and a new calculation starts with 0x00.

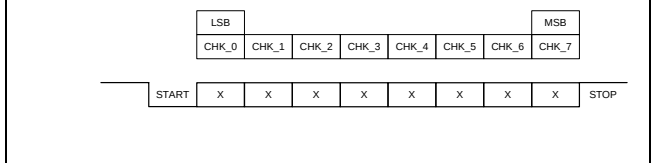


Figure 29. Single wire checksum byte

In single wire mode the checksum is handled automatically. So calculation, reset and transmission depend on the command that is executed, see 7.4.3.

For details on the checksum calculation and error handling see 7.4.

7.3.2 Single wire Operation and LIN 2.0 Compatibility

7.3.2.1 General

The PJF7992A provides a proprietary single-wire protocol. Complete LIN compatibility can be reached by implementing a system with an additional microcontroller attached to the SPI interface of the PJF7992A. This microcontroller has to handle the complete LIN protocol stack including PID and diagnosis handling. In this case the LIN interface of the PJF7992A has to be controlled via the device configuration register LINCFG.

In single-wire configuration the device is designed to be LIN ‘tolerant’ but not fully LIN compliant. The implemented single-wire protocol features some LIN compliant command structures and timings (e.g. wake-up sequence and command used for entering sleep mode). Commands and protocols used for transponder communication violate the LIN standard protocol. Despite these limitations, the device is designed for the use in LIN systems without affecting or influencing the behavior of other LIN slaves.

Every PJF7992A protocol is framed by a break-sync sequence with a dedicated fixed PID. If the PJF7992A detects commands with different PID’s it is assigned to, these commands are ignored until the next break-sync sequence with the next PID is transmitted. The wake-up sequence of the PJF7992A including all relevant timing is compliant to the LIN protocol restrictions. This implementation allows the connection of the PJF7992A to further LIN nodes without influencing the LIN communication in the LIN network.

7.3.2.2 LIN compliant / tolerant commands

The wake-up sequence with the following sync-break sequence is designed to be LIN compliant with some restrictions. Baud-rates are supported from 8 to 20 kBd and

will be adapted automatically for each protocol-frame, dependent on the received break-sync timing.

The PID of the PJF7992A is fix and cannot be configured. The usage of the PJF7992A in 'open' LIN systems with dynamic PID assignment and full LIN diagnosis features is thus not supported.

The power-down sequence is entered with a LIN compliant sleep command. Hence, the device will enter power-down mode together with all other LIN slaves connected to the same node. This feature allows synchronous wake-up and power-down mode of all LIN slaves in the respective network.

Another possibility to enter power-down mode is a watchdog overflow. For this, the watchdog period should be set to T_{WTD_0} seconds (see LIN 2.0).

7.3.2.3 LIN violations

All transponder communication commands (buffered and un-buffered communication) are not LIN compliant. The buffered transponder communication violates the maximum communication length of 8 consecutive bytes. The protocol (hand-shake mode with 'new byte request') is not in line with the LIN specification.

When the buffered communication mode is used, the baud-rate used on the LIN bus should be double the baud-rate used for transponder communication, since only one data-byte can be buffered by the PJF7992A. If transponders of the HITAG2 (PCF7936), HT2-Extended (PCF7937) or HT-Pro (PCF7939) families are used, the baud-rate on the LIN bus has to be at least 9 kBaud. (transfer of 10bits per byte + data-request + idle-time).

The un-buffered communication violates protocol length and protocol timing. In this case the communication on the LIN bus is the transparent data stream as it is exchanged with the transponder. Protocol and timing on the LIN bus is the same as used by the transponder.

7.4 Serial interface data integrity

Several structures are implemented to increase the data integrity.

7.4.1 Parity

The protected identifier and command bytes are secured by two parity bits. Each PID or command byte consists of 6 bits data and 2 bits parity. The parity calculation is done in the following manner.

$P0 = BIT0 \oplus BIT1 \oplus BIT2 \oplus BIT4$

$P1 = \neg(BIT1 \oplus BIT3 \oplus BIT4 \oplus BIT5)$

The parity calculation works independent from the serial interface mode and is active in single wire mode as well as in SPI mode.

7.4.2 Checksum

The PJF7992A calculates the checksum for each byte that is transmitted via the serial interface. The checksum is thus available in single wire mode as well as in SPI mode.

7.4.2.1 Checksum calculation

The calculation of the checksum is done by addition of each received or sent byte to the current checksum. The overflow is checked and added afterwards to the result.

The algorithm of the checksum calculation is described at the example of a WR_SCFG command in single wire mode.

Considering a device in idle condition, the following sequence has to be executed:

BREAK → SYNC → PID → CMD*(WR_SCFG DCON0)* →

→ DATA → CHECKSUM

The data bytes for the checksum calculation are assumed to be:

PID … 0xCF

CMD … 0x20

DATA … 0x55

The related checksum calculation is illustrated in Table 20.

Table 20 Checksum calculation example

	hex	***CY***	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0xCF	0x0CF	*0*	1	1	0	0	1	1	1	1
+0x20	0x020	*0*	0	0	1	0	0	0	0	0
Sum	**0x0EF**	***0***	**1**	**1**	**1**	**0**	**1**	**1**	**1**	**1**
+0x55	0x055	*0*	0	1	0	1	0	1	0	1
Sum	**0x144**	***1***	**0**	**1**	**0**	**0**	**0**	**1**	**0**	**0**
+carry	0x001	*0*	0	0	0	0	0	0	0	1
Sum	**0x045**	***0***	**0**	**1**	**0**	**0**	**0**	**1**	**0**	**1**
Inv	**0x0BA**		**1**	**0**	**1**	**1**	**1**	**0**	**1**	**0**

The calculated checksum corresponds to the Sum value displayed in the second last row. The Inv value shown in the last row is the inverted value of the calculated checksum and in general suitable for single wire mode only.

7.4.2.2 Checksum handling

The handling of the checksum value as well as the checksum error handling depends on the interface mode.

In single wire mode the calculation, transmission and initialization of the checksum value is done automatically by

the PJF7992A (see command description for more details). It has to be considered that in single wire mode the protected identifier byte is part of the checksum calculation (enhanced checksum) and that the inverted calculated checksum is transmitted. The master should perform an XOR operation of the received value and of the calculated value whereas the result must be 0xFF to prove the consistency of the received frame.

The only command that transmits a checksum to the PJF7992A is the write command WR_SCFG in single wire mode. Using this command, the inverted calculated checksum Inv has to be transmitted to the PJF7992A. The PJF7992A performs an XOR operation of the calculated checksum and of the received checksum whereas the result must be 0xFF to prove the consistency of the transmitted frame.

For all other commands in single wire mode, the PJF7992A transmits the inverted checksum at the end of each command, respectively.

In SPI mode the checksum value is not transmitted via the SPI interface, but is accessible via register CHKSUM (0xCh). Initialization, reading and handling of the checksum value in SPI mode is up to the application.

In order to initialize the checksum value in SPI mode, the command CLRCHKSUM has to be executed. After this command the checksum value (register CHKSUM) is set to 0.

In order to read the checksum value in SPI mode, a read access to register CHKSUM has to be performed. The corresponding command byte (RD_SCFG command corresponding to 0x9C) will not be added to the PJF7992A checksum value.

7.4.2.3 Checksum error handling

The only command that transmits a checksum to the PJF7992A is the write command WR_SCFG in single wire mode. Therefore a checksum error can be caused by this command only in case a wrong checksum is transmitted to the PJF7992A. A checksum error is indicated by the bit SWCS, which consequently is available in single wire mode only.

In SPI mode, the checksum error handling is with the application.

7.4.3 Frame error detection

A frame error is indicated by the corresponding bit SWFRM and is available in single wire mode only.

The frame error detection checks each data frame for correct timing of start bit (must be low) and stop bit (must be high).

7.4.4 Response error detection

A response error is indicated by the bit SWRES and is available in single wire mode only.

The response error detection checks for each bit the PJF7992A is transmitting that the LIN line has the correct state. The LIN line is checked in the middle of each bit.

In case a response error occurs the PJF7992A terminates the actual transmission, the LIN transceiver switches to recessive state and the corresponding bit SWRES is set. A response error can occur due to a bus collision in case another LIN node is transmitting at the same time or if the LIN line has a short cut to VBAT or ground.

7.5 Command Set

All commands are applicable in SPI mode as well as in Single-Wire mode (Table 21). The differences are indicated in the diagrams. The only exception is the command CLRCHKSUM that is applicable in SPI mode only.

Table 21 Command overview

Command	Coding [hex]	Coding [binary]	Description
WR_CFG	0xF0	11110000b	Write 1-n configuration registers
RD_CFG	0xB1	10110001b	Read 1-n configuration registers
WR_SCFG	0xXX	xx10xxxxb	Write one configuration register
RD_SCFG	0xXX	xx01xxxxb	Read one configuration register
WR_BUF	0xC1	11000001b	Buffered transponder com. (write only access)
WR_RD_BUF	0x49	01001001b	Buffered transponder com. (read after write access)
WR_TAG	0x03	00000011b	Transparent transponder com. (write only access)
RD_TAG	0xC4	11000100b	Transparent transponder com. (read only access)
WR_RD_TAG	0x85	10000101b	Transparent transponder com. (read after write access)
CLRCHKSUM		11001111b	Clear checksum

Note 1: The command coding includes the parity bits.

Note 2: The coding of the commands WR_SCFG and RD_SCFG depends on the destination address (see chapter 7.6)

7.6 Device configuration

7.6.1 Principle

For device configuration several commands for read and write access to the registers are available.

7.6.2 Device configuration commands

7.6.2.1 Write Configuration Register

The command WR_CFG [0xF0h] provides write access to several registers. The first parameter of the command is the address information. The higher nibble contains the end address and the lower nibble the start address of the write access. All registers from the start address to the end address are written. The checksum is calculated by the PJF7992A and sent to the master after the last data byte has been received.

Note: Registers 0x0, 0x1 and 0x2 can be written by the 'WR_SCFG' command only.

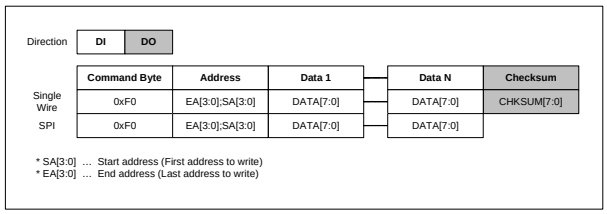


Figure 30. Write configuration register

Example

Write RCON0 = 0x0C
Write RCON1 = 0x10
Write PHMEAS = 0x00 (register not writeable)
Write SMPLC = 0x2A

Table 22 Example 'WR_CFG' – SPI mode

Cmd	Adr	RCON0	RCON1	PHMEAS	SMPLC
0xF0	0x63	0x0C	0x10	0x00	0x2A

Table 23 Example 'WR_CFG' – single wire mode

Break	Sync	PID	Cmd	Adr	RCON0	RCON1	PHMEAS	SMPLC	CHK SUM
	0x55	0xCF	0xF0	0x63	0x0C	0x10	0x00	0x2A	0xAB

7.6.2.2 Read Configuration Register

The command RD_CFG [0xB1h] provides read access to several registers. The command works in the same manner as the command 'WR_CFG', see 7.6.2.1.

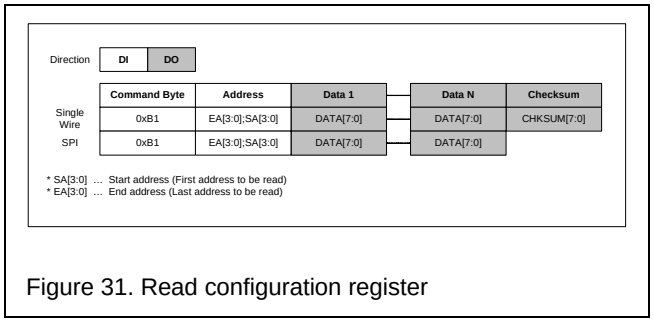


Figure 31. Read configuration register

Example

Read RCON0 = 0x0C
Read RCON1 = 0x10
Read PHMEAS = 0x15
Read SMPLC = 0x2A

Table 24 Example 'RD_CFG' – SPI mode

Cmd	Adr	RCON0	RCON1	PHMEAS	SMPLC
0xF0	0x63	0x0C	0x10	0x15	0x2A

Table 25 Example 'RD_CFG' – single wire mode

Break	Sync	PID	CMD	Adr	RCON0	RCON1	PHMEAS	SMPLC	CHK SUM
	0x55	0xCF	0xF0	0x63	0x0C	0x10	0x00	0x2A	0xAB

7.6.2.3 Write Single Configuration Register

The command WR_SCFG [0xXXh] provides fast write access to a single register. The second nibble of the command contains the destination address. For this command the calculated checksum has to be sent to the PJF7992A and is verified for successful write access. If the received checksum is incorrect the write access to the destination register is not executed and the corresponding error bit SWCS is set.

Note: Registers 0x0, 0x1 and 0x2 can be written by this command only.

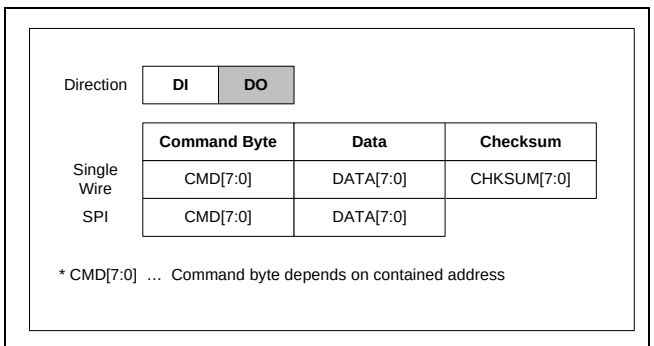


Figure 32. Write single configuration register

Table 26 Coding of 'WR_SCFG' command

Reg	Addr	P1	P0	C5	C4	C3	C2	C1	C0	HEX
DCON0	0x0	0	0	1	0	0	0	0	0	0x20
DCON1	0x1	0	1	1	0	0	0	0	1	0x61
LINCFG	0x2	1	1	1	0	0	0	1	0	0xE2
RCON0	0x3	1	0	1	0	0	0	1	1	0xA3
RCON1	0x4	0	1	1	0	0	1	0	0	0x64
PHMEAS	0x5	0	0	1	0	0	1	0	1	0x25
SMPLC	0x6	1	0	1	0	0	1	1	0	0xA6
TXCON	0x7	1	1	1	0	0	1	1	1	0xE7
DRVCON	0x8	1	0	1	0	1	0	0	0	0xA8
COMCON	0x9	1	1	1	0	1	0	0	1	0xE9
STATUS	0xA	0	1	1	0	1	0	1	0	0x6A
BCDAT	0xB	0	0	1	0	1	0	1	1	0x2B
CHKSUM	0xC	1	1	1	0	1	1	0	0	0xEC

Example

Write DCON1 = 0x40

Table 27 Example 'WR_CFG' – SPI mode

Cmd	DCON1
0x61	0x40

Table 28 Example 'WR_CFG' – single wire mode

Break	Sync	PID	Cmd	DCON1	CHK SUM
	0x55	0xCF	0x61	0x40	0x8E

7.6.2.4 Read Single Configuration Register

The command RD_SCFG [0xXXh] provides fast read access to a single register. The second nibble of the command byte contains the address of the register for the read access.

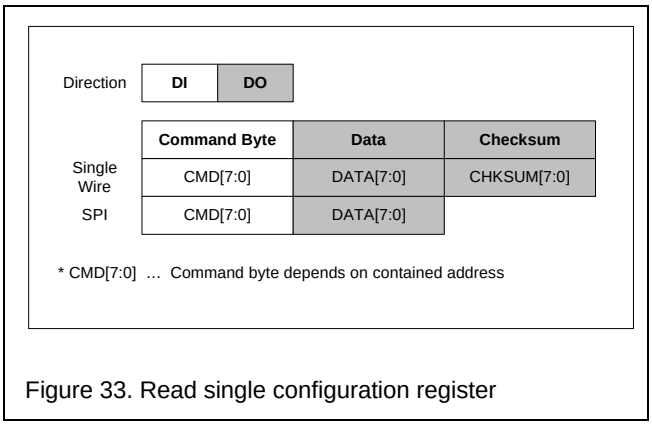


Figure 33. Read single configuration register

Table 29 Coding of 'RD_SCFG' command

Reg	Addr	P1	P0	C5	C4	C3	C2	C1	C0	HEX
DCON0	0x0	0	1	0	1	0	0	0	0	0x50
DCON1	0x1	0	0	0	1	0	0	0	1	0x11
LINCFG	0x2	1	0	0	1	0	0	1	0	0x92
RCON0	0x3	1	1	0	1	0	0	1	1	0xD3
RCON1	0x4	0	0	0	1	0	1	0	0	0x14
PHMEAS	0x5	0	1	0	1	0	1	0	1	0x55
SMPLC	0x6	1	1	0	1	0	1	1	0	0xD6
TXCON	0x7	1	0	0	1	0	1	1	1	0x97
DRVCON	0x8	1	1	0	1	1	0	0	0	0xD8
COMCON	0x9	1	0	0	1	1	0	0	1	0x99
STATUS	0xA	0	0	0	1	1	0	1	0	0x1A
BCDAT	0xB	0	1	0	1	1	0	1	1	0x5B
CHKSUM	0xC	1	0	0	1	1	1	0	0	0x9C

Example

Read DCON1 = 0x40

Table 30 Example 'RD_SCFG' – SPI mode

Cmd	DCON1
0x11	0x40

Table 31 Example 'rd_scfg' – single wire mode

Brk	Syn	PID	Cmd	DCON1	CHK SUM
	0x55	0xCF	0x11	0x40	0xDE

7.6.2.5 Clear Checksum

The command CLRCHKSUM [0xCFh] is provided to clear the checksum register in SPI mode. In single wire mode the checksum is handled and cleared automatically.

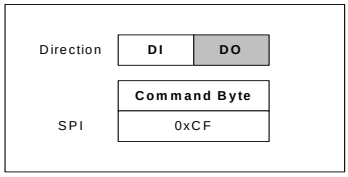


Figure 34. Clear Checksum command

7.7 Buffered transponder communication

7.7.1 Principle

In buffered communication mode, an internal data buffer is used to send and receive transponder data in order to relax the real-time processing requirements of the controlling microcontroller. The buffered mode is available in SPI and single wire configuration.

The buffered communication employs an 8-bit buffer and a shift register to ensure a continuous bit stream to and from the transponder. The handling of the buffered communication depends on the interface mode (SPI or single wire).

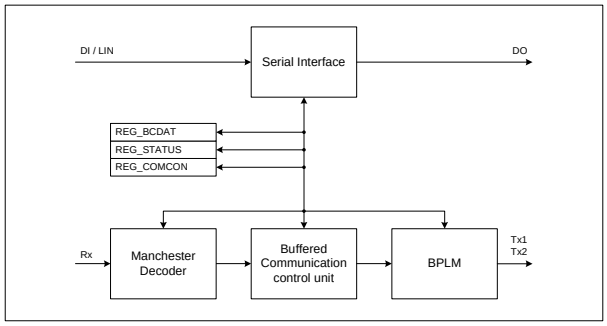


Figure 35. Buffered communication block diagram

The buffered transponder communication is controlled by a set of registers (Table 32).

Table 32 Buffered communication control registers

Reg	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
COMCON	*RFU*	**MDPOL**	**RFU**	**MODE**	**MPW3**	**MPW2**	**MPW1**	**MPW0**
STATUS	**STAT**	**BFP_2**	**BFP_1**	**BFP_0**	**BFLB**	**BFPR**	**RDY**	**DREQ**
BCDAT	**BCD_7**	**BCD_6**	**BCD_5**	**BCD_4**	**BCD_3**	**BCD_2**	**BCD_1**	**BCD_0**

MDPOL	Manchester decoder polarity configuration. By setting this bit the polarity of the Manchester decoder input signal will be inverted.
MODE	Manchester decoder mode configuration. 0 … 2 edge sensitive decoding mode 1 … 1 edge sensitive decoding mode
MPW[3 :0]	Modulation pulse timer pulse width configuration, see 6.9.1
DREQ	Data request status signal. Is used in buffered communication to indicate the reception or transmission of a full byte.
RDY	Ready status signal that indicates the end of a buffered write sequence and a waiting condition of the device while waiting for the transponder response.
BFPR	Bitfail indication for bitfail at a location before the last received byte.
BFLB	Bitfail indication for bitfail at a location in the last received byte
BFP[2:0]	Bifail position indicator that indicates the bit position of a bitfail in the last received byte.
STAT	Status bit that indicates a buffered communication sequence. This bit is set while a buffered write or a buffered read sequence is ongoing. By clearing this bit a running communication is finished and the corresponding blocks (Manchester decoder, binary pulse length modulator) are initialised.

7.7.2 Manchester Decoder

For buffered communication the device features an implemented Manchester decoder. The decoded data are stored in the BCDAT register or transmitted immediately after reception depending on the interface mode.

The internal state machine controls the Manchester decoder. The decoder is enabled after the settling sequence of the WR_RD_BUF command automatically. The timing is designed for the transponder families HITAG2, HT2-Extended and HT-Pro where the decoder synchronizes to the data stream using the last bit in the start bit sequence of the transponder response. Manual adaptation of the timing as well as manual control of the decoder is not supported.

The Manchester decoder is able to work in two different modes that can be configured by the bit MODE in register COMCON. By setting this bit the decoder is switched from a 2-edge sensitive decoder to a 1-edge sensitive decoder. The 2-edge sensitive decoder mode should be preferred because only for this mode the bitfail location structure works without the inaccuracy of 1 bit, see 7.7.5.

In case of a missing transponder response, at low noise levels the activated Manchester decoder of the PJF7992A is not synchronized and no data output is available. Later synchronization by noise leads to a delayed availability of data (LIN: data stream, SPI: DREQ bit).

In case of a decoder error, the PJF7992A generates a stream of 0 bits.

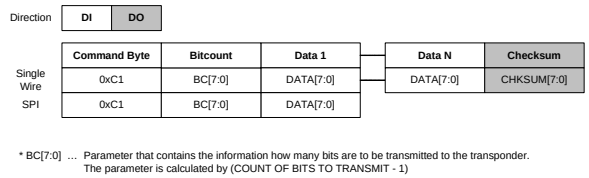
Further it is possible to switch the polarity of the Manchester decoder input signal. The effect is the same as to change the sample & hold timing by 180°.

7.7.3 Buffered communication commands

The structure of this communication mode depends on the serial interface mode. In single wire mode the communication protocol is fixed while in SPI mode the application software has to serve correct data and timing by reading status bits and writing the data register (BCDAT).
Two commands are available to perform a buffered communication sequence. It is possible to execute a write only or a write with automatic switch to read sequence.

7.7.3.1 Write Buffered

The command WR_BUF [0xC1] provides buffered write access to the transponder data.



* BC[7:0] … Parameter that contains the information how many bits are to be transmitted to the transponder. The parameter is calculated by (COUNT OF BITS TO TRANSMIT - 1)

Figure 36. Write buffered command

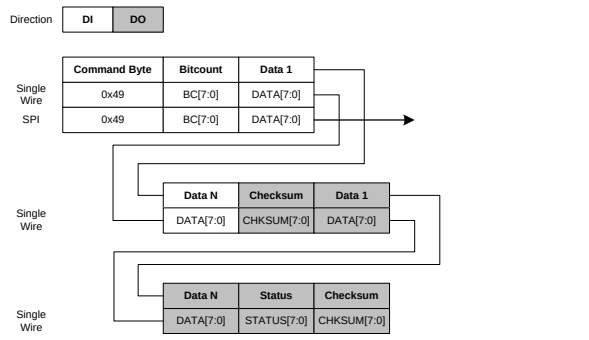
The PJF7992A needs information of the count of bits to transmit to the transponder. The 'Bitcount' parameter contains this information. The parameter is calculated in the following manner.

BITCNT = Bits to send – 1

For details to the different phases of the buffered communication sequence see 0.

7.7.3.2 Write and Read Buffered

The command WR_RD_BUF [0x49] provides buffered write and subsequent read access to the transponder data.



* BC[7:0] … Parameter that contains the information how many bits are to be transmitted to the transponder. The parameter is calculated by (COUNT OF BITS TO TRANSMIT - 1)
*STATUS[7:0] … Content of the STATUS register is transmitted automatically at the end of each wr-rd-procedure (only in single wire mode)

Figure 37. Write and read buffered command

The write sequence has to be initiated in the same manner as it is for the 'WR_BUF' command, see 7.7.3.1.

For details to the different phases of the buffered communication sequence see 0.

7.7.4 Buffered communication sequence

A full buffered communication sequence consists of 4 sub sequences (see Figure 38 and Figure 39).

It starts with the command sequence that initiates the buffered communication state machine and prepares all necessary data for start of the write procedure. After reception of the bit count information and the first data byte the state machine starts modulating the field to transmit the data to a transponder in field.

In the write sequence the application has to serve the PJF7992A with the correct data to keep up a continuous communication to the transponder. After transmitting the count of bits given in the bitcount parameter the PJF7992A transmits a final stop bit and changes into the settling sequence.

During the settling sequence the automatic fast settling sequence of the receiver is performed. After the settling sequence the device switches into the read sequence automatically. The application has to wait for the end of the settling sequence.

In the read sequence an internal Manchester decoder decodes the response of the transponder. The data are stored in the BCDAT register or transmitted immediately after decoding depending on the serial interface mode. The end of the read sequence has to be triggered by the application. The way of finishing the sequence depends on the interface mode (see chapter 7.7.4.1 and 7.7.4.2).

7.7.4.1 SPI mode

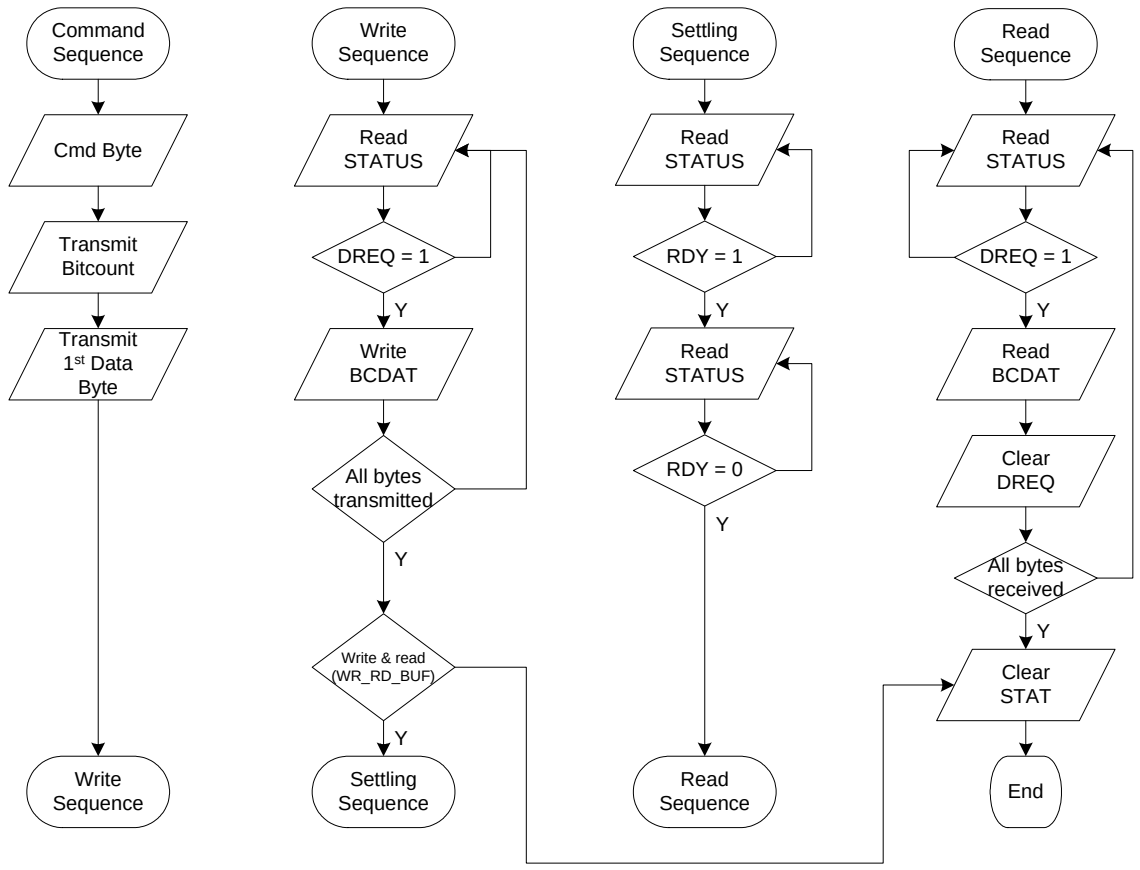


Figure 38. Buffered communication sequence – SPI mode

The Command sequence is identical for both interface modes. The command byte followed by the bitcount parameter and first data byte has to be transmitted to the PJF7992A. After reception of the first data byte the PJF7992A starts modulating the LF-field to transmit the data to a transponder in field.

In the write sequence the application has to read the STATUS register periodically and check the data request bit DREQ. If a data request is indicated the next data byte must be written to the BCDAT register. The data request STATUS bit DREQ is cleared automatically when the data byte is written to the BCDAT register.

When the PJF7992A has transmitted the last bit to the transponder it sends an additional stop bit and changes into the settling sequence by setting the status bit RDY. The status bit RDY is kept ‘1’ by the PJF7992A as long as the device is waiting for the transponder response. During this time the ‘Fast settling sequence’ of the receiver is executed to prepare the device for receiving of the transponder response. The application can monitor the status of the settling sequence by reading the STATUS bit RDY.

When the device starts with the read sequence it clears the RDY bit and enables the internal Manchester decoder for decoding of the Manchester coded transponder response. Every time a full byte has been decoded it is stored in the BCDAT register and the DREQ bit is set by the PJF7992A. Hence the application has to read the STATUS register periodically. In case the DREQ bit is set the application has to read the BCDAT register and clear the DREQ status bit by writing a ‘1’ to the corresponding bit location of the STATUS register. Additionally the bitfail information contained in the STATUS register must be evaluated by the application to ensure a correct data byte.

When the application has received the expected count of data bytes the buffered communication sequence has to be finished by clearing the status bit STAT in the STATUS register. By clearing this bit all other status bits in this register are cleared to.

7.7.4.2 Single wire mode

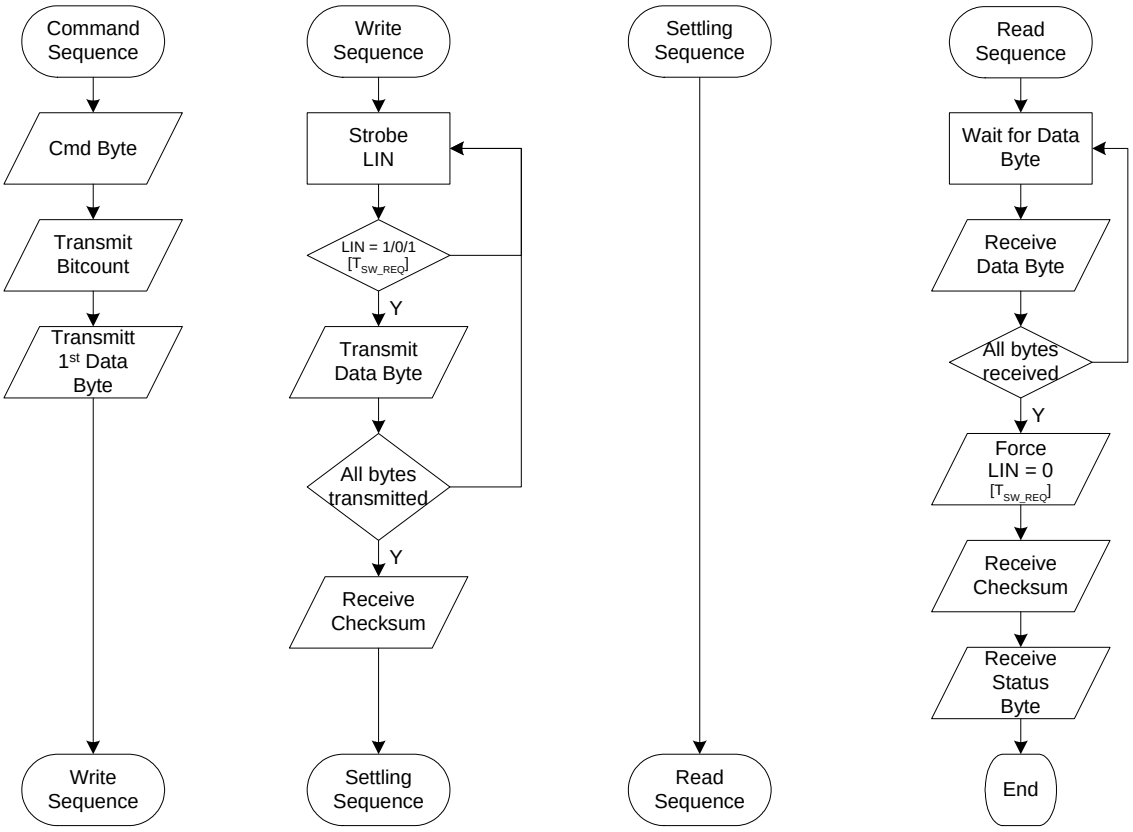


Figure 39. Buffered communication sequence – LIN mode

In single wire mode the handling of the buffered communication sequence is different because of a fixed flow controlled by an internal state machine.

The Command sequence is identical for both interface modes. The command byte followed by the bitcount parameter and first data byte has to be transmitted to the PJF7992A. After reception of the first data byte the PJF7992A starts modulating the LF-field to transmit the data to a transponder in field.

During the write sequence the application has to strobe the LIN line for a low pulse with a length of T_{SW_REQ}. This low pulse on the LIN line indicates a data request and the bus master has to serve the data in time to keep up a continuous data stream to the transponder. The end of the write sequence is indicated by the PJF7992A by transmitting the calculated checksum of the write procedure.

After the checksum has been transmitted the PJF7992A performs the automatic settling sequence of the receiver and waits for the transponder response.

The read sequence starts automatically by enabling the internal Manchester decoder. Every time a complete data byte has been decoded it is transmitted via the LIN line immediately. In multiple slave applications the bus master has to ensure that the LIN network is not occupied by another communication. During the whole read sequence the bus master must be sensitive for receiving the decoded data bytes.

After receiving all expected data bytes the bus master must finish the read sequence by forcing the LIN line to ‘0’ (dominant) for T_{SW_REQ} immediately after the last data byte has been received. If the PJF7992A detects the end trigger for the read sequence it transmits the last two bytes containing the checksum of the read sequence and the STATUS register. After that the buffered communication is finished without any additional settings necessary.

7.7.5 Bitfail structure

The bitfail information in the STATUS register indicates corrupt Manchester code in the received data. If a bitfail occurs the Manchester decoder enters an error state and does not decode data anymore. Nevertheless the Manchester decoder is still clocked meaning the data stream will continue while the data content is '0' for each bit. The usage of the bitfail information depends on the serial interface mode.

7.7.5.1 SPI mode

In SPI mode the STATUS register is polled regularly and the bitfail information can be evaluated for each byte immediately after reception. Therefore the application software can check for a bitfail in the last byte by evaluating the bit BFLB. If a bitfail is indicated (BFLB=1) the location of the bitfail is indicated by the bits BFP[2:0] which contain the binary coded information of the bitfail position.

7.7.5.2 Single wire mode

In single wire mode the content of the STATUS can only be read after the complete buffered read sequence is finished. Therefore the application does not have any information on bit failures after receiving a data byte via the LIN line.

To evaluate the bitfail information in the STATUS register, transmitted after the read sequence, the application has to check the BFPR bit first. If this bit indicates a bitfail at a location before the last received byte, a bit failure inside the significant data stream has occurred. It is up to the application to repeat the complete communication.

If the BFPR bit is not set the application has to check the BFLB bit for a bitfail in the last received byte. If a bitfail in the last byte is indicated, the bit location of the failure is available by evaluating the content of BFP[2:0] which contain the bitfail position in binary coded manner. With this information the application is able to identify a bitfail inside the significant data stream.

Note – Manchester Decoder Mode
The exact bitfail location (BFL bits) is determined only for Manchester Decoder in 2 edge sensitive decoding mode (MODE bit in COMCON register). For the 1 edge decoding mode an inaccuracy of the bitfail location of 1 bit has to be taken into account.

7.8 Transparent transponder communication

7.8.1 Principle

In transparent mode, the DI, DO or LIN line provides direct control over the antenna driver and direct access to the demodulated receive signal, compatible to the implementation of the PCF7991. In addition commands are incorporated that automatically switches from transponder WRITE state to READ state (WR_RD_TAG) and that feature auto settling (fast settling sequence) of the receiver circuitry (Figure 40).

Before a transparent communication can be performed the antenna driver has to be switched on by setting the corresponding bit (ACT).

The transparent communication sequence is entered by certain commands. A write command (WR_TAG, WR_RD_TAG) sets the IC in transparent write condition. A synchronization sequence (single wire) or CSN = 1 (SPI) can end a transparent write or read procedure. Without a synchronization sequence the write procedure ends in the command state awaiting the next command after LIN/DI = 1 for T > 0.5ms.

In order to relax the timing needs for the controlling device a special form of transparent communication is available by using the 4 configuration bits MPW[3:0] in register COMCON. If these configuration bits are different from 0, the controlling device will trigger the start of antenna field modulation, while the MPW bits define the duration of the modulation.

If the configuration setting is 0 then the interface is working in full transparent mode where the controlling device gives via LIN/DI the exact timing (beginning and duration) of the antenna field modulation.

The command WR_RD_TAG sets the interface into transparent write mode and switches directly into transparent read mode when the writing procedure is finished. The end of the writing process is indicated by LIN/DI = 1 for T > 0.5ms. In this case the internal state machine controls the fast settling sequence.

The transparent read mode can only be left by performing a synchronization sequence (single wire mode) or by setting CSN = 1 (SPI mode).

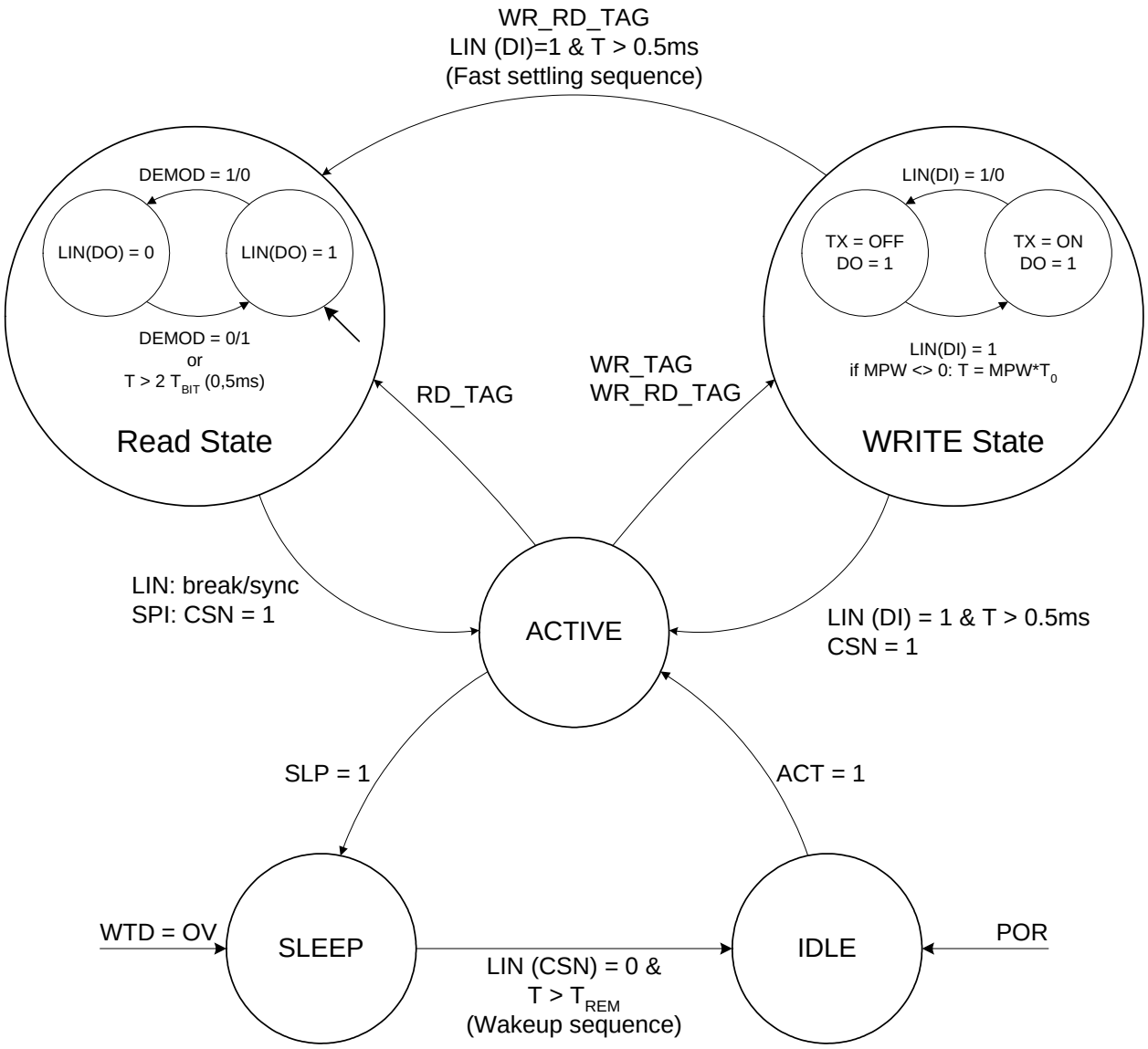


Figure 40. Transparent communication flow chart

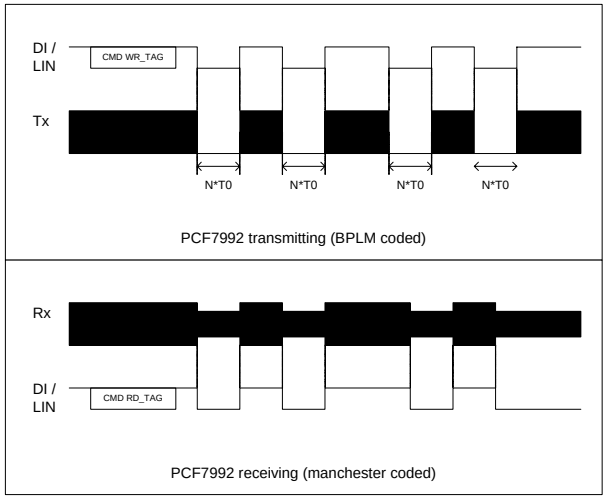


Figure 41. Transparent communication timing

N … 4 bit configuration value MPW<3:0>
T0 … 8µs

7.8.2 Transparent communication commands

7.8.2.1 Write Tag

The command WR_TAG [0x03h] sets the device into transparent write mode. This mode gives transparent write access to a transponder located in the LF-field.

After a timeout period of > 0.5ms (LIN/DI=1) the serial interface is ready to receive the next command. In SPI mode the CSN line must be low for the whole communication sequence. Releasing the CSN line (CSN = 1) terminates the command immediately.

Direction: DI | DO

	Command Byte	Transparent write mode
Single Wire	0x03	Binary Phase Length modulated data
SPI	0x03	Binary Phase length modulated data

Figure 42. Write Tag command structure

7.8.2.2 Read Tag

The command RD_TAG [0xC4h] sets the device into transparent read mode.

In single wire mode a new synchronization sequence (break/sync) finishes the transparent read mode.

In SPI mode the CSN line must be low for the whole communication sequence. Releasing the CSN line (CSN = 1) terminates the transparent read mode.

Direction: DI | DO

	Command Byte	Transparent read mode
Single Wire	0xC4	Manchester coded data from Transponder
SPI	0xC4	Manchester coded data from Transponder

Figure 43. Read Tag command structure

7.8.2.3 Write and Read Tag

The command WR_RD_TAG: [0x85h] sets the device into transparent write mode and automatically change to transparent read mode after the write mode is finished.

The device switches from transparent write to read mode if the data line (DI or LIN) is idle for at least 0.5 ms.

The procedure to finish the following read mode depends on the interface mode.

In single wire mode a new synchronization sequence (break/sync) finishes the transparent read mode.

In SPI mode the CSN line must be low for the whole communication sequence. Releasing the CSN line (CSN = 1) terminates the transparent read mode.

Direction: DI | DO

	Command Byte	Transparent write mode
Single Wire	0x85	Binary phase length modulated data to transponder @ LIN
SPI	0x85	Binary phase length modulated data to transponder @ DI

Transparent read mode
Manchester coded data from transponder @ LIN
Manchester coded data from transponder @ DO

Figure 44. Write and read Tag command structure

8 LIMITING VALUES

All values are in accordance with Absolute Maximum Rating System (IEC 134)

PARAMETER	MIN	MAX	UNIT
Operating temperature range	-40	+85	°C
Storage temperature range	-55	+125	°C
Virtual junction temperature	-40	+150	°C
Supply Voltage (IOREF)	-0.3	5.5	V
Voltage at any digital I/O pin	-0.3	V_{IOREF} + 0.3	V
Voltage at XTAL1	-0.3	3.5	V
Voltage at pin TX1 and TX2	-0.3	5.5	V
Voltage at pin VRC1 and VRC2	-0.3	5.5	V
Voltage at pin RX, Note 1	-120	+120	Vp
Supply Voltage at pin VB (t < 400ms)	-0.3	40	V
Voltage at pin LIN	-27	40	V
Latch-up current, Note 2	100		mA
ESD, human body model, Note 3	2		kV
ESD, human body model for pins V_{BAT} and V_{SS}, Note 3	4		kV
ESD, human body model for LIN pin	8		kV
ESD, machine model, Note 4	200		V
Transient voltage on pin LIN, $V_{trt(LIN)}$ (ISO7637)	-150	100	V
Power dissipation, Note 5		1.4	W
$R_{th(j-a)}$ Note 6	46		K/W
$R_{th(j-c)}$ Note 7	34		K/W

Notes

1. Voltages >100Vp may lead to ‘deep-snap-back’ of the implemented ESD protection devices, in case of a ‘snap-back’ event the voltage on the RX pin will be clamped to 10Vp. The effect is reversible when the applied voltage on RX is removed.
2. According to JEDEC, JESD 17
3. According to JEDEC, JESD 22-A114
4. According to JEDEC, JESD 22-A115
5. Dependent of the thermal coupling between package and PCB, air flow and Virtual junction Temperature
6. Dependent of the thermal coupling between package and PCB, simulated value for JEDEC Test Card: 4-Layer, 4 x 4.5" with 2 ground planes; @ 0 m/s air flow
7. Dependent of the thermal coupling between package and PCB, simulated value for Junction to case, if case is connected to an infinite heat sink PCB area, @ 0 m/s air flow

The product lifetime is qualified according to AEC Q100 for automotive grade 3: -40°C to +85°C ambient operating temperature range. Lifetime tests were performed with a virtual junction temperature of 150°C over 1000h. Calculation of failure rates and performance levels are determined for a given junction temperature of 70°C as determined from SHTL/DHTL test results; the life prediction of 10 years reflecting an Arrhenius activation energy of 0.7eV at a 60% confidence level. If the device is operated constantly at higher temperatures the lifetime prediction will decrease accordingly until a limit of 1000h at a constant operating junction temperature of 150°C.

9 ELECTRICAL CHARACTERISTICS

9.1 Operating Conditions

Tamb = -40 to +85°C, V_B = 12V, V_{SS} = 0V, unless otherwise specified

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
V_B	Battery supply voltage, Note 1		6.0		27	V
I_B	Supply current	I_{TX} = 0		3.5	7	mA
$I_{B,IDLE}$	- IDLE	XTAL and digital part running		1.5	5	mA
$I_{B,SLEEP}$	- SLEEP			55	100	uA
Temperature Shutdown						
T_{SHD}	Temperature Shutdown threshold		150		190	°C

Notes

1. External measures for reverse battery connection must be provided.

9.2 AC/DC Characteristics

Tamb = -40 to +85°C, V_B = 12V, V_{SS} = 0V, unless otherwise specified

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
f_{osc}	Oscillator frequency		4		16	MHz
f_c	Carrier frequency			125		kHz
T_0	Carrier period			8		µs
Voltage Regulator 1, C_{EXT} = 22µF						
$V_{VRC1,HI}$	Maximum Output Voltage	AVR[3:0]=0000b	4.1	4.7	5.1	V
$V_{VRC1,LO}$	Minimum Output Voltage	AVR[3:0]=1111b	1.6	2	2.3	V
$V_{VRC1,step}$	Voltage between two consecutive steps		150	190	240	mV
I_{VRC1}	Maximum external load current	Current delivered to external circuitry, Note 1			20	mA
C_{VRC1}	Required Load Capacitor	On pin VRC1	18	22	27	µF
C_{VRC1P}	Recommended parallel Load Capacitor (EMC performance)	On pin VRC1	47	100	150	nF
	Ripple rejection	20 LOG (V_{DD-AC} / V_{B-AC}) f = 10Hz to 10kHz			45	dB
		20 LOG (V_{DD-AC} / V_{B-AC}) f = 10Hz to 1MHz			29	dB
δV_{BAT1}	Supply voltage regulation	VBAT = 6V to 27V	-10		90	mV
δV_{IL1}	Load regulation	OOK of TX, I_{TX} = 100mA			200	mV
Voltage Regulator 2, C_{EXT} = 220nF						
V_{VRC2}	Output Voltage		4.1	4.7	5.1	V
I_{VRC2}	Maximum external load current	Current delivered to external circuitry, Note 2			0.5	mA
C_{VRC2}	Required Load Capacitor	On pin VRC2	180	220	270	nF
	Ripple rejection	20 LOG (V_{DD-AC} / V_{B-AC}) f = 10Hz to 10kHz			55	dB
		20 LOG (V_{DD-AC} / V_{B-AC}) f = 10Hz to 1MHz			39	dB
δV_{BAT2}	Supply voltage regulation	VBAT = 6V to 27V	-10		50	mV
δV_{IL2}	Load regulation	Operation of RX, I_{RX} = 2mA			100	mV

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Antenna Driver						
f_{TX}	Frequency			125		kHz
I_{TX}	Drive current	Peak-current, Note 3			200	mA
$R_{O,TX,GND}$	Output resistance (one driver)	95mA, Current sink, AVR[3:0] = 0000,		3.5	6.0	Ω
$R_{O,TX,VRC1}$	Output resistance (one driver)	95mA, Current source, AVR[3:0] = 0000		4.0	7.5	Ω
Receiver						
$V_{I,RX}$	Input voltage range	With respect to V_{QGND}	-100		100	V_P
V_{QGND}	Analog Ground		2.0	2.3	2.6	V
$V_{RX,SENS}$	Sensitivity	RNG = 00, Note 4		25		mV_{PP}
R_{RX}	Input resistance		120	250	400	kΩ
$f_{LP,EMI}$	EMI Low Pass cutoff frequency	3dB cutoff + range setting	160	280	400	kHz
Serial Interface						
V_{IOREF}	Supply voltage		2.7		5.5	V
$V_{IOREF,IMS}$	Interface mode select threshold		1.0	1.5	2.5	V
Interface I/O Level, pin DI, DO, CLK, CSN, TxD, RxD						
V_{OL}	Low level output voltage	(XTO, Rxd, DO – SPI mode) I_O = -1mA ; f_{XTAL} = 4MHz, 8MHz			0.4	V
V_{OL}	Low level output voltage	XTO I_O = -1mA ; f_{XTAL} = 16MHz			0,8	
V_{OH}	High level output voltage	(XTO, RxD – SPI mode) I_O = 1mA; f_{XTAL} = 4MHz, 8MHz	V_{IOREF} – 0.4			V
		XTO I_O = 1mA; f_{XTAL} = 16MHz	2			V
$V_{OH,RSTN}$	High level output voltage	Open collector pin			5.5	V
V_{IL}	Low level input voltage	(DI, CLK, CSN, TxD – SPI mode)	-0.3		0.25 V_{IOREF}	V
V_{IH}	High level input voltage	(DI, CLK, CSN, TxD – SPI mode)	0.75 V_{IOREF}		V_{IOREF} + 0.3	V
LIN Driver						
$V_{O,REC}$	Output voltage, recessive state	V_{TXD} = 5V, I_{LIN} = 0A	0.9		1.0	VB
$V_{O,DOM}$	Output voltage, dominant state	V_{TXD} = 0V; 5.5V < VB < 7V		1.0	1.5	V
		V_{TXD} = 0V; 7.0V < VB < 18V R_{VB-LIN} = 500Ω			0.2	VB
$VI_{,DOM}$	Input threshold voltage	7.0V < VB < 27V	0.4		0.6	VB

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Power On Reset						
$V_{B2,POR}$	Power On Reset threshold		3.0	5.0	6.0	V

Notes

1 External current supply: only resistive loads allowed, an external load connected to VRC1 may only draw constant current, any load current variation due to an external device will deteriorate Rx performance significantly (superimposition of the transponder load modulation)

2 External current supply: only small resistive loads allowed (e.g. control signals for switches), an external load connected to VRC2 may only draw constant current, any load current variation due to an external device will deteriorate Rx performance significantly (PSRR of the receiver path)

3 The max. drive-current I_{TX} always has to be considered together with the max. power dissipation and max. virtual junction temperature. The absolute maximum ratings shall not be exceeded.

4 Compares with ABIC, PCF7991, specification, when the increased input voltage range (+/-100V) is taken into account

9.3 Timing Characteristics

Tamb = -40 to +85°C, V_B = 12V, V_{SS} = 0V, unless otherwise specified

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
T_{REM}	Remote Bus Wake-Up pulse width		280	400	1000	µs
$T_{LIN,NOM}$	Nominal single wire bit length		50		125	µs
T_{SW_REQ}	Single wire Data request pulse width		$T_{LIN,NOM}$ – 10%	$T_{LIN,NOM}$	$T_{LIN,NOM}$ + 10%	
T_{SYS}	System clock	Note 1		250		ns
T_{WUP}	Device Wakeup time	Note 2	1	5	10	ms
T_{RST}	Device wakeup reset pulse length	T_{SYS} = 250ns	1		1.5	ms
T_{WTD_0}	Watchdog timeout period	WDMD = 0, Note 3		4.1		s
$T_{SLP,DLY}$	Watchdog SLEEP Delay timeout	WDMD = 1, Note 4		10		ms
T_{CSS}	Chip select setup time		0.4			µs
T_{CSH}	Chip select hold time		0.4			µs
T_{CLKH}	Clock high time		0.4			µs
T_{CLKL}	Clock low time		0.4			µs
T_{DIS}	Data In setup time		0.1			µs
T_{DIH}	Data In hold time		0.3			µs
T_{DOD}	Data Out delay				0.4	µs

Note 1: T_{SYS} is the system clock derived from the divided oscillator clock f_{OSC}. T_{SYS} has to be set by the FSEL bits located in the DCON0 register.

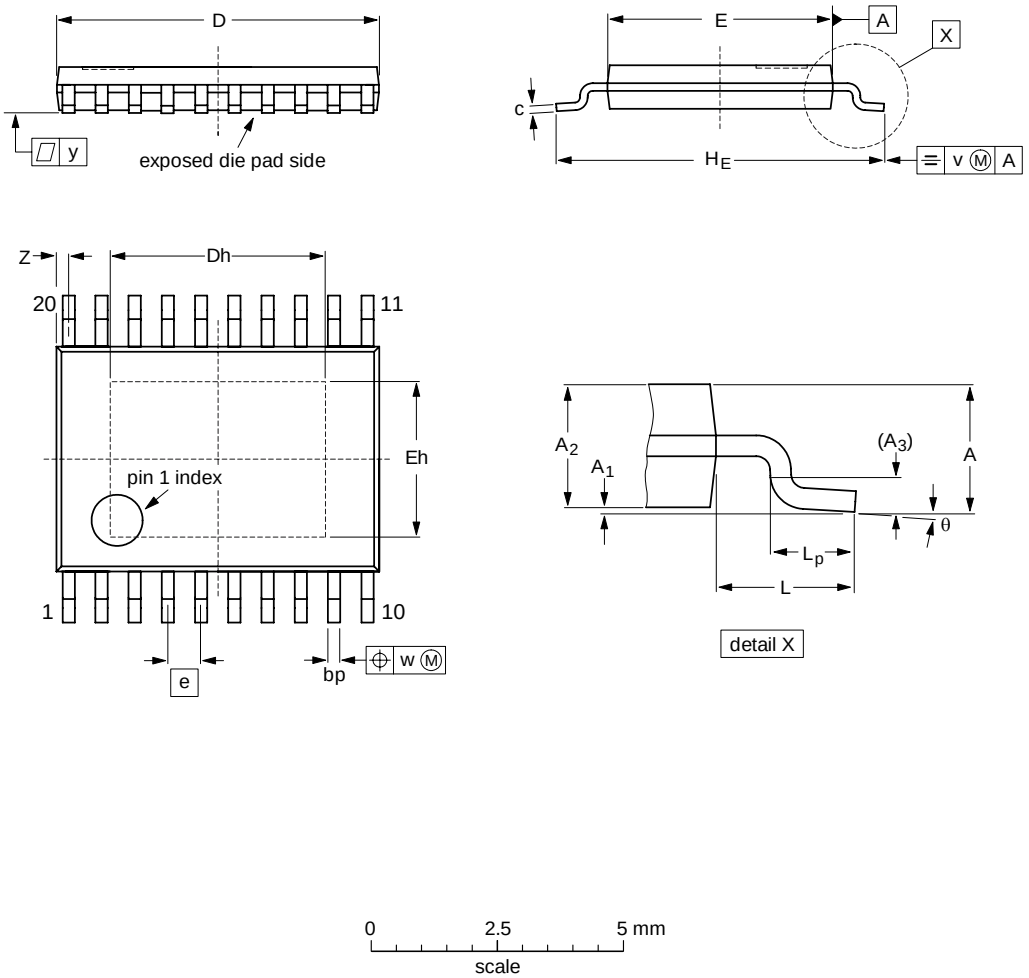
Note 2: Depending on the startup timing of the external oscillator (XTAL)

Note 3: T_{WTD_0} is derived from the divided system clock T_{SYS}. T_{WTD_0} is 16E6 times T_{SYS}.

Note 4: $T_{SLP,DLY}$ is derived from the divided system clock T_{SYS}. $T_{SLP,DLY}$ is 40E3 times T_{SYS}.

10 PACKAGE OUTLINE

HTSSOP20: plastic thermal enhanced thin shrink small outline package; 20 leads; body width 4.4 mm; exposed die pad **SOT527-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A1	A2	A3	bp	c	D(1)	Dh	E(2)	Eh	e	HE	L	Lp	v	w	y	Z(1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.20 0.09	6.6 6.4	4.3 4.1	4.5 4.3	3.1 2.9	0.65	6.6 6.2	1	0.75 0.50	0.2	0.13	0.1	0.5 0.2	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT527-1						~~03-02-18~~ 03-04-07

11 RELATED DOCUMENTS

Type	Name / Reference	Description
Application Note	ABIC 2 Application Note	Design of immobilizer basestations with the PJF7992A

12 ANOMALY NOTES

This section provides additional information concerning known anomalies discovered with the device and reports changes that are subject to implementation with future device versions.

13 REVISION HISTORY

Revision	Page	Description
29.11.2007		Editorial updates and corrections, based on Data Sheet of PJF7992M from May 14th 2007
	5	Minimum battery supply voltage for digital part changed from 5.5 to 6V
	5	Upper watchdog timeout limit changed from 4.0 s to 4.1 s to be conform to LIN 2.0
	5	Note concerning replacement of 7992M by 7992A removed
	5	Note concerning usage of resonators (crystal not allowed) added
	5	Chapter 2, usage of crystals excluded
	6	Type number changed form PJF7992MTW/B0D to PJF7992ATW/B2B
	8	Mandatory Zener Diode removed, not needed for PJF7992A
	8	Recommendation for blocking capacitor at pin IOREF in SPI mode added
	8	Type “input” added for XTAL1 and type “output” added for XTAL2
	10	Chapter 7.1 and 7.2, references to capacitors C_{VRC1} and C_{VRC2} added
	10	Bits TSHDIS, DISHPL, BDRT, HPF, LPF and TRIM changed to RFU bits
	10	PHMEAS reset values changed
	11	Bits TSHDIS, DISHPL, LPF and HPF removed (RFU bits)
	11	DCON1, bits SWCS, SWFRM and SWRES not cleared automatically after reading
	11	Bit TSHUT, access changed from Read Only to Read / Clear, reset condition changed from N.A. to P/S/R
	11	RCON1, reset conditions for Bits FRZ0 and FRZ1 changed from P to P/S/R
	12	PHMEAS, reset value changed from 000000b to 111100b
	12	Note 1 added. (reset conditions of PHMEAS)
	12	DRVCON, bit TRIM removed (RFU bit)
	12	BCDAT, Reset Conditions changed from P to P/S/R
	13	Fig 3 updated
	14	Chapter 6.4.3, condition to enter ACTIVE mode modified (temperature below T_{SHD})
	14	Chapter 6.5, remark added that a wake-up event leads to SLP = 0
	14	Chapter 6.5.1, specification of value an external pull-up resistor has to be connected to
	14	Fig 4, 5 and 6 updated
	15	Fig 8 updated
	16	Chapter 6.7, text regarding external clock source added
	16	Chapter 6.7, in Note “all” exchanged against “most”
	16	Table 5, Table 6, bit TSHDIS changed to RFU bit
	17	Chapter 6.7.1, usage of crystals excluded
	17	Chapter 6.7.2, text concerning change of FSEL added

Revision	Page	Description
	17, 18	Fig 10, Fig.11, Fig. 12, T_c replaced by T_0
	19	Table 11, Bit TRIM changed to RFU bit
	19, 21	Fig. 13, Fig. 16,VDD replaced by VRC2
	20	Chapter 6.9.4.2, Automatic Drive Voltage Adjustment removed
	21	Table 14, Bits HPF and LPF changed to RFU bits
	22	Chapter 6.10.3, Data rate of 8 kbds removed, corresponding bits HPF for high pass filter settings and LPF for low pass filter settings changed to RFU bits
	23	Chapter 6.12.2, text updated and bit TSHDIS removed (RFU bit)
	24	Chapter 6.13, LIN compliance and slope change updated
	26	Chapter 7.3, data rate lower limit changed from 1 kbps to 8 kbps
	29	Chapter 7.3.2.2, data rate lower limit changed from 1 kbps to 8 kbps, description of automatical adaption added, paragraph regarding LIN physical layer removed to chapter 6.13.
	29	Chapter 7.4.2, restructured and partly reworded
	33	Table 35, bit BDRT changed to RFU bit
	34	Chapter 7.7.2, Description of behaviour in case of missing transponder added, description regarding 8 kBd removed
	35, 36	Fig. 41 and Fig. 42 updated
	38	Fig. 43, write-active and write-read timing changed to 0.5ms
	38	Chapter 7.81 LIN idle time changed from 0.25 ms to 0.5 ms
	39, 40	Chapter 7.81, 7.8.2.1, 7.8.2.3, LIN idle time changed from 0.25 ms to 0.5 ms
	41	Chapter 8, limiting values for Voltage at XTAL1 and for $R_{th(j-c)}$added
	41	Chapter 8, limiting values for Power dissipation and for $R_{th(j-a)}$ updated
	41	Text regarding product lifetime test added
	42	I_{TX} removed due to double specification in chapter 9.2
	42	VB = 6.0V for both digital and analog part inserted, VB = 5.5V for functional digital part removed
	43	Voltage Regulator 1, max. output voltage $V_{VRC1,HI}$ and voltage between two consecutive steps $V_{VRC1,step}$ adapted
	43	I_{VRC1} added
	43	Voltage Regulator 1, ripple rejection maximum values added
	43	Voltage Regulator 1, supply voltage regulation δV_{BAT1}. min. value added and max. value adapted
	43	Voltage Regulator 2, output voltage V_{VRC2} adapted
	43	I_{VRC2} added
	43	Voltage Regulator 2, ripple rejection, maximum values added
	43	Voltage Regulator 2, supply voltage regulation δV_{BAT2}, min. value added and max. value adapted
	43	Antenna Driver, output resistance $R_{O,LOW}$ renamed in $R_{O,TX,GND}$ and $R_{O,HIGH}$ renamed in $R_{O,TX,VRC1,}$ conditions and maximum values adapted

Revision	Page	Description
	44	Receiver, analog ground V_{QGND} values adapted
	44	Receiver, Input dynamic range α_{in} removed
	44	Receiver, EMI low pass cut-off frequency $f_{LP,EMI}$, min. and max. value added
	44	High level output voltage for open collector pin renamed from V_{OH} to $V_{OH,RSTN}$
	44	LIN Driver, output voltage, dominant state $V_{O,DOM,}$ max. value added
	45	Power on reset threshold $V_{B2,POR}$ added
	45	Power on reset threshold, rising edge $V_{B2,POR,UP}$, falling edge $V_{B2,POR,DWN}$ and hysteresis $V_{B2,POR,HYS}$ removed
	46	Remote bus wake-up pulse width T_{REM}, min value changed from 250 µs to 280 µs
	46	Nominal single wire bit length $T_{LIN,NOM}$, max. value changed from 1000 µs to 125 µs
	46	Single wire Data request pulse width T_{SW_REQ}, min. and max. value added
	46	Watchdog timeout changed from 4.0s to 4.1s
	48	Chapter RELATED DOCUMENTS added
	48, 49	Anomaly Notes removed
	50, 51	Revision History updated

14 LEGAL INFORMATION

14.1 Data sheet status

Document status	Product status	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification or product development
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification
Product [short] data sheet	Production	This document contains the product specification

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