DATASHEET

PCF7991AT

Advanced Basestation IC (ABIC)

Product Specification 2009 Mar 11

CONFIDENTIAL

CONTENTS

1 FEATURES 特性

Fully integrated single chip basestation
Compatible with PCF79xx transponder families (HT2, HT2-Extended, HT-Pro)
Robust antenna coil power driver stage with modulator
High performance adaptive sampling time AM/PM demodulator (patent pending)
Read and write function
Programmable modulator/demodulator characteristics
On-chip clock oscillator and divider in the case of external clock reference
Antenna rupture and short circuit detection
Low power consumption
Very low power stand-by mode
Low external component count
Small package (SO14)

2 GENERAL DESCRIPTION 概述

The PCF7991AT is a fully integrated Advanced Basestation IC, ABIC, designed for car immobilizer systems providing read and write access to an identification transponder. The device is intended for use with the NXP transponder family (PCF79xx) as well as other transponder types operating at 125 kHz and employing ASK, Amplitude Shift Keying for write and AM/PM for the read operation. The receiver characteristics (amplifier gain, filter cutoff frequencies) can be optimized to system and transponder requirements. The PCF7991AT IC is designed for easy integration into immobilizer read/write and read-only systems featuring a high degree of integration and very low external component count. The device integrates a powerful antenna driver/modulator, a low-noise adaptive sampling time demodulator, programmable filters/amplifier and digitizer, required to design high-performance basestations. A three wire microcontroller interface is provided for programming the PCF7991AT as well as for the bidirectional communication with the transponder. The three-wire interface can be configured for two wire operation by connecting the data input and the data output.

该 PCF7991AT 是一个完全集成的高级基站集成电路，ABIC，为汽车发动机防盗系统而设计的，提供对 ID 应答器的读和写访问。该装置是为了使用 NXP 系列 PCF79xx 或其他类型的工作在 125kHz 和使用 ASK 写且 AM/PM 读操作的应答器，接收器特性(放大器增益，滤波器截止频率)可以按系统和应答器的需求进行优化。该 PCF7991AT 是为了易于集成到发动机防盗的读写或只读系统而设计的，特色是高度集成和外部元件数量非常少。该器件集成了一个强大的天线驱动器/调制器，低噪声自适应采样时间解调器，可编程滤波器/放大器和数字转换器，需要设计高性能的基站。PCF7991AT 可以和应答器进行双向通信，通过连接 DI 和 DO，三线接口可以配置为两线接口操作.

The device employs a unique Adaptive Sampling Time (AST) demodulation technique that extends the system operation range and eliminates the effect of a zero amplitude modulation response from the transponder, as a result of resonance frequency tolerances. 该设备采用一种独特的自适应采样时间(AST)的解调技术，扩展了系统的运作范围，且消除了应答器的零振幅调制响应的影响，作为谐振频率的公差结果。

3 ORDERING INFORMATION 订货须知

EXTENDED TYPE NUMBER	PACKAGE			TEMPERATURE
	NAME	DESCRIPTION	OUTLINE VERSION	RANGE (℃)
PCF7991AT/1081	SO14	plastic small outline package; 14 leads	SOT108-1	-40℃ to +85℃

4 BLOCK DIAGRAM 框图

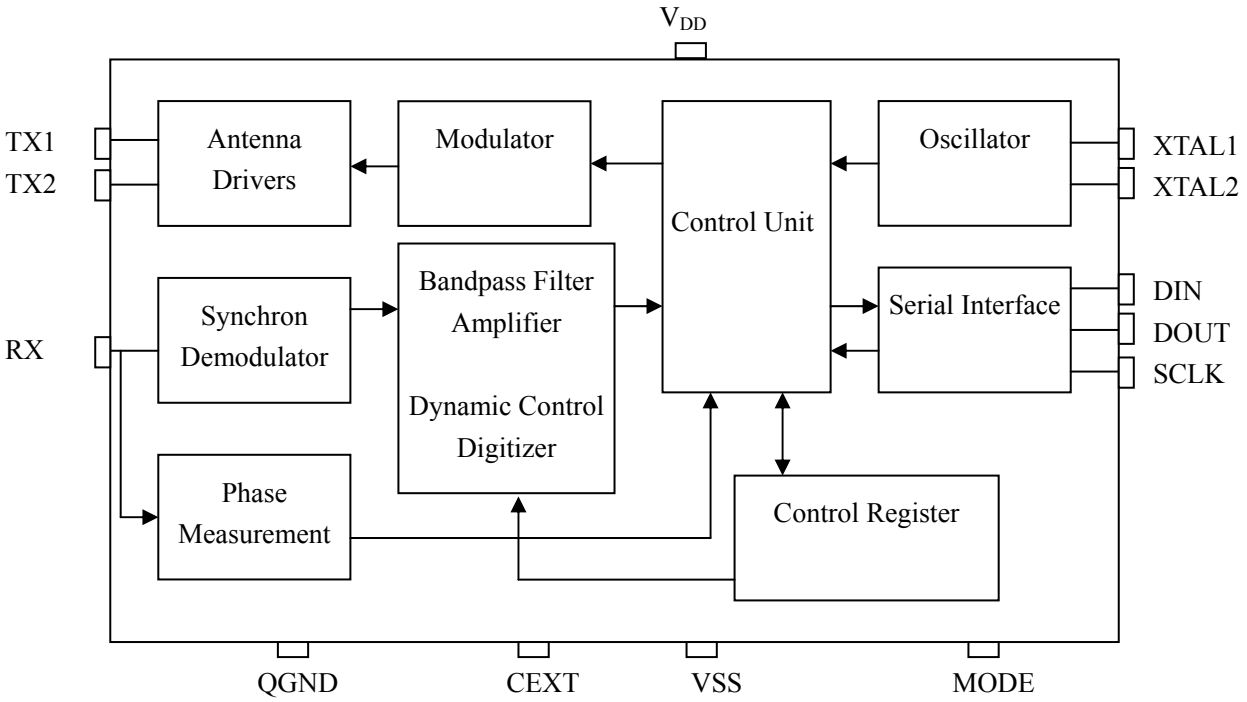


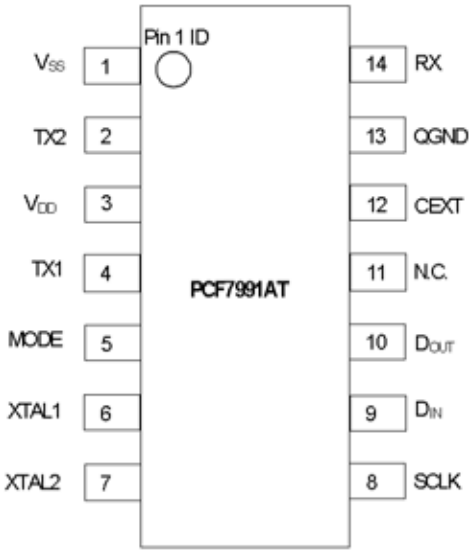
Figure 1.Blockdiagram advanced basestation PCF7991AT

5 QUICK REFERENCE DATA 快速参考

PARAMETER	VALUE		
	MIN	MAX	UINT
Supply voltage	4.5	5.5	V
Power-down current		20	μA
Clock/Oscillator frequency (antenna carrier frequency 125 kHz)	4	16	MHz
Antenna driver current		400	mAp
Receiver sensitivity	2		mVpp
Serial interface	CMOS compatible		
Package	SO14		
Operation temperature range	40℃ to +85℃		

6 PINNING

6.1 Pinning Diagram



6.2 Pinning Information

Table 1 Pin Description for PCF7991AT

SYMBOL	PIN	DESCRIPTION
V_{CC}	1	Common ground GND
TX2	2	Antenna driver output
V_{DD}	3	Supply voltage input, stabilized
TX1	4	Antenna driver output
MODE	5	Microcontroller interface mode select
XTAL1	6	Oscillator interface external clock reference input
XTAL2	7	Oscillator interface
SCLK	8	Microcontroller interface: serial clock input
DIN	9	Microcontroller interface: serial data in
DOUT	10	Microcontroller interface: serial data out
NC	11	Not connected
CEXT	12	High pass filter decoupling
QGND	13	Analog ground bias
RX	14	Receiver input

7 MINIMUM APPLICATION CIRCUITRY 最小应用电路

Figure 3 shows a minimal application circuitry for the PCF7991AT. The antenna coil La together with the capacitor Ca form a series resonant LC circuit (f = 125 kHz). The antenna tap voltage is attenuated by RV and the input impedance of the RX-pin. The capacitors at XTAL1 and XTAL2 are selected according to the crystal or ceramic resonator specification. In the case of an external clock reference they may be omitted. The capacitors at QGND and CEXT are for device internal biasing and decoupling purposes. 图 3 显示了一个最小的 PCF7991AT 应用电路。天线线圈 La 与电容器 Ca 形成一个串联谐振 LC 电路(f= 125kHz)。该天线电压 是由 RV 和 RX 引脚的输入阻抗衰减。XTAL1 and XTAL2 的电容选择根据晶体或陶瓷谐振器规格。在外部参考时钟情况下，他们可以省略。在 QGND 电容器和 CEXT 是器件内部偏置和去耦目的。

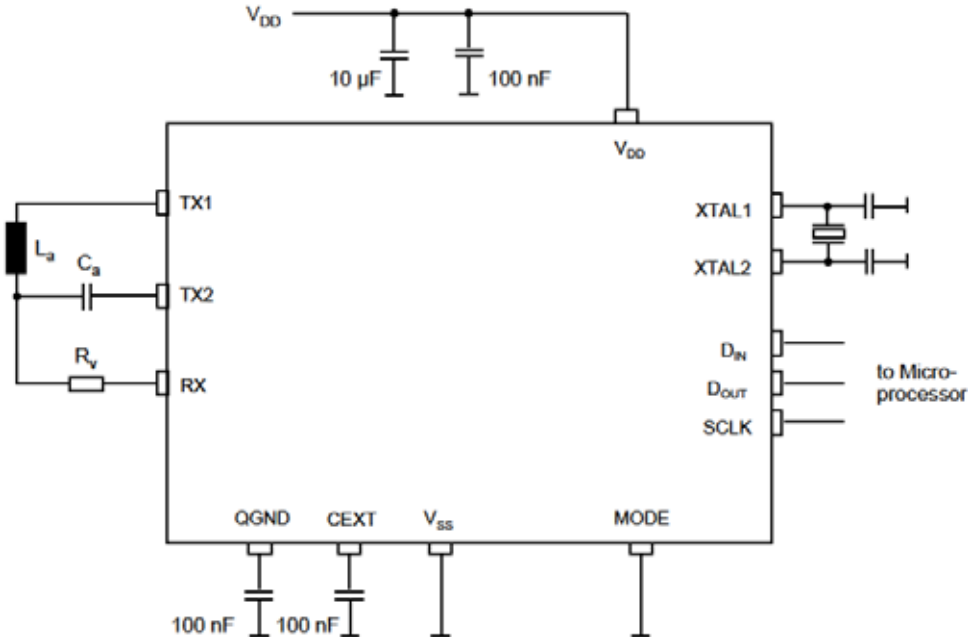


Figure 3. Minimum application circuitry

8 FUNCTIONAL DESCRIPTION 功能说明

8.1 Power Supply 电源

The PCF7991AT operates from an external 5V power supply. For optimum performance a stabilized supply voltage should be applied.
该 PCF7991AT 工作于外部 5V 电源供电。为了达到最佳的性能，应提供一个稳定的电源电压。

8.2 Antenna driver 天线驱动

The antenna drivers are configured as a full bridge capable to deliver a square wave shaped voltage to the series

resonant antenna circuit, which is connected between TX1 and TX2. The full bridge drivers are characterized by a low output impedance featuring a large drive voltage to the resonant antenna circuit. The antenna carrier frequency is 125 kHz typically. 该天线驱动器配置为一个全桥，有能力提供一个方波电压到串行谐振的天线电路，它是连接在 Tx1，2 之间的。全桥驱动器的特点是低输出阻抗，它对谐振天线电路具有较大的驱动电压。该天线的标准载波频率为 125 kHz。

8.3 Modulator 调制器

The modulator enables ASK (Amplitude Shift Keying) modulation of the antenna RF signal after switching the device into transparent mode (WRITE_TAG mode) by a WRITE_TAG or WRITE_TAG_N command (see Table 2). ASK modulation is achieved by blanking the antenna drive signal under control of the data input (DIN). The modulator features a timer circuitry that supports carrier blanking with a programmable duration (see Table 2).

调制器允许 ASK 调制由 WRITE_TAG 或 WRITE_TAG_N 命令切换设备到透明模式(WRITE_TAG mode)之后的天线上的 RF 信号，ASK 调制是通过消隐在 DIN 控制下的天线上的驱动信号实现的。该调制器具有一个定时器电路，支持可编程持续时间消隐的载波器(见表 2)。

8.4 Oscillator 振荡器

The on-chip oscillator operates either with a crystal or ceramic resonator connected to XTAL1/2. Alternatively, an external clock source (CMOS compatible) may be applied at XTAL1. The oscillator frequency feeds a programmable divider in order to derive the system clock and the antenna carrier frequency of 125 kHz. The programmable divider supports an oscillator frequency of 4, 8, 12 and 16 MHz (see Table 11).

片上振荡器是使用连接到 XTAL1/ 2 的晶体或陶瓷谐振器工作的。另外，可以由 XTAL1 采用外部时钟源(CMOS 兼容)。振荡器为可编程分频器提供频率，以获得系统时钟和天线的 125kHz 载频。可编程分频器支持振荡器频率为 4，8，12 和 16 兆赫(见表 11)。

8.5 Receiver 接收器

The receiver senses and demodulates the absorption modulation applied by a transponder that is inside the antenna RF field. The demodulated and digitized signal is available at the data output (DOUT) after switching the device into transparent mode (READ_TAG mode) by a READ_TAG command (see Table 2).

接收器感应和解调由一个应答器 LF 场天线上提供的调制输入，由 READ_TAG 命令切换设备到透明模式(READ_TAG 模式)后的 DOUT 上解调和数字化的信号是有效的。

The receiver features a high sensitivity and an extended input voltage range to ensure a large receiver dynamic range. The antenna tap signal is fed to the receiver input (RX) after attenuation by means of an external series resistor (RV) and the receiver input impedance (RIRX) in order to match the receiver input voltage specification. The receive signal passes an on-chip second order low pass filter and is further attenuated before it is fed to the synchron demodulator and phase measurement circuitry.

接收器具有高灵敏度和可扩展输入电压范围，以确保接收器的动态范围大。该天线上的信号衰减后，反馈到接收器输入(RX)端子，衰减是依靠外部的串联电阻(RV)和接收器输入阻抗(RIRX)，)为了匹配接收器的输入电压规范。接收的信号通过一个片上二阶低通滤波器，在反馈到同步解调器和相位测量电路之前，进一步衰减，

8.5.1 Synchron Demodulator 同步解调器

The antenna current and therefore the tap voltage is modulated by the transponder in amplitude and/or phase depending on various system parameters. By employing a unique Adaptive Sampling Time (AST) demodulation technique, amplitude and phase modulation of the receive signal is detected featuring an extended system operation range. The receive sampling time is set by the SET_SAMPLING_TIME command (see Table 2). The appropriate sampling time can be derived from an on-chip phase measurement and an offset that accounts for the external antenna interface component values. 该天线电流，以及由 应答器在 AM/PM 调制时产生的的端子电压 取决于各种不同的系统参数。通过采用独特的 AST 解调技术，接收信号的 AM/PM 被检测，扩展了系统的工作范围。接收采样时间则是由 SET_SAMPLING_TIME 命令设置的(见表 2)。适当的采样时间可以由一个片上的相位测量和一个外部天线接口的元件值偏移量驱动。

Receive signal sampling is inhibited when a WRITE_TAG or WRITE_TAG_N command is issued in order to avoid that write pulses de-sensitize the amplifier and digitizer circuitry. Signal sampling is resumed when the WRITE_TAG mode is terminated. For better receiver setting a short delay after the last write pulse has to be provided before the WRITE_TAG mode is terminated. 当 WRITE_TAG or WRITE_TAG_N 命令被执行时，为了避免写脉冲降低放大器和数字转化电路的灵敏度，禁止接收信号的采样。当 WRITE_TAG 模式终止时，恢复信号采样。为了更好的，WRITE_TAG 模式被终止之前，在最后一个写脉冲之后，接收器必需提供设置一个短的延时。

8.5.2 Bandpass Filter, Amplifier and Digitizer 带通滤波器，放大器，数据转换器

After demodulation the receive signal passes a baseband filter and amplifier prior to digitization. The amplifier gain and bandpass filter cutoff frequencies are adjustable by the SET_CONFIG_PAGE 0 command, in order to adapt the receiver path to the system coupling factor and transponder data rate.

解调之后，在数字化之前，接收信号经过一个带滤波器和一个放大器。该放大器增益和带通滤波器的截止频率由 SET_CONFIG_PAGE 0 命令可调的，以适应接收器回路的系统耦合因子和应答器数据速率。

For fast receiver settling after device power-up, sampling time shift or when switching from WRITE_TAG mode to READ_TAG mode the bandpass filter, amplifier and digitizer circuit biasing condition can be initialized and restored by a set of control bits accessible via the SET_CONFIG_PAGE commands.

在设备上电之后，为了接收机快速的设置，由一组控制位通过 SET_CONFIG_PAGE 命令很容易实现：采样时间的偏移，或者当由 WRITE_TAG 模式切换到 READ_TAG 模式时，带通滤波器，放大器和数字化电路的偏置条件可以被初始化和恢复。

8.5.3 Phase Measurement 相位测量

The optimum receive signal sampling time depends on the actual tuning condition of the resonant antenna circuitry. The actual tuning condition of the resonance antenna is determined by measuring the phase relationship between the exciting signal at the antenna driver output and the antenna tap voltage applied to the receiver input. In case of perfect tuning, the phase should be 90 degree plus an offset that accounts for the receiver input attenuation and low pass filter.

接收信号的最佳采样时间取决于谐振天线电路的实际调谐情况。该谐振天线的实际调谐情况由接收器提供的天线驱动输出和天线端子电压上存在的信号之间的相位关系的测量决定的。如果调谐完好， 相位是一个由接收器输入衰减和低通滤波器引起的偏移量，加上 90 度。

Miss-tuning of the resonance antenna circuit by component spreads or due to ambient temperature changes results in a change of the phase relationship. The actual phase relationship is determined by a READ_PHASE command (see Table 6) and used to calculate the optimum receive signal sampling time with support of an external microcontroller.

谐振天线电路的失调是由零件的偏差或环境温度的改变引起相位关系的变化，实际相位关系由 READ_PHASE 命令检测，用于计算最佳的接收信号采样时间，需要一个外部的 MCU。

8.5.4 Determing the Sampling Time 采样时间测定

Measurement, calculation and setting of the sampling time is typically implemented during system power-up initialization when the transponder is also in its power-up sequence not sending any data. As soon as the oscillator and resonance antenna circuit are settled a phase measurement is initiated and the sampling time determined according to the following relation:

采样时间的测量，计算和设置通常是在系统上电初始化时执行的，同样，当应答器在上电序列时，不发送任何数据。振荡器和天线谐振电路一旦稳定，就开始相位测量，采样时间由下面的关系确定。

$T_S = 2 * T_{ANT} + T_{OFFSET}$

T_S Receive signal sampling time 采样时间

T_{ANT} Actual phase measurement 实际测量相位

T_{OFFSET} Offset that accounts for the phase shift due to the antenna tap voltage attenuation and low pass filtering. 由于天线端子电压衰减和 LPF 产生的相移总数的偏移量。

After setting the sampling time the receiver has to settle before data can be demodulated and digitized properly.在设置采样时间之后，在数据被正确解调和数字化之前，接收器必须稳定。

8.5.5 Data Amplitude Comparison 数字振幅比较

For advanced receiver sampling time optimization the demodulated data signal strength can be weighted by amplitude comparison and the result reported in the status bit AMPCOMP (see Table 13).

When the ACQAMP control bit (see Table 10) is set by a SET_CONFIG_PAGE command, the actual demodulated data signal amplitude is stored as reference. After resetting the ACQAMP control bit the status bit AMPCOMP is set, when the actual data signal amplitude is larger than the stored reference otherwise it is cleared.

对于先进的接收器采样时间的优化，解调的数据信号强度可由在状态位 AMPCOMP(见表 13)报告的结果和幅度比较加权。当 ACQAMP 控制位由 SET_CONFIG_PAGE 命令置位，真实的解调数据信号振幅作为基准值存储，ACQAMP 控制位复位后，当实际数据信号振幅大于存储的基准值时，AMPCOMP 状态位置位，否则它被清 0。

8.5.6 System Diagnostics 系统诊断

In order to detect an antenna short or open condition the receiver input voltage at the RX-pin is monitored and an antenna fail condition is reported in the status bit ANTFAIL, (see Table 13). If the receiver input voltage does not exceed the diagnostic threshold level VDTH (see Chapter 11), the status bit ANTFAIL is set, otherwise it is cleared. The status bit is updated once per antenna carrier period and can be read by a GET_CONFIG_Page 2 or 3 command (see Table 13). The status bit is undefined in Power-down or Idle mode, during the oscillator start-up time and when the antenna drivers are disabled. Advanced system diagnostics are feasible by considering the phase measurement information also.

为了检测天线的短路或开路，接收器的 RX-pin 上的输入电压被监视，且天线故障由状态位 ANTFAIL 报告。如果接收器的输入电压没有超过诊断阈值电平 VDTH，状态位 ANTFAIL 置位，反之清 0。该状态位每个天线载波周期更新一次。而且可由 GET_CONFIG_Page2，3 命令读取。在掉电或挂起模式时、在振荡器启动时间、当天线驱动器被禁止时，该状态位是不确定的(ANTFAIL)。就相位的测量信息而言，高级系统诊断也是可行的。

8.6 Power-On Reset 上电复位

The device generates an internal power-on reset to initialize the chip after power-on or power fail condition. As a result the control register is initialized according to Table 11. 在上电或电源故障的条件下，设备产生一个内部的上电复位，初始化芯片。因此，按 Table 11，控制寄存器被初始化。

8.7 Power-Down Modes 掉电复位

After a power-on reset condition the device operates in ACTIVE mode. The PCF7991AT supports an Idle and Power-down mode for power saving means. The mode of operation is determined by control bits addressed by an SET_CONFIG_PAGE 1 command (see Table 10).

In Idle mode only the oscillator and a minimum of other circuitry is active. In Power-down mode the device is in OFF state completely. The serial interface is operational in any case in order to provide access to the control register. 在上电复位之后，设备工作在激活模式。为了省电的目的，该芯片支持一个挂起和掉电模式。由 SET_CONFIG_PAGE 1 命令寻址的控制位决定它的工作模式，仅在挂起模式，振荡器和一小部分的其它电路被激活，在掉电模式，设备处于完全关断状态。无论如何，为了访问控制寄存器，串行接口都是可使用的。

8.8 Serial Interface 串行接口

The communication between the PCF7991AT and the microcontroller is done via a three wire digital interface. The interface is used to issue commands for writing and reading of device configuration data and for writing to and reading from the transponder in one of the transparent modes (READ_TAG, WRITE_TAG / WRITE_TAG_N). Device configuration is stored in a control register with read back feature.

PCF7991AT 与 MCU 之间的通讯，由一个三线的数字接口完成的。该接口用于 在透明模式之一(READ_TAG, WRITE_TAG / WRITE_TAG_N)，为了设备配置数据的写和读，以及为了写和从应答器读，发送命令。设备配置存储在一个具有可读特性的控制寄存器中。

The interface is operated by the following signals: 这个接口由下面的信号操作
SCLK Clock 施密特触发器输入
DIN Data Input 施密特触发器输入
DOUT Data Output 开漏极输出，内部有一个弱上拉电阻器
SCLK and DIN are realized as Schmitt-Trigger inputs. DOUT is an open drain output with a weak internal pull-up resistor.

Any communication between the PCF7991AT and The microcontroller begins with an initialization of the serial interface before the desired command can be issued. The interface initialization condition is a low-to-high transition of the signal DIN while SCLK is high (see Figure 4).

在需要的命令被发送之前，PCF7991AT 与 MCU 之间的任何通讯是由初始化串行接口开始的。接口的初始化条件是：当 SCLK 是高时，DIN 信号一个由低到高的跳变(see Figure 4)。

All commands are transmitted to the PCF7991AT serial interface starting with Most Significant Bit (MSB). DIN is latched with a high state at SCLK. DOUT is valid during the high state of SCLK (MODE pin connected to VSS).

所有的命令被传输到 PCF7991AT 串行接口，是由最高有效位开始的。在 SCLK 高状态，DIN 被锁存，在 SCLK 的高状态期间(MODE pin connected to VSS)，DOUT 是有效的。

DOUT and DIN may be connected to each other in order to form a two-wire communication link with the microcontroller (always half duplex communication). 为了与 MCU 组成一个两线通信链路，DOUT 和 DIN 也可以连接在一起(始终是半双工通信)。

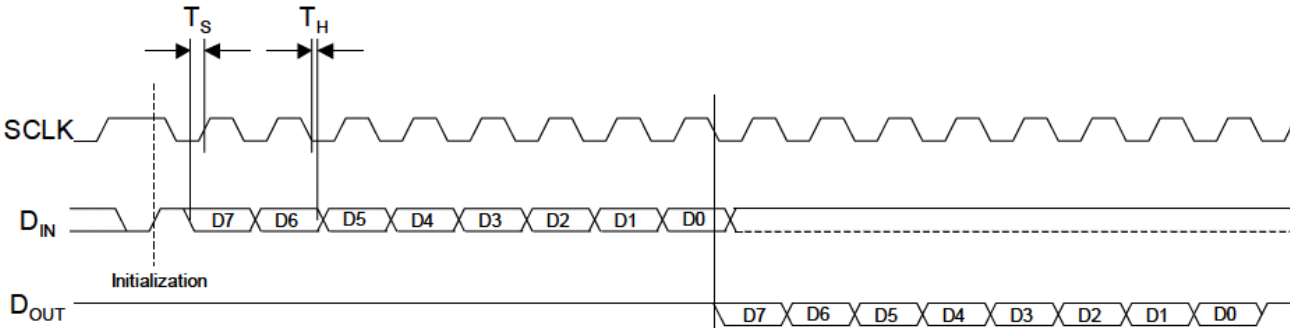


Figure 4. Serial Interface Timing

8.8.1 Serial Interface Mode 串行接口模式

The serial interface supports two modes of operation, filtered and non-filtered communication.

串行接口支持两种操作模式，滤波和无滤波通信

If MODE is connected to VSS, no filtering is applied and the state of the interface signals is directly available at the internal circuitry. The maximum data rate of the serial interface is limited by the set-up and hold time as specified (see Chapter 11.2).

如 MODE 是连到 VSS， 无滤波被接受，而且接口信号状态在内部电路中是一直有效的.串行接口的最大数据速率由规范的建立和保持时间限制。

If MODE is connected to VDD, digital filtering of SCLK and DIN is performed offering improved immunity against glitches, reflections and EMC on these interface signals. This mode of operation is intended for use for so-called ‘Active Antenna Applications’, where the PCF7991AT and the microcontroller have to communicate via long interface wires.

如果 MODE 连接到 VDD ，SCLK 和 DIN 的数字滤波通过改良的抗扰性能阻止接口上的虚假、反射、EMC 信号。当 PCF991AT 和 MCU 必须通过长接口线通信时，这个操作模式是为所谓的“有源天线应用”

而设计的。

The digital filtering is provided by sampling the SCLK and DIN inputs at a rate of 1/fTX, 8 µs typically. The internal state of these signals is updated only after two successive samples of the same logic level. The result of this evaluation is delayed by another 8µs. Hence, all state changes at the SCLK or DIN inputs are delayed by 16 µs to 24 µs, until they are recognized by the internal circuitry.

数字滤波器是以 1/fTX, 8 µs 标准值的速率，采样 SCLK 和 DIN 输入 提供的。信号的内部状态仅在两次连续采样到相同的逻辑电平时更新. 评估结果被另外的 8 µs 延时。此后，所有的 SCLK 或 DIN 输入状态变化都被延时 16～24 µs ，直到他们被内部电路识别。

When filtered SPI communication is used, it must be avoided that a level change of both input signals occurs in the same sampling period. The setup time becomes (Figure 5):

当滤波的 SPI 通信被使用时，它必须避免在相同的采样周期两个输入信号发生改变。这个建立时间 (Figure 5):

$$T_{S,MODE1} = 1/f_{TX} + T_{S,MODE0} + TH$$

The absolute accuracy of fTX has to be considered for the calculation of the minimum value of TS,MODE1. If DIN and DOUT are connected to each other to form a two- wire communication link, the filtering delay between DIN and DOUT must be considered in order to meet TS,MODE1. Since data at pin DOUT is clocked out with the negative edge of the deglitched signal SCLK, the maximum propagation delay between the negative edge of SCLK and the change of DOUT has to be considered (Figure 6): 为了计算 $T_{S,MODE1}$ 的最小值，必须考虑 f_{TX} 的绝对准确度。如果 DIN 和 DOUT 相互连接到一起，组成一个两线通信链路时，为了符合 $T_{S,MODE1}$，必须考虑 DIN 和 DOUT 的滤波延时。自从 DOUT 脚上的数据信号 在 SCLK 抗尖峰脉冲信号的负沿 时，时钟输出，必须考虑 SCLK 的下降沿和 DOUT 的变化之间的最大传播延时：

$$T_{DOUT,\ MODE1,\ max} = 3/f_{TX,min} + T_{S,MODE0} + T_{DEL}$$

The additional delay TDEL depends on the external circuitry (e.g. caused by line drivers or capacitive loads) and is calculated to be: 附加延时 TDEL 由外部电路决定 (线驱动或容性负载引起) 。

$$T_{DEL} \cong 5 * (C_{DOUT} + C_{EXT}) (R_P \parallel R_{EXT})$$

In Figure 7, the maximum delays to be considered for two- wire communication are summarized in a block diagram. 对于两线通信中，必须考虑最大延时，总结在一个方框图中。

If digital filtering of SCLK and DIN is enabled and the device has been forced into Power-down mode, this mode can be terminated by setting SCLK to LOW and DIN unequal to the status bit TXDIS (see Table 10). As a result, the XTAL oscillator is restarted and the configuration bit PD_MODE is cleared, which causes the device to enter Idle mode. 如果 SCLK 和 DIN 的数字滤波已启用，而且设备已被迫进入掉电模式，通过设置 SCLK 为低，而且 DIN 与状态位 TXDIS 不相等, 可以终止这种模式. (见表 10)。因此，晶体振荡器重新启动，配置位 PD_MODE 被清除，这将导致器件进入空闲模式。

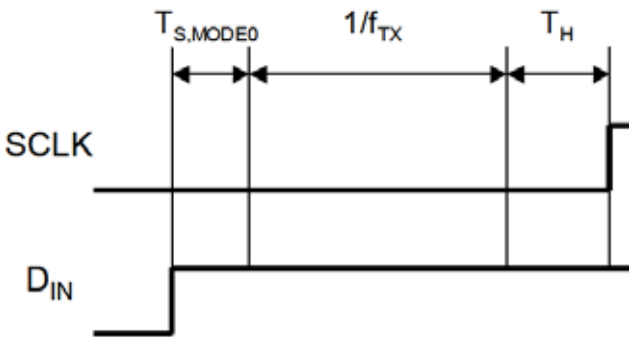


Figure 5. Setup time for DIN and SCLK for filtered SPI communication

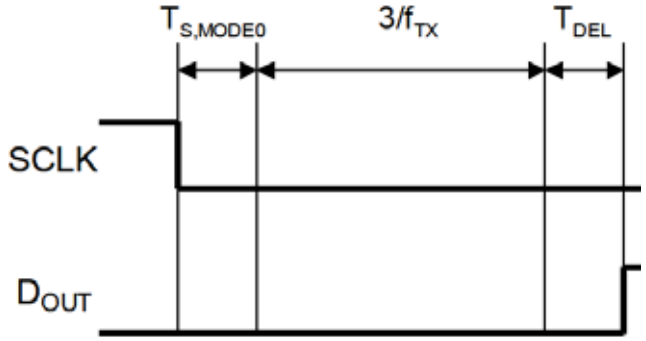


Figure 6. Max. output delay for DOUT for filtered SPI communication (two-wire communication)

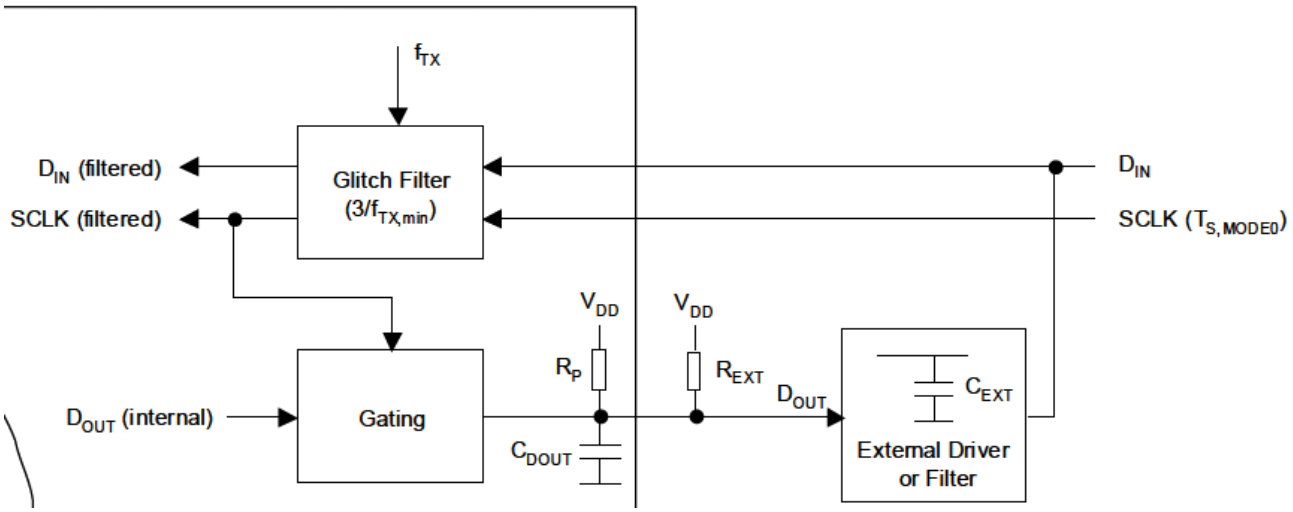


Figure 7. Filtering delay during two-wire communication 2 线通信时的滤波延时

9 COMMAND SET 命令集

Table 2 Command set summary

COMMAND NAME	MSB BIT NO. LSB								RESPONSE
	7	6	5	4	3	2	1	0	
GET_SAMPLING_TIME	0	0	0	0	0	0	1	0	8 bit (0 0 D5-D0)
GET_CONFIG_PAGE	0	0	0	0	0	1	P1	P0	8 bit (X3 X2 X1 X0 D3-D0)
READ_PHASE	0	0	0	0	1	0	0	0	8 bit (0 0 D5 - D0)
READ_TAG	1	1	1	-	-	-	-	-	enter READ_TAG-mode
WRITE_TAG_N	0	0	0	1	N3	N2	N1	N0	enter WRITE_TAG-mode with pulse width
WRITE_TAG	1	1	0	-	-	-	-	-	enter WRITE_TAG-mode
SET_CONFIG_PAGE	0	1	P1	P0	D3	D2	D1	D0	4 bit per config page addressed
SET_SAMPLING_TIME	1	0	D5	D4	D3	D2	D1	D0	8 bit (00 D5 - D0)9.1 READ_TAG

9.1 READ_TAG

This command is used to read the demodulated bit stream from a transponder: After the assertion of the three command bits the PCF7991AT instantaneously switches to READ_TAG-mode and the demodulated, filtered and digitized data from the transponder is available at the data output DOUT for decoding by the microcontroller.

此命令用于从应答器读取解调位流，在三个命令位断定之后，PCF7991 立即切换到 READ_TAG 模式，而且从应答器中已解调，已滤波和数字化的数据是可使用的，在 DOUT 输出，以便 MCU 解码。

READ_TAG-mode is terminated immediately by a low to high transition at SCLK.

READ_TAG 模式由 SCLK 一个低到高的跳变,立即终止

Table 3 READ_TAG command sequence

BIT NO.	7	6	5	4	3	2	1	0	Remark
Command	1	1	1	-	-	-	-	-	Received data available at DOUT

9.2 WRITE_TAG_N

This command is used to write data to a transponder and to set the modulator blanking characteristics.

该命令是用于写数据到应答器，设置调制器消隐的参数

If N3-N0 are set to zero, the signal from DIN is transparently switched to the drivers. A high level at DIN corresponds to antenna drivers switched off, a low level corresponds to antenna drivers switched on.

如果 N3-N0 设置为 0，DIN 上的信号透明地切换到驱动器，DIN 上的高电平相当于天线驱动关闭，低电平相当于天线驱动打开。

If any binary number between 1 and 1111 is loaded into N3-N0, the drivers are switched off at the next positive transition of DIN. The driver off state is maintained for a time interval equal to N * T0 (T0=8 μs) regardless the state of DIN. This method relaxes the timing resolution requirements to the microcontroller and to the software implementation while providing an exact, selectable write pulse timing.

如果在 1～1111 这间的任何二进制数被装入到 N3-N0， 驱动器在 DIN 的下一个极性过渡时关闭。无认 DIN 状态怎样, 驱动器的关闭状态保持一个时间间隔 N*T0(T0=8 μs).。当提供一个精确的，可选择的写脉冲定时时，这个方法放松了 MCU 和软件执行对时间分辨率的要求。

WRITE_TAG-mode is terminated immediately by a low to high transition at SCLK. As a result, the driver resume their initial state, regardless the actual state of the modulation pulse timer.

WRITE_TAG 模式由 SCLK 低到高的跳变来终止。因此，不管调制脉冲定时器的激活状态，驱动器重启它们的初始状态，

Table 4 WRITE_TAG_N command sequence

BIT NO.	7	6	5	4	3	2	1	0	Remark
Command	0	0	0	1	N3	N2	N1	N0	no response 无应答

9.3 WRITE_TAG

This is the 3 bit short form of the command WRITE_TAG_N. It allows to switch into WRITE_TAG-mode with a minimum communication time.

这是 WRITE_TAG_N 命令的 3 位简单格式。它允许在最少的通信时间里切换到 WRITE_TAG-模式。

The behaviour of the WRITE_TAG command is identical to WRITE_TAG_N with two exceptions:

WRITE_TAG 命令与 WRITE_TAG_N 行为是完全相同的，有两个例外:

WRITE_TAG-mode is entered after assertion of the 3rd command bit. 第三个命令位断定之后，进入 WRITE_TAG 模式。

No N parameter is specified with this command; instead the N value which has been programmed with the most recent WRITE_TAG_N command is used. If no WRITE_TAG_N was issued so far, a default N=0 (transparent mode) will be assumed. 这个命令没有规定 N 参数， WRITE_TAG_N 命令已在最近使用过，用已经被编程的值代替 N，如果至今没有执行过 WRITE_TAG_N，默认 N= 0 (transparent mode)。

WRITE_TAG-mode is terminated immediately by a low to high transition at SCLK. As a result, the driver resume their initial state, regardless the actual state of the modulation pulse timer. WRITE_TAG 模式由 SCLK 上低到高的跳变终止，因此，不管调制脉冲定时器的激活状态，驱动器恢复他们的初始状态。

Table 5 WRITE_TAG command sequence

BIT NO.	7	6	5	4	3	2	1	0	Remark
Command	1	1	0	-	-	-	-	-	no response 无应答

9.4 READ_PHASE

This command is used to read the antennaμs phase T_{ANT}, which is measured at every carrier cycle. The phase is coded binary in D5-D0.

此命令用于读取天线的相位，TANT，它是在每个载波周期里测量的。相位用二进制编码。

Table 6 READ_PHASE command sequence

BIT NO.	7	6	5	4	3	2	1	0	Remark
Command	0	0	0	0	1	0	0	0	
Response	0	0	D5	D4	D3	D2	D1	D0	

9.5 SET_SAMPLING_TIME

This command specifies the demodulator sampling time Ts. The sampling time is coded binary in D5-D0.

该命令指定调制器的采样时间，TS，采样时间用二进制编码

Table 7 SET_SAMPLING_TIME command sequence

BIT NO.	7	6	5	4	3	2	1	0	Remark
Command	1	0	D5	D4	D3	D2	D1	D0	no response 无应答

9.6 GET_SAMPLING_TIME

This command is used to read back the sampling time Ts set with SET_SAMPLING_TIME. The sampling time is coded binary in D5-D0.

该命令用于读回采样时间 TS 的设置，

Table 8 GET_SAMPLING_TIME command sequence

BIT NO.	7	6	5	4	3	2	1	0	Remark
Command	0	0	0	0	0	0	1	0	
Response	0	0	D5	D4	D3	D2	D1	D0	

9.7 SET_CONFIG_PAGE

This command is used to configure the receiver characteristics (cutoff frequencies, gain factors) and the different operation modes. P1 and P0 select one of four configuration pages. 该命令用于配置接收器参数表(截止频率，增益因子)，和不同的操作模式，P1，P0 选择 1～4 个配置页。

Table 9 SET_CONFIG_PAGE command sequence

BIT NO.	7	6	5	4	3	2	1	0	Remark
Command	0	1	P1	P0	D3	D2	D1	D0	no response 无应答

Table 10 SET_CONFIG_PAGE mapping

BIT NO. Command/Page NO.	P1	P0	D3	D2	D1	D0
SET_CONFIG_PAGE 0	0	0	GAIN1	GAIN0	FILTERH	FILTERH

SET_CONFIG_PAGE 1	0	1	PD_MODE	PD	HYSTERESIS	TXDIS
SET_CONFIG_PAGE 2	1	0	THRESET	ACQAMP	FREEZE1	FREEZE0
SET_CONFIG_PAGE 3	1	1	DISPL1	DISSMARTCOMP	FSEL1	FSEL0

Table 11 Configuration bit description 配置位描述

BIT NAME	DESCRIPTION	RESET CONDITION	
FILTERL	main low pass cutoff frequency	0	0:fL=3kHz; 1: fL= 6kHz
FILTERH	main high pass cutoff frequency	0	0:fH=40kHz; 1: fH= 160Hz
GAIN0	amplifier_0 gain factor 增益因子	0	0: gain0 =16; 1: gain0= 32
GAIN1	amplifier_1 gain factor	1	0: gain1 =6.22; 1: gain1= 31.5
TXDIS	disable antenna driver	0	0: driver active; 1: driver inactive
HYSTERESIS	data comparator hysteresis 数据比较器滞后	0	0: hysteresis OFF; 1: hysteresis ON
PD	Power-down mode enable 允许掉电	0	0: device active; 1: Power-down mode
PD_MODE	select Power-down mode, if PD = 1	0	0: Idle mode; 1: Power-down mode
FREEZE0	receiver characteristics override 接收器参数表覆盖	0	Note 1
FREEZE1	receiver characteristics override 0 Note 1	0	Note 1
ACQAMP	reference for later amplitude comparison 存储信号的振幅，最后的振幅比较作为基准	0	see Section 8.5.5
THRESET	reset threshold generation of digitizer 数字转化器复位阈值的产生	0	Note 3
FSEL0	clock frequency select LSB	0	Note 2
FSEL1	clock frequency select MSB	0	Note 2
DISSMART COMP	disable smart comparator 禁止智能比较器	0	0: comparator = ON, 1: comparator = OFF
DISLP1	disable main low pass 禁止主低通	0	0: low pass = ON, 1: low pass = OFF

1. In order to achieve fast receiver settling the amplifier and filter characteristics can temporarily be overridden:
为了快速接收，设置放大器和滤波器参数表可以暂时被覆盖

FREEZE1	FREEZE0	Remark
0	0	normal operation according to configuration page 0 按配置 0 正常操作
0	1	main low pass is frozen and main high pass is initialized to QGND 主低通被冻结，主高通初始化到 QGND10
1	0	main low pass is frozen and the time constant of the main high pass is reduced by a factor of 16 for FILTERH = 0 and by a factor of 8 for FILTERH = 1
1	1	time constant of the main high pass is reduced by a factor of 16 for FILTERH = 0 and by a factor of 8 for FILTERH = 1. Second high pass is initialized to QGND 主高通的时间常量由 16 的因数减小，第二高通初始化到 QGND

2. In order to derive an antenna carrier frequency fTX of 125 kHz; the clock divider has to be programmed as

follows: 为了驱动一个天线，时钟驱动器必须按下面编程

FSEL1	FSEL0	OSCILLATOR FREQUENCY
0	0	4 MHz
0	1	8 MHz
1	0	12 MHz
1	1	16 MHz

3. If the THRESET is set, the threshold generator is disabled and initialized according to the receive signal conditions.
如果 THRESET 被设置，阈值发生器被禁止，并且按接收信号条件初始化。

9.8 GET_CONFIG_PAGE

This command has three functions:
1. Reading back the configuration parameters set by SET_CONFIG_PAGE command 读回配置参数集
2. Reading back the transmit pulse width programmed with WRITE_TAG_N 读回已编程的发射器脉冲宽度，
3. Reading the system status information

P1 and P0 select one of four configuration pages. The response (X3 X2 X1 X0 D3 D2 D1 D0) contains the contents of the selected configuration page in its lower nibble. For P = 0 or P = 1 the higher nibble reflects the current setting of N (the transmit pulse width). For P = 2 or P = 3 the system status information is returned in the higher nibble. 在它的低半字节包含了选定页的内容，高半字节反映了 N 的当前设置

Table 12 GET_CONFIG_PAGE command sequence

BIT NO.	7	6	5	4	3	2	1	0	Remark
Command	0	0	0	0	0	1	P1	P0	
response	X3	X2	X1	X0	D3	D2	D1	D0	

Table 13 GET_CONFIG_PAGE mapping

BIT NO.	BIT NUMBER							
Command/Page NO.	7	6	5	4	3	2	1	0
GET_CONFIG_PAGE 0	N3	N2	N1	N0	D3	D2	D1	D0
GET_CONFIG_PAGE 1	N3	N2	N1	N0	D3	D2	D1	D0
GET_CONFIG_PAGE 2	0	0	AMPCOMP	ANTFAIL	D3	D2	D1	D0
GET_CONFIG_PAGE 3	0	0	AMPCOMP	ANTFAIL	D3	D2	D1	D0

Table 14 Status Bit description

BIT	NAME	DESCRIPTION
ANTFAIL	antenna failure 天线故障	see Section 8.5.6
AMPCOMP	amplitude comparison result 放大器比较结果	see Section 8.5.5

10 LIMITING VALUES 极限值

All values are in accordance with Absolute Maximum Rating System (IEC 134) 所有值与 AMRS 一致

PARAMETER	MIN	MAX	UNIT
Operating temperature range	-40	+85	℃
Storage temperature range	-65	+125	℃
Junction temperature range		+140	T
Vol tage at any pin to ground, except pin RX RX 例外	-0.3	+6.5	V
Voltage at any pin to ground, except pins RX, DIN, DOUT, SCLK	-0.3	VDD+0.3	V
Voltage at pin RX to ground	-10	+12	V
Input current for pins DIN, DOUT, SCLK		10	mA
ESD, human body model, Note 1		2	kV
Power dissipation 功耗		200	mW

Note 1. According to MIL-STD 883D, Method 3015,7d

11 ELECTRICAL CHARACTERISTICS 电气特性

11.1 DC Characteristics DC 特性

Tamb = -40 to +85℃,VDD = 5.5V,VSS=0V, Unless otherwise specified

SYMBOL	PARAMETER	CONDITION	MIN	Typ	MAX	UNIT
Supply						
VDD	Supply voltage	With respect to VSS	4.5	5.0	5.5	V
I_{ON}	Operating supply current	ITX1 = ITX2 = 0		4.0	10	mA
I_{ID}	Supply current, IDLE mode	Note 1		0.2	0.4	mA
I_{PD}	Supply current, Power-Down mode	Note 2		7.0	20	µA
Antenna Driver(TX1,TX2)						
I_{TXCW}	Output peak-current	Continuous wave			200	mAp
$I_{TXPULSE}$	Output peak-current	On/Off-ratio = 1:4 ton < 400 ms			400	mAp
R_{OTX}	Output resistance	Full bridge, ROTX = ROTX1 + ROTX2		2.5	7.0	Ω
Receiver input (RX)						
V_{IRX}	Input voltage range	With respect to QGND	-8		+8	Vp
V_{QGND}	Analog ground		0.35VDD	0.42VDD	0.50VDD	V
R_{IRX}	Input impedance 输入阻抗		17	25	33	kΩ
V_{DTH}	Diagnostic threshold level 诊断阈值电平	With respect to QGND	-1.5	-1.15	-0.8	V

Serial Interface (DIN, DOUT , SCLK)						
Data Input, serial clock input (DIN, SCLK)						
V_{IL}	Input voltage LOW		-0.3		0.3VDD	V
V_{IH}	Input voltage HIGH		0.7VDD		VDD+0.3	V
I_{IL}	Input current LOW	V_{IH} = 0V			-2	µA
I_{IH}	Input current HIGH	V_{IH} = VDD			+2	µA
Data Output (DOUT), open drain with internal Pull Up						
V_{OL}	Output voltage LOW	I_{OL} < 1mA			0.4	V
I_{OL}	Output current LOW	V_{OL} ≤ 0.4V	1			mA
I_{OPU}	Output current HIGH	V_{OL} = 0V	-10			µA

Note 1. Does not include power consumption of XTAL or other external components.不包含晶体或外部元件上的功耗

11.2 AC Characteristics AC 特性

Tamb = -40 to +85℃,VDD = 5.5V,VSS=0V, f_{TX} = 125kHz; Unless otherwise specified

SYMBOL	PARAMETER	CONDITION	MIN	Typ	MAX	UNIT
XTAL Oscillator (XTAL1, XTAL2)						
f_{OSC}	Frequency range	Depending on FSEL	4		16	MHz
T_{SUP}	Start-up time 启动时间			4	10	ms
R_{FB}	Feedback resistance	XTAL1 to XTAL2	0.5	1.3	3	MΩ
External Clock Input (XTAL1)						
f_{EXT}	Frequency range	Depending on FSEL	4		16	MHz
	Duty cycle		40		60	%
C_{XTAL1}	Input capacitance	XTAL1		5		pF
Serial Interface						
$T_{S,MODE0}$	Set-up time	MODE pin at VSS	50			ns
T_H	Hold time 保持时间	MODE pin at VSS	50			ns
C_{DOUT}	Output Capacitance 输出电容	MODE pin at VSS			15	pF
C_{IN}	Input Capacitance 输入电容			3	7	pF
Receiver						
V_{RX}	Receiver sensitivity 接收灵敏度	With respect to QGND	2	1		mV_{PP}
T_{RCV0}	Receiver delay 接收延时	FILTER = 0	290	310	340	µs
T_{RCV1}	Receiver delay 接收延时	FILTER = 1	160	175	190	µs
	Phase measurement error 相位测量误差				±5.7	°
Recovery from clock stable to demodulator valid						
T_{RPD}	Recovery time demodulator	Note 1			5	ms
Recovery from WRITE-pulse						
T_{RWD}	Recovery time demodulator	Note 1			500	µs
Recovery from AST-step						
T_{RAST}	Recovery time demodulator	Note 1		0.4	1.5	ms
Response delay data input to antenna driver 数据输入到天线的驱动器响应延时						
T_{DITX}	Response delay DIN to TX	MODE pin at VSS; Note 2			10	µs

Note

1. Specific command sequence required. 需要特定的命令序列

2. Applicable for WRITE_TAG and WRITE_TAG_N commands. Due to device internal signal synchronization measures, TDITX is the response delay between a change at DIN and the resulting change at the antenna drivers. In the case of N is zero, TDITX applies for both the rising and failing transition at DIN, while for N unequal zero it applies for the rising transition at DIN only.

适用于 WRITE_TAG 和 WRITE_TAG_N 命令。由于设备内部信号同步测量，TDITX 是 DIN 的变化与在天线驱动器产生的变化之间的响应延迟。在 N 等于零的情况下，TDITX 适用于 DIN 的上升和下降沿两者，当 N 不平等于零，只适用于 DIN 上升沿。

12 PACKAGE OUTLINE 封装外形

(略)

13 REVISION HISTORY 版本历史

REVSION	Page	DESCRIPTION
2007 Aug 24		Change to NXP style
		Editorial updates and corrections
	3	Statement for compatibility HT2-Extended and HT-Pro Family added
	8-9	Chapter8.8 “Serial Interface Description” extended
	10	Figures 5 to 7 added
	16-18	Limiting values, DC CHARACTERISTICE AND AC CHARACTERISTICS adopted according to Product Specification Annex, 2000 Sep 18
	18	Specification of Output Capacitance C_{DOUT} added.
2009 Mar 11		Editorial updates and corrections

14 LEGAL INFORMATION 法律信息

14.1 Data sheet status 数据表状态

Document status	Product status	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification or product development
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification
Product [short] data sheet	Production	This document contains the product specification

14.2 Definitions 定义

Draft

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