NCJ29D5DHN

Ultra Wideband Transceiver with MAC support

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Document information

Information	Content
Keywords	Secure Ranging, Secure Interface, UWB transceiver, IEEE 802.15.4 HPR, IEEE draft 802.15.4z HRP, ARM® Cortex®-M33, ARM® TrustZone
Abstract	The device is a fully integrated single chip Impulse Radio Ultra Wideband (IR-UWB) low-energy transceiver IC compliant to IEEE 802.15.4 HRP UWB PHY and IEEE draft 802.15.4z BPRF/HPRF UWB PHY. It is designed for Secure Ranging applications in an automotive environment. It can be used to determine distance to a precision of up to 10 cm. It supports data transfer rates up to 6.8 Mbps (BPRF) and 7.8 Mbps (HPRF). It features a dedicated MAC firmware to ease UWB ranging set-up and session control.

1 General information

The device is a fully integrated single chip Impulse Radio Ultra Wideband (IR-UWB) low-energy low-cost transceiver IC. The device supports frame formats, which are compliant to IEEE 802.15.4 HRP UWB PHY (see [4]) and IEEE draft 802.15.4z BPRF/HPRF UWB PHY (see [5]). It is designed for Secure Ranging applications in an automotive environment. It can be used in 2-way ranging location systems to determine distance to a precision of up to 10 cm. It also supports data transfer rates up to 6.8 Mbps for BPRF and 7.8 Mbps for HPRF. The device features a dedicated MAC firmware to ease UWB ranging set-up and session control.

The main objective of a UWB ranging device is to provide a distance estimate, between an initiator and a responder. The distance estimate is based on a Time of Flight measurement, and is practically immune to relay station attacks. This drastically improves PHY layer security compared to a RSSI or phase based distance measurement, which is susceptible to relay station attacks.

A UWB system can give an accurate distance estimate, when there is a direct line-of-sight (LOS) propagation path between the initiator and the responder. All other propagation paths are caused by reflections, hence have a longer time of flight.

The device is capable of detecting the LOS propagation path, even if a non-line-of-sight (NLOS) path is much stronger. This can happen due to body attenuation for example, which weakens the LOS path. Good first path sensitivity and large first path dynamic range are highly desirable for the application, since they lead to an accurate ranging estimate, even under adverse channel conditions.

The new IEEE draft 802.15.4z BPRF/HPRF UWB PHY (see [5]) draft standard enables secure ranging. It achieves this by adding a Scrambled Timestamp Sequence (STS) to the ranging frame. Figure 1 shows how the STS is included in the frame format. To receive the STS, the receiver needs to have acquired frame timing first. The STS is hence transmitted after the SFD as shown in Figure 1.

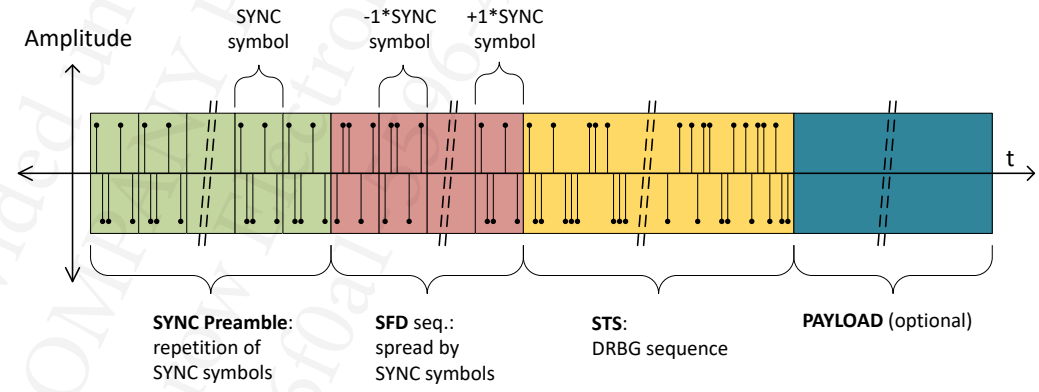


Figure 1. Ranging Frame

It is important that the adversary cannot guess the whole STS sequence by looking at the first part of the sequence. A deterministic random bit generator (DRBG) compliant to NIST SP 800-90A Rev. 1 (see [10] §10.2.1 CTR_DRBG based on AES128) is used to guarantee the randomness of the STS. The DRBG seed and the DRBG advance both have to be agreed upon by initiator and responder upfront on higher protocol level.

The receiver performs the first path detection by correlating the received STS against the expected sequence and captures the correlation peak as a first path estimate.

2 Features and benefits

- IEEE 802.15.4 HRP UWB PHY compliant (see [4])
- On-chip MAC firmware to ease UWB ranging set-up and session control
- Supports SHF UWB bands from 6.0 GHz to 8.5 GHz for worldwide use
- Center Frequency from 6.5 GHz to 8.0 GHz
- Programmable transmitter output power of up to 12 dBm peak
- 128 MHz PRF mode doubles available mean TX power compared to IEEE 802.15.4 (see [4])
- Optimized for Short Frame Mode operation
- Fully coherent receiver for maximum range and accuracy
- Integrates all required RF components (i.e. balun, TRX switch)
- Supply voltage 1.8 V to 3.6 V
- Low energy consumption
- Configurable current limiter for applications with coin cell battery supply
- Data rates of 110 kbps (BPRF), 850 kbps (BRRF), 6.8 Mbps (BPRF), 7.8 Mbps (HPRF)
- Supports 2-way ranging
- IEEE draft 802.15.4z BPRF/HPRF UWB PHY (see [5]) to counter distance manipulation by e.g. Cicada and Preamble Injection attacks
- Scrambled Timestamp Sequence (STS) generation compliant to NIST SP 800-90A [10]
- Integrated I/Q phase and amplitude mismatch compensation
- Narrow Band Interference Cancellation (NBIC) for superior co-channel interference rejection
- XO buffer for sharing the XTAL with another device (e.g. UHF or BLE transceiver)
- 6 mm x 6 mm 40-pin QFN package with 0.5 mm lead pitch and wettable flanks
- AEC-Q100 Qualified
- Small number of external components
- ARM® Cortex-M33 32 Bit processor 55.2 MHz
- ARM® AHB-Lite bus matrix and dual master NS-DMA for fast data transfer
- 256 kByte Non Volatile Memory
- 40 kByte RAM
- 96 kByte ROM
- ARM® TrustZone technology and S-DMA for security
- Advanced Encryption Standard (AES) with 128 bit key and 256 bit key
- Elliptic curve cryptography (ECC) with 256 bit key, 384 bit key and 512 bit key
- Secure Hash Algorithm 2 with 256 bit (SHA2-256)
- Secure Interface (enables GlobalPlatform protocols (see [11]))
- Coprocessor for Cyclic Redundancy Check (CRC) calculation
- True random number generation (TRNG)
- SPI, UART and LIN compatible interface
- API to simplify custom application development
- Several timers for application development
- Low power wake-up timer
- Watch dog timer
- Support high accuracy external temperature sensor for precise crystal temperature drift compensation
- Integrated temperature sensor for crystal temperature drift compensation
- General purpose ADC 10 Bit

3 Applications

The IC supports the following system applications:

- Relay Attack Defense for LF based Passive Keyless Entry Systems (PKE)
- Handsfree smart access based on UWB localization
- Secure Ranging Applications in automotive systems (Remote Park Control)
- Comfort functions in automotive systems

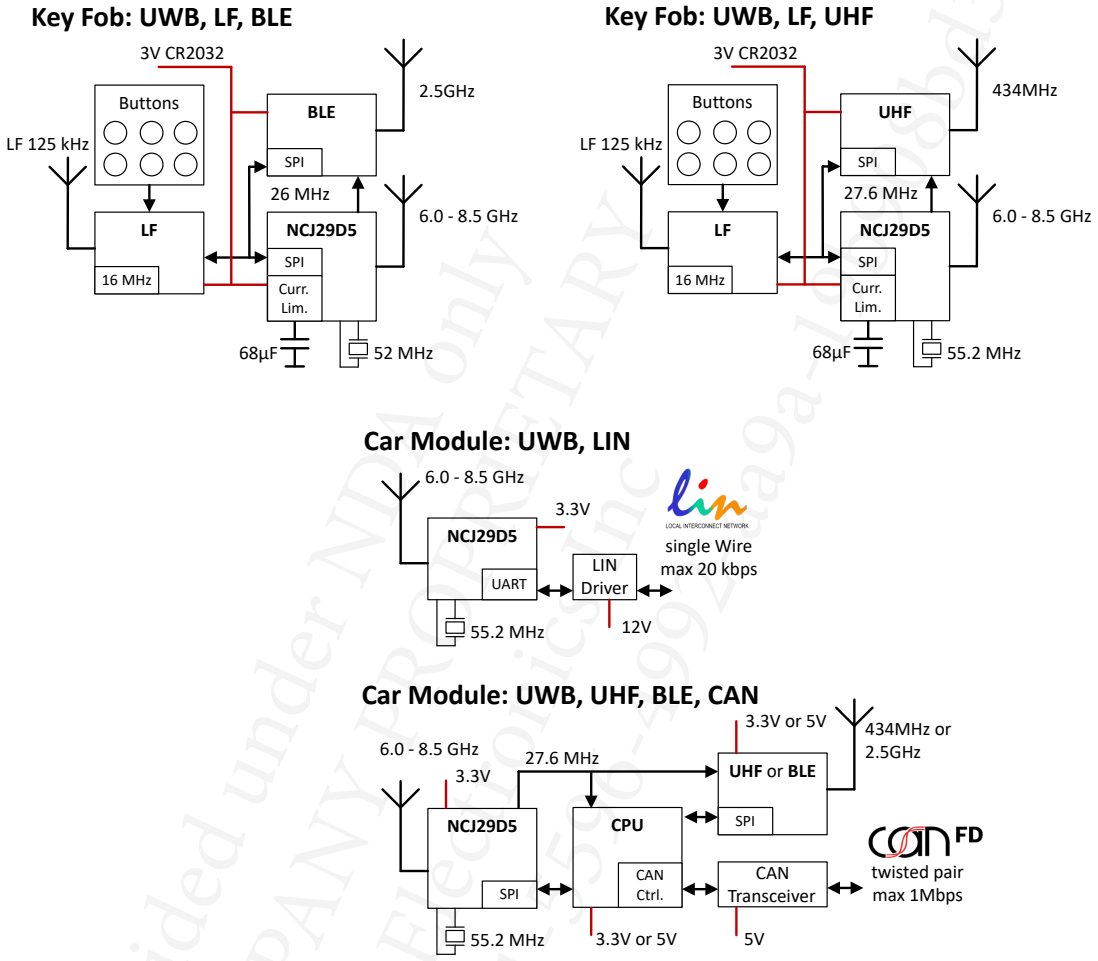


Figure 2. Key Fob and Car Module application

4 Quick reference data

Table 1. Quick reference data

Parameter	Conditions	Min	Typ	Max	Unit
Center Frequency		6.5		8.0	GHz
Ambient Temperature		-40		+115	°C
Supply Voltage		1.8	3.3	3.6	V
Supply Current	Hard Power Down State (HPD) at 3.3V supply		485		nA
	Active State, WFI instruction, CPU subsys. sleep, snapshot unit running on XO (used to recharge energy storage capacitor between ranging frames)		2.07		mA
	Active State, WFI instruction		4.0		mA
	Active State, CPU running		5.1		mA
Supply Current RX	Active State, UWB RX, NBIC ON, high performance		163		mA
	Active State, UWB RX, NBIC OFF, high performance		131		mA
	Active State, UWB RX, NBIC OFF, ECO Min		114		mA
Supply Current TX	Active State, UWB TX, 12dBm output power		115		mA
Max. input level	CW signal, no damage	10			dBm
	UWB signal, functional	-20			dBm
Data Rate		0.110		7.8	Mbps
Pulse Repetition Rate	average	15.6		124.8	MHz
Data Transfer: Payload Sensitivity[1] • AWGN • 20 Byte Payload • no STS • @ 10% FER	IEEE (110 kbps)		-108		dBm
	IEEE (6.8 Mbps)		-95		dBm
	HP (7.8 Mbps)		-94		dBm
	ECO Std (7.8 Mbps)		-94		dBm
	ECO Min (7.8 Mbps)		-93		dBm
Secure Ranging: AWGN Sensitivity [1] • AWGN • STS • no Payload • @ 10% FER	IEEE		-99		dBm
	high performance		-99		dBm
	ECO Std		-96		dBm
	ECO Min		-95		dBm
Secure Ranging: First Path Dynamic Range • 2 Tap Channel • STS • Main tap power = nominal First Path Sensitivity + 45dB	IEEE		32		dB
	high performance		37		dB
	ECO Std		34		dB
	ECO Min		31		dB

Table 1. Quick reference data*...continued*

Parameter	Conditions	Min	Typ	Max	Unit
Secure Ranging: First Path Sensitivity [1] • 2 Tap Channel • STS • Main tap power = first tap power + 15dB	IEEE		-107		dBm
	high performance		-110		dBm
	ECO Std		-107		dBm
	ECO Min		-102		dBm
Secure Ranging: Energy per RX frame [2] • 2V supply • STS • no Payload	high performance, NBIC ON		38		µJ
	high performance, NBIC OFF		31		µJ
	ECO Std, NBIC OFF		15		µJ
	ECO Min, NBIC OFF		10		µJ
Secure Ranging: Energy per TX frame [2] • 2V supply • 12dBm output power • STS • no Payload	high performance		27		µJ
	ECO Std		14		µJ
	ECO Min		10		µJ
Secure Ranging: ToA accuracy • AWGN • 95% of results within limit	high performance, ECO Std, ECO Min		+/-10		cm
Double Sided Pulse Band Width	10 dB attenuation	500			MHz
Non Volatile Memory	reserved for customer application and MAC firmware	128		128	kByte
Start-up time	from wake-up or reset release to start of application execution		1.4		ms
Temperature sensor tolerance		-7		+4	°C
ESD HBM	1500 Ω, 100 pF	2			kV
ESD CDM		500			V
Crystal oscillator frequency[3]	XTAL		52.0 or 55.2		MHz
Supply current XTAL_OUT mode	DPD, XO running, external clock without load		550		µA

[1] Measured in Channel 9 (see [4], fc=7987.2MHz); Sensitivity is approximately 2dB better in channel 5 (see [4], fc=6489.6MHz) than in channel 9
[2] From the beginning of the frame until the end of the frame (i.e. excluding start-up, TX pre-processing, RX ToA post-processing and shut-down).
[3] The use of a 55.2 MHz XTAL is recommended. The use of a 38.4 MHz TCXO is also supported.

Table 2 defines the performance modes used in Table 1.

Table 2. Performance mode definition

	IEEE 110 kbps[1]	IEEE 6.8 Mbps[2]	high performance (HP)[3]	ECO Std[3]	ECO Min[4]	unit
Preamble symbol length	508	508	364	364	364	Chips
Preamble symbol type	ternary	ternary	ternary	ternary	ternary	

Table 2. Performance mode definition*...continued*

	IEEE 110 kbps[1]	IEEE 6.8 Mbps[2]	high performance (HP)[3]	ECO Std[3]	ECO Min[4]	unit
Preamble length	1024	64	64	32	32	symbols
SFD length	64	8	8	4	4	symbols
STS AES128 bit	N/A	4096	8192	4096	2048	bit
STS length	N/A	32768 or OFF	32768 or OFF	16384 or OFF	8192 or OFF	Chips
STS type	N/A	binary	binary	binary	binary	
PHR	ON	ON or OFF	ON or OFF	ON or OFF	ON or OFF	
PHR data rate	0.11	0.85	7.8	7.8	7.8	Mbps
Payload	ON	ON or OFF	ON or OFF	ON or OFF	ON or OFF	
Pulse repetition frequency	62.4	62.4	124.8	124.8	124.8	MHz
Payload data rate	0.11	6.8	7.8	7.8	7.8	Mbps
Rx oversampling rate	2x	2x	2x	2x	1x	499.2 MHz

[1] Compliant to IEEE 802.15.4 HRP UWB PHY (see [4])
[2] Compliant to BPRF mode in IEEE draft 802.15.4z BPRF/HPRF UWB PHY (see [5]) .
[3] Compliant to the HRP-ERDEV HPRF mode with 124.8 MHz PRF and the optional HRP-ERDEV convolutional encoder (where Reed-Solomon coding is not applied) as defined in IEEE draft 802.15.4z BPRF/HPRF UWB PHY (see [5]§16.3.4.3 Table 56) .
[4] Not compliant to IEEE draft 802.15.4z BPRF/HPRF UWB PHY (see [5]) due to the reduced STS length.

5 Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
NCJ29D5DHN	HVQFN40	Ultra Wideband Transceiver with MAC support; Plastic thermal enhanced very thin quad flat package; no leads; 40terminals; body 6 x 6 x 0.85 mm; terminal pitch 0.5 mm; wettable flanks	SOT618-7

The MAC Layer and a Software Development Kit (SDK) can be downloaded from https://www.nxp.com/.

6 Marking

Table 4. Marking information

Line	Example	Description
A	J29D5x	J29D5 = Type number x = unique identifier
B1	** xx	* = Diffusion lot number (e.g. 11) x = Assembly ID (e.g. 01)
B2	sS938*	s = Manufacturer Code GF S = Assembly Centre Kaohsiung yww = Date Code (y = year, w = calendar week) * = Release Status X = customer engineering sample Y = customer qualification sample 0 = released sample
C	** xxx	* = Mask (e.g. B0) x = ROM code (e.g. 002)
D	********	* = Serial ID

7 Block diagram

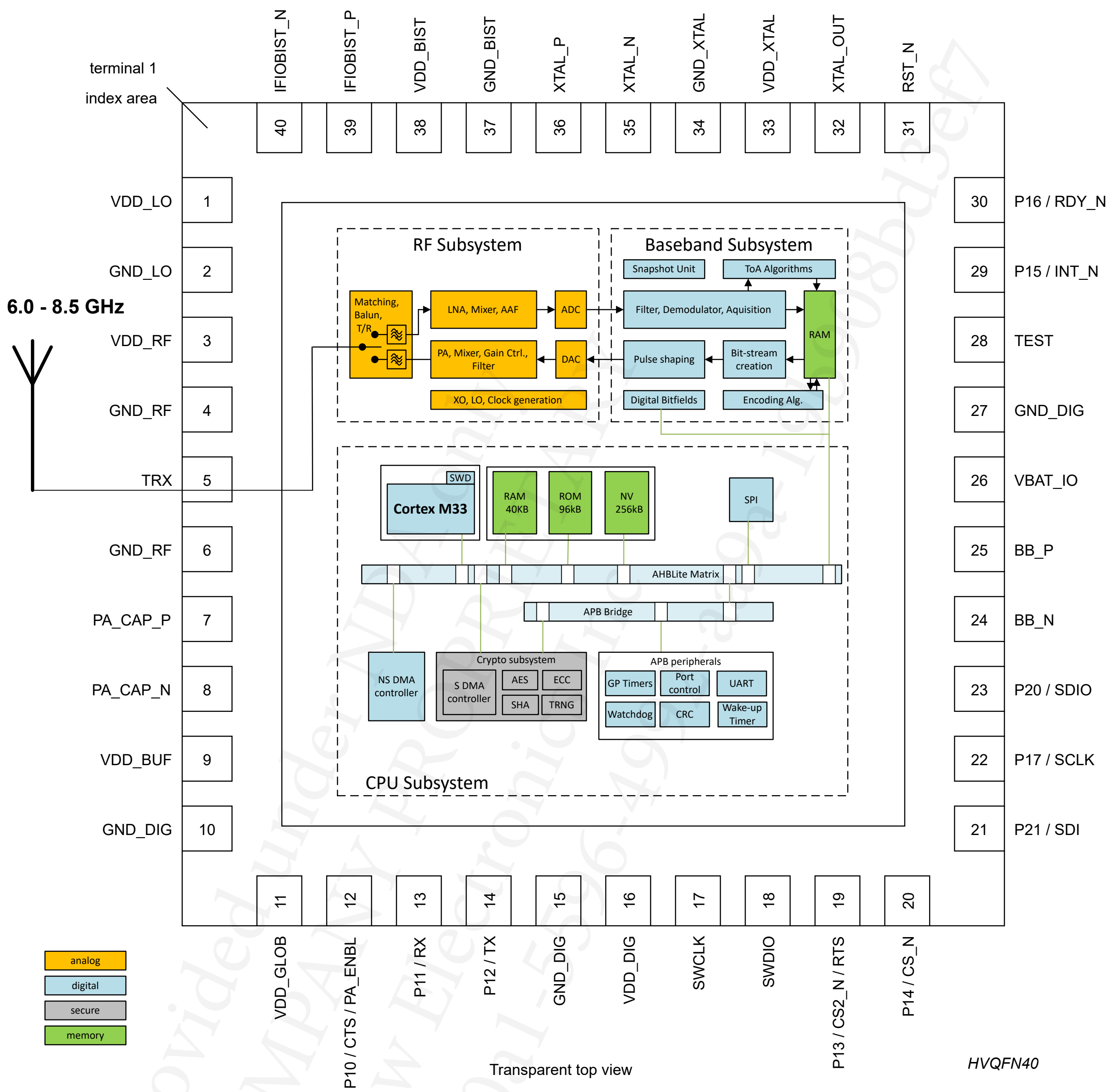


Figure 3. Block diagram

8 Pinning information

The circuit is packaged in a HVQFN40 with wettable flanks.

8.1 Pinning

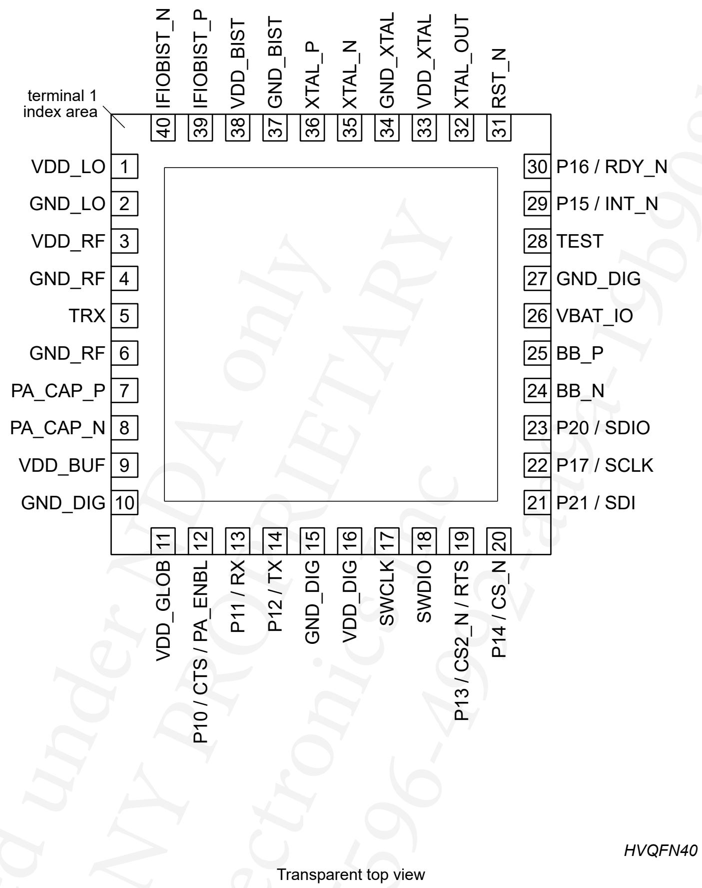


Figure 4. Pinout HVQFN40

8.1.1 Pin 1 keep out area

For the purpose of package orientation, so called "pin 1" identification is included. This can either be as an additional small pin / pad as shown in design 1 (left) of Figure 5, or a notch in the die pad as shown in design 2 (right) of Figure 5.

Note that the pin 1 identifier is electrically connected to the ground plate.

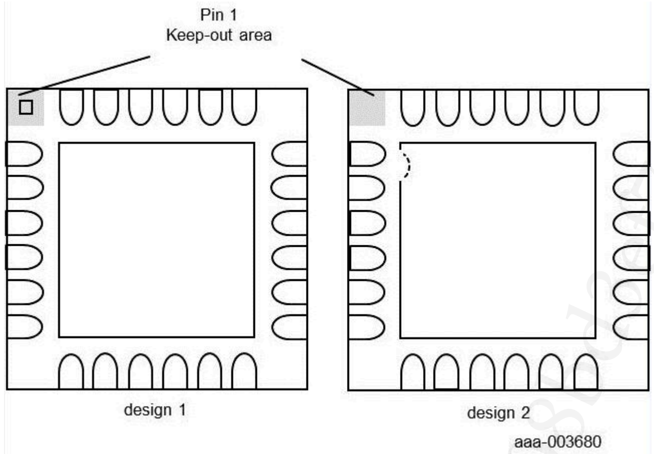


Figure 5. Pin 1 keep out area

8.2 Pin description

Table 5. Pinning description

Symbol	Pin	Description
VDD_LO	1	Power supply for local oscillator generation of the analog receiver and transmitter
GND_LO	2	Ground
VDD_RF	3	Power supply for analog receiver and transmitter
GND_RF	4	Ground
TRX	5	Single-ended, RF receiver input and RF transmitter output, a DC level of 2.1V is used for transmission
GND_RF	6	Ground
PA_CAP_P [1]	7	External decoupling capacitor between pin 7 and 8. 100 nF
PA_CAP_N [1]	8	External decoupling capacitor between pin 7 and 8. 100 nF
VDD_BUF	9	Internally connected to VBAT_IO (pin 26) via programmable current limiter, supply for global LDO and PA
GND_DIG	10	Ground (digital)
VDD_GLOB	11	Output voltage of the global LDO, 2.1V typical
P10 / CTS / PA_ENBL [2]	12	GPIO CTS - "Clear To Send" in UART operation PA_ENBL - Gating signal for an optional external PA
P11 / RX [2]	13	GPIO RX - Data input in LIN/UART operation (e.g. connected to the output of the LIN transceiver)
P12 / TX [2]	14	GPIO TX - Data output in LIN/UART operation (e.g. connected to the input of the LIN transceiver)
GND_DIG	15	Ground (digital)
VDD_DIG	16	Power supply for digital domain; Connect to VDD_BUF on PCB
SWCLK	17	Serial Wire Debug (SWD) clock, internal pull-up resistor

Table 5. Pinning description*...continued*

Symbol	Pin	Description
SWDIO	18	Serial Wire Debug (SWD) data, internal pull-up resistor
P13 / CS2_N / RTS [2]	19	GPIO CS2_N - Second Chip Select (active low) output in SPI Master operation RTS - "Request To Send" in UART operation
P14 / CS_N [2]	20	GPIO CS_N - Chip Select (active low); output in SPI Master operation; input in SPI Slave operation
P21 / SDI [2]	21	GPIO SDI - Data input for SPI full duplex operation
P17 / SCLK [2]	22	GPIO SCLK - Data clock for SPI operation; output in SPI Master operation; input in SPI Slave operation
P20 / SDIO [2]	23	GPIO SDIO - Data I/O for SPI operation; output in full duplex operation; input/output in half duplex operation
BB_N [3]	24	External decoupling capacitor between pin 24 and 25. 470 nF
BB_P [3]	25	External decoupling capacitor between pin 24 and 25. 470 nF
VBAT_IO	26	Power supply for digital I/Os and power supply for the chip via current limiter; Current limiter connected between pin 26 and pin 9 (VDD_BUF)
GND_DIG	27	Ground (digital)
TEST [4]	28	Test pin (must be connected to ground in the application)
P15 / INT_N [2]	29	GPIO INT_N - Interrupt output (active low) in 6-wire SPI operation
P16 / RDY_N [2]	30	GPIO RDY_N - Ready output (active low) in 6-wire SPI operation
RST_N [5]	31	Reset input (active low), internal pull-up resistor. To perform a reset, RST_N shall be active for at least 5 us.
XTAL_OUT [6]	32	Clock Reference (typical 27.6MHz) for external IC. XTAL clock output buffer, optionally divided. Trapezoid-wave with configurable slope to guaranty minimum 0.6Vpp at typical 27.6MHz when capacitive load (i.e PCB) is not higher 10pF. This pin can be left OPEN or be connected to GND. It should NOT be pulled to VDD.
VDD_XTAL	33	Power supply for XTAL; Connect to VDD_BUF on PCB
GND_XTAL	34	Ground
XTAL_N	35	External crystal (55.2 MHz typical) connected between pins 35 and 36
XTAL_P	36	External crystal (55.2 MHz typical) connected between pins 35 and 36
GND_BIST	37	Ground
VDD_BIST	38	Power supply for BIST, ADC, DAC, system clock generation
IFIOBIST_P	39	Pin for supplying an external resistive voltage divider with NTC for temperature sensing. Connect Pins 39 and 40 (IFIOBIST_N resp. _P) to ground in case they are not needed for application.

Table 5. Pinning description*...continued*

Symbol	Pin	Description
IFIOBIST_N	40	Pin for sensing the external temperature sensor voltage with internal ADC. Connect Pins 39 and 40 (IFIOBIST_N resp. _P) to ground in case they are not needed for application.

[1] PA_CAP_P and PA_CAP_N shall not be pulled to high voltages nor to GND.
[2] Unused GPIO pins should be left open.
[3] BB_P and BB_N shall not be pulled to high voltages nor to GND.
[4] Pin TEST must be connected to ground in the application.
[5] RST_N shall be connected only with a 4.7 kΩ resistor in series.
[6] The frequency of the crystal clock output signal is not corrected for temperature drift.

9 Design Information

In this chapter, high level information will be presented about the internal architecture, features, programming options and way of working for several of the core functional units of the device. Detailed information can be found in the User Manual (see [1]).

9.1 UWB Customized Device

The UWB device firmware offers the opportunity to implement a customized application software. Therefore, the UWB device firmware offers the following application programmable interface (API):

- Software interface to configure and control the device
  - Direct access to hardware peripheral registers (SPI, UART, Timers)
  - Access to persistant memory
  - Optional software libraries for use in customized application to control hardware peripherals (e.g. Timers, SPI)
  - Secure channel protocols
- Software interface to support ranging applications including key management for encryption on the physical channel
- In-the-field software update interface
  - Update UWB device firmware
  - Update customized application software

The software interface abstracts the hardware functions of the device, and extends them to powerful system functions. The application can call and execute these functions to implement a complex ranging protocol. The Programmer's Manual (see [3]) gives guidance on how to program the device, and refers to Compiled HTML Help (CHM) files documenting the API functions available to the customized application. The device also offers powerful debug capabilities for developing a customized application software.

The device offers a Software Update Program (SWUP) method to perform secure in-the-field software updates. The Software update program offers an API for the application to activate the update process. Moreover, it offers an API for custom wired communication interfaces to be used during the update process. Alternatively, an SPI based communication interface is available to interact with SWUP, as described in the SWUP User Manual (see [2]).

Figure 6 illustrates the external interfaces of the device and internal software interfaces for the customized application. A host accesses the device via the external SPI or UART interface and interacts with the customized application.

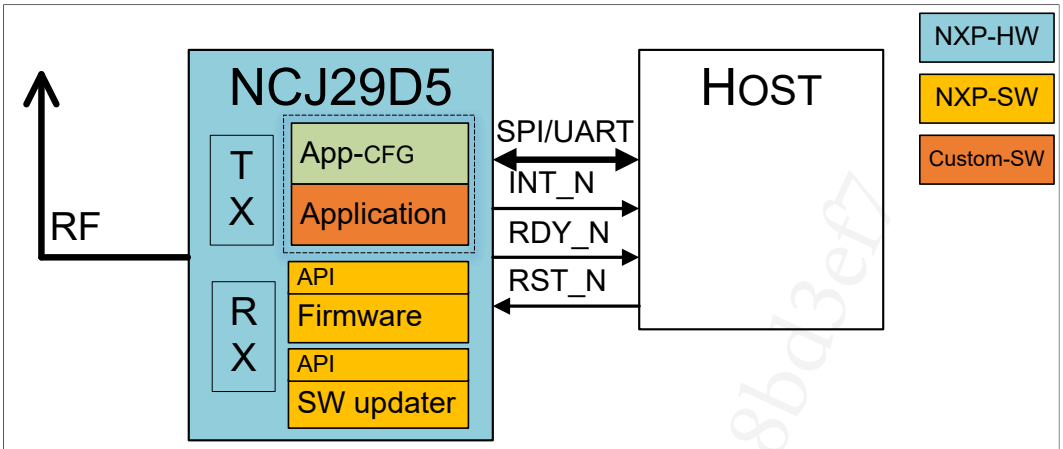


Figure 6. Customized system diagram

9.2 RF Subsystem

The RF subsystem is the analog RF frontend of the device. It integrates all RF components required to perform UWB data transfer and ranging operations in the band from 6.0 GHz to 8.5 GHz. A 50Ω UWB antenna has to be connected via a matching circuit.

The RF RX comprises the following functions:

- LNA
- Mixer
- Automatic Gain Control
- Anti-Aliasing Filter (AAF)
- 8-Bit ADC running at 1GHz sampling rate

The RF TX comprises the following functions:

- 7-Bit DAC running at 2 GHz
- Reconstruction Filter
- Mixer
- PA Gain Control
- PA

The RF subsystem also comprises the following additional functions:

- XO clock and buffer
- Fractional System PLL (SYS-PLL) generating the clock for DAC, ADC, RF-PLL and digital baseband domain
- Fractional RF PLL (RfPll) generating the LO
- Matching network
- Balun
- TRX switch

9.3 Baseband Subsystem

The baseband subsystem implements advanced digital RX algorithms for data transfer and time of arrival (ToA) measurement. Flexible TX encoding and frame generation functions. The Baseband Subsystem is designed to transmit or receive a frame at the time. The scheduling of complete ranging sequences is the task of the CPU.

Figure 7 shows a block diagram of the Baseband Subysystem.

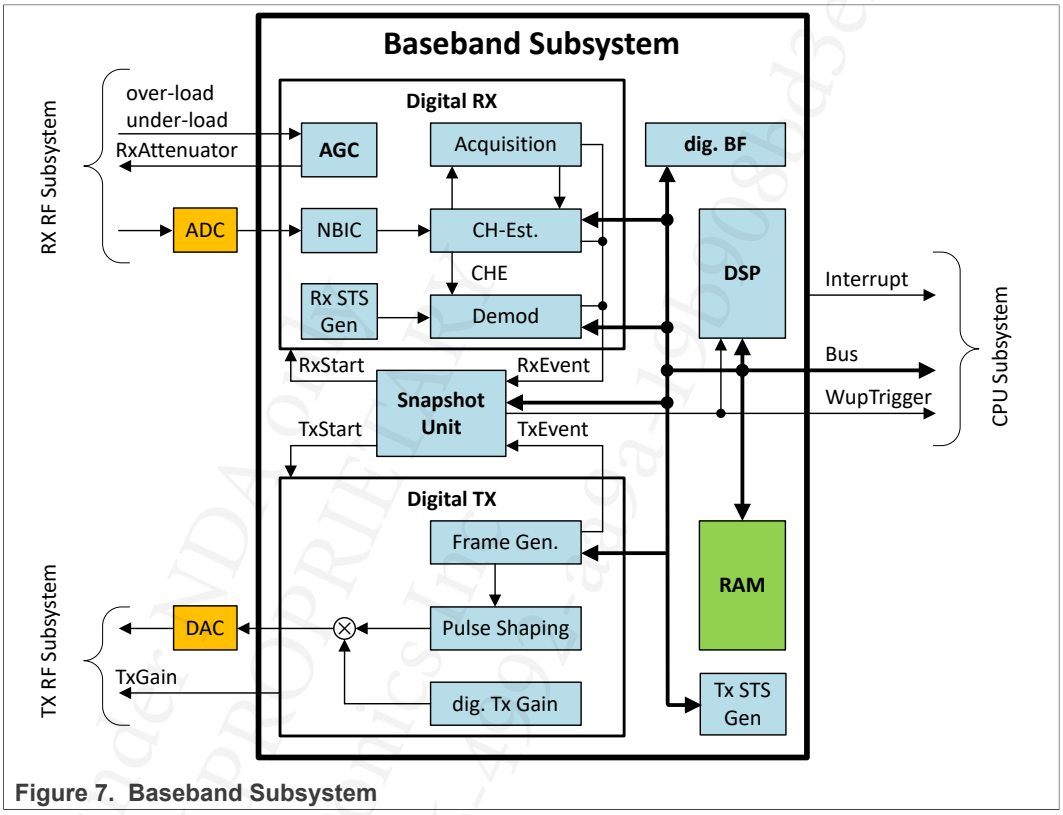


Figure 7. Baseband Subsystem

The digital RX is initialized and configured by the CPU. It is designed to receive one frame at the time and to generate an interrupt to the CPU once it has received a frame. The CPU can then read the decoded payload and timestamp information.

The digital RX comprises the following functions:

- Acquisition of frequency offset and timing offset during the preamble part of the frame (SYNC)
- Detection of the Start of Frame Delimiter (SFD)
- Time of Arrival (ToA) measurement
  - For secure ranging applications the ToA algorithm operates on the STS
  - The expected STS sequence is generated by dedicated HW (Tx / Rx STS Gen)
  - For non-secure ranging applications the STS is not transmitted and the ToA algorithm operates on the SYNC
- Physical Header (PHR) demodulation
- Payload demodulation
- Viterbi Decoding
- Reed Solomon (RS) Decoding

- SECDED Decoding
- Narrow Band Interference Cancellation (NBIC) rejects in-band interferer

The digital TX is initialized and configured by the CPU. It is designed to transmit one frame at the time and to generate and interrupt the CPU once it has transmitted a frame.

The digital TX comprises the following functions:

- Convolutional Encoding
- RS Encoding
- SECDED Encoding
- STS sequence generation
- Bit-stream creation (SYNC, SFD, STS, PHR, Payload)
- Pulse shaping with a programmable FIR filter

The Snapshot Unit implements the ranging timer. The CPU SW has to combine the timestamps captured due to RX and TX events with the ToA estimate generated by the digital RX to calculate the precise timestamp information needed in the ranging protocol.

The Snapshot Unit comprises the following functions:

- Precise trigger for delayed RX (RxStart)
- Precise trigger for delayed TX (TxStart)
- Capture time when a frame was received (RxEvent)
- Capture time when a frame was transmitted (TxEvent)
- Wake-Up the DSP (WupTrigger)
- Wake-Up the CPU (WupTrigger)

9.4 CPU Subsystem

The digital control of the device is done with an ARM® Cortex®-M33 processor (see [6]). The 32-bit microcontroller implements the ARM® TrustZone extension (see [7]), which is based on ARM®v8-M architecture (see [8]). It is designed to provide security for low power and high performance applications.

The CPU has optimized peripherals to facilitate quick and efficient control of the baseband subsystem and the analog RF subsystem. Timers and mathematical units are also implemented in hardware to allow the CPU to concentrate upon the main application level challenges. Dedicated hardware blocks implement strong cypher functions and data movement and thus increase the computing power available for the user application.

9.4.1 Serial Peripheral Interface (SPI)

A single serial peripheral interface (SPI) block is provided. It supports the following key features.

- Master and slave operation
- Data transmissions of 1 to 16 bit supported directly. Larger frames supported by software
- The SPI building block supports separate transmit and receive FIFO buffers with 8 entries each with 16 bit width
- DMA transfers are supported: SPI transmit and receive functions can be operated with the system DMA controller
- Data can be transmitted to a slave without the need to read incoming data
- The device supports wake-up from power saving modes through events on the SPI interface

9.4.2 LIN/UART Serial Interface

A LIN/UART Serial Interface is available for data communications, monitoring, and control. The module features dedicated HW support for LIN operation. But it can also be configured as a universal asynchronous receive / transmit (UART) interface. The supported high level features include

- LIN operation
  - LIN Protocol Handler
  - Master mode
  - Slave mode
  - LIN message buffer
  - Filtering Unit (slave)
  - Re-synchronization (slave)
  - Enhanced error detection
- Standard UART/SCI mode
  - Full duplex
  - 8-bit / 9-bit
  - Even / Odd parity

9.4.3 Clock Generation

All internal clock signals required for RF communication are derived from a quartz crystal oscillator. This includes clocks required for baseband signal processing as well as the RF local oscillator signal, which defines the actual radio carrier frequency.

An external crystal quartz device is required, which defines the basic reference clock signal frequency. Alternatively, a reference signal provided by a temperature compensated crystal oscillator (TCXO) can also be used.

Clock signal management ensures that clock signals not currently used for operation of the device will be disabled in order to conserve power.

9.4.4 General Purpose Timers

Four general purpose timers are provided with level triggered interrupt to the main CPU. They operate at system clock with a prescaler shared among all four timers. The timers can each be programmed for single-shot or free running down counter operation. The general purpose timer registers are each 32 bit wide.

9.4.5 Watchdog Timer

The watchdog timer circuit generates a reset output signal in case it is not properly reset within a pre-programmed time. It uses a clock that is independent from the CPU subsystem. The watchdog timeout period can be specified with a resolution of 100µs.

After the watchdog is configured, the watchdog can be locked to protect against unintended reconfiguration. Once it is locked, the timeout period can no longer be changed. The SW can however still restart the watchdog, before it expires.

As an additional feature, the watchdog timer supports a "timeout pre-emption" function, which causes an interrupt when the watchdog timer counter reaches a pre-defined value just before it expires.

9.4.6 Wake-up Timer

The wake-up timer can be used to wake-up the device from DPD mode after a specified time interval. The wake-up timer uses a crystal calibrated divided low-power FRO as clock source. The wake-up time generation is configurable up to a maximum of 55 minutes. A time counter frequency of 20 kHz or 40 kHz can be selected. The wake-up timer register is 26 bit wide.

9.4.7 Direct Memory Access (DMA)

The direct memory access controller supports fast data transfers without causing any load on the main CPU. It is connected to the internal Advanced High-Performance Bus ("AHB"). The DMA controller is represented as a single slave on the AHB for programming and two masters for data transfers.

A total of eight DMA channels are provided by the DMA controller. Direct memory access can be used as per bus connection.

Besides a generally available Non-Secure DMA controller, there is also a Secure DMA controller, which is not available for general programming and reserved for device firmware internal uses.

9.4.8 Port Control Block

Ten device pins are designated as general purpose input / output pins ("GPIO pins"). The port control block handles their specific configuration options, when used as GPIO pin. The supported configuration options include

- Selection if to be used as input or output pin
- Selection of resistor pull-up, pull-down, or no resistor when programmed as input pin
- Wake-up detection in DPD mode / interrupt option on all GPIO pins with enable registers
- CS_N, RX and TRX provide Wake-up detection in HPD mode
- GPIO configurations are unaffected by DPD and HPD modes

On reset, wake-up from HPD and watchdog expiry, all GPIO pins are configured as input pins with pull-up resistor enabled.

9.4.9 Cryptography Support Block

A dedicated hardware accelerator supports computations used in symmetric key and public key cryptography. It efficiently performs basic arithmetic and logical operations on multi-precision integer numbers. A typical use of this block would be in cryptography using the Advanced Encryption Standard (AES) or the Elliptic Curve Cryptography (ECC) algorithm. Computation of SHA hashes as well as true random number generation are also available.

- Advanced Encryption Standard (AES) with 128 bit key and 256 bit key
- Elliptic Curve Cryptography (ECC) with 256 bit key, 384 bit key, and 512 bit key
- Secure Hash Algorithm 2 with 256 bit (SHA2-256)

The cryptography support block is connected to both, the AHB and APB bus. The secure CPU can access these blocks, data transfers can be executed efficiently via the Secure DMA Controller.

The application can access the hardware accelerator via dedicated secure API ROM functions. The application can use these functions to implement a Secure Interface (e.g. GlobalPlatform SCP11, SCP03 protocols (see [[11]]))

9.4.10 Cyclic Redundancy Check (CRC)

Operations associated with message integrity and cyclic redundancy check parity bits are supported by the CRC building block. The block supports CRC generation as well as CRC verification / checking functionality. The main features include

- Configurable CRC polynomial from CRC1 to CRC32
- Internal 32 bit CRC data register
- Configurable CRC start value
- Parallel CRC calculation for 8 bit input data
- Support for LSBit / MSBit first aligned input data

9.4.11 Temperature measurement

The temperature can be measured in two ways, either with the internal temperature sensor or using an external temperature sensor, connected to the on-chip 10 bit ADC. Access to the temperature measurement subsystem is through software API.

An external temperature sensor can be used, connected as shown in Figure 8, with connections made to pins IFIOBIST_N and IFIOBIST_P.

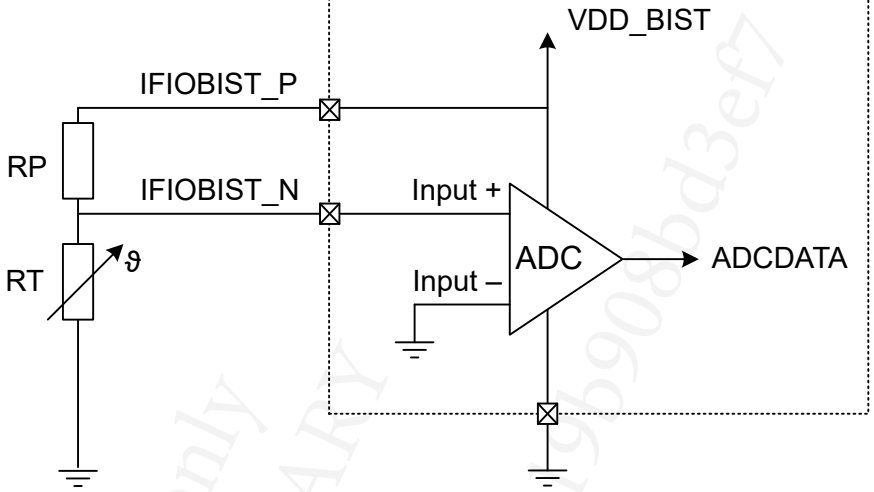


Figure 8. External temperature sensor measurement

9.4.12 Voltage Measurement

The device facilitates the measurement of several voltages. Access to the voltage measurement function is through software API. Dedicated API functions are provided to perform these device internal measurements. No external components are required to perform these measurements. The following voltages can be measured:

- Voltage on pin VBAT_IO
  This feature is intended to be used to monitor the battery supply voltage.
- Voltage on pin VDD_BUF
  This feature is intended to be used in Key Fob applications, to monitor the available charge in the energy storage capacitor.
- Voltage on pin VDD_GLOB
- Voltage on pin VDD_DIG

9.4.13 Serial Wire Debug (SWD) Interface

The in-circuit Serial Wire Debug (SWD) interface (see [9]) is intended for non intrusive debug operation during application program development. The interface allows manipulating the embedded peripherals and provides means to initialize the NV. It is implemented as two-wire serial interface using the dedicated pins SWDIO and SWCLK. The NV has a programming granularity of 512 byte.

The SWD Interface is available when the device is set into INIT mode, which is the factory default setting. When performing system tests and field trials, the device shall be set to PROTECTED mode. Latter one disables debug features and the SWD Interface. The device may be forced back into INIT mode by a dedicated command.

9.5 Power management

9.5.1 Modes of operation

The device supports operation in a 3 V environment supporting the following supply use cases:

1. Device and digital interface supplied with regulated 3 V (3.3 V) supply
   - Digital signaling between all devices in the system is done at 3 V (3.3 V) level.
2. Device and digital interface supplied with a 3 V battery
   - Digital signaling between all devices in the system is done at battery voltage level.
   - An energy storage capacitor is required to deliver the required peak current during frame reception and frame transmission.

Connection diagrams for these different use cases are depicted in Figure 9.

9.5.2 External power supply domains

Several power supply pins are present to provide the required supply isolation between various RF, analog and digital blocks (external power supply domains). The device can either be supplied via a regulator output or a battery.

When the device is supplied via a regulator output, then the 3V power supply pins shall be directly connected to the regulator output. The 2.1V power supply pins shall be connected to VDD_GLOB. Note that the Global LDO shall only be used to supply NCJ29D5, it shall not be used to supply another device.

When the device is supplied via a battery, then the current limiter should be employed to limit the battery stress due to high peak currents. Only the VBAT_IO power supply pin has to be directly connected to the battery. The VDD_BUF is the output of the current limiter, it supplies both, VDD_XTAL and VDD_DIG in this case. Note that the current limiter shall only be used for NCJ29D5 , it shall not be used to limit the supply current of another device. The 2.1V power supply pins have to be connected to VDD_GLOB.

Adequate blocking capacitors have to be connected to the external supply pins. External supply switches are not required.

Table 6. External power supply domains

Power supply pin	Voltage range[1]	Description
VBAT_IO, GND_DIG	3 V	Power supply for the I/O port pins, the power-on reset circuit, the power state logic, the I/O port control latches and the wake-up timer.
VDD_BUF	3 V	Main power supply domain of the device; Note that the transition out of DPD STATE and RESET STATE is only completed, when VBAT_IO - VDD_BUF < ~20mV[2] (i.e. fob application: wait until energy storage capacitor is fully charged; car application: not relevant as VDD_BUF is connected to VBAT_IO on the PCB; see Figure 9 and Figure 10).
VDD_XTAL, GND_XTAL,	3 V	Power supply for the crystal oscillator.
VDD_DIG; GND_DIG;	3 V	Power supply for the CPU and digital baseband processing.
VDD_GLOB	2.1 V	Regulated power supply output.

Table 6. External power supply domains*...continued*

Power supply pin	Voltage range[1]	Description
VDD_LO; GND_LO; VDD_RF, GND_RF; VDD_BIST; GND_BIST	2.1 V	Power supply for the local oscillator (fractional-N PLL), the radio frontend, and the BIST logic.

[1] Voltage ranges are given here only for information purpose. Please refer to the electrical characteristics for detailed voltage range specification.
[2] A minimum value of 5mV was established via analog PVT simulations.

The external power supply domains with the associated power supply pins are briefly described in the Table 6.

The package HVQFN has an exposed die pad at the back which is intended as heat sink and additional ground connection.

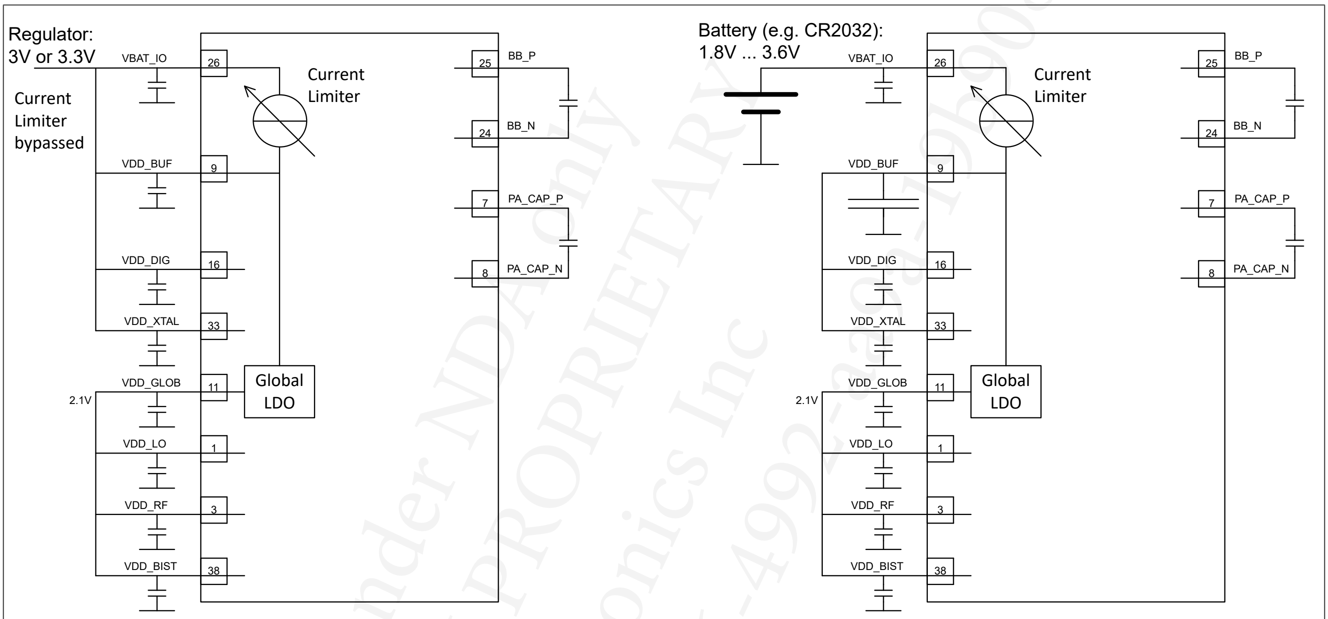


Figure 9. Connection of external power supply domains

9.5.3 Recommended external capacitors in the supply domains

The device is supplied by an external supply with 3 V (3.3 V):

- Pin 1 VDD_LO: 10 nF (± 10%) capacitor
- Pin 3 VDD_RF: 10 nF (± 10%) capacitor
- Between Pin 7 PA_CAP_P and Pin 8 PA_CAP_N: 100 nF (± 10%) capacitor (mandatory)
- Pin 9 VDD_BUF:
  - 100 nF (± 10%) when used on car side
  - 100 µF (± 10%) capacitor is typically required when coin cell battery powered
- Pin 11 VDD_GLOB: 100 nF (± 10%) capacitor
- Pin 16 VDD_DIG: 100 nF (± 10%) capacitor
- Between Pin 24 BB_N and Pin 25 BB_P: 470 nF (± 10%) capacitor (mandatory)
- Pin 26 VBAT_IO: 100 nF (± 10%) capacitor
- Pin 33 VDD_XTAL: 100 nF (± 10%) capacitor
- Pin 38 VDD_BIST: 10 nF (± 10%) capacitor

9.5.4 Power supply states

The device supports the following power states:

- RESET state
  - The CPU performs a boot, when ACTIVE state is entered from RESET state.
- ACTIVE state (normal operation)
- DEEP POWER DOWN (DPD) state (wake-up timer active)
  - SW can choose to retain the CPU RAM before entering DPD.
  - SW can choose to retain the BB RAMs and CPU RAMs and keep the ranging timer running before entering DPD.
  - The CPU Subsystem is reset in DPD state.
  - The CPU performs a boot, when ACTIVE state is entered from DPD state.
- HARD POWER DOWN (HPD) state (lowest power consumption)
  - activate RST_N to wake-up the device
  - CS_N, RX and TX pin can be configured to wake-up the device. The device wakes up, when the level is low on any of the pins configured for wake-up.

The state diagram for the functional power supply states is given in Figure 10. Note that the IC contains the power domains AO, NV, CPU_RET, CPU, BB_RET, BB. Each one has a dedicated monitor. The corresponding outputs are called Power-OK signals. A '1' signals that the LDO of the respective domain is turned on and operational.

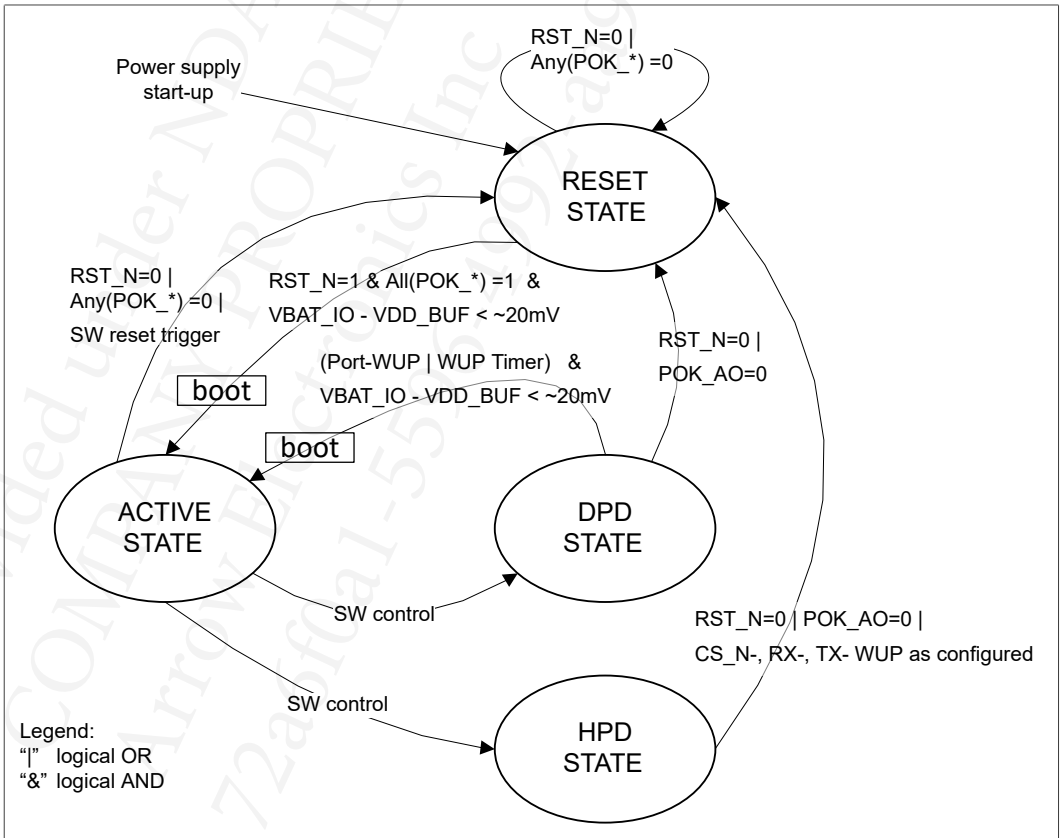


Figure 10. Power supply state diagram

9.5.5 Current Limiter

The current limiter is intended for applications with coin cell battery supply, to maximize the lifetime of the battery. It minimizes battery stress by limiting the maximal current drawn by the IC. The current limit is configurable by SW. Figure 9 shows how the current limiter is connected in the application.

The current limiter comprises the following functions:

- Configurable current limit from 5 mA to 20 mA, in steps of 1 mA
- Limits the battery current drawn from the IC
  - Except for the GPIOs
  - GPIOs are directly supplied by VDD_BAT, to guarantee that the signaling level matches the battery voltage.
- ON mode
  - Current is limited to the configured maximum
  - Automatically selected in RESET state and ACTIVE state
- OFF mode
  - VDD_BUF is disconnected from VDD_IO
  - Can be selected for HPD state
  - Leakage of the energy storage capacitor does not impact the battery current drawn in HPD mode
  - Note that the power management state machine makes sure that the re-boot is only starting once the energy storage capacitor is fully charged. The transition out of RESET STATE is only completed when the difference between VBAT_IO and VDD_BUF is smaller than ~20mV [1] (i.e. fob application: wait until energy storage capacitor is fully charged; car application: not relevant as VDD_BUF is connected to VBAT_IO on the PCB; see Figure 9 and Figure 10).
- CHARGING/CHARGED mode
  - VDD_BUF is connected to VDD_IO.
  - Can be selected for HPD and DPD state.
  - The HW charges the energy storage capacitor with the current limiter enabled.
  - Once the capacitor is charged (i.e. the difference between VBAT_IO and VDD_BUF is smaller than ~20mV [2]), the current limiter is bypassed and the current is no longer limited.
  - The energy storage capacitor remains charged to facilitate a fast wake-up time.

1 A minimum value of 5mV was established via analog PVT simulations.
2 A minimum value of 5mV was established via analog PVT simulations.

9.6 Device modes

The device features the following Device Modes. The Device Modes are maintained and set by SW (see [3]):

- INIT
- PROTECTED
- TAMPERED

The Device Modes affect the overall device behavior, the SWD Interface operation and the user ability to access the NV.

A Device Mode is controlled by a set of configuration bytes, which are located in the NV.

The configuration bytes may not be altered by the user directly, instead, the corresponding command has to be used. Device Mode transitions are protected by a strong cryptographic mechanism.

9.6.1 INIT

When the device is supplied from NXP, it is configured in INIT mode by default.

The INIT mode shall be used during software development only. The SWD Interface is fully operational, enabling the customer to initialize the NV as desired for the application.

9.6.2 PROTECTED

In the moment the device is set into PROTECTED mode, the SWD Interface is disabled. The PROTECTED mode has to be used during system testing and in the final application.

9.6.3 TAMPERED

The TAMPERED mode is entered temporarily during the transition from one device mode to another. If this sequence does not complete successfully, the device remains in TAMPERED mode.

9.7 System routines

9.7.1 Boot routine

The ROM based boot routine is called immediately after battery insertion, device reset or wake-up from DPD or HPD state.

The boot routine executes a sequence of instructions to evaluate the device mode and configures the device, using device protection and configuration flags and passes control to the application code at the boot vector in the NV.

The reset cause is preserved and reported via an API function.

10 Characterization Information

10.1 Limiting values

Table 7. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134) - guaranteed by design

Parameter	Condition	Min	Typ	Max	Unit
Moisture Sensitivity Level (MSL)	2a				
Junction temperature				125	°C
VBAT_IO; Voltage at any digital I/O pin		-0.3		3.6	V
Voltage at digital I/O pins (3.6 V must not be exceeded)		-0.3		VBAT_IO + 0.3	V
VDD_BUF; VDD_XTAL; VDD_DIG	Must not exceed VBAT_IO	-0.3		3.6	V
VDD_LO; VDD_RF; VDD_BIST		-0.3		2.8	V
VDD_GLOB		-0.3		2.8	V
BB_P		-0.3		1.25	V
BB_N		-0.3		0.3	V
XTAL_N; XTAL_P		-0.3		1.25	V
IFIOBIST_N: IFIOBIST_P		-0.3		VDD_RF	V
TRX		-0.3		3.6	V
PA_CAP_P		-0.3		2.4	V
PA_CAP_N		-0.3		0.3	V
XTAL_OUT		-0.3		1.25	V
Maximum input level without damage	CW signal	10			dBm
Maximum input level functional	UWB signal	-20			dBm
NV data retention for the first 1k program/erase (P/E) cycles to a page	[1]	15			Years
NV data retention for the first 10k program/erase (P/E) cycles to a page	[1]	10			Years
NV endurance		10k			P/E cycles
TX on time over lifetime[2]	[1]	657			h
RX on time over lifetime	[1]	6570			h

[1] AEC-Q100-005 measurement method with Ambient mission profile: 6 % @ -40 °C, 20 % @ 25 °C, 65 % @ 85 °C, 5 % @ 105 °C and 4 % @ 115 °C

[2] The minimum TX on time matches the hourly homologation limit defined by ETSI, accumulated over 15 years lifetime. The highest Duty Cycle for LDC in the ETSI standard (see [[12]] §4.5.3) is 0.5% (i.e. LDC of 18s/h). 18s/h * 24h/d * 365d/y * 15y / 3600s/h = 657h

10.2 Recommended operating conditions

Table 8. Recommended operating conditions

Parameter	Condition	Min	Typ	Max	Unit
Parametric ambient temperature range A[1]	• All specification parameters fulfilled	-40	25	105	°C

Table 8. Recommended operating conditions...*continued*

Parameter	Condition	Min	Typ	Max	Unit
Parametric ambient temperature range B[1]	• Device fully functional • Deviating RX and TX characteristics • Depending on the thermal resistance of the module, continuous RX operation may not be supported.	105		115	°C
Supply voltage range A	• All specification parameters fulfilled	2.4	3.3	3.6	V
Supply voltage range B	• Device fully functional • TX PA peak power shall not be set higher than 9dBm, to avoid potential regulatory spectral mask violations. • Deviating RX and TX characteristics	1.8		2.4	V

[1] The maximal junction temperature (Table 7) must not be exceeded. Thermal resistance from die to PCB (Rth_jc) is defined in Table 12.

10.3 Characteristics

10.3.1 General

Table 9. Condition

This table defines conditions used for characterization. They are referred by their ID in the "Note" column in the characteristic tables.

ID	Description
[1]	Tested in production test; -40 °C, 25 °C, 105°C
[2]	Characterized at 1.8 V, 2.4V, 3.3 V, 3.6 V, -40 °C, 25 °C, 105 °C, 115 °C with 32 parts, Crystal type: NX2016SA 55.2MHz EXS00A-CS12398
[3]	Characterized at 1.8 V, 2.4V, 3.3 V, 3.6 V, -40 °C, -20°C, 25 °C, 65°C, 85°C, 105 °C, 115 °C with 32 parts, Crystal type: NX2016SA 55.2MHz EXS00A-CS12398
[4]	Characterized at 3.3 V; -40 °C, 25 °C, 105 °C, 115 °C limited sample size, Crystal type: NX2016SA 55.2MHz EXS00A-CS12398
[5]	Characterized at 3.3 V; -40 °C, 25 °C, 105 °C, 115 °C, ext. clock 55.2MHz
[6]	Guaranteed by design

Table 10. Temperature

This table defines temperatures used for characterization. They are referred by their ID in the "Conditions" column in the characteristic tables.

ID	Description
CT	-40°C
LT	-20°C
RT	+25°C
KT	+65°C
XT	+85°C
MT	+105°C

Table 10. Temperature*...continued*

This table defines temperatures used for characterization. They are referred by their ID in the "Conditions" column in the characteristic tables.

ID	Description
HT	+115°C

Table 11. Scenario definition

This table defines scenarios used for characterization. They are referred by their name throughout the characteristics section.

	IEEE 110 kbps	IEEE 6.8 Mbps		HP (high perf.) 7.8 Mbps		ECO Std 7.8 Mbps		ECO Min 7.8 Mbps		
	data	data	ranging	data	ranging	data	ranging	data	ranging	
Preamble sym. length	508	508		364		364		364		Chips
Preamble symbol	ternary	ternary		ternary		ternary		ternary		
Preamble length	1024	64		64		32		32		symbols
SFD length	64	8		8		4		4		symbols
STS AES128 bit	-	-	4096	-	8192	-	4096	-	2048	bit
STS length	OFF	OFF	32768	OFF	32768	OFF	16384	OFF	8192	Chips
STS type	-	-	binary	-	binary	-	binary	-	binary	
PHR	ON	ON	-	ON	-	ON	-	ON	-	
PHR data rate	0.11	0.85	-	7.8	-	7.8	-	7.8	-	Mbps
Payload	20	20	-	20	-	20	-	20	-	Byte
Pulse repetition freq.	62.4			124.8						MHz
Payload data rate	0.11	6.8	-	7.8	-	7.8	-	7.8	-	Mbps
Rx oversampling	2x							1x		499.2MHz
Tx pulse shape	RRC, β=0.5, minimum phase[1]									

[1] IEEE 6.8 Mbps frames were also validated with a linear phase RRC TX pulse shape with β=0.45, for sensitivity and ToA precision. A RX configuration optimized for this pulse shape was used. Only a minor degradation in sensitivity and ToA precision was measured.

Table 12. Application relevant limits

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
1	Frequency of external reference crystal connected to XTAL_N and XTAL_P			55.2		MHz	[6]
				52.0			
2	Frequency of external TCXO connected to XTAL_N (XTAL_P is not connected)			38.4		MHz	[6]
3	Input voltage level at XTAL_N when XO LDO is disabled or not ready	LDO_XO_OK = 0	-0.1		0.1	V	[6]
4	Duty cycle of external clock input signal XTAL_N		45		55	%	[6]
5	Pin capacitance (XTAL_N to XTAL_P)			2.1		pF	[6]

Table 12. Application relevant limits...*continued*

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
6	Thermal resistance from die to PCB (Rth_jc)	soldered exposed die pad		6		K/W	[6]

10.3.2 RX

Table 13. Interferer definition

Short	Description	Modulation	Comment
J.CW	Continuous wave	none	
J.LTE	LTE signal with 3 Resource Blocks	OFDM	1.62 MHz BW
J.WIFI	WIFI signal	OFDM	160 MHz BW

10.3.2.1 Data Transfer: Payload Sensitivity

Table 14. Characteristics - Data Transfer: Payload Sensitivity CH9

Measurement of RX sensitivity level for

- *AWGN*
- *20 Byte Payload*
- *no STS*
- *@ 10% FER*

Following characteristics are valid for conditions as follows (unless otherwise specified)
T_{amb} = -40 °C to 115 °C , VDD = 1.8 V to 3.6 V, f_C = 7987.2 MHz, crystal = 55.2 MHz
VDD = VBAT_IO, VDD_DIG, VDD_BUF, VDD_XTAL, GPIO pins in defined, non hi-Z, state

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
1	HP 7.8Mbps data frame	CT, RT		-94	-93	dBm	[2]
		MT, HT		-93	-91	dBm	[2]
2	ECO Std 7.8Mbps data frame	CT, RT		-94	-92	dBm	[2]
		MT, HT		-92	-91	dBm	[2]
3	ECO Min 7.8Mbps data frame • Rx oversampling: 1x	CT, RT		-93	-92	dBm	[2]
		MT, HT		-91	-90	dBm	[2]
4	IEEE 6.8Mbps data frame	CT, RT		-95	-94	dBm	[2]
		MT, HT		-93	-92	dBm	[2]
5	IEEE 850kbps data frame	CT, RT		-104	-102	dBm	[2]
		MT, HT		-102	-100	dBm	[2]
6	IEEE 110kbps data frame	CT, RT		-108	-106	dBm	[2]
		MT, HT		-106	-104	dBm	[2]

Table 15. Characteristics - Data Transfer: Payload Sensitivity CH5

Measurement of RX sensitivity level for

- *AWGN*
- *20 Byte Payload*
- *no STS*
- *@ 10% FER*

Following characteristics are valid for conditions as follows (unless otherwise specified)

T_{amb} = -40 °C to 115 °C , VDD = 1.8 V to 3.6 V, f_C = 6489.6 MHz, crystal = 55.2 MHz

VDD = VBAT_IO, VDD_DIG, VDD_BUF, VDD_XTAL, GPIO pins in defined, non hi-Z, state

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
1	HP 7.8Mbps data frame	CT, RT		-96	-95	dBm	[2]
		MT, HT		-95	-93	dBm	[2]
2	ECO Std 7.8Mbps data frame	CT, RT		-95	-94	dBm	[2]
		MT, HT		-94	-92	dBm	[2]
3	ECO Min 7.8Mbps data frame • Rx oversampling: 1x	CT, RT		-94	-93	dBm	[2]
		MT, HT		-93	-92	dBm	[2]
4	IEEE 6.8Mbps data frame	CT, RT		-97	-95	dBm	[2]
		MT, HT		-95	-94	dBm	[2]
5	IEEE 850kbps data frame	CT, RT		-105	-104	dBm	[2]
		MT, HT		-103	-102	dBm	[2]
6	IEEE 110kbps data frame	CT, RT		-110	-108	dBm	[2]
		MT, HT		-108	-106	dBm	[2]

10.3.2.2 Secure Ranging: AWGN Sensitivity

Table 16. Characteristics - Secure Ranging: AWGN Sensitivity CH9

Measurement of RX sensitivity level for

- *AWGN*
- *no Payload*
- *STS*
- *@ 10% FER*

Following characteristics are valid for conditions as follows (unless otherwise specified)

T_{amb} = -40 °C to 115 °C , VDD = 1.8 V to 3.6 V, f_C = 7987.2 MHz, crystal = 55.2 MHz

VDD = VBAT_IO, VDD_DIG, VDD_BUF, VDD_XTAL, GPIO pins in defined, non hi-Z, state

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
1	HP ranging frame	CT, RT		-99	-98	dBm	[2]
		MT, HT		-97	-96	dBm	[2]
2	ECO Std ranging frame	CT, RT		-96	-94	dBm	[2]
		MT, HT		-94	-93	dBm	[2]
3	ECO Min ranging frame • Rx oversampling: 1x	CT, RT		-95	-93	dBm	[2]
		MT, HT		-93	-92	dBm	[2]
4	IEEE ranging frame	CT, RT		-99	-97	dBm	[2]
		MT, HT		-97	-96	dBm	[2]

Table 16. Characteristics - Secure Ranging: AWGN Sensitivity CH9*...continued*

Measurement of RX sensitivity level for

- *AWGN*
- *no Payload*
- *STS*
- *@ 10% FER*

Following characteristics are valid for conditions as follows (unless otherwise specified)

T_{amb} = -40 °C to 115 °C , VDD = 1.8 V to 3.6 V, f_C = 7987.2 MHz, crystal = 55.2 MHz

VDD = VBAT_IO, VDD_DIG, VDD_BUF, VDD_XTAL, GPIO pins in defined, non hi-Z, state

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
5	HP ranging frame • CFO: +/-50ppm	CT, RT		-99	-96	dBm	[2]
		MT, HT		-96	-95	dBm	[2]
6	ECO Std ranging frame • CFO: +/-50ppm	CT, RT		-96	-94	dBm	[2]
		MT, HT		-94	-92	dBm	[2]
7	ECO Min ranging frame • CFO: +/-70ppm • Rx oversampling: 1x	CT, RT		-94	-92	dBm	[2]
		MT, HT		-92	-90	dBm	[2]
8	IEEE ranging frame • CFO: +/-50ppm	CT, RT		-99	-97	dBm	[2]
		MT, HT		-97	-95	dBm	[2]

Table 17. Characteristics - Secure Ranging: AWGN Sensitivity CH5

Measurement of RX sensitivity level for

- *AWGN*
- *no Payload*
- *STS*
- *@ 10% FER*

Following characteristics are valid for conditions as follows (unless otherwise specified)

T_{amb} = -40 °C to 115 °C , VDD = 1.8 V to 3.6 V, f_C = 6489.6 MHz, crystal = 55.2 MHz

VDD = VBAT_IO, VDD_DIG, VDD_BUF, VDD_XTAL, GPIO pins in defined, non hi-Z, state

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
1	HP ranging frame	CT, RT		-101	-99	dBm	[2]
		MT, HT		-99	-98	dBm	[2]
2	ECO Std ranging frame	CT, RT		-98	-96	dBm	[2]
		MT, HT		-96	-94	dBm	[2]
3	ECO Min ranging frame • Rx oversampling: 1x	CT, RT		-97	-94	dBm	[2]
		MT, HT		-95	-93	dBm	[2]
4	IEEE ranging frame	CT, RT		-100	-99	dBm	[2]
		MT, HT		-99	-97	dBm	[2]
5	HP ranging frame • CFO: +/-50ppm	CT, RT		-100	-97	dBm	[2]
		MT, HT		-98	-96	dBm	[2]
6	ECO Std ranging frame • CFO: +/-50ppm	CT, RT		-97	-95	dBm	[2]
		MT, HT		-96	-93	dBm	[2]

Table 17. Characteristics - Secure Ranging: AWGN Sensitivity CH5*...continued*

Measurement of RX sensitivity level for

- *AWGN*
- *no Payload*
- *STS*
- *@ 10% FER*

Following characteristics are valid for conditions as follows (unless otherwise specified)

T_{amb} = -40 °C to 115 °C , VDD = 1.8 V to 3.6 V, f_C = 6489.6 MHz, crystal = 55.2 MHz

VDD = VBAT_IO, VDD_DIG, VDD_BUF, VDD_XTAL, GPIO pins in defined, non hi-Z, state

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
7	ECO Min ranging frame • CFO: +/-70ppm • Rx oversampling: 1x	CT, RT		-96	-93	dBm	[2]
		MT, HT		-94	-90	dBm	[2]
8	IEEE ranging frame • CFO: +/-50ppm	CT, RT		-100	-99	dBm	[2]
		MT, HT		-99	-97	dBm	[2]

10.3.2.3 Secure Ranging: First Path Dynamic Range

Table 18. Characteristics - Secure Ranging: First Path Dynamic Range

Measurement of RX sensitivity level for

- *2 Tap Channel (first path 12 ns earlier than main path)*
- *no Payload*
- *STS*
- *@ 10% first path FER*
- *main tap power = nominal First Path Sensitivity level + 45dB*
- *Security Level = 4*

Following characteristics are valid for conditions as follows (unless otherwise specified)

T_{amb} = -40 °C to 115 °C , VDD = 1.8 V to 3.6 V, f_C = 6489.6 MHz or 7987.2 MHz, crystal = 55.2 MHz

VDD = VBAT_IO, VDD_DIG, VDD_BUF, VDD_XTAL, GPIO pins in defined, non hi-Z, state

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
1	HP ranging frame		35	37		dB	[2]
2	ECO Std ranging frame		32	34		dB	[2]
3	ECO Min ranging frame • Rx oversampling: 1x		28	31		dB	[2]
4	IEEE ranging frame		29	32		dB	[2]

10.3.2.4 Secure Ranging: First Path Sensitivity

Table 19. Characteristics - Secure Ranging: First Path Sensitivity CH9

Measurement of RX sensitivity level for

- *2 Tap Channel (first path 7 ns earlier than main path)*
- *no Payload*
- *STS*
- *@ 10% first path FER*
- *Main tap power = first tap power + 15dB*
- *Security Level = 4*

Following characteristics are valid for conditions as follows (unless otherwise specified)

T_{amb} = -40 °C to 115 °C , VDD = 1.8 V to 3.6 V, f_C = 7987.2 MHz, crystal = 55.2 MHz

VDD = VBAT_IO, VDD_DIG, VDD_BUF, VDD_XTAL, GPIO pins in defined, non hi-Z, state

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
1	HP ranging frame	CT, RT		-110	-108	dBm	[2]
		MT, HT		-108	-107	dBm	[2]
2	ECO Std ranging frame	CT, RT		-107	-105	dBm	[2]
		MT, HT		-105	-104	dBm	[2]
3	ECO Min ranging frame • Rx oversampling: 1x	CT, RT		-102	-100	dBm	[2]
		MT, HT		-100	-99	dBm	[2]
4	IEEE ranging frame	CT, RT		-107	-105	dBm	[2]
		MT, HT		-105	-104	dBm	[2]

Table 20. Characteristics - Secure Ranging: First Path Sensitivity CH5

Measurement of RX sensitivity level for

- *2 Tap Channel (first path 7 ns earlier than main path)*
- *no Payload*
- *STS*
- *@ 10% first path FER*
- *Main tap power = first tap power + 15dB*
- *Security Level = 4*

Following characteristics are valid for conditions as follows (unless otherwise specified)

T_{amb} = -40 °C to 115 °C , VDD = 1.8 V to 3.6 V, f_C = 6489.6 MHz MHz, crystal = 55.2 MHz

VDD = VBAT_IO, VDD_DIG, VDD_BUF, VDD_XTAL, GPIO pins in defined, non hi-Z, state

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
1	HP ranging frame	CT, RT		-111	-109	dBm	[2]
		MT, HT		-110	-108	dBm	[2]
2	ECO Std ranging frame	CT, RT		-108	-106	dBm	[2]
		MT, HT		-107	-105	dBm	[2]
3	ECO Min ranging frame • Rx oversampling: 1x	CT, RT		-104	-101	dBm	[2]
		MT, HT		-102	-100	dBm	[2]
4	IEEE ranging frame	CT, RT		-109	-106	dBm	[2]
		MT, HT		-107	-105	dBm	[2]

10.3.2.5 Co-Channel Rejection

Table 21. Characteristics - RX - Co-Channel Rejection, NBIC disabled

Measurement of Interferer power / Wanted power for

- *AWGN*
- *@ 10% FER*

Following characteristics are valid for conditions as follows (unless otherwise specified)

T_{amb} = -40 °C to 115 °C , VDD = 1.8 V to 3.6 V, f_C = 7987.2 MHz, crystal = 55.2 MHz

VDD = VBAT_IO, VDD_DIG, VDD_BUF, VDD_XTAL, GPIO pins in defined, non hi-Z, state

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
1	HP 7.8Mbps data frame • NBIC: OFF • Wanted: -88 dBm • Interferer: J.CW @ f_C - 200 MHz		10	14		dB	[2]
2	IEEE 6.8Mbps data frame • NBIC: OFF • Wanted: -89 dBm • Interferer: J.CW @ f_C + 100 MHz		10	13		dB	[2]
3	HP 7.8Mbps data frame • NBIC: OFF • Wanted: -88 dBm • Interferer: J.CW @ f_C + 100 MHz		10	12		dB	[2]

Table 22. Characteristics - RX - Co-Channel Rejection, NBIC enabled

Measurement of Interferer power / Wanted power for

- *AWGN*
- *@ 10% FER*

Following characteristics are valid for conditions as follows (unless otherwise specified)

T_{amb} = -40 °C to 115 °C, VDD = 1.8 V to 3.6 V, f_C = 7987.2 MHz, crystal = 55.2 MHz

VDD = VBAT_IO, VDD_DIG, VDD_BUF, VDD_XTAL, GPIO pins in defined, non hi-Z, state

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
1	HP 7.8Mbps data frame • NBIC: ON, linear phase filter, 12MHz BW • Wanted: -88 dBm • Interferer: J.CW @ f_C - 200 MHz		35	42		dB	[2]
2	IEEE 6.8Mbps data frame • NBIC: ON, linear phase filter, 12MHz BW • Wanted: -89 dBm • Interferer: J.CW @ f_C + 100 MHz		40	46		dB	[2]
3	HP 7.8Mbps data frame • NBIC: ON, linear phase filter, 12MHz BW • Wanted: -88 dBm • Interferer: J.CW @ f_C + 100 MHz		40	46		dB	[2]

10.3.2.6 Out-of-Band Blocker Rejection

Table 23. Characteristics - RX - Out-of-Band Blocker Rejection, NBIC disabled, CH9

Measurement of Interferer power / Wanted power for

- *AWGN*
- *@ 10% FER*

Following characteristics are valid for conditions as follows (unless otherwise specified)

T_{amb} = -40 °C to 115 °C , VDD = 1.8 V to 3.6 V, f_C = 7987.2 MHz, crystal = 55.2 MHz

VDD = VBAT_IO, VDD_DIG, VDD_BUF, VDD_XTAL, GPIO pins in defined, non hi-Z, state

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
1	HP 7.8Mbps data frame • NBIC: OFF • Wanted: -88 dBm • Interferer: J.WIFI @ 5.865 GHz		65	68		dB	[2]
2	HP 7.8Mbps data frame • NBIC: OFF • Wanted: -88 dBm • Interferer: J.LTE @ 2.3 GHz		76	81		dB	[2]
3	IEEE 6.8Mbps data frame • NBIC: OFF • Wanted: -89 dBm • Interferer: J.LTE @ 2.6 GHz		67	70		dB	[2]
4	HP 7.8Mbps data frame • NBIC: OFF • Wanted: -88 dBm • Interferer: J.LTE @ 2.6 GHz		65	67		dB	[2]

Table 24. Characteristics - RX - Out-of-Band Blocker Rejection, NBIC disabled, CH5

Measurement of Interferer power / Wanted power for

- *AWGN*
- *@ 10% FER*

Following characteristics are valid for conditions as follows (unless otherwise specified)

T_{amb} = -40 °C to 115 °C , VDD = 1.8 V to 3.6 V, f_C = 6489.6 MHz, crystal = 55.2 MHz

VDD = VBAT_IO, VDD_DIG, VDD_BUF, VDD_XTAL, GPIO pins in defined, non hi-Z, state

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
1	HP 7.8Mbps data frame • NBIC: OFF • Wanted: -88dBm • Interferer: WIFI @ 5.865GHz		67	70		dB	[2]
2	HP 7.8Mbps data frame • NBIC: OFF • Wanted: -88dBm • Interferer: LTE @ 2.3GHz		76	81		dB	[2]
3	IEEE 6.8Mbps data frame • NBIC: OFF • Wanted: -89dBm • Interferer: LTE @ 2.6GHz		78	80		dB	[2]

Table 24. Characteristics - RX - Out-of-Band Blocker Rejection, NBIC disabled, CH5*...continued*

Measurement of Interferer power / Wanted power for

- *AWGN*
- *@ 10% FER*

Following characteristics are valid for conditions as follows (unless otherwise specified)

T_{amb} = -40 °C to 115 °C , VDD = 1.8 V to 3.6 V, f_C = 6489.6 MHz, crystal = 55.2 MHz

VDD = VBAT_IO, VDD_DIG, VDD_BUF, VDD_XTAL, GPIO pins in defined, non hi-Z, state

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
4	HP 7.8Mbps data frame • NBIC: OFF • Wanted: -89dBm • Interferer: LTE @ 2.6GHz FER: 10%		77	80		dB	[2]

Table 25. Characteristics - RX - Out-of-Band Blocker Rejection, NBIC enabled, CH9

Measurement of Interferer power / Wanted power for

- *AWGN*
- *@ 10% FER*

Following characteristics are valid for conditions as follows (unless otherwise specified)

T_{amb} = -40 °C to 115 °C, VDD = 1.8 V to 3.6 V, f_C = 7987.2 MHz, crystal = 55.2 MHz

VDD = VBAT_IO, VDD_DIG, VDD_BUF, VDD_XTAL, GPIO pins in defined, non hi-Z, state

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
1	IEEE 6.8Mbps data frame • NBIC: ON, linear phase filter, 12MHz BW • Wanted: -89dBm • Interferer: J.LTE @ 2.6GHz FER: 10%		72	76		dB	[2]
2	HP 7.8Mbps data frame • NBIC: ON, linear phase filter, 12MHz BW • Wanted: -88dBm • Interferer: J.LTE @ 2.6GHz FER: 10%		70	75		dB	[2]

Table 26. Characteristics - RX - Out-of-Band Blocker Rejection, NBIC enabled, CH5

Measurement of Interferer power / Wanted power for

- *AWGN*
- *@ 10% FER*

Following characteristics are valid for conditions as follows (unless otherwise specified)

T_{amb} = -40 °C to 115 °C, VDD = 1.8 V to 3.6 V, f_C = 6489.6 MHz, crystal = 55.2 MHz

VDD = VBAT_IO, VDD_DIG, VDD_BUF, VDD_XTAL, GPIO pins in defined, non hi-Z, state

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
1	IEEE 6.8Mbps data frame NBIC: ON, minimum phase filter, 12MHz BW Wanted: -89dBm Interferer: LTE @ 2.6GHz FER: 10%		78	80		dB	[2]
2	HP 7.8Mbps data frame NBIC: ON, minimum phase filter, 12MHz BW Wanted: -88dBm Interferer: LTE @ 2.6GHz FER: 10%		77	80		dB	[2]

10.3.2.7 Spurious emissions

Table 27. Characteristics - RX - Spurious emissions, CH9

Measurement of Spurious emissions for

- *HP ranging frame*

Following characteristics are valid for conditions as follows (unless otherwise specified)

T_{amb} = -40 °C to 115 °C , VDD = 1.8 V to 3.6 V, f_C = 7987.2 MHz, crystal = 55.2 MHz

VDD = VBAT_IO, VDD_DIG, VDD_BUF, VDD_XTAL, GPIO pins in defined, non hi-Z, state

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
1	HP ranging frame, RX in-band: 6GHz to 8.5GHz			-82	-71	dBm/1MHz	[2]
2	HP ranging frame, RX spurious: 170MHz to 222MHz			-105	-104	dBm/1MHz	[2]
3	HP ranging frame, RX spurious: 470MHz to 710MHz			-105	-97	dBm/1MHz	[2]
4	HP ranging frame, RX spurious: 710MHz to 1.6GHz			-102	-87	dBm/1MHz	[2]
5	HP ranging frame, RX spurious: 1.6GHz to 2.7GHz			-88	-80	dBm/1MHz	[2]
6	HP ranging frame, RX spurious: 2.7GHz to 6GHz			-81	-76	dBm/1MHz	[2]
7	HP ranging frame, RX spurious: 6GHz to 7.25GHz			-98	-78	dBm/1MHz	[2]
8	HP ranging frame, RX spurious: 8.5GHz to 10.25GHz			-93	-90	dBm/1MHz	[2]
9	HP ranging frame, RX spurious: 10.6GHz to 16GHz			-96	-90	dBm/1MHz	[2]

Table 28. Characteristics - RX - Spurious emissions, CH5

Measurement of Spurious emissions for

- *HP ranging frame*

Following characteristics are valid for conditions as follows (unless otherwise specified)

T_{amb} = -40 °C to 115 °C , VDD = 1.8 V to 3.6 V, f_C = 6489.6 MHz, crystal = 55.2 MHz

VDD = VBAT_IO, VDD_DIG, VDD_BUF, VDD_XTAL, GPIO pins in defined, non hi-Z, state

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
1	HP ranging frame, RX in-band: 6GHz to 8.5GHz			-87	-80	dBm/1MHz	[2]
2	HP ranging frame, RX spurious: 170MHz to 222MHz			-105	-104	dBm/1MHz	[2]
3	HP ranging frame, RX spurious: 470MHz to 710MHz			-105	-99	dBm/1MHz	[2]
4	HP ranging frame, RX spurious: 710MHz to 1.6GHz			-102	-95	dBm/1MHz	[2]
5	HP ranging frame, RX spurious: 1.6GHz to 2.7GHz			-87	-79	dBm/1MHz	[2]
6	HP ranging frame, RX spurious: 2.7GHz to 6GHz			-81	-76	dBm/1MHz	[2]
7	HP ranging frame, RX spurious: 6GHz to 7.25GHz			-84	-78	dBm/1MHz	[2]
8	HP ranging frame, RX spurious: 8.5GHz to 10.25GHz			-93	-90	dBm/1MHz	[2]
9	HP ranging frame, RX spurious: 10.6GHz to 16GHz			-96	-91	dBm/1MHz	[2]

10.3.2.8 Secure Ranging: ToA accuracy

Table 29. Characteristics - RX - Secure Ranging: ToA accuracy
Measurement of ToA accuracy for
- *AWGN*
- *95% of results within limit*

Following characteristics are valid for conditions as follows (unless otherwise specified)
T_{amb} = -40 °C to 115 °C , VDD = 1.8 V to 3.6 V, f_C = 6489.6 MHz and 7987.2 MHz, ext. clock = 55.2 MHz
VDD = VBAT_IO, VDD_DIG, VDD_BUF, VDD_XTAL, GPIO pins in defined, non hi-Z, state

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
1	HP ranging frame			0.28	0.35	ns	[5]
2	ECO Std ranging frame			0.23	0.35	ns	[5]
3	ECO Min ranging frame • Rx oversampling: 1x			0.23	0.35	ns	[5]
4	IEEE ranging frame			0.23	0.3	ns	[5]

10.3.2.9 Signal Power Measurement

Table 30. Characteristics - RX - Signal Power Measurement
Following characteristics are valid for conditions as follows (unless otherwise specified)
T_{amb} = -40 °C to 115 °C , VDD = 1.8 V to 3.6 V, f_C = 6489.6 MHz and 7987.2 MHz, crystal = 55.2 MHz
VDD = VBAT_IO, VDD_DIG, VDD_BUF, VDD_XTAL, GPIO pins in defined, non hi-Z, state

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
1	Signal Power Measurement accuracy - from -93dBm to -45dBm - HP ranging frame	CT, RT	-3		4		[2]
		MT, HT	-6		6		[2]
2	Signal Power Measurement accuracy - from -45dBm to -20dBm - HP ranging frame	CT, RT	-4		7		[2]
		MT, HT	-7		7		[2]

10.3.3 TX

10.3.3.1 10dB Bandwidth

Table 31. Characteristics - TX - 10dB Bandwidth
Following characteristics are valid for conditions as follows (unless otherwise specified)
T_{amb} = -40 °C to 115 °C , VDD = 1.8 V to 3.6 V, f_C = 6489.6 MHz or 7987.2 MHz, crystal = 55.2 MHz
VDD = VBAT_IO, VDD_DIG, VDD_BUF, VDD_XTAL, GPIO pins in defined, non hi-Z, state

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
1	HP ranging frame		580	610		MHz	[2]
2	IEEE ranging frame		580	610		MHz	[2]

10.3.3.2 Power Control

Table 32. Characteristics - TX - Power Control

Following characteristics are valid for conditions as follows (unless otherwise specified)

T_{amb} = -40 °C to 115 °C , VDD = 1.8 V to 3.6 V, f_C = 6489.6 MHz or 7987.2 MHz, crystal = 55.2 MHz

VDD = VBAT_IO, VDD_DIG, VDD_BUF, VDD_XTAL, GPIO pins in defined, non hi-Z, state

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
1	Coarse analog power step size from -12dBm to +12dBm • CW signal			1	2	dB	[2]
2	Fine digital power step size size from 0dB to 0.75dB • CW signal			0.25		dB	[6]
3	TX power variation over temperature -40°C -> 105°C • IEEE ranging frame • TX power: 12dBm			0.5	2	dB	[2]
4	TX power variation over supply Voltage 2.4V - 3.6V • IEEE ranging frame • TX power: 12dBm			0.2	2	dB	[2]
5	TX power variation over temperature -40°C -> 115°C • IEEE ranging frame • TX power: 12dBm			0.5	3	dB	[2]
6	TX power variation over temperature -40°C -> 105°C • HP ranging frame • TX power: 12dBm			0.5	2	dB	[2]
7	TX power variation over supply Voltage 2.4V - 3.6V • HP ranging frame • TX power: 12dBm			0.2	2	dB	[2]
8	TX power variation over temperature -40°C -> 115°C • HP ranging frame • TX power: 12dBm			0.5	3	dB	[2]

10.3.3.3 Average Power

Table 33. Characteristics - TX - Average Power

Conducted average power measurement. PA configured for +12dBm output power.

Following characteristics are valid for conditions as follows (unless otherwise specified)

T_{amb} = -40 °C to 115 °C , VDD = 1.8 V to 3.6 V, f_C = 6489.6 MHz or 7987.2 MHz, crystal = 55.2 MHz

VDD = VBAT_IO, VDD_DIG, VDD_BUF, VDD_XTAL, GPIO pins in defined, non hi-Z, state

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
1	IEEE ranging frame, max PSD value		-39	-36		dBm/1MHz	[2]
2	IEEE ranging frame, integrated PSD over 500 MHz BW		-14	-11		dBm	[2]
3	ECO Min ranging frame, max PSD value		-41	-38		dBm/1MHz	[2]
4	ECO Min ranging frame, integrated PSD over 500 MHz BW		-16	-13		dBm	[2]
5	IEEE 6.8Mbps data frame, max PSD value		-40	-37		dBm/1MHz	[2]
6	IEEE 6.8Mbps data frame, integrated PSD over 500 MHz BW		-15	-12		dBm	[2]

Table 33. Characteristics - TX - Average Power*...continued*

Conducted average power measurement. PA configured for +12dBm output power.

Following characteristics are valid for conditions as follows (unless otherwise specified)

T_{amb} = -40 °C to 115 °C , VDD = 1.8 V to 3.6 V, f_C = 6489.6 MHz or 7987.2 MHz, crystal = 55.2 MHz

VDD = VBAT_IO, VDD_DIG, VDD_BUF, VDD_XTAL, GPIO pins in defined, non hi-Z, state

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
7	HP ranging frame, max PSD value		-38	-34		dBm/1MHz	[2]
8	HP ranging frame, integrated PSD over 500 MHz BW		-12	-9		dBm	[2]
9	HP 7.8Mbps data frame, max PSD value		-40	-37		dBm/1MHz	[2]
10	HP 7.8Mbps data frame, integrated PSD over 500 MHz BW		-15	-12		dBm	[2]

10.3.3.4 Peak Power

Table 34. Characteristics - TX - Peak Power

Conducted peak power measurement with 50MHz RBW. PA configured for +12dBm output power.

Following characteristics are valid for conditions as follows (unless otherwise specified)

T_{amb} = -40 °C to 115 °C , VDD = 1.8 V to 3.6 V, f_C = 6489.6 MHz or 7987.2 MHz, crystal = 55.2 MHz

VDD = VBAT_IO, VDD_DIG, VDD_BUF, VDD_XTAL, GPIO pins in defined, non hi-Z, state

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
1	IEEE ranging frame		-8	-4		dBm/50MHz	[2]
2	ECO Min ranging frame		-7	-3.5		dBm/50MHz	[2]
3	IEEE 6.8Mbps data frame		2	5		dBm/50MHz	[2]
4	HP ranging frame		-7	-3		dBm/50MHz	[2]
5	HP 7.8Mbps data frame		-3	0.5		dBm/50MHz	[2]

10.3.3.5 Spurious Emissions Average Power

Table 35. Characteristics - TX - Spurious Emissions Mean Power Spectral Density CH9

Conducted Mean Power Spectral Density measurement with 1MHz RBW (i.e. without external filter).

Tx power was reduced just enough, such that the regulatory Mean Power Spectral Density limit of -41.3 dBm/1MHz, as well as the Peak Power limit of 0 dBm/50MHz were fulfilled. Note, that in practice the Tx power may need to be reduced further, to account for antenna gain. There is typically a non-linear relationship between the level of a Tx spur and the Tx power (e.g. a Tx power reduction of 2dB could result in a Tx spur level reduction of more than 2dB). An external filter can also reduce the TX spurs.

Following characteristics are valid for conditions as follows (unless otherwise specified)

T_{amb} = -40 °C to 115 °C , VDD = 3.3 V, f_C = 7987.2 MHz, crystal = 55.2 MHz

VDD = VBAT_IO, VDD_DIG, VDD_BUF, VDD_XTAL, GPIO pins in defined, non hi-Z, state

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
1	ECO Min ranging frame: 50MHz - 500MHz			-88	-85	dBm/1MHz	[4]
2	ECO Min ranging frame: 500MHz - 5640MHz			-100[1]		dBm/100kHz	[4]
3	ECO Min ranging frame: 5640MHz - 6340MHz			-82	-78	dBm/1MHz	[4]
4	ECO Min ranging frame: 6340MHz - 7100MHz			-85	-80	dBm/1MHz	[4]
5	ECO Min ranging frame: 7100MHz - 7287MHz			-84	-75	dBm/1MHz	[4]
6	ECO Min ranging frame: 8500MHz - 9000MHz			-81	-74	dBm/1MHz	[4]

Table 35. Characteristics - TX - Spurious Emissions Mean Power Spectral Density CH9*...continued*

Conducted Mean Power Spectral Density measurement with 1MHz RBW (i.e. without external filter).

Tx power was reduced just enough, such that the regulatory Mean Power Spectral Density limit of -41.3 dBm/1MHz, as well as the Peak Power limit of 0 dBm/50MHz were fulfilled. Note, that in practice the Tx power may need to be reduced further, to account for antenna gain. There is typically a non-linear relationship between the level of a Tx spur and the Tx power (e.g. a Tx power reduction of 2dB could result in a Tx spur level reduction of more than 2dB). An external filter can also reduce the TX spurs.

Following characteristics are valid for conditions as follows (unless otherwise specified)

T_{amb} = -40 °C to 115 °C , VDD = 3.3 V, f_C = 7987.2 MHz, crystal = 55.2 MHz

VDD = VBAT_IO, VDD_DIG, VDD_BUF, VDD_XTAL, GPIO pins in defined, non hi-Z, state

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
7	ECO Min ranging frame: 9000MHz - 9634MHz			-87	-81	dBm/1MHz	[4]
8	ECO Min ranging frame: 9634MHz - 10334MHz			-81	-77	dBm/1MHz	[4]
9	ECO Min ranging frame: 10334MHz - 10600MHz			-88	-86	dBm/1MHz	[4]
10	ECO Min ranging frame: 10600MHz - 15474MHz			-100[1]		dBm/100kHz	[4]
11	ECO Min ranging frame: 15474MHz - 16474MHz			-73	-67	dBm/1MHz	[4]
12	ECO Min ranging frame: 16474MHz - 26000MHz			-95[1]		dBm/100kHz	[4]
13	IEEE 6.8Mbps data frame: 50MHz - 500MHz			-89	-87	dBm/1MHz	[4]
14	IEEE 6.8Mbps data frame: 500MHz - 5640MHz			-99[1]		dBm/100kHz	[4]
15	IEEE 6.8Mbps data frame: 5640MHz - 6340MHz			-83	-79	dBm/1MHz	[4]
16	IEEE 6.8Mbps data frame: 6340MHz - 7100MHz			-85	-80	dBm/1MHz	[4]
17	IEEE 6.8Mbps data frame: 7100MHz - 7287MHz			-84	-80	dBm/1MHz	[4]
18	IEEE 6.8Mbps data frame: 8500MHz - 9000MHz			-83	-77	dBm/1MHz	[4]
19	IEEE 6.8Mbps data frame: 9000MHz - 9634MHz			-88	-84	dBm/1MHz	[4]
20	IEEE 6.8Mbps data frame: 9634MHz - 10334MHz			-82	-80	dBm/1MHz	[4]
21	IEEE 6.8Mbps data frame: 10334MHz - 10600MHz			-88	-87	dBm/1MHz	[4]
22	IEEE 6.8Mbps data frame: 10600MHz - 15474MHz			-100[1]		dBm/100kHz	[4]
23	IEEE 6.8Mbps data frame: 15474MHz - 16474MHz			-78	-73	dBm/1MHz	[4]
24	IEEE 6.8Mbps data frame: 16474MHz - 26000MHz			-95[1]		dBm/100kHz	[4]

[1] noise floor of spectrum analyzer

Table 36. Characteristics - TX - Spurious Emissions Mean Power Spectral Density CH5

Conducted Mean Power Spectral Density measurement with 1 MHz RBW (i.e. without external filter).

Tx power was reduced just enough, such that the regulatory Mean Power Spectral Density limit of -41.3 dBm/1MHz, as well as the Peak Power limit of 0 dBm/50MHz were fulfilled. Note, that in practice the Tx power may need to be reduced further, to account for antenna gain. There is typically a non-linear relationship between the level of a Tx spur and the Tx power (e.g. a Tx power reduction of 2dB could result in a Tx spur level reduction of more than 2dB). An external filter can also reduce the TX spurs.

Following characteristics are valid for conditions as follows (unless otherwise specified)

T_{amb} = -40 °C to 115 °C , VDD = 3.3 V, f_C = 6489.6 MHz, crystal = 55.2 MHz

VDD = VBAT_IO, VDD_DIG, VDD_BUF, VDD_XTAL, GPIO pins in defined, non hi-Z, state

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
1	ECO Min ranging frame: 50MHz - 500MHz			-88	-82	dBm/1MHz	[4]

Table 36. Characteristics - TX - Spurious Emissions Mean Power Spectral Density CH5*...continued*

Conducted Mean Power Spectral Density measurement with 1 MHz RBW (i.e. without external filter).

Tx power was reduced just enough, such that the regulatory Mean Power Spectral Density limit of -41.3 dBm/1MHz, as well as the Peak Power limit of 0 dBm/50MHz were fulfilled. Note, that in practice the Tx power may need to be reduced further, to account for antenna gain. There is typically a non-linear relationship between the level of a Tx spur and the Tx power (e.g. a Tx power reduction of 2dB could result in a Tx spur level reduction of more than 2dB). An external filter can also reduce the TX spurs.

Following characteristics are valid for conditions as follows (unless otherwise specified)

T_{amb} = -40 °C to 115 °C , VDD = 3.3 V, f_C = 6489.6 MHz, crystal = 55.2 MHz

VDD = VBAT_IO, VDD_DIG, VDD_BUF, VDD_XTAL, GPIO pins in defined, non hi-Z, state

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
2	ECO Min ranging frame: 500MHz - 4142MHz			-97[1]		dBm/100kHz	[4]
3	ECO Min ranging frame: 4142.80 - 4842MHz			-86	-84	dBm/1MHz	[4]
4	ECO Min ranging frame: 4842MHz - 5789MHz			-86	-79	dBm/1MHz	[4]
5	ECO Min ranging frame: 5789MHz - 6000MHz			-80	-70	dBm/1MHz	[4]
6	ECO Min ranging frame: 7189MHz - 8163MHz			-86	-75	dBm/1MHz	[4]
7	ECO Min ranging frame: 8163MHz - 8836MHz			-81	-79	dBm/1MHz	[4]
8	ECO Min ranging frame: 8836MHz - 12479MHZ			-96[1]		dBm/100kHz	[4]
9	ECO Min ranging frame: 12479MHz - 13479MHz			-69	-62	dBm/1MHz	[4]
10	ECO Min ranging frame: 13479MHz - 25000MHz			-90[1]		dBm/100kHz	[4]
11	IEEE 6.8Mbps data frame: 50MHz - 500MHz			-89	-88	dBm/1MHz	[4]
12	IEEE 6.8Mbps data frame: 500MHz - 4142MHz			-97[1]		dBm/100kHz	[4]
13	IEEE 6.8Mbps data frame: 4142.80 - 4842MHz			-87	-84	dBm/1MHz	[4]
14	IEEE 6.8Mbps data frame: 4842MHz - 5789MHz			-87	-83	dBm/1MHz	[4]
15	IEEE 6.8Mbps data frame: 5789MHz - 6000MHz			-84	-72	dBm/1MHz	[4]
16	IEEE 6.8Mbps data frame: 7189MHz - 8163MHz			-88	-76	dBm/1MHz	[4]
17	IEEE 6.8Mbps data frame: 8163MHz - 8836MHz			-84	-76	dBm/1MHz	[4]
18	IEEE 6.8Mbps data frame: 8836MHz - 12479MHZ			-97[1]		dBm/100kHz	[4]
19	IEEE 6.8Mbps data frame: 12479MHz - 13479MHz			-75	-62	dBm/1MHz	[4]
20	IEEE 6.8Mbps data frame: 13479MHz - 25000MHz			-95[1]		dBm/100kHz	[4]

[1] noise floor of spectrum analyzer

10.3.3.6 Spurious Emissions Peak Power

Table 37. Characteristics - TX - Spurious Emissions Peak Power CH9

Conducted peak power measurement with 1 MHz RBW (i.e. without external filter).

Tx power was reduced just enough, such that the regulatory Mean Power Spectral Density limit of -41.3 dBm/1MHz, as well as the Peak Power limit of 0 dBm/50MHz were fulfilled. Note, that in practice the Tx power may need to be reduced further, to account for antenna gain. There is typically a non-linear relationship between the level of a Tx spur and the Tx power (e.g. a Tx power reduction of 2dB could result in a Tx spur level reduction of more than 2dB). An external filter can also reduce the TX spurs.

Following characteristics are valid for conditions as follows (unless otherwise specified)

T_{amb} = -40 °C to 115 °C , VDD = 3.3 V, f_C = 7987.2 MHz, crystal = 55.2 MHz

VDD = VBAT_IO, VDD_DIG, VDD_BUF, VDD_XTAL, GPIO pins in defined, non hi-Z, state

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
1	ECO Min ranging frame: 50MHz - 500MHz			-75	-68	dBm/1MHz	[4]
2	ECO Min ranging frame: 500MHz - 5640MHz			-89[1]		dBm/100kHz	[4]
3	ECO Min ranging frame: 5640MHz - 6340MHz			-60	-55	dBm/1MHz	[4]
4	ECO Min ranging frame: 6340MHz - 7100MHz			-67	-58	dBm/1MHz	[4]
5	ECO Min ranging frame: 7100MHz - 7287MHz			-64	-54	dBm/1MHz	[4]
6	ECO Min ranging frame: 8500MHz - 9000MHz			-60	-52	dBm/1MHz	[4]
7	ECO Min ranging frame: 9000MHz - 9634MHz			-68	-60	dBm/100kHz	[4]
8	ECO Min ranging frame: 9634MHz - 10250MHz			-59	-55	dBm/1MHz	[4]
9	ECO Min ranging frame: 10250MHz - 10600MHz			-70	-65	dBm/1MHz	[4]
10	ECO Min ranging frame: 10600MHz - 15474MHz			-89[1]		dBm/100kHz	[4]
11	ECO Min ranging frame: 15474MHz - 16474MHz			-59	-53	dBm/1MHz	[4]
12	ECO Min ranging frame: 16474MHz - 26000MHz			-84[1]		dBm/100kHz	[4]
13	IEEE 6.8Mbps data frame: 50MHz - 500MHz			-80	-78	dBm/1MHz	[4]
14	IEEE 6.8Mbps data frame: 500MHz - 5640MHz			-89[1]		dBm/100kHz	[4]
15	IEEE 6.8Mbps data frame: 5640MHz - 6340MHz			-63	-59	dBm/1MHz	[4]
16	IEEE 6.8Mbps data frame: 6340MHz - 7100MHz			-71	-64	dBm/100kHz	[4]
17	IEEE 6.8Mbps data frame: 7100MHz - 7287MHz			-67	-62	dBm/100kHz	[4]
18	IEEE 6.8Mbps data frame: 8500MHz - 9000MHz			-66	-61	dBm/1MHz	[4]
19	IEEE 6.8Mbps data frame: 9000MHz - 9634MHz			-73	-68	dBm/100kHz	[4]
20	IEEE 6.8Mbps data frame: 9634MHz - 10250MHz			-63	-60	dBm/1MHz	[4]
21	IEEE 6.8Mbps data frame: 10250MHz - 10600MHz			-74	-70	dBm/1MHz	[4]
22	IEEE 6.8Mbps data frame: 10600MHz - 15474MHz			-89[1]		dBm/100kHz	[4]
23	IEEE 6.8Mbps data frame: 15474MHz - 16474MHz			-64	-59	dBm/1MHz	[4]
24	IEEE 6.8Mbps data frame: 16474MHz - 26000MHz			-83[1]		dBm/100kHz	[4]

[1] noise floor of spectrum analyzer

10.3.4 Current and Energy consumption

Table 38. Power State default configuration

The following power state configurations are valid for the characteristics in this section, unless otherwise specified.

	ACTIVE STATE	DPD STATE	HPD STATE
CurrLim	ON	CHARGING/CHARGED	CHARGING/CHARGED
VddCpu	ON	OFF	OFF
VddCpuRet	ON	OFF	OFF
VddBb	OFF	OFF	OFF
VddBbRet	OFF	OFF	OFF
AO Clk	1.2 MHz FRO	1.2 MHz FRO	OFF
CPU Clk	38.4 MHz FRO	OFF	OFF
BB Clk	OFF	OFF	OFF
Snapshot Clk	OFF	OFF	OFF
XTAL_OUT	OFF	OFF	OFF
WUP Timer	ON	ON	OFF
Port Logic	ON	ON	OFF

10.3.4.1 Current

Table 39. Characteristics - Current consumption - Power States

Following characteristics are valid for conditions as follows (unless otherwise specified)

T_{amb} = -40 °C to 115 °C , VDD = 1.8 V to 3.6 V, f_C = 6489.6 MHz or 7987.2 MHz, crystal = 55.2 MHz

VDD = VBAT_IO, VDD_DIG, VDD_BUF, VDD_XTAL, GPIO pins in defined, non hi-Z, state

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
1	ACTIVE STATE, CPU running • VddBbRet: ON	CT, LT, RT		5.1	5.5	mA	[3]
		KT		5.6	6.4	mA	[3]
		XT		6.3	7.6	mA	[3]
		MT, HT		8.1	11	mA	[3]
2	ACTIVE STATE, WFI instruction	CT, LT, RT		4	4.3	mA	[3]
		KT		4.2	4.6	mA	[3]
		XT		4.5	5.1	mA	[3]
		MT, HT		5.3	6.8	mA	[3]
3	ACTIVE STATE between ranging frames, SysPll disabled, WFI instruction • CPU Subsystem Sleep • UART/LIN block clock gated • CPU Clk: XO divided by 8 • VddBbRet: ON • Snapshot Clk: XO	CT, LT, RT		2.07	2.3	mA	[3]
		KT		2.62	3.3	mA	[3]
		XT		3.3	4.5	mA	[3]
		MT, HT		5.2	7.8	mA	[3]

Table 39. Characteristics - Current consumption - Power States*...continued*

Following characteristics are valid for conditions as follows (unless otherwise specified)

T_{amb} = -40 °C to 115 °C , VDD = 1.8 V to 3.6 V, f_C = 6489.6 MHz or 7987.2 MHz, crystal = 55.2 MHz

VDD = VBAT_IO, VDD_DIG, VDD_BUF, VDD_XTAL, GPIO pins in defined, non hi-Z, state

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
4	ACTIVE STATE between ranging frames, SysPll enabled • VddBbRet: ON • CPU Clk: XO • Snapshot Clk: SysPll	CT, LT, RT		22.5	23.5	mA	[3]
		KT		23.5	26	mA	[3]
		XT		25	29	mA	[3]
		MT, HT		29.8	37	mA	[3]
5	DPD STATE AO Clk: 32kHz FRO • phscaAppHal_EnterPowerMode command (see [13]) • parameter aoVoutBoostDisable = 0x1[1]	CT, LT, RT		2.2	2.7	uA	[3]
		KT		4	5.5	uA	[3]
		XT		8	11	uA	[3]
		MT, HT		24.5	33	uA	[3]
6	DPD STATE with CPU-RAM retention • VddCpuRet: ON	CT, LT, RT		556	650	uA	[3]
		KT		588	680	uA	[3]
		XT		628	740	uA	[3]
		MT, HT		760	940	uA	[3]
7	DPD STATE with CPU- and BB-RAM retention • VddCpuRet: ON • VddBbRet: ON	CT, LT, RT		650	850	uA	[3]
		KT		965	1400	uA	[3]
		XT		1350	2100	uA	[3]
		MT, HT		2500	4100	uA	[3]
8	DPD STATE between ranging frames • VddCpuRet: ON • VddBbRet: ON • Snapshot Clk: XO	CT, LT, RT		1010	1200	uA	[3]
		KT		1340	1800	uA	[3]
		XT		1750	2500	uA	[3]
		MT, HT		2900	4500	uA	[3]
9	DPD STATE, shared XO with other device • XTAL_OUT: ON	CT, LT, RT, KT		0.55	0.65	mA	[3]
		MT, HT		0.6	0.7	mA	[3]
10	DPD STATE, shared XO with other device • VddCpuRet: ON • XTAL_OUT: ON	CT, LT, RT		1.11	1.2	mA	[3]
		KT		1.15	1.25	mA	[3]
		XT		1.21	1.32	mA	[3]
		MT, HT		1.34	1.52	mA	[3]
11	HPD STATE • CurrLim: CHARGING/CHARGED	CT, LT, RT - 3.3V		485	600	nA	[3]
		KT		1950	2600	nA	[3]
		XT		4750	6200	nA	[3]
		MT, HT		19800	25000	nA	[3]

[1] When parameter aoVoutBoostDisable = 0x0 is used, the current consumption is ~40uA higher. This is a legacy mode, which has no advantage for the application.

Table 40. Characteristics - Current consumption - RX operation

Measurement of current, when RX enabled and no frame provided

Following characteristics are valid for conditions as follows (unless otherwise specified)

T_{amb} = -40 °C to 115 °C , VDD = 1.8 V to 3.6 V, f_C = 6489.6 MHz or 7987.2 MHz, crystal = 55.2 MHz

VDD = VBAT_IO, VDD_DIG, VDD_BUF, VDD_XTAL, GPIO pins in defined, non hi-Z, state

ACTIVE STATE: VddBb: ON; VddBbRet: ON; CPU Clk: XO; BB Clk: SysPll; Snapshot Clk: SysPll; NBIC: OFF

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
1	HP ranging frame • NBIC: ON, linear phase filter • Interferer: CW	CT, LT, RT		163	172	mA	[3]
		KT		168	176	mA	[3]
		XT		171	180	mA	[3]
		MT, HT		179	190	mA	[3]
2	HP ranging frame • NBIC: ON, minimum phase filter • Interferer: CW	CT, LT, RT		152	160	mA	[3]
		KT		157	166	mA	[3]
		XT		160	172	mA	[3]
		MT, HT		168	185	mA	[3]
3	HP ranging frame	CT, LT, RT		131	136	mA	[3]
		KT		135	142	mA	[3]
		XT		139	148	mA	[3]
		MT, HT		145	156	mA	[3]
4	ECO Std ranging frame	CT, LT, RT		130	136	mA	[3]
		KT		134	142	mA	[3]
		XT		138	148	mA	[3]
		MT, HT		145	156	mA	[3]
5	ECO Min ranging frame • ADC: 500MHz	CT, LT, RT		114	120	mA	[3]
		KT		119	126	mA	[3]
		XT		122	132	mA	[3]
		MT, HT		129	140	mA	[3]
6	IEEE ranging frame • NBIC: ON, linear phase filter • Interferer: CW	CT, LT, RT		165	172	mA	[3]
		KT		170	180	mA	[3]
		XT		173	184	mA	[3]
		MT, HT		180	192	mA	[3]
7	IEEE ranging frame • NBIC: ON, minimum phase filter • Interferer: CW	CT, LT, RT		154	162	mA	[3]
		KT		159	166	mA	[3]
		XT		162	172	mA	[3]
		MT, HT		170	184	mA	[3]
8	IEEE ranging frame	CT, LT, RT		132	138	mA	[3]
		KT		137	144	mA	[3]
		XT		141	148	mA	[3]
		MT, HT		147	158	mA	[3]

Table 41. Characteristics - Current consumption - TX operation
Measurement of average current during transmission of a frame
Following characteristics are valid for conditions as follows (unless otherwise specified)
T_{amb} = -40 °C to 115 °C , VDD = 1.8 V to 3.6 V, f_C = 6489.6 MHz or 7987.2 MHz, crystal = 55.2 MHz
VDD = VBAT_IO, VDD_DIG, VDD_BUF, VDD_XTAL, GPIO pins in defined, non hi-Z, state
ACTIVE STATE: VddBb: ON; VddBbRet: ON; CPU Clk: XO; BB Clk: SysPll; Snapshot Clk: SysPll;

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
1	HP ranging frame	CT, LT, RT		115	120	mA	[3]
		KT		119	126	mA	[3]
		XT		122	130	mA	[3]
		MT, HT		129	138	mA	[3]
2	ECO Std ranging frame	CT, LT, RT		115	120	mA	[3]
		KT		119	126	mA	[3]
		XT		122	130	mA	[3]
		MT, HT		126	138	mA	[3]
3	ECO Min ranging frame	CT, LT, RT		114	120	mA	[3]
		KT		119	126	mA	[3]
		XT		122	130	mA	[3]
		MT, HT		126	138	mA	[3]
4	IEEE ranging frame	CT, LT, RT		110	115	mA	[3]
		KT		115	121	mA	[3]
		XT		118	125	mA	[3]
		MT, HT		124	133	mA	[3]

10.3.4.2 Energy

Table 42. Characteristics - Energy consumption - RX operation
Measurement of electric charge consumed, during the reception of a valid ranging frame, from the beginning of the frame until the end of the frame (i.e. excluding start-up, RX ToA post-processing and shut-down). The charge is multiplied by 2V, to give an energy value.
Following characteristics are valid for conditions as follows (unless otherwise specified)
T_{amb} = -40 °C to 115 °C , VDD = 1.8 V to 3.6 V, f_C = 6489.6 MHz or 7987.2 MHz, crystal = 55.2 MHz
VDD = VBAT_IO, VDD_DIG, VDD_BUF, VDD_XTAL, GPIO pins in defined, non hi-Z, state
ACTIVE STATE: VddBb: ON; VddBbRet: ON; CPU Clk: XO; BB Clk: SysPll; Snapshot Clk: SysPll; NBIC: OFF

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
1	HP ranging frame • NBIC: ON, linear phase filter • Interferer: CW	CT, LT, RT		38	45	uJ	[3]
		KT		39	44	uJ	[3]
		XT		40	47	uJ	[3]
		MT, HT		41	48	uJ	[3]
2	HP ranging frame • NBIC: ON, minimum phase filter • Interferer: CW	CT, LT, RT		36	39	uJ	[3]
		KT		37	39	uJ	[3]
		XT		38	40	uJ	[3]

Table 42. Characteristics - Energy consumption - RX operation*...continued*

Measurement of electric charge consumed, during the reception of a valid ranging frame, from the beginning of the frame until the end of the frame (i.e. excluding start-up, RX ToA post-processing and shut-down). The charge is multiplied by 2V, to give an energy value.

Following characteristics are valid for conditions as follows (unless otherwise specified)

T_{amb} = -40 °C to 115 °C , VDD = 1.8 V to 3.6 V, f_C = 6489.6 MHz or 7987.2 MHz, crystal = 55.2 MHz

VDD = VBAT_IO, VDD_DIG, VDD_BUF, VDD_XTAL, GPIO pins in defined, non hi-Z, state

ACTIVE STATE: VddBb: ON; VddBbRet: ON; CPU Clk: XO; BB Clk: SysPll; Snapshot Clk: SysPll; NBIC: OFF

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
		MT, HT		39	43	uJ	[3]
3	HP ranging frame	CT, LT, RT		31	33	uJ	[3]
		KT		32	34	uJ	[3]
		XT		33	35	uJ	[3]
		MT, HT		34	38	uJ	[3]
4	ECO Std ranging frame	CT, LT, RT		15	17	uJ	[3]
		KT		16	18	uJ	[3]
		XT		17	18	uJ	[3]
		MT, HT		17	19	uJ	[3]
5	ECO Min ranging frame • ADC: 500MHz	CT, LT, RT		10	11	uJ	[3]
		KT		10	11	uJ	[3]
		XT		10	11	uJ	[3]
		MT, HT		11	12	uJ	[3]
6	IEEE ranging frame • NBIC: ON, linear phase filter • Interferer: CW	CT, LT, RT		44	53	uJ	[3]
		KT		45	55	uJ	[3]
		XT		47	54	uJ	[3]
		MT, HT		49	57	uJ	[3]
7	IEEE ranging frame • NBIC: ON, minimum phase filter • Interferer: CW	CT, LT, RT		41	44	uJ	[3]
		KT		43	45	uJ	[3]
		XT		43	46	uJ	[3]
		MT, HT		45	48	uJ	[3]
8	IEEE ranging frame	CT, LT, RT		36	38	uJ	[3]
		KT		37	40	uJ	[3]
		XT		38	41	uJ	[3]
		MT, HT		40	43	uJ	[3]

Table 43. Characteristics - Energy consumption - TX operation

Measurement of electric charge consumed, during the reception of a valid ranging frame, from the beginning of the frame until the end of the frame (i.e. excluding start-up, TX pre-processing and shut-down). The charge is multiplied by 2V, to give an energy value.

Following characteristics are valid for conditions as follows (unless otherwise specified)

T_{amb} = -40 °C to 115 °C , VDD = 1.8 V to 3.6 V, f_C = 6489.6 MHz or 7987.2 MHz, crystal = 55.2 MHz

VDD = VBAT_IO, VDD_DIG, VDD_BUF, VDD_XTAL, GPIO pins in defined, non hi-Z, state

ACTIVE STATE: VddBb: ON; VddBbRet: ON; CPU Clk: XO; BB Clk: SysPll; Snapshot Clk: SysPll;

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
1	HP ranging frame	CT, LT, RT		27	29	uJ	[3]
		KT		29	32	uJ	[3]
		XT		30	31	uJ	[3]
		MT, HT		31	33	uJ	[3]
2	ECO Std ranging frame	CT, LT, RT		14	15	uJ	[3]
		KT		14.5	16	uJ	[3]
		XT		15	17	uJ	[3]
		MT, HT		16	17	uJ	[3]
3	ECO Min ranging frame	CT, LT, RT		10	11	uJ	[3]
		KT		10.5	12	uJ	[3]
		XT		11	13	uJ	[3]
		MT, HT		11.5	13	uJ	[3]
4	IEEE ranging frame	CT, LT, RT		30	34	uJ	[3]
		KT		32	36	uJ	[3]
		XT		33	36	uJ	[3]
		MT, HT		35	38	uJ	[3]

10.3.5 Timings

Table 44. Characteristics - Timings - Analog Startup

Following characteristics are valid for conditions as follows (unless otherwise specified)

T_{amb} = -40 °C to 115 °C , VDD = 1.8 V to 3.6 V, f_C = 6489.6 MHz or 7987.2 MHz, crystal = 55.2 MHz

VDD = VBAT_IO, VDD_DIG, VDD_BUF, VDD_XTAL, GPIO pins in defined, non hi-Z, state

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
1	Analog calibration time: time duration to calibrate SysPll, RfPll and ADC (XO is already running)			255	300	us	[2]
2	Analog SysPll startup time: time duration to startup SysPll, such that TX or RX can be started (XO is already running)			112	155	us	[2]
3	Analog TX startup time: time duration to startup RfPll, LO, DAC and PA, such that TX can start (SysPll is already running).			45	50	us	[2]
4	Analog RX startup time: time duration to startup RfPll, LO and ADC, such that RX can start (SysPll is already running).			67	74	us	[2]

Table 45. Characteristics - Timings - Transition Times

Following characteristics are valid for conditions as follows (unless otherwise specified)

T_{amb} = -40 °C to 115 °C , VDD = 1.8 V to 3.6 V, f_C = 6489.6 MHz or 7987.2 MHz, crystal = 55.2 MHz

VDD = VBAT_IO, VDD_DIG, VDD_BUF, VDD_XTAL, GPIO pins in defined, non hi-Z, state

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
1	Cold Boot Time: Supply Voltage stable to ACTIVE STATE			2.2	2.55	ms	[2]
2	Boot Time: RST_N de-asserted to ACTIVE STATE			1.7	1.85	ms	[2]
3	DPD Boot Time (w/o fast-boot): Wake-up event to ACTIVE STATE			1.39	1.47	ms	[2]
4	HPD Boot Time: Wake-up event to ACTIVE STATE			1.7	1.85	ms	[2]
5	RX to TX turnaround time			105	110	us	[2]
6	TX to RX turnaround time			134	140	us	[2]

Table 46. Characteristics - Timings - XO Startup

Following characteristics are valid for conditions as follows (unless otherwise specified)

T_{amb} = -40 °C to 115 °C , VDD = 1.8 V to 3.6 V, f crystal = 55.2 MHz

VDD = VBAT_IO, VDD_DIG, VDD_BUF, VDD_XTAL, GPIO pins in defined, non hi-Z, state

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
2	LDO_XO_ENBL to XO_OK and stable within +/-10ppm			277	340	us	[2]

Table 47. Characteristics - Timings - SPI

Following characteristics are valid for conditions as follows (unless otherwise specified)

T_{amb} = -40 °C to 115 °C , VDD = 1.8 V to 3.6 V

VDD = VBAT_IO, VDD_DIG, VDD_BUF, VDD_XTAL, GPIO pins in defined, non hi-Z, state

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
1	SPI data rate				10	MHz	[6]
2	Master Mode, propagation time (t1) of data output (SDIO) with respect to SCLK edge				20	ns	[6]
3	Master Mode, setup time (t2) for data input (SDI) with respect to SCLK edge				28	ns	[6]
4	Slave Mode, propagation time (t3) of data output (SDIO) with respect to CS_N edge				31	ns	[6]
5	Slave Mode, propagation time (t4) of data output (SDIO) with respect to SCLK edge				31	ns	[6]
6	Slave Mode, setup time (t5) for data input (SDI) with respect to SCLK edge				16	ns	[6]

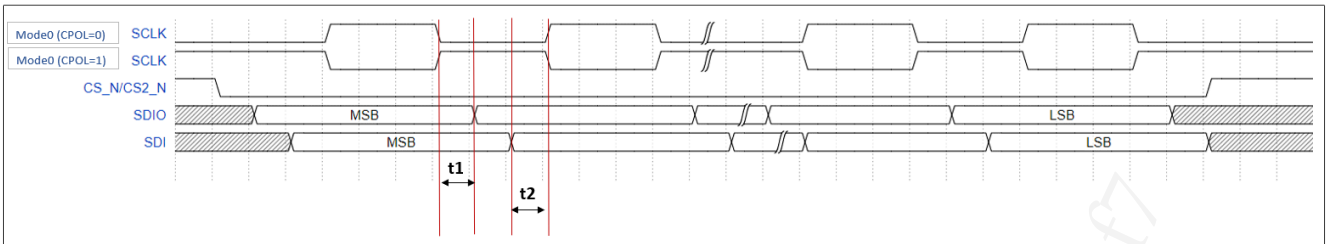


Figure 11. SPI Timing Master Mode

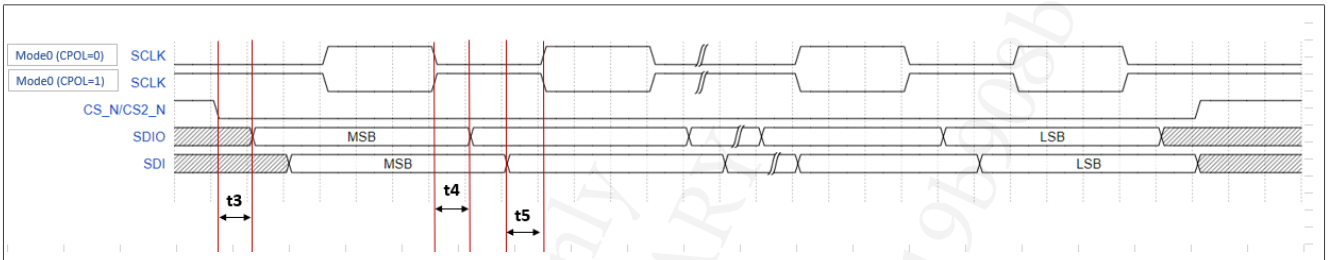


Figure 12. SPI Timing Slave Mode

10.3.6 Auxiliary functions

Table 48. Characteristics - Auxiliary functions - Internal temperature sensor

Following characteristics are valid for conditions as follows (unless otherwise specified)
T_{amb} = -40 °C to 115 °C , VDD = 1.8 V to 3.6 V, f_C = 6489.6 MHz or 7987.2 MHz, crystal = 55.2 MHz
VDD = VBAT_IO, VDD_DIG, VDD_BUF, VDD_XTAL, GPIO pins in defined, non hi-Z, state

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
1	Internal temperature sensor accuracy	CT, RT	-5		4	°C	[2]
		MT, HT	-7		1	°C	[2]

Table 49. Characteristics - Auxiliary functions - Current Limiter

Following characteristics are valid for conditions as follows (unless otherwise specified)
T_{amb} = -40 °C to 115 °C , VDD = 1.8 V to 3.6 V, f_C = 6489.6 MHz or 7987.2 MHz, crystal = 55.2 MHz
VDD = VBAT_IO, VDD_DIG, VDD_BUF, VDD_XTAL, GPIO pins in defined, non hi-Z, state

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
1	Current Limiter range: difference between highest (20mA) and lowest (5mA) setting[1]		13	15		mA	[2]
2	Current Limiter accuracy			1	1.3	mA	[2]

[1] Note that the current limiter should not be set below 8mA in the application, to ensure that the average current required for SW execution can be delivered.

Table 50. Characteristics - Auxiliary functions - Voltage Measurement

Following characteristics are valid for conditions as follows (unless otherwise specified)

T_{amb} = -40 °C to 115 °C , VDD = 1.8 V to 3.6 V, f_C = 6489.6 MHz or 7987.2 MHz, crystal = 55.2 MHz

VDD = VBAT_IO, VDD_DIG, VDD_BUF, VDD_XTAL, GPIO pins in defined, non hi-Z, state

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
1	VBAT_IO Voltage measurement error • VBAT_IO set to 1.8V, 2.4V, 3.3V, 3.6V • VBAT_IO measured on chip via API function			30	120	mV	[2]
2	VDD_BUF Voltage measurement error • VDD_BUF set to 1.8V, 2.4V, 3.3V, 3.6V • VDD_BUF measured on chip via API function			30	120	mV	[2]
3	VDD_GLOB Voltage measurement error • VDD_GLOB set to 1.8V, 2.1V • VDD_GLOB measured on chip via API function			30	120	mV	[2]
4	VDD_DIG Voltage measurement error • VDD_DIG set to 1.8V, 2.4V, 3.3V, 3.6V • VDD_DIG measured on chip via API function			30	120	mV	[2]

10.3.7 Pins

Table 51. Characteristics for ESD

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
1	ESD HBM Electrostatic Discharge (Human Body Model)[1]	1500 Ω, 100 pF, All pins	2			kV	[6]
2	ESD CDM Electrostatic Discharge (Charged Device Model)[2]	All pins	500			V	[6]

[1] JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
[2] JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Table 52. Static Characteristics I/O Ports

Following characteristics are valid for conditions as follows (unless otherwise specified)

T_{amb} = -40 °C to 115 °C , VBAT_IO = 1.8 V to 3.6 V

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
1	High level input voltage		0.7 × VBAT_IO		VBAT_IO	V	[1]
2	Low level input voltage		0		0.3 × VBAT_IO	V	[1]
3	Input hysteresis voltage		0.1 × VBAT_IO			V	[6]
4	Output high current	At VOH =VDDE - 0.4V	2			mA	[1]
5	Output low current	At VOL =0.4V	2			mA	[1]
6	Pull-up resistor	VI = 0	40	50	62	kΩ	[1]
7	Pull-down resistor	VI = VDDE	40	50	62	kΩ	[1]

Table 53. Dynamic Characteristics I/O Ports

Following characteristics are valid for conditions as follows (unless otherwise specified)

T_{amb} = -40 °C to 115 °C , VBAT_IO = 1.8 V to 3.6 V

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
1	Output rise time	10 pF load	1.2		4.6	ns	[6]
2	Output fall time	10 pF load	1.2		4.6	ns	[6]

11 Typical Performance

11.1 RX Frame Error Rate (FER) vs Input Level

Measurement setup:

- conducted
- Signal Generator to device

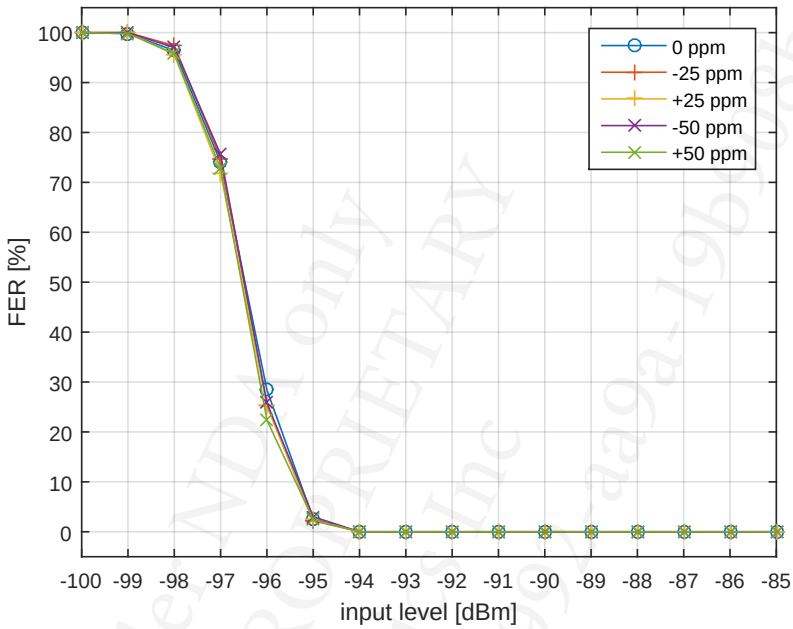


Figure 13. IEEE 6.8 Mbps data frame: RX FER vs Input Level in CH9 for different carrier frequency offsets

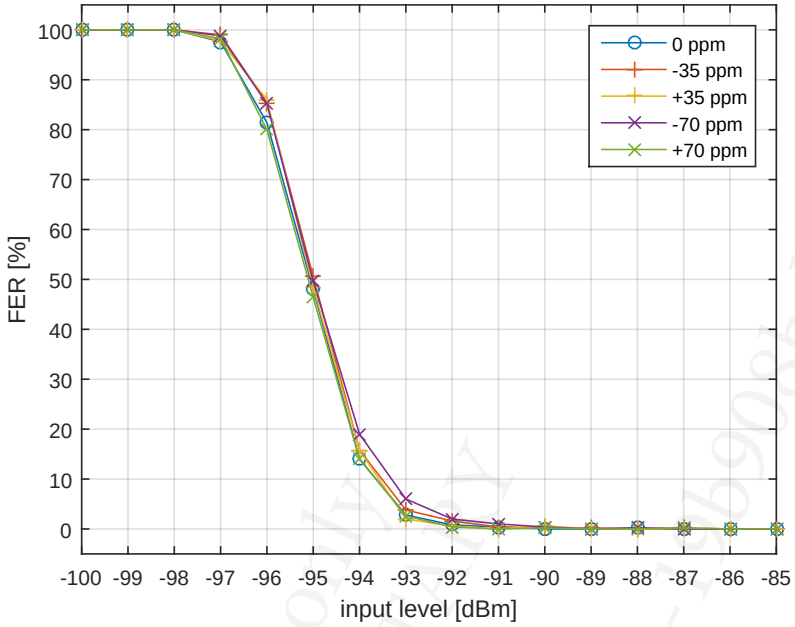


Figure 14. ECO Min 7.8 Mbps data frame: RX FER vs Input Level in CH9 for different carrier frequency offsets

11.2 RX Co-Channel Rejection

Measurement setup:

- conducted
- Signal Generator + CW to device

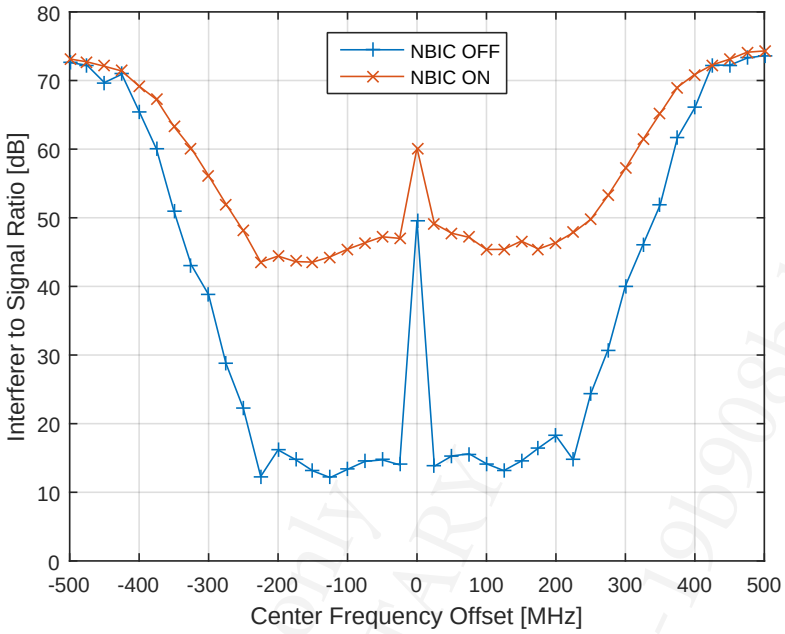


Figure 15. IEEE 6.8 Mbps data frame: RX Co-Channel Rejection Interferer/Signal-Ratio vs CW Interferer Sweep CH9

11.3 TX Mean Power Spectral Density

Measurement setup:

- conducted
- device to Spectrum Analyzer
- Tx PA power setting: 12dBm (Note that the power level can be decreased in 0.25dB steps to meet the -41.3 dBm/MHz regulation limit.)

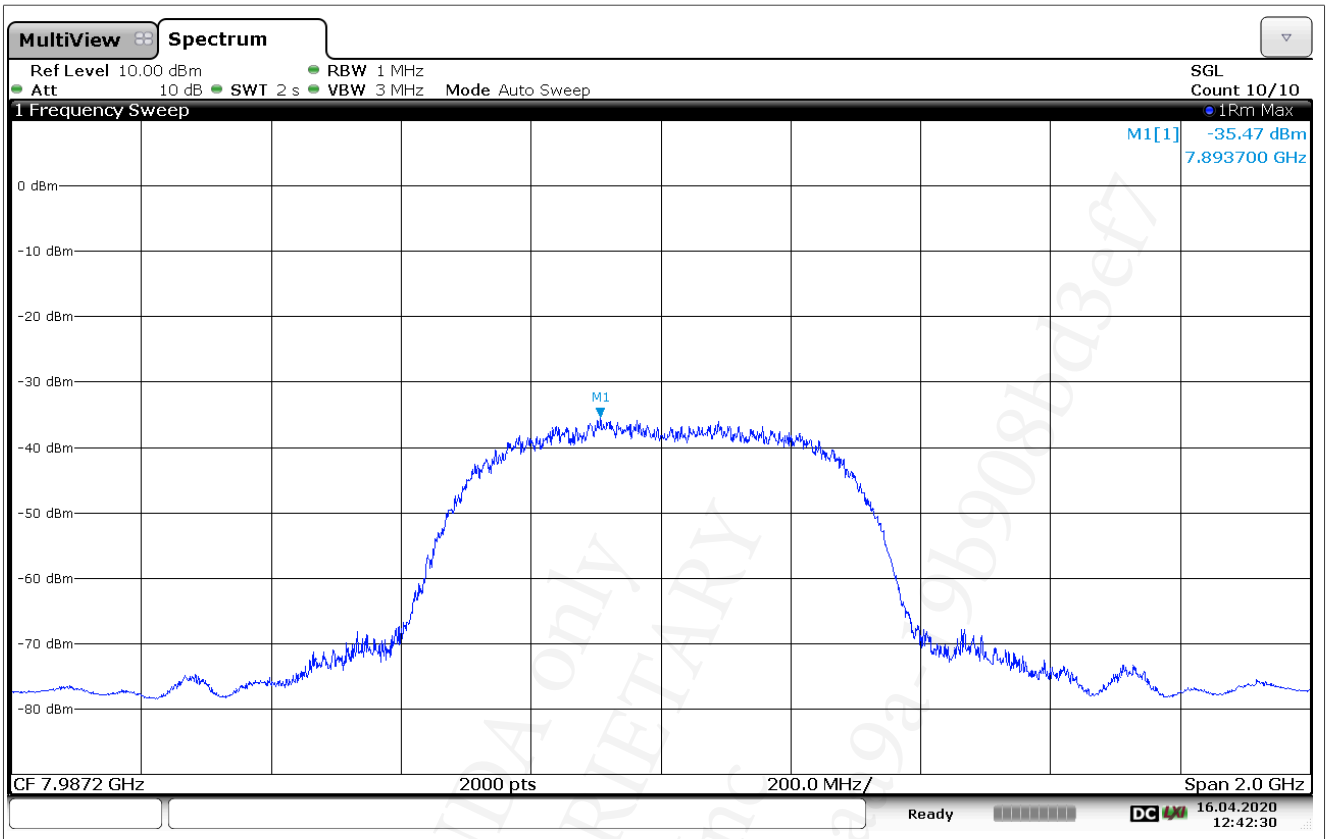


Figure 16. IEEE 6.8 Mbps ranging frame, 12 dBm PA power: TX Mean Power Spectral Density

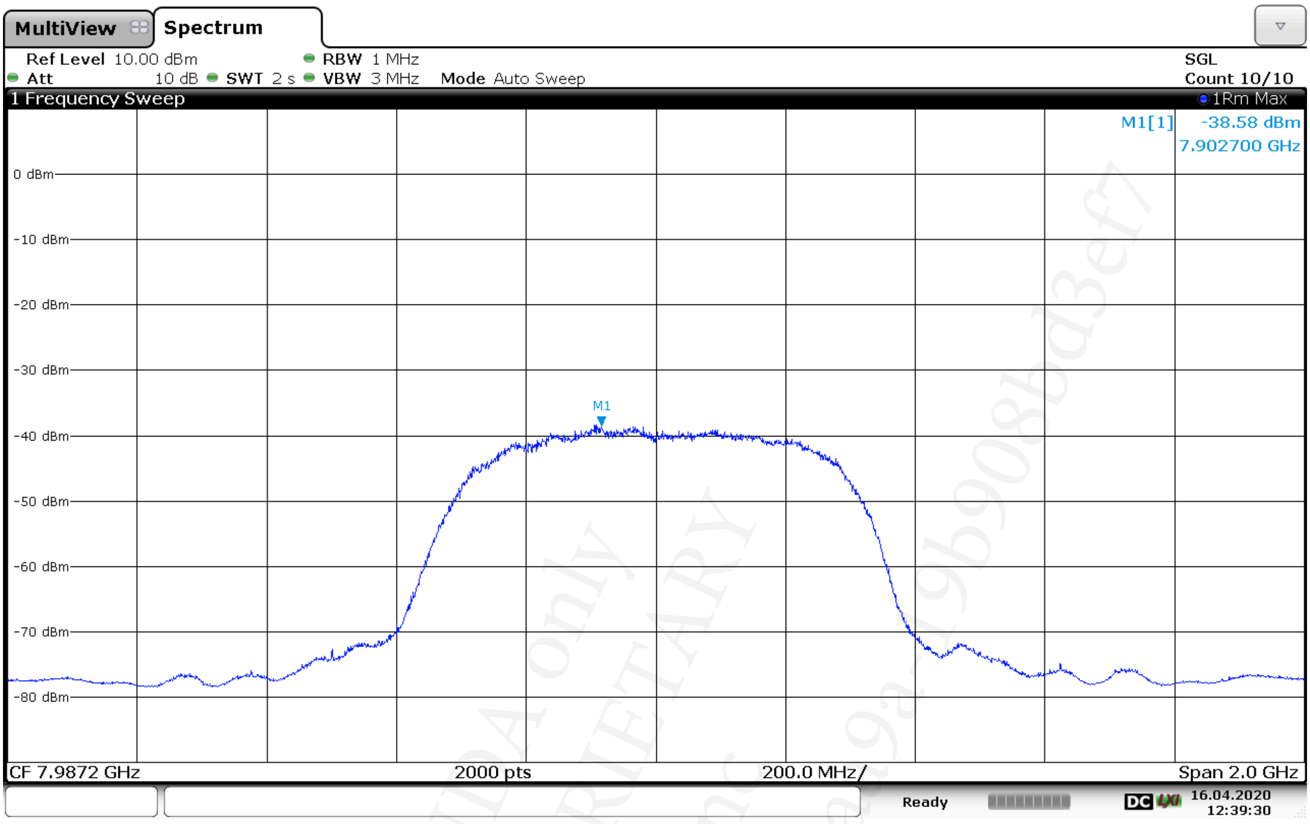


Figure 17. ECO Min 7.8 Mbps ranging frame, 12 dBm PA power: TX Mean Power Spectral Density

11.4 Histogram Double-Sided Two-Way Ranging

Measurement setup:

- conducted
- device to device
- Rx power level: -60 dBm

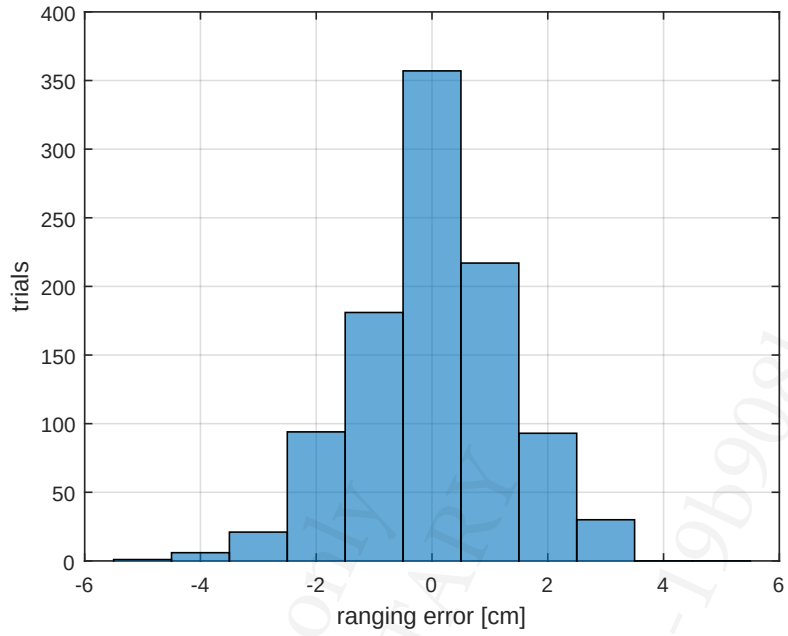


Figure 18. IEEE 6.8 Mbps ranging frame: Histogram Double-Sided Two-Way Ranging (1000 trials)

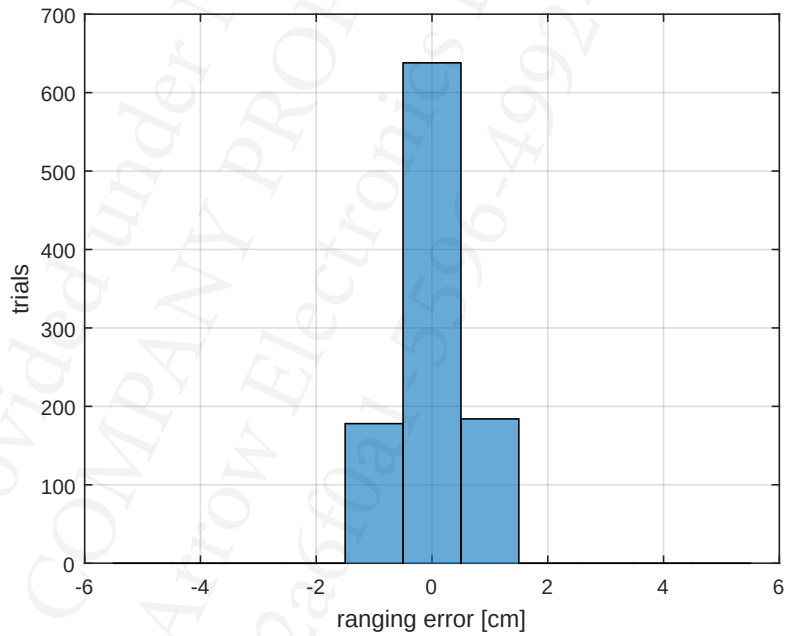


Figure 19. ECO Std 7.8 Mbps ranging frame: Histogram Double-Sided Two-Way Ranging (1000 trials)

11.5 Current Profile Double-Sided Two-Way Ranging

Figure 20 shows the current and voltage trace of a ranging exchange in a RSD application, for the initiator side (i.e. key-fob). ECO Min 7.8Mbps ranging frames are

used. The current limiter is set to 10mA. The supply Voltage is 2.05V (i.e. modeling a CR2032 battery at the end of life). The inter frame timing is adjusted such that the average current is 10mA. It can be seen that the current drawn from the battery is almost constant at ~10mA. The peak current required for frame reception and frame transmission is delivered by an energy storage capacitor (2x47uF Ceramic Capacitors were used). The Voltage on the energy storage capacitor rises between the frames when it is charged and drops during the frame when it is discharged. Between the frames the device stays in ACTIVE STATE executing the WFI instruction, with the Snapshot Unit running on the XO (i.e. SysPll disabled).

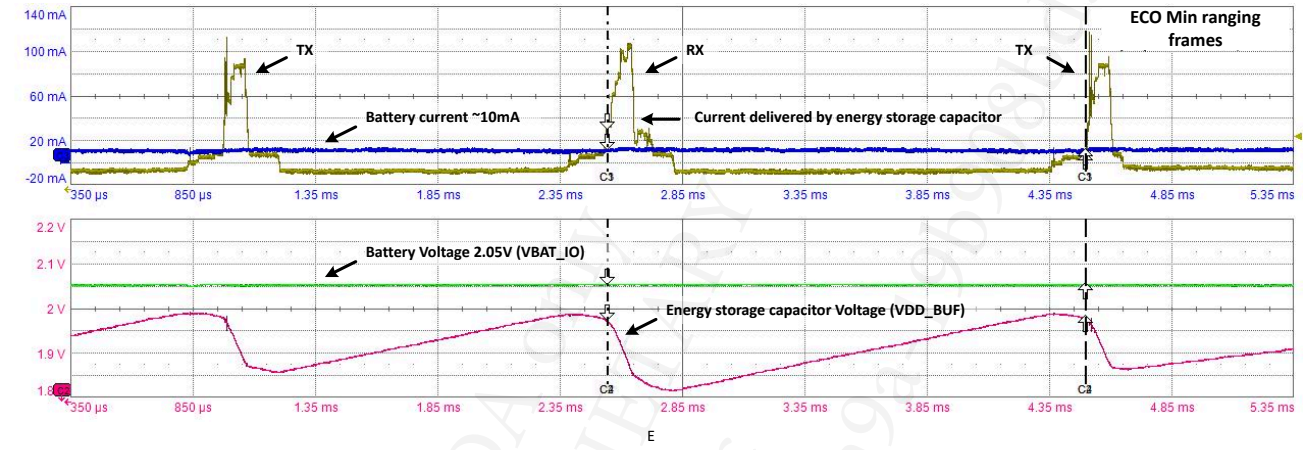
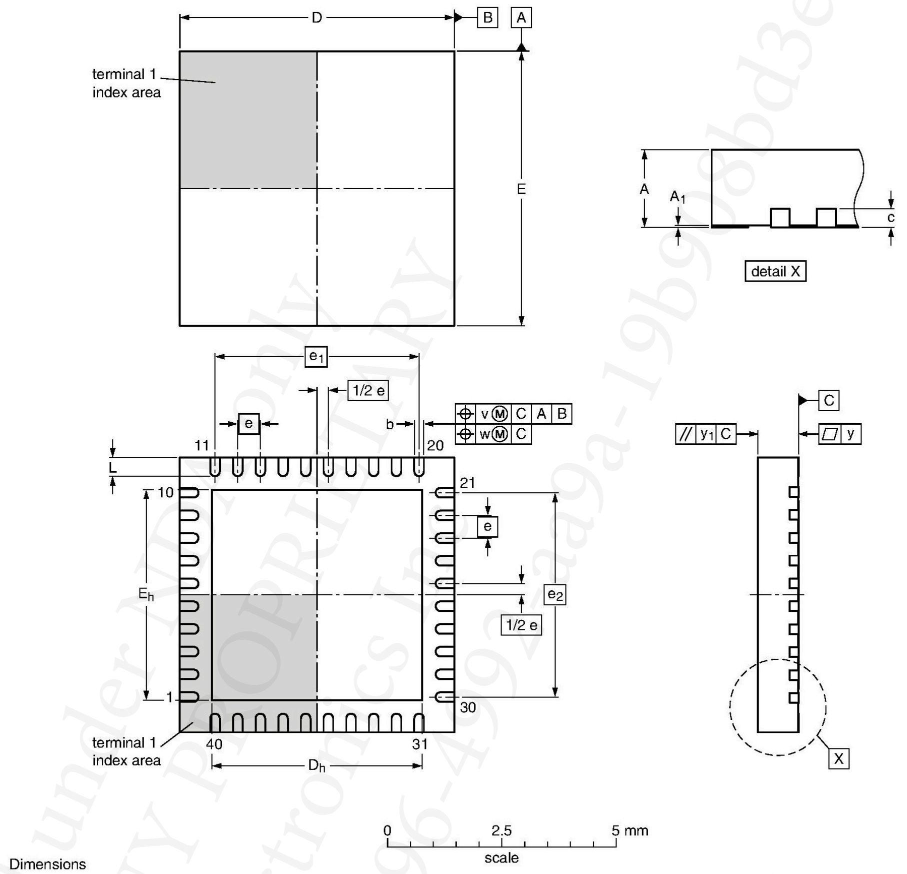


Figure 20. ECO Min 7.8 Mbps ranging frame: Current Profile Double-Sided Two-Way Ranging Tx → Rx → TX

12 Mechanical information

12.1 Package outline

HVQFN40: plastic thermal enhanced very thin quad flat package; no leads; 40 terminals; body 6 x 6 x 0.85 mm **SOT618-7**



Dimensions

Unit		A(1)	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	max	1.00	0.05	0.30		6.1	4.75	6.1	4.75				0.5				
	nom	0.85	0.02	0.21	0.2	6.0	4.60	6.0	4.60	0.5	4.5	4.5	0.4	0.1	0.05	0.05	0.1
	min	0.80	0.00	0.18		5.9	4.45	5.9	4.45				0.3				

Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot618-7_po

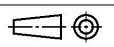
Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT618-7		MO-220	- - -			~~10-11-01~~ 10-11-05

Figure 21. Package outline HVQFN40

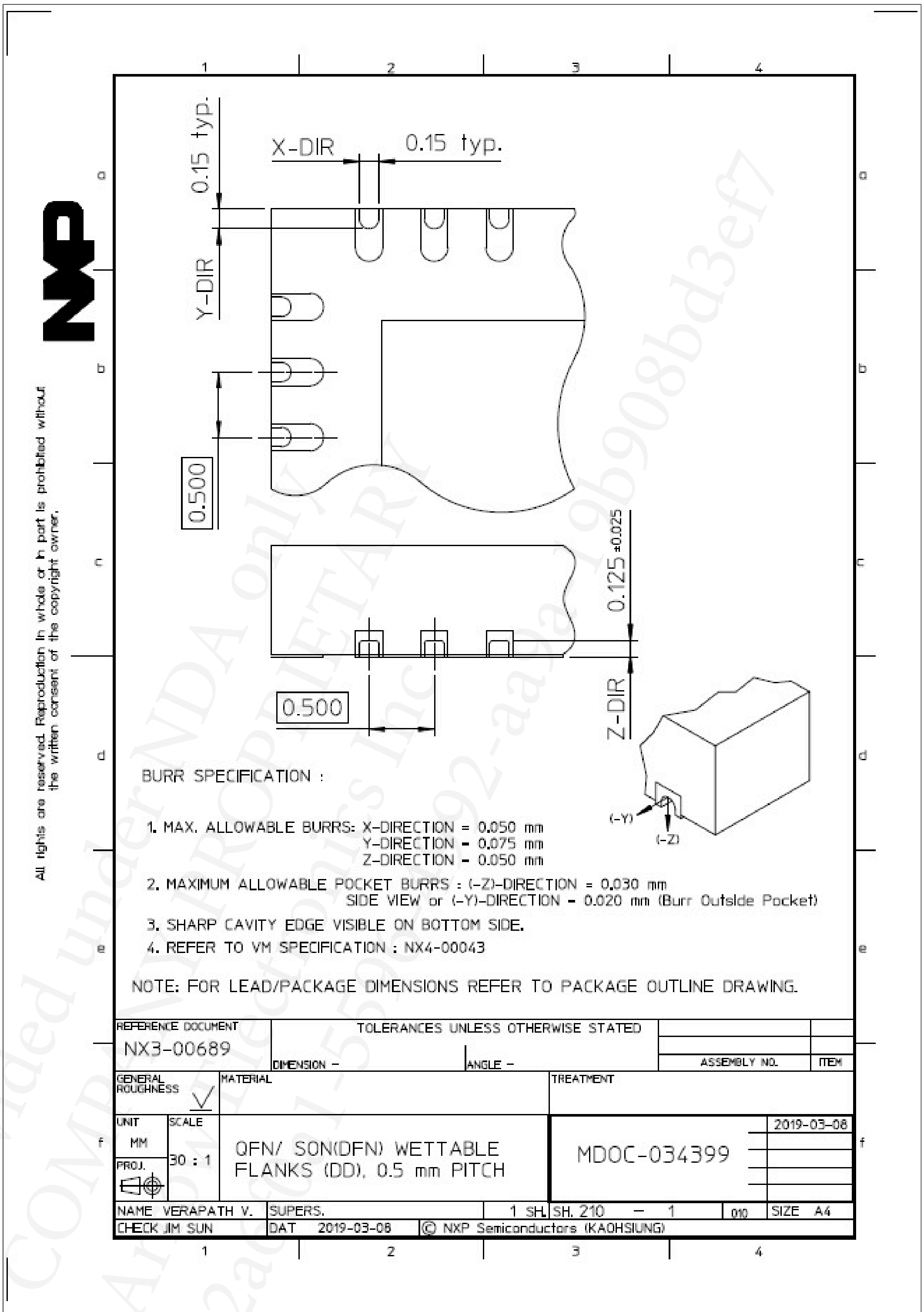


Figure 22. Package detail wettable flanks

13 Glossary

AC	Alternating Current
ADC	Analog to Digital Converter
AES	Advanced Encryption Standard
AFC	Automatic Frequency Calibration
AGC	Automatic Gain Control
API	Application Programming Interface
Balun	Balanced to Unbalanced
BIST	Built-in Self Test
BF	Bit Field
BW	BandWidth
CP	Charge Pump
CPU	Central Processing Unit
CRC	Cyclic Redundancy Check
CW	Continuous Wave
DAC	Digital to Analog Converter
DC	Direct Current
DMA	Direct Memory Access
DPD	Deep Power Down
DRBG	Deterministic Random Bit Generator
ECC	Elliptic Curve Cryptography
ESD	ElectroStatic Discharge
EDLC	Early Detect Late Commit
FAR	False Alarm Rate
FER	Frame Error Rate
FRO	Free-Running Oscillator
FSM	Finite State Machine
HBM	Human Body Model
HPD	Hard Power Down
ISR	Interrupt Service Routine
ISM	Industrial, Scientific and Medical
IR-UWB	Impulse Radio Ultra Wideband
LIN	Local Interconnect Network
LNA	Low Noise Amplifier
LO	Local Oscillator
LOS	Line-Of-Sight
LPF	Low-Pass Filter
MUX	Multiplexer
NBIC	Narrow Band Interference Cancellation
NC	Not Connected
NLOS	Non-Line-Of-Sight
NV	Non Volatile Memory
NS-DMA	Non Secure DMA
PLL	Phase Locked Loop

POR	Power-On-Reset
POK	Power OK
PKE	Passive Keyless Entry
PRN	Pseudo-Random Number
PRNG	Pseudo-Random Number Generator
PVT	Process, Voltage and Temperature
RF	Radio Frequency
RFU	Reserved for Future Use
RS	Reed Solomon
RSSI	Received Signal Strength Indicator
RX	Receiver
S-DMA	Secure DMA
SFD	Start of Frame Delimiter
SECDED	Single Error Correction, Double Error Detection
SHA	Secure Hash Algorithm
SHF	Super High Frequency
SPI	Serial Peripheral Interface
STS	Scrambled Timestamp Sequence
SWD	Serial Wire Debug
TDOA	Time Difference Of Arrival
TIA	Trans-Impedance Amplifier
TX	Transmitter
TRX	Transmitter Receiver
UART	Universal Asynchronous Receiver and Transmitter
UHF	Ultra High Frequency
UWB	Ultra Wideband
VCO	Voltage Controlled Oscillator
WUP	Wake-UP
XTAL	Crystal
XO	Crystal Oscillator

14 References

[1] **NCJ29D5 User Manual**

[2] **NCJ29D5 SWUP User Manual** — NCJ29D5 Software Update Program User Manual, UM11383

[3] **NCJ29D5 Programmer's Manual** — NCJ29D5 Software, UM11218

[4] **IEEE Std 802.15.4™-2015** (Revision of IEEE Std 802.15.4-2011) IEEE Standard for Local and metropolitan area networks – Part 15.4: Low-Rate Wireless Personal Area Networks (LR-WPANs). IEEE Computer Society Sponsored by the LAN/MAN Standards Committee.
http://standards.ieee.org

[5] **IEEE Std 802.15.4z™-D08** (Draft Revision of IEEE Std 802.15.4-2015) Amendment: Enhanced Ultra Wide-4 Band (UWB) Physical Layers (PHYs) and Associated Ranging Techniques
https://www.techstreet.com/ieee/standards/ieee-p802-15-4z?gateway_code=ieee&vendor_id=7291&product_id=2087572

[6] ARM® Cortex®-M33 Processor - Technical Reference Manual
Rev. r0p2

[7] ARM® TrustZone

[8] ARM®v8-M Architecture Reference Manual

[9] ARM® Serial Wire Debug (SWD)

[10] NIST Special Publication 800-90A Revision 1 2015. Recommendation for Random Number Generation Using Deterministic Random Bit Generators

[11] GlobalPlatform® https://www.globalplatform.org/

[12] **ETSI EN 302 065-3 V2.1.1 (2016-11)** Short Range Devices (SRD) using Ultra Wide Band technology (UWB);Harmonised Standard covering the essential requirements of article 3.2 of the Directive 2014/53/EU; Part 3: Requirements for UWB devices for ground based vehicular applications http://www.etsi.org/standards-search

[13] **APP HAL API** NCJ29D5_AppHAL.chm

15 Revision history

Table 54. Revision history

Document Version	Release date	Modifications
Rev. 1.2	2023-02-03	MAC related information has been moved, to another document. Updated pin description. Replaced device nickname by NCJ29D5.
Rev. 1.1	2022-01-31	Updated pin description
Rev. 1.0	2020-11-27	Initial version

16 Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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