

## 4-BIT SINGLE-CHIP MICROCOMPUTER

### DESCRIPTION

The μPD75P316A is a product of the μPD75316 with on-chip ROM having been replaced with the one-time PROM or EPROM.

It is most suitable for test production during system development and for production in small amounts since it can operate under the same supply voltage as mask products.

The one-time PROM product is capable of writing only once and is effective for production of many kinds of sets in small quantities and early startup. The EPROM product allows program writing and rewriting, and is therefore suitable for system evaluation. The on-chip RAM has twice the capacity of the μPD75316/75P316, enabling large amounts of data to be processed.

**Details of functions are described in the User's Manual shown below. Be sure to read in design.**

**μPD75308 User's Manual : IEM-5016**

### FEATURES

- Compatible (excluding mask option) with the mask products
- Memory capacity
  - Program memory (PROM) : 16256 × 8 bits
  - Data memory (RAM) : 1024 × 4 bits
- Low-voltage operation capability: 2.7 to 6.0 V

### ORDERING INFORMATION

Ordering Code	Package	On-Chip ROM
μPD75P316AGF-3B9	80-pin plastic QFP (14 × 20 mm)	One-time PROM
μPD75P316AK	80-pin ceramic WQFN (LCC with window)	EPROM

### QUALITY GRADE

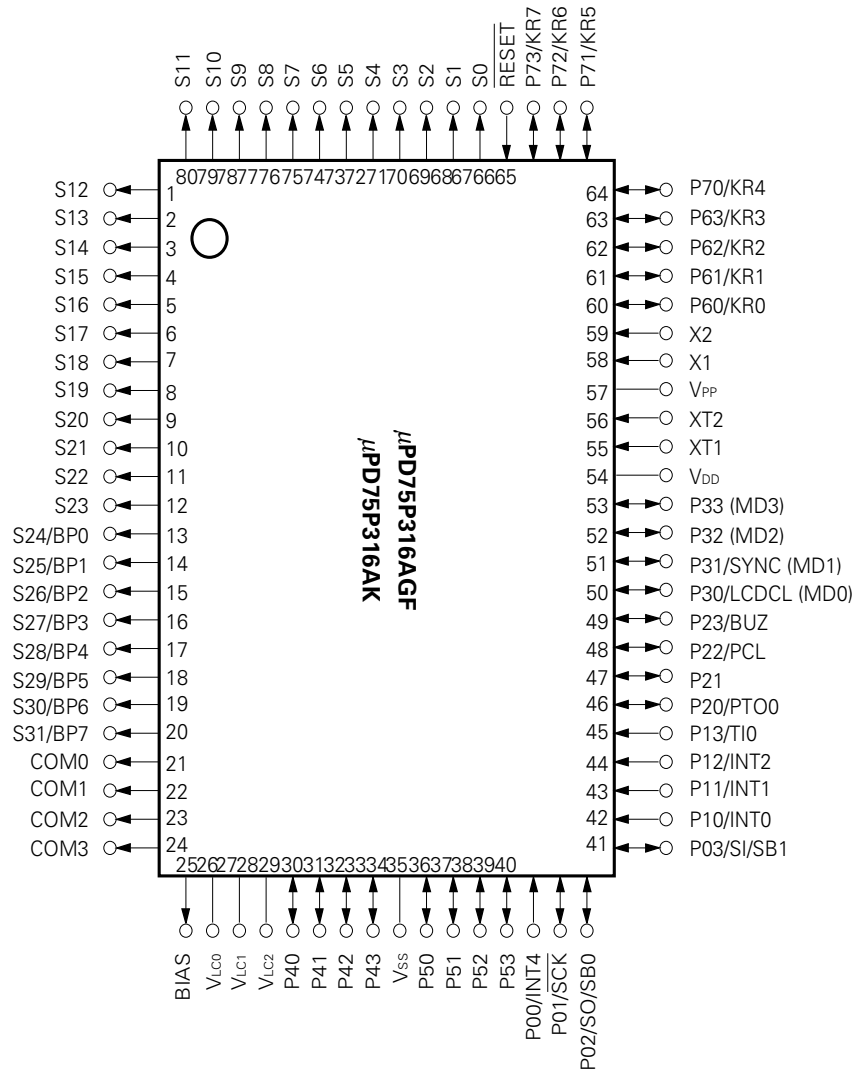
Ordering Code	Package	Quality Grade
μPD75P316AGF-3B9	80-pin plastic QFP (14 × 20 mm)	Standard
μPD75P316AK	80-pin ceramic WQFN (LCC with window)	Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

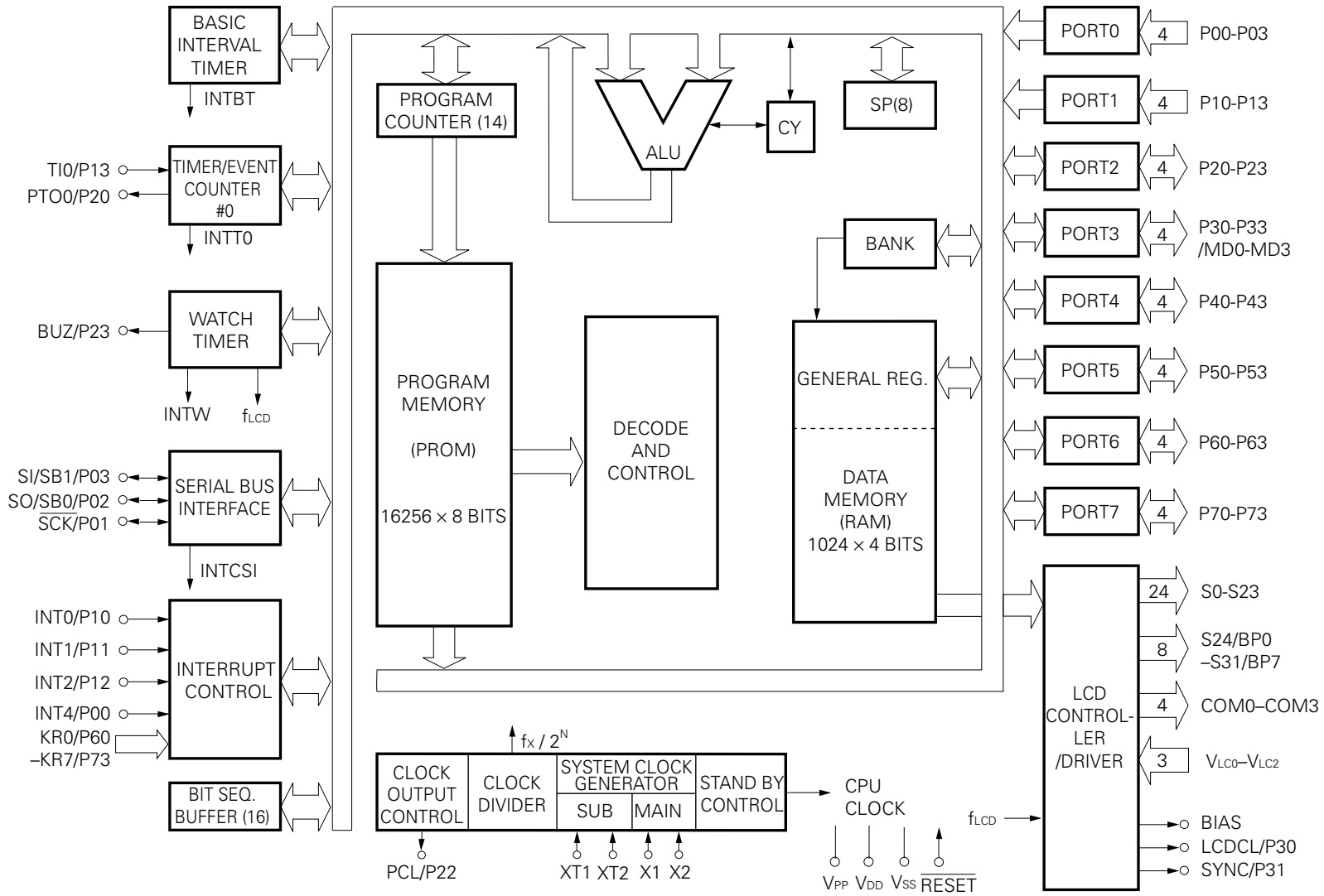
**In descriptions common to one-time PROM products and EPROM products in this document, the term "PROM" is used.**

The information in this document is subject to change without notice.

**PIN CONFIGURATION (Top View)**



BLOCK DIAGRAM



CONTENTS

1. PIN FUNCTIONS ..... 5

    1.1 PORT PINS ..... 5

    1.2 OTHER PINS ..... 7

    1.3 PIN INPUT/OUTPUT CIRCUITS ..... 9

★ 1.4 CAUTION ON USING P00/INT4 PIN AND  $\overline{\text{RESET}}$  PIN ..... 11

2. DIFFERENCES BETWEEN PRODUCTS IN SERIES ..... 11

3. DATA MEMORY (RAM) ..... 13

4. PROGRAM MEMORY WRITE AND VERIFY ..... 15

    4.1 PROGRAM MEMORY WRITE/VERIFY OPERATING MODES ..... 15

    4.2 PROGRAM MEMORY WRITING PROCEDURE ..... 16

    4.3 PROGRAM MEMORY READING PROCEDURE ..... 17

    4.4 ERASURE METHOD ..... 18

5. ELECTRICAL SPECIFICATIONS ..... 19

6. PACKAGE INFORMATION ..... 35

7. RECOMMENDED SOLDERING CONDITIONS ..... 37

APPENDIX A. DEVELOPMENT TOOLS ..... 38

★ APPENDIX B. RELATED DOCUMENTS ..... 39

1. PIN FUNCTIONS

1.1 PORT PINS (1/2)

Pin Name	Input/Output	Dual-Function Pin	Function	8-Bit I/O	Afer Reset	I/O Circuit Type*1
P00	Input	INT4	4-bit input port (PORT0) Internal pull-up resistor specification by software is possible for P01 to P03 as a 3-bit unit.	×	Input	ⓑ
P01	Input/output	SCK				ⓕ - A
P02	Input/output	SO/SB0				ⓕ - B
P03	Input/output	SI/SB1				Ⓜ - C
P10	Input	INT0	4-bit input port (PORT1) Internal pull-up resistor specification by software is possible as a 4-bit unit. With noise elimination circuit	×	Input	ⓑ - C
P11		INT1				
P12		INT2				
P13		TI0				
P20	Input/output	PTO0	4-bit input/output port (PORT2) Internal pull-up resistor specification by software is possible as a 4-bit unit.	×	Input	E - B
P21		—				
P22		PCL				
P23		BUZ				
P30 *2	Input/output	LCDCL MD0	Programmable 4-bit input/output port (PORT3) Input/output settable bit-wise. Internal pull-up resistor specification by software is possible as a 4-bit unit.	×	Input	E - B
P31 *2		SYNC MD1				
P32 *2		MD2				
P33 *2		MD3				
P40 to P43*2	Input/output	—	N-ch open-drain 4-bit input/output port (PORT 4). Data input/output pins for program memory (PROM) write/verify (low-order 4 bits).	○	High impedance	M - A
P50 to P53 *2	Input/output	—	N-ch open-drain 4-bit input/output port (PORT 5) Data input/output pins for program memory (PROM) write/verify (high-order 4 bits).		High impedance	M - A
P60	Input/output	KR0	Programmable 4-bit input/output port (PORT6). Input/output settable bit-wise. Internal pull-up resistor specification by software is possible as a 4-bit unit.	○	Input	ⓕ - A
P61		KR1				
P62		KR2				
P63		KR3				
P70	Input/output	KR4	4-bit input/output port (PORT7). Internal pull-up resistor specification by software is possible as a 4-bit unit.	○	Input	ⓕ - A
P71		KR5				
P72		KR6				
P73		KR7				

- \* 1. ○ : Indicates a Schmitt-triggered input.
- 2. Direct LED drive capability.

1.1 PORT PINS (2/2)

Pin Name	Input/Output	Dual-Function Pin	Function	8-Bit I/O	After Reset	I/O Circuit TYPE
BP0	Output	S24	1-bit output port (BIT PORT) Dual-function as segment output pins.	×	*	G - C
BP1		S25				
BP2		S26				
BP3		S27				
BP4	Output	S28				
BP5		S29				
BP6		S30				
BP7		S31				

\* For BP0 to BP7, V<sub>LC1</sub> is selected as the input source. The output level depends on BP0 to BP7 and the V<sub>LC1</sub> external circuit, however.

1.2 OTHER PINS

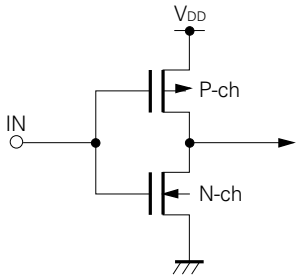
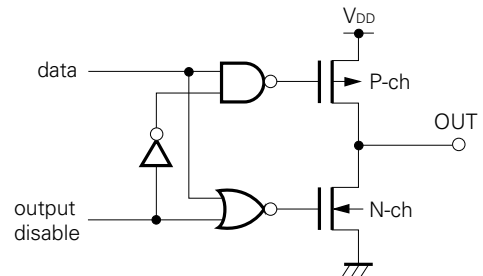
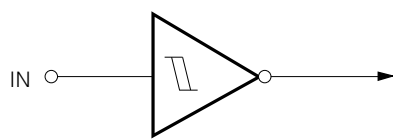
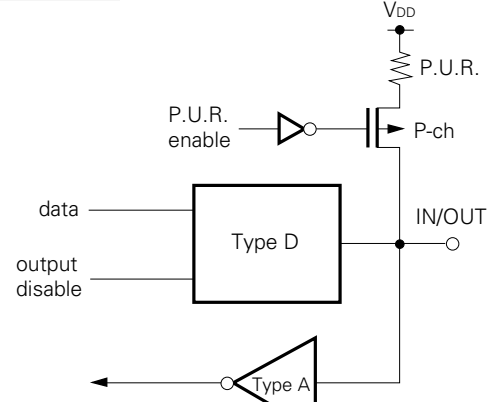
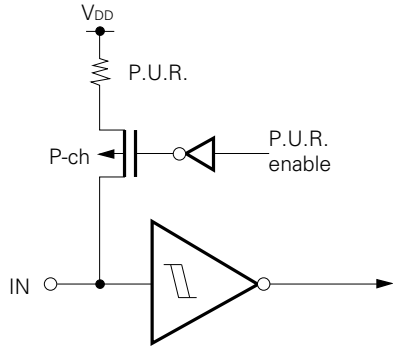
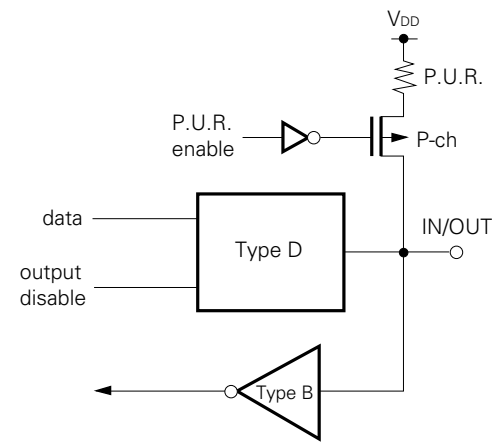
Pin Name	Input/Output	Dual-Function Pin	Function	After Reset	I/O Circuit Type *1
T10	Input	P13	External event pulse input pin for timer/event counter.	—	ⓑ - C
PTO0	output	P20	Timer/event counter output pin	Input	E - B
PCL	Input/output	P22	Clock output pin	Input	E - B
BUZ	Input/output	P23	Fixed frequency output pin (for buzzer or system clock trimming)	Input	E - B
$\overline{\text{SCK}}$	Input/output	P01	Serial clock input/output pin	Input	Ⓕ - A
SO/SB0	Input/output	P02	Serial data output pin Serial bus input/output pin	Input	Ⓕ - B
SI/SB1	Input/output	P03	Serial data input pin Serial bus input/output pin	Input	Ⓜ - C
INT4	Input	P00	Edge-detected vectored interrupt input pin (rising or falling edge detection).	—	ⓑ
INT0	Input	P10	Edge-detected vectored interrupt input pin (detection edge selectable)	—	ⓑ - C
INT1		P11			
INT2	Input	P12	Edge-detected testable input pin (rising edge detection)	—	ⓑ - C
KR0 to KR3	Input/output	P60 to P63	Testable Input/output pins (parallel falling edge detection)	Input	Ⓕ - A
KR4 to KR7	Input/output	P70 to P73	Testable Input/output pins (parallel falling edge detection)	Input	Ⓕ - A
S0 to S23	Output	—	Segment signal output pins	*3	G - A
S24 to S31	Output	BP0 to 7	Segment signal output pins	*3	G - C
COM0 to COM3	Output	—	Common signal output pins	*3	G - B
$V_{LC0}$ to $V_{LC2}$	—	—	LCD drive power supply pins	—	—
BIAS	—	—	External split cutting output pin	High impedance	—
LCDCL*2	Input/output	P30	External extension driver drive clock output pin	Input	E - B
SYNC*2	Input/output	P31	External extension driver synchronization clock output pin	Input	E - B
X1, X2	Input	—	Main system clock oscillation crystal/ceramic connection pins. When an external clock is used, the clock is input to X1 and the inverted clock to X2.	—	—
XT1, XT2	Input	—	Subsystem clock oscillation crystal connection pins When an external clock is used, the clock is input to XT1 and the inverted clock to XT2. XT1 can be used as a 1-bit input (test) pin.	—	—
$\overline{\text{RESET}}$	Input	—	System reset input pin (low-level active).	—	ⓑ
MD0 to MD3	Input/output	P30 to P33	Mode selection pin for program memory (PROM) write/verify.	Input	E - B
$V_{PP}$	—	—	Program voltage application pin for program memory (PROM) write/verify. Connected to $V_{DD}$ in normal operation. Applies +12.5 V in program memory write/verify.	—	—
$V_{DD}$	—	—	Positive power supply pin	—	—
$V_{SS}$	—	—	GND potential pin	—	—

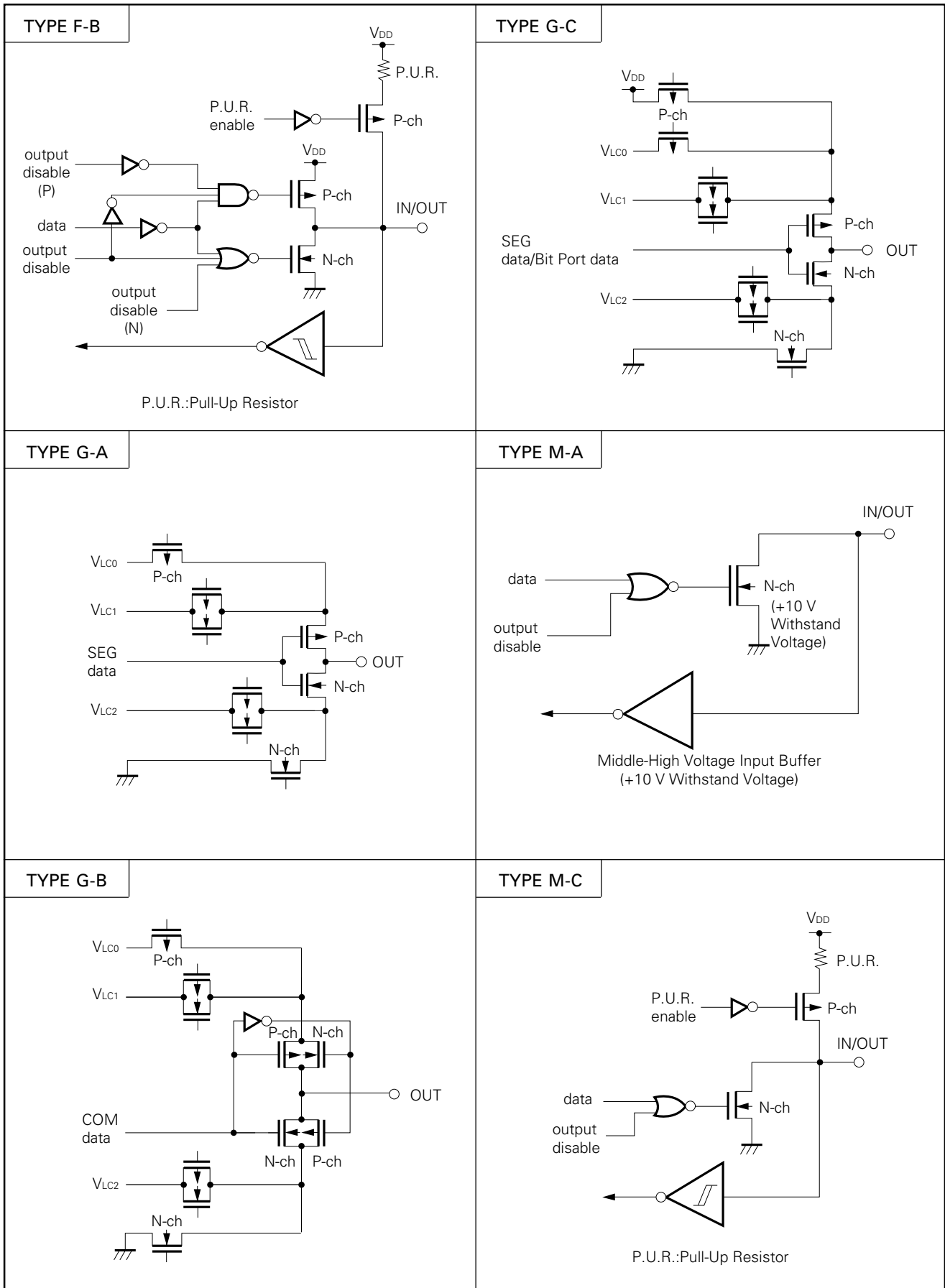
- \* 1. ○ : Indicates a Schmitt-triggered input.
- 2. Pins provided for future system expansion. Currently used only as pins 30 and 31.
- 3.  $V_{LCx}$  shown below can be selected for display outputs.  
S0 to S31:  $V_{LC1}$ , COM0 to COM2:  $V_{LC2}$  , COM3:  $V_{LC0}$   
However, display output levels depend on the display output and  $V_{LCx}$  external circuit.



1.3 PIN INPUT/OUTPUT CIRCUITS

The input/output circuits of each pin of the μPD75P316A are shown by in abbreviated form.

<p><b>TYPE A (For TYPE E-B)</b></p>  <p>CMOS standard input buffer</p>	<p><b>TYPE D (For TYPE E-B, F-A)</b></p>  <p>Push-pull output that can be made high-impedance output (P-ch and N-ch OFF)</p>
<p><b>TYPE B</b></p>  <p>Schmitt trigger input with hysteresis characteristic</p>	<p><b>TYPE E-B</b></p>  <p>P.U.R.: Pull-Up Resistor</p>
<p><b>TYPE B-C</b></p>  <p>P.U.R. : Pull-Up Resistor</p> <p>Schmitt trigger input with hysteresis characteristic</p>	<p><b>TYPE F-A</b></p>  <p>P.U.R.: Pull-Up Resistor</p>



**1.4 CAUTION ON USING P00/INT4 PIN AND RESET PIN**



The P00/INT4 and  $\overline{\text{RESET}}$  pins have a test mode setting function (IC test only) which tests internal operations of the μPD75P316A in addition to those functions given in 1.1 and 1.2.

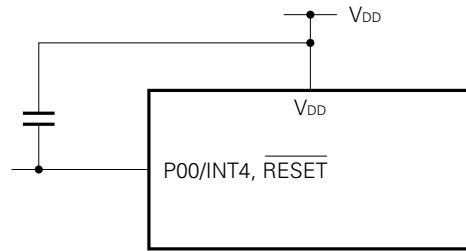
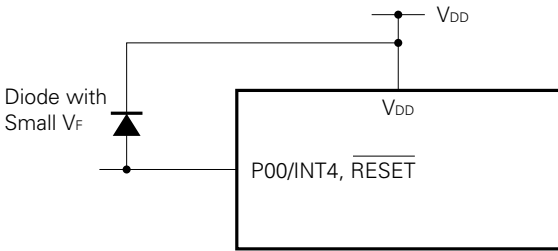
The test mode is set when voltage greater than  $V_{DD}$  is applied to either pin. Therefore, even during normal operation, the test mode is engaged when noise greater than  $V_{DD}$  is added, thus causing interference with normal operation.

For example, this problem may occur if the P00/INT4 and  $\overline{\text{RESET}}$  pins wiring is too long, causing line noise.

To avoid this, try to suppress line noise in wiring. If line noise is still high, try eliminating the noise using the exterior add-on components shown in the Figures below.

- Connect a diode with low  $V_F$  between the  $V_{DD}$  and the pin.

- Connect a condenser between the  $V_{DD}$  and the pin.



**2. DIFFERENCES BETWEEN PRODUCTS IN SERIES**

The μPD75P316A is a product of the μPD75316 with on-chip mask ROM having been replaced with the one-time PROM or EPROM. If you use PROM for debugging the applied system or trial manufacturing, and proceed to use masked ROM products for mass production, do so only with a full understanding of their differences beforehand.

Also, μPD75P316A functions are an extension of those of the μPD75P316. Table 2-1 shows the differences between the series products. All products have the same functions except as indicated in this table.

For the details of the CPU functions and the built-in hardware, please refer to the μPD75308 User's Manual (IEM-5016).

Table 2-1 Differences between Products in Series

Product Name		$\mu$ PD75304/75306/75308	$\mu$ PD75312/75316	$\mu$ PD75304B/75306B/75308B	$\mu$ PD75312B/75316B	$\mu$ PD75P308	$\mu$ PD75P316	$\mu$ PD75P316A	$\mu$ PD75P316B*1		
Comparison Item											
ROM( $\times$ 8 bits)		Mask ROM 4K/6K/8K	Mask ROM 12K/16K	Mask ROM 4K/6K/8K	Mask ROM 12K/16K	One-time PROM, EPROM 8K	One-time PROM 16K	One-time PROM, EPROM 16K	One-time PROM 16K		
RAM( $\times$ 4 bits)		512			1024	512		1024			
Mask option		Port 4, 5 pull-up resistor incorporated LCD driving power supplying split resistor				No					
Pin connection	No. 50 to 53	P30 to P33				P30/MD0 to P33/MD3					
	No. 57	NC			IC	$V_{PP}$					
★ Electrical specifications		Masked ROM products and PROM products have different current dissipation and operating temperature range *2. For details, refer to the electrical specifications of respective data sheet.									
Power supply voltage range		2.7 to 6.0 V		2.0 to 6.0 V		2.0 to 5.5 V		5 V $\pm$ 5 %			
Operating temperature range		-40 to +85 °C				-10 to +70 °C		-40 to +85 °C		Under investigation	
Package		• 80-pin plastic QFP (14 $\times$ 20)		• 80-pin plastic QFP (□14) • 80-pin plastic QFP (14 $\times$ 20) • 80-pin plastic TQFP (□12)		• 80-pin plastic QFP (□14) • 80-pin plastic TQFP (□12)		• 80-pin plastic QFP (14 $\times$ 20) • 80-pin ceramic WQFN (LCC with window)		• 80-pin plastic QFP (14 $\times$ 20) • 80-pin ceramic WQFN (LCC with window)	
★ On-chip PROM product		$\mu$ PD75P308	$\mu$ PD75P316 $\mu$ PD75P316A	$\mu$ PD75P316A $\mu$ PD75P316B	$\mu$ PD75P316B	—					
★ Others		Masked ROM products and PROM products have different noise endurance limits and noise radiation due to differing circuit scales and mask layouts.									

- \* 1. The  $\mu$ PD75P316B is under development.  
2. The  $\mu$ PD75P316A is the same as the mask ROM products.

★ **Note** PROM and masked ROM have different noise endurance limits and noise radiation. When considering replacement of masked ROM products after trial manufacturing with PROM products, sufficient evaluation of CS products (not ES products) with masked ROM products should be performed.

### 3. DATA MEMORY (RAM)

Fig. 3-1 shows the data memory configuration. It consists of a data area and a peripheral hardware area. The data memory consists of memory banks 0 to 3 with each bank consisting of 256 words × 4 bits. Peripheral hardware has been assigned to the area of memory bank 15.

#### (1) Data area

The data area comprises a static RAM. It is used to store program data and as a subroutine, interrupt execution stack memory. Even if the CPU operation is stopped in the standby mode, it is possible to hold the memory content for a long time by battery backup, etc. The data area is operated by memory manipulation instructions.

The static RAM has been mapped to memory banks 0, 1, 2 and 3 by 256 × 4 bits each. Bank 0 has been mapped as a data area but is also available as a general register area (000H to 007H) and a stack area (000H to 0FFH) (banks 1, 2 and 3 are available only as a data area).

In the static RAM, 1 address consists of 4 bits. It can be operated in units of 8 bits by 8-bit memory manipulation instructions or in bits by bit manipulation instructions, however. In an 8-bit manipulation instruction, an even address should be specified.

##### (a) General register area

The general register area can be operated either by general register operation instructions or by memory manipulation instructions. Up to eight 4-bit registers are available. That part of the 8 general registers which is not used in the program is available as a data area or a stack area.

##### (b) Stack area

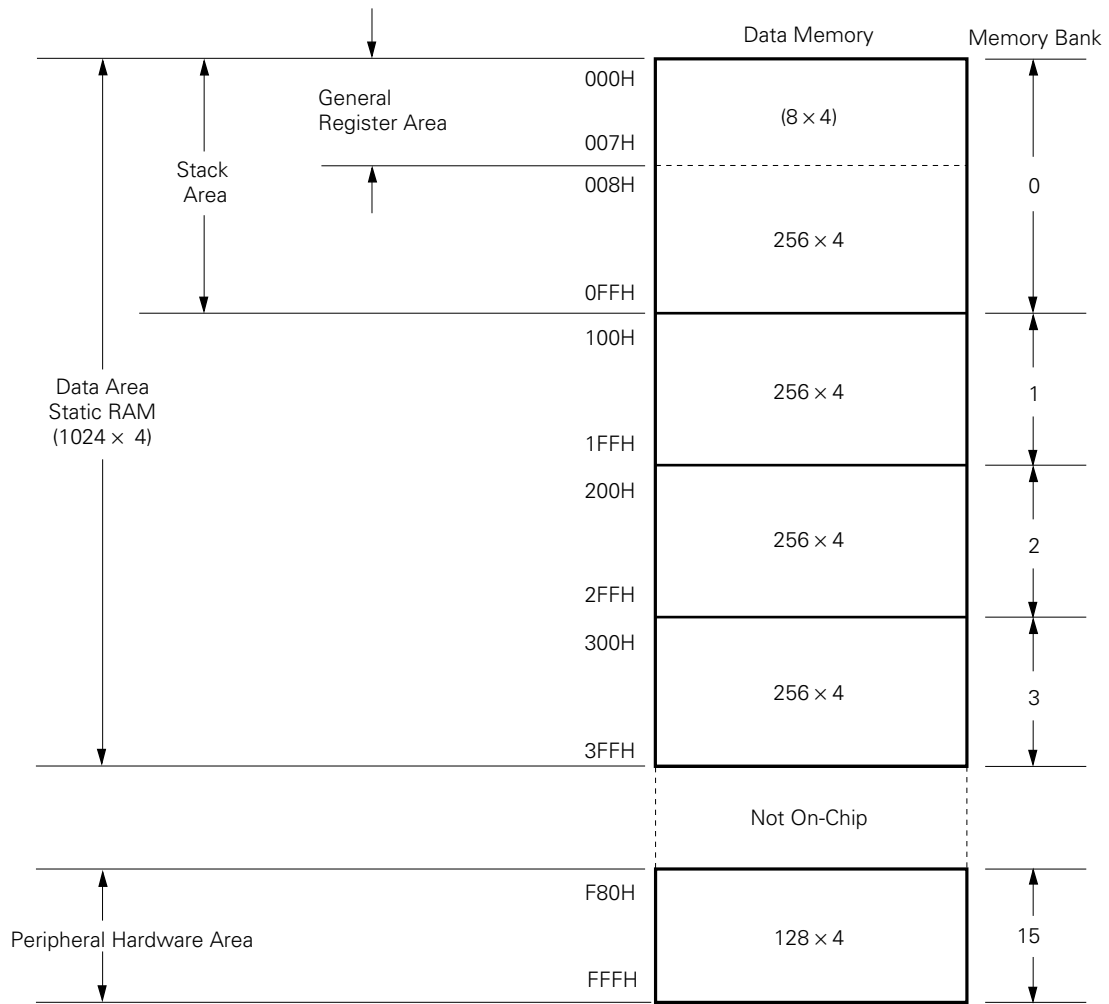
The stack area is set by an instruction. It is available as a subroutine execution or interrupt service execution save area.

#### (2) Peripheral hardware area

The peripheral hardware area has been mapped to F80H to FFFH of memory bank 15.

It is operated by memory manipulation instructions just as the static RAM. In the peripheral hardware, however, the operable bit unit differs from one address to another. An address to which peripheral hardware has not been assigned is inaccessible since no data memory is built in.

Fig. 3-1 Data Memory Map



#### 4. PROGRAM MEMORY WRITE AND VERIFY

The ROM built into the μPD75P316A is a 16256×8-bit electrically writable one-time PROM. The table below shows the pins used to program this PROM. There is no address input; instead, a method to update the address by the clock input via the X1 pin is adopted.

Pin Name	Function
V <sub>PP</sub>	Voltage application pin for program memory write/verify (normally V <sub>DD</sub> potential).
X1, X2	Address update clock inputs for program memory write/verify. Inverse of X1 pin signal is input to X2 pin.
MD0 to MD3	Operating mode selection pins for program memory write/verify.
P40 to P43 (low-order 4 bits) P50 to P53 (high-order 4 bits)	8-bit data input/output pins for program memory write/verify.
V <sub>DD</sub>	Supply voltage application pin. Applies 2.7 to 6.0 V in normal operation, and 6 V for program memory write/verify.

- Note**
1. A lightshield cover film should be applied to the μPD75P316AK provided with an erasure window, except when erasing the EPROM.
  2. The one-time PROM version of μPD75P316AGF is not provided with an erasure window, and therefore UV erasure is not possible.

##### 4.1 PROGRAM MEMORY WRITE/VERIFY OPERATING MODES

The μPD75P316A assumes the program memory write/verify mode when +6 V and +12.5 V are applied respectively to the V<sub>DD</sub> and V<sub>PP</sub> pins. The table below shows the operating modes available by the MD0 to MD3 pin setting in this mode. All the remaining pins are at the V<sub>SS</sub> potential by the pull-down resistor.

Operating Mode Setting						Operating Mode
V <sub>PP</sub>	V <sub>DD</sub>	MD0	MD1	MD2	MD3	
+12.5 V	+6 V	H	L	H	L	Program memory address zero-clear
		L	H	H	H	Write mode
		L	L	H	H	Verify mode
		H	×	H	H	Program inhibit mode

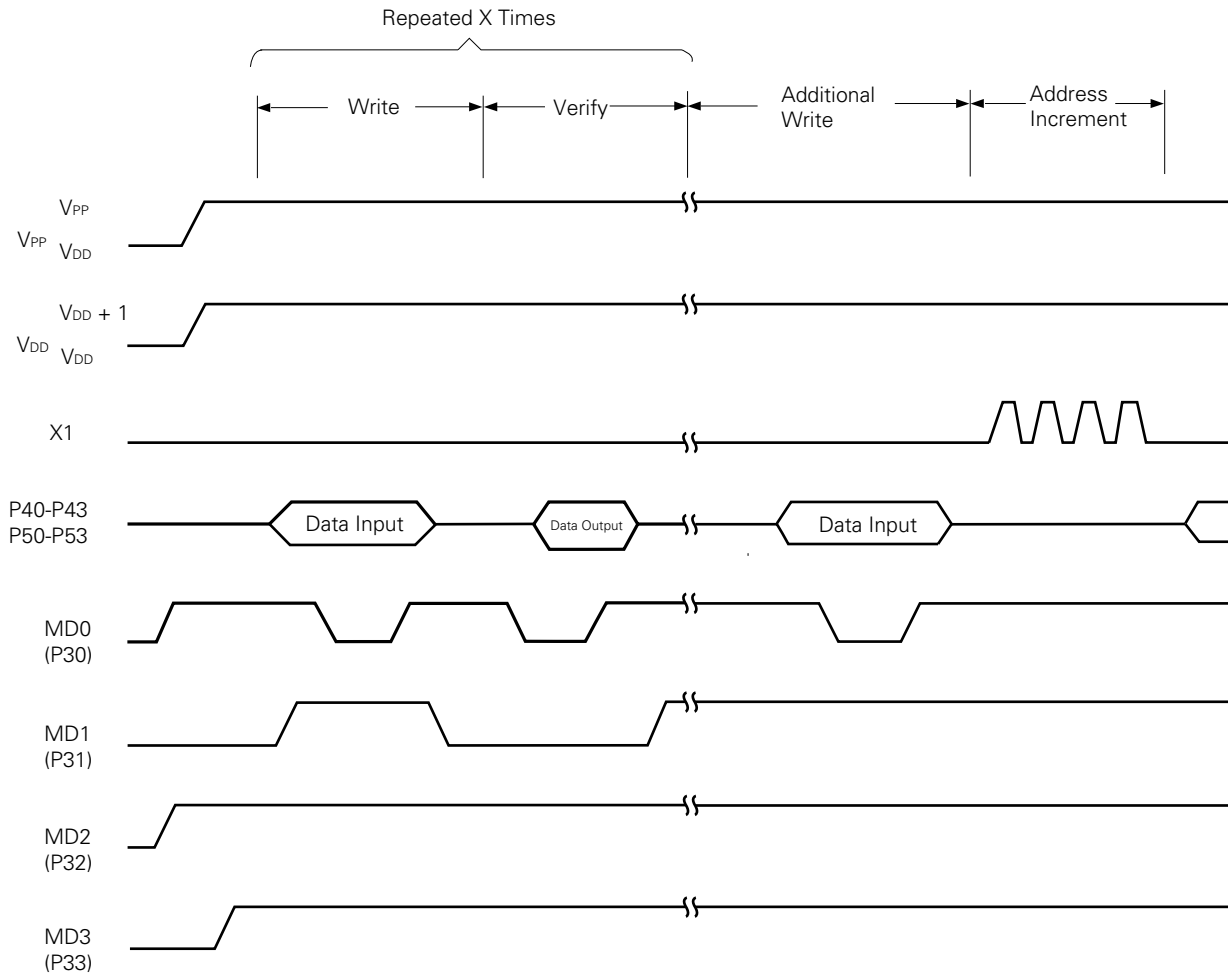
×: L or H

**4.2 PROGRAM MEMORY WRITING PROCEDURE**

The program memory writing procedure is shown below. High-speed write is possible.

- (1) Pull down a pin which is not used to V<sub>SS</sub> via the resistor. The X1 pin is at the low level.
- (2) Supply 5 V to the V<sub>DD</sub> and V<sub>PP</sub> pins.
- (3) 10 μs wait.
- (4) The program memory address 0 clear mode.
- (5) Supply 6 V and 12.5 V respectively to V<sub>DD</sub> and V<sub>PP</sub>.
- (6) The program inhibit mode.
- (7) Write data in the 1-ms write mode.
- (8) The program inhibit mode.
- (9) The verify mode. If written, proceed to (10); if not written, repeat (7) to (9).
- (10) (Number of times written in (7) to (9): X) × 1-ms additional write.
- (11) The program inhibit mode.
- (12) Update (+1) the program memory address by inputting 4 pulses to the X1 pin.
- (13) Repeat (7) to (12) up to the last address.
- (14) The program memory address 0 clear mode.
- (15) Change the V<sub>DD</sub> and V<sub>PP</sub> pins voltage to 5 V.
- (16) Power off.

The diagram below shows the procedure of the above (2) to (12).



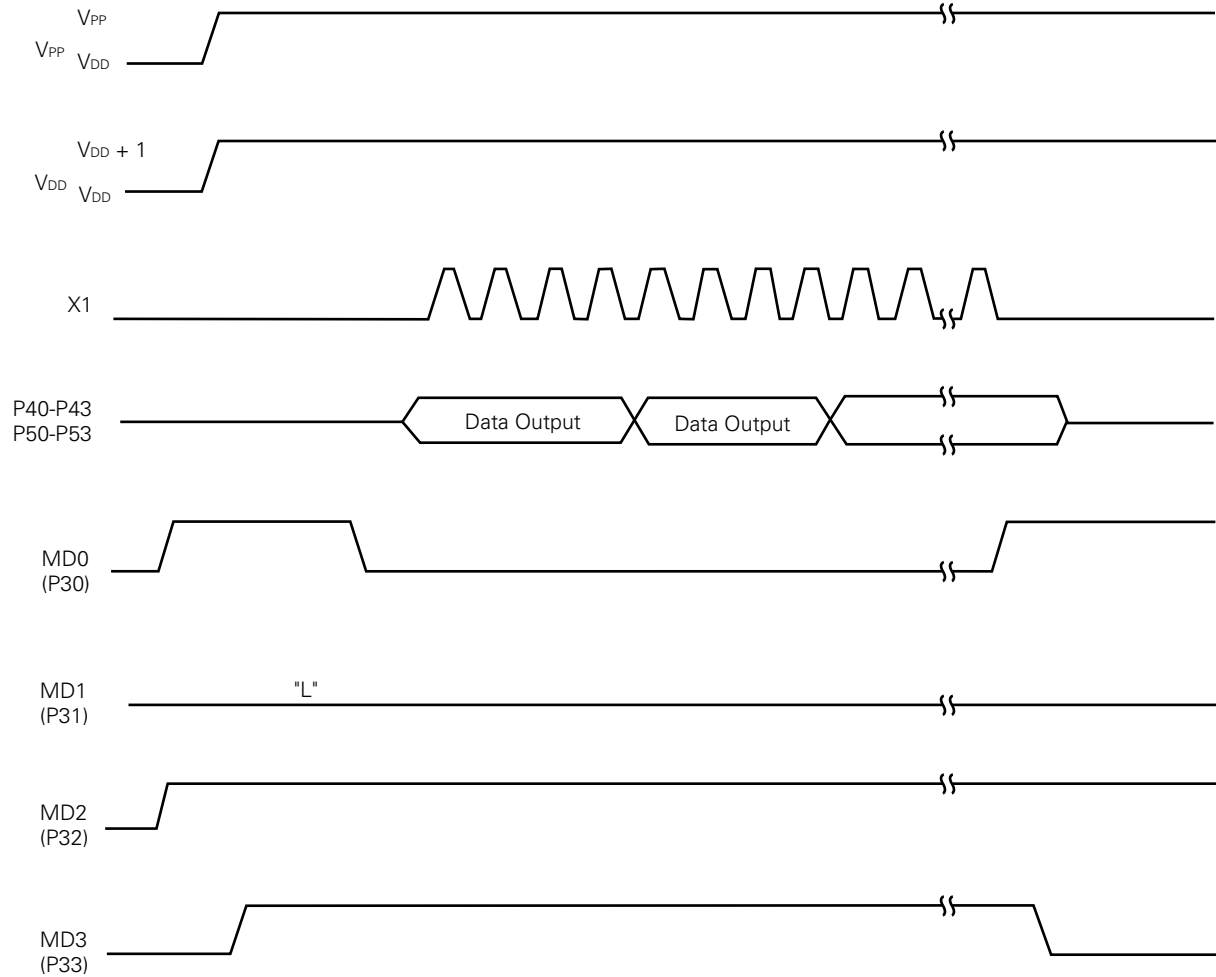


**4.3 PROGRAM MEMORY READING PROCEDURE**

The μPD75P316A can read the content of the program memory in the following procedure. It reads in the verify mode.

- (1) Pull down a pin which is not used to V<sub>SS</sub> via the resistor. The X1 pin is at the low level.
- (2) Supply 5 V to the V<sub>DD</sub> and V<sub>PP</sub> pins.
- (3) 10 μs wait.
- (4) The program memory address 0 clear mode.
- (5) Supply 6 V and 12.5 V respectively to V<sub>DD</sub> and V<sub>PP</sub>.
- (6) The program inhibit mode.
- (7) The verify mode. If clock pulses are input to the X1 pin, data is output sequentially 1 address at a time at the period of inputting 4 pulses.
- (8) The program inhibit mode.
- (9) The program memory address 0 clear mode.
- (10) Change the V<sub>DD</sub> and V<sub>PP</sub> pins voltage to 5 V.
- (11) Power off.

The diagram below shows the procedure of the above (2) to (9).



#### 4.4 ERASING METHOD ( $\mu$ PD75P316AK ONLY)

The content of the data programmed in the  $\mu$ PD75P316A is erased as ultraviolet rays are irradiated to the window in the upper part.

The erasable ultraviolet-ray wavelength is about 250 nm.

The dose required for complete erasure is  $15 \text{ W}\cdot\text{s}/\text{cm}^2$  (ultraviolet-ray intensity  $\times$  erasure time). If a commercially available ultraviolet-ray lamp (wavelength 254 nm, intensity  $12 \text{ mW}/\text{cm}^2$ ) is used, it takes about 15 to 20 minutes to erase.

- Note**
1. The content may be erased if exposed to direct sunlight or fluorescent lamp light for a long time. To protect the content, the window in the upper part should be masked with a lightshield cover film. NEC attaches such a lightshield cover film to each UV EPROM product.
  2. When erasing, the distance between the ultraviolet-ray lamp and the  $\mu$ PD75P316A should be kept normally within 2.5 cm.

**Remarks** It may take longer to erase if the ultraviolet-ray lamp has deteriorated or if the package window is dirty and so on.

5. ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C)

PARAMETER	SYMBOL	TEST CONDITIONS		RATING	UNIT
Power supply voltage	V <sub>DD</sub>			-0.3 to +7.0	V
	V <sub>PP</sub>			-0.3 to +13.5	V
Input voltage	V <sub>I1</sub>	Except ports 4, 5		-0.3 to V <sub>DD</sub> +0.3	V
	V <sub>I2</sub>	Ports 4, 5	Open-drain	-0.3 to +11	V
Output voltage	V <sub>O</sub>			-0.3 to V <sub>DD</sub> +0.3	V
Output current high	I <sub>OH</sub>	1 pin		-15	mA
		All pins		-30	mA
Output current low	I <sub>OL</sub> *	1 pin	Peak value	30	mA
			Effective value	15	mA
		Total of ports 0, 2, 3, 5	Peak value	100	mA
			Effective value	60	mA
		Total of ports 4, 6, 7	Peak value	100	mA
			Effective value	60	mA
Operating temperature	T <sub>opt</sub>			-40 to +85	°C
Storage temperature	T <sub>stg</sub>			-65 to +150	°C

\* Calculate the effective value with the formula [Effective value] = [Peak value] × √duty.

CAPACITANCE (Ta = 25 °C, V<sub>DD</sub> = 0 V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C <sub>IN</sub>	f = 1 MHz Unmeasured pin returned to 0 V			15	pF
Output capacitance	C <sub>OUT</sub>				15	pF
Input /output capacitance	C <sub>IO</sub>				15	pF

**MAIN SYSTEM CLOCK OSCILLATOR CHARACTERISTICS (Ta = -40 to +85 °C, VDD = 2.7 to 6.0 V)**

RESONATOR	RECOMMENDED CIRCUIT	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Ceramic resonator		Oscillator frequency (fx) *1		1.0		5.0*3	MHz
		Oscillation stabilization time *2	After VDD reaches the minimum value in the oscillation voltage range			4	ms
Crystal resonator		Oscillator frequency (fx) *1		1.0	4.19	5.0*3	MHz
		Oscillation stabilization time *2	VDD = 4.5 to 6.0 V			10	ms
External clock		X1 input frequency (fx) *1		1.0		5.0*3	MHz
		X1 high and low level widths (txH, txL)		100		500	ns

- \* 1. Oscillator characteristics only. Refer to the description of AC characteristics for details of instruction execution time.
- 2. Time required for oscillation to become stabilized after VDD reaches MIN. of the oscillation voltage range or after STOP mode release.
- 3. When the oscillator frequency is 4.19 MHz < fx ≤ 5.0 MHz, do not select PPC = 0011 as instruction execution time. If PCC = 0011 is selected, 1 machine cycle becomes less than 0.95 μs, with the result that specified MIN. value 0.95 μs can not be observed.

**SUBSYSTEM CLOCK OSCILLATOR CHARACTERISTICS (Ta = -40 to +85 °C, VDD = 2.7 to 6.0 V)**

RESONATOR	RECOMMENDED CIRCUIT	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Crystal resonator		Oscillator frequency (fxT)		32	32.768	35	kHz
		Oscillation stabilization time*	VDD = 4.5 to 6.0 V			1.0	2
External clock		XT1 input frequency (fxT)		32		100	kHz
		XT1 high and low level widths (txTH, txTL)		5		15	μs

- \* Time required for oscillation to become stabilized after  $V_{DD}$  reaches MIN. of the oscillation voltage range or after STOP made release.

**Note** When the main system clock and subsystem clock oscillation circuit are used, the area enclosed by dotted line in the figure should be wired as follows to prevent influence from the wiring capacitance, etc..

- Wiring should be as short as possible.
- Do not cross other signal lines.  
Do not place the circuit closed to a line in which varying high current flows.
- The connecting point of oscillation circuit capacitor should always be the same potential as  $V_{DD}$ . Do not connect it to the power supply pattern in which high current flows.
- Do not pick up a signal from the oscillation circuit.

The subsystem clock oscillation circuit is designed to be low amplification circuit for low dissipation current, thus misoperation due to noise occurs more often than with the main system clock oscillation circuit. Therefore, when the subsystem clock is used, care is needed especially for the wiring procedure.

DC CHARACTERISTICS (Ta = -40 to +85 °C, VDD = 2.7 to 6.0 V) (1/2)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Input voltage high	V <sub>IH1</sub>	Ports 2 and 3		0.7 V <sub>DD</sub>		V <sub>DD</sub>	V
	V <sub>IH2</sub>	Ports 0, 1, 6, 7, $\overline{\text{RESET}}$		0.8 V <sub>DD</sub>		V <sub>DD</sub>	V
	V <sub>IH3</sub>	Ports 4 and 5	Open-drain	0.7 V <sub>DD</sub>		10	V
	V <sub>IH4</sub>	X1, X2, XT1		V <sub>DD</sub> - 0.5		V <sub>DD</sub>	V
Input voltage low	V <sub>IL1</sub>	Ports 2, 3, 4 and 5		0		0.3 V <sub>DD</sub>	V
	V <sub>IL2</sub>	Ports 0, 1, 6, 7, $\overline{\text{RESET}}$		0		0.2 V <sub>DD</sub>	V
	V <sub>IL3</sub>	X1, X2, XT1		0		0.4	V
Output voltage high	V <sub>OH1</sub>	Ports 0, 2, 3, 6, 7, BIAS	V <sub>DD</sub> = 4.5 to 6.0 V I <sub>OH</sub> = -1 mA	V <sub>DD</sub> - 1.0			V
			I <sub>OH</sub> = -100 μA	V <sub>DD</sub> - 0.5			V
	V <sub>OH2</sub>	BP0 to BP7 (with 2 I <sub>OH</sub> outputs)	V <sub>DD</sub> = 4.5 to 6.0 V I <sub>OH</sub> = -100 μA	V <sub>DD</sub> - 2.0			V
			I <sub>OH</sub> = -30 μA	V <sub>DD</sub> - 1.0			V
Output voltage low	V <sub>OL1</sub>	Ports 0, 2, 3, 4, 5, 6 and 7	Ports 3, 4 and 5 V <sub>DD</sub> = 4.5 to 6.0 V I <sub>OL</sub> = 15 mA		0.4	2.0	V
			V <sub>DD</sub> = 4.5 to 6.0 V I <sub>OL</sub> = 1.6 mA			0.4	V
			I <sub>OL</sub> = 400 μA			0.5	V
		SB0, 1	Open-drain pull-up resistor ≥ 1 kΩ			0.2 V <sub>DD</sub>	V
	V <sub>OL2</sub>	BP0 to BP7 (with 2 I <sub>OL</sub> outputs)	V <sub>DD</sub> = 4.5 to 6.0 V I <sub>OL</sub> = 100 μA			1.0	V
			I <sub>OL</sub> = 50 μA			1.0	V
Input leakage current high	I <sub>LIH1</sub>	V <sub>IN</sub> = V <sub>DD</sub>	Other than below			3	μA
	I <sub>LIH2</sub>		X1, X2, XT1			20	μA
	I <sub>LIH3</sub>	V <sub>IN</sub> = 10 V	Ports 4 and 5 (when open-drain)			20	μA
Input leakage current low	I <sub>LIL1</sub>	V <sub>IN</sub> = 0 V	Other than below			-3	μA
	I <sub>LIL2</sub>		X1, X2, XT1			-20	μA

DC CHARACTERISTICS (Ta = -40 to +85 °C, VDD = 2.7 to 6.0 V) (1/2)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	
Output leakage current high	I <sub>LOH1</sub>	V <sub>OUT</sub> = V <sub>DD</sub>	Other than below			3	μA	
	I <sub>LOH2</sub>	V <sub>OUT</sub> = 10 V	Ports 4 and 5 (when open-drain)			20	μA	
Output leakage current low	I <sub>LOL</sub>	V <sub>OUT</sub> = 0 V				-3	μA	
On-chip pull-up resistor	R <sub>L1</sub>	Ports 0, 1, 2, 3, 6 and 7 (Except P00) V <sub>IN</sub> = 0 V	V <sub>DD</sub> = 5.0 V ±10%	15	40	80	kΩ	
			V <sub>DD</sub> = 3.0 V ±10%	30		300	kΩ	
LCD drive voltage	V <sub>LCD</sub>			2.5		V <sub>DD</sub>	V	
LCD output voltage deviation*1 (common)	V <sub>ODC</sub>	I <sub>O</sub> = ±5 μA	V <sub>LCD0</sub> = V <sub>LCD</sub> V <sub>LCD1</sub> = V <sub>LCD</sub> × 2/3 V <sub>LCD2</sub> = V <sub>LCD</sub> × 1/3	0		±0.2	V	
LCD output voltage deviation*1 (segment)	V <sub>ODC</sub>	I <sub>O</sub> = ±5μA	2.7 V ≤ V <sub>LCD</sub> ≤ V <sub>DD</sub>	0		±0.2	V	
Supply current*2	I <sub>DD1</sub>	4.19 MHz*3 crystal oscillation C1=C2 22 pF	V <sub>DD</sub> = 5 V ±10%*4		4.5	14	mA	
			V <sub>DD</sub> = 3 V ±10%*5		0.9	3	mA	
	I <sub>DD2</sub>		HALT mode V <sub>DD</sub> = 5 V ±10%		700	2100	μA	
			V <sub>DD</sub> = 3 V ±10%		300	900	μA	
	I <sub>DD3</sub>	32 kHz*6 crystal oscillation	Operating mode V <sub>DD</sub> = 3 V ±10%		100	300	μA	
	I <sub>DD4</sub>		HALT mode V <sub>DD</sub> = 3 V ±10%		20	60	μA	
	I <sub>DD5</sub>	XT1 = 0 V STOP mode	V <sub>DD</sub> = 5 V ±10%			0.5	20	μA
			V <sub>DD</sub> = 3 V ±10%		0.1	10	μA	
T <sub>a</sub> = 25°C					0.1	5	μA	
I <sub>DD6</sub>	32 kHz crystal oscillation STOP mode	V <sub>DD</sub> = 3 V ±10%*7			5	15	μA	

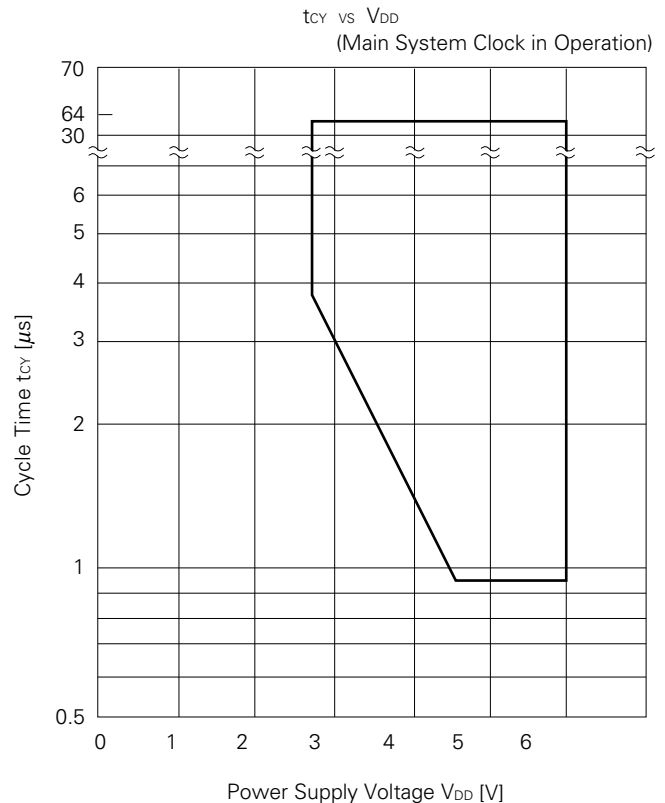
- \* 1. The voltage deviation is a difference between the segment and common output ideal value ( $V_{LCDn}$ ;  $n = 0, 1, 2$ ) and output voltage.
- 2. Current flowing in the internal pull-up resistor and LCD split resistor are not included.
- 3. Includes when the subsystem clock is oscillated.
- 4. When the processor clock control register (PCC) is set to 0011 and operated in high-speed mode.
- 5. When the PCC is set to 0000 and operated in low-speed mode.
- 6. When operated by the subsystem clock with the system clock control register (SCC) set to 1011 and the main system clock stops.
- 7. When the STOP instruction is executed during the main system clock operation and the subsystem clock is oscillated.



AC CHARACTERISTICS (Ta = -40 to +85 °C , VDD = 2.7 to 6.0 V)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
CPU clock cycle time (minimum instruction execution time = 1 machine cycle ) *1	tcy	Operation with main system clock	VDD = 4.5 to 6.0 V	0.95		64	μs
				3.8		64	μs
		Operation with subsystem clock		114	122	125	μs
T10 input frequency	fTi	VDD = 4.5 to 6.0 V		0		1	MHZ
				0		275	kHz
T10 input high and low-level widths	tTIH,	VDD = 4.5 to 6.0 V		0.48			μs
	tTIL			1.8			μs
Interrupt input high and low-level widths	tINTH,	INT0		*2			μs
	tINTL	INT1, 2, 4		10			μs
		KR0-7		10			μs
RESET low-level width	trSL			10			μs

- \* 1. CPU clock (Φ) cycle time is determined by oscillator frequency of the connected resonator, system clock control register (SCC) and processor clock control register (PCC). Characteristics for power supply voltage VDD vs • cycle time tcy in main system clock operation is shown below.
- 2. It becomes 2tcy or 128/fx by interrupt mode register (IM0) setting.



**Serial Transfer Operation**

**2-wire and 3-wire serial I/O mode ( $\overline{\text{SCK}}$ ...Internal clock output)**

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
$\overline{\text{SCK}}$ cycle time	$t_{\text{KCY1}}$	$V_{\text{DD}} = 4.5 \text{ to } 6.0 \text{ V}$		1600			ns
				3800			ns
$\overline{\text{SCK}}$ high and low level widths	$t_{\text{KL1}}$	$V_{\text{DD}} = 4.5 \text{ to } 6.0 \text{ V}$		$t_{\text{KCY1}}/2-50$			ns
	$t_{\text{KH1}}$			$t_{\text{KCY1}}/2-150$			ns
SI setup time (to $\overline{\text{SCK}}\uparrow$ )	$t_{\text{SIK1}}$			150			ns
SI hold time (from $\overline{\text{SCK}}\uparrow$ )	$t_{\text{KSI1}}$			400			ns
SO output delay time from $\overline{\text{SCK}}\downarrow$	$t_{\text{KS01}}$	$R_{\text{L}} = 1 \text{ k } \Omega, C_{\text{L}} = 100 \text{ pF}^*$	$V_{\text{DD}} = 4.5 \text{ to } 6.0 \text{ V}$			250	ns
						1000	ns

\*  $R_{\text{L}}$  and  $C_{\text{L}}$  are SO output line load resistance and load capacitance, respectively.

**2-wire and 3-wire serial I/O mode ( $\overline{\text{SCK}}$ ...External clock input)**

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
$\overline{\text{SCK}}$ cycle time	$t_{\text{KCY2}}$	$V_{\text{DD}} = 4.5 \text{ to } 6.0 \text{ V}$		800			ns
				3200			ns
$\overline{\text{SCK}}$ high and low level widths	$t_{\text{KL2}}$	$V_{\text{DD}} = 4.5 \text{ to } 6.0 \text{ V}$		400			ns
	$t_{\text{KH2}}$			1600			ns
SI setup time (to $\overline{\text{SCK}}\uparrow$ )	$t_{\text{SIK2}}$			100			ns
SI hold time (from $\overline{\text{SCK}}\uparrow$ )	$t_{\text{KSI2}}$			400			ns
SO output delay time from $\overline{\text{SCK}}\downarrow$	$t_{\text{KS02}}$	$R_{\text{L}} = 1 \text{ k } \Omega, C_{\text{L}} = 100 \text{ pF}^*$	$V_{\text{DD}} = 4.5 \text{ to } 6.0 \text{ V}$			300	ns
						1000	ns

\*  $R_{\text{L}}$  and  $C_{\text{L}}$  are SO output line load resistance and load capacitance, respectively.

**SBI mode ( $\overline{\text{SCK}}$ ...Internal clock output (master))**

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
$\overline{\text{SCK}}$ cycle time	t <sub>KCY3</sub>	V <sub>DD</sub> = 4.5 to 6.0 V		1600			ns
				3800			ns
$\overline{\text{SCK}}$ high and low level widths	t <sub>KL3</sub>	V <sub>DD</sub> = 4.5 to 6.0 V		t <sub>KCY3</sub> /2-50			ns
	t <sub>KH3</sub>			t <sub>KCY3</sub> /2-150			ns
SB0 and SB1 setup time (to $\overline{\text{SCK}}\uparrow$ )	t <sub>SIK3</sub>			150			ns
SB0 and SB1 holdtime (from $\overline{\text{SCK}}\uparrow$ )	t <sub>KSI3</sub>			t <sub>KCY3</sub> /2			ns
SB0 and SB1 output delay time from $\overline{\text{SCK}}\downarrow$	t <sub>KSO3</sub>	R <sub>L</sub> = 1 k Ω, C <sub>L</sub> = 100 pF*	V <sub>DD</sub> = 4.5 to 6.0 V	0		250	ns
				0		1000	ns
SB0, SB1↓ from $\overline{\text{SCK}}\uparrow$	t <sub>KSB</sub>			t <sub>KCY3</sub>			ns
$\overline{\text{SCK}}$ from SB0, SB1↓	t <sub>SBK</sub>			t <sub>KCY3</sub>			ns
SB0 and SB1 low-level widths	t <sub>SBL</sub>			t <sub>KCY3</sub>			ns
SB0 and SB1 high-level widths	t <sub>SBH</sub>			t <sub>KCY3</sub>			ns

\* R<sub>L</sub> and C<sub>L</sub> are SO output line load resistance and load capacitance, respectively.

**SBI mode ( $\overline{\text{SCK}}$ ...External clock input (slave))**

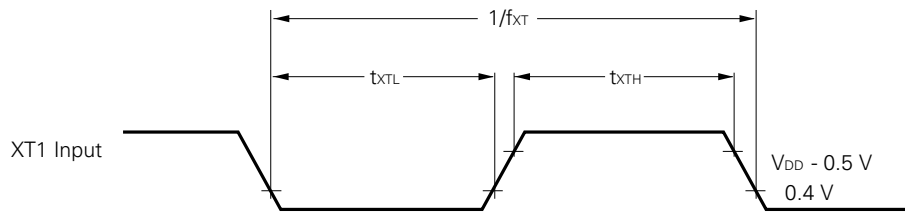
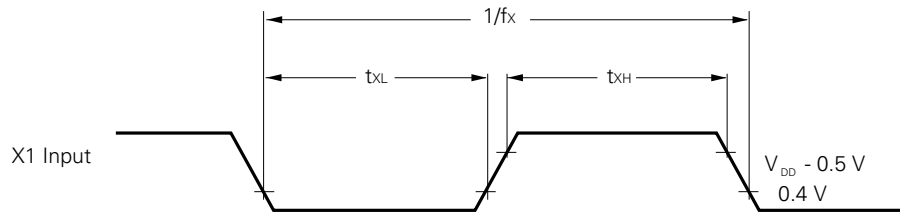
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
$\overline{\text{SCK}}$ cycle time	t <sub>KCY4</sub>	V <sub>DD</sub> = 4.5 to 6.0 V		800			ns
				3200			ns
$\overline{\text{SCK}}$ high and low level widths	t <sub>KL4</sub>	V <sub>DD</sub> = 4.5 to 6.0 V		400			ns
	t <sub>KH4</sub>			1600			ns
SB0 and SB1 setup time (to $\overline{\text{SCK}}\uparrow$ )	t <sub>SIK4</sub>			100			ns
SB0 and SB1 holdtime (from $\overline{\text{SCK}}\uparrow$ )	t <sub>KSI4</sub>			t <sub>KCY3</sub> /2			ns
SB0 and SB1 output delay time from $\overline{\text{SCK}}\downarrow$	t <sub>KSO4</sub>	R <sub>L</sub> = 1 k Ω, C <sub>L</sub> = 100 pF*	V <sub>DD</sub> = 4.5 to 6.0 V	0		300	ns
				0		1000	ns
SB0, SB1↓ from $\overline{\text{SCK}}\uparrow$	t <sub>KSB</sub>			t <sub>KCY4</sub>			ns
$\overline{\text{SCK}}$ from SB0, SB1↓	t <sub>SBK</sub>			t <sub>KCY4</sub>			ns
SB0 and SB1 low-level widths	t <sub>SBL</sub>			t <sub>KCY4</sub>			ns
SB0 and SB1 high-level widths	t <sub>SBH</sub>			t <sub>KCY4</sub>			ns

\* R<sub>L</sub> and C<sub>L</sub> are SO output line load resistance and load capacitance, respectively.

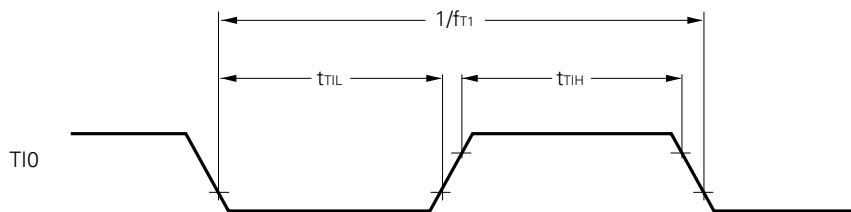
**AC Timing Test Points (Except X1 and XT1 Inputs)**



**Clock Timing**



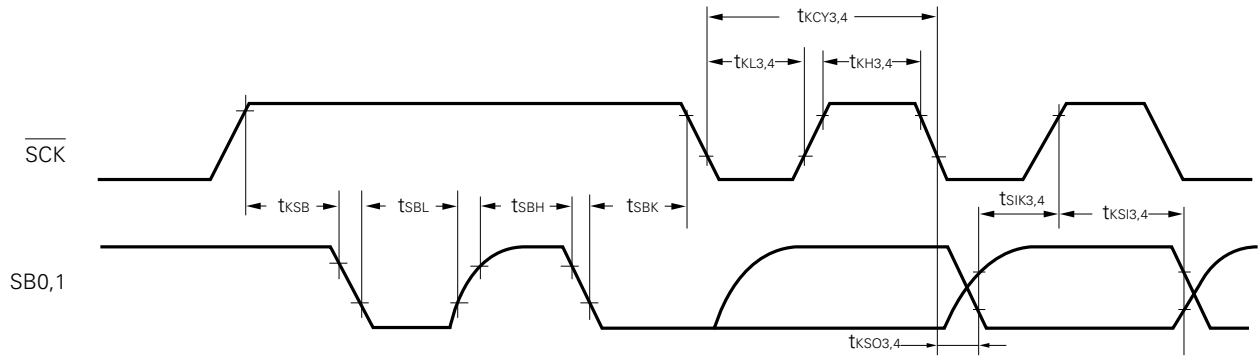
**T10 Timing**



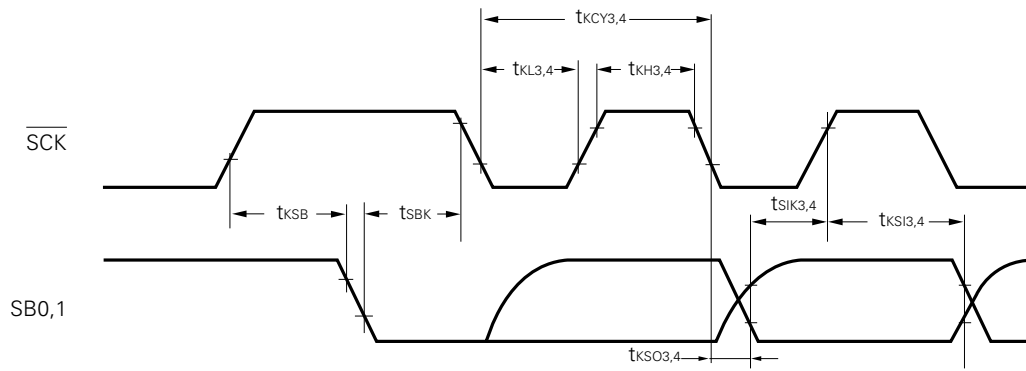


**Serial Transfer Timing**

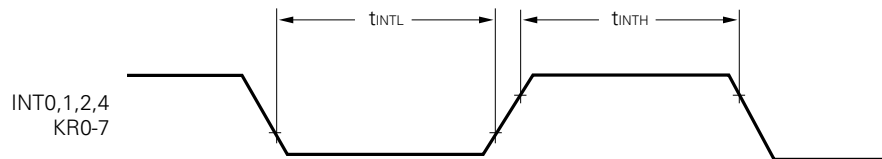
**Bus release signal transfer:**



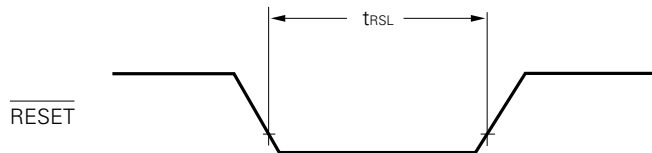
**Command signal transfer:**



**Interrupt Input Timing**



**RESET Input Timing**



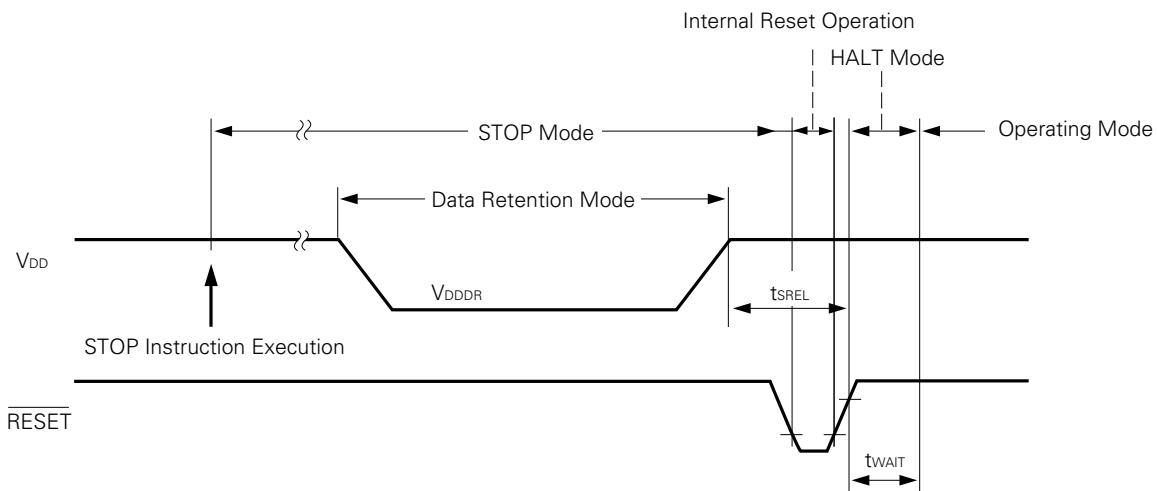
**DATA MEMORY STOP MODE LOW POWER SUPPLY VOLTAGE DATA RETENTION CHARACTERISTICS (Ta = -40 to +85 °C)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Data retention power supply voltage	V <sub>DDDR</sub>		2.0		6.0	V
Data retention power supply current *1	I <sub>DDDR</sub>	V <sub>DDDR</sub> = 2.0 V		0.1	10	μA
Release signal set time	t <sub>SREL</sub>		0			μs
Oscillation stabilization wait time *2	t <sub>WAIT</sub>	Release by $\overline{\text{RESET}}$		2 <sup>17</sup> /f <sub>x</sub>		ms
		Release by interrupt request		*3		ms

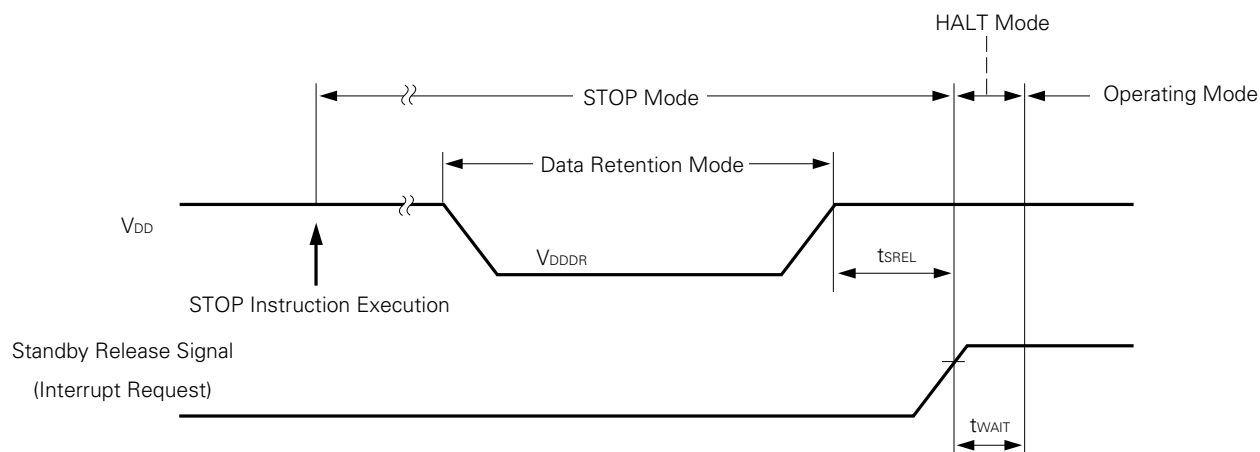
- \* 1. Current to the internal pull-up resistor is not included.
- 2. Oscillation stabilization wait time is time to stop CPU operation to prevent unstable operation upon oscillation start.
- 3. According to the setting of the basic interval timer mode register (BTM) (see below).

BTM3	BTM2	BTM1	BTM0	Wait Time (Values at f <sub>xx</sub> = 4.19 MHz in parentheses)
—	0	0	0	2 <sup>20</sup> /f <sub>xx</sub> (approx. 250 ms)
—	0	1	1	2 <sup>17</sup> /f <sub>xx</sub> (approx. 31.3 ms)
—	1	0	1	2 <sup>15</sup> /f <sub>xx</sub> (approx. 7.82 ms)
—	1	1	1	2 <sup>13</sup> /f <sub>xx</sub> (approx. 1.95 ms)

**Data Retention Timing (STOP Mode Release by  $\overline{\text{RESET}}$ )**



**Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Signal)**



**DC PROGRAMMING CHARACTERISTICS (Ta = -25 to ±5 °C, V<sub>DD</sub> = 6.0 ±0.25 V, V<sub>PP</sub> = 12.5 ±0.3 V, V<sub>SS</sub> = 0 V)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input voltage high	V <sub>IH1</sub>	Except X1, X2	0.7 V <sub>DD</sub>		V <sub>DD</sub>	V
	V <sub>IH2</sub>	X1, X2	V <sub>DD</sub> - 0.5		V <sub>DD</sub>	V
Input voltage low	V <sub>IL1</sub>	Except X1, X2	0		0.3 V <sub>DD</sub>	V
	V <sub>IL2</sub>	X1, X2	0		0.4	V
Input leakage current	I <sub>LI</sub>	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub>			10	μA
Output voltage high	V <sub>OH</sub>	I <sub>OH</sub> = -1mA	V <sub>DD</sub> - 1.0			V
Output voltage low	V <sub>OL</sub>	I <sub>OL</sub> = 1.6 mA			0.4	V
V <sub>DD</sub> power supply current	I <sub>DD</sub>				30	mA
V <sub>PP</sub> power supply current	I <sub>PP</sub>	MD0 = V <sub>IL</sub> , MD1 = V <sub>IH</sub>			30	mA

- Note**
1. V<sub>PP</sub> including overshoot should not exceed +13.5 V.
  2. V<sub>DD</sub> should be applied before V<sub>PP</sub> and should be cut after V<sub>PP</sub>.

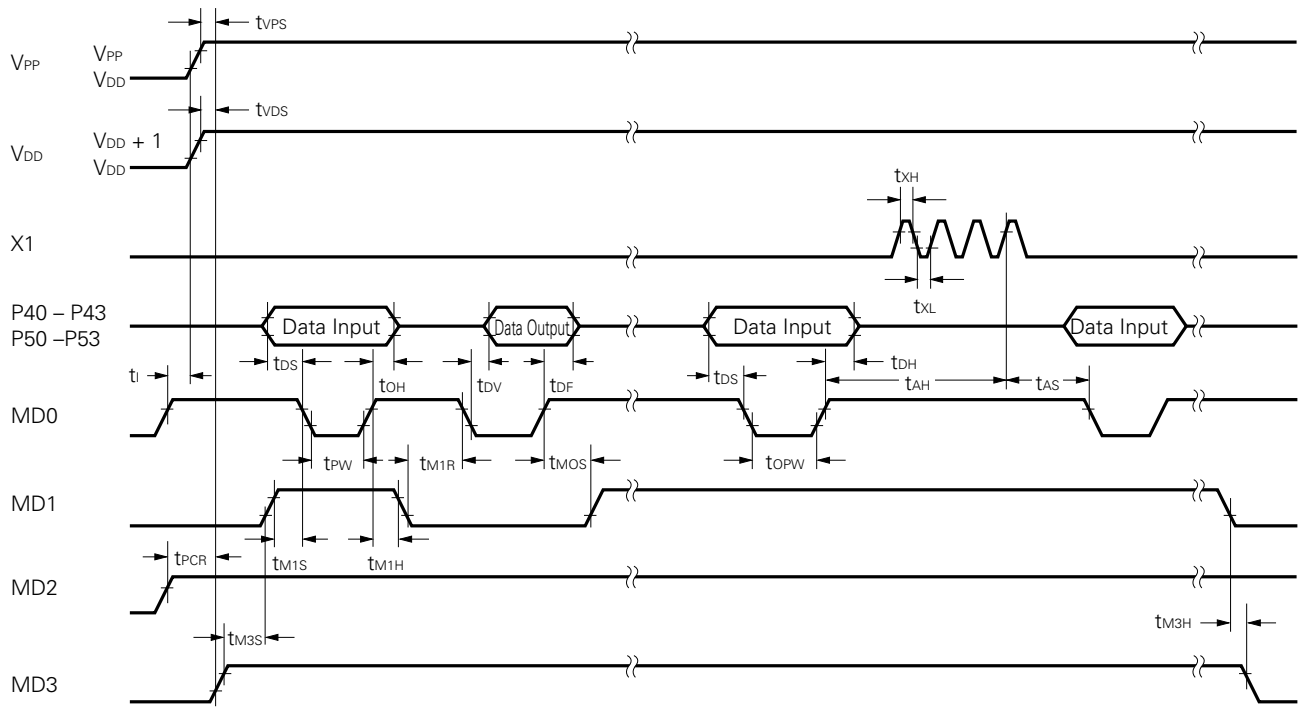


AC PROGRAMMING CHARACTERISTICS (Ta = 25 to  $\pm 5$  °C, V<sub>DD</sub> = 6.0  $\pm$ 0.25 V, V<sub>PP</sub> = 12.5  $\pm$ 0.3 V, V<sub>SS</sub> = 0 V)

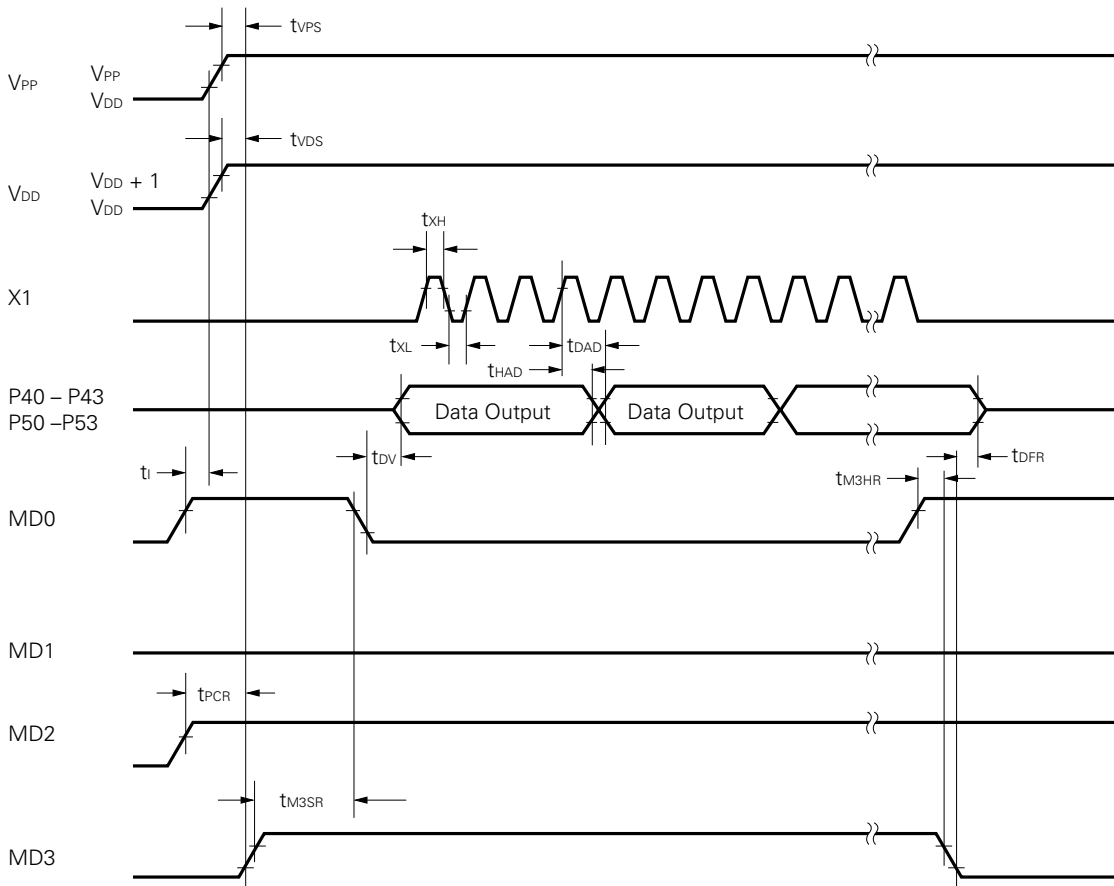
PARAMETER	SYMBOL	*1	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Address setup time*2 (to MD0 ↓)	t <sub>AS</sub>	t <sub>AS</sub>		2			$\mu$ s
MD1 setup time (to MD0 ↓)	t <sub>M1S</sub>	t <sub>OES</sub>		2			$\mu$ s
Data setup time (to MD0 ↓)	t <sub>DS</sub>	t <sub>DS</sub>		2			$\mu$ s
Address hold time*2 (from MD0 ↑)	t <sub>AH</sub>	t <sub>AH</sub>		2			$\mu$ s
Data hold time (to MD0 ↑)	t <sub>DH</sub>	t <sub>DH</sub>		2			$\mu$ s
Data output float delay time from MD0 ↑	t <sub>DF</sub>	t <sub>DF</sub>		0		130	ns
V <sub>PP</sub> setup time (to MD3 ↑)	t <sub>VPS</sub>	t <sub>VPS</sub>		2			$\mu$ s
V <sub>DD</sub> setup time (to MD3 ↑)	t <sub>VDS</sub>	t <sub>VCS</sub>		2			$\mu$ s
Initial program pulse width	t <sub>PW</sub>	t <sub>PW</sub>		0.95	1.0	1.05	ms
Additional program pulse width	t <sub>OPW</sub>	t <sub>OPW</sub>		0.95		21.0	ms
MD1 setup time (to MD1 ↑)	t <sub>MOS</sub>	t <sub>CES</sub>		2			$\mu$ s
Data output delay time from MD0 ↓	t <sub>DV</sub>	t <sub>DV</sub>	MD0 = MD1 = V <sub>IL</sub>			1	$\mu$ s
MD1 hold time (from MD0 ↑)	t <sub>M1H</sub>	t <sub>OEH</sub>	t <sub>M1H</sub> + t <sub>M1R</sub> $\geq$ 50 $\mu$ s	2			$\mu$ s
MD1 recovery time (from MD0 ↓)	t <sub>M1R</sub>	t <sub>OR</sub>		2			$\mu$ s
Program counter reset time	t <sub>PCR</sub>	–		10			$\mu$ s
X1 input high/low level width	t <sub>XH</sub> , t <sub>XL</sub>	–		0.125			$\mu$ s
X1 input frequency	f <sub>X</sub>	–				4.19	MHz
Initial mode set time	t <sub>I</sub>	–		2			$\mu$ s
MD3 setup time (to MD1 ↑)	t <sub>M3S</sub>	–		2			$\mu$ s
MD3 hold time (from MD1 ↓)	t <sub>M3H</sub>	–		2			$\mu$ s
MD3 setup time (to MD0 ↓)	t <sub>M3SR</sub>	–	When reading program memory	2			$\mu$ s
Data output delay time from address*2	t <sub>DAD</sub>	t <sub>ACC</sub>	When reading program memory			2	$\mu$ s
Data output hold time from address*2	t <sub>HAD</sub>	t <sub>OH</sub>	When reading program memory	0		130	ns
MD3 hold time (from MD0 ↑)	t <sub>M3HR</sub>	–	When reading program memory	2			$\mu$ s
Data output float delay time from MD3 ↓	t <sub>DFR</sub>	–	When reading program memory			2	$\mu$ s

- \* 1. Symbol of the corresponding  $\mu$ PD27C256A.  
 2. The internal address signal is incremented (+1) at the rising edge of the fourth X1 input. The signal is not connected to pins.

**Program Memory Write Timing**

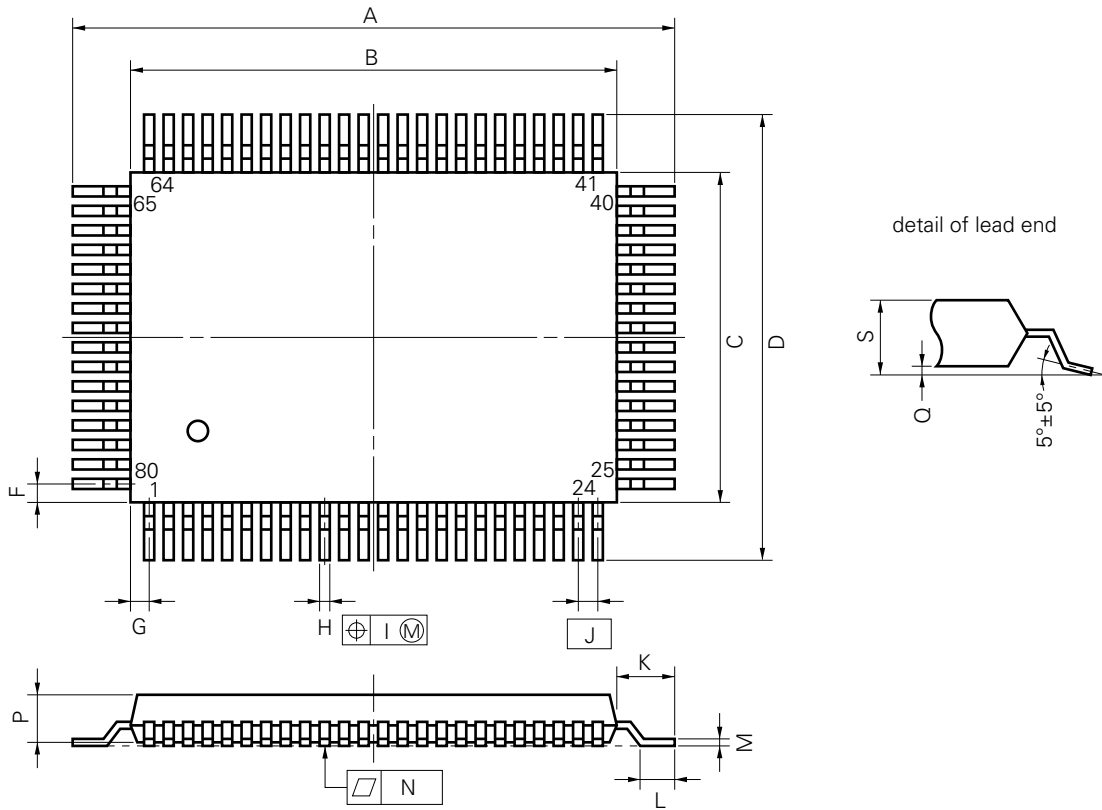


**Program Memory Read Timing**



6. PACKAGE INFORMATION

80 PIN PLASTIC QFP (14×20)



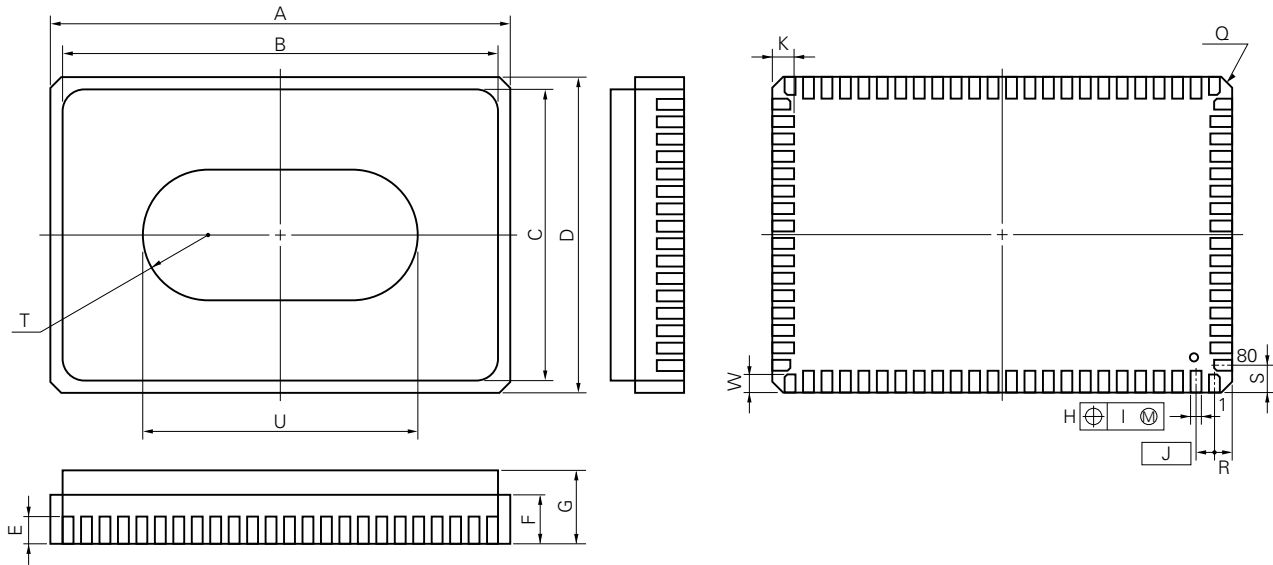
NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

P80GF-80-3B9-2

ITEM	MILLIMETERS	INCHES
A	23.6±0.4	0.929±0.016
B	20.0±0.2	0.795 <sup>+0.009</sup> <sub>-0.008</sub>
C	14.0±0.2	0.551 <sup>+0.009</sup> <sub>-0.008</sub>
D	17.6±0.4	0.693±0.016
F	1.0	0.039
G	0.8	0.031
H	0.35±0.10	0.014 <sup>+0.004</sup> <sub>-0.005</sub>
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	1.8±0.2	0.071 <sup>+0.008</sup> <sub>-0.009</sub>
L	0.8±0.2	0.031 <sup>+0.009</sup> <sub>-0.008</sub>
M	0.15 <sup>+0.10</sup> <sub>-0.05</sub>	0.006 <sup>+0.004</sup> <sub>-0.003</sub>
N	0.15	0.006
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
S	3.0 MAX.	0.119 MAX.

80 PIN CERAMIC WQFN



**NOTE**

Each lead centerline is located within 0.08 mm (0.003 inch) of its true position (T.P.) at maximum material condition.

X80KW-80A-1

ITEM	MILLIMETERS	INCHES
A	20.0±0.4	0.787 <sup>+0.017</sup> <sub>-0.016</sub>
B	19.0	0.748
C	13.2	0.520
D	14.2±0.4	0.559±0.016
E	1.64	0.065
F	2.14	0.084
G	4.064 MAX.	0.160 MAX.
H	0.51±0.10	0.020±0.004
I	0.08	0.003
J	0.8 (T.P.)	0.031 (T.P.)
K	1.0±0.2	0.039 <sup>+0.009</sup> <sub>-0.008</sub>
Q	C 0.5	C 0.020
R	0.8	0.031
S	1.1	0.043
T	R 3.0	R 0.118
U	12.0	0.472
W	0.75±0.2	0.030 <sup>+0.008</sup> <sub>-0.009</sub>

**7. RECOMMENDED SOLDERING CONDITIONS**

The μPD75P316A should be soldered and mounted under the conditions recommended in the table below.

For detail of recommended soldering conditions, refer to the information document “**Semiconductor Device Mount Manual**” (IEI-1207).

For soldering methods and conditions other than those recommended below, contact our salesman.

**Table 7-1 Surface Mounting Type Soldering Conditions**

**μPD75P316AGF-3B9 : 80-pin plastic QFP (14 × 20 mm)**

Solderring Method	Solderring Conditions	Recommended Condition Symbol
Wave soldering	Solder bath temperature: 260 °C or below. , Duration: 10 sec. max. Number of times: Once, Time limit: 7 days*(thereafter 20 hours prebaking required at 125 °C)	WS60-207-1
Infrared reflow	Package peak temperature: 230 °C, Duration: 30 sec. max. (at 210 °C or above), Number of times: Once, Time limit: 7 days*(thereafter 20 hours prebaking required at 125 °C)	IR30-207-1
VPS	Package peak temperature: 215 °C, Duration: 40 sec. max. (at 200 °C or above), Number of times: Once, Time limit: 7 days*(thereafter 20 hours prebaking required at 125 °C)	VP15-207-1
Pin part heating	Pin part temperature: 300 °C or below , Duration: 3 sec. max. (per device side)	—

\* For the storage period after dry-pack decapsulation, storage conditions are max. 25 °C, 65 % RH.

**Note Use more than one soldering method should be avoided (except in the case of pin part heating).**

**For Your Information**

**Products to improve the recommended soldering conditions are available.**

**(Improvements : Extension of the infrared reflow peak temperature to 235 °C, doubled frequency, increased life, etc.)**

**For further details, consult our sales personnel.**

**APPENDIX A. DEVELOPMENT TOOLS**

The following development tools are available for system development using the μPD75P316A.

Hardware	IE-75000-R*1 IE-75001-R	In-circuit emulator for use with the 75X series
	IE-75000-R-EM*2	Emulation board for use with the IE-75000-R and the IE-75001-R
	EP-75308GF-R EV-9200G-80	Emulation probe for use with the μPD75P308GF 80-pin conversion socket EV-9200G-80 included
	PG-1500	PROM programmer
	PA-75P308GF	Connect to PG-1500 with PROM programmer adapter for use with the μPD75P308GF
	PA-75P308K	Connect to PG-1500 with PROM programmer adapter for use with the μPD75P308K
	Software	IE-control program
PG-1500 controller		
RA75X relocatable assembler		

- \* 1. Maintenance product  
 2. Not a built-in component in the IE-75001-R  
 3. Ver. 5.00/5.00A has a task swaping function, which cannot be used with this software.

**Remarks** Refer to the **75X Series Selection Guide (IF-151)** for third-party development tools.

**APPENDIX B. RELATED DOCUMENTS**

**Device Related Documents**

Document Name	Document Number
User's Manual	IEM-5016
Instruction Application Table	IEM-994
75X Series Selection Guide	IF-151

**Development Tools Documents**

Document Name		Document Number	
Hardware	IE-75000-R/IE-75001-R User's Manual	EEU-846	
	IE-75000-R-EM User's Manual	EEU-673	
	EP-75308GF-R User's Manual	EEU-689	
	PG-1500 User's Manual	EEU-651	
Software	RA75X Assembler Package User's Manual	Operation Volume	EEU-731
		Language Volume	EEU-730
	PG-1500 Controller User's Manual	EEU-704	

**Other Documents**

Document Name	Document Number
Package Manual	IEI-635
Surface Mount Technology Manual	IEI-1207
Quality Grade on NEC Semiconductor Devices	IEI-1209
NEC Semiconductor Device Reliability & Quality Control	IEM-5068
Electrostatic Discharge (ESD) Test	MEM-539
Semiconductor Devices Quality Guide Guarantee Guide	MEI-603
Microcomputer Related Products Guide Other Other Manufacturers Volume	MEI-604

**Note** The information in these related documents is subject to change without notice. For design purpose, etc., check if your documents are the latest ones and be sure to use the latest ones.







[MEMO]

No part of this document may be copied or reproduced in any form or by any means without the prior written consent of NEC Corporation. NEC Corporation assumes no responsibility for any errors which may appear in this document.

NEC Corporation does not assume any liability for infringement of patents, copyrights or other intellectual property rights of third parties by or arising from use of a device described herein or any other liability arising from use of such device. No license, either express, implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of NEC Corporation or others.

The devices listed in this document are not suitable for use in aerospace equipment, submarine cables, nuclear reactor control systems and life support systems. If customers intend to use NEC devices for above applications or they intend to use "Standard" quality grade NEC devices for applications not intended by NEC, please contact our sales people in advance.

Application examples recommended by NEC Corporation

Standard : Computer, Office equipment, Communication equipment, Test and Measurement equipment, Machine tools, Industrial robots, Audio and Visual equipment, Other consumer products, etc.

Special : Automotive and Transportation equipment, Traffic control systems, Antidisaster systems, Anticrime systems, etc.

M4 92.6

MS-DOS is a trademark of MicroSoft Corporation.

PC DOS and PC/AT are trademarks of IBM Corporation.

This datasheet has been downloaded from:

[www.DatasheetCatalog.com](http://www.DatasheetCatalog.com)

Datasheets for electronic components.