Analog Reinvented

ES9312
Dual Ultra Low Noise Regulator
Product Datasheet

The ES9312 is a 2nd generation dual ultra low noise linear regulator optimized to supply the reference voltages for ESS Technology's SABRE® products as well as maximize all DAC and ADC performance.

Each regulator's output noise, as low as 1µVrms from 10Hz to 100kHz, allows for the highest achievable dynamic range and lowest noise performance making it the ideal low noise regulator for use with all ESS SABRE® DACs and ADCs as well as general very low noise voltage requirements.

The ES9312Q provides several unique features not available in standard regulators. Incorporating the ability for self-calibration when paired with selected ESS DACs to help maintain constant output levels. Internal fixed mode that supports +1.2V/+1.8V/+3.3V/+4.5V presets to help simplify device configuration for standard voltages. External fixed mode which allows for output adjustment to a flexible reference voltage.

As an example, the ES9312Q enables ESS Technology's DACs to achieve up to +140dB DNR and THD+N of -122dB with the ES9039PRO and allows for various voltage outputs to be configured through a simple pin configuration.

The ES9312Q is available in a small 16-pin, 3mm x 3mm QFN package providing a cost effective solution.

FEATURE	DESCRIPTION
Ultra low noise regulated to 180mA per output at multiple voltage levels	Excellent line and load regulation for output current to maintain peak performance
1µVrms output noise (10Hz to 100kHz)	Excellent performance to maintain highest DNR and THD+N measurements
Over-current, under-voltage, over-temperature warning and protection	Protection for regulator and device against system issues
Calibration mode for Sabre DACs	Allows adjustment of output voltage to ensure output levels are maintained in selected ESS DACs such as the ES9069, ES9039Q2M and others
Internal voltage fixed mode presets	Fixed mode allows for simple pin configuration for 1.2/1.8/3.3/4.5V output
External fixed mode	Both regulator voltages are configurable with external resistors
Dual regulators in one package	Reducing BOM requirements and setup
Operating supply	Supply voltage of +5V
Low pin count packaging	3mm x 3mm, 16 pin QFN, minimizing PCB footprint and board space

APPLICATIONS

- ESS SABRE DAC Supply in Calibration Mode with Calibration Resistor
- General Ultra-Low Noise Supply for DACs and ADCs

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ES9312 Pinout[1]

16 QFN Pinout

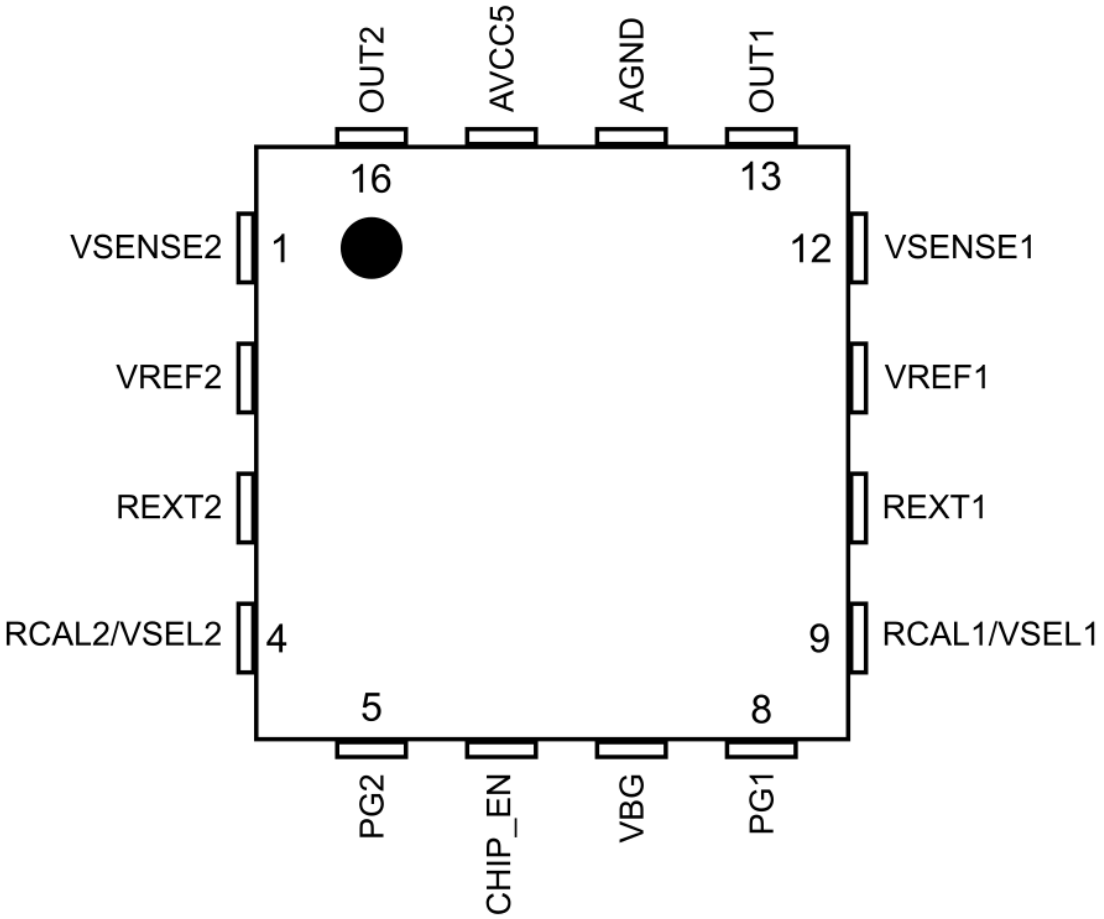


Figure 1 - 16 QFN Pinout

[1] Pin 17 is a package pad, used for heat dissipation and is not electrically connected.

16 QFN Pin Descriptions

Pin	Name	Pin Type	Pin Description
1	VSENSE2	AI	Voltage sense point for regulator 2, feedback to amplifier input
2	VREF2	AO	Voltage reference for regulator 2
3	REXT2	AI	External resistor for setting output voltage for regulator 2 when using calibration mode
4	RCAL2	AI	Calibration resistor for regulator 2
	VSEL2		Internal voltage selector for regulator 2
5	PG2	AO	"**P**ower **G**ood" indicator, open drain output for regulator 2
6	CHIP_EN	AI	Chip enable
7	VBG	AO	Internal bandgap voltage reference, no connect
8	PG1	AO	"**P**ower **G**ood" indicator, open drain output for regulator 1
9	RCAL1	AI	Calibration resistor for regulator 1
	VSEL1		Internal voltage selector for regulator 1
10	REXT1	AI	External resistor to set output voltage for regulator 1 in calibration mode
11	VREF1	AO	Voltage reference for regulator 1
12	VSENSE1	AI	Voltage sense point for regulator 1, feedback to amplifier input
13	OUT1	AO	Output (Force) voltage for regulator 1
14	AGND	Ground	Ground
15	AVCC5	Power	Power
16	OUT2	AO	Output (Force) voltage for regulator 2
17*	Package Pad	-	Package PAD, used for thermal dissipation

Table 1 - 16 QFN Pin Descriptions

* Note: Pin 17 is the package pad and should be connected to AGND, AO = Analog Output, AI = Analog Input

Functional Block Diagram

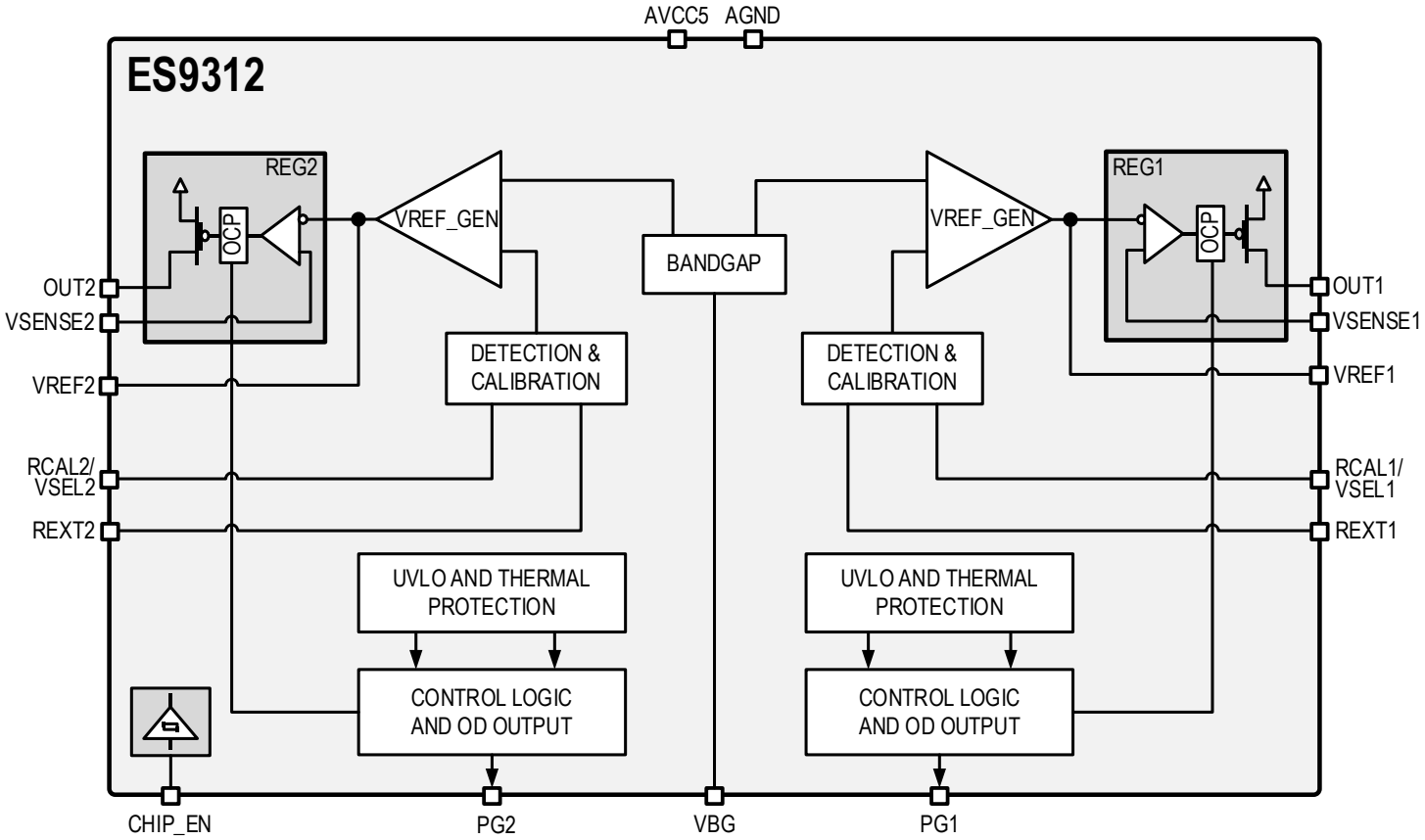


Figure 2 - Functional Block Diagram

Note: See Reference Schematics for connection diagrams.

Functional Description

The ES9312 is a dual output ultra-low noise regulator for powering noise sensitive applications. The ES9312 features multiple voltage output modes making it the perfect companion for ESS DACs or ADCs. The dual regulator features overcurrent, undervoltage, overtemperature warnings as well as overtemperature shutdown. The ES9312 can output up to 180mA per channel at preset settings of 1.2V/1.8V/3.3V and can output up to 100mA at 4.5V.

The ES9312's dual outputs can operate in any of three modes: Internal Fixed Voltage Mode for using the preset voltage output, External Fixed Voltage Mode for adjusting the output voltage using a combination of two resistors connected to RCALx/VSELx and REXTx, and Calibration Mode for using with compatible ESS DACs.

Internal Fixed Voltage Mode

The ES9312 has internal fixed voltage modes that can output 4.5V, 3.3V, 1.8V, and 1.2V per channel, using the voltage select pin (VSEL), pins 4 and 9. To enable the functionality of the VSEL pin, the corresponding REXT pin must be floating. The VSEL pin is then set to 4 possible different states to determine the channels output voltage. When using both channels in internal fixed voltage mode, independent resistors must be used per VSEL pin.

REXT	VSEL1/2 Setting	VSEL1/2 Resistor (Ω)	Vout (V)
Floating (NC)	Tie High	47 to AVCC	4.5[2]
	Pull High	47k to AVCC	3.3
	Pull Low	47k to GND	1.8
	Tie Low	47 to GND	1.2

Table 2 - Preset Voltage Mode Settings

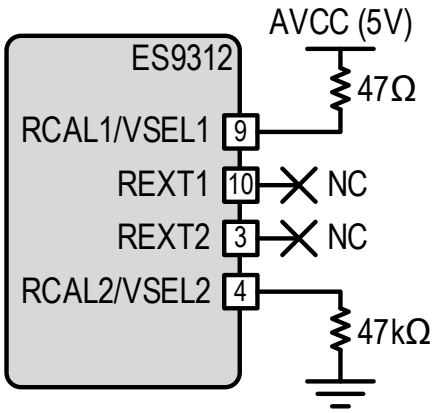


Figure 3 - Example of Fixed Voltage Mode for 4.5V (CH1) and 1.8V (CH2)

[2] For Internal Fixed 4.5V Mode, V_{IN} must not go below 5V

External Fixed Voltage Mode

The External Fixed Voltage Mode is intended to configure the ES9312 to output any voltage within the range of 1.2V to 4.5V. This can be done by applying a ratio of resistance on the RCAL and REXT pins according to the following equation.

$$V_{out} = 2.57 * \frac{R_{sel}}{R_{ext}}$$

Equation 1 - External Fixed Voltage Mode Equation

	R_{ext} [Ω]	R_{sel} [Ω]
MIN	21k	10.3k
MAX	1M	2 x R_{ext}

Table 3 - External Fixed Resistor Limits

The resistors used should be of the 0.1% tolerance variety to ensure an accurate voltage output.

Example for setting a 4.5V output:

$$V_{out} = 2.57 * \frac{R_{sel}}{R_{ext}} \rightarrow V_{out} = 2.57 * \frac{46.4k}{26.5k} \cong 4.499V$$

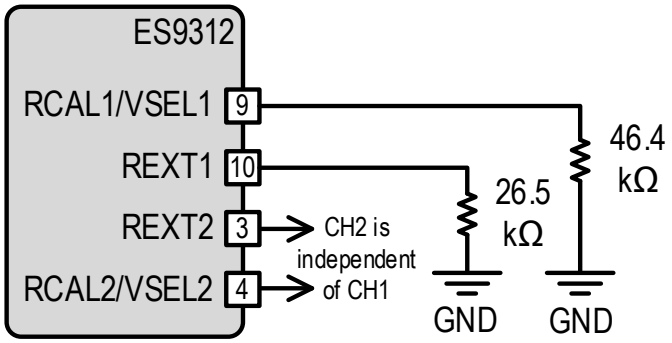


Figure 4 - Example External Fixed Voltage Mode for 4.5V Circuit

Calibration Mode

The Calibration Mode is designed to be paired with compatible ESS devices using their integrated calibration resistor. The calibration resistor pin on the ESS device will be located on one of its GPIOs, for this information please see the respective devices datasheet. This calibration resistor must be connected to the RCAL1/2 pin on the ES9312. Then an external resistor (R_{ext}) is connected from the REXT1/2 pin to ground. The resistance of R_{ext} will depend on the calibration resistor value.

ESS Part Number	Calibration Resistor Value [Ω]	R_{ext} Value [Ω]	V_{OUT} [V]
ES9039PRO	50k	37k	3.3
ES9069	50k	37k	
ES9039Q2M	50k	37k	
ES9027PRO	50k	37k	
ES9017	100k	74k	

Table 4 - ESS Calibration Resistor Compatible Devices

The resistors used for R_{ext} should be 0.1% tolerance to ensure an accurate voltage output.

The ES9312 can have one output in calibration mode and the other output set for fixed mode, or it can have both outputs set in calibration mode. This is controlled through the REXT and RCAL pins.

Note: R_{ext} MUST double when combining both RCAL1 and RCAL2 together using a single calibration resistor.

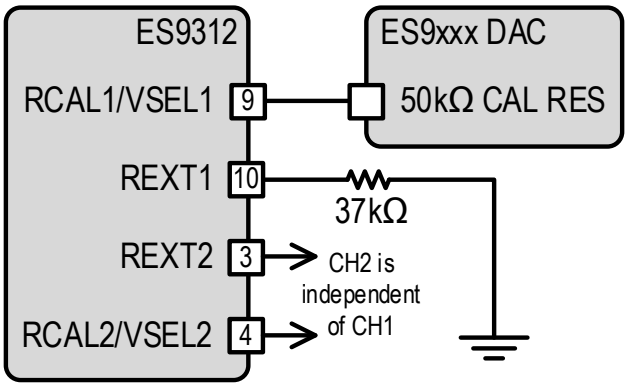


Figure 5 - Example of Calibration Mode with Independent Calibration Resistor

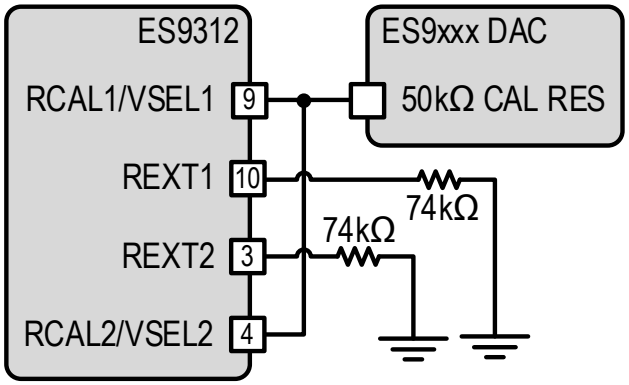


Figure 6 - Example of Calibration Mode with Combined Calibration Resistor

See Simplified Application Diagram with ES9039Q2M for supplying an ESS DAC with calibration resistor with ES9312.

Power Good (PG) Pins

The ES9312 includes two "power good" pins (PG1 and PG2), one for each output. The PG pins (Pins 5 and 8) are open-drain outputs during normal operation and will be pulled low through a 2kΩ or 10kΩ resistor depending on which flag is set. To measure the voltage output, the pin must be pulled high through an external resistor (R_{PG_EXT}) to chosen external voltage supply ($AVCC_{PG}$). The voltage is then measured from the pin to ground as seen in the below figure. The two voltages can also be calculated using the below equation. If the PG error/warnings are not required, PG1 & PG2 can be no connects.

Flag State	Internal Resistance (R_{PG_INT})
Normal Operation	OPEN
Warning	10kΩ
Error	1.7kΩ

Table 5 - Power Good (PG) Pin States

$$AVCC_{PG} \leq 4V$$

$$V_{PG} = AVCC_{PG} * \left(\frac{R_{PG\_INT}}{R_{PG\_INT} + R_{PG\_EXT}} \right)$$

Equation 2 - Power Good (PG) Voltage Equation

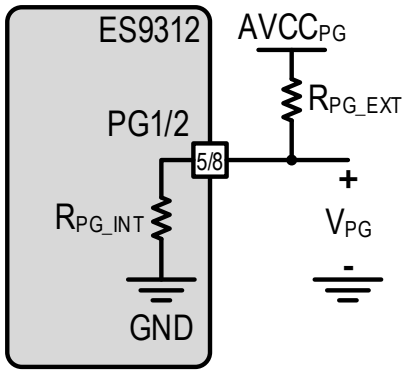


Figure 7 - Power Good (PG) Pin Voltage Divider

Note: When the chip is shutdown (CHIP_EN=LOW), the PG pins will always output the "error" flag.

Overcurrent

The ES9312 features overcurrent detection and limiting, where the corresponding PG pin will output a flag and will, at high currents, implement a current limit depending on the current value.

Mode	Current	Hysteresis	PG Flag	Conditions
1.2V	140mA	16mA	Warning	-
1.8V	140mA	7mA	Warning	-
3.3V	140mA	7mA	Warning	-
4.5V	105mA	3mA	Warning	-
All	200mA	-	Warning	Current Limit

Table 6 - Overcurrent Flags

Undervoltage

The ES9312 features undervoltage detection, where the corresponding PG pin will output a flag depending on the supply voltage.

Mode	Flag Voltage	PG Flag
1.2V 1.8V 3.3V	3.6V	Warning ON
	4.4V	Warning OFF
4.5V	4.5V	Warning ON and OFF

Table 7 - Under Voltage Flags

Overtemperature

The ES9312 features overtemperature protection. The regulator will output two different flags depending on what temperature region the chip is in. Once reaching a specific threshold, the regulator will shut itself off until the chip cools sufficiently past the hysteresis point.

Mode	Temperature	Hysteresis	PG Flag	Conditions
All	105ºC	25ºC	Warning	-
	155ºC	35ºC	Error	Chip Shutdown

Table 8 - Overtemperature flags with 50mA load

Analog Performance

Note: All measurements are taken with both regulators operational.

1.2V

Test Conditions (unless otherwise noted)
V_{IN} = 5V, T_A = 25ºC, C_{AVCC} = 1µF, C_{OUT} = 1µF, C_{VREF} = 4.7µF, C_{CHIP_EN} = 1 µF, Mode = Internal Fixed 1.2V

Parameter	Symbol	Conditions	MIN	TYP	MAX	UNIT
Supply						
Input Voltage Range	V_{IN}			5		V
Quiescent Current	I_Q	I_{Load} = 0mA		6.8		mA
Shutdown Current	I_{SD}	CHIP_EN = GND		8		µA
Chip Enable Threshold High	VTH_{CHIP_EN}			1.55		V
Chip Enable Threshold Low	VTL_{CHIP_EN}			1.05		V
Power Supply Rejection	PSR	20Hz to 20kHz, I_{Load} = 10mA		80		dB
Noise						
Output Noise	en	10Hz to 100kHz, C_{VREF} = 10µF		1.03		µVrms
Noise Spectral Density	en	10kHz Spot Noise, C_{VREF} = 10µF		4		nV/√Hz
Output						
Output Voltage	V_{OUT}	I_{Load} = 50mA, T_A = +25ºC		1.23		V
Load Current *	I_{Load}	Maximum output for each supply		180		mA
Short-circuit current	I_{SC}	Per Regulator Output		200		mA
Rise Time from Enable	T_{SU}	I_{Load} = Open Circuit		18		µs
		I_{Load} = 20mA		20		µs
		I_{Load} = 145mA		32		µs
Regulation						
Load Regulation	$\Delta V_{OUT}/\Delta I_{OUT}$	I_{Load} = 1mA to 100mA		4		mV/A
		I_{Load} = 1mA to 180mA		6		mV/A
Thermal Protection						
Over-Temperature Warning	OTW	I_{Load} = 50mA		105		ºC
Hysteresis	OTW_{HYS}			25		ºC
Over-Temperature Shutdown	OTS			155		ºC
Hysteresis	OTS_{HYS}			35		ºC
Current Protections						
Over-Current Warning	OCW	T_A = +25ºC		140		mA
Hysteresis	OCW_{HYS}			16		mA
Over-Current Limit	OCL			200		mA
Under-Voltage Warning						
VIN Rising	UVW			4.4		V
VIN Falling				3.6		V

Table 9 - Preset 1.2V Analog Performance

* Note: OCW (Overcurrent Warning) will be set before the maximum supply current is reached (140mA)

1.8V

Test Conditions (unless otherwise noted)
V_{IN} = 5V, T_A = 25ºC, C_{AVCC} = 1µF, C_{OUT} = 1µF, C_{VREF} = 4.7µF, C_{CHIP_EN} = 1 µF, Mode = Internal Fixed 1.8V

Parameter	Symbol	Conditions	MIN	TYP	MAX	UNIT
Supply						
Input Voltage Range	V_{IN}			5		V
Quiescent Current	I_Q	I_{Load} = 0mA		6.9		mA
Shutdown Current	I_{SD}	CHIP_EN = GND		8		µA
Chip Enable Threshold High	VTH_{CHIP_EN}			1.55		V
Chip Enable Threshold Low	VTL_{CHIP_EN}			1.05		V
Power Supply Rejection	PSR	20Hz to 20kHz, I_{Load} = 10mA		80		dB
Noise						
Output Noise	en	10Hz to 100kHz, C_{VREF} = 10µF		1.04		µVrms
Noise Spectral Density	en	10kHz Spot Noise, C_{VREF} = 10µF		4		nV/√Hz
Output						
Output Voltage	V_{OUT}	I_{Load} = 50mA, T_A = +25ºC		1.85		V
Load Current *	I_{Load}	Maximum output for each supply		180		mA
Short-circuit current	I_{SC}	Per Regulator Output		200		mA
Rise Time from Enable	T_{SU}	I_{Load} = Open Circuit		28		µs
		I_{Load} = 20mA		30		µs
		I_{Load} = 145mA		50		µs
Regulation						
Load Regulation	$\Delta V_{OUT}/\Delta I_{OUT}$	I_{Load} = 1mA to 100mA		5		mV/A
		I_{Load} = 1mA to 180mA		6		mV/A
Thermal Protection						
Over-Temperature Warning	OTW	I_{Load} = 50mA		105		ºC
Hysteresis	OTW_{HYS}			25		ºC
Over-Temperature Shutdown	OTS			155		ºC
Hysteresis	OTS_{HYS}			35		ºC
Current Protections						
Over-Current Warning	OCW	T_A = +25ºC		140		mA
Hysteresis	OCW_{HYS}			7		mA
Over-Current Limit	OCL			200		mA
Under-Voltage Warning						
VIN Rising	UVW			4.4		V
VIN Falling				3.6		V

Table 10 - Preset 1.8V Analog Performance

* Note: OCW (Overcurrent Warning) will be set before the maximum supply current is reached (140mA)

3.3V

Test Conditions (unless otherwise noted)
V_{IN} = 5V, T_A = 25ºC, C_{AVCC} = 1µF, C_{OUT} = 1µF, C_{VREF} = 4.7µF, C_{CHIP_EN} = 1 µF, Mode = Internal Fixed 3.3V

Parameter	Symbol	Conditions	MIN	TYP	MAX	UNIT
Supply						
Input Voltage Range	V_{IN}			5		V
Quiescent Current	I_Q	I_{Load} = 0mA		6.9		mA
Shutdown Current	I_{SD}	CHIP_EN = GND		8		µA
Chip Enable Threshold High	VTH_{CHIP_EN}			1.55		V
Chip Enable Threshold Low	VTL_{CHIP_EN}			1.05		V
Power Supply Rejection	PSR	20Hz to 20kHz, I_{Load} = 10mA		80		dB
Noise						
Output Noise	en	10Hz to 100kHz, C_{VREF} = 10µF		1.06		µVrms
Noise Spectral Density	en	10kHz Spot Noise, C_{VREF} = 10µF		4		nV/√Hz
Output						
Output Voltage	V_{OUT}	I_{Load} = 50mA, T_A = +25ºC		3.38		V
Load Current *	I_{Load}	Maximum output for each supply		180		mA
Short-circuit current	I_{SC}	Per Regulator Output		200		mA
Rise Time from Enable	T_{SU}	I_{Load} = Open Circuit		72		µs
		I_{Load} = 20mA		72		µs
		I_{Load} = 145mA		88		µs
Regulation						
Load Regulation	$\Delta V_{OUT}/\Delta I_{OUT}$	I_{Load} = 1mA to 100mA		5		mV/A
		I_{Load} = 1mA to 180mA		7		mV/A
Thermal Protection						
Over-Temperature Warning	OTW	I_{Load} = 50mA		105		ºC
Hysteresis	OTW_{HYS}			25		ºC
Over-Temperature Shutdown	OTS			155		ºC
Hysteresis	OTS_{HYS}			35		ºC
Current Protections						
Over-Current Warning	OCW	T_A = +25ºC		140		mA
Hysteresis	OCW_{HYS}			7		mA
Over-Current Limit	OCL			200		mA
Under-Voltage Warning						
VIN Rising	UVW			4.4		V
VIN Falling				3.6		V

Table 11 - Preset 3.3V Analog Performance

* Note: OCW (Overcurrent Warning) will be set before the maximum supply current is reached (140mA)

4.5V

Test Conditions (unless otherwise noted)
V_{IN} = 5V, T_A = 25ºC, C_{AVCC} = 1µF, C_{OUT} = 1µF, C_{VREF} = 4.7µF, C_{CHIP_EN} = 1 µF, Mode = Internal Fixed 4.5V

Parameter	Symbol	Conditions	MIN	TYP	MAX	UNIT
Supply						
Input Voltage Range	V_{IN}			5		V
Quiescent Current	I_Q	I_{Load} = 0mA		6.8		mA
Shutdown Current	I_{SD}	CHIP_EN = GND		8		µA
Chip Enable Threshold High	VTH_{CHIP_EN}			1.55		V
Chip Enable Threshold Low	VTL_{CHIP_EN}			1.05		V
Power Supply Rejection	PSR	20Hz to 20kHz, I_{Load} = 10mA		80		dB
Noise						
Output Noise	en	10Hz to 100kHz, C_{VREF} = 10µF		1.1		µVrms
Noise Spectral Density	en	10kHz Spot Noise, C_{VREF} = 10µF		4		nV/√Hz
Output						
Output Voltage	V_{OUT}	I_{Load} = 50mA, T_A = +25ºC		4.59		V
Load Current *	I_{Load}	Maximum output for each supply		100		mA
Short-circuit current	I_{SC}	Per Regulator Output		200		mA
Rise Time from Enable	T_{SU}	I_{Load} = Open Circuit		130		µs
		I_{Load} = 20mA		131		µs
		I_{Load} = 145mA		140		µs
Regulation						
Load Regulation	$\Delta V_{OUT}/\Delta I_{OUT}$	I_{Load} = 1mA to 100mA		6		mV/A
Thermal Protection						
Over-Temperature Warning	OTW	I_{Load} = 50mA		105		ºC
Hysteresis	OTW_{HYS}			25		ºC
Over-Temperature Shutdown	OTS			155		ºC
Hysteresis	OTS_{HYS}			35		ºC
Current Protections						
Over-Current Warning	OCW	T_A = +25ºC		105		mA
Hysteresis	OCW_{HYS}			3		mA
Over-Current Limit	OCL			200		mA
Under-Voltage Warning						
VIN Rising	UVW			4.5		V
VIN Falling				4.5		V

Table 12 - Preset 4.5V Analog Performance

* Note: OCW (Overcurrent Warning) will be set before the maximum supply current is reached (105mA)

Performance Characteristics

Figure 8 - Chip Enable Hysteresis[3]

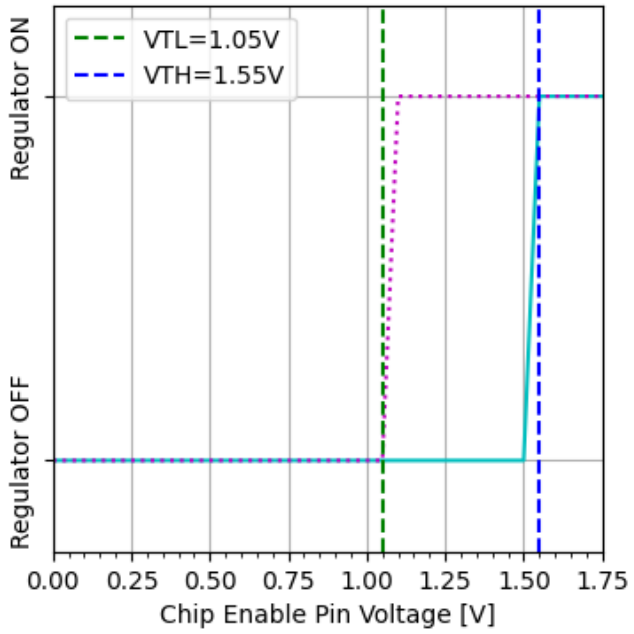


Figure 9 - Ground Current

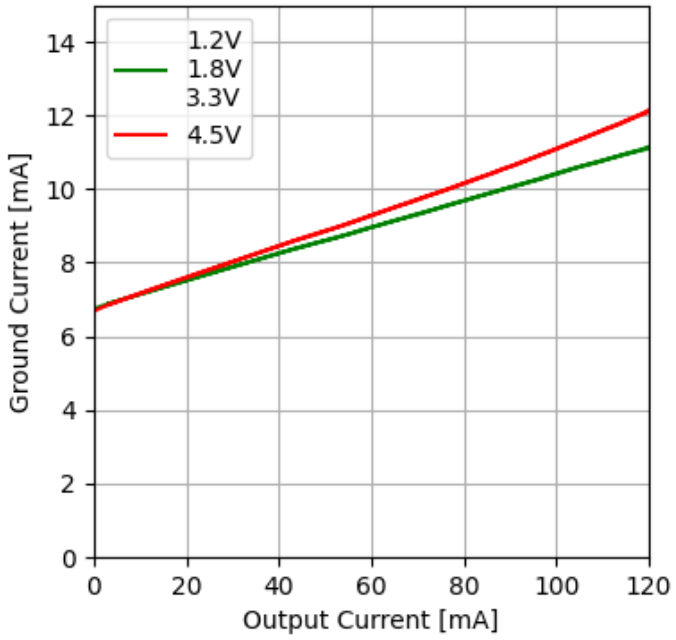


Figure 10 - Noise Spectral Density[4]

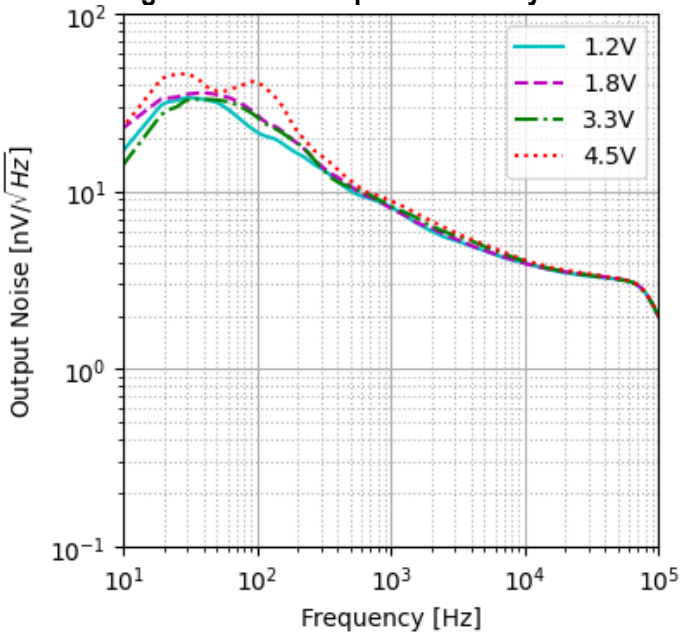
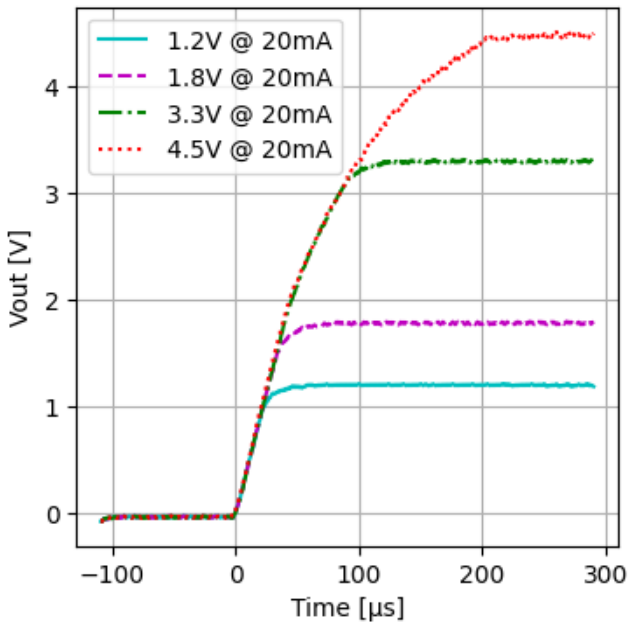


Figure 11 - Start-up Time from CHIP_EN[5]



[3] 25ºC

[4] 10Hz - 100kHz Bandwidth

[5] CHIP_EN is asserted at t = 0s

Figure 12 - PSRR 1.2V Output

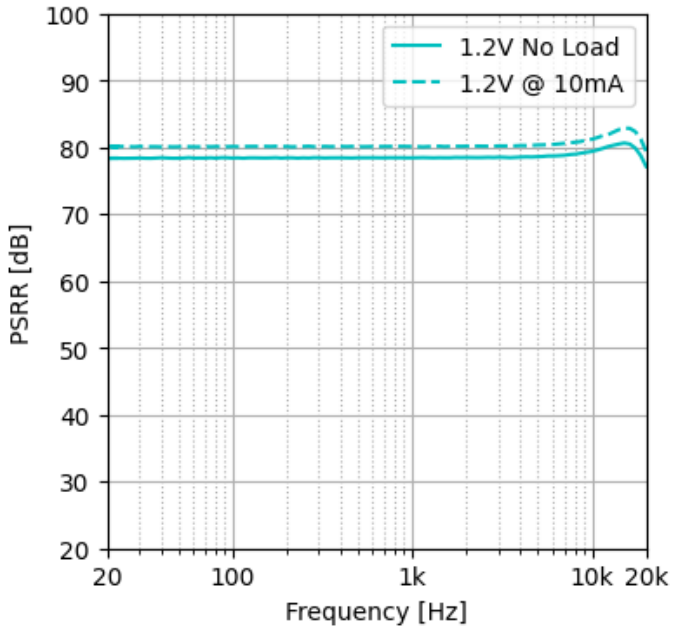


Figure 13 - PSRR 1.8V Output

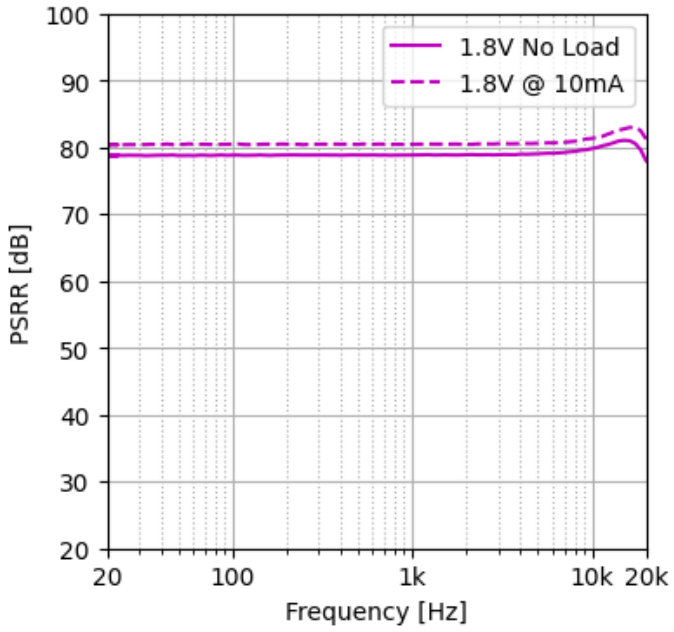


Figure 14 - PSRR 3.3V Output

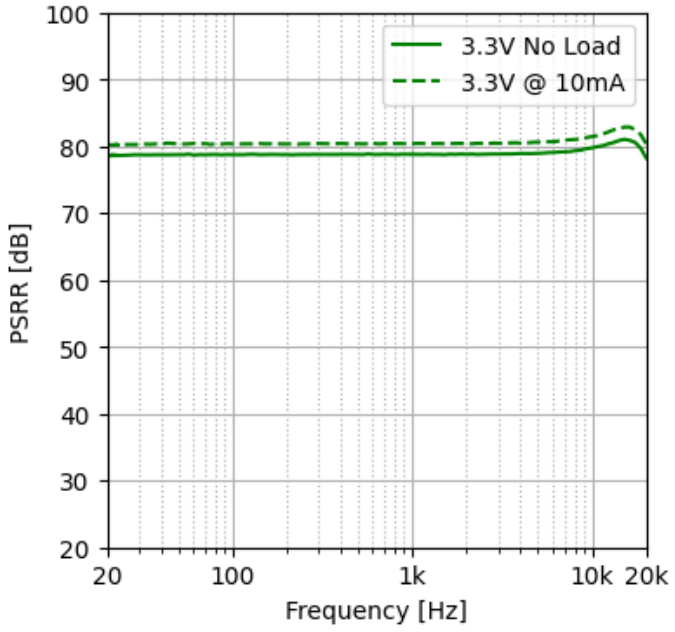


Figure 15 - PSRR 4.5V Output

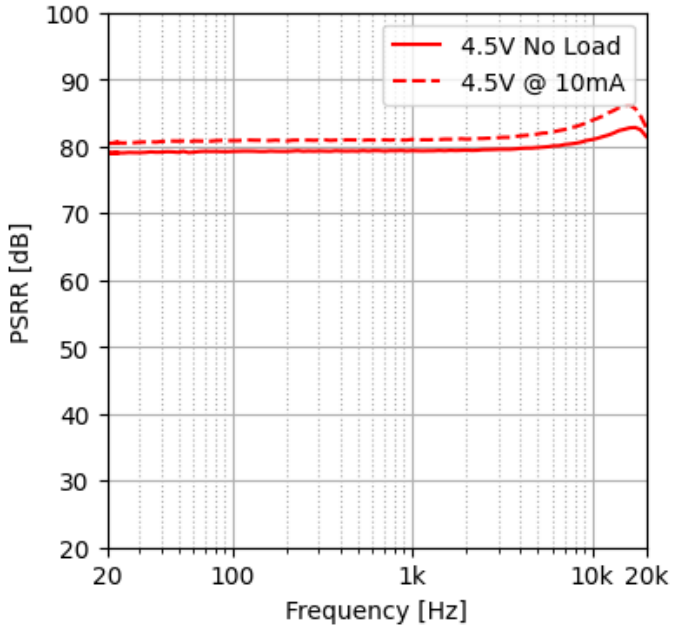


Figure 16 - Load Regulation 1.2V Output

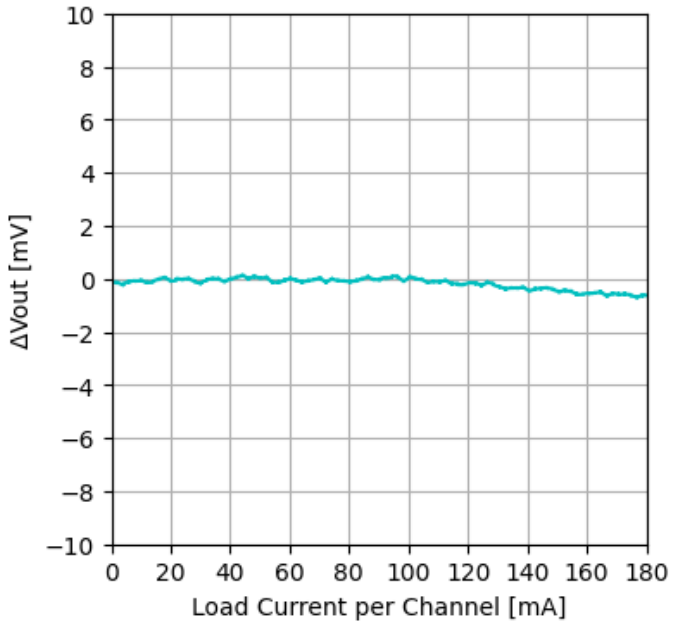


Figure 17 - Load Regulation 1.8V Output

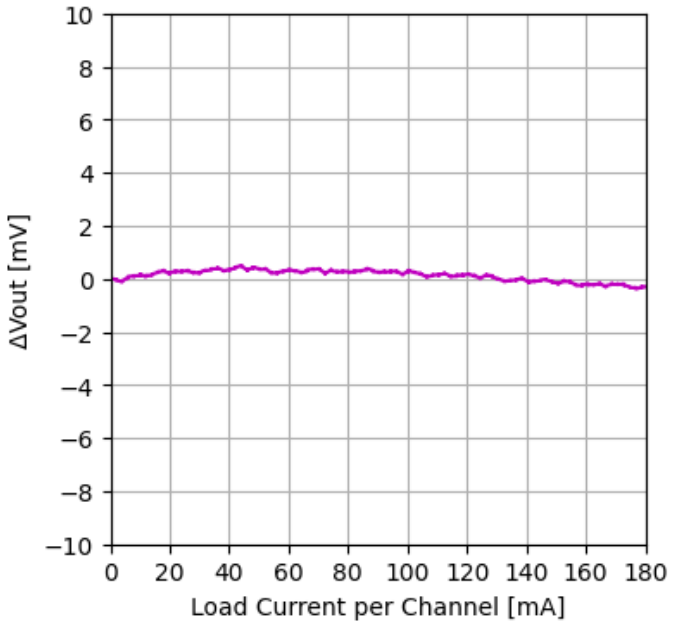


Figure 18 - Load Regulation 3.3V Output

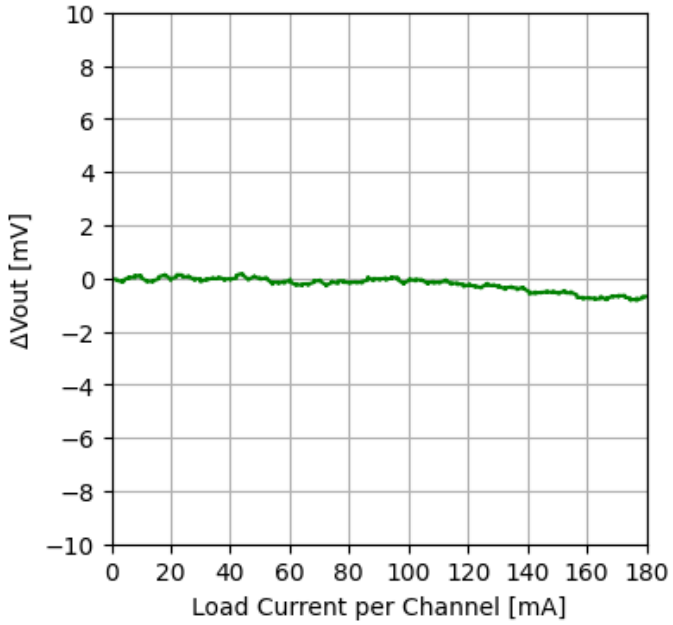


Figure 19 - Load Regulation 4.5V Output

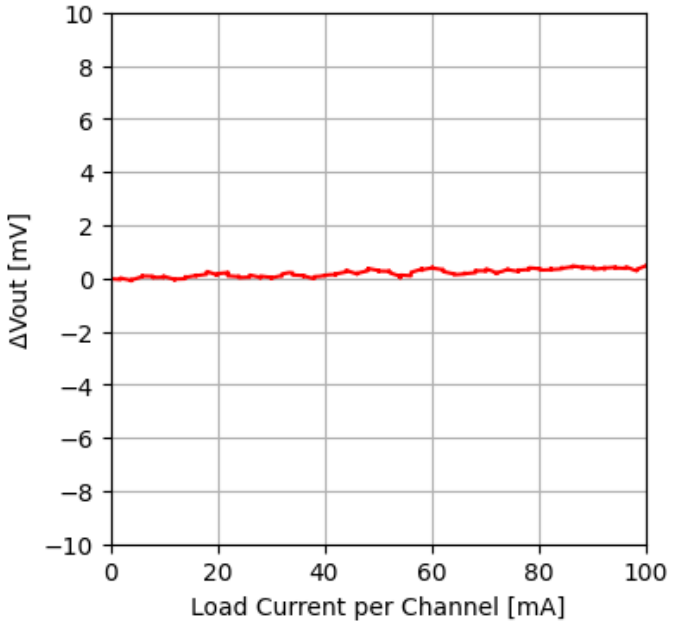


Figure 20 - Overcurrent Hysteresis 1.2V Output

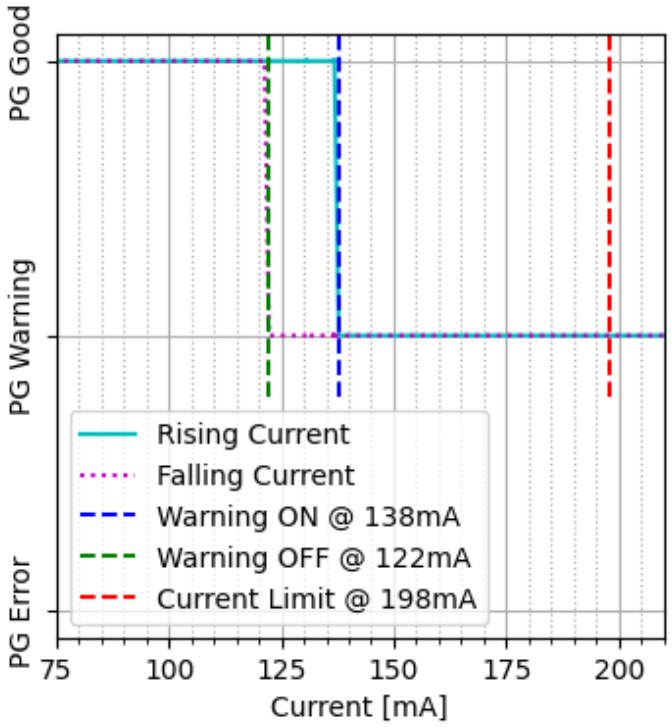


Figure 21 - Overcurrent Hysteresis 1.8V Output

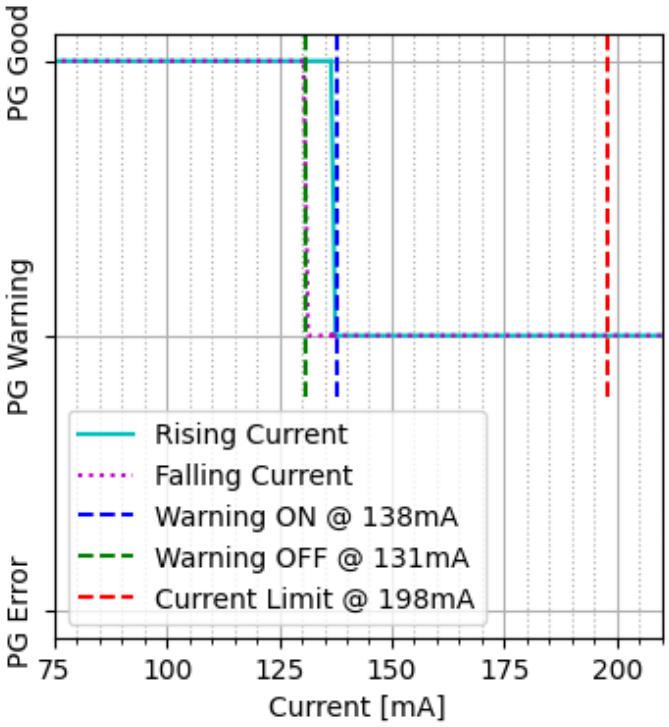


Figure 22 - Overcurrent Hysteresis 3.3V Output

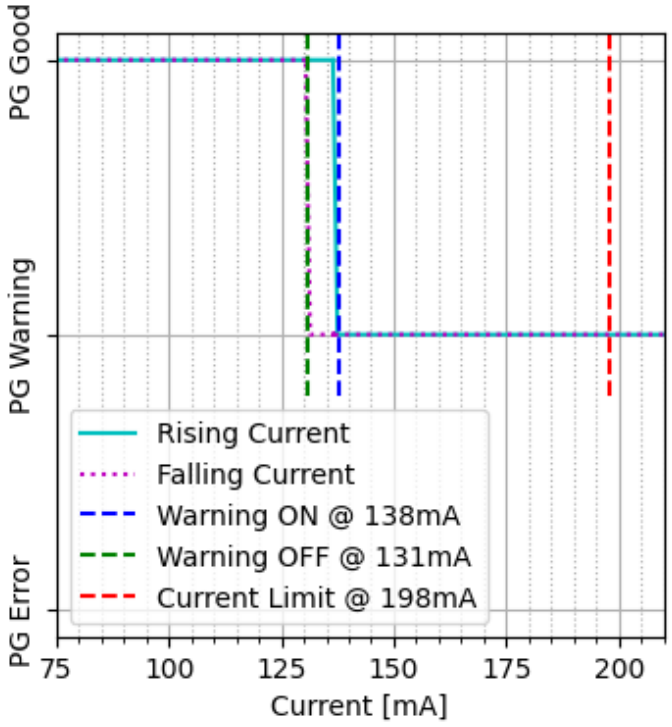


Figure 23 - Overcurrent Hysteresis 4.5V Output

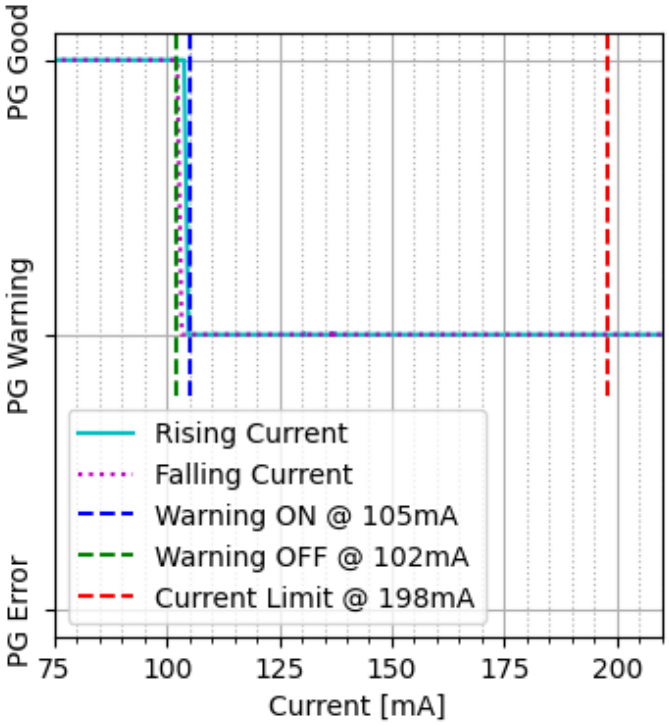
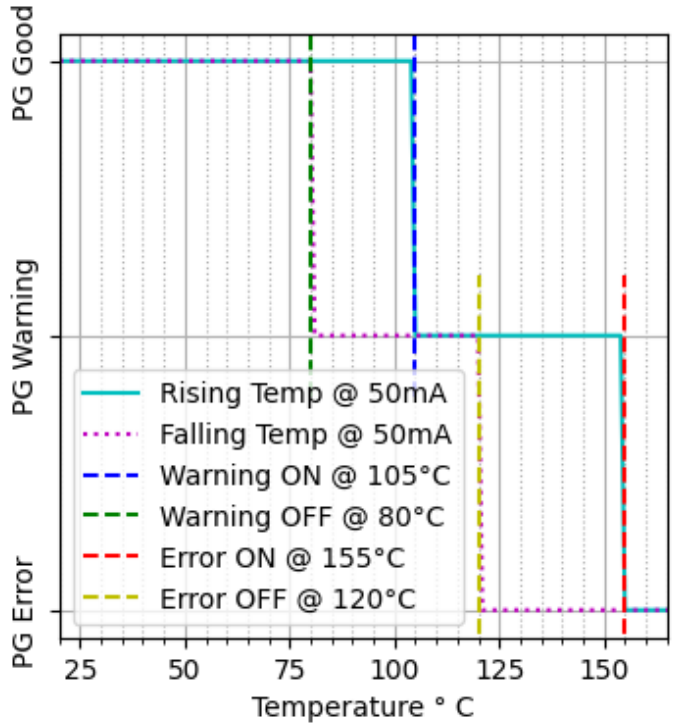


Figure 24 - Overtemperature Hysteresis



Absolute Maximum Ratings

PARAMETER	RATING
Power Supply Voltage	5.5V
Storage temperature	–65°C to +150°C
Operating Junction Temperature	+125°C
ESD Protection Human Body Model (HBM) Machine Model (CDM)	 2kV 500V

Table 13 - Absolute Maximum Ratings

WARNING: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

WARNING: Electrostatic Discharge (ESD) can damage this device. Proper procedures must be followed to avoid ESD when handling this device.

Recommended Operating Conditions

Parameter	Symbol	Conditions
Operating Temperature Range	T_A	-20ºC to +85ºC

Power Supply	Symbol	Voltage[6]	Quiescent Current	Standby Current
AVCC5	V_{IN}	5V ± 5%	7mA	8µA

Table 14 - Recommended Operating Conditions

Note: **ES9312 outputs cannot be used as a current sink.**

DC Electrical Characteristics

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
High-level input voltage	ENH	0.8			V
Low-level input voltage	ENL			0.4	V
Hysteresis			200		mV

Table 15 - DC Electrical Characteristics

[6] For Internal Fixed 4.5V Mode, V_{IN} must not go below 5V

ES9312 Reference Schematics

Internal Fixed Voltage Mode

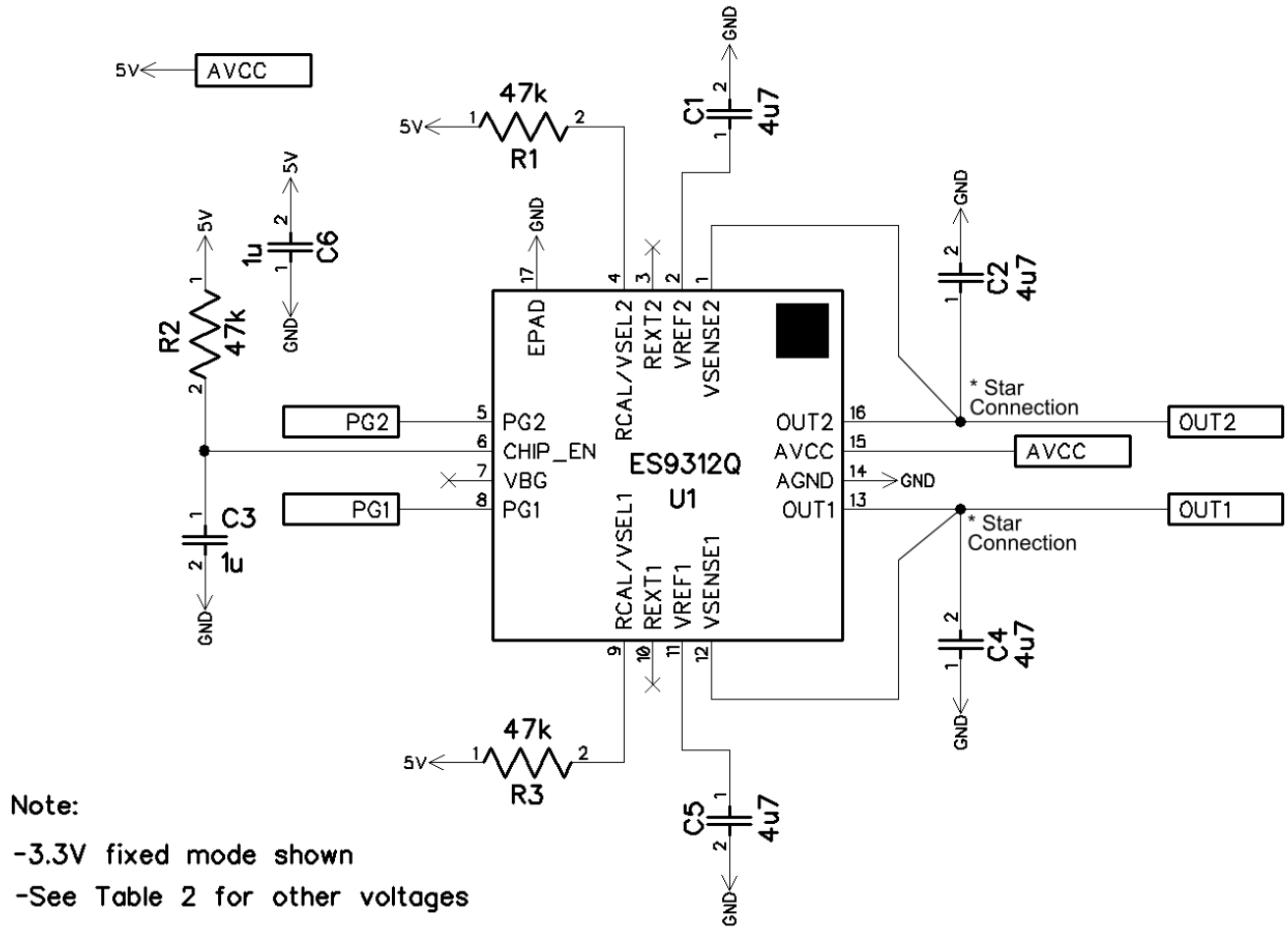


Figure 25 - Fixed Voltage Reference Schematic

Note: In all configurations V_{BG} must remain floating. VSENSEx and OUTx pins need to be star connected to 4.7uF capacitors which are located close to ES9312.

External Fixed Voltage Mode

The ratio of the resistors connected to pins REXT and RCAL will determine the output voltages between 1.2V and 5V.

$$V_{out1} = 2.57 * (R_4/R_5) \qquad V_{out2} = 2.57 * (R_2/R_1)$$

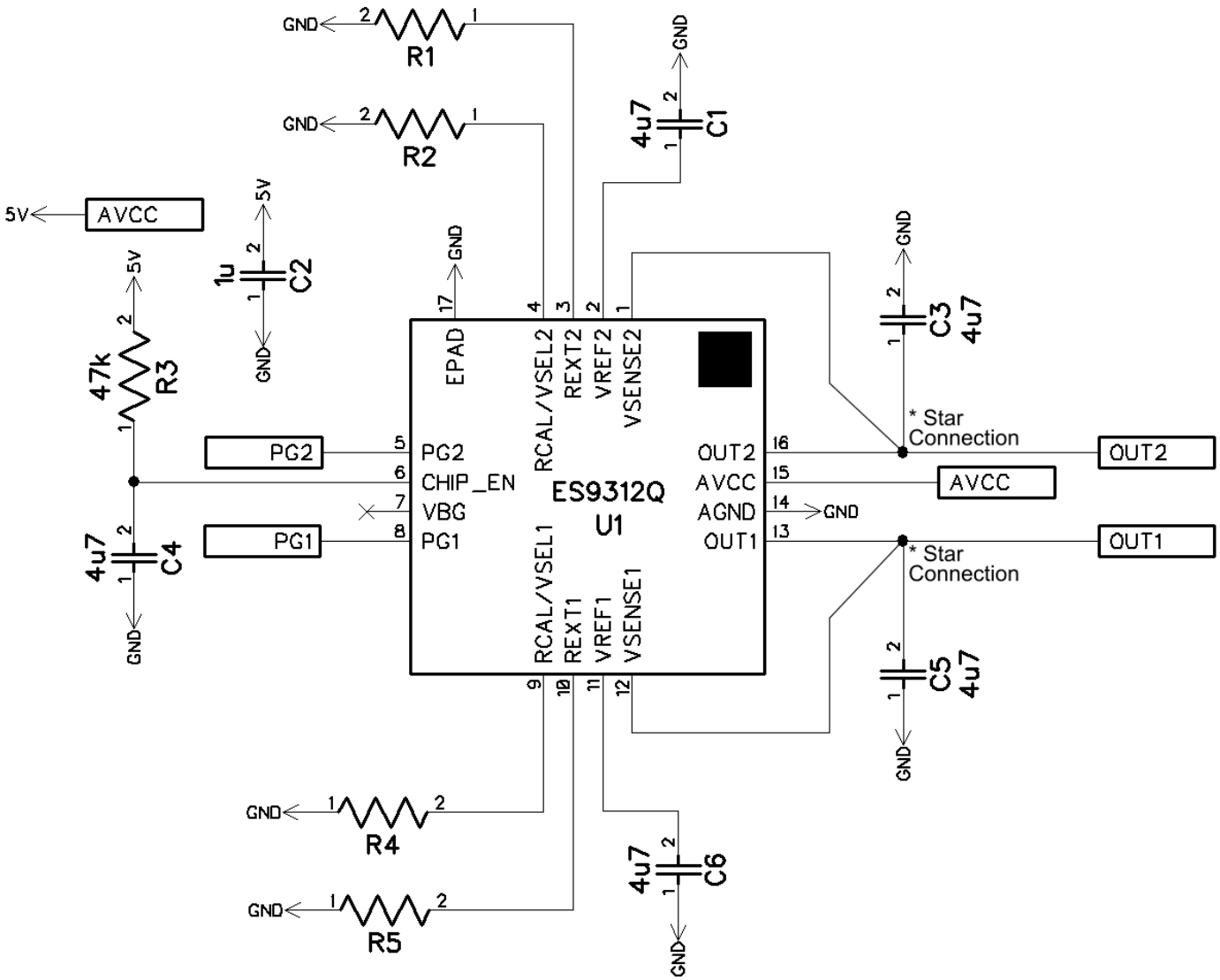


Figure 26 - External Fixed Voltage Reference Schematic

Note: In all configurations V_{BG} must remain floating. VSENSEx and OUTx pins need to be star connected to 4.7uF capacitors which are located close to ES9312.

Calibration Mode

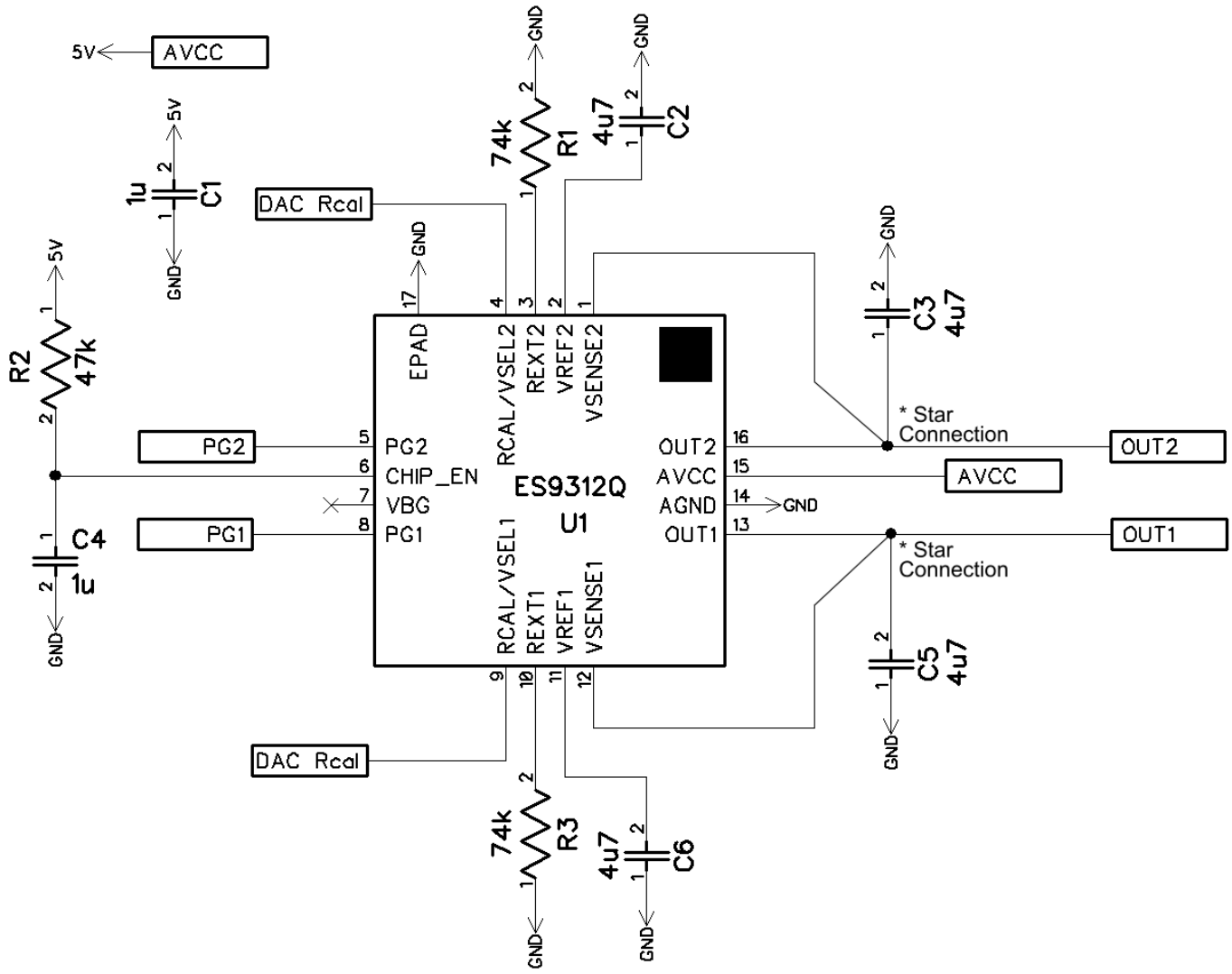


Figure 27 - Calibration Reference Schematic

Note: In all configurations V_{BG} must remain floating. VSENSEx and OUTx pins need to be star connected to 4.7uF capacitors which are located close to ES9312.

Simplified Application Diagram with ES9039Q2M

Example connection of ES9312 with ES9039Q2M for AVCC_DAC1/2 and RCAL for calibration.

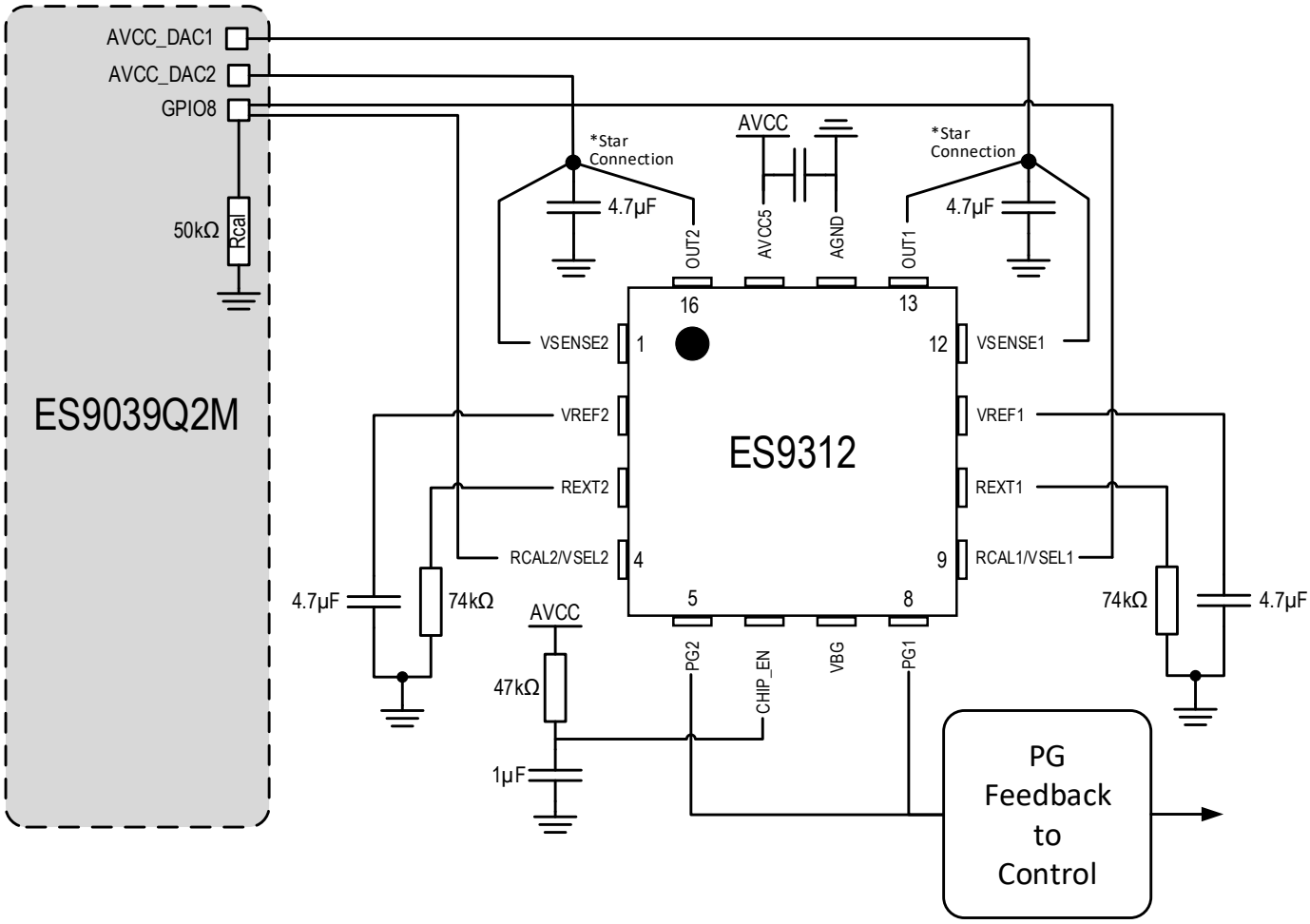
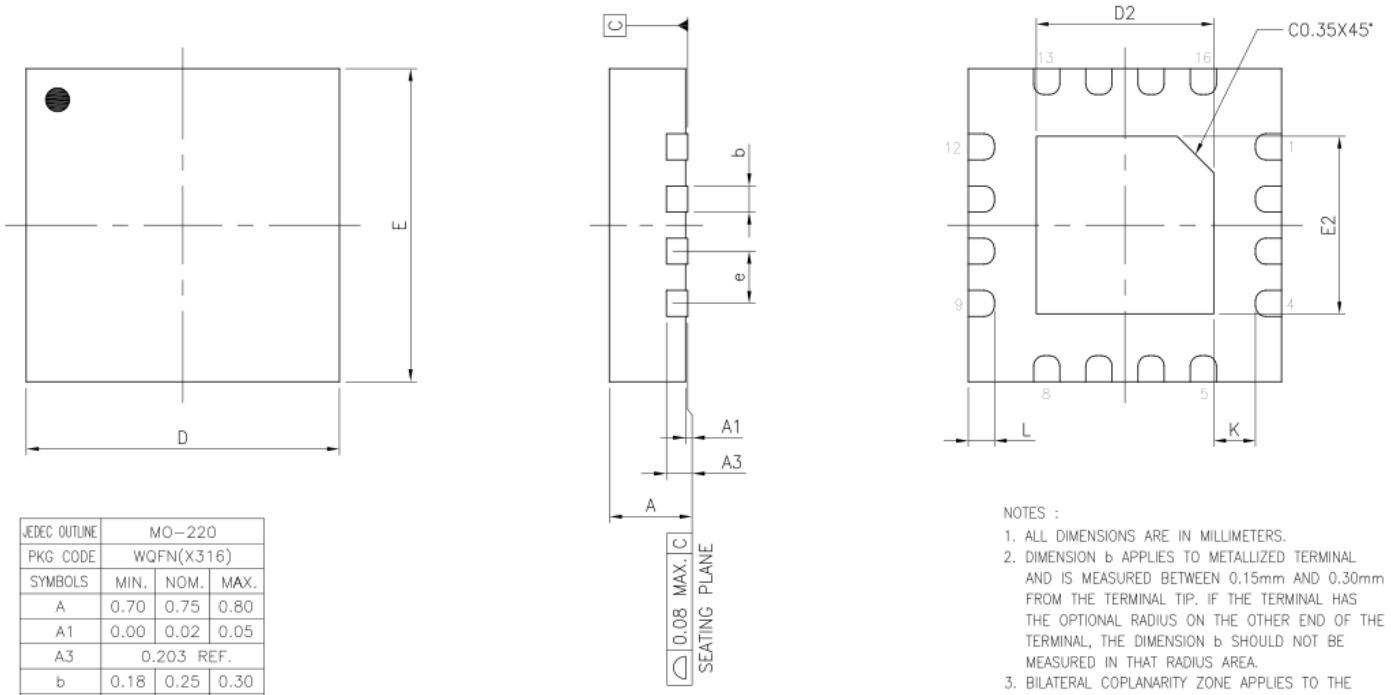


Figure 28 - Calibration Mode Connection with ES9039Q2M

*Note: VSENSEx and OUTx pins need to be star connected to 4.7uF capacitors which is located close to ES9312.

16 QFN Package Dimensions



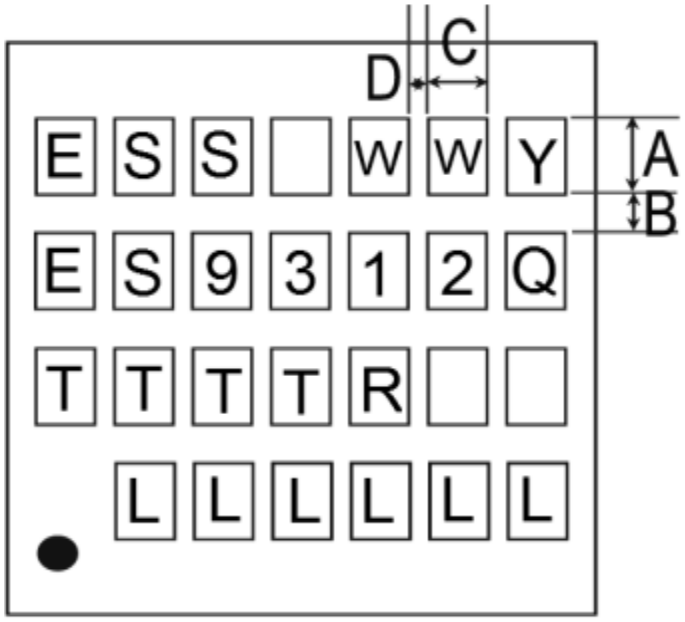
JEDEC OUTLINE	MO-220		
PKG CODE	WQFN(X316)		
SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203 REF.		
b	0.18	0.25	0.30
D	2.90	3.00	3.10
E	2.90	3.00	3.10
e	0.50 BSC		
L	0.20	0.25	0.30
K	0.20	—	—

PAD SIZE	D2			E2			LEAD FINISH		JEDEC CODE
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF	
87X87* MIL	1.65	1.70	1.75	1.65	1.70	1.75	V	X	N/A

NOTES :
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

Figure 29 - ES9312 16 QFN Package Dimensions

16 QFN Top View Marking



	Dimension in mm			
Package Type	A	B	C	D
QFN 3mm x 3mm	0.4	0.2	0.25	0.1

T	Tracking Number
W	Work Week
Y	Last Digit of Year
L	Lot Number
R	Silicon Revision

Table 16 - ES9312 Marking Diagram

Reflow Process Considerations

Temperature Controlled

For lead-free soldering, the characterization and optimization of the reflow process is the most important factor to consider.

The lead-free alloy solder has a melting point of 217°C. This alloy requires a minimum reflow temperature of 235°C to ensure good wetting. The maximum reflow temperature is in the 245°C to 260°C range, depending on the package size (RPC-2-Pb-Free Process - Classification Temperatures (Tc)). This narrows the process window for lead-free soldering to 10°C to 20°C.

The increase in peak reflow temperature in combination with the narrow process window makes the development of an optimal reflow profile a critical factor for ensuring a successful lead-free assembly process. The major factors contributing to the development of an optimal thermal profile are the size and weight of the assembly, the density of the components, the mix of large and small components, and the paste chemistry being used.

Reflow profiling needs to be performed by attaching calibrated thermocouples well adhered to the device as well as other critical locations on the board to ensure that all components are heated to temperatures above the minimum reflow temperatures and that smaller components do not exceed the maximum temperature limits (Table RPC-2).

To ensure that all packages can be successfully and reliably assembled, the reflow profiles studied and recommended by ESS are based on the JEDEC/IPC standard J-STD-020 revision D.1.

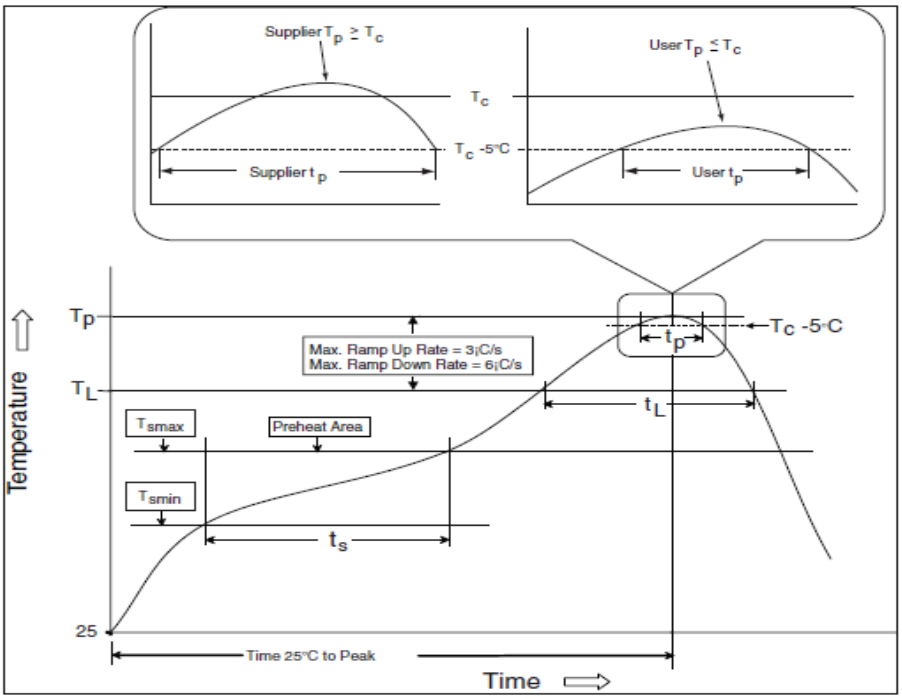


Figure 30 - IR/Convection Reflow Profile (IPC/JEDEC J-STD-020D.1)

Reflow is allowed 3 times. Caution must be taken to ensure time between re-flow runs does not exceed the allowed time by the moisture sensitivity label. If the time elapsed between the re-flows exceeds the moisture sensitivity time bake the board according to the moisture sensitivity label instructions.

Manual

Allowed up to 2 times with maximum temperature of 350ºC no longer than 3 seconds.

RPC-1 Classification Reflow Profile

Profile Feature	Pb-Free Assembly
Preheat/Soak Temperature Min (Tsmin) Temperature Max (Tsmax) Time (ts) from (Tsmin to Tsmax)	 150°C 200°C 60-120 seconds
Ramp-up rate (TL to Tp)	3°C / second maximum
Liquidous temperature (TL) Time (tL) maintained above TL	217°C 60-150 seconds
Peak package body temperature (Tp)	For users Tp must not exceed the classification temp in Table RPC-2. For suppliers Tp must equal or exceed the Classification temp in Table RPC-2.
Time (tp)* within 5°C of the specified classification temperature (Tc)	30* seconds
Ramp-down rate (Tp to TL)	6°C / second maximum
Time 25°C to peak temperature	8 minutes maximum
* Tolerance for peak profile temperature (Tp) is defined as a supplier minimum and a user maximum.	

Table 17 - RPC-1 Classification Reflow Profile

All temperatures refer to the center of the package, measured on the package body surface that is facing up during assembly reflow (e.g., live-bug). If parts are reflowed in other than the normal live-bug assembly reflow orientation (i.e., dead-bug), Tp shall be within ±2°C of the live-bug Tp and still meet the Tc requirements, otherwise, the profile shall be adjusted to achieve the latter. To accurately measure actual peak package body temperatures, refer to JEP140 for recommended thermocouple use.

Reflow profiles in this document are for classification/preconditioning and are not meant to specify board assembly profiles. Actual board assembly profiles should be developed based on specific process needs and board designs and should not exceed the parameters in Table RPC-1.

For example, if Tc is 260°C and time tp is 30 seconds, this means the following for the supplier and the user.
For a supplier: The peak temperature must be at least 260°C. The time above 255°C must be at least 30 seconds.
For a user: The peak temperature must not exceed 260°C. The time above 255°C must not exceed 30 seconds.

All components in the test load shall meet the classification profile requirements.

RPC-2-Pb-Free Process - Classification Temperatures (Tc)

Package Thickness	Volume mm3, <350	Volume mm3, 350 to 2000	Volume mm3, >2000
<1.6 mm	260°C	260°C	260°C
1.6 mm – 2.5 mm	260°C	250°C	245°C
>2.5 mm	250°C	245°C	245°C

Table 18 - RPC-2 Pb Free Classification Temperature

At the discretion of the device manufacturer, but not the board assembler/user, the maximum peak package body temperature (Tp) can exceed the values specified in Table RPC-2. The use of a higher Tp does not change the classification temperature (Tc).

Package volume excludes external terminals (e.g., balls, bumps, lands, leads) and/or nonintegral heat sinks.

The maximum component temperature reached during reflow depends on package thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD packages may still exist.

Ordering Information

Part Number	Description	Package
ES9312Q	SABRE 2 Channel Regulator	3mm x 3mm 16 QFN
ES9312QT	ES9312Q with Extended Temperature Range (-40ºC to 105ºC)	

Table 19 - Ordering Information

Revision History

Current Version 0.2.1

Rev.	Date	Notes
0.2.0	March, 2024	Initial release
0.2.1	March, 2024	• Updated Figure 4 & 5 for clarity • Added note to PG section.