Analog Reinvented

ES9290
Stereo High Performance CODEC
Product Brief

The SABRE® ES9290 is a synchronous stereo analog-to-digital (A/D) and digital-to-analog (D/A) CODEC targeted for professional audio interfaces such as Professional Audio Interfaces, Live stream media, High-quality microphones, and professional DAW (Digital Audio Workstation) Audio Recording.

The ES9290 is a cost-effective solution that has 2 integrated ADCs & DACs which use ESS' patented Hyperstream® IV Architecture, which delivers unprecedented audio sound quality and specifications, including a DNR of +116dB and a THD+N of -110dB/-108dB (DAC/ADC) per channel. A direct monitoring path is also provided with very low latency.

The SABRE CODEC supports synchronous I2S master/slave, and TDM input and outputs.

The ES9290 has built-in programmable gain amplifiers (PGAs) with a gain of up to +30dB, 2Vrms Line Driver Buffers for simplification of BOM requirements, custom pre-programmed filters as well as high pass filters that are complementary to both ADC & DAC, and a Digital Full Biquad (DBQ) filter with many presets and for custom biquad filters.

The ES9290 ADCs have an Ultra-Low Noise Floor Bandwidth of 200kHz. This bandwidth is up to 10 times wider than the competition.

Low latency Direct Monitoring and stereo ADC/DAC mixing are new advanced features.

FEATURE	DESCRIPTION
+116dB DNR per Ch, DAC & ADC -110dB/-108dB THD+N per Ch. (DAC/ADC)	High performance dynamic range and very low distortion for both ADCs & DACs
High Sample Rates	Up to 768kHz (in 64FS mode)
Customizable Filter Characteristics	Presets of digital optimal filters for ADC & DAC, and a DBQ for High Pass Filters and RIAA filters that are customizable
Multiple I/O Formats Available	I2S & TDM inputs/outputs are available, TDM daisy chain is supported
I2C, SPI, and Hardware interface control	Configured by microcontroller or other I2C/SPI source, or pins through Hardware Mode for simplification of control
Direct Monitoring	Low Latency direct monitoring
Programmable Input Amplifies (PGA)	PGA frontend with gain of +0 to +30dB in +3dB steps with 5kΩ input impedance
Digital Volume Control (I2C/SPI) Digital Gain Control (I2C/SPI)	-127 to +6dB in increments of +0.5dB +0 to +42dB in increments of +6dB for creating maximum gain
Integrated DAC Line Driver	Simplifying BOM requirements for the DAC output stage
Programmable MICBIAS	Programmable Microphone BIAS for Analog microphone support
Integrated Analog PLL	Reduces need for additional clocks
Ultra-Low Noise Floor Bandwidth on ADC	200kHz bandwidth enabling higher resolution at higher sample rates
Integrated low noise reference regulators	Reduced BOM cost, PCB area and improved DNR
Low Power Consumption	Simplifies power supply design
Low Pin Count Packaging	5mm x 5mm 40 pin QFN

APPLICATIONS

- Professional Digital Audio Workstation (DAW) Audio Recording
- Very High-Quality Microphones
- Live Stream Media
- Professional Audio Interfaces

Functional Block Diagram

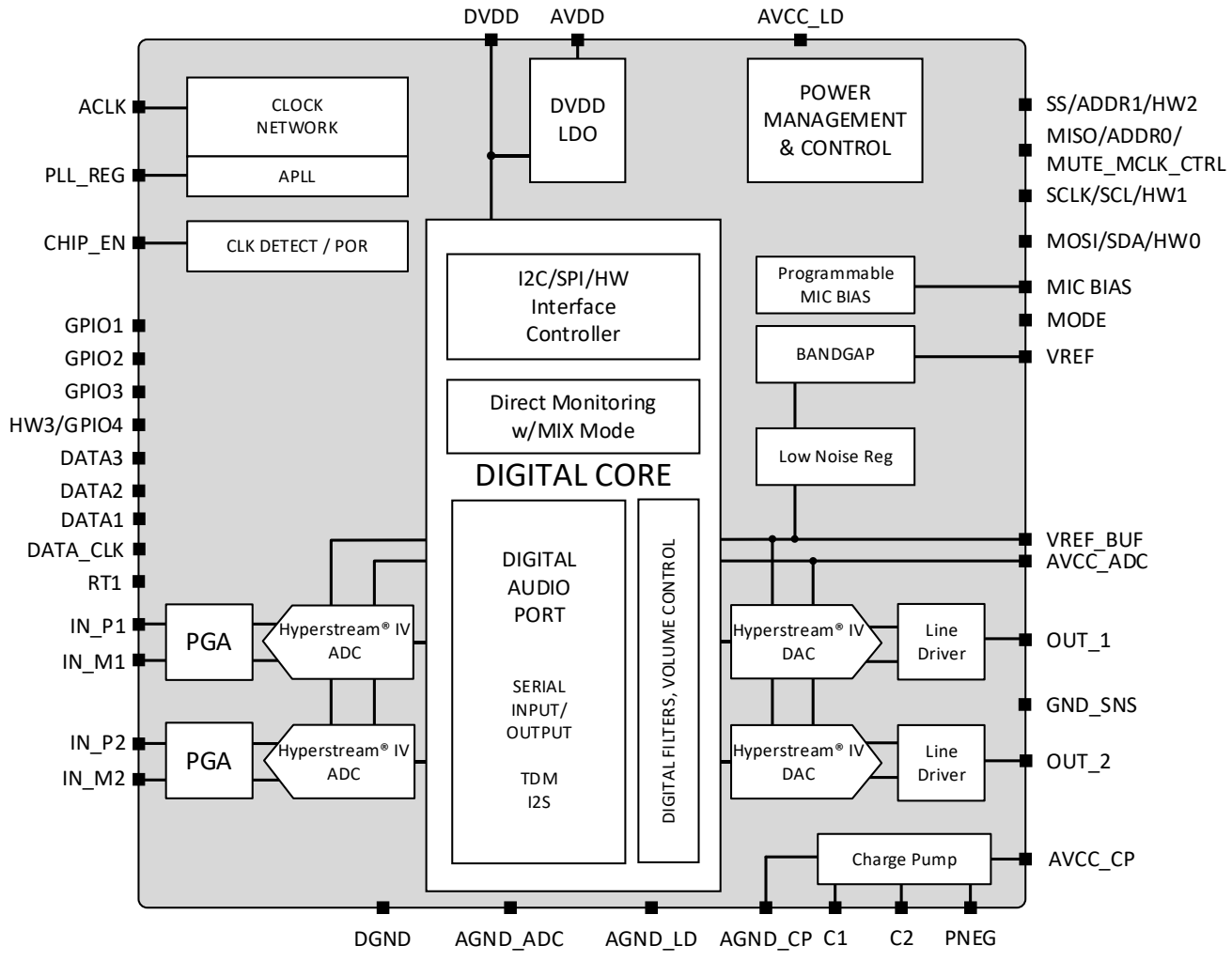

Figure 1 - ES9290 Block Diagram

ES9290 Package

40 QFN Pinout

(Note: Pin 41 will be the QFN package pad)

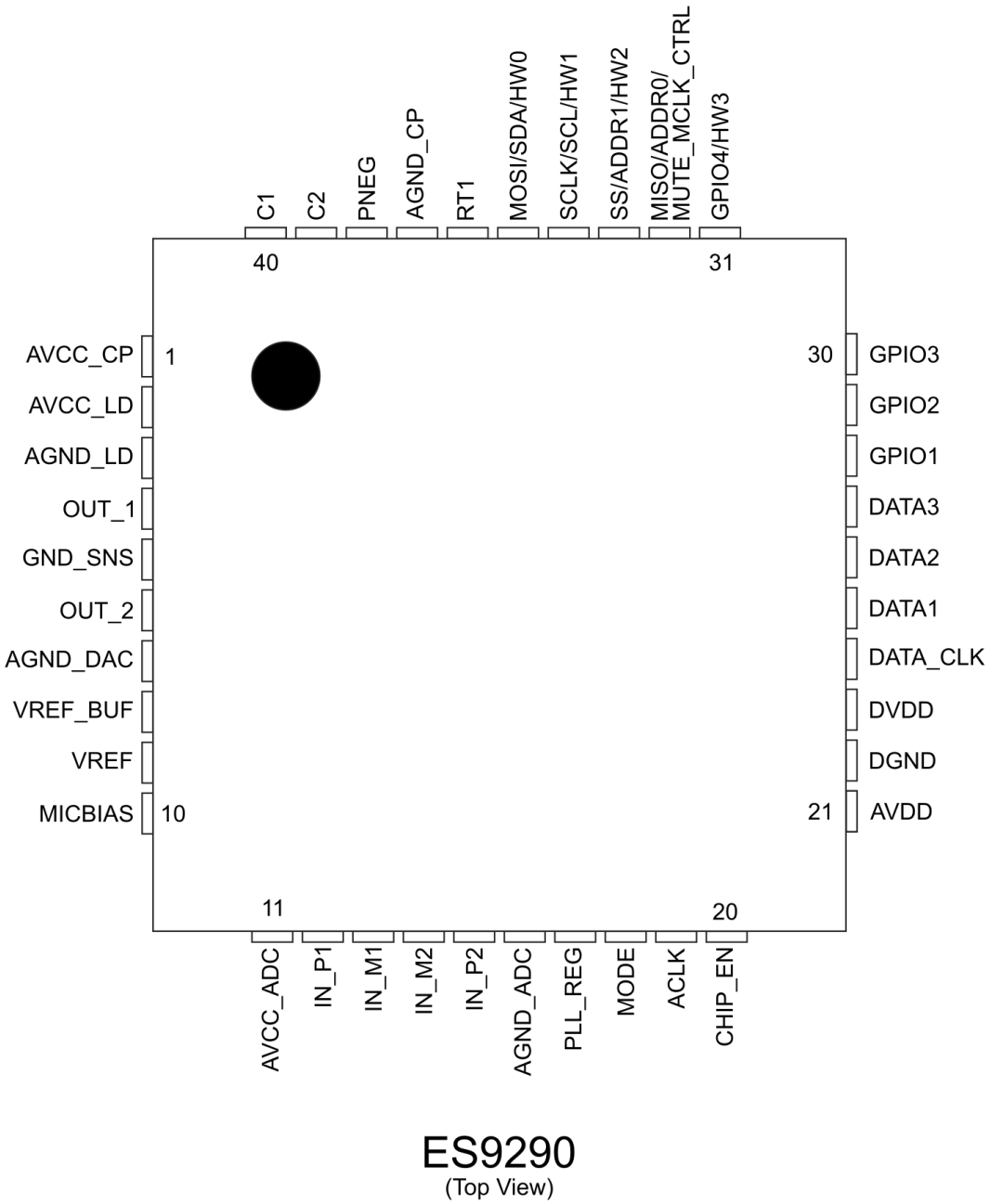

Figure 2 - ES9290 40 QFN Pinout

40 QFN Pin List

Pin	Name	Pin Type	Reset State	Pin Description
1	AVCC_CP	Power	Power	3.3V Supply for Charge Pump
2	AVCC_LD	Power	Power	3.3V Supply for Line Driver
3	AGND_LD	Ground	Ground	Analog Ground for Line Driver
4	OUT_1	A O	Ground	Line Driver Output 1
5	GND_SNS	A I/O	-	Line Driver Ground Sense
6	OUT_2	A O	Ground	Line Driver Output 2
7	AGND_DAC	Ground	Ground	Analog Ground for DAC
8	VREF_BUF	Power	P/D	Low Noise Supply for DAC/ADC, internally generated
9	VREF	Power	P/D	Low Noise Voltage Reference, internally generated
10	MICBIAS	Power	P/D	Low Noise Supply for Microphone Bias, internally generated
11	AVCC_ADC	Power	Power	3.3V Supply for ADC
12	IN_P1	A I	HiZ	ADC Channel 1 Differential Positive (+) Input
13	IN_M1	A I	HiZ	ADC Channel 1 Differential Negative (-) Input
14	IN_M2	A I	HiZ	ADC Channel 2 Differential Negative (-) Input
15	IN_P2	A I	HiZ	ADC Channel 2 Differential Positive (+) Input
16	AGND_ADC	Ground	Ground	Analog Ground for ADC
17	PLL_REG	Power	P/D	Low Noise Supply for PLL, internally generated
18	MODE	D I/O	HiZ	I2C/SPI Control Selection or HW Mode
19	ACLK	A I	HiZ	Clock Input
20	CHIP_EN	D I/O	D I/O	Active-High Chip Enable (Defines Reset State)
21	AVDD	Power	Power	3.3V Supply for Digital I/O
22	DGND	Ground	Ground	Digital Ground for Digital Core
23	DVDD	Power	P/D	1.2V Supply for Digital Core, internally generated
24	DATA_CLK	D I/O	HiZ	Serial Data Clock Pin
25	DATA1	D I/O	HiZ	Serial DATA1
26	DATA2	D I/O	HiZ	Serial DATA2
27	DATA3	D I/O	HiZ	Serial DATA3
28	GPIO1	D I/O	HiZ	General I/O 1
29	GPIO2	D I/O	HiZ	General I/O 2
30	GPIO3	D I/O	HiZ	General I/O 3
31	GPIO4	D I/O	HiZ	General I/O 4
	HW3	D I/O	HiZ	Hardware 3 interface pin, controlled by MODE
32	MISO	D I/O	HiZ	SPI Main In Sub Out pin, controlled by MODE
	ADDR0			I2C Address 0 pin, controlled by MODE

	MUTE_MCLK_CTRL			Hardware Mute Control pin, controlled by MODE
33	SS	D I/O	HiZ	SPI Slave Select pin, controlled by MODE
	ADDR1			I2C Address 1 pin, controlled by MODE
	HW2			Hardware 2 interface pin, controlled by MODE
34	SCLK	D I/O	HiZ	SPI Serial Clock pin, controlled by MODE
	SCL			I2C Serial Clock pin, controlled by MODE
	HW1			Hardware 1 interface pin, controlled by MODE
35	MOSI	D I/O	HiZ	SPI Main Out Sub In pin, controlled by MODE
	SDA			I2C Serial Data pin, controlled by MODE
	HW0			Hardware 0 interface pin, controlled by MODE
36	RT1	D I/O	HiZ	Reserved. Must be connected to GND for normal operation.
37	AGND_CP	Ground	Ground	Analog Ground for Charge Pump
38	PNEG	Power	Ground	-3.3V Supply for Line Driver, internally generated.
39	C2	A I/O	Ground	Charge Pump negative flying capacitor pin
40	C1	A I/O	Ground	Charge Pump positive flying capacitor pin
41	Package Pad[1]	-	-	Not electrically connected, used for heat dissipation. Connect to DGND.

Table 1 – 40 QFN Pin List

[1] Pin 41 is the package pad. See 40 QFN package dimensions for sizing. Connect to DGND.

Direct Monitoring

Direct Monitoring for the ES9290 is a low latency path (< 10 Samples) for monitoring the incoming analog source.

The digital path incorporates a digital gain of +0dB to +42dB in +6dB steps for both ADC & DAC and a channel mixer for maximum configurability.

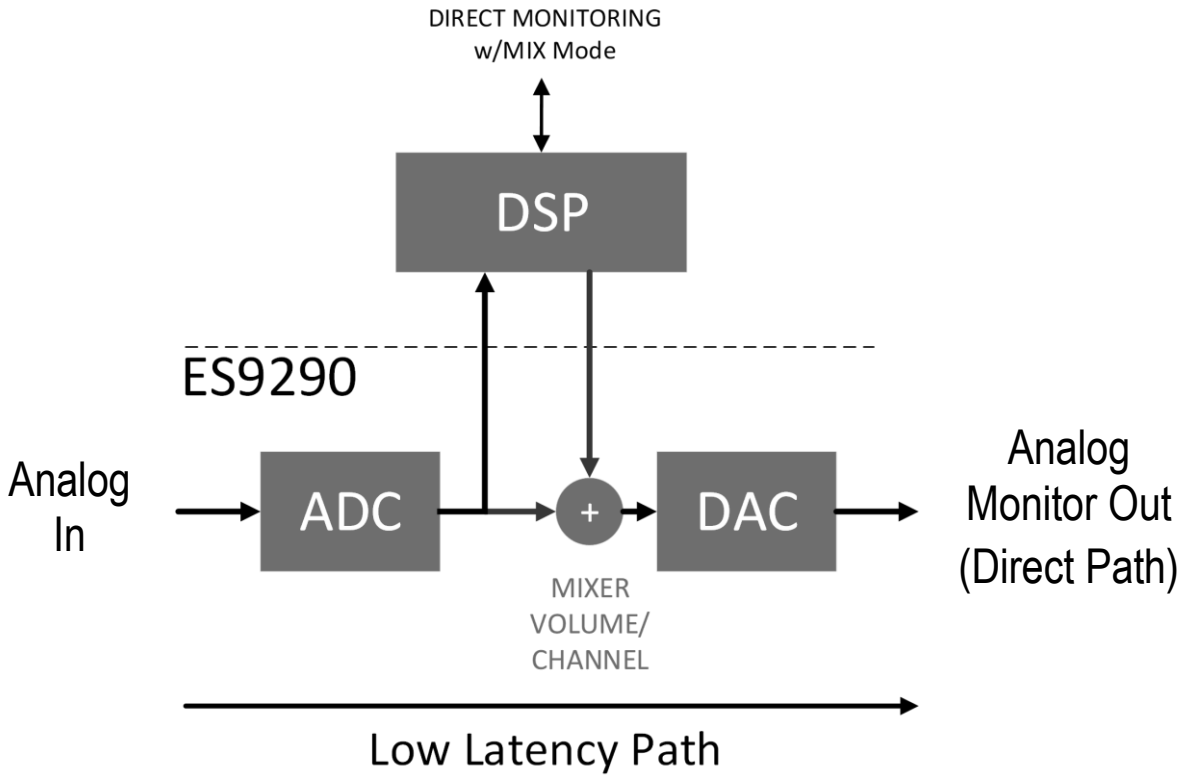

Figure 3 - ES9290 Direct Monitoring

Ordering Information

Part Number	Description	Package
ES9290Q	SABRE 32-bit 2 Channel ADC/DAC CODEC with built in digital filters, and multiple input/output formats	5mm x 5mm 40 QFN

Revision History

Current Version 0.9.4

Rev.	Date	Notes
0.9.4	January 22, 2024	Initial release