Analog Reinvented

SABRE HiFi

ES9118
32-bit Stereo Low Power DAC with Headphone Amplifier and Output Switch

The ***ES9118 SABRE DAC with Headphone Amp*** is a high-performance 32-bit, 2-channel audio D/A converter with headphone amplifier and output switch designed for audiophile-grade portable power sensitive applications such as digital music players, consumer applications such as USB DACs and A/V receivers, as well as professional applications such as mixer consoles and digital audio workstations.

Using the critically acclaimed ESS patented 32-bit HyperStream® DAC architecture and Time Domain Jitter Eliminator, the ***ES9118*** delivers up to 125dB SNR and –112dB THD+N, a performance level that will satisfy the most demanding audio enthusiasts.

The ***ES9118's*** integrated SABRE DAC supports up to up to 32-bit 384kHz PCM and DSD256 data in master or slave timing modes. A fully programmable FIR filter with seven presets provides a customizable sound signature and the integrated headphone amp supports up to 1.1Vrms output. The patented, integrated output switch allows non-HiFi sources, such as speech, to bypass the ***ES9118*** to minimize power consumption. Residual distortion from suboptimal PCB components and layout can be minimized using ***ES9118's*** unique THD compensation circuit, while PCB footprint and bill-of-materials are minimized by the integrated low-noise DAC reference LDO.

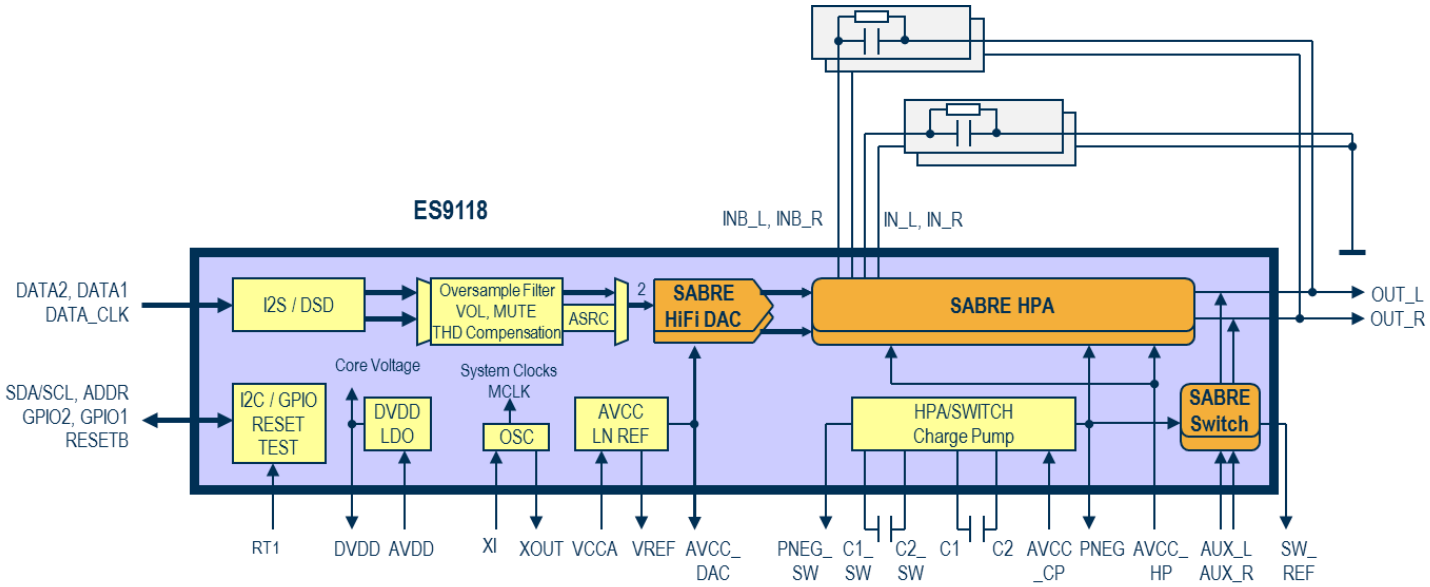
The ***ES9118*** sets the standard for HD audio performance enabling **SABRE HiFi** experience all the way from the audio source to headphones in an easy-to-use 40-CSP package or 40 pin QFN package.

FEATURE	DESCRIPTION
Patented 32-bit HyperStream® DAC/HPA ○ +125dB SNR, +120dB DNR ○ –112dB THD+N, 1.1Vrms into 600Ω ○ –105dB THD+N, 15mW into 32Ω	○ Industry's highest performance 32-bit mobile audio DAC/HPA with unprecedented dynamic range & ultra-low distortion ○ Support synchronous and asynchronous sampling modes ○ Enable **SABRE HiFi** experience all the way to headphones
Patented Time Domain Jitter Eliminator	○ Unmatched audio clarity free from input clock jitter
64-bit accumulator & 32-bit processing	○ Distortion free signal processing
Versatile digital input	○ Support master/slave PCM (I^2S, LJ 16-32-bit) or DSD
Customizable filter characteristics	○ 7 preset filters ○ User-programmable filter for custom sound signature
Output Switch for Auxiliary Source	○ Voice mode bypass with negligible power consumption
Integrated Low Noise AVCC LDO	○ Eliminate external LDO and reduce PCB size
THD Compensation	○ Minimize distortion from external PCB components and layout
40-CSP Package and 40 pin QFN package	○ Minimize PCB footprint
1.8/3.3V Digital Supply 1.8/3.3V DAC Analog Supply 1.8V HPA Supply	○ Support 1.8/3.3V logic levels ○ Customizable DAC analog performance ○ Minimize HPA power consumption
32mW low-power mode consumption <1mW standby mode consumption	○ Maximize battery life

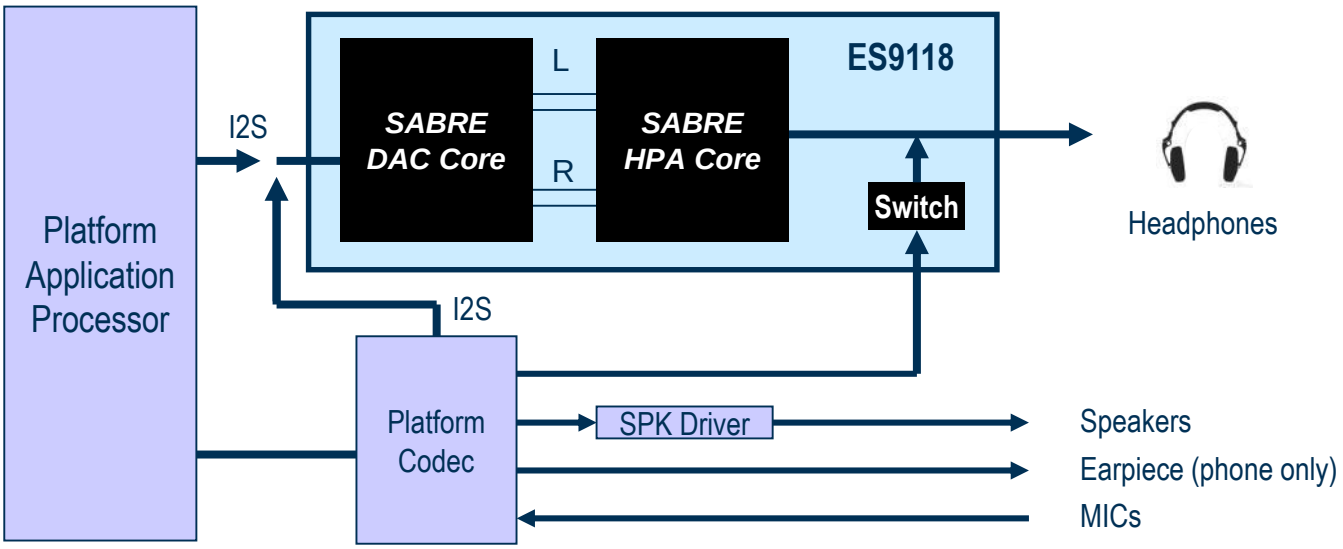
APPLICATIONS

- Mobile phones / Tablets / Digital music players / Portable multimedia players
- Consumer and Audiophile USB DAC headphone amplifiers and A/V receivers
- Professional digital audio workstations and mixer consoles

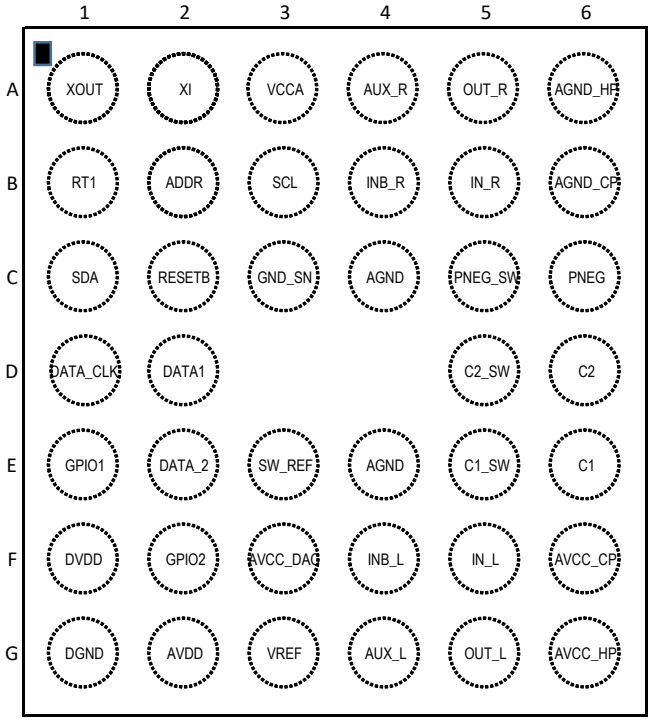
FUNCTIONAL BLOCK DIAGRAM



TYPICAL APPLICATION DIAGRAM



ES9118EC (40-CSP) PIN LAYOUT



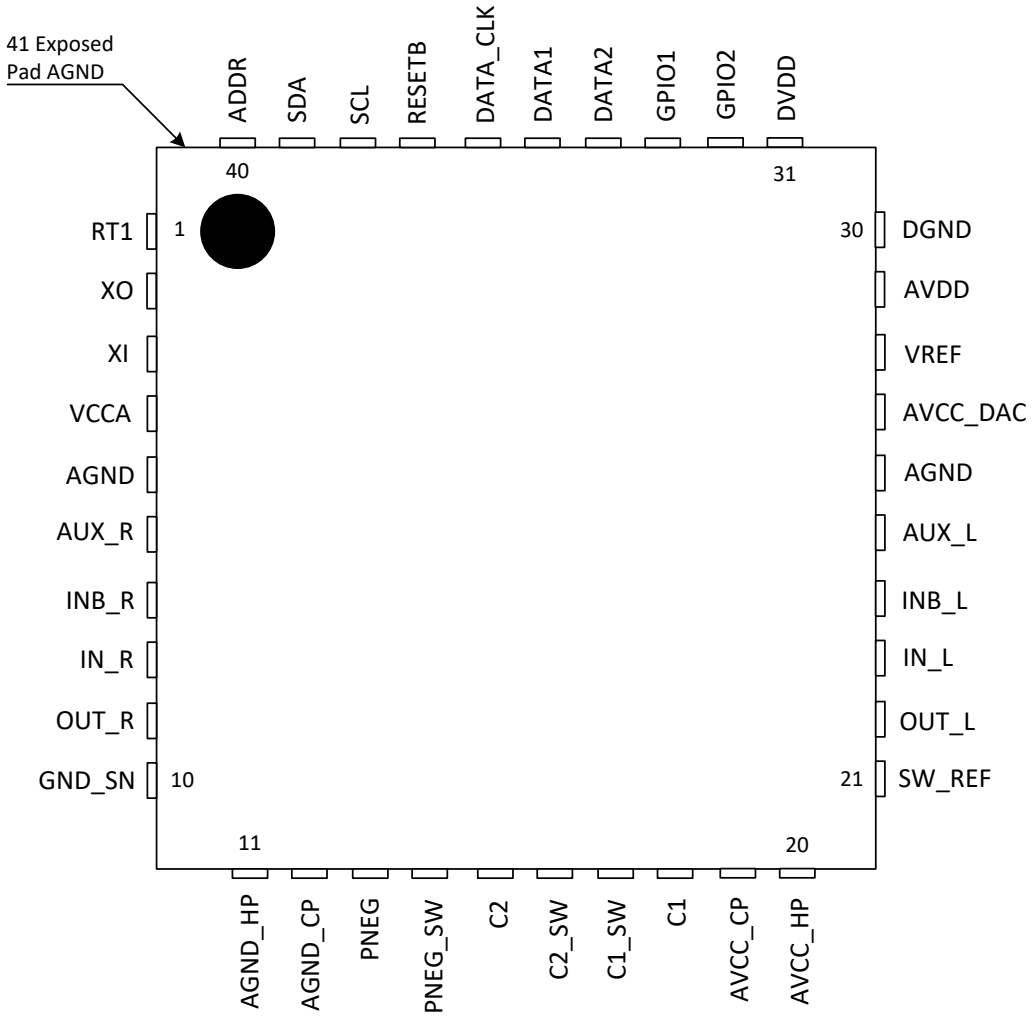
Pin Layout of ES9118EC
(Top View)

ES9118EC (40CSP) PIN DESCRIPTIONS

Pin	Name	Pin Type	Reset State	Pin Description
A1	XOUT	AO	Floating	XTAL output
A2	XI	AI	Floating	XTAL input
A3	VCCA	Power	Power	Analog 1.8V / 3.3V for OSC and on-chip AVCC_DAC regulator
A4	AUX_R	AI	-	Auxiliary analog input (Right Channel)
A5	OUT_R	AO	-	Amplifier output (Right Channel)
A6	AGND_HP	Ground	Ground	Amplifier analog ground
B1	RT1	I	Tri-stated	Reserved. Must be connected to DGND for normal operation
B2	ADDR	I	Tri-stated	I^2C address select
B3	SCL	I	Tri-stated	I^2C serial clock input
B4	INB_R	AI	-	Amplifier differential inverting input (Right Channel)
B5	IN_R	AI	-	Amplifier differential non-inverting input (Right Channel)
B6	AGND_CP	Ground	Ground	Charge pump analog ground
C1	SDA	I/O	Tri-stated	I^2C serial data input/output
C2	RESETB	I	1'b0	Power down (active low)
C3	GND_SN			Amplifier load ground sense
C4	AGND	Ground	Ground	DAC analog ground
C5	PNEG_SW	Power	Power	Negative supply for bypass switch. Internally supplied
C6	PNEG	Power	Power	Amplifier negative supply. Internally supplied
D1	DATA_CLK	I/O	Tri-stated	Slave Mode: Input for PCM Bit Clock or DSD Bit Clock, Master Mode: Output for PCM Bit Clock
D2	DATA1	I/O	Tri-stated	Slave Mode: Input for PCM Frame Clock or Input for DSD Data1 (Left Channel) Master Mode: Output for PCM Frame Clock
D5	C2_SW	-	-	Bypass switch charge pump negative flying capacitor pin
D6	C2	-	-	Amplifier charge pump negative flying capacitor pin
E1	GPIO1	I/O	Tri-stated	GPIO 1
E2	DATA2	I	Tri-stated	PCM Data Ch1+Ch2 or DSD Data2 (Right Channel)
E3	SW_REF	AI	-	Switch transition rate setting
E4	AGND	Ground	Ground	DAC analog ground
E5	C1_SW	-	-	Bypass switch charge pump positive flying capacitor pin
E6	C1	-	-	Amplifier charge pump positive flying capacitor pin
F1	DVDD	Power	Power	Digital core supply. Internally supplied
F2	GPIO2	I/O	Tri-stated	GPIO 2 *special Aux. Path function in standby*
F3	AVCC_DAC	Power	Power	DAC analog supply. Internally supplied.
F4	INB_L	AI	-	Amplifier differential inverting input (Left Channel)
F5	IN_L	AI	-	Amplifier differential non-inverting input (Left Channel)
F6	AVCC_CP	Power	Power	Analog 1.8V supply for amplifier charge pump
G1	DGND	Ground	Ground	Digital ground
G2	AVDD	Power	Power	Digital 1.8V / 3.3V supply for I/O and on-chip DVDD regulator
G3	VREF	Power	Power	Low Noise reference for on-chip AVCC_DAC regulator
G4	AUX_L	AI	-	Auxiliary analog input (Left Channel)
G5	OUT_L	AO	-	Amplifier output (Left Channel)
G6	AVCC_HP	Power	Power	Analog 1.8V supply for Amplifier and Switch

Note D3 & D4 do not have bumps.

ES9118EQ (40-QFN) PIN LAYOUT



Pin Layout of ES9118EQ
(Top View)

ES9118EQ (40QFN) PIN DESCRIPTIONS

Pin	Name	Pin Type	Reset State	Pin Description
1	RT1	I	Tri-stated	Reserved. Must be connected to DGND for normal operation
2	XOUT	AO	Floating	XTAL output
3	XI	AI	Floating	XTAL input
4	VCCA	Power	Power	Analog 1.8V / 3.3V for OSC and on-chip AVCC_DAC regulator
5	AGND	Ground	Ground	DAC analog ground
6	AUX_R	AI	-	Auxiliary analog input (Right Channel)
7	INB_R	AI	-	Amplifier differential inverting input (Right Channel)
8	IN_R	AI	-	Amplifier differential non-inverting input (Right Channel)
9	OUT_R	AO	-	Amplifier output (Right Channel)
10	GND_SN			Amplifier load ground sense
11	AGND_HP	Ground	Ground	Amplifier analog ground
12	AGND_CP	Ground	Ground	Charge pump analog ground
13	PNEG	Power	Power	Amplifier negative supply. Internally supplied
14	PNEG_SW	Power	Power	Negative supply for bypass switch. Internally supplied
15	C2	-	-	Amplifier charge pump negative flying capacitor pin
16	C2_SW	-	-	Bypass switch charge pump negative flying capacitor pin
17	C1_SW	-	-	Bypass switch charge pump positive flying capacitor pin
18	C1	-	-	Amplifier charge pump positive flying capacitor pin
19	AVCC_CP	Power	Power	Analog 1.8V supply for amplifier charge pump
20	AVCC_HP	Power	Power	Analog 1.8V supply for Amplifier and Switch
21	SW_REF	Power	Power	Switch transition rate setting
22	OUT_L	AO	-	Amplifier output (Left Channel)
23	IN_L	AI	-	Amplifier differential non-inverting input (Left Channel)
24	INB_L	AI	-	Amplifier differential inverting input (Left Channel)
25	AUX_L	AI	-	Auxiliary analog input (Left Channel)
26	AGND	Ground	Ground	DAC analog ground
27	AVCC_DAC	Power	Power	DAC analog supply. Internally supplied
28	VREF	Power	Power	Low Noise reference for on-chip AVCC_DAC regulator
29	AVDD	Power	Power	Digital 1.8V / 3.3V supply for I/O and on-chip DVDD regulator
30	DGND	Ground	Ground	Digital ground
31	DVDD	Power	Power	Digital core supply. Internally supplied
32	GPIO2	I/O	Tri-stated	GPIO 2 *special Aux. Path function in standby*
33	GPIO1	I/O	Tri-stated	GPIO 1
34	DATA2	I	Tri-stated	PCM Data Ch1+Ch2 or DSD Data2 (Right Channel)
35	DATA1	I/O	Tri-stated	Slave Mode: Input for PCM Frame Clock or Input for DSD Data1 (Left Channel) Master Mode: Output for PCM Frame Clock
36	DATA_CLK	I/O	Tri-stated	Slave Mode: Input for PCM Bit Clock or DSD Bit Clock, Master Mode: Output for PCM Bit Clock
37	RESETB	I	1'b0	Power down (active low)
38	SCL	I	Tri-stated	I^2C serial clock input
39	SDA	I/O	Tri-stated	I^2C serial data input/output
40	ADDR	I	Tri-stated	I^2C address select
41	AGND	Ground	Ground	Exposed pad

FUNCTIONAL DESCRIPTION – AUDIO INPUTS

Sample Rate Notation

Mode	fs (target sample rate)	FSR (raw sample rate)
DSD	DATA_CLK / 64	DSD data rate
Serial (PCM) Normal Mode	Frame Clock Rate	Frame Clock Rate
Serial (PCM) OSF Bypass Mode	Frame Clock Rate / 8	Frame Clock Rate

System Clock (XIN) and Audio Master Clock (MCLK)

The system clock (XIN) can be generated with a crystal using the built-in oscillator or supplied externally.

- The maximum XIN frequency is 50MHz as specified in ANALOG PERFORMANCE and XI Timing.
- The audio master clock (MCLK) is divided down from XIN via *clk_gear* in Register 0: System Registers.
- The minimum MCLK frequency for a given raw sample rate FSR is specified in ANALOG PERFORMANCE.
- The minimum MCLK frequency for a given I2C clock is specified in the table under I2C Timing Table.

PCM Pin Connections

Pin Name	Description
DATA1	Frame clock
DATA2	2-channel PCM serial data
DATA_CLK	Bit clock for PCM audio format

Note: DATA_CLK frequency must be (2 x *serial_length*) x FSR.
serial_length can be set in Register 1: Input selection.

DSD Pin Connections

Pin Name	Description
DATA1	DSD data input - Left
DATA2	DSD data input – Right
DATA_CLK	Bit clock for DSD data input

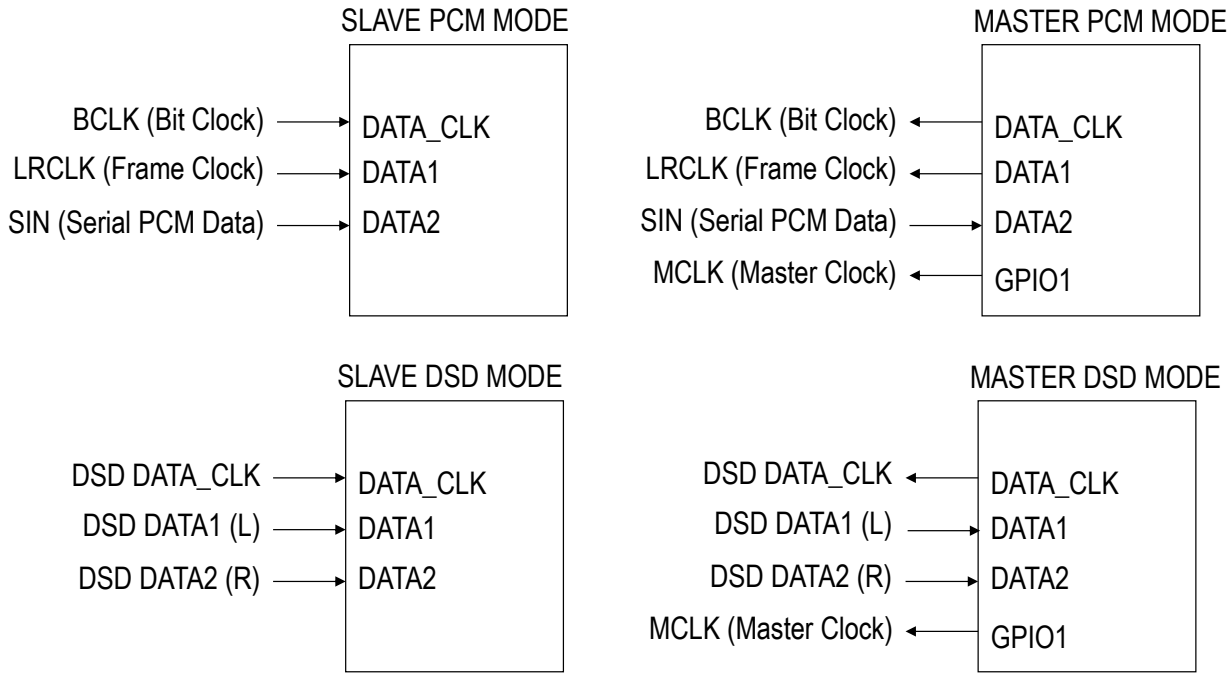
Note: DATA_CLK frequency must be FSR.

Master Mode

The DAC can become an audio timing master via *master_mode* in Register 10: Master Mode and Sync Configuration.
- The 'input_select' bits in Register 1: Input selection must be set correctly to select either DSD or serial master mode.

The Bit Clock frequency can be configured using one of the following two methods:
- *Set the desired master_div* in Register 10: Master Mode and Sync Configuration, or
- Use NCO mode to set FSR using Register 34-37: Programmable NCO. When in NCO mode the *master_div* setting will be ignored.

An available GPIO pin can be configured to output MCLK using Register 8: GPIO1-2 Configuration.



FUNCTIONAL DESCRIPTION – DIGITAL FEATURES

Soft Mute

When Mute is asserted the output signal will ramp to the –∞ level. When Mute is reset the attenuation level will ramp back up to the previous level set by the volume control register. Asserting Mute will not change the value of the volume control register. The ramp rate is set by Register 6: Volume Ramp Rate according to the following relationship:

$$\text{rate} = \frac{2^{\text{vol\_rate}} * \text{FSR}}{512} \text{ dB/s}$$

Automute (PCM mode only)

Automute must be enabled and configured using Register 2: Mixing, Serial Data and Automute Configuration. It is disabled by default. Automute is triggered when the following conditions are met:

Mode	Detection Condition	Time
PCM	Data is lower than *automute_level* for the specified time	$\frac{2096896}{\text{automute\_time} * \text{FSR}}$ (s)

Automute_time can be set using Register 4: Automute Time.
Automute_level can be set using Register 5: Automute Level.

Digital Volume Control (not applicable in OSF Bypass mode)

Each channel has an independently controlled digital attenuation circuit which can be set to attenuate from 0dB to –127dB in 0.5dB steps. When a new volume level is set, the digital attenuation circuit will ramp softly to the new level. To ensure silent digital volume transitions each 0.5dB step can take as many as 64 intermediate steps depending on the *volume_rate* setting in Register 6: Volume Ramp Rate.

Master Trim (not applicable in OSF Bypass mode)

The master trim sets the 0dB reference level for the digital volume control of each DAC. The master trim is programmable via Register 17-20: Master Trim. The master trim registers store a 32bit signed number. This register value should never exceed the full scale signed value 32'h7FFFFFFF

System Clock (XI)

See XI Timing for supported XI frequencies. The audio master clock (MCLK) is derived from XI via Clock Gearing and must also satisfy the following conditions:

Data Type	Minimum MCLK Frequency
DSD Data	MCLK > 3 x FSR , FSR = 2.8224MHz x (1, 2, or 4)
Serial Normal Mode	MCLK > 192 x FSR, FSR ≤ 192kHz MCLK = 128 x FSR (synchronous MCLK) with FSR ≤ 384kHz
Serial OSF Bypass Mode	MCLK > 24 x FSR, FSR ≤ 768kHz

Preset FIR Filters

Seven pre-programmed digital filters are included for PCM serial mode. See PCM Filter Characteristics for more information.

Programmable FIR filter

A two stage interpolating FIR design is used. The interpolating FIR filter is generated using MATLAB, and can then be downloaded using a custom C code.

Example Source Code for Loading a Filter

```
// only accept 128 or 16 coefficients
// Note:  The coefficients must be quantized to 24 bits for this method!
// Note:  Stage 1 consists of 128 values (0-127 being the coefficients)
// Note:  Stage 2 consists of 16 values (0-13 being the coefficients, 14-15 are zeros)
// Note:  Stage 2 is symmetric about coefficient 13.  See the example filters for more information.
byte reg40 = (byte)(coeffs.Count == 128 ? 0 : 128);
for (int I = 0; I < coeffs.Count; i++)
{
    // stage 1 contains 128 coefficients, while stage 2 contains 16 coefficients
    registers.WriteRegister(40, (byte)(reg26 + i));

    // write the coefficient data
    registers.WriteRegister(41, (byte)(coeffs[i] & 0xff));
    registers.WriteRegister(42, (byte)((coeffs[i] >> 8) & 0xff));
    registers.WriteRegister(43, (byte)((coeffs[i] >> 16) & 0xff));

    registers.WriteRegister(44, 0x02);   // set the write enable bit
}
// disable the write enable bit when we're done
registers.WriteRegister(44, (byte)(setEvenBit ? 0x04 : 0x00));
```

OSF Bypass

The oversampling FIR filter can be bypassed using *bypass_osf* in Register 7: Filter Bandwidth and System Mute, sourcing data directly into the IIR filter. The audio input should be oversampled at 8 x fs rate when OSF is bypassed to have the same IIR filter bandwidth as PCM audio sampled at fs rate. For example, an external signal at 44.1kHz can be oversampled externally to 8 x 44.1kHz = 352.8kHz and then applied to the serial decoder in either I^2S or LJ format. The maximum sample rate that can be applied is 768kHz (8 x 96kHz).

DSD Filter

A DSD filter with cutoff at 47kHz scaled by fs/44100 is available. See DSD FILTER Characteristics for more information.

THD Compensation

THD Compensation can be used to minimize distortion from external PCB components and layout through the generation of inverse second and third harmonic components matching the target system distortion profile.

THD compensation can be enabled via *thd_enb* in Register 13: THD Compensation Bypass
The coefficient for manipulating second harmonic distortion is stored in Register 22-23: THD Compensation C2
The coefficient for manipulating third harmonic distortion is stored in Register 24-25: THD Compensation C3

Left and right channels use the same compensation coefficients.

Time Domain Jitter Eliminator and DPLL

By default, the DAC works in Jitter Eliminator mode allowing the audio interface timing to be asynchronous to MCLK. A DPLL constantly updates the FSR/MCLK ratio to calculate the true 32-bit timing of the incoming audio samples allowing the ESS patented Time Domain Jitter Eliminator to remove any distortion caused by jitter.

- The DPLL acquisition speed can be set by *lock_speed* in Register 10: Master Mode and Sync Configuration.
- The PCM/SPDIF DPLL bandwidth can be set via dpll_bw_serial in Register 12: ASRC/DPLL Bandwidth.
- The DSD DPLL bandwidth can be set via *dpll_bw_dsd* in Register 12: ASRC/DPLL Bandwidth.

For best performance, the DPLL bandwidth should be set to the minimum setting that will keep the DPLL reliably in lock.

Sample Rate Calculation

The raw sample rate (FSR) can be calculated from Register 66-69 (Read-Only): DPLL Number using the following formula:

$$\mathrm{FSR} = \frac{(\mathrm{dpll\_num} * \mathrm{MCLK})}{2^{32}}$$

Synchronous Mode (PCM mode only)

The DPLL can be bypassed if the incoming PCM audio is synchronous to MCLK with the relationship MCLK=128FSR. This can be enabled via *128fs_mode* in Register 10: Master Mode and Sync Configuration.

Standby Mode

For lowest power consumption the following should be performed to enter stand-by mode:

1. Shut down the amplifier portion of the chip with Register 32: Amplifier Mode
2. Pull RESETB low. This will:
    a. Shut off the DACs, oscillator and internal regulators.
    b. Force all digital I/O pins into tri-state mode
3. If XI is supplied externally, it should be stopped at a logic low level
4. Disable any power supplies connected to the chip

To resume from standby mode:

1. Enable all power supplies
2. Pull RESETB up
3. Reinitialize all registers

DVDD Supply

The ES9118 is equipped with a regulated DVDD supply powered from AVDD. The internal DVDD regulator should be decoupled to DGND with a capacitor that maintains a minimum value of 1μF at 1.2V over the target operating temperature range

FUNCTIONAL DESCRIPTION – AMPLIFIER AND SWITCH

Charge Pump

The ES9118 includes two charge pumps. The switches are sequence controlled to minimize pops and clicks. Both use the same 500kHz switching frequency so they do not interfere with audio signals and so no intermodulation frequencies are generated.

The main charge pump requires a 2.2µF low ESR ceramic flying capacitor across pins C1 and C2. This charge pump also requires a 22µF low ESR ceramic hold capacitor between PNEG to AGND_CP. The hold capacitor size may be reduced at the expense of reduced output power.

The auxiliary charge pump requires a 1µF ceramic flying capacitor across pins C1_SW and C2_SW as well as a 1µF (minimum) ceramic hold capacitor from PNEG_SW to AGND_CP.

Select capacitors with an Equivalent Series Resistance (ESR) of less than 100mΩ for optimum performance. Low-ESR ceramic capacitors minimize the output impedance of the charge pump. For best performance over the extended temperature range select capacitors with a minimum X5R dielectric, the X7R dielectric is preferred.

Compensation Components

For optimum performance, matching resistors and capacitors between OUT_L and INB_L, IN_L and GND_SN, OUT_R and INB_R, IN_R and GND_SN should be included in all configurations of the ES9118 to control the bandwidth of the headphone amplifier. These compensation capacitors should have a low temperature coefficient, NP0/C0G types are recommended.

Short-Circuit Protection

The ES9118 includes internal short-circuit protection. This feature is disabled by default.
The short circuit protection can be enabled using Register 21: GPIO Input Selection and Amp Over-Current Limit.

Output Switch

The output signal is selected by an ultra-low THD analog switch that connects either to the HiFi audio headphone amplifier or to an alternate audio source. A typical alternate source may be voice or low fidelity music.

Aux (LowFi) Mode

The ultra-low THD analog switch may be controlled using Register 32: Amplifier Mode. This allows audio to pass from an alternate source to the output. The digital section of the ES9118 remains powered on and ready for a quick transition back to HiFi mode. All supplies must be enabled.

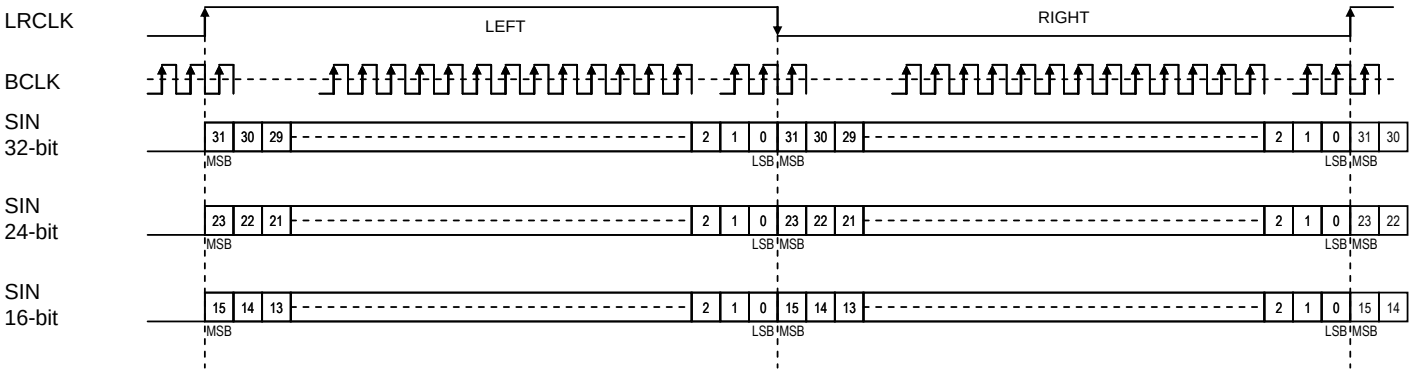
Low Power Bypass Mode

The ultra-low THD analog switch may be controlled using GPIO2 when the ES9118 is in standby. This allows audio to pass from an alternate source to the output without the use of the digital section of the ES9118. AVCC_HP and AVCC_CP supplies must be enabled.

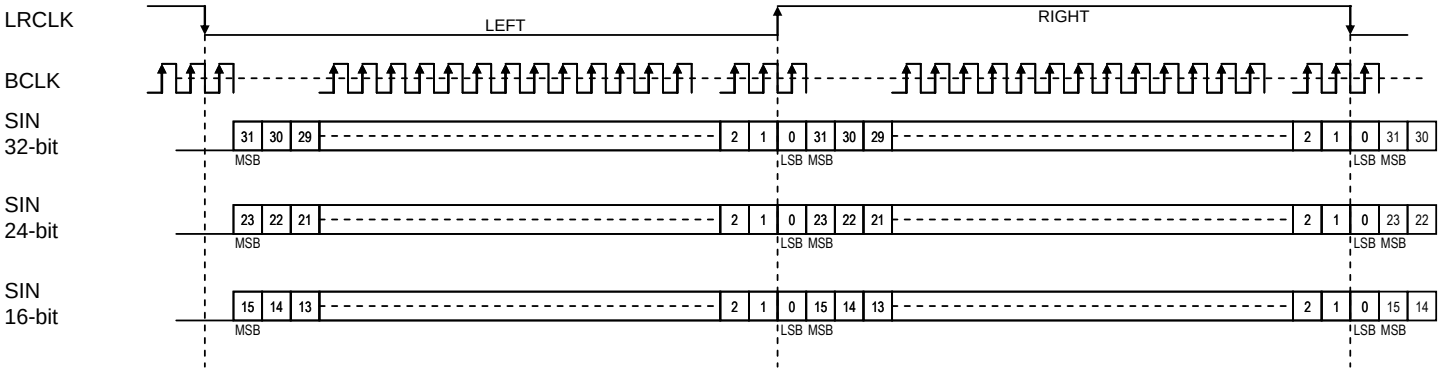
This mode is activated when RESETB = pulled down and GPIO2=pulled up.

AUDIO INTERFACE FORMATS

Several digital audio transport formats are supported to allow direct connection to common audio processors. The ES9118 includes autodetect circuitry (enabled by default) to detect the input format. The input mode can be explicitly set using Register 1: Input selection. The following diagrams outline the supported formats.



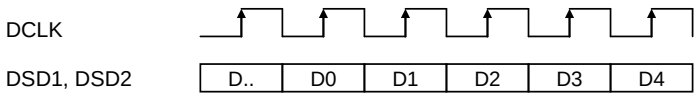
LEFT JUSTIFIED FORMAT



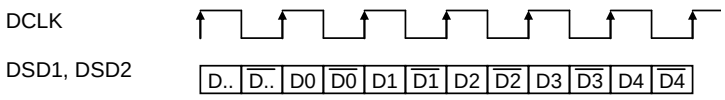
I2S FORMAT

For Left-Justified and I²S formats, the following number of BCLK edges are present per frame (left plus right):

- 16-bit mode: 32 BCLKs
- 24-bit mode: 48 BCLKs
- 32-bit mode: 64 BCLKs



DSD NORMAL MODE

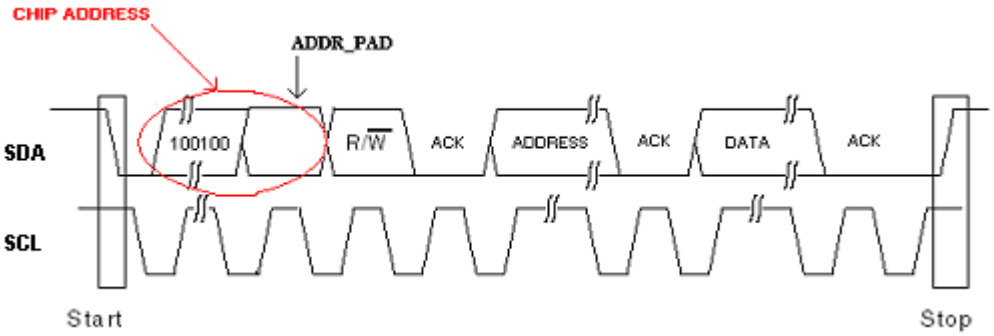


DSD PHASE MODE

SERIAL CONTROL INTERFACE

Registers are programmed via an I²C interface. The diagrams below outline the timing requirements for this interface. The chip address can be set to 2 different settings with the ADDR pin.

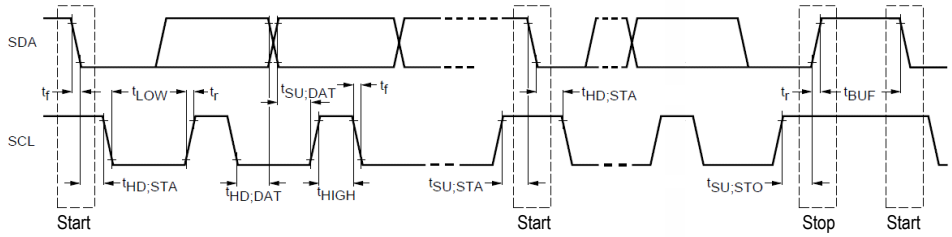
ADDR	CHIP ADDRESS
0	0x90
1	0x92



Notes:

1. The ADDR pin is used to set the chip I²C address.
2. The first byte after the *chip address* is the *register address*.
3. The second byte after the *chip address* is the register data to be programmed at the *register address*.
4. Multi-byte reads are NOT supported and will cause the I2C decoder to become unresponsive until a reset occurs.

I2C Timing Table



Parameter	Symbol	MCLK Constraint	Standard-Mode		Fast-Mode		Unit
			MIN	MAX	MIN	MAX	
SCL Clock Frequency	f_{SCL}	< MCLK/20	0	100	0	400	kHz
START condition hold time	$t_{HD,STA}$		4.0	-	0.6	-	µs
LOW period of SCL	t_{LOW}	>10/MCLK	4.7	-	1.3	-	µs
HIGH period of SCL (>10/MCLK)	t_{HIGH}	>10/MCLK	4.0	-	0.6	-	µs
START condition setup time (repeat)	$t_{SU,STA}$		4.7	-	0.6	-	µs
SDA hold time from SCL falling - All except NACK read - NACK read only	$t_{HD,DAT}$		0 2/MCLK	-	0 2/MCLK	-	µs s
SDA setup time from SCL rising	$t_{SU,DAT}$		250	-	100	-	ns
Rise time of SDA and SCL	t_r		-	1000		300	ns
Fall time of SDA and SCL	t_f		-	300		300	ns
STOP condition setup time	$t_{SU,STO}$		4	-	0.6	-	µs
Bus free time between transmissions	t_{BUF}		4.7	-	1.3	-	µs
Capacitive load for each bus line	C_b		-	400	-	400	pF

REGISTER MAP

Address (dec)	Register	Default (hex)	7	6	5	4	3	2	1	0
Read/Write										
0	**System Registers**	**00**	osc_drv				clk_gear		*reserved*	soft_reset
1	**Input Selection**	**CC**	serial_length		serial_mode		auto_select		input_select	
2	**Mixing, Serial Data and Automute Configuration**	**34**	automute_config		serial_bits		ch2_mix_sel		ch1_mix_sel	
3	**Reserved**	**40**	*reserved*							
4	**Automute Time**	**00**	automute_time							
5	**Automute Level**	**68**	*reserved*	automute_level						
6	**Volume Ramp Rate**	**02**	*reserved*					volume_rate		
7	**Filter Bandwidth and System Mute**	**80**	filter_shape			*reserved*	bypass_osf	*reserved*		mute
8	**GPIO1-2 Configuration**	**DD**	gpio2_cfg				gpio1_cfg			
9	**Reserved**	**22**	*reserved*							
10	**Master Mode and Sync Configuration**	**02**	master_mode	master_div		128fs_mode	lock_speed			
11	**Reserved**	**22**	*reserved*							
12	**ASRC/DPLL Bandwidth**	**5A**	dpll_bw_serial				dpll_bw_dsd			
13	**THD Compensation Bypass**	**40**	*reserved*	thd_enb	*reserved*					
14	**Soft Start Configuration**	**0A**	*reserved*	*reserved*	*reserved*	soft_start_time				
15	**Volume Control**	**50**	volume1							
16	**Volume Control**	**50**	volume2							
17	**Master Trim**	**FF**	master_trim							
18		**FF**								
19		**FF**								
20		**7F**								
21	**GPIO Input Selection and Amp Over-Current Limit**	**00**	gpio_sel2		gpio_sel1		amp_loop_pdb	amp_oc_en	amp_oc_limit	
22	**THD Compensation C2**	**00**	thd_comp_c2							
23		**00**								
24	**THD Compensation C3**	**00**	thd_comp_c3							
25		**00**								
26	**Charge Pump Soft Start Delay**	**62**	cp_ss_delay							
27	**General Configuration**	**D4**	asrc_en	*reserved*	*reserved*	*reserved*	ch1_volume	latch_vol	*reserved*	
28	**Reserved**	**F0**	*reserved*							
29	**GPIO Configuration and Band Gap**	**00**	invert_gpio		*reserved*		aref_tuneb	avcc_enb	fast_enb	abq_sel
30	**Charge Pump Clock**	**00**	cp_clk_sel		cp_clk_en		cp_clk_div			
31		**00**	cp_clk_div							
32	**Amplifier Mode**	**00**	amp_pdb_ss	ss_delay_enb	cp_ext_o	cp_ext_oe	amp_mode2		amp_mode1	
33	**Interrupt Mask**	**3C**	*reserved*		amp_limit_mask				automute_mask	lock_mask
34	**Programmable NCO**	**00**	nco_num							
35		**00**								
36		**00**								
37		**00**								
38	**Reserved**	**00**	*reserved*							
39	**Reserved**	***00***	*reserved*							
40	**Programmable FIR RAM Address**	**00**	prog_coeff_addr							
41	**Programmable FIR RAM Data**	**00**	prog_coeff_data							
42		**00**								
43		**00**								
44	**Programmable FIR Configuration**	**00**	*reserved*					stage2_even	prog_we	prog_en
45	**Reserved**	**00**	*reserved*							
46	**Reserved**	**00**	*reserved*							
Read Only										
64	**Chip ID and Active Status**	**C0**	chip_id						automute_status	lock_status
65	**GPIO Readback**	**00**	*reserved*						gpio2	gpio1
66	**DPLL Number**	**00**	dpll_num							
67		**00**								
68		**00**								
69		**00**								
70	**Reserved**	**00**	*reserved*							
71	**Reserved**	***00***	*reserved*							
72	**Input Selection and Automute Status**	**00**	oc_sd_mute		am2, am1		*reserved*		i2s_select	dsd_select
73	**RAM Coefficient Readback**	**00**	prog_coeff_out							
74		**00**								
75		**00**								
76	**Amp Status**	**00**	*reserved*				amp_plimit		amp_nlimit	

REGISTER DESCRIPTIONS

Register 0: System Registers

Bits	[7:4]	[3:2]	[1]	[0]
Mnemonic	osc_drv	clk_gear	reserved	soft_reset
Default	4'b0000	2'b00	1'b0	1'b0

Bit	Mnemonic	Description
[7:4]	osc_drv	Oscillator drive specifies the bias current to the oscillator pad. 4'b0000: full bias (default) 4'b1000: ¾ bias 4'b1100: ½ bias 4'b1110: ¼ bias 4'b1111: shut down the oscillator
[3:2]	clk_gear	Configures a clock divider network that can reduce the power consumption of the chip by reducing the clock frequency supplied to both the digital core and analog stages. 2'b00: MCLK = XI (default) 2'b01: MCLK = XI / 2 2'b10: MCLK = XI / 4 2'b11: MCLK = XI / 8
[1]	reserved	
[0]	soft_reset	Software configurable hardware reset with the ability to reset the design to its initial power-on configuration. 1'b0: normal operation (default) 1'b1: resets the ES9118 to its power-on defaults Note: This register will always read as "1'b0" as the power-on default for this register is "1'b0". A reset can be verified by checking the status of other modified registers.

Register 1: Input selection

Bits	[7:6]	[5:4]	[3:2]	[1:0]
Mnemonic	serial_length	serial_mode	auto_select	input_select
Default	2'b11	2'b00	2'b11	2'b00

Bit	Mnemonic	Description
[7:6]	serial_length	Selects how many DATA_CLK pulses exist per data word. 2'b00: 16-bit data words 2'b01: 24-bit data words 2'b10: 32-bit data words 2'b11: 32-bit data words (default)
[5:4]	serial_mode	Configures the type of serial data. 2'b00: I2S mode (default) 2'b01: left-justified mode 2'b11 or 2'b10: right-justified mode
[3:2]	auto_select	Allows the ES9118 to automatically select between either serial (I2S) or DSD input formats. 2'b00: disable automatic input decoder and instead use the information provided by register 1[1:0] 2'b01: automatically select between DSD or serial data 2'b10: reserved 2'b11: reserved
[1:0]	input_select	Configures the ES9118 to use a particular input decoder if auto_select is disabled. 2'b00: serial (default) 2'b11: DSD Note: Register 1[3:2] must be set to 2'b00 for input_select to function.

Register 2: Mixing, Serial Data and Automute Configuration

Bits	[7:6]	[5:4]	[3:2]	[1:0]
Mnemonic	automute_config	serial_bits	ch2_mix_sel	ch1_mix_sel
Default	2'b00	2'b11	2'b01	2'b00

Bit	Mnemonic	Description
[7:6]	automute config	Configures the automute state machine, which allows the ES9118 to perform different power saving and sound optimizations. 2'b00: normal operation (default) 2'b01: perform a mute when an automute condition is asserted 2'b10: ramp all channels to ground when an automute condition is asserted 2'b11: perform a mute and then ramp all channels to ground when an automute condition is asserted Note: Ramping DAC outputs to ground can reduce the power consumption of the ES9118 in some situations. Note: This process can be sped up by using the automute_time, volume_rate and soft_start_time registers.
[5:4]	serial_bits	Selects how many bits consist of a data word in the serial data stream. 2'b00: 16-bit data words 2'b01: 24-bit data words 2'b10: 32-bit data words 2'b11: 32-bit data words (default)
[3:2]	ch2_mix_sel	Selects which data is mapped to DAC 2. 2'b00: ch1 2'b01: ch2 (default) 2'b10: (ch1+ch2) 2'b11: (ch1+ch2)/2
[1:0]	ch1_mix_sel	Selects which data is mapped to DAC 1. 2'b00: ch1 (default) 2'b01: ch2 2'b10: (ch1+ch2) 2'b11: (ch1+ch2)/2

Register 3: Reserved

Bits	[7:4]	[3:0]
Mnemonic	reserved	reserved
Default	4'd4	4'd0

Register 4: Automute Time

Bits	[7:0]
Mnemonic	automute_time
Default	8'd0

Bit	Mnemonic	Description
[7]	automute time	Configures the amount of time the audio data must remain below the automute_level before an automute condition is flagged. Defaults to 0 which disables automute. $$\text{Time in seconds} = \frac{2096896}{\text{automute\_time} * \text{FSR}}$$

Register 5: Automute Level

Bits	[7]	[6:0]
Mnemonic	reserved	automute_level
Default	1'b0	7'd104

Bit	Mnemonic	Description
[7]	reserved	
[6:0]	automute level	Configures the threshold which the audio must be below before an automute condition is flagged. The level is measured in decibels (dB) and defaults to -104dB. Note: This register works in tandem with automute_time to create the automute condition.

Register 6: Volume Ramp Rate

Bits	[7:3]	[2:0]
Mnemonic	reserved	volume_rate
Default	5'b00000	2'b010

Bit	Mnemonic	Description
[7:3]	reserved	Reserved
[2:0]	volume_rate	Selects a volume ramp rate to use when transitioning between different volume levels. The volume ramp rate is measured in decibels per second (dB/s). $$\text{rate} = \frac{2^{\text{vol\_rate}} * \text{FSR}}{512} \text{ dB/s}$$

Register 7: Filter Bandwidth and System Mute

Bits	[7:5]	[4]	[3]	[2:1]	[0]
Mnemonic	filter_shape	reserved	bypass_osf	reserved	mute
Default	3'b100	1'b0	1'b0	2'b00	1'b0

Bit	Mnemonic	Description
[7:5]	filter_shape	Selects the type of filter to use during the 8x FIR interpolation phase. 3'b111: brick wall filter 3'b110: hybrid fast roll-off filter 3'b101: reserved 3'b100: apodizing fast roll-off filter (default) 3'b011: minimum phase slow roll-off filter 3'b010: minimum phase fast roll-off filter 3'b001: linear phase slow roll-off filter 3'b000: linear phase fast roll-off filter
[4]	reserved	
[3]	bypass_osf	Allows the use of an external 8x upsampling filter, bypassing the internal interpolating FIR filter. 1'b0: uses the built-in oversampling filter (default) 1'b1: uses an external upsampling filter, which requires data oversampled by 8x externally
[2:1]	reserved	
[0]	mute	Mutes all 2 channels of the ES9118. 1'b0: normal operation (default) 1'b1: mute both channels

GPIO Modes

The following table describes the supported values for **Error! Reference source not found.** gpio1_cfg or gpio2_cfg and their function.

gpioX_cfg	Name	I/O Direction	Details
4'd 0	Automute Status	Output	Output is high when an automute has been triggered. This signal is analogous to the automute_status register (register 64).
4'd 1	Lock Status	Output	Output is high when lock is triggered. This signal is analogous to the lock_status register (register 64).
4'd 2	Volume Min	Output	Output is high when all digital volume controls have been ramped to minus full scale. This can occur, for example, if automute is enabled and set to mute the volume.
4'd 3	CLK	Output	Output is a buffered MCLK signal which can be used to synchronize other devices.
4'd 4	Automute/Lock Interrupt	Output	Output is high when the contents of register 64 have been modified (meaning that the lock_status or automute_status register have been changed). Reading register 64 will clear this interrupt.
4'd 5	Reserved		
4'd 6	Reserved		
4'd 7	Output 1'b0	Output	Output is forced low
4'd 8	Standard Input	Input	Places the GPIO into a high impedance state, allowing the customer to provide a digital signal and then read that signal back via the I2C register 65.
4'd 9	Input Select	Input	Places the GPIO into a high impedance state and allows the customer to toggle the input selection between two modes using the GPIO. See register 15 for more information.
4'd 10	Mute All	Input	Places the GPIO into a high impedance state and allows the customer to force a mute condition by applying a logic high signal to the GPIO. When a logic low signal is applied the DAC will exhibit normal operation.
4'd11	Amp Mode Select	Input	Activates the amplifier mode set in Register 32: Amplifier Mode when the gpio is pulled up.
4'd12	Reserved		
4'd 13	Shut Down	Input	Shutdown all blocks except I2C when the gpio is pulled up
4'd 14	Soft Start Complete	Output	Output is high when the DAC output is ramped to ground. The DAC can be ramped to ground via an automute condition when appropriately programmed, or via register 14.
4'd 15	Output 1'b1	Output	Output is forced high

Register 8: GPIO1-2 Configuration

See GPIO Modes for all supported values.

Bits	[7:4]	[3:0]
Mnemonic	gpio2_cfg	gpio1_cfg
Default	4'd13	4'd13

Register 9: Reserved

Bits	[7:4]	[3:0]
Mnemonic	reserved	reserved
Default	4'd2	4'd2

Register 10: Master Mode and Sync Configuration

Bits	[7]	[6:5]	[4]	[3:0]
Mnemonic	master_mode	master_div	128fs_mode	lock_speed
Default	1'b0	2'b00	1'b0	4'd2

Bit	Mnemonic	Description
[7]	master_mode	Enables master mode which causes the ES9118 to drive the DATA_CLK and DATA1 signals when in I2S mode. Can also be enabled when in DSD mode to enable DATA_CLK only. 1'b0: disables master mode (default) 1'b1: enables master mode Note: The input selection type (reg#1[1:0]) must match the type of data that is being generated in master mode.
[6:5]	master_div	Sets DATA_CLK frequency when in master mode. This register is used when in normal synchronous operation. 2'b00: DATA_CLK frequency = MCLK/4 (default) 2'b01: DATA_CLK frequency = MCLK/8 2'b10: DATA_CLK frequency = MCLK/16 2'b11: DATA_CLK frequency = MCLK/32 Note: The input selection type (reg#1[1:0]) must match the type of data that is being generated in master mode.
[4]	128fs_mode	Enables operation of the DAC while in synchronous mode with a 128*FSR MCLK in PCM normal or OSF bypass mode only. 1'b0: disables MCLK = 128*FSR mode (default) 1'b1: enables MCLK = 128*FSR mode
[3:0]	lock_speed	Sets the number of audio samples required before the DPLL and ASRC lock to the incoming signal. More audio samples gives a better initial estimate of the MCLK/FSR ratio at the expense of a longer locking interval. 4'd0: 16384 FSL edges 4'd1: 8192 FSL edges 4'd2: 5461 FSL edges (default) 4'd3: 4096 FSL edges 4'd4: 3276 FSL edges 4'd5: 2730 FSL edges 4'd6: 2340 FSL edges 4'd7: 2048 FSL edges 4'd8: 1820 FSL edges 4'd9: 1638 FSL edges 4'd10: 1489 FSL edges 4'd11: 1365 FSL edges 4'd12: 1260 FSL edges 4'd13: 1170 FSL edges 4'd14: 1092 FSL edges 4'd15: 1024 FSL edges Note: FSL=FSR except in DSD Mode FSL=FSR*64

Register 11: Reserved

Bits	[7:0]
Mnemonic	reserved
Default	8'd0

Register 12: ASRC/DPLL Bandwidth

Bits	[7:4]	[3:0]
Mnemonic	dpll_bw_serial	dpll_bw_dsd
Default	4'd5	4'd10

Bit	Mnemonic	Description
[7:4]	dpll_bw_serial	Sets the bandwidth of the DPLL when operating in I2S mode. 4'd0: DPLL Off 4'd1: Lowest Bandwidth 4'd2: 4'd3: 4'd4: 4'd5: (default) 4'd6: 4'd7: 4'd8: 4'd9: 4'd10: 4'd11: 4'd12: 4'd13: 4'd14: 4'd15: Highest Bandwidth
[3:0]	dpll_bw_dsd	Sets the bandwidth of the DPLL when operating in DSD mode. 4'd0: DPLL Off 4'd1: Lowest Bandwidth 4'd2: 4'd3: 4'd4: 4'd5: 4'd6: 4'd7: 4'd8: 4'd9: 4'd10: (default) 4'd11: 4'd12: 4'd13: 4'd14: 4'd15: Highest Bandwidth

Register 13: THD Compensation Bypass

Bits	[7]	[6]	[5:0]
Mnemonic	reserved	thd_enb	reserved
Default	1'b0	1'b1	6'd0

Bit	Mnemonic	Description
[7]	reserved	
[6]	thd_enb	Selects whether to disable the THD compensation logic. THD compensation is enabled by default and can be configured to correct for second and third harmonic distortion. 1'b0: enable THD compensation (default) 1'b1: disable THD compensation
[5:0]	reserved	

Register 14: Soft Start Configuration

Bits	[7:6]	[4:0]
Mnemonic	reserved	soft_start_time
Default	3'b000	5'd10

Bit	Mnemonic	Description
[7:5]	reserved	
[4:0]	soft_start_time	Sets the amount of time that it takes to perform a soft start ramp. This time affects both ramp *down* to ground and ramp *up* to mute AVCC/2. Values from 0 to 20 are valid. $$\text{time (s)} = 4096 * \frac{2^{(\text{soft\_start\_time}+1)}}{\text{MCLK (Hz)}}$$

Register 15-16: Volume Control

Bits	[7:0]
Register 15	volume1
Register 16	volume2
Default	8'd80

Bit	Mnemonic	Description
[7:0]	volume1	Volume level setting for Ch1. Default of 8'd80 (-40dB) -0dB to -127.5dB with 0.5dB steps
[7:0]	volume2	Volume level setting for Ch2. Default of 8'd80 (-40dB) -0dB to -127.5dB with 0.5dB steps

Register 17-20: Master Trim

Bits	[31:0]
Mnemonic	master_trim
Default	32'h7fffffff

Bit	Mnemonic	Description
[31:0]	master_trim	A 32 bit signed value that sets the 0dB level for all volume controls. Defaults to full-scale (32'h7FFFFFFF).

Register 21: GPIO Input Selection and Amp Over-Current Limit

Bits	[7:6]	[5:4]	[3]	[2]	[1:0]
Mnemonic	gpio_sel2	gpio_sel1	reserved	amp_oc_en	amp_oc_limit
Default	2'b00	2'b00	1'b0	1'b0	2'b00

Bit	Mnemonic	Description
[7:6]	gpio_sel2	Selects which input type will be selected when GPIOX = 1'b1 2'd0: serial data (I2S/LJ) (default) 2'd3: DSD data
[5:4]	gpio_sel1	Selects which input type will be selected when GPIOX = 1'b0 2'd0: serial data (I2S/LJ) (default) 2'd3: DSD data
[3]	amp_loop_pd	Enables the amplifier overcurrent protection. ○ 1'b1: enables over current protection • Automatically limits the maximum peak current for either AVCC_HP or PNEG to 200mA. • This limit is not adjustable. ○ 1'b0: Disables overcurrent protection. (default) • (Warning this mode can damage the device if too much current is drawn)
[2]	amp_oc_en	Enables the amplifier overcurrent warning flags.
[1:0]	amp_oc_limit	Sets the current limit at which the overcurrent warning flags are set.

amp_oc_limit[1:0]	00		01/10		11	
(mA)	Limit ON	Limit OFF	Limit ON	Limit OFF	Limit ON	Limit OFF
Plimit	190	127	124	89	68	47
Nlimit	173	124	125	86	66	45

Limit ON: Triggers the flag.
Limit OFF: Clears the flag.

The overcurrent status can be monitored using Register 76 (Read-Only): Amp Status when amp_oc_en = 1.

Register 22-23: THD Compensation C2

Bits	[15:0]
Mnemonic	thd_comp_c2
Default	16'd0

Bit	Mnemonic	Description
[15:0]	thd_comp_c2	A 16-bit signed coefficient for correcting for the second harmonic distortion. Defaults to 16'd0.

Register 24-25: THD Compensation C3

Bits	[15:0]
Mnemonic	thd_comp_c3
Default	16'd0

Bit	Mnemonic	Description
[15:0]	thd_comp_c3	A 16-bit signed coefficient for correcting for the third harmonic distortion. Defaults to 16'd0.

Register 26: Charge Pump Soft Start Delay

Bits	[7:0]
Mnemonic	cp_ss_delay
Default	8'd98

Bit	Mnemonic	Description
[7:0]	cp_ss_delay	Configures the delay between the weak charge pump enable and the strong/medium charge pump enable. $$\text{delay}(s) = \frac{256 * \text{cps}_{\text{delay}}}{f_{\text{MCLK}}}$$

Register 27: General Configuration

Bits	[7]	[6-4]	[3]	[2]	[1:0]
Mnemonic	asrc_en	reserved	ch1_volume	latch_vol	reserved
Default	1'b1	3'b101	1'b0	1'b1	2'b00

Bit	Mnemonic	Description
[7]	asrc_en	Selects whether the ASRC is enabled. 1'b0: ASRC is disabled and the output from the THD compensation block is piped directly into the modulators. 1'b1: The ASRC is used as normal, providing a first order correction on the sample rate converted data.
[6]	reserved	
[5]	reserved	
[4]	reserved	
[3]	ch1_volume	Allows channel 2 to share the channel 1 volume control. This allows for perfectly syncing up the two channel gains. 1'b0: Allow independent control of both channel 1 and channel volume controls (default) 1'b1: Use the channel 1 volume control for both channel 1 and channel 2 This bit can only be used for PCM audio data, it cannot be used for DSD
[2]	latch_volume	Keeps the volume coefficients in synchronization with the programmed volume register. 1'b0: Disables updates of the internal volume coefficients (useful for updating each channel volume independently and then moving the volume coefficients in tandem) 1'b1: The internal volume coefficient is kept in synchronization with the volume registers
[1:0]	reserved	

Register 28: Reserved

Bits	[7:0]
Mnemonic	reserved
Default	8'd11110000

Bit	Mnemonic	Description
[7:0]	reserved	

Register 29: GPIO Configuration and Band Gap

Bits	[7:6]	[5]	[4]	[3]	[2]	[1]	[0]
Mnemonic	invert_gpio	amp_pdb_on_oc	reserved	aref_tuneb	avcc_enb	fast_enb	abq_sel
Default	2'b00	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bit	Mnemonic	Description
[7:6]	invert_gpio	Allows each GPIO output to be inverted independently. 2'b00: Normal GPIO operation (default) 2'b01: Invert GPIO1 output only 2'b10: Invert GPIO2 output only 2'b11: Invert both GPIO outputs
[5]	amp_pdb_on_oc	Powers down the amplifier stage when overcurrent is detected.
[4]	reserved	
[3]	aref_tuneb	aref_tuneb and abg_sel are used to configure the output of the reference of the analog regulator (ABG). abg_sel = 0, aref_tuneb = 0: ABG = 1.25V abg_sel = 0, aref_tuneb = 1: ABG = 1.3V abg_sel = 1, aref_tuneb = 0: ABG = 2.5V abg_sel = 1, aref_tuneb = 1: ABG = 2.6V
[2]	avcc_enb	Controls the ana_ref block which provides a voltage reference to the analog regulator and a current reference for the amplifier. These blocks are shut down in low power bypass, bypass and LowFi modes and this bit can be set to 1'b0 to save power. 1'b0: Shuts down the analog reference 1'b1: Enables the analog reference
[1]	fast_enb	Configures the fast charge capacitor 1'b0: Enable the fast charge capacitor 1'b1: Disable the fast charge capacitor
[0]	abq_sel	abg_sel and aref_tuneb are used together to configure the analog regulator. See the description of aref_tuneb (Register 29[3]) for more information.

Register 30-31: Charge Pump Clock

Bits	[15:14]	[13:12]	[11:0]
Mnemonic	cp_clk_sel	cp_clk_en	cp_clk_div
Default	2'b00	2'b00	12'd0

Bit	Mnemonic	Description
[15:14]	cp_clk_sel	Selects which clock will be used as the reference clock for the charge pump clock. 2'b00: f_{CLK} = XI (default) 2'b01: reserved 2'b10: reserved 2'b11: reserved
[13:12]	cp_clk_en	Sets the state of the charge pump clock. 2'b00: Tristate output (default) 2'b01: Tied to GND 2'b10: Tied to DVDD 2'b11: Active
[11:0]	cp_clk_div	Sets the divider ratio for the charge pump clock. f_{CLK} is the frequency of the clock selected by cp_clk_sel. $$f_{cp} = \frac{f_{CLK}}{cp\_clk\_div * 2}$$

Register 32: Amplifier Mode

Bits	[7]	[6]	[5]	[4]	[3:2]	[1:0]
Mnemonic	amp_pdb_ss	ss_delay_enb	cp_ext_o	cp_ext_oe	amp_mode2	amp_mode1
Default	1'b0	1'b0	1'b0	1'b0	2'b00	2'b00

Bit	Mnemonic	Description
[7]	amp_pdb_ss	Powers the amplifier stage down when the digital core ramps to ground. This is useful when powering down the amplifier when in automute mode. 1'b0: Amplifier PDB is controlled by the amp_mode (default) 1'b1: Shuts the amplifier down when the DAC is ramped to ground
[6]	ss_delay_enb	Allows the charge pump soft start delay to be bypassed. 1'b0: Soft start works normally for the charge pump (default) 1'b1: Disable the charge pump soft start, instantly enabling the strong and medium charge pumps when applicable
[5]	cp_ext_o	Controls the external charge pump signal.
[4]	cp_ext_oe	Controls the external charge pump output enable signal.
[3:2]	amp_mode2	Selects which amplifier mode is activated when an appropriately configured GPIO is pulled up. Set the desired GPIO pin to *Amp Mode Select* in Register 8: GPIO1-2 Configuration to use this feature. 2'b00: Amplifier Standby operation 2'b01: AUX Input Source 2'b11: Sabre DAC + Amplifier
[1:0]	amp_mode1	Selects the default amplifier mode. If a GPIO is not used to select the amp mode then this register will determine the active amp mode. The ES9118 powers up with the amplifier in standby mode, awaiting configuration via I^2C. The amplifier can then be configured to accept HiFi audio from the Sabre DAC or audio from an alternate analog signal source. 2'b00: Amplifier Standby operation 2'b01: AUX Input Source 2'b11: Sabre DAC + Amplifier

Register 33: Interrupt Mask

Bits	[7:6]	[5:2]	[1]	[0]
Mnemonic	reserved	amp_limit_mask	automute_mask	lock_mask
Default	2'b00	4'b1111	1'b0	1'b0

Bit	Mnemonic	Description
[7:6]	reserved	
[5:2]	amp_limit_mask	Masks the 4 read-only bits from the amplifier.
[1]	automute_mask	Masks the automute bit from flagging an interrupt.
[0]	lock_mask	Masks the lock status bit from flagging an interrupt.

Register 34-37: Programmable NCO

Bits	[31:0]
Mnemonic	nco_num
Default	32'd0

Bit	Mnemonic	Description
[31:0]	nco_num	An unsigned 32-bit quantity that provides the ratio between MCLK and DATA_CLK. This value can be used to generate arbitrary DATA_CLK frequencies in master mode. A value of 0 disables this operating mode. Note: Master mode must still be enabled for the Sabre to drive the DATA_CLK and DATA1 pins. You must also select either serial mode or DSD mode in the input_select register to determine whether DATA_CLK should be driven alone (DSD mode) or both DATA_CLK and DATA1 should be driven (serial mode). • 32'd0: disables NCO mode (default) • 32'd?: enables NCO mode Note: NCO is determined by the following equation $$\mathrm{FSR} = \frac{(\mathrm{nco\_num} * \mathrm{MCLK})}{2^{32}}$$

Register 38: Reserved

Bits	[7:0]
Mnemonic	reserved
Default	8'd0

Register 39: Reserved

Bits	[7:0]
Mnemonic	reserved
Default	8'd0

Register 40: Programmable FIR RAM Address

Bits	[7]	[6:0]
Mnemonic	prog_coeff_stage	prog_coeff_addr
Default	1'b0	7'd0

Bit	Mnemonic	Description
[7]	coeff_stage	Selects which stage of the filter to write. 1'b0: selects stage 1 of the oversampling filter (default) 1'b1: selects stage 2 of the oversampling filter
[6:0]	coeff_addr	Selects the coefficient address when writing custom coefficients for the oversampling filter.

Register 41-43: Programmable FIR RAM Data

Bits	[23:0]
Mnemonic	prog_coeff_data
Default	24'd0

Bit	Mnemonic	Description
[23:0]	coeff_data	A 24bit signed filter coefficient that will be written to the address defined in prog_coeff_addr.

Register 44: Programmable FIR Configuration

Bits	[7:3]	[2]	[1]	[0]
Mnemonic	reserved	stage2_even	prog_we	prog_en
Default	5'b00000	1'b0	1'b0	1'b0

Bit	Mnemonic	Description
[7:3]	reserved	
[2]	stage2_even	Selects the symmetry of the stage 2 oversampling filter. 1'b0: Uses a sine symmetric filter (27 coefficients) (default) 1'b1: Uses a cosine symmetric filter (28 coefficients)
[1]	prog_we	Enables writing to the programmable coefficient RAM. 1'b0: Disables write signal to the coefficient RAM (default) 1'b1: Enables write signal to the coefficient RAM
[0]	prog_en	Enables the custom oversampling filter coefficients. 1'b0: Uses a built-in filter selected by filter_shape (default) 1'b1: Uses the coefficients programmed via prog_coeff_data

Register 45: Reserved

Bits	[7:0]
Mnemonic	reserved
Default	8'd0

Register 46: Reserved

Bits	[7:0]
Mnemonic	reserved
Default	8'd0

Register 64 (Read-Only): Chip ID and Status

Bits	[7:2]	[1]	[0]
Mnemonic	chip_id	automute_status	lock_status
Default	6'b110000	1'b0	1'b0

Bit	Mnemonic	Description
[7:2]	chip_id	6'b110000: ES9118
[1]	automute_status	Indicator for when automute has become active. 1'b0: Automute condition is inactive. 1'b1: Automute condition has been flagged and is active.
[0]	lock_status	Indicator for when the DPLL is locked (when in slave mode) or 1'b1 when the ES9118 is the master. 1'b0: DPLL is not locked to the incoming audio sample rate (which could mean that no audio input is present, the lock has not completed, or the Sabre is unable to lock due to clock jitter or drift). 1'b1: DPLL is locked to the incoming audio sample rate, or the Sabre is in master mode or 128*fs mode.

Register 65 (Read-Only): GPIO Readback

Bits	[7:2]	[1]	[0]
Mnemonic	reserved	gpio2	gpio1
Default	4'd0	1'b0	1'b0

Bit	Mnemonic	Description
[7:2]	Reserved	
[1]	gpio2	Contains the state of the GPIO2 pin.
[0]	gpio1	Contains the state of the GPIO1 pin.

Register 66-69 (Read-Only): DPLL Number

Bits	[31:0]
Mnemonic	dpll_num
Default	32'd0

Bit	Mnemonic	Description
[31:0]	dpll_num	Contains the ratio between the MCLK and the audio clock rate once the DPLL has acquired lock. This value is latched on reading the LSB, so register 66 must be read first to acquire the latest DPLL value. The value is latched on LSB because the DPLL number can be changing as the I²C transactions are performed. $$\mathrm{FSR} = \frac{(\mathrm{dpll\_num} * \mathrm{MCLK})}{2^{32}}$$

Registers 70 (Read-Only): Reserved

Bits	[7:0]
Mnemonic	reserved
Default	8'd0

Register 71 (Read-Only): Reserved

Bits	[7:0]
Mnemonic	reserved
Default	8'd0

Register 72 (Read-Only): Input Selection and Automute Status

Bits	[7:6]	[5:4]	[3:2]	[1]	[0]
Mnemonic	reserved	am2, am1	reserved	i2s_select	dsd_select
Default	2'b00	2'b00	2'd0	1'b0	1'b0

Bit	Mnemonic	Description
[7:6]	oc_sd_mute	Per channel indicator of whether an overcurrent condition has been detected. An overcurrent condition will result in the signal on that channel being digitally muted.
[5:4]	automute_status	Per channel indicator of whether an automute condition has been detected. 2'b00: No automute condition on either channel 2'b01: Data channel 1 has triggered an automute condition 2'b10: Data channel 2 has triggered an automute condition 2'b11: Both data channels have triggered an automute condition
[3:2]	reserved	
[1]	i2s_select	Contains the status of the I2S decoder. 1'b0: The I2S decoder has not found a valid frame clock or bit clock. 1'b1: The I2S decoder has detected a valid frame clock and bit clock arrangement.
[0]	dsd_select	Contains the status of the DSD decoder. 1'b0: The DSD decoder is not being used. 1'b1: The DSD decoder is being used as a fallback option if I2S has failed to decode their respective input signals.

Register 73-75 (Read-Only): Reserved

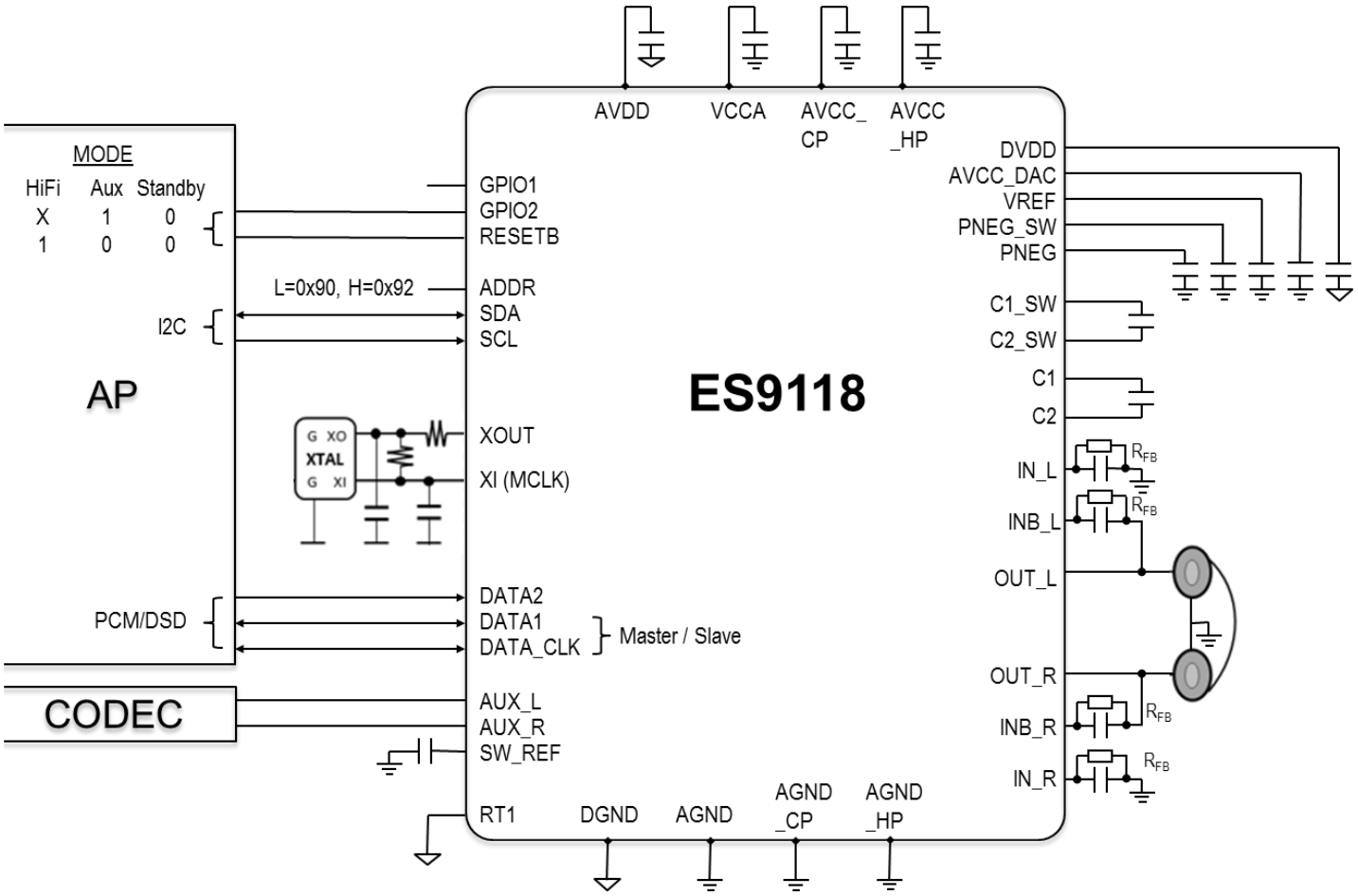
Bits	[7:0]
Mnemonic	reserved
Default	8'd0

Register 76 (Read-Only): Amp Status

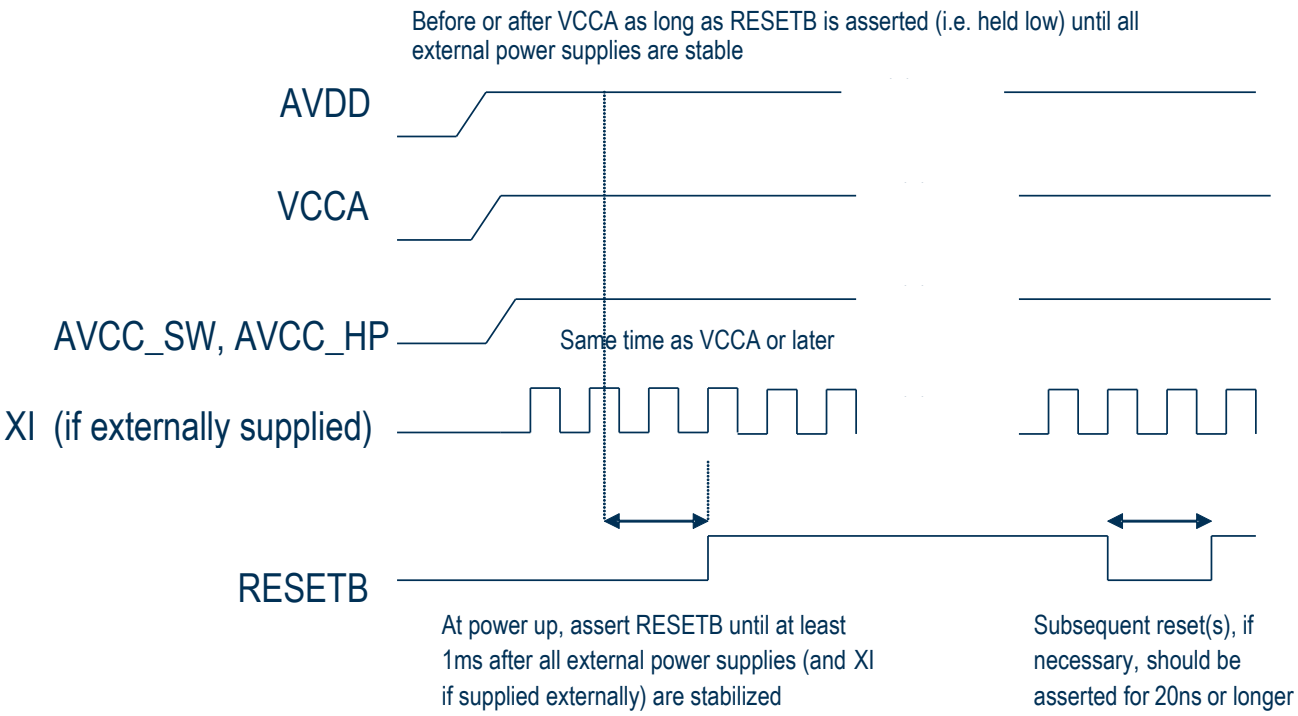
Bits	[7:4]	[3:2]	[1:0]
Mnemonic	reserved	amp_plimit	amp_nlimit
Default	4'b0000	2'b00	2'b00

Bit	Mnemonic	Description
[7:4]	reserved	
[3:2]	amp_plimit	Status of the P-side MOSFETs of the amplifier. • 2'b00: Neither Right Channel or Left Channel Limit Set • 2'b01: Left Channel Flag set • 2'b10: Right Channel Flag Set • 2'b11: Both Channel Flags Set
[1:0]	amp_nlimit	Status of the N-side MOSFETs of the amplifier. • 2'b00: Neither Right Channel or Left Channel Limit Set • 2'b01: Left Channel Flag set • 2'b10: Right Channel Flag Set • 2'b11: Both Channel Flags Set

APPLICATION DIAGRAM



RECOMMENDED POWER UP SEQUENCE



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING
Positive Supply Voltage • AVDD, VCCA • AVCC_HP, AVCC_CP • DVDD	 +4.7V with respect to GND +2.7V with respect to GND +1.8V with respect to GND
Negative Supply Voltage (PNEG & PNEG_SW)	–2.7V with respect to GND
Output Short-Circuit to GND (OUT_L, OUT_R)	Continuous
Storage temperature	–65°C to +150°C
Operating Junction Temperature	+125°C
Voltage range for digital input pins	–0.3V to AVDD+ 0.3V
ESD Protection Human Body Model (HBM) Charged Device Model (CDM)	 2000V 500V

WARNING: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

WARNING: Electrostatic Discharge (ESD) can damage this device. Proper procedures must be followed to avoid ESD when handling this device.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL		CONDITIONS
Operating temperature	T_A		–20°C to +70°C

Power Supply	Symbol	Voltage	Nominal current / power consumption		
			HiFi Mode RESETB=1 (Note 1)	Aux Mode RESETB=0 GPIO2=1	Standby Mode RESETB=0 GPIO2=0
Internally generated supplies (Note 2)	DVDD AVCC_DAC PNEG PNEG_SW	+1.2V ±5% +1.25, 1.3, 2.5 or 2.6V ±5% -1.8V ±5% -1.8V ±5%	Internally supplied		
Low power systems: VCCA=1.8V, AVCC_DAC=1.25V					
Analog core	VCCA	+1.8V ±5%	4.3 mA	TBD	TBD
Analog power	AVCC_HP, AVCC_CP	+1.8V ±5%	6.7 mA	300 uA	TBD
Digital power	AVDD	+1.8V ±5%	6.6 mA	TBD	TBD
Total power			32 mW	TBD <1 mW	TBD <1 mW
High performance systems: VCCA=3.3V, AVCC_DAC=2.5V					
Analog core	VCCA	+3.3 ±5%	8.1 mA	TBD	TBD
Analog power	AVCC_HP AVCC_CP	+1.8V ±5%	7.9 mA	300 uA	TBD
Digital power	AVDD	+1.8V ±5%	6.6 mA	TBD	TBD
Total power			53 mW	TBD <1 mW	TBD <1 mW

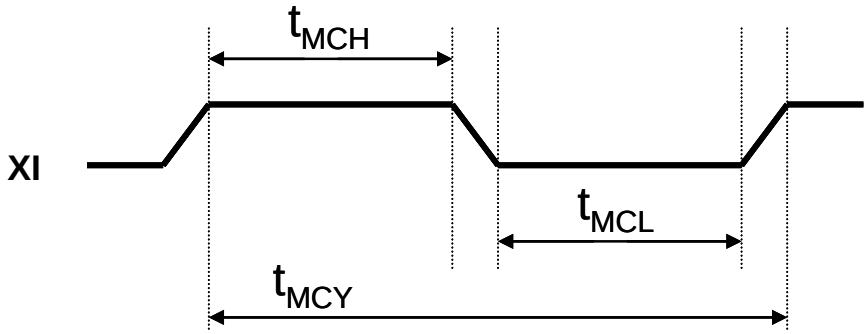
Notes:

1) fs = 44.1kHz, external XI=38MHz, MCLK=9.5MHz, I²S input, output unloaded, all external supply voltages at nominal values.
2) 2.5 or 2.6V AVCC_DAC is available with VCCA=3.3V.

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	MINIMUM	MAXIMUM	UNIT	COMMENTS
High-level input voltage	VIH	DVCC / 2 + 0.4		V	
Low-level input voltage	VIL		0.4	V	
High-level output voltage	VOH	DVCC – 0.2		V	IOH = 100μA
Low-level output voltage	VOL		0.2	V	IOL = 100μA

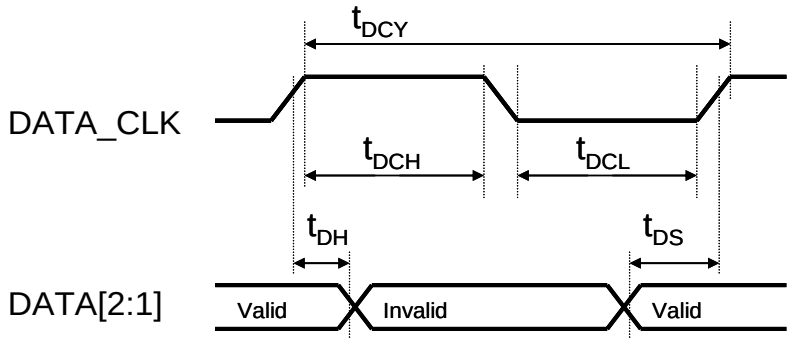
XI TIMING



Parameter	Symbol	Min	Max	Unit
XI pulse width high	T_{MCH}	9		ns
XI pulse width low	T_{MCL}	9		ns
XI cycle time	T_{MCY}	20		ns
XI duty cycle		45:55	55:45	

Based on timing requirements, the maximum supported XI frequency is 50MHz.

AUDIO INTERFACE TIMING



Parameter	Symbol	Min	Max	Unit
DATA_CLK pulse width high	t_{DCH}	9		ns
DATA_CLK pulse width low	t_{DCL}	9		ns
DATA_CLK cycle time	t_{DCY}	20		ns
DATA_CLK duty cycle		45:55	55:45	
DATA set-up time to DATA_CLK rising edge	t_{DS}	4.1		ns
DATA hold time to DATA_CLK rising edge	t_{DH}	2		ns

Notes:

- Audio data on DATA1 and DATA2 are sampled at the rising edges of DATA_CLK and must satisfy the setup and hold time requirements relative to the rising edge of DATA_CLK
- For DSD Phase mode, the normal data (D0, D1, D2... on p.10) must satisfy the setup and hold time requirements relative to the rising edge of DATA_CLK. The complimentary data ($\overline{D0}$, $\overline{D1}$, etc.) will be ignored.

ANALOG PERFORMANCE

Test Conditions (unless otherwise stated)

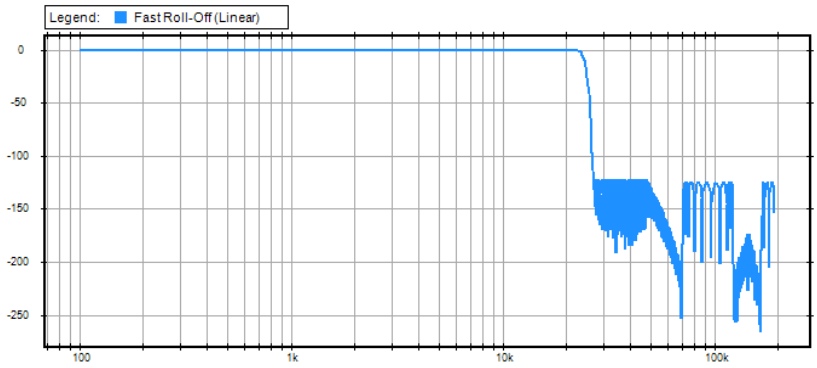
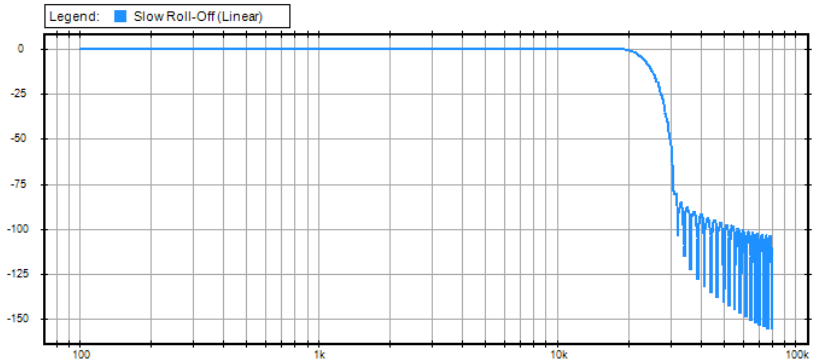
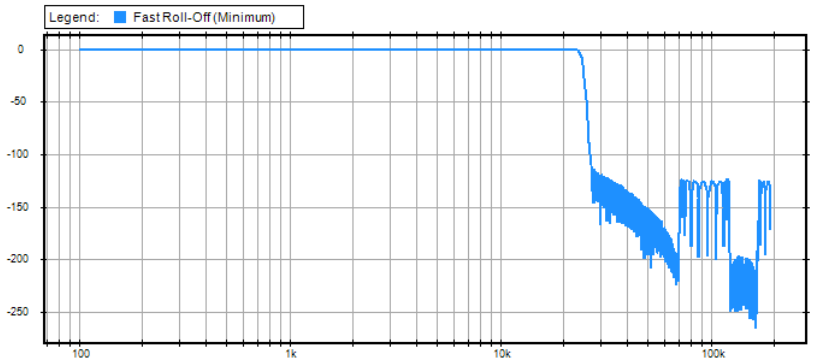
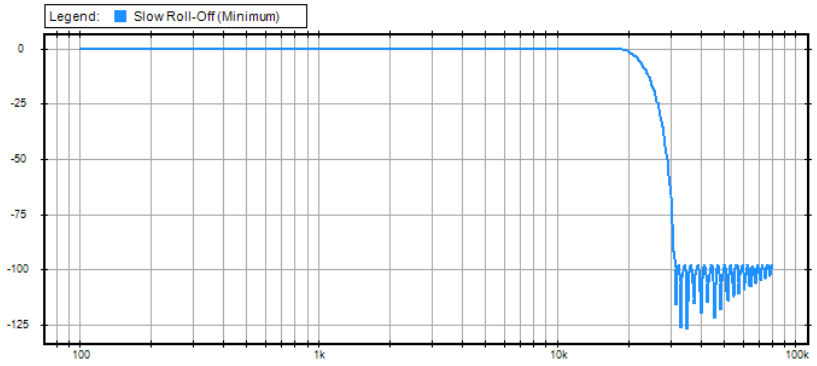
1. T_A = 25ºC, VCCA=AVDD=3.3V, AVCC_CP=AVCC_HP=1.8V, AVCC_DAC=2.5V, R_{FB}=500Ω
2. fs = 44.1kHz, MCLK = 27MHz, 32-bit data
3. SNR/DNR: A-weighted over 20Hz-20kHz in averaging mode
   THD+N: un-weighted over 20Hz-20kHz bandwidth

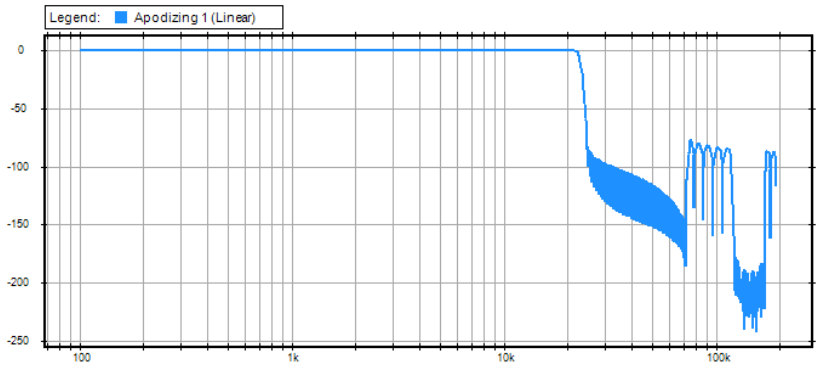
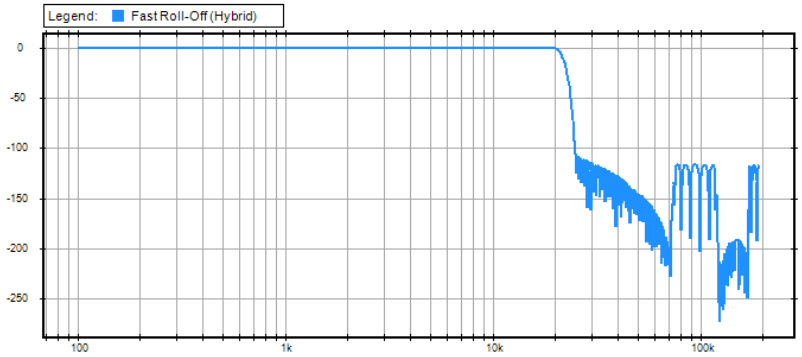
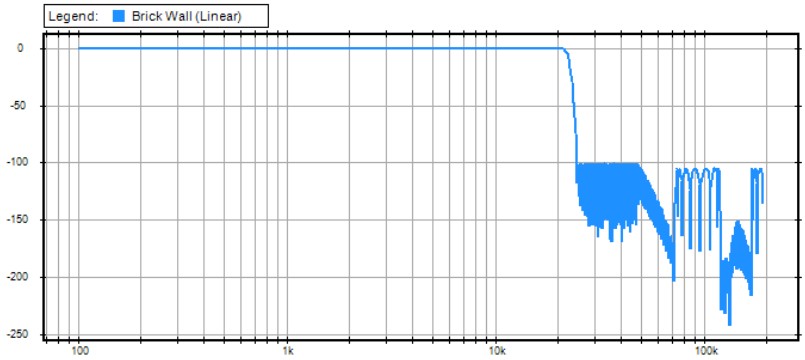
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
Resolution				32		Bits
XI Frequency					50M	Hz
MCLK (PCM normal mode)		Custom FIR mode Asynchronous mode Synchronous mode	256FSR 192FSR 128FSR		$\frac{XI}{2^{clk\_gear}}$	Hz
MCLK (PCM OSF bypass mode)		Asynchronous mode Synchronous mode	24FSR 16FSR			
MCLK (DSD mode)		Asynchronous mode Synchronous mode	3FSR 2FSR			
FSR (PCM normal mode)		Asynchronous mode Synchronous mode			192k 384k	Hz
FSR (PCM OSF bypass mode)					768k	Hz
FSR (DSD mode)		Asynchronous mode Synchronous mode			5.6M 11.3M	Hz
DYNAMIC PERFORMANCE (digital input to headphone amplifier output)						
Full Scale Output		0dBFS into 600Ω		1.1		Vrms
SNR		Zero input		125		dB-A
DNR		–60dBFS		120		dB-A
THD+N		1.1Vrms into 600Ω		–112		dB
THD+N		15mW into 32Ω		–105		dB
OUTPUT AMPLIFIER						
Output offset voltage		OUT_L & AGND_HP, OUT_R & AGND_HP. DAC outputs at mid-supply	–2.0	0.1	+2.0	mV
AUXILIARY ANALOG INPUTS						
Input voltage					1.0	Vrms
Digital Filter Performance						
Mute Attenuation				127		dB
PCM Filter Characteristics (Linear Phase Fast Roll Off)						
Pass band		±0.002dB			0.453 x fs	Hz
		–3dB			0.484 x fs	Hz
Stop band		< –120dB	0.55 x fs			Hz
Group Delay				35 / fs		s
PCM Filter Characteristics (Linear Phase Slow Roll Off)						
Pass band		±0.01dB			0.357 x fs	Hz
		–3dB			0.450 x fs	Hz
Stop band		< –82dB	0.639 x fs			Hz
Group Delay				8.75 / fs		s

PCM Filter Characteristics (Minimum Phase Fast Roll Off)						
Pass band		±0.005dB			0.453 x fs	Hz
		–3dB			0.491 x fs	Hz
Stop band		< –100dB	0.547 x fs			Hz
Group Delay				5.4 / fs		s
PCM Filter Characteristics (Minimum Phase Slow Roll Off)						
Pass band		±0.015dB			0.363 x fs	Hz
		–3dB			0.435 x fs	Hz
Stop band		< -97dB	0.634 x fs			Hz
Group Delay				3.5 / fs		s
PCM Filter Characteristics (Apodizing Fast Roll Off)						
Pass band		±0.075dB			0.409 x fs	Hz
		–3dB			0.461 x fs	Hz
Stop band		< -80dB < -100dB	0.5 x fs 0.66 x fs			Hz
Group Delay				35 / fs		s
PCM Filter Characteristics (Hybrid Fast Roll Off)						
Pass band		±0.01dB			0.404 x fs	Hz
		–3dB			0.430 x fs	Hz
Stop band		< -94.5dB < -106dB	0.504 x fs 0.513 x fs			Hz
Group Delay				18.5 / fs		s
PCM Filter Characteristics (Brick Wall)						
Pass band		±0.015dB			0.435 x fs	Hz
		–3dB			0.451 x fs	Hz
Stop band		< -100dB	0.5 x s			Hz
Group Delay				35 / fs		s

PCM FILTER CHARACTERISTICS

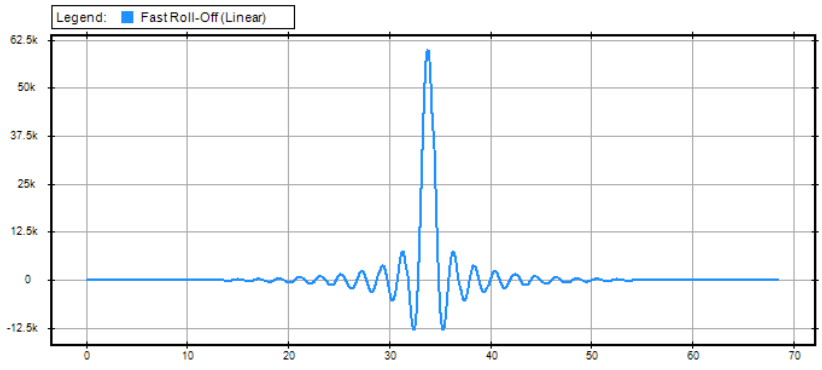
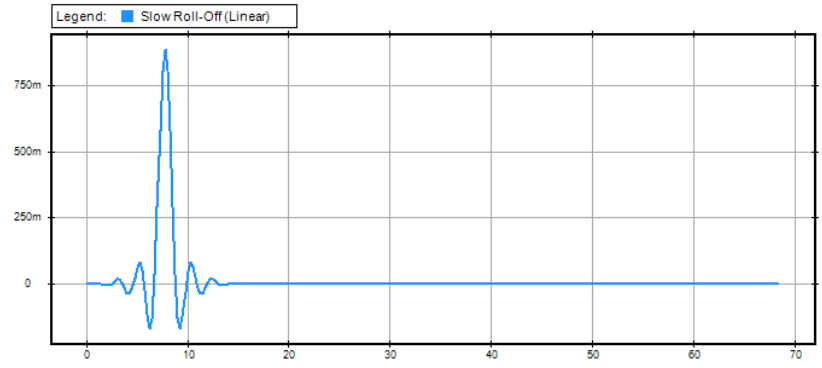
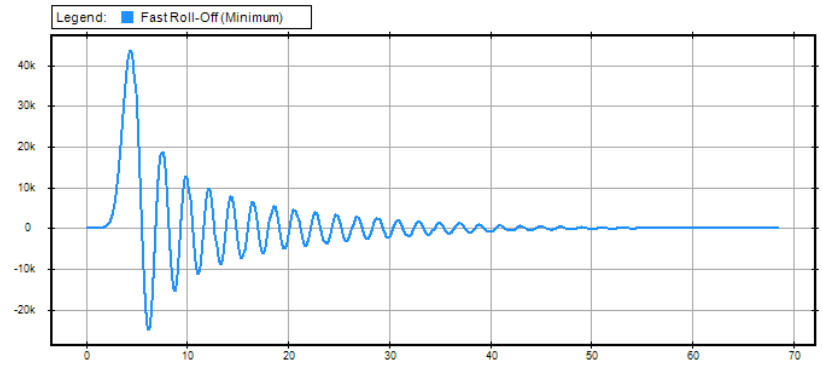
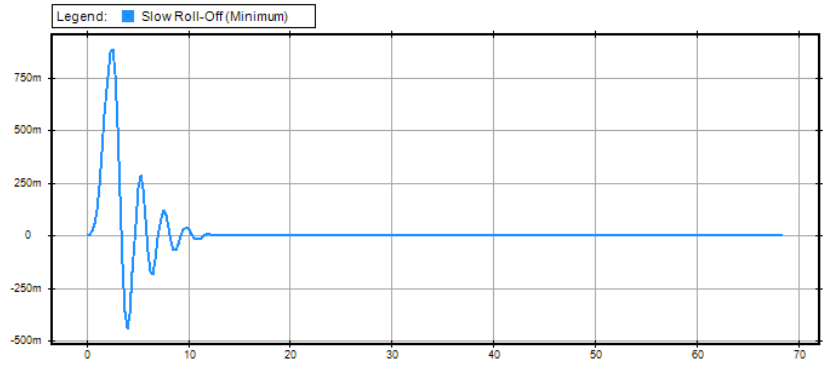
PCM Filter Frequency Responses

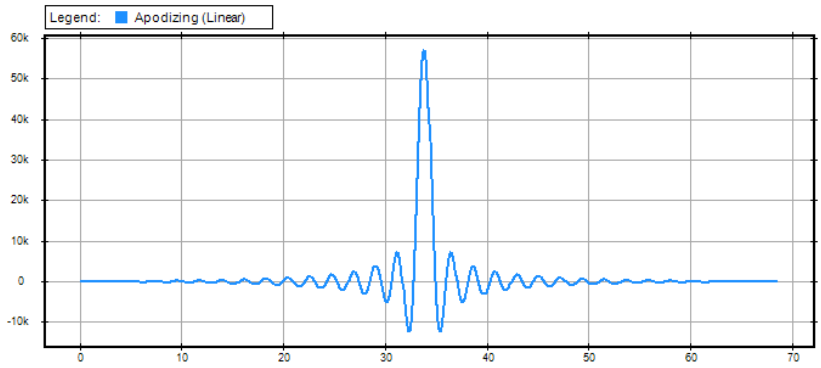
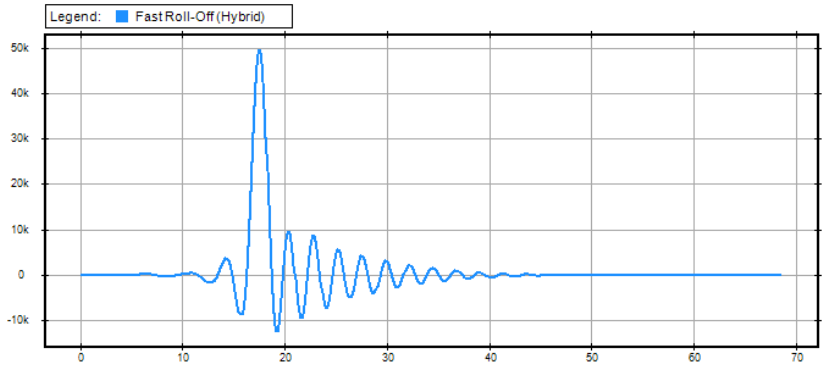
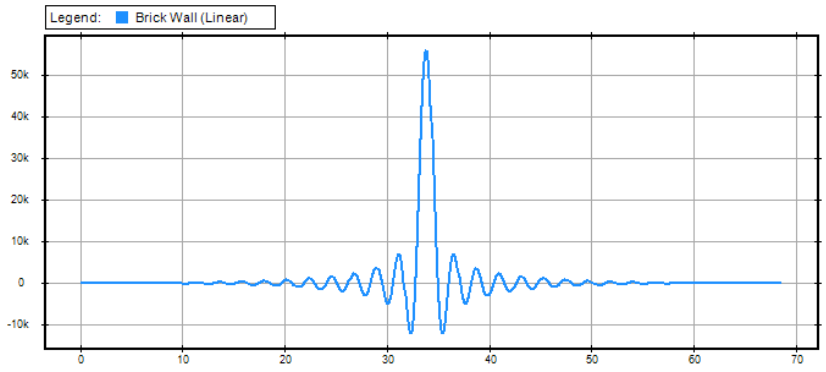
Linear phase fast roll-off filter (dB)	
Linear phase slow roll-off filter (dB)	
Minimum phase fast roll-off filter (dB)	
Minimum phase slow roll-off filter (dB)	

Apodizing fast roll-off filter (default, dB)	
Hybrid fast roll-off filter (dB)	
Brick wall filter (dB)	

Unit: fs (Hz) / 48000

PCM Filter Impulse Responses

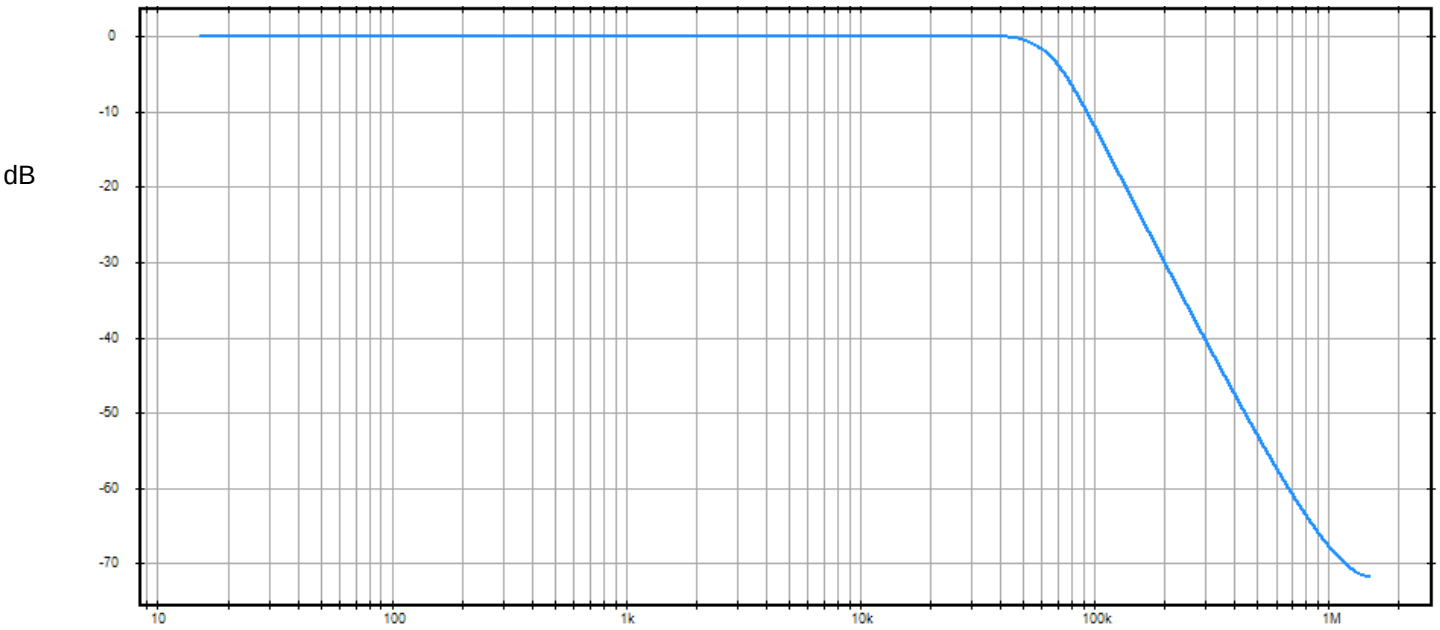
Linear phase fast roll-off filter	
Linear phase slow roll-off filter	
Minimum phase fast roll-off filter	
minimum phase slow roll-off filter	

Apodizing fast roll-off filter (default)	
Hybrid fast roll-off filter	
Brick wall filter	

Unit: 1/fs (s)

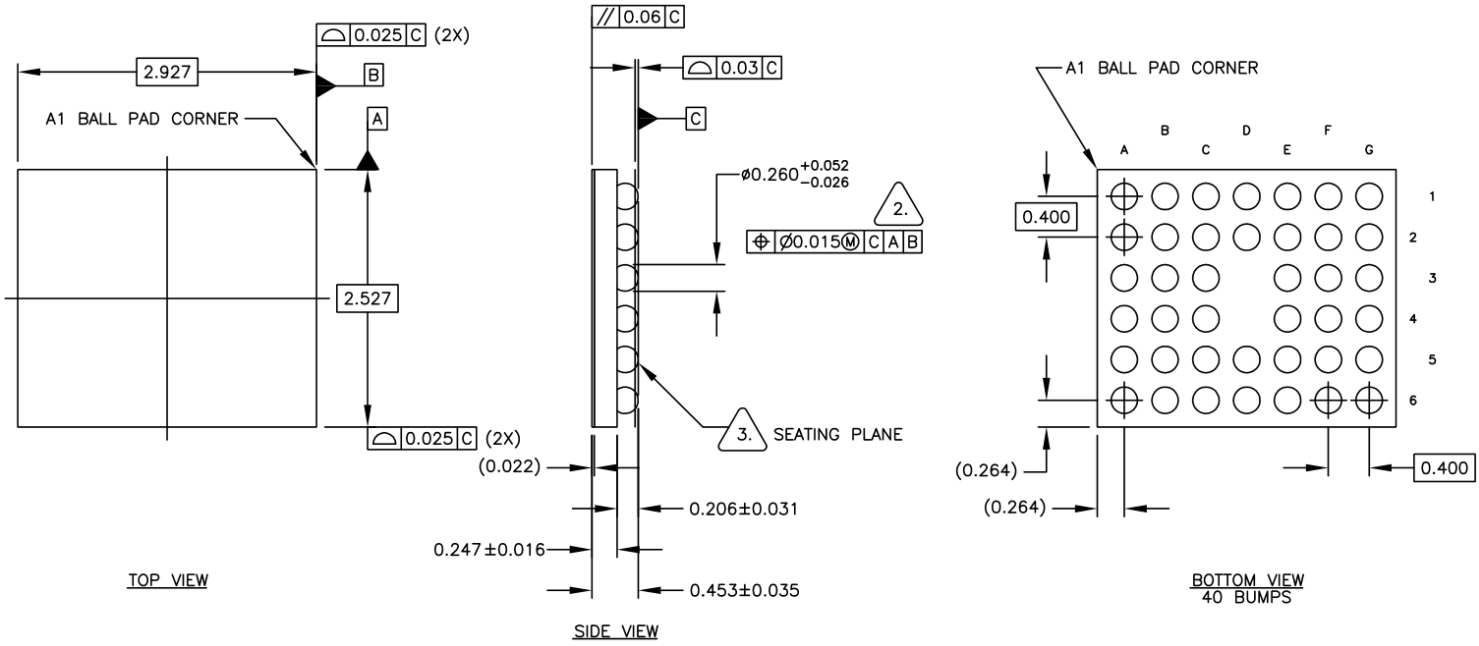
DSD FILTER CHARACTERISTICS

DSD Filter Frequency Response



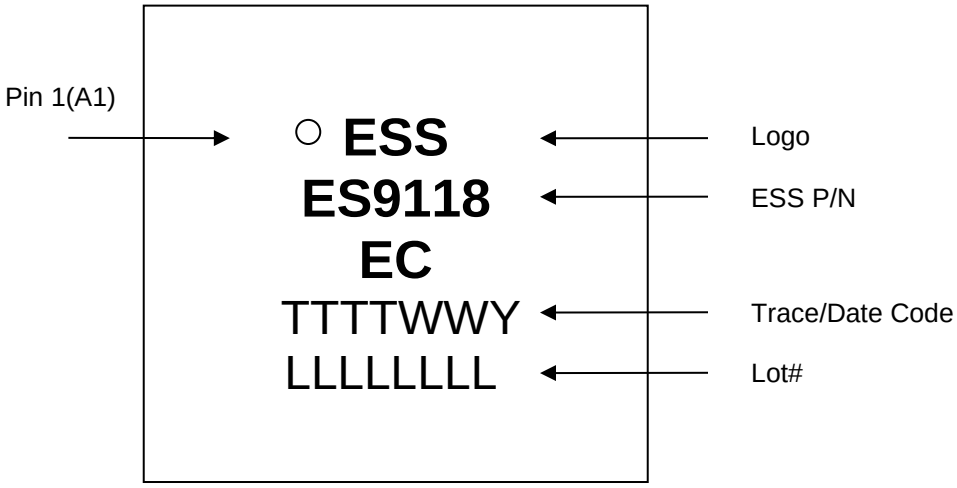
Unit: DATA_CLK (Hz) / 2822400

40-BALL CSP MECHANICAL DIMENSIONS



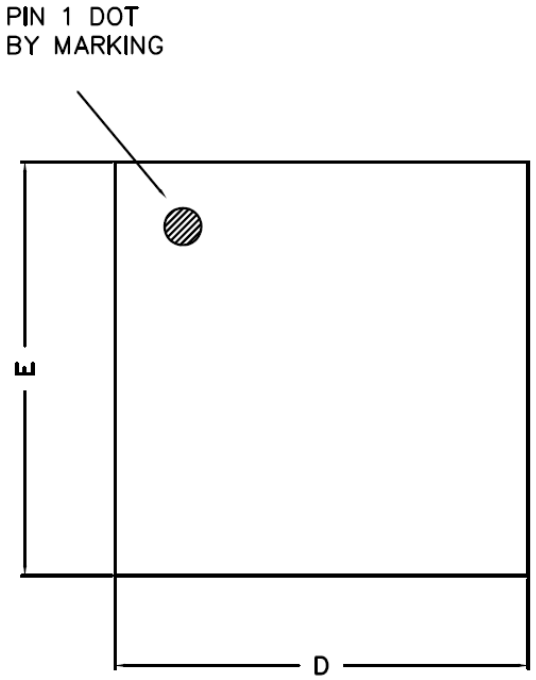
	(mm)		
	MIN	NOM	MAX
Package Body Dimension D(A)	2.502	2.527	2.552
Package Body Dimension E(B)	2.902	2.927	2.952
Package Height	0.418	0.453	0.488
Ball Height	0.175	0.206	0.237
Package Body Thickness	0.231	0.247	0.263
Ball Dimension	0.234	0.26	0.312
Ball Pitch E		0.4	
Ball Pitch D		0.4	
Total Ball Count		40	

40-BALL CSP TOP VIEW MARKING

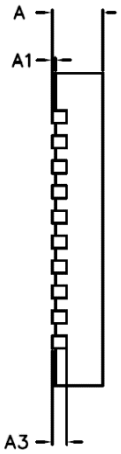


Marking is subject to change. This drawing is not to scale.

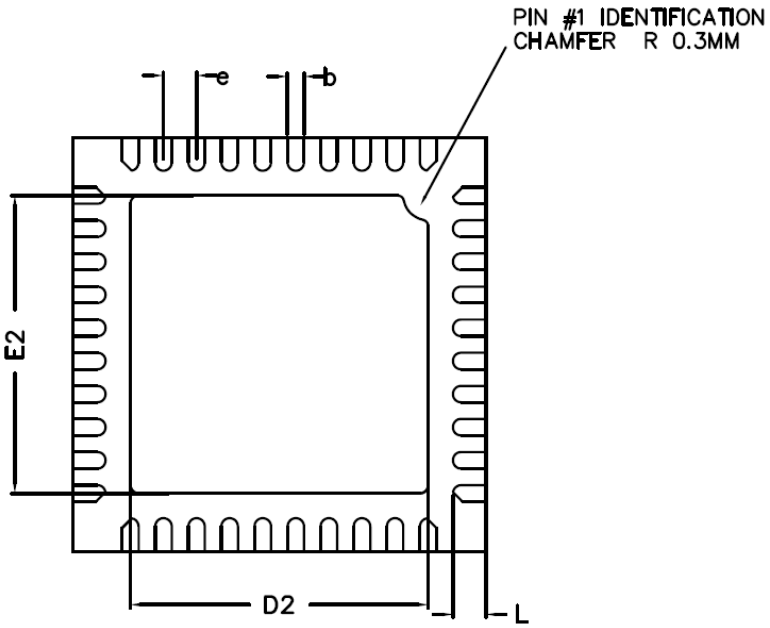
40-PIN QFN MECHANICAL DIMENSIONS



Top View



Side View



Bottom View

COMMON DIMENSIONS (mm)			
PKG.	W: VERY VERY THIN		
REF.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	-	0.05
A3	0.2 REF.		
D	4.95	5.00	5.05
E	4.95	5.00	5.05
b	0.15	0.20	0.25
L	0.30	0.40	0.50
D2	3.45	3.60	3.70
E2	3.45	3.60	3.70
e	0.4 BSC		

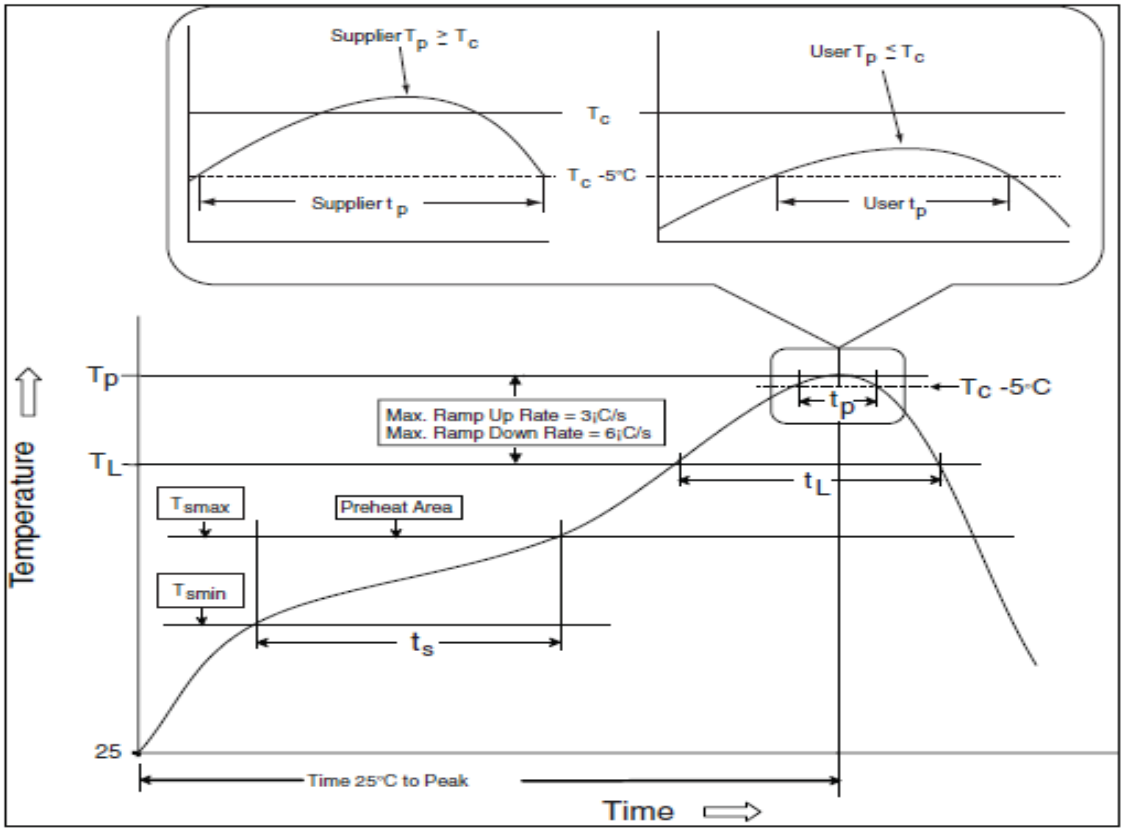
Package Dimensions

REFLOW PROCESS CONSIDERATIONS

For lead-free soldering, the characterization and optimization of the reflow process is the most important factor you need to consider.
The lead-free alloy solder has a melting point of 217°C. This alloy requires a minimum reflow temperature of 235°C to ensure good wetting. The maximum reflow temperature is in the 245°C to 260°C range, depending on the package size *(Table RPC-2)*. This narrows the process window for lead-free soldering to 10°C to 20°C.
The increase in peak reflow temperature in combination with the narrow process window makes the development of an optimal reflow profile a critical factor for ensuring a successful lead-free assembly process. The major factors contributing to the development of an optimal thermal profile are the size and weight of the assembly, the density of the components, the mix of large and small components, and the paste chemistry being used.
Reflow profiling needs to be performed by attaching calibrated thermocouples well adhered to the device as well as other critical locations on the board to ensure that all components are heated to temperatures above the minimum reflow temperatures and that smaller components do not exceed the maximum temperature limits *(Table RPC-2)*.

To ensure that all packages can be successfully and reliably assembled, the reflow profiles studied and recommended by ESS are based on the JEDEC/IPC standard J-STD-020 revision D.1.

Figure RPC-1. IR/Convection Reflow Profile (IPC/JEDEC J-STD-020D.1)



Note: Reflow is allowed 3 times. Caution must be taken to ensure time between re-flow runs does not exceed the allowed time by the moisture sensitivity label. If the time elapsed between the re-flows exceeds the moisture sensitivity time bake the board according to the moisture sensitivity label instructions.

Manual

Allowed up to 2 times with maximum temperature of 350ºC no longer than 3 seconds.

Table RPC-1 Classification reflow profile

Profile Feature	Pb-Free Assembly
Preheat/Soak Temperature Min (Tsmin) Temperature Max (Tsmax) Time (ts) from (Tsmin to Tsmax)	 150°C 200°C 60-120 seconds
Ramp-up rate (TL to Tp)	3°C / second maximum
Liquidous temperature (TL) Time (tL) maintained above TL	217°C 60-150 seconds
Peak package body temperature (Tp)	For users Tp must not exceed the classification temp in Table RPC-2. For suppliers Tp must equal or exceed the Classification temp in Table RPC-2.
Time (tp)* within 5°C of the specified classification temperature (Tc), see Figure RPC-1	30* seconds
Ramp-down rate (Tp to TL)	6°C / second maximum
Time 25°C to peak temperature	8 minutes maximum
** Tolerance for peak profile temperature (Tp) is defined as a supplier minimum and a user maximum.*	

Note 1: All temperatures refer to the center of the package, measured on the package body surface that is facing up during assembly reflow (e.g., live-bug). If parts are reflowed in other than the normal live-bug assembly reflow orientation (i.e., dead-bug), Tp shall be within ±2°C of the live-bug Tp and still meet the Tc requirements, otherwise, the profile **shall** be adjusted to achieve the latter. To accurately measure actual peak package body temperatures, refer to JEP140 for recommended thermocouple use.

Note 2: Reflow profiles in this document are for classification/preconditioning and are not meant to specify board assembly profiles. Actual board assembly profiles should be developed based on specific process needs and board designs and should not exceed the parameters in Table RPC-1.
For example, if Tc is 260°C and time tp is 30 seconds, this means the following for the supplier and the user.
For a supplier: The peak temperature must be at least 260°C. The time above 255°C must be at least 30 seconds.
For a user: The peak temperature must not exceed 260°C. The time above 255°C must not exceed 30 seconds.

Note 3: All components in the test load shall meet the classification profile requirements.

Table RPC-2 Pb-Free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3, <350	Volume mm^3, 350 to 2000	Volume mm^3, >2000
<1.6 mm	260°C	260°C	260°C
1.6 mm – 2.5 mm	260°C	250°C	245°C
>2.5 mm	250°C	245°C	245°C

Note 1: At the discretion of the device manufacturer, but not the board assembler/user, the maximum peak package body temperature (Tp) can exceed the values specified in Table RPC-2. The use of a higher Tp does not change the classification temperature (Tc).

Note 2: Package volume excludes external terminals (e.g., balls, bumps, lands, leads) and/or non-integral heat sinks.

Note 3: The maximum component temperature reached during reflow depends on package thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD packages may still exist.

ORDERING INFORMATION

Part Number	Description	Package
ES9118EC	SABRE 32-bit Low Power Stereo DAC with Headphone Amplifier and Output Switch	40-ball CSP
ES9118EQ	SABRE 32-bit Low Power Stereo DAC with Headphone Amplifier and Output Switch	40-pin QFN

REVISION HISTORY

Rev.	Date	Notes
0.1	March 9, 2016	Initial release
0.11	April 4, 2016	Update FIR filter types General cleanup
0.2H	June 20, 2016	General updates Link XI and MCLK via clock gearing Update MCLK requirement for custom FIR mode Update volume and trim control conditions Remove polarity swap
0.3	July 27, 2016	Update chip performance Update block and application diagrams Update register description
0.31	July 28, 2016	Update power consumption
0.32	August 9, 2016	Update CSP package height
0.55	September 30, 2016	Update to ES9118EC, updated register settings, updated figures
0.6	November 3, 2016	Update ES9118EQ and pinout
0.65	November 22, 2016	Update CSP pinout
0.7	December 21, 2016	Update header
0.8	October 20, 2017	Update Register 27[3]
0.9	November 15, 2018	Add Low Power Audio DAC description, removed Advanced Information
1.0	August 22, 2022	Update HQ address