Analog Reinvented

ES9080

32-bit High-Performance 8-Channel DAC

Product Datasheet

The Sabre ES9080 High Performance Audio DAC is a 32-Bit, 8-channel audio DAC that brings professional, digital audio quality to the consumer home entertainment market.

Using ESS' patented HyperStream® II architecture, the Sabre ES9080 delivers studio quality audio with 120dB DNR and –108dB THD+N to digital audio applications such as media streaming.

With the integrated line drivers, the ES9080 reduces BOM costs by eliminating the need for external amplifier to produce a line level 2Vrms output.

The Sabre® ES9080 flexible input architecture accepts up to serial 32 bit serial PCM data to 768kHz sample rate & DSD512. The ES9080 also has a 2 S/PDIF outputs which supports up to 192k @ 24 bits for a PCM to S/PDIF solution.

The Sabre Premier DAC sets a new standard for high-quality audio performance in a cost-effective, compact, easy to use form factor for today's most demanding digital audio applications.

Feature	Description
+120dB DNR per channel w/DRE -108dB THD+N per channel	Unprecedented dynamic range and ultra-low distortion
High Sample Rates	Support for up to PCM 768kHz & DSD512
8-channel DAC + Line Driver in 40-QFN	Reduced footprint and simplifies board layout
Multiple formats available	PCM, TDM, DSD, DoP, with support for S/PDIF output
Customizable filter characteristics	5 preset filters, with de-emphasis 32kHz, 44.1kHz & 48kHz filters
I2C interface control	Configured by microcontroller or other I2C source
Integrated low noise DAC reference regulators	Reduced BOM cost, PCB area and improved DNR.
Dual PCM to SPDIF transcoding	Encode PCM data into SPDIF format
Low Pin Count Standardized Packaging	5mm x 5mm, 40 pin QFN
2Vrms Integrated Line Driver	Reduces BOM costs w/o required external amplifier required for line driver levels

APPLICATIONS

- Media Streamer Applications
- Gaming Motherboards
- Audio Receivers
- Professional Audio Equipment

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Functional Block Diagram

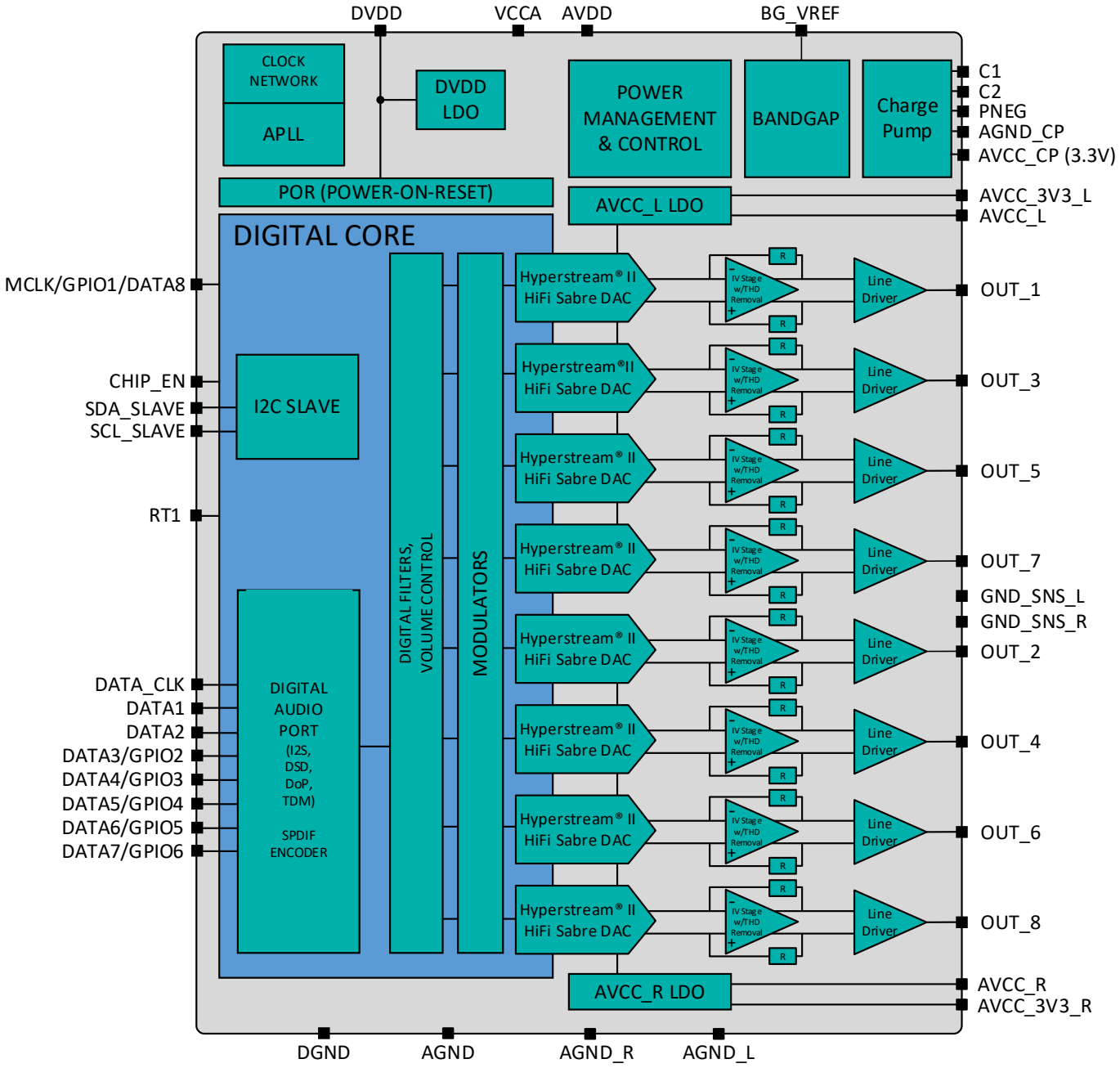


Figure 1 - ES9080 Block Diagram

ES9080Q Package

40 QFN Pinout

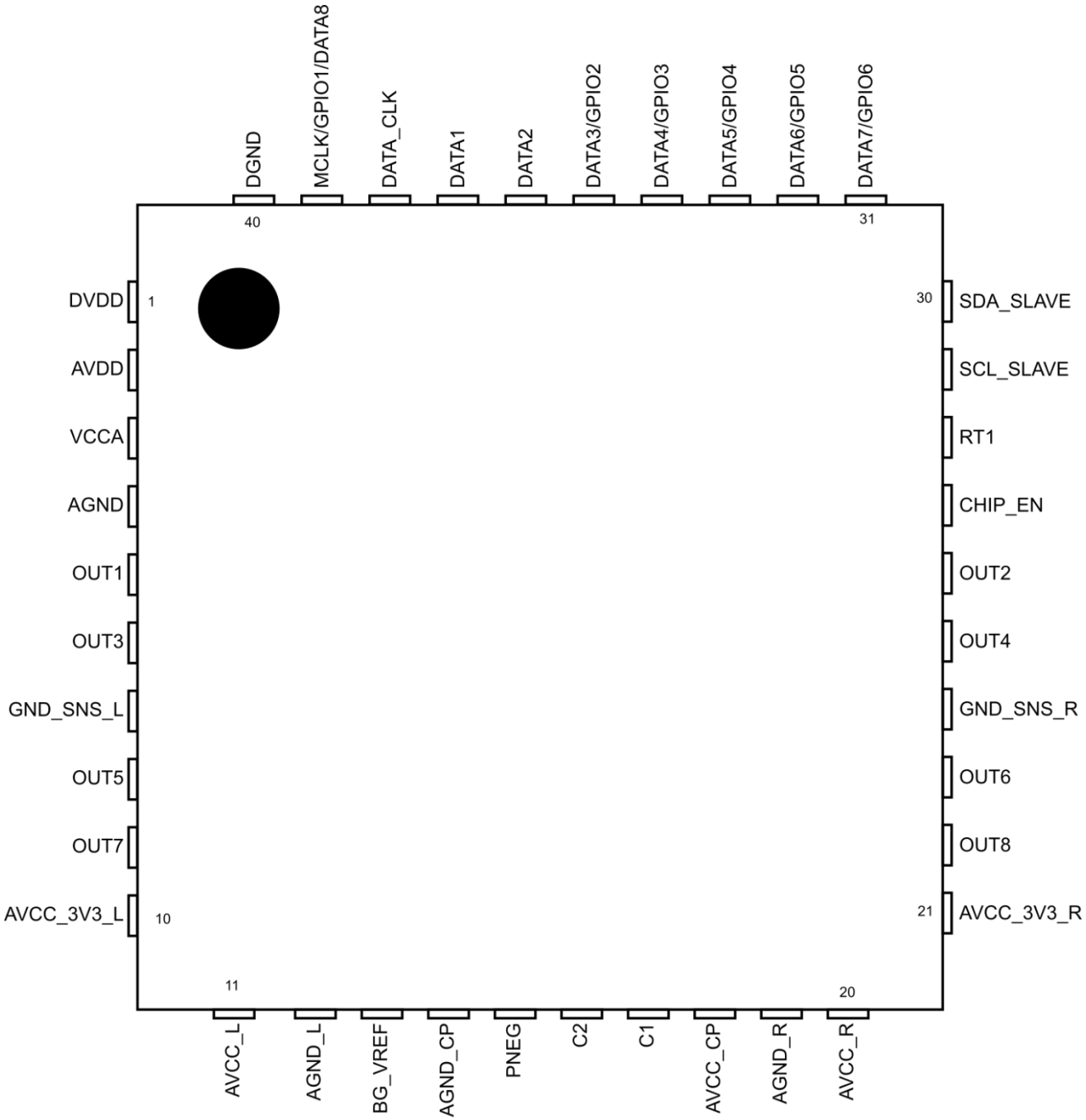


Figure 2 - 40 QFN Pinout

40 QFN Pin Descriptions

Pin	Name	Pin Type	Reset State	Pin Description
1	DVDD	Power	Power	Digital core supply, internally supplied
2	AVDD	Power	Power	3.3V or 1.8V I/O supply
3	VCCA	Power	Power	Analog Supply
4	AGND	Ground	Ground	Analog ground
5	OUT1	AO	Ground	Output channel 1
6	OUT3	AO	Ground	Output channel 3
7	GND_SNS_L	AI	Ground	Line driver load ground voltage sense (left, CH 1,3,5,7)
8	OUT5	AO	Ground	Output channel 5
9	OUT7	AO	Ground	Output channel 7
10	AVCC_3V3_L	Power	Power	Analog Regulator 3.3V Supply (left)
11	AVCC_L	Power	Power	Analog Regulator Output (left), internally supplied
12	AGND_L	Ground	Ground	Analog Ground (left)
13	BG_VREF	AO	Ground	Voltage reference
14	AGND_CP	Ground	Ground	Analog Ground for charge pump
15	PNEG	Power	Ground	Integrated chargepump output. Line driver negative supply.
16	C2	-	-	Line driver negative flying capacitor
17	C1	-	-	Line driver positive flying capacitor
18	AVCC_CP	Power	Power	Analog Supply for charge Pump
19	AGND_R	Ground	Ground	Analog Ground (right)
20	AVCC_R	Power	Power	Analog regulator output (right), internally supplied
21	AVCC_3V3_R	Power	Power	Analog Regulator 3.3V Supply (right)
22	OUT8	AO	Ground	Output channel 8
23	OUT6	AO	Ground	Output channel 6
24	GND_SNS_R	AI	Ground	Line driver load ground voltage sense (right, CH 2,4,6,8)
25	OUT4	AO	Ground	Output channel 4
26	OUT2	AO	Ground	Output channel 2
27	CHIP_EN	I/O	HiZ	Active-high chip enable.
28	RT1	I	HiZ	Reserved. **Must be connected to DGND for normal operation**.
29	SCL_SLAVE	I/O	HiZ	I2C slave interface serial clock input
30	SDA_SLAVE	I/O	HiZ	I2C slave interface data input/output
31	DATA7/GPIO6	I/O	HiZ	Serial DATA7, General I/O 6
32	DATA6/GPIO5	I/O	HiZ	Serial DATA6, General I/O 5

33	DATA5/GPIO4	I/O	HiZ	Serial DATA5, General I/O 4
34	DATA4/GPIO3	I/O	HiZ	Serial DATA4, General I/O 3
35	DATA3/GPIO2	I/O	HiZ	Serial DATA3, General I/O 2
36	DATA2	I/O	HiZ	Serial DATA2
37	DATA1	I/O	HiZ	Serial DATA1
38	DATA_CLK	I	HiZ	Serial data clock
39	MCLK/GPIO1/DATA8	I/O	HiZ	MCLK input, General I/O 1, Serial DATA8
40	DGND	Ground	Ground	Digital core ground
41	Package PAD[1]	-	-	No electrically connected, used for heat dissipation

Table 1 - 40 QFN Pin Descriptions

[1] Pin 41 is the package pad. See 40 QFN package dimensions for sizing

Digital Features

Digital Signal Path

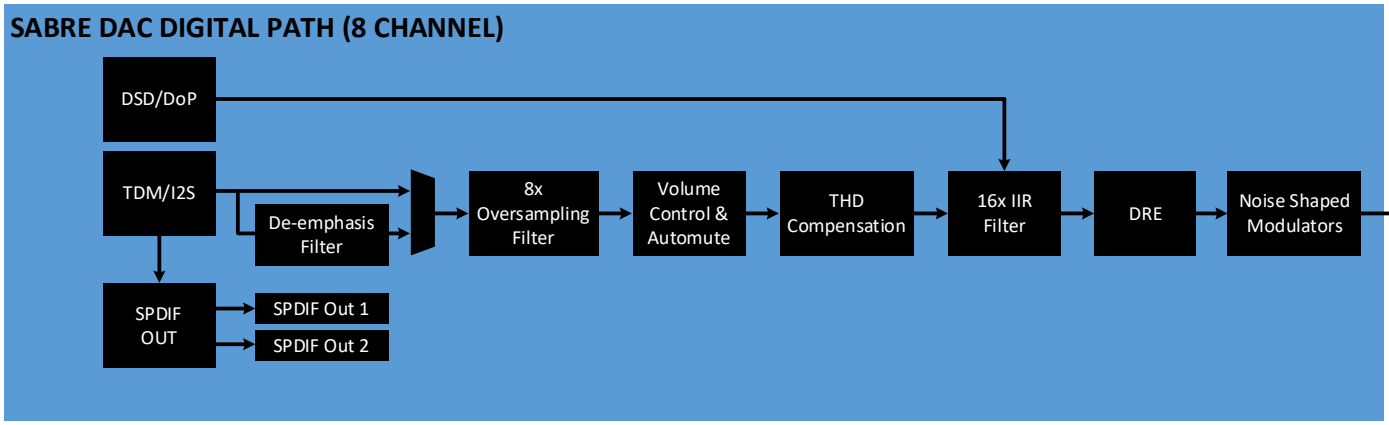


Figure 3 - Digital signal path

De-emphasis Filter

The De-emphasis filters are only applicable to channels 1 & 2 only.

The de-emphasis filters can be enabled or bypassed through the *BYPASS_DEEMPH* registers. The filters are configured for a 48kHz FS by default, however this can be changed via the *SEL_DEEMPH* register.

De-emphasis Filter Configuration Registers

- *Register 108[6]: BYPASS_DEEMPH*
- *Register 108[4:3]: SEL_DEEMPH*

Volume Control

This volume control is intended for use during audio playback. Each channel can be digitally attenuated from 0dB to –127.5dB. When a new volume level is set, the attenuation circuit will ramp softly to the new level at a rate specified in the *DAC VOL UP RATE, DAC VOL DOWN RATE* and *DAC VOL DOWN RATE FAST* registers.

By default, channel volumes are updated as soon as the volume registers are written. However, the volume control can only be changed once the *RUN_VOLUME* bit is toggled. This feature can be enabled or disabled through the *FORCE_VOLUME* bit

Each output channel has an independent volume control. The attenuation for each channel can be independent or synchronized in pairs by setting the *DAC_USE_MONO_VOLUME* bit.

Volume Control Registers

- *Registers 94-101: VOLUMEx*
- *Register 102: DAC VOL UP RATE*
- *Register 103: DAC VOL DOWN RATE*
- *Register 104: DAC VOL DOWN RATE FAST*
- *Register 105[4]: RUN_VOLUME*
- *Register 105[6]: FORCE_VOLUME*
- *Register 105[5]: DAC_USE_MONO_VOLUME*

Soft Mute

When Mute is asserted the digital signal level will be smoothly ramped to minimum. When Mute is de-asserted the digital signal level will ramp back up to the set volume levels. Asserting Mute will not change the value stored in the volume control register. The volume level and ramp rate are controlled through the Volume Control Registers.

Mute can be engaged through either the automute feature or by setting the mute bits for any individual channel through the MUTE CTRL register.

Volume Control Registers

- *Registers 94-101: VOLUMEx*
- *Register 102: DAC VOL UP RATE*
- *Register 103: DAC VOL DOWN RATE*
- *Register 104: DAC VOL DOWN RATE FAST*

Mute Control Registers

- *Register 106: MUTE_CTRL*

Automute

Automute is disabled by default and is triggered when any one of the following conditions are met:

Mode	Detection Condition	Time
PCM	Data is lower than *automute_level* for longer than the *automute_time*	$\frac{2\text{^}18}{(automute\_time * FS)}$
DoP	DSD data contains an equal number of 1s and 0s in any 8 consecutive bits of data	$\frac{2\text{^}18}{(automute\_time * DCLK)}$

Table 2 - Automute configuration

The automute feature is enabled for each channel individually through the *AUTOMUTE ENABLE* register. The thresholds that trigger and disable automute can be configured through the *AUTOMUTE LEVEL* and *AUTOMUTE OFF LEVEL* registers.

Automute Configuration Registers

- *Register 119: AUTOMUTE ENABLE*
- *Register 120-121: AUTOMUTE TIME*
- *Register 122-123: AUTOMUTE LEVEL*
- *Register 124-125: AUTOMUTE OFF LEVEL*

THD Compensation

The ES9080 has built-in THD compensation to help compensate for second and third harmonics that may be present on the output signal. The compensation is controlled through 4 individual 16-bit coefficients in the THD Compensation Coefficient Registers.

Using THD Compensation for differential mode (4 channel mode) where Channels 1&2, 3&4, 5&6, 7&8 are paired to create 4 differential channels, THD coefficients need to be the same for each pair. Therefore, C2 & C3 would be the same for all channels.

The following equation displays how the second and third harmonics are affected by the C2 and C3 values:

$$output = x + c2 * x^2 + c3 * x^3$$

THD Compensation Coefficient Registers

- *Registers 111-112: THD COMP C2 CH1/3/5/7*
- *Registers 113-114: THD COMP C3 CH1/3/5/7*
- *Registers 115-116: THD COMP C2 CH2/4/6/8*
- *Registers 117-118: THD COMP C3 CH2/4/6/8*

Dynamic Range Enhancement (DRE)[2]

The DRE controller is composed of a peak detector with a programmable rate. If the input audio stream peak level decays below the *DRE ON THRESHOLD* value, the controller will attenuate the analog gain by 16.37 dB, while simultaneously increasing the digital gain by the value of DRE GAIN CHx/x/x/x. DRE will remain engaged until the input audio stream peak level rises above the DRE OFF THRESHOLD value. The rate at which the peak level decay is determined by DRE DECAY RATE.

Control over various device functions is given to the DRE peak filter through the *DRE ATT EN AND THDR CTRL* registers. Once configured, the *DRE FORCE* registers may be configured to enable DRE on the desired channels.

The DRE peak filter is disabled by default and is enabled by setting the PEAK FILTER bit.

DRE Configuration Registers

- *Register 144-145: DRE ON THRESHOLD*
- *Register 140-141: DRE GAIN CH1/3/5/7*
- *Register 142-143: DRE GAIN CH2/4/6/8*
- *Register 146-147: DRE OFF THRESHOLD*
- *Register 148: DRE DECAY RATE*
- *Register 136: DRE ATT EN AND THDR CTRL*
- *Register 139: DRE FORCE*
- *Register 108[5]: PEAK_FILTER*

Note: Some implementations of DRE may experience a pop noise due to a possible small DC level change between DRE transitions, in particular when used with external output stage.

[2] For more information regarding the DRE Peak Filter, please reference the DRE Configuration application note. Available from your local FAE upon request.

GPIO Configuration

GPIO#_CFG	Function	I/O Direction
0	1'b0	Output
1	1'b0	Output
2	1'b1	Output
3	128 FS Block	Output
4	Interrupt	Output
5	Mute all channel	Input
6	System mode Control	Input
7	Reserved	Output
8	CLK_VALID flag	Output
9	PWM1	Output
10	PWM2	Output
11	PWM3	Output
2	Volume min	Output
13	Automute status	Output
14	Soft Ramp finished	Output
15	S/PDIF stream output (selects S/PDIF 1&2 outputs by S/PDIF_SEL in Reg 64-67	Output

Table 3 – Standard GPIO Functions

Each GPIO can be configured using GPIO#_CFG, where # corresponds to the GPIO number (eg GPIO1)

These configurations can be access through Registers 53-57.

Audio Input Formats

For configuring TDM & I2S, use Registers 77-91.

Time-division multiplexing (TDM)

The ES9080 supports up to 16 channel TDM modes. Application Note regarding setup for TDM is available.

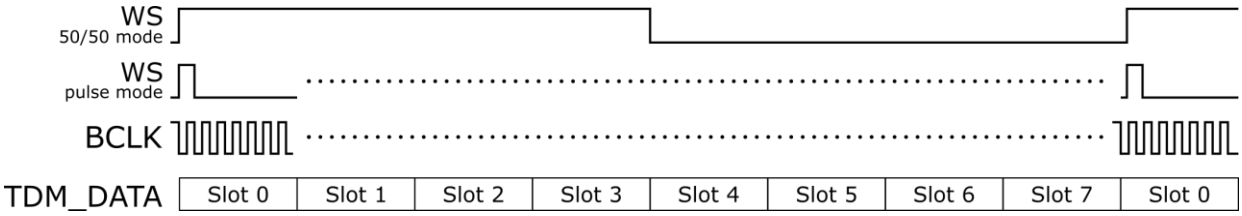


Figure 4 - Example of using 8 channels of TDM showing both a 50/50 word select mode and a pulse word select mode.

I2S (subset of TDM interface)

Data is latched on the positive edge of BCK

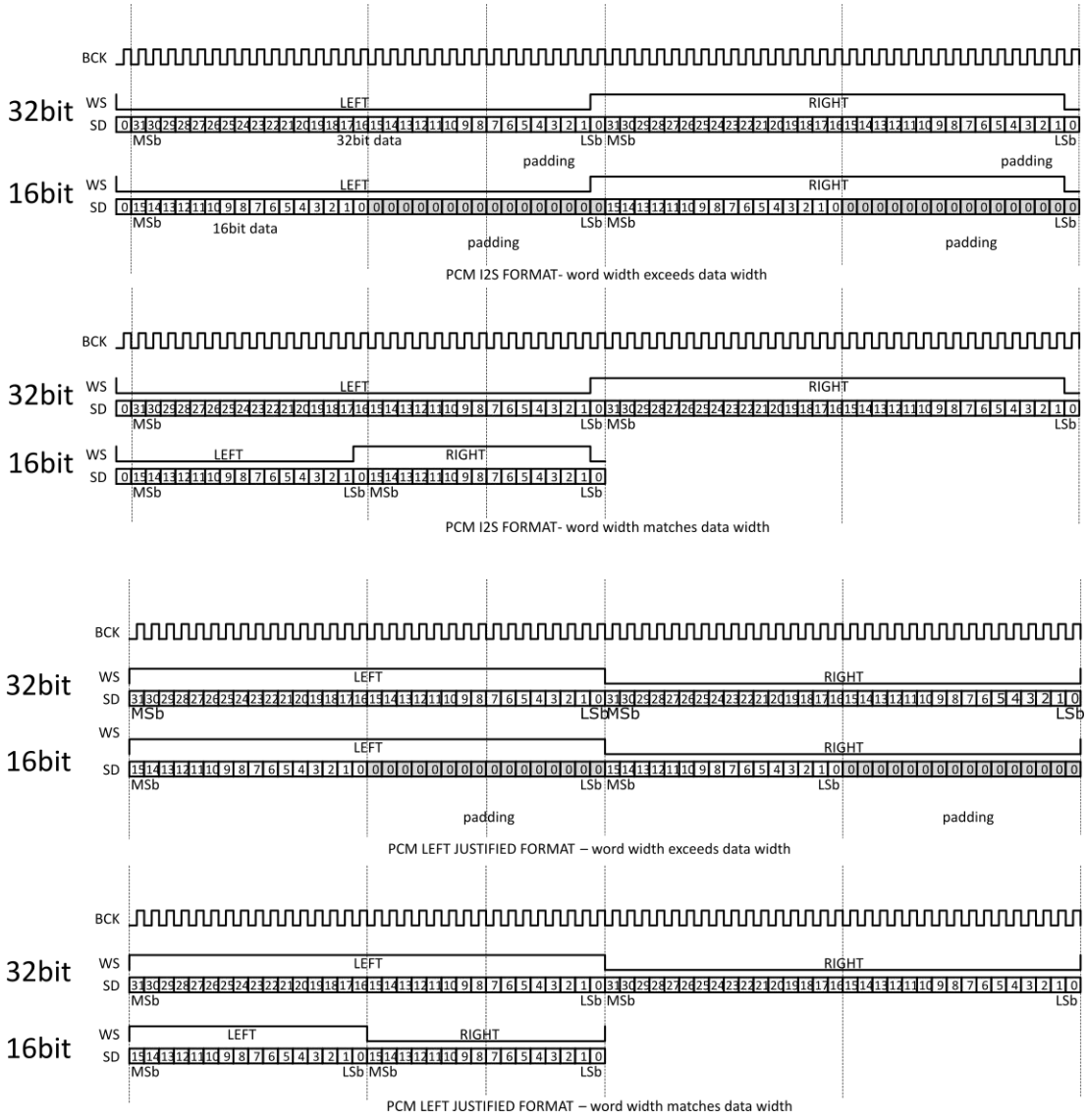


Figure 5 - I2S & LJ Output Format

DSD

Data is latched on the positive edge of DCLK

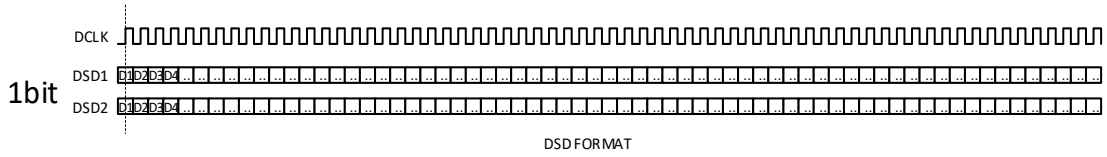


Figure 6 - DSD Format

Note: DSD does not work with the automute feature.

Audio Output Formats

S/PDIF Encoders

The ES9080 included 2 S/PDIF encoders.

The S/PDIF encoders are accessible using the following registers:

- Register 3[7] ENABLE_SPDIF_ENCODE
- Register 52[7:6] SPDIF2_SEL
- Register 52[5:4] SPDIF1_SEL
- Registers 53-55
- Registers 159-155: SPDIF1 CS
- Registers 164-160: SPDIF2 CS

S/PDIF can be enabled on the GPIO pins through Registers 64-65[15:10] *SPDIF_SEL_GPIO#.*

An application note on configuring the S/PDIF output on the ES9080 is available. Ask FAE for support.

Pre-Programmed Digital Filters

The ES9080 has 5 pre-programmed digital filters. The latency for each filter reduces (scales) with increasing sample rates.

- Minimum Phase
- Linear Phase Apodizing
- Linear Phase Fast Roll-off Low Ripple
- Minimum Phase Slow Roll-off
- Minimum Phase Slow Roll-off Low Dispersion

PCM Filter Properties

The following filter properties were obtained from software simulations of these filters.

Minimum Phase					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band	±0.0207dB			0.460 x fs	Hz
	–3dB			0.484 x fs	
Stop band	<-91.4dB	0.547 x fs			Hz
Group Delay			17 / fs		s
Flatness (ripple)	±0.002dB				dB

Linear Phase Apodizing					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band	±0.026dB			0.421 x fs	Hz
	–3dB			0.449 x fs	
Stop band	<-60.3dB	0.5 x fs			Hz
Group Delay			32 / fs		s
Flatness (ripple)	±0.026dB				dB

Linear Phase Fast Roll-off Low Ripple					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band	±0.021dB			0.470 x fs	Hz
	–3dB			0.492 x fs	
Stop band	<-57.84	0.547 x fs			Hz
Group Delay			32 / fs		s
Flatness (ripple)	±0.021dB				dB

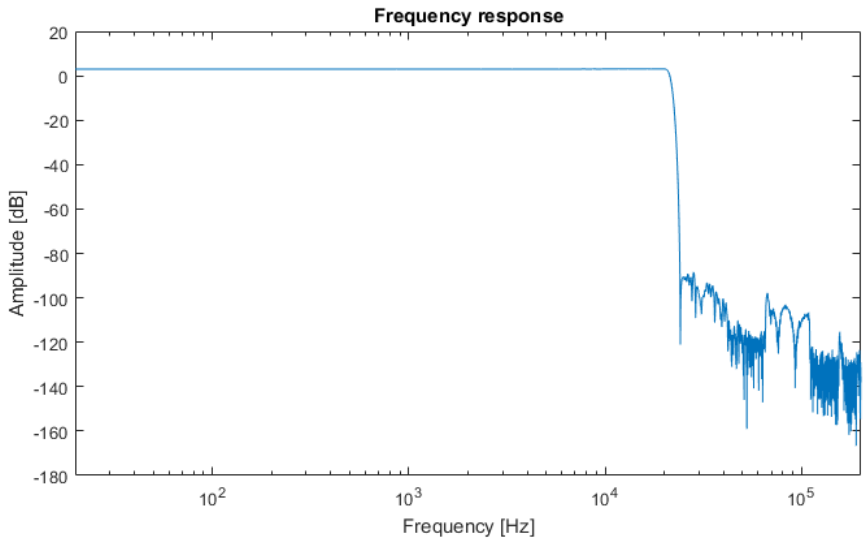
Minimum Phase Slow Roll-off					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band	±0.0034			0.305 x fs	Hz
	–3dB			0.438 x fs	
Stop band	<-83.72dB	0.789 x fs			Hz
Group Delay			2 / fs		s
Flatness (ripple)	±0.0034dB				dB

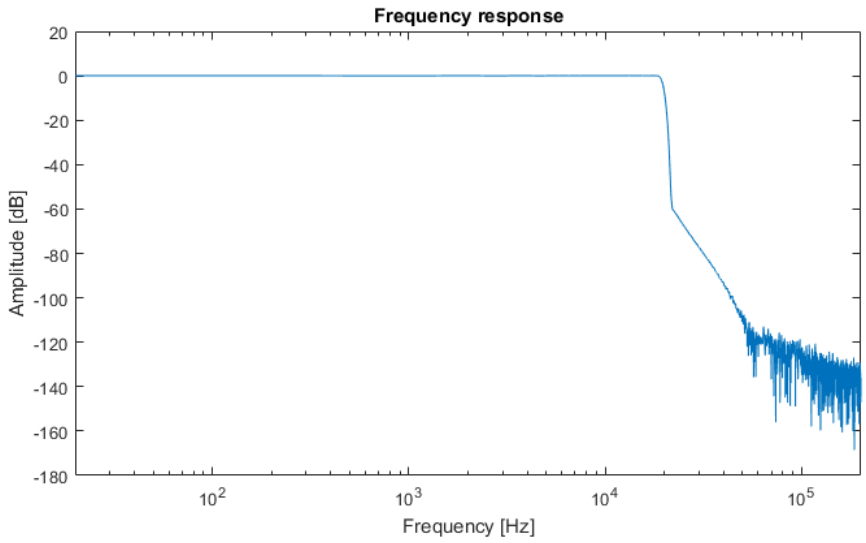
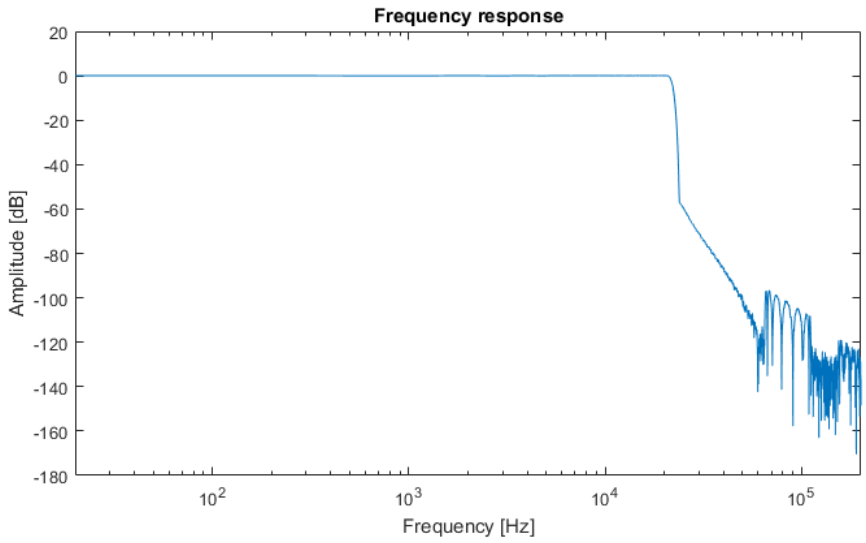
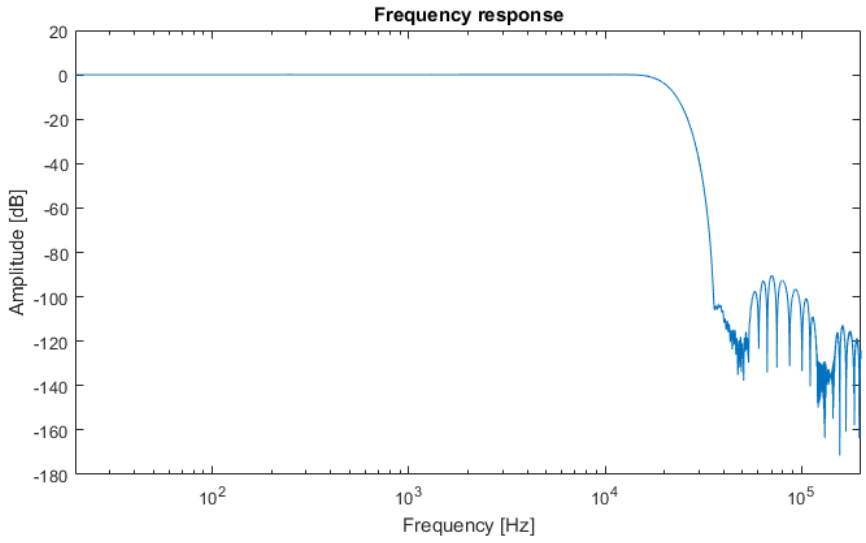
Minimum Phase Slow Roll-off Low Dispersion					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band	±0.0053dB			0.306 x fs	Hz
	–3dB			0.43 x fs	
Stop band	<-83.72dB	0.797 x fs			Hz
Group Delay			9 / fs		s
Flatness (ripple)	±0.0053dB				dB

Table 4 - PCM filter properties

PCM Filter Frequency Response

The following frequency responses were obtained from software simulations of these filters. Simulation sample rate is 44.1kHz.

Filter	Frequency Response
Minimum Phase	

Linear Phase Apodizing	
Linear Phase Fast Roll-off Low Ripple	
Minimum Phase Slow Roll-off	

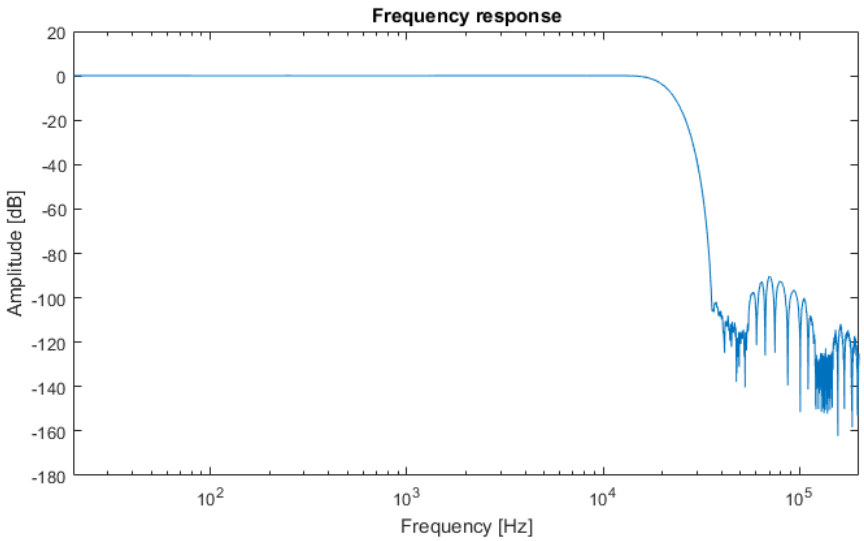
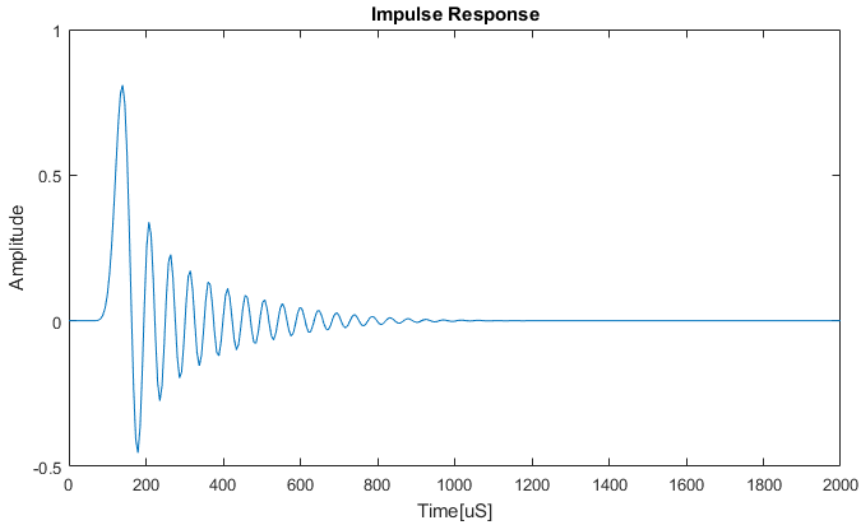
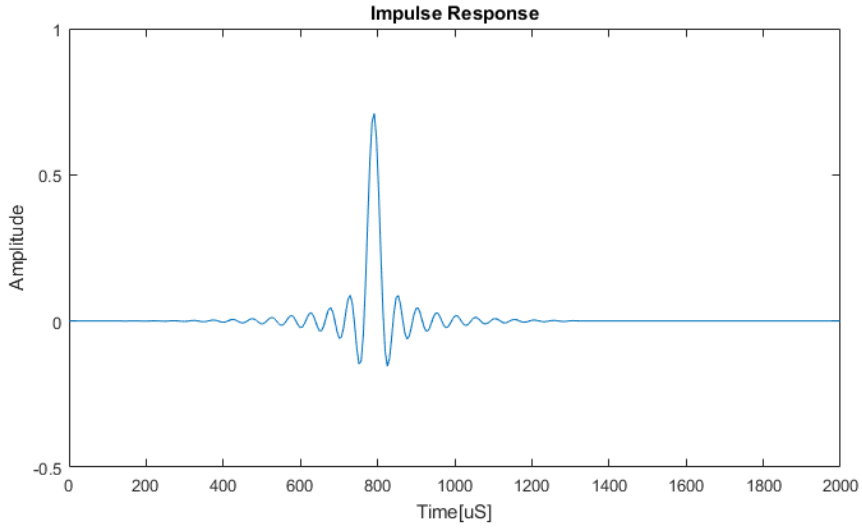
Minimum Phase Slow Roll-off Low Dispersion	

Table 5 - PCM filter frequency response

PCM Filter Impulse Response

The following impulse responses were obtained from software simulations of these filters. Simulation sample rate is 44.1kHz.

Filter	Impulse Response
Minimum Phase	
Linear Phase Apodizing	

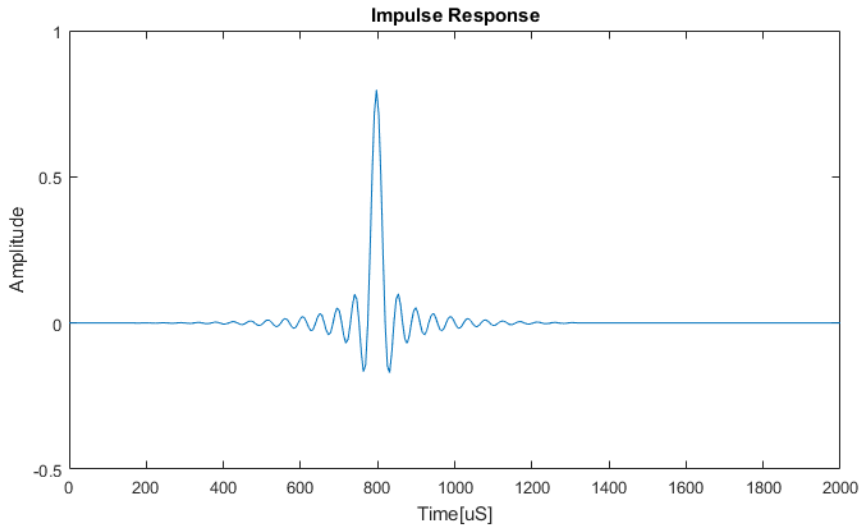
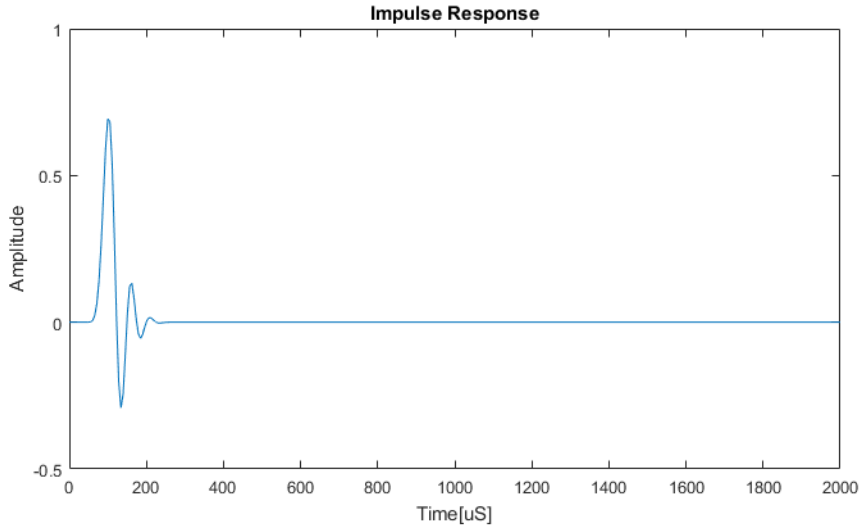
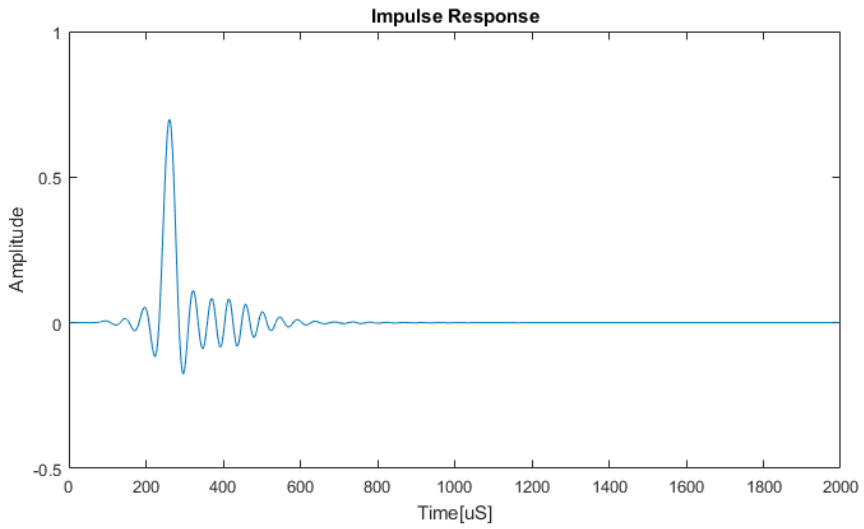
Linear Phase Fast Roll-off Low Ripple	
Minimum phase slow roll-off	
Minimum phase slow roll-off low dispersion	

Table 6 - PCM filter impulse response

Clock Distribution

The ES9080 includes features for selecting and manipulating the input clock source.

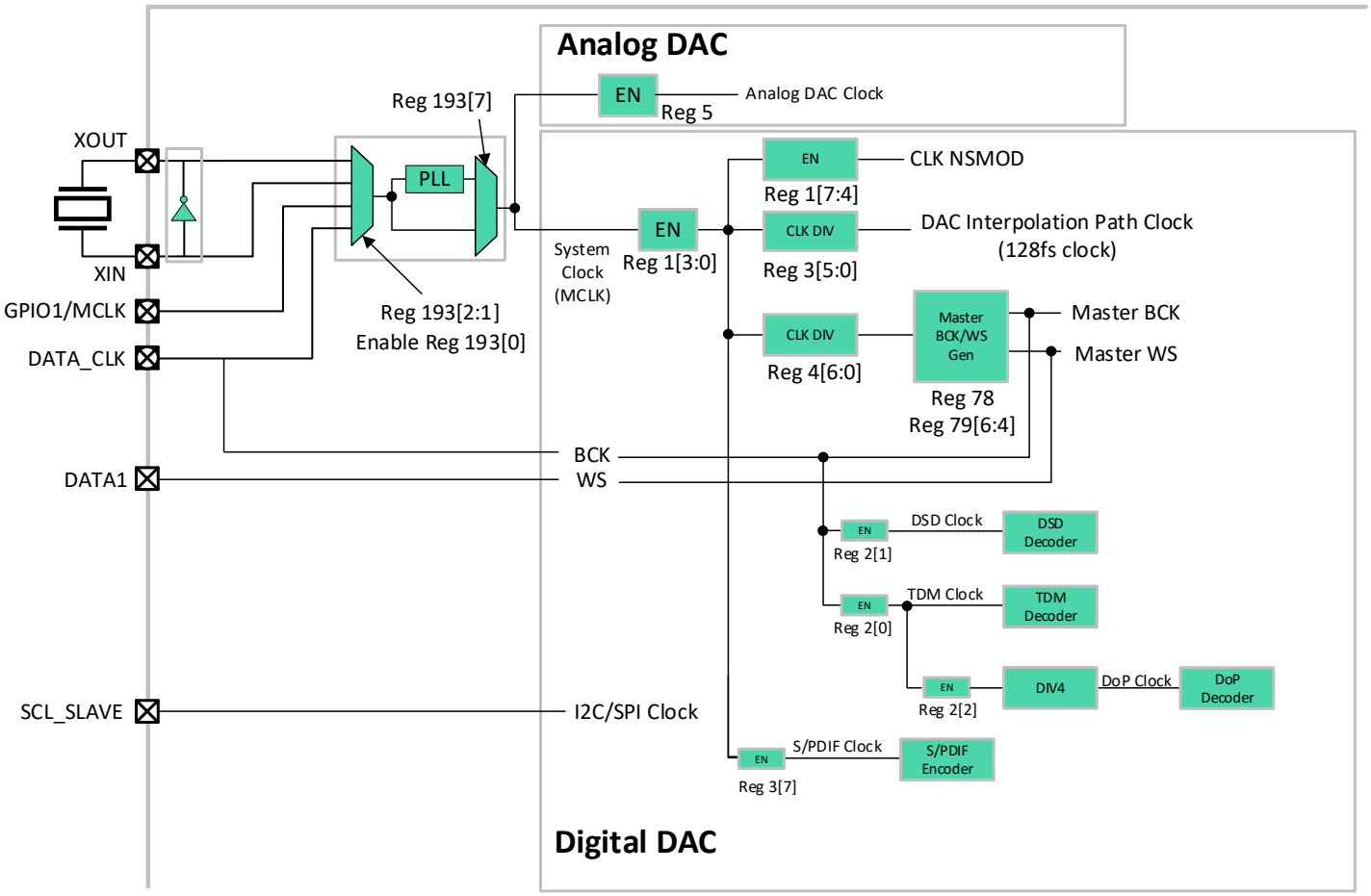


Figure 7 - Clock Distribution Diagram with Registers

The following list shows the various clocks of the ES9080 and the associated registers for configuration.

Analog DAC Clock

- Reg 5 (ANALOG_DAC_ENABLE)
- Reg 193[7] (PLL_BYP)
- Reg 193[2:1] (SEL_PLL_IN)
- Reg 193[0] (EN_PLL_CLKIN)

NSMOD Clock

The NSMOD clock is utilized by the HyperStream® II **N**oise **S**haped **MOD**ulators.

- Reg 1[7:4] (ENABLE_NSMOD_CHxx)
- Reg 1[3:0] (ENABLE_DAC_CHxx)
- Reg 193[7] (PLL_BYP)
- Reg 193[1] (SEL_PLL_IN)
- Reg 193[0] (EN_PLL_CLKIN)

DAC Interpolation Path Clock

- Reg 3[5:0] (SELECT_IDAC_NUM)
- Reg 1[3:0] (ENABLE_DAC_CHxx)
- Reg 193[7] (PLL_BYP)
- Reg 193[1] (SEL_PLL_IN)
- Reg 193[0] (EN_PLL_CLKIN)

Master BCK and WS

- Reg 78 (MASTER MODE CONFIG)
- Reg 79[6:4] (MASTER_WS_SCALE)
- Reg 4[6:0] (SELECT_MENC_NUM)
- Reg 1[3:0] (ENABLE_DAC_CHxx)
- Reg 193[7] (PLL_BYP)
- Reg 193[1] (SEL_PLL_IN)
- Reg 193[0] (EN_PLL_CLKIN)

DSD Clock

- Reg 2[1] (ENABLE_DSD_DECODE)

TDM Clock

- Reg 2[0] (ENABLE_TDM_DECODE)

DoP Clock

- Reg 2[2] (ENABLE_DOP_DECODE)
- Reg 2[0] (ENABLE_TDM_DECODE)

S/PDIF

- Reg 3[7] (ENABLE_SPDIF_ENCODE)
- Reg 1[3:0] (ENABLE_DAC_CHxx)
- Reg 193[7] (PLL_BYP)
- Reg 193[1] (SEL_PLL_IN)
- Reg 193[0] (EN_PLL_CLKIN)

I2S Master Clock Rate Configurations

WS can be scaled down further than shown via Register 79 [6:4] *MASTER_WS_SCALE*.

When enabling 16-bit mode, the following registers must be modified:

- Register 81 [7:6] – set TDM bit width to 16
- Register 78 [4:3] – set master frame length to 16-bits

Table 7 - I2S Master Clock Rate Configurations

MCLK Frequency	WS [kHz]	BCK [MHz]	Bits	Channels	Register 3 [5:0] SELECT_IDAC_NUM		Register 0 [6:0] SELECT_MENC_NUM	
					value	divider	value	divider
22.579 MHz	44.1	2.822	32	2	6'd3	4	7'd3	4
	88.2	5.645		2	6'd1	2	7'd1	2
	176.4	11.290		2	6'd0	1	7'd0	1
	44.1	1.411	16	2	6'd3	4	7'd3	4
	88.2	2.822		2	6'd1	2	7'd1	2
	176.4	5.645		2	6'd0	1	7'd0	1
24.576 MHz	48	3.072	32	2	6'd3	4	7'd3	4
	96	6.144		2	6'd1	2	7'd1	2
	192	12.288		2	6'd0	1	7'd0	1
	48	1.536	16	2	6'd3	4	7'd3	4
	96	3.072		2	6'd1	2	7'd1	2
	192	6.144		2	6'd0	1	7'd0	1
45.158 MHz	44.1	2.822	32	2	6'd7	8	7'd7	8
	88.2	5.645		2	6'd3	4	7'd3	4
	176.4	11.290		2	6'd1	2	7'd1	2
	352.8	22.579		2	6'd0	1	7'd0	1
	44.1	1.411	16	2	6'd7	8	7'd7	8
	88.2	2.822		2	6'd3	4	7'd3	4
	176.4	5.645		2	6'd1	2	7'd1	2
	352.8	11.290		2	6'd0	1	7'd0	1
49.152 MHz	48	3.072	32	2	6'd7	8	7'd7	8
	96	6.144		2	6'd3	4	7'd3	4
	192	12.288		2	6'd1	2	7'd1	2
	384	24.576		2	6'd0	1	7'd0	1
	48	1.536	16	2	6'd7	8	7'd7	8
	96	3.072		2	6'd3	4	7'd3	4
	192	6.144		2	6'd1	2	7'd1	2
	384	12.288		2	6'd0	1	7'd0	1

I2S Slave Clock Rate Configurations

MCLK Frequency	WS [kHz]	BCK	Channels	Register 3 [5:0] SELECT_IDAC_NUM		Register 0 [6] ENABLE_2X_MODE	
				value	divider	value	multiplier
22.579 MHz	44.1	512FS	2	7'd3	4	1'b0	1x
	88.2	256FS	2	7'd1	2	1'b0	1x
	176.4	128FS	2	7'd0	1	1'b0	1x
	352.8	64FS	2	7'd0	1	1'b1	2x
24.576 MHz	48	512FS	2	7'd3	4	1'b0	1x
	96	256FS	2	7'd1	2	1'b0	1x
	192	128FS	2	7'd0	1	1'b0	1x
	384	64FS	2	7'd0	1	1'b1	2x
45.158 MHz	44.1	1024FS	2	7'd7	8	1'b0	1x
	88.2	512FS	2	7'd3	4	1'b0	1x
	176.4	256FS	2	7'd1	2	1'b0	1x
	352.8	128FS	2	7'd0	1	1'b0	1x
49.152 MHz	48	1024FS	2	7'd7	8	1'b0	1x
	96	512FS	2	7'd3	4	1'b0	1x
	192	256FS	2	7'd1	2	1'b0	1x
	384	128FS	2	7'd0	1	1'b0	1x

Table 8 - I2S Slave Clock Rate Configurations

Audio Interface Timing

Audio data on DATA1-7 are sampled at the rising edges of DATA_CLK and must satisfy the setup and hold time requirements relative to the rising edge of DATA_CLK.

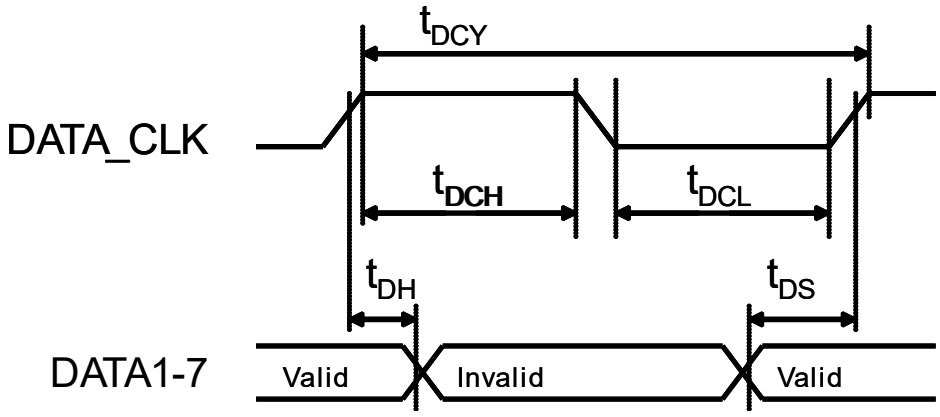


Figure 8 - Audio Interface Timing

Parameter	Symbol	Min	Max	Unit
DATA_CLK pulse width high	t_{DCH}	9.0		ns
DATA_CLK pulse width low	t_{DCL}	9.0		ns
DATA_CLK cycle time	t_{DCY}	20		ns
DATA_CLK duty cycle		45:55	55:45	
DATAx set-up time to DATA_CLK rising edge	t_{DS}	4.1		ns
DATAx hold time to DATA_CLK rising edge	t_{DH}	2.0		ns

Table 9 - Audio Interface Timing Definitions

Analog Features

APLL

The ES9080 features a built-in Analog PLL (APLL) for generating arbitrary system clock frequencies (Fout) when no dedicated external clock is available. The APLL employs a fractional feedback divider to produce virtually any input/out frequency combination.

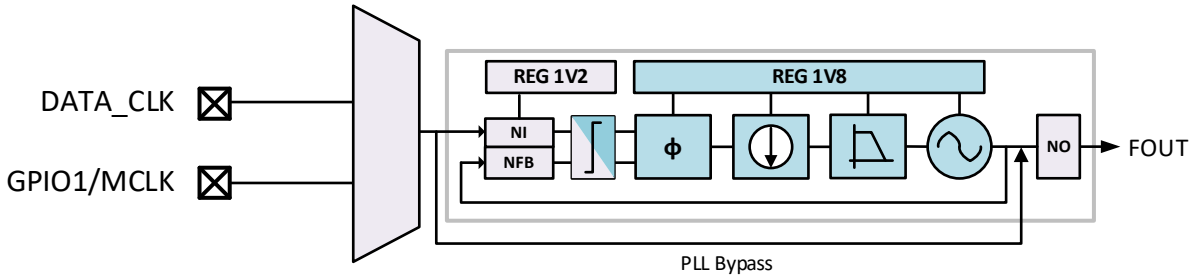


Figure 9 - Functional Block Diagram of ES9080 APLL

The following equation describes the relationship between input frequency (Fin) and output frequency (Fout) of the APLL:

$$F_{out} = \left(\frac{F_{in}}{N_i}\right) * \frac{N_{fb}}{N_o}$$

The divider ratios are configured using the synchronous I2C register interface using while observing the constraints on the reference (Fref) and VCO frequencies (Fvco):

$$F_{ref} = \left(\frac{F_{in}}{N_i}\right) \qquad 0.70MHz < F_{ref} < 1.25MHz$$

$$F_{VCO} = F_{out} * N_o \qquad 90MHz < F_{VCO} < 100MHz$$

The divider ratios are set using the synchronous I2C interface:

a. Ni = input dividing ratio. Reg 202-200[9:1], **PLL_CLK_IN_DIV**
b. Nfb = feedback dividing ratio. The feedback divider ratio is a 24 bit fractional value to achieve a high resolution output frequency and is calculated using:

$$N_{fb} = \frac{2^{25}}{FBDIV}$$

FBDIV is accessible in Reg 199-197[23:0], **PLL_CLK_FB_DIV**
c. No = output dividing ratio. Reg 202-200[18:10], **PLL_CLK_OUT_DIV**

Table 10 provides a list of recommended divider ratios for common input/output frequency combinations when using DATA_CLK as the input source. The values are shown for 48kHz families. The same dividers can be used for 44.1kHz families to produce the appropriate audio clock.

Fin (MHz)	Ni	FBDIV (Nfb)	No	Fout (MHz)
1.536	2	0x40000 (128)	2	49.152
3.072	4	0x40000 (128)	2	49.152
6.144	8	0x40000 (128)	2	49.152
12.288	16	0x40000 (128)	2	49.152
24.576	32	0x40000 (128)	2	49.152

Table 10 - Recommended PLL divider ratios for DATA_CLK rates

The APLL also allows for audio clock generation for 44.1kHz families from a 48kHz compatible MCLK source. Table 11 lists divider ratios for conversion between 48kHz and 44.1kHz families.

Fin (MHz)	Ni	FBDIV (Nfb)	No	Fout (MHz)
49.152	54	0x528F5 (99.225)	2	45.1584
24.076	27	0x528F5 (99.225)	2	45.1584
45.1584	62	0x3CB26 (134.966)	2	49.152
22.5792	31	0x3CB26 (134.966)	2	49.152

Table 11 - Recommended PLL divider ratios for MCLK 48kHz-44.1kHz clock rate conversions

APLL Configuration

Setting up the APLL requires a synchronous I2C register writes to set the divider ratios, input source and analog parameters. The following sequences are recommended for optimal performance. For more details consult the Register Listings, Reg 192-203

The APLL must be bypassed when using an external clock source through the GPIO1 pin. When using an external clock source these register settings should be used:

- Reg 202 = 0x40
- Reg 192 = 0x03
- Reg 193 = 0xC3

Configuring the APLL with DATA_CLK input source requires setting the following registers:

- Reg 202 = 0xC8
- Reg 192 = 0x01
- Reg 193 = 0x5F
- Reg 196 = 0x43
- Reg 197-199 = FBDIV (feedback divider value)
- Reg 200[0] = 1'b1
- Reg 201[1:0], Reg 200[7:1] = Ni (input divider value)
- Reg 202[2:0], Reg 201[7:2] = No (output divider value)
- Reg 203 = 0x30
- Reg 195 = 0xFF
- Reg 194 = 0x05

Note: Set AUTO_LOCK_EN (Reg 194[2]) & VREF_HOLD_ENABLE (Reg 194[0], once all other PLL registers are set.

IMPORTANT NOTE, when using the PLL, Register 202 (PLL REGISTER7) should be the first register to be configured in both sequences.

Table 12 provides some general configurations for the PLL:

Bits	Sample Rate [kHz]	BCLK [MHz]	Register 200-202 [9:1]: PLL_CLK_IN_DIV	VCO Frequency [MHz]	Register 197-199 [23:0]: PLL_CLK_FB_DIV	Register 200-202 [18:10]: PLL_CLK_OUT_DIV	F_OUT [MHz]
FS = 44.1kHz							
32	352.8	22.5792 (64FS)	8	90.3168	0x100000	2	45.1584
	176.4	11.2896 (64FS)	4	90.3168	0x100000	2	45.1584
	88.2	5.6448 (64FS)	2	90.3168	0x100000	2	45.1584
	44.1	2.8224 (64FS)	2	90.3168	0x080000	2	45.1584
24	352.8	16.9344 (48FS)	6	90.3168	0x100000	2	45.1584
	176.4	8.4672 (48FS)	3	90.3168	0x100000	2	45.1584
	88.2	4.2336 (48FS)	3	90.3168	0x080000	2	45.1584
	44.1	2.1168 (48FS)	3	90.3168	0x040000	2	45.1584
FS = 48kHz							
32	384	24.576 (64FS)	8	98.304	0x100000	2	49.152
	192	12.288 (64FS)	4	98.304	0x100000	2	49.152
	96	6.144 (64FS)	4	98.304	0x080000	2	49.152
	48	3.072 (64FS)	2	98.304	0x080000	2	49.152
24	384	18.432 (48FS)	6	98.304	0x100000	2	49.152
	192	9.216 (48FS)	3	98.304	0x100000	2	49.152
	96	4.608 (48FS)	3	98.304	0x080000	2	49.152
	48	2.304 (48FS)	3	98.304	0x040000	2	49.152

Table 12 – General PLL Configurations

Absolute Maximum Ratings

PARAMETER	RATING
Positive Supply Voltage • AVCC_3V3_L, AVCC_3V3_R • AVCC_CP • VCCA • AVDD • DVDD	 • +3.7V with respect to Ground • +3.7V with respect to Ground • +3.7V with respect to Ground • +3.7V with respect to Ground • +1.4V with respect to Ground
Storage temperature	–65°C to +150°C
Operating Junction Temperature	+125°C
Voltage range for digital input pins	–0.3V to AVDD(nom)+0.3V
ESD Protection Human Body Model (HBM) Charge Device Model (CDM)	 2kV 500V

Table 13 - Absolute Maximum Ratings

WARNING: Stresses beyond those listed under here may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied.

WARNING: Electrostatic Discharge (ESD) can damage this device. Proper procedures must be followed to avoid ESD when handling this device.

IO Electrical Characteristics

PARAMETER	SYMBOL	MINIMUM	MAXIMUM	UNIT	COMMENTS
High-level input voltage	VIH	(AVDD / 2) + 0.4		V	
Low-level input voltage	VIL		0.4	V	
High-level output voltage	VOH	AVDD – 0.2		V	IOH = ((AVDD / 2) +1.4) mA
Low-level output voltage	VOL		0.2	V	IOL = ((AVDD / 2) + 1.7) mA

Table 14 - IO electrical characteristics

Recommended Operating Conditions

There are the recommended operating conditions for the ES9080.

PARAMETER	SYMBOL	CONDITIONS
Operating temperature	T_A	–20°C to +85°C
DVDD		Internally Generated
AVDD		3.3V
VCCA		3.3V
AVCC_L, AVCC_R		Internally Generated
AVCC_CP		3.3V
AVCC_3V3_L, AVCC_3V3_R		3.3V

Table 15 - Recommended operating conditions

Recommended Power up Sequence

The recommended power up sequence is show in the following diagram. All supplies and MCLK should be stable before CHIP_EN goes high.

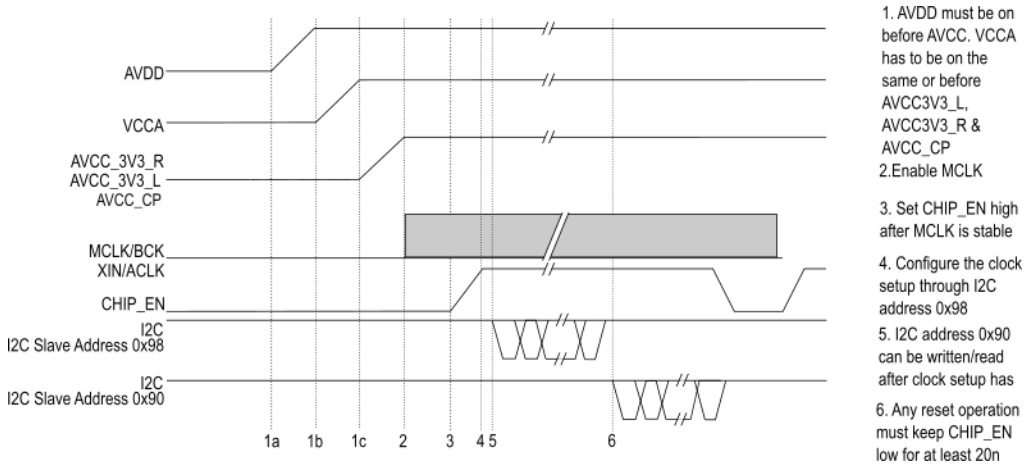


Figure 10 - Timing diagram for recommended power up sequence

Recommended Power down Sequence

The recommended power down sequence is show in the following diagram. CHIP_EN is to be deasserted before MCLK & Power supplies are turned off.

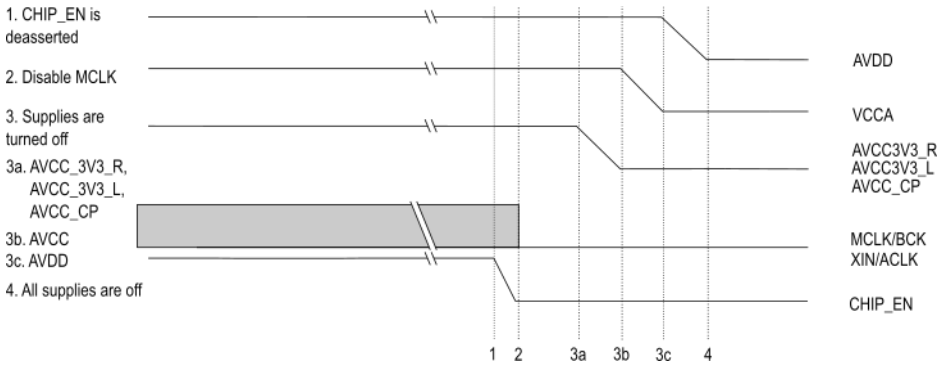


Figure 11 - Timing diagram for recommended power down sequence

Power Consumption

Power numbers are given when the device is in slave mode.

Test Conditions 1 (unless otherwise noted)

T_A = 25°C, AVCC_3V3_L = AVCC_3V3_R = AVCC_CP = VCCA = AVDD = +3.3V, fs = 48kHz, **MCLK = 49.152MHz**, I2S streaming zero

Parameter		Min	Typ	Max	Unit
Supply Current during 48kHz 8ch mode					
AVCC (all supplies except AVDD)			31.6		mA
AVDD			24.8		mA
Standby					
AVCC (all supplies except AVDD)			<1		uA
AVDD			<1		uA

Table 16 - Power consumption test 1

Test Conditions 2 (unless otherwise noted)

T_A = 25°C, AVCC_3V3_L = AVCC_3V3_R = AVCC_CP = VCCA = AVDD = +3.3V, fs = 48kHz, **MCLK = 49.152MHz**, I2S input, w/1kHz full scale

Parameter		Min	Typ	Max	Unit
Supply Current during 48kHz 8ch mode					
AVCC (all supplies except AVDD)			70.9		mA
AVDD			29.5		mA
Standby					
AVCC (all supplies except AVDD)			<1		uA
AVDD			<1		uA

Table 17 - Power consumption test 2

Test Conditions 3 (unless otherwise noted)

T_A = 25ºC, AVCC_3V3_L = AVCC_3V3_R = AVCC_CP = VCCA = AVDD = +3.3V, fs = 48kHz, **MCLK = 24.576MHz**, I2S input, w/1kHz full scale

Parameter		Min	Typ	Max	Unit
Supply Current during 48kHz 8ch mode					
AVCC (all supplies except AVDD)			67.9		mA
AVDD			20.4		mA
Standby					
AVCC (all supplies except AVDD)			<1		uA
AVDD			<1		uA

Table 18 - Power consumption test 3

Test Conditions 4 (unless otherwise noted)

T_A = 25ºC, AVCC_3V3_L = AVCC_3V3_R = AVCC_CP = VCCA, ***AVDD = +1.8V***, fs = 48kHz, ***MCLK = 24.576MHz***, I2S output, w/1kHz full scale

Parameter		*Min*	*Typ*	*Max*	*Unit*
Supply Current during 48kHz 8ch mode					
AVCC			***67.8***		mA
AVDD			***19.7***		mA
Standby					
AVCC			***<1***		uA
AVDD			***<1***		uA

Table 19 - Power consumption test 4

Test Conditions 5 (unless otherwise noted)

T_A = 25°C, AVCC_3V3_L = AVCC_3V3_R = AVCC_CP = VCCA, ***AVDD = +1.8V***, fs = 48kHz, ***MCLK = 49.152MHz***, I2S output, w/1kHz full scale

Parameter		*Min*	*Typ*	*Max*	*Unit*
Supply Current during 48kHz 8ch mode					
AVCC			***70.7***		mA
AVDD			***28.6***		mA
Standby					
AVCC			***<1***		uA
AVDD			***<1***		uA

Table 20 - Power consumption test 5

Performance

Test Conditions (unless otherwise noted)

T_A = 25ºC, AVDD = AVCC_CP = AVCC_3V3_L = AVCC_3V3_R = VCCA = +3.3V, fs = 48kHz, **MCLK = 49.152MHz**, I2S input

Parameter			Min	Typ	Max	Unit
Resolution				32		Bit
THD+N Ratio @ fs=48kHz, BW=20Hz-20kHz	8 ch SE mode			-108		dB
	4 ch SE mode			-110		
	4 ch DIFF mode			-112		
	1 ch MONO mode			-112		
DNR A-weighted (w/DRE, w/o APLL)	8 ch SE mode	-60dBFS		120		dB
	4 ch SE mode			123		
	4 ch DIFF mode			125		
	1 ch MONO mode			127		
DNR A-weighted (w/o DRE, w/o APLL)	8 ch SE mode	-60dBFS		113		dB
	4 ch SE mode			116		
	4 ch DIFF mode			117		
	1 ch MONO mode			119		
Interchannel Gain Mismatch				<±0.01	±0.05	dBFS
Output Amplitude	0dB FS SE			2		Vrms
	0dB FS Diff			4		

Table 21 - Device performance

*Note: SE = Single ended output, DIFF = differential (2 DAC channels as a differential pair), Mono = All 8 channels are summed together

Differential mode pairs are Channels 1&2, 3&4, 5&6, 7&8

Register Overview

When the ES9080 is powered up and CHIP_EN is pulled “high”, the default I2C address is 0x90/0x98. The I²C address can be changed to 0x92/0x9A by using Register 192 [2], I2C_ADDR. This is useful if 2 ES9080 devices will be used together as they will require separate I²C address for control.

Order for changing the I²C address:

1) CHIP_EN is pulled high on Device 1, Device 2 is still held in reset
2) I2C_ADDR changed on Device 1 (Address now 0x92)
3) CHIP_EN is pulled high on Device 2.

I²C Slave Interface (Device Address 0x90,0x92)

This interface contains Read/Write and Read-only registers. A system clock must be present.

Multi-byte registers must be written from LSB to MSB. Data is latched when MSB is written.

Multi-byte registers must be read from LSB to MSB. Data is latched when LSB is read.

MSB is always stored in the highest register address.

Read/Write Register Addresses

Registers 0–164 (0x00 – 0xB3) are read/write registers

Read-only Register Addresses

Registers 224 – 255 (0xE0 – 0xFF) are read only registers.

I²C Synchronous Slave Interface (Device Address 0x98,0x9A)

This interface contains Write-only registers. These registers can be written even when there is no system clock present.

When the device is inactive, all peripherals are automatically disabled and all clocks are stopped. A reset can wake the ES9080

Write-only Register Addresses.

Registers 192 – 203 (0xC0 – 0xCB) are write only registers.

Multi-Byte Registers

Multi-byte registers must be written from LSB to MSB. Data is latched when MSB is written.

MSB is always stored in the highest register address.

I²C Slave/Synchronous Slave Interface Timing

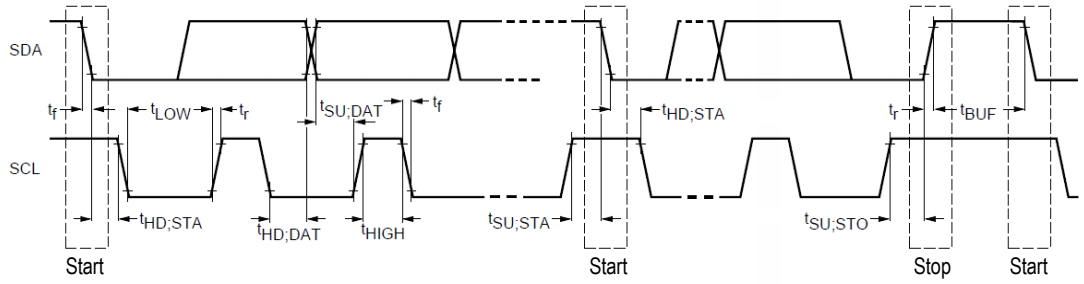


Figure 12 - I2C Slave Control Interface Timing

Parameter	Symbol	CLK Constraint	Standard-Mode		Fast-Mode		Unit
			MIN	MAX	MIN	MAX	
SCL Clock Frequency	f_{SCL}	< CLK/20	0	100	0	400	kHz
START condition hold time	$t_{HD;STA}$		4.0	-	0.6	-	µs
LOW period of SCL	t_{LOW}	>10/CLK	4.7	-	1.3	-	µs
HIGH period of SCL (>10/CLK)	t_{HIGH}	>10/CLK	4.0	-	0.6	-	µs
START condition setup time (repeat)	$t_{SU;STA}$		4.7	-	0.6	-	µs
SDA hold time from SCL falling - All except NACK read - NACK read only	$t_{HD;DAT}$		0 2/CLK	-	0 2/CLK	-	µs s
SDA setup time from SCL rising	$t_{SU;DAT}$		250	-	100	-	ns
Rise time of SDA and SCL	t_r		-	1000		300	ns
Fall time of SDA and SCL	t_f		-	300		300	ns
STOP condition setup time	$t_{SU;STO}$		4	-	0.6	-	µs
Bus free time between transmissions	t_{BUF}		4.7	-	1.3	-	µs
Capacitive load for each bus line	C_b		-	400	-	400	pF

Table 22 - Slave Control Interface Timing Definitions

Register Map

Address (Hex)	Address (Dec)	Register	7	6	5	4	3	2	1	0
0x0	0	SYSTEM CONFIG	SOFT_RESET	ENABLE_2X_MODE	CH78_SEL		CH56_SEL	CH34_SEL	AMP_MODE_REG	RESERVED
0x1	1	CLOCK ENABLE	ENABLE_NSMOD_CH78	ENABLE_NSMOD_CH56	ENABLE_NSMOD_CH34	ENABLE_NSMOD_CH12	ENABLE_DAC_CH78	ENABLE_DAC_CH56	ENABLE_DAC_CH34	ENABLE_DAC_CH12
0x2	2	SYS MODE CONFIG	RESERVED					ENABLE_DOP_DECODE	ENABLE_DSD_DECODE	ENABLE_TDM_DECODE
0x3	3	DAC CONFIG	ENABLE_SPDIF_ENCODE	SELECT_IDAC_HALF	SELECT_IDAC_NUM					
0x4	4	MASTER CLOCK CONFIG	SELECT_MENC_HALF	SELECT_MENC_NUM						
0x5	5	ANALOG DAC ENABLE	ENABLE_ANALOG_DAC_CH8	ENABLE_ANALOG_DAC_CH7	ENABLE_ANALOG_DAC_CH6	ENABLE_ANALOG_DAC_CH5	ENABLE_ANALOG_DAC_CH4	ENABLE_ANALOG_DAC_CH3	ENABLE_ANALOG_DAC_CH2	ENABLE_ANALOG_DAC_CH1
0x6	6	CP CLOCK DIV	CP_CLK_DIV							
0x7	7	ANALOG CTRL DELAY	DAC_REG_DELAY_SEL		FC_LN_DELAY_SEL			SYS_MODE_CLK_GEAR		
0x8-0xC	8-12	RESERVED	RESERVED							
0xD	13	INTERUPT VOL MIN MASK P	VOL_MIN_CH8_MASKP	VOL_MIN_CH7_MASKP	VOL_MIN_CH6_MASKP	VOL_MIN_CH5_MASKP	VOL_MIN_CH4_MASKP	VOL_MIN_CH3_MASKP	VOL_MIN_CH2_MASKP	VOL_MIN_CH1_MASKP
0xE	14	INTERRUPT AUTOMUTE MASKP	DRE_FLAG_CH1_MASKP							AUTOMUTE_FLAG_CH1_MASKP
0xF	15	INTERRUPT DRE MASKP	DRE_FLAG_CH8_MASKP	DRE_FLAG_CH7_MASKP	DRE_FLAG_CH6_MASKP	DRE_FLAG_CH5_MASKP	DRE_FLAG_CH4_MASKP	DRE_FLAG_CH3_MASKP	DRE_FLAG_CH2_MASKP	DRE_FLAG_CH1_MASKP
0x10	16	INTERRUPT SOFT RAMP MASKP	SOFT_RAMP_CH8_MASKP	SOFT_RAMP_CH7_MASKP	SOFT_RAMP_CH6_MASKP	SOFT_RAMP_CH5_MASKP	SOFT_RAMP_CH4_MASKP	SOFT_RAMP_CH3_MASKP	SOFT_RAMP_CH2_MASKP	SOFT_RAMP_CH1_MASKP
0x11	17	INTERRUPT MASK P	INPUT_DATA_TYPE_MASKP		TDM_DATA_VALID_FLAG_MASKP	CLK_AVALID_FLAG_MASKP	RWS_REFERENCE_COUNTER_FULL_FLAG_MASKP	BCK_WS_FAILED_FLAG_MASKP	RESERVED	DOP_VALID_MASKP
0x12	18	RESERVED	RESERVED							
0x13	19	INTERRUPT VOL MIN MASKN	VOL_MIN_CH8_MASKN	VOL_MIN_CH7_MASKN	VOL_MIN_CH6_MASKN	VOL_MIN_CH5_MASKN	VOL_MIN_CH4_MASKN	VOL_MIN_CH3_MASKN	VOL_MIN_CH2_MASKN	VOL_MIN_CH1_MASKN
0x14	20	INTERRUPT AUTOMUTE MASKN	AUTOMUTE_FLAG_CH8_MASKN	AUTOMUTE_FLAG_CH7_MASKN	AUTOMUTE_FLAG_CH6_MASKN	AUTOMUTE_FLAG_CH5_MASKN	AUTOMUTE_FLAG_CH4_MASKN	AUTOMUTE_FLAG_CH3_MASKN	AUTOMUTE_FLAG_CH2_MASKN	AUTOMUTE_FLAG_CH1_MASKN
0x15	21	INTERRUPT DRE MASKN	DRE_FLAG_CH8_MASKN	DRE_FLAG_CH7_MASKN	DRE_FLAG_CH6_MASKN	DRE_FLAG_CH5_MASKN	DRE_FLAG_CH4_MASKN	DRE_FLAG_CH3_MASKN	DRE_FLAG_CH2_MASKN	DRE_FLAG_CH1_MASKN
0x16	22	INTERRUPT SOFT RAMP MASKN	SOFT_RAMP_CH8_MASKN	SOFT_RAMP_CH7_MASKN	SOFT_RAMP_CH6_MASKN	SOFT_RAMP_CH5_MASKN	SOFT_RAMP_CH4_MASKN	SOFT_RAMP_CH3_MASKN	SOFT_RAMP_CH2_MASKN	SOFT_RAMP_CH1_MASKN
0x17	23	INTERRUPT MASK N	INPUT_DATA_TYPE_MASKN		TDM_DATA_VALID_FLAG_MASKN	CLK_AVALID_FLAG_MASKN	RWS_REFERENCE_COUNTER_FULL_FLAG_MASKN	BCK_WS_FAILED_FLAG_MASKN	RESERVED	DOP_VALID_MASKN
0x18	24	RESERVED	RESERVED							
0x19	25	INTERRUPT VOL MIN CLEAR	VOL_MIN_CH8_CLEAR	VOL_MIN_CH7_CLEAR	VOL_MIN_CH6_CLEAR	VOL_MIN_CH5_CLEAR	VOL_MIN_CH4_CLEAR	VOL_MIN_CH3_CLEAR	VOL_MIN_CH2_CLEAR	VOL_MIN_CH1_CLEAR
0x1A	26	INTERRUPT AUTOMUTE CLEAR	AUTOMUTE_FLAG_CH8_CLEAR	AUTOMUTE_FLAG_CH7_CLEAR	AUTOMUTE_FLAG_CH6_CLEAR	AUTOMUTE_FLAG_CH5_CLEAR	AUTOMUTE_FLAG_CH4_CLEAR	AUTOMUTE_FLAG_CH3_CLEAR	AUTOMUTE_FLAG_CH2_CLEAR	AUTOMUTE_FLAG_CH1_CLEAR
0x1B	27	INTERRUPT DRE FLAG CLEAR	DRE_FLAG_CH8_CLEAR	DRE_FLAG_CH7_CLEAR	DRE_FLAG_CH6_CLEAR	DRE_FLAG_CH5_CLEAR	DRE_FLAG_CH4_CLEAR	DRE_FLAG_CH3_CLEAR	DRE_FLAG_CH2_CLEAR	DRE_FLAG_CH1_CLEAR
0x1C	28	INTERRUPT SOFT RAMP CLEAR	SOFT_RAMP_CH8_CLEAR	SOFT_RAMP_CH7_CLEAR	SOFT_RAMP_CH6_CLEAR	SOFT_RAMP_CH5_CLEAR	SOFT_RAMP_CH4_CLEAR	SOFT_RAMP_CH3_CLEAR	SOFT_RAMP_CH2_CLEAR	SOFT_RAMP_CH1_CLEAR
0x1D	29	INTERRUPT CLEAR	INPUT_DATA_CLEAR		TDM_DATA_VALID_CLEAR	CLK_AVALID_FLAG_CLEAR	REFERENCE_COUNTER_FULL_FLAG_CLEAR	BCK_WS_FAILED_FLAG_CLEAR	RESERVED	DOP_VALID_CLEAR
0x1E	30	RESERVED	RESERVED							
0x1F	31	ANALOG CTRL CONFIG	RESERVED		AMP_PDB_ON_SS	AMP_PDB_CLK_INVALID	RESERVED	LP_DAC_REG_R	LP_DAC_REG_L	EN_FCB
0x20-0x22	32-34	RESERVED	RESERVED							
0x23	35	OCP LDRV CTRL	ENB_OCP_LDRV_CH8	ENB_OCP_LDRV_CH6	ENB_OCP_LDRV_CH7	ENB_OCP_LDRV_CH5	ENB_OCP_LDRV_CH4	ENB_OCP_LDRV_CH2	ENB_OCP_LDRV_CH3	ENB_OCP_LDRV_CH1
0x24	36	DAC TRIB CTRL	TRIB_DAC_CH1		TRIB_DAC_CH7		TRIB_DAC_CH4		TRIB_DAC_CH3	
0x25-0x30	37-48	RESERVED	RESERVED							
0x31	49	DIGITAL CTRL OVERRIDE	RESERVED		BCK_WS_FAILED_CONFIG		CLK_AVAILD_CONFIG		RESERVED	
0x32	50	FB_DIV TUNING CONFIG	RESERVED	CLEAR_CLK_REF_CNT	RWS_REF_CNT_SEL			RESERVED		ENABLE_FBDIV_TUNE
0x33	51	RESERVED	RESERVED							

0x34	52	SPDIF CONFIG	SPDIF2_SEL		SPDIF1_SEL		RESERVED		
0x35	53	GPIO1/2 CONFIG	GPIO2_CFG				GPIO1_CFG		
0x36	54	GPIO3/4 CONFIG	GPIO4_CFG				GPIO3_CFG		
0x37	55	GPIO5/6 CONFIG	GPIO6_CFG				GPIO5_CFG		
0x38-0x39	56-57	RESERVED	RESERVED						
0x3A	58	GPIO INVERT AND OUTPUT LOGIC	RESERVED		INVERT_GPIO6	INVERT_GPIO5	INVERT_GPIO4	INVERT_GPIO3	INVERT_GPIO2	INVERT_GPIO1
0x3B	59	GPIO INVERT AND OUTPUT LOGIC	GPIO_OR_SS_RAMP	GPIO_OR_VOL_MIN	GPIO_OR_AUTOMUTE	GPIO_AND_SS_RAMP	GPIO_AND_VOL_MIN	GPIO_AND_AUTOMUTE	RESERVED	
0x3C	60	GPIO WEAK EN AND CH SEL	RESERVED		GPIO6_WK_EN	GPIO5_WK_EN	GPIO4_WK_EN	GPIO3_WK_EN	GPIO2_WK_EN	GPIO1_WK_EN
0x3D	61	GPIO WEAK EN AND CH SEL	RESERVED			GPIO_SEL			RESERVED	
0x3E	62	GPIO INPUT ENABLE	RESERVED		GPIO6_IE	GPIO5_IE	GPIO4_IE	GPIO3_IE	GPIO2_IE	GPIO1_IE
0x3F	63	GPIO INPUT ENABLE	RESERVED						RESERVED	
0x40	64	GPIO OUTPUT ENABLE	RESERVED		GPIO6_OE	GPIO5_OE	GPIO4_OE	GPIO3_OE	GPIO2_OE	GPIO1_OE
0x41	65	GPIO OUTPUT ENABLE	SPDIF_SEL_GPIO6	SPDIF_SEL_GPIO5	SPDIF_SEL_GPIO4	SPDIF_SEL_GPIO3	SPDIF_SEL_GPIO2	SPDIF_SEL_GPIO1	RESERVED	
0x42	66	GPIO READ ENABLE	RESERVED		GPIO6_READ	GPIO5_READ	GPIO4_READ	GPIO3_READ	GPIO2_READ	GPIO1_READ
0x43	67	GPIO READ ENABLE	RESERVED				GPIO_AMP_MODE	GPIO1_AS_DATA8	RESERVED	
0x44	68	PWM1 COUNT	PWM1_COUNT							
0x45	69	PWM1 FREQUENCY	PWM1_FREQ							
0x46	70	PWM1 FREQUENCY	PWM1_FREQ							
0x47	71	PWM2 COUNT	PWM2_COUNT							
0x48	72	PWM2 FREQUENCY	PWM2_FREQ							
0x49	73	PWM2 FREQUENCY	PWM2_FREQ							
0x4A	74	PWM3 COUNT	PWM3_COUNT							
0x4B	75	PWM3 FREQUENCY	PWM3_FREQ							
0x4C	76	PWM3 FREQUENCY	PWM3_FREQ							
0x4D	77	INPUT CONFIG	RESERVED		DSD_MASTER_MODE	ENABLE_MASTER_MODE	INPUT_SEL		AUTO_INPUT_SELECT	
0x4E	78	MASTER MODE CONFIG	RESERVED	MASTER_BCK_DIV1	MASTER_WS_IDLE	MASTER_FRAME_LENGTH		MASTER_WS_PULSE_MODE	MASTER_WS_INVERT	MASTER_BCK_INVERT
0x4F	79	TDM CONFIG1	TDM_RESYNC	MASTER_WS_SCALE			TDM_CH_NUM			
0x50	80	TDM CONFIG2	TDM_LJ_MODE	TDM_VALID_EDGE	TDM_VALID_PULSE_LEN					
0x51	81	TDM CONFIG3	TDM_BIT_WIDTH		TDM_CHAIN_MODE	TDM_DATA_LATCH_ADJ				
0x52	82	BCK/WS MONITOR CONFIG	RESERVED		ENABLE_WS_MONITOR	ENABLE_BCK_MONITOR	BCK_TIMER_DIV			
0x53	83	TDM VALID PULSE CONFIG	TDM_VALID_PULSE_POS							
0x54	84	TDM CH1 CONFIG	TDM_VALID_PULSE_POS_MSB	RESERVED	TDM_CH1_LINE_SEL		TDM_CH1_SLOT_SEL			
0x55	85	TDM CH2 CONFIG	RESERVED		TDM_CH2_LINE_SEL		TDM_CH2_SLOT_SEL			
0x56	86	TDM CH3 CONFIG	RESERVED		TDM_CH3_LINE_SEL		TDM_CH3_SLOT_SEL			
0x57	87	TDM CH4 CONFIG	RESERVED		TDM_CH4_LINE_SEL		TDM_CH4_SLOT_SEL			
0x58	88	TDM CH5 CONFIG	RESERVED		TDM_CH5_LINE_SEL		TDM_CH5_SLOT_SEL			
0x59	89	TDM CH6 CONFIG	RESERVED		TDM_CH6_LINE_SEL		TDM_CH6_SLOT_SEL			
0x5A	90	TDM CH7 CONFIG	RESERVED		TDM_CH7_LINE_SEL		TDM_CH7_SLOT_SEL			
0x5B	91	TDM CH8 CONFIG	RESERVED		TDM_CH8_LINE_SEL		TDM_CH8_SLOT_SEL			
0x5C	92	RESYNC CONFIG	RESERVED			SYNC_DAC_CLK_DIV	DOP_CLK_RESYNC	VOL_THD_RESYNC	FIR_RESYNC	FS_RESYNC
0x5C-0x5D	92-93	RESERVED	RESERVED							
0x5E	94	VOLUME1	VOLUME1							

0x5F	95	VOLUME2	VOLUME2							
0x60	96	VOLUME3	VOLUME3							
0x61	97	VOLUME4	VOLUME4							
0x62	98	VOLUME5	VOLUME5							
0x63	99	VOLUME6	VOLUME6							
0x64	100	VOLUME7	VOLUME7							
0x65	101	VOLUME8	VOLUME8							
0x66	102	DAC VOL UP RATE	DAC_VOL_RATE_UP							
0x67	103	DAC VOL DOWN RATE	DAC_VOL_RATE_DOWN							
0x68	104	DAC VOL DOWN RATE FAST	DAC_VOL_RATE_FAST							
0x69	105	VOLUME AND MONO CTRL	RESERVED	FORCE_VOLUME	DAC_USE_MONO_VOLUME	RUN_VOLUME	RESERVED			
0x6A	106	MUTE CTRL	DAC_MUTE_CH8	DAC_MUTE_CH7	DAC_MUTE_CH6	DAC_MUTE_CH5	DAC_MUTE_CH4	DAC_MUTE_CH3	DAC_MUTE_CH2	DAC_MUTE_CH1
0x6B	107	DATA INVERT CTRL	DAC_INVERT_CH8	DAC_INVERT_CH7	DAC_INVERT_CH6	DAC_INVERT_CH5	DAC_INVERT_CH4	DAC_INVERT_CH3	DAC_INVERT_CH2	DAC_INVERT_CH1
0x6C	108	FILTER CONFIG	RESERVED	BYPASS_DEEMPH	PEAK_FILTER	SEL_DEEMPH		FILTER_SHAPE		
0x6D	109	IIR Config	IIR_DITHER_SCALE		RESERVED			IIR1_BW		
0x6E	110	RESERVED	RESERVED							
0x6F	111	THD COMP C2 CH1/3/5/7	THD_C2_CH1357							
0x70	112	THD COMP C2 CH1/3/5/7	THD_C2_CH1357							
0x71	113	THD COMP C3 CH1/3/5/7	THD_C3_CH1357							
0x72	114	THD COMP C3 CH1/3/5/7	THD_C3_CH1357							
0x73	115	THD COMP C2 CH2/4/6/8	THD_C2_CH2468							
0x74	116	THD COMP C2 CH2/4/6/8	THD_C2_CH2468							
0x75	117	THD COMP C3 CH2/4/6/8	THD_C3_CH2468							
0x76	118	THD COMP C3 CH2/4/6/8	THD_C3_CH2468							
0x77	119	AUTOMUTE ENABLE	AUTOMUTE_EN_CH8	AUTOMUTE_EN_CH7	AUTOMUTE_EN_CH6	AUTOMUTE_EN_CH5	AUTOMUTE_EN_CH4	AUTOMUTE_EN_CH3	AUTOMUTE_EN_CH2	AUTOMUTE_EN_CH1
0x78	120	AUTOMUTE TIME	AUTOMUTE_TIME							
0x79	121	AUTOMUTE TIME	AUTOMUTE_RAMP_TO_GROUND	AUTOMUTE_WAIT_ON_DRE	RESERVED			AUTOMUTE_TIME		
0x7A	122	AUTOMUTE LEVEL	AUTOMUTE_LEVEL							
0x7B	123	AUTOMUTE LEVEL	AUTOMUTE_LEVEL							
0x7C	124	AUTOMUTE OFF LEVEL	AUTOMUTE_OFF_LEVEL							
0x7D	125	AUTOMUTE OFF LEVEL	AUTOMUTE_OFF_LEVEL							
0x7E	126	SOFT RAMP CONFIG	RESERVED		SOFT_RAMP_TYPE	SOFT_RAMP_TIME				
0x7F	127	RESERVED	RESERVED							
0x80	128	NSMOD DITHER INVERT	NSMOD_DITHER_INVERT_CH8	NSMOD_DITHER_INVERT_CH7	NSMOD_DITHER_INVERT_CH6	NSMOD_DITHER_INVERT_CH5	NSMOD_DITHER_INVERT_CH4	NSMOD_DITHER_INVERT_CH3	NSMOD_DITHER_INVERT_CH2	NSMOD_DITHER_INVERT_CH1
0x81	129	NSMOD AND DITHER CONFIG	RESERVED	IIR_DITHER_SEL			RESERVED	ENABLE_1_8TH_GAIN_MODE	RESERVED	
0x82	130	RESERVED	RESERVED							
0x83	131	NSMOD DITHER CH12	DITHER_SCALE_CH2				DITHER_SCALE_CH1			
0x84	132	NSMOD DITHER CH34	DITHER_SCALE_CH4				DITHER_SCALE_CH3			
0x85	133	NSMOD DITHER CH56	DITHER_SCALE_CH6				DITHER_SCALE_CH5			
0x86	134	NSMOD DITHER CH78	DITHER_SCALE_CH8				DITHER_SCALE_CH7			
0x87	135	MIN_PEAK	RESERVED							MIN_PEAK
0x88-0x8B	136-139	RESERVED	RESERVED							
0x89	136	DRE ATT EN AND THDR CTRL	DRE_THDR_CTRL_CH78	DRE_THDR_CTRL_CH56	DRE_THDR_CTRL_CH34	DRE_THDR_CTRL_CH12	DRE_ATT_ENABLE_CH78	DRE_ATT_ENABLE_CH56	DRE_ATT_ENABLE_CH34	DRE_ATT_ENABLE_CH12
0x8A-0x8	137-138	RESERVED	RESERVED							
0x8B	139	DRE FORCE	DRE_FORCE_CH8	DRE_FORCE_CH6	DRE_FORCE_CH4	DRE_FORCE_CH2	DRE_FORCE_CH7	DRE_FORCE_CH5	DRE_FORCE_CH3	DRE_FORCE_CH1
0x8C	140	DRE GAIN CH1/3/5/7	DRE_GAIN1357							

0x8D	141	DRE GAIN CH1/3/5/7	DRE_GAIN1357						
0x8E	142	DRE GAIN CH2/4/6/8	DRE_GAIN2468						
0x8F	143	DRE GAIN CH2/4/6/8	DRE_GAIN2468						
0x90	144	DRE ON THRESHOLD	DRE_ON_THRESH						
0x91	145	DRE ON THRESHOLD	DRE_ON_THRESH						
0x92	146	DRE OFF THRESHOLD	DRE_OFF_THRESH						
0x93	147	DRE OFF THRESHOLD	DRE_OFF_THRESH						
0x94	148	DRE DECAY RATE	DRE_FORCE_LEVEL	RESERVED	DRE_DECAY_RATE				
0x95	149	DC OFFSET CH1/3/5/7	DC_OFFSET1357						
0x96	150	DC OFFSET CH1/3/5/7	DC_OFFSET1357						
0x97	151	DC OFFSET CH2/4/6/8	DC_OFFSET2468						
0x98	152	DC OFFSET CH2/4/6/8	DC_OFFSET2468						
0x99	153	DC RAMP RATE	DC_RAMP_RATE						
0x9A	154	GAIN 18DB	GAIN_18DB_CH8	GAIN_18DB_CH6	GAIN_18DB_CH4	GAIN_18DB_CH2	GAIN_18DB_CH7	GAIN_18DB_CH5	GAIN_18DB_CH3	GAIN_18DB_CH1
0x9B	155	SPDIF1 CS	SPDIF1_CS						
0x9C	156	SPDIF1 CS	SPDIF1_CS						
0x9D	157	SPDIF1 CS	SPDIF1_CS						
0x9E	158	SPDIF1 CS	SPDIF1_CS						
0x9F	159	SPDIF1 CS	SPDIF1_CS						
0xA0	160	SPDIF2 CS	SPDIF2_CS						
0xA1	161	SPDIF2 CS	SPDIF2_CS						
0xA2	162	SPDIF2 CS	SPDIF2_CS						
0xA3	163	SPDIF2 CS	SPDIF2_CS						
0xA4	164	SPDIF2 CS	SPDIF2_CS						
0xC0	192	PLL REGISTER1	AO_SOFT_RESET	PLL_SOFT_RESET	RESERVED			I2C_ADDR	GPIO1_SDB_AO	PLL_CLKHV_PHASE_INV
0xC1	193	PLL REGISTER2	PLL_BYP	DVDD_SHUNTB	SEL_1V_DREG	PLL_HVREG_VREF_SEL		SEL_PLL_IN		EN_PLL_CLKIN
0xC2	194	PLL REGISTER3	RESERVED					AUTO_LOCK_EN	RESERVED	
0xC3	195	PLL REGISTER4	PLL_CP_BIAS_SEL			PLL_ID_SEL		PLL_VCO_FMAX	PLL_VCO_PDB	PLL_CP_PDB
0xC4	196	RESERVED	RESERVED							
0xC5	197	PLL REGISTER6	PLL_CLK_FB_DIV							
0xC6	198	PLL REGISTER6	PLL_CLK_FB_DIV							
0xC7	199	PLL REGISTER6	PLL_CLK_FB_DIV							
0xC8	200	PLL REGISTER7	PLL_CLK_IN_DIV							PLL_FB_DIV_LOAD
0xC9	201	PLL REGISTER7	PLL_CLK_OUT_DIV						PLL_CLK_IN_DIV	
0xCA	202	PLL REGISTER7	PLL_REG_PDB	RESERVED			PLL_LOW_BW	PLL_CLK_OUT_DIV		
0xCB	203	PLL REGISTER8	PLL_VCO_FLIMIT_CTRL	PLL_DIG_RSTB	PLL_VCO_DIODE_EN	RESERVED				PLL_RCOSC_EN
0xE0	224	SYS READ	RESERVED						ADDR	RESERVED
0xE1	225	CHIP ID READ	CHIP_ID							
0xE2-0xE4	226-228	RESERVED	RESERVED							
0xE5	229	INTERRUPT STATE	INTERRUPT_STATE							
0xE6	230	INTERRUPT STATE	INTERRUPT_STATE							
0xE7	231	INTERRUPT STATE	INTERRUPT_STATE							
0xE8	232	INTERRUPT STATE	INTERRUPT_STATE							
0xE9	233	INTERRUPT STATE	INTERRUPT_STATE							
0xEA	234	INTERRUPT STATE	INTERRUPT_STATE							
0xEB	235	INTERRUPT SOURCE	INTERRUPT_SOURCES							
0xEC	236	INTERRUPT SOURCE	INTERRUPT_SOURCES							
0xED	237	INTERRUPT SOURCE	INTERRUPT_SOURCES							

0xEE	238	INTERRUPT SOURCE	INTERRUPT_SOURCES							
0xEF	239	INTERRUPT SOURCE	INTERRUPT_SOURCES							
0xF0	240	INTERRUPT SOURCE	INTERRUPT_SOURCES							
0xF1	241	RWS REF CNT STATUS	RWS_REF_CNT							
0xF2	242	RWS REF CNT STATUS	RWS_REF_CNT							
0xF3	243	RWS REF CNT STATUS	RWS_REF_CNT							
0xF4	244	RWS REF CNT STATUS	RWS_REF_CNT	RESERVED					RWS_REF_CNT	
0xF5-0xF6	245-246	RESERVED	RESERVED							
0xF7	247	GPIO AND JD CMP READ	GPIO_I_READ							
0xF8	248	GPIO AND JD CMP READ	GPIO_I_READ	RESERVED					GPIO_I_READ	
0xF9	249	AUTOMUTE READ	AUTOMUTE_CH8	AUTOMUTE_CH7	AUTOMUTE_CH6	AUTOMUTE_CH5	AUTOMUTE_CH4	AUTOMUTE_CH3	AUTOMUTE_CH2	AUTOMUTE_CH1
0xFA	250	VOL MIN READ	VOL_MIN_CH8	VOL_MIN_CH7	VOL_MIN_CH6	VOL_MIN_CH5	VOL_MIN_CH4	VOL_MIN_CH3	VOL_MIN_CH2	VOL_MIN_CH1
0xFB	251	SOFT RAMP UP READ	SS_RAMP_UP_CH8	SS_RAMP_UP_CH7	SS_RAMP_UP_CH6	SS_RAMP_UP_CH5	SS_RAMP_UP_CH4	SS_RAMP_UP_CH3	SS_RAMP_UP_CH2	SS_RAMP_UP_CH1
0xFC	252	SOFT RAMP DOWN READ	SS_RAMP_DOWN_CH8	SS_RAMP_DOWN_CH7	SS_RAMP_DOWN_CH6	SS_RAMP_DOWN_CH5	SS_RAMP_DOWN_CH4	SS_RAMP_DOWN_CH3	SS_RAMP_DOWN_CH2	SS_RAMP_DOWN_CH1
0xFD	253	DRE STATUS READ	DRE_SELECT_CH8	DRE_SELECT_CH6	DRE_SELECT_CH4	DRE_SELECT_CH2	DRE_SELECT_CH7	DRE_SELECT_CH5	DRE_SELECT_CH3	DRE_SELECT_CH1
0xFE	254	DRE DETECT READ	DRE_DETECT_CH8	DRE_DETECT_CH6	DRE_DETECT_CH4	DRE_DETECT_CH2	DRE_DETECT_CH7	DRE_DETECT_CH5	DRE_DETECT_CH3	DRE_DETECT_CH1
0xFF	255	DATA FLAG READ	RESERVED	TDM_DATA_VALID	DOP_VALID_CH78	DOP_VALID_CH56	DOP_VALID_CH34	DOP_VALID_CH12	RESERVED	

Table 23 - Register map

Register Listings

Some RESERVED registers do not default to 0x00 and should not be modified for normal operation. If the value of the reserved registers is changed from the default state, it will be noted.

System Registers

Register 0: SYSTEM CONFIG

Bits	[7]	[6]	[5:2]	[1]	[0]
Default	1'b0	1'b0	4'b0000	1'b0	1'b0

Bits	Mnemonic	Description
[7]	SOFT_RESET	Performs soft reset to digital core except for the PLL Registers. • 1'b0: Disabled (default) • 1'b1: Enabled
[6]	ENABLE_2X_MODE	Enables 2x mode for 768k sample rate. • 1'b0: 2x mode disabled (default) • 1'b1: 2x mode enabled
[5:2]	RESERVED	NA
[1]	AMP_MODE_REG	System mode settings. • 1'b0: Power Down (default) • 1'b1: HIFI
[0]	RESERVED	NA

Register 1: CLOCK ENABLE

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	ENABLE_NSMOD_CH78	Enables ch78 nsmod clock. • 1'b0: Clock disabled (default) • 1'b1: Clock enabled
[6]	ENABLE_NSMOD_CH56	Enables ch56 nsmod clock. • 1'b0: Clock disabled (default) • 1'b1: Clock enabled
[5]	ENABLE_NSMOD_CH34	Enables ch34 nsmod clock. • 1'b0: Clock disabled (default) • 1'b1: Clock enabled
[4]	ENABLE_NSMOD_CH12	Enables ch12 nsmod clock. • 1'b0: Clock disabled (default) • 1'b1: Clock enabled
[3]	ENABLE_DAC_CH78	Enables DAC ch78 interpolation path clock. • 1'b0: Clock disabled (default) • 1'b1: Clock enabled
[2]	ENABLE_DAC_CH56	Enables DAC ch56 interpolation path clock. • 1'b0: Clock disabled (default) • 1'b1: Clock enabled
[1]	ENABLE_DAC_CH34	Enables DAC ch34 interpolation path clock. • 1'b0: Clock disabled (default) • 1'b1: Clock enabled
[0]	ENABLE_DAC_CH12	Enables DAC ch12 interpolation path clock. • 1'b0: Clock disabled (default) • 1'b1: Clock enabled

Register 2: SYS MODE CONFIG

Bits	[7:3]	[2]	[1]	[0]
Default	5'b00000	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7:3]	RESERVED	NA
[2]	ENABLE_DOP_DECODE	Enables DoP decoding. • 1'b0: Disabled (default) • 1'b1: Enabled
[1]	ENABLE_DSD_DECODE	Enables DSD decoding. • 1'b0: Disabled (default) • 1'b1: Enabled
[0]	ENABLE_TDM_DECODE	Enables TDM decoding. • 1'b0: Disabled (default) • 1'b1: Enabled

Register 3: DAC CONFIG

Bits	[7]	[6]	[5:0]
Default	1'b0	1'b0	6'd0

Bits	Mnemonic	Description
[7]	ENABLE_SPDIF_ENCODE	Enable S/PDIF Encoding • 1'b0: Disabled (default) • 1'b1: S/PDIF encoding enabled
[6]	SELECT_IDAC_HALF	Specifies whether to half CLK_IDAC divider. • 1'b0: Divide by SELECT_IDAC_NUM + 1 (default) • 1'b1: Divide by half of SELECT_IDAC_NUM + 1 Note: Can only produce half of an odd number divide
[5:0]	SELECT_IDAC_NUM	CLK_IDAC divider. Whole number divide value + 1 for CLK_IDAC (SYS_CLK/divide_value). • 6'd0: Whole number divide value + 1 = 1 (default) • 6'd1: Whole number divide value + 1 = 2 • 6'd63: Whole number divide value + 1 = 64

Register 4: MASTER CLOCK CONFIG

Bits	[7]	[6:0]
Default	1'b0	7'd0

Bits	Mnemonic	Description
[7]	SELECT_MENC_HALF	Master Encoder (MENC) division select. • 1'b0: Divide by SELECT_MENC_NUM + 1 (default) • 1'b1: Divide by half of SELECT_MENC_NUM + 1 Note: Can only produce half of an odd number divide
[6:0]	SELECT_MENC_NUM	Master mode clock divider. Whole number divide value + 1 for CLK_Master (SYS_CLK/divide_value). • 7'd0: Whole number divide value + 1 = 1 (default) • 7'd1: Whole number divide value + 1 = 2 • 7'd127: Whole number divide value + 1 = 128

Register 5: ANALOG DAC ENABLE

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b1	1'b1

Bits	Mnemonic	Description
[7]	ENABLE_ANALOG_DAC_CH8	Enables ch8 analog DAC. • 1'b0: Disabled (default) • 1'b1: Enabled
[6]	ENABLE_ANALOG_DAC_CH7	Enables ch7 analog DAC. • 1'b0: Disabled (default) • 1'b1: Enabled
[5]	ENABLE_ANALOG_DAC_CH6	Enables ch6 analog DAC. • 1'b0: Disabled (default) • 1'b1: Enabled
[4]	ENABLE_ANALOG_DAC_CH5	Enables ch5 analog DAC. • 1'b0: Disabled (default) • 1'b1: Enabled
[3]	ENABLE_ANALOG_DAC_CH4	Enables ch4 analog DAC. • 1'b0: Disabled (default) • 1'b1: Enabled
[2]	ENABLE_ANALOG_DAC_CH3	Enables ch3 analog DAC. • 1'b0: Disabled (default) • 1'b1: Enabled
[1]	ENABLE_ANALOG_DAC_CH2	Enables ch2 analog DAC. • 1'b0: Disabled • 1'b1: Enabled (default)
[0]	ENABLE_ANALOG_DAC_CH1	Enables ch1 analog DAC. • 1'b0: Disabled • 1'b1: Enabled (default)

Register 6: CP CLOCK DIV

Bits	[7:0]
Default	8'd6

Bits	Mnemonic	Description
[7:0]	CP_CLK_DIV	Specifies the clk divider for the CP clock source. Valid from 8'd0 to 8'd255. • 8'd6: Default • 8'dx: CP clock is SYS_CLK/((x+1)*2) Note: CP_CLK_DIV value should reflect a CP clock source frequency of between 500kHz-1MHz

Register 7: ANALOG CTRL DELAY

Bits	[7:6]	[5:3]	[2:0]
Default	2'd2	3'd5	3'd3

Bits	Mnemonic	Description
[7:6]	DAC_REG_DELAY_SEL	Sets the delay between DAC reference is enabled and DAC regulators are enabled. • 2'd0: zero delay • 2'd1: (5ms * (50MHz / FSYS_CLK)) / 2^SYS_MODE_CLK_GEAR • 2'd2: (10ms * (50MHz / FSYS_CLK)) / 2^SYS_MODE_CLK_GEAR (default) • 2'd3: (20ms * (50MHz / FSYS_CLK)) / 2^SYS_MODE_CLK_GEAR
[5:3]	FC_LN_DELAY_SEL	Sets the delay between DAC reference is enabled and LN mode is enabled. • 3'd0: zero delay • 3'd1: (20ms * (50MHz / FSYS_CLK)) / 2^SYS_MODE_CLK_GEAR • 3'd2: (40ms * (50MHz / FSYS_CLK)) / 2^SYS_MODE_CLK_GEAR • 3'd3: (80ms * (50MHz / FSYS_CLK)) / 2^SYS_MODE_CLK_GEAR • 3'd4: (160ms * (50MHz / FSYS_CLK)) / 2^SYS_MODE_CLK_GEAR • 3'd5: (200ms * (50MHz / FSYS_CLK)) / 2^SYS_MODE_CLK_GEAR (default) • 3'd6: (400ms * (50MHz / FSYS_CLK)) / 2^SYS_MODE_CLK_GEAR • 3'd7: (800ms * (50MHz / FSYS_CLK)) / 2^SYS_MODE_CLK_GEAR
[2:0]	SYS_MODE_CLK_GEAR	Speeds up analog control delays by 2^SYS_MODE_CLK_GEAR times. • 3'd3: Default

Register 8: CP SOFT START DELAY

Bits	[7:0]
Default	8'd30

Bits	Mnemonic	Description
[7:0]	SS_DELAY_SM_MCP	Sets the delay between when weak mode is enabled and when strong mode is enabled during the variable charge pump soft start. $Delay = (4096 * SS\_DELAY\_SM\_MCP / FSYS\_CLK) / 2\text{^}SYS\_MODE\_CLK\_GEAR$

Register 12-9: RESERVED

Register 13: INTERUPT VOL MIN MASK P

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	VOL_MIN_CH8_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[6]	VOL_MIN_CH7_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[5]	VOL_MIN_CH6_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[4]	VOL_MIN_CH5_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[3]	VOL_MIN_CH4_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[2]	VOL_MIN_CH3_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[1]	VOL_MIN_CH2_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[0]	VOL_MIN_CH1_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive

Register 14: INTERRUPT AUTOMUTE MASKP

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	AUTOMUTE_FLAG_CH8_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[6]	AUTOMUTE_FLAG_CH7_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[5]	AUTOMUTE_FLAG_CH6_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[4]	AUTOMUTE_FLAG_CH5_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[3]	AUTOMUTE_FLAG_CH4_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[2]	AUTOMUTE_FLAG_CH3_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[1]	AUTOMUTE_FLAG_CH2_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[0]	AUTOMUTE_FLAG_CH1_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive

Register 15: INTERRUPT DRE MASKP

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	DRE_FLAG_CH8_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[6]	DRE_FLAG_CH7_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[5]	DRE_FLAG_CH6_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[4]	DRE_FLAG_CH5_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[3]	DRE_FLAG_CH4_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[2]	DRE_FLAG_CH3_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[1]	DRE_FLAG_CH2_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[0]	DRE_FLAG_CH1_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive

Register 16: INTERRUPT SOFT RAMP MASKP

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	SOFT_RAMP_CH8_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[6]	SOFT_RAMP_CH7_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[5]	SOFT_RAMP_CH6_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[4]	SOFT_RAMP_CH5_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[3]	SOFT_RAMP_CH4_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[2]	SOFT_RAMP_CH3_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[1]	SOFT_RAMP_CH2_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[0]	SOFT_RAMP_CH1_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive

Register 18-17: INTERRUPT MASK P

Bits	[15:8]	[7:6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	8'b00000000	2'b00	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[15:8]	RESERVED	NA
[7:6]	INPUT_DATA_TYPE_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[5]	TDM_DATA_VALID_FLAG_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[4]	CLK_AVALID_FLAG_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[3]	RWS_REFERENCE_COUNTER_FULL_FLAG_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[2]	BCK_WS_FAILED_FLAG_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[1]	RESERVED	NA
[0]	DOP_VALID_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive

Register 19: INTERRUPT VOL MIN MASKN

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	VOL_MIN_CH8_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[6]	VOL_MIN_CH7_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[5]	VOL_MIN_CH6_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[4]	VOL_MIN_CH5_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[3]	VOL_MIN_CH4_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[2]	VOL_MIN_CH3_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[1]	VOL_MIN_CH2_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[0]	VOL_MIN_CH1_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative

Register 20: INTERRUPT AUTOMUTE MASKN

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	AUTOMUTE_FLAG_CH8_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[6]	AUTOMUTE_FLAG_CH7_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[5]	AUTOMUTE_FLAG_CH6_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[4]	AUTOMUTE_FLAG_CH5_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[3]	AUTOMUTE_FLAG_CH4_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[2]	AUTOMUTE_FLAG_CH3_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[1]	AUTOMUTE_FLAG_CH2_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[0]	AUTOMUTE_FLAG_CH1_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative

Register 21: INTERRUPT DRE MASKN

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	DRE_FLAG_CH8_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[6]	DRE_FLAG_CH7_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[5]	DRE_FLAG_CH6_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[4]	DRE_FLAG_CH5_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[3]	DRE_FLAG_CH4_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[2]	DRE_FLAG_CH3_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[1]	DRE_FLAG_CH2_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[0]	DRE_FLAG_CH1_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative

Register 22: INTERRUPT SOFT RAMP MASKN

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	SOFT_RAMP_CH8_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[6]	SOFT_RAMP_CH7_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[5]	SOFT_RAMP_CH6_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[4]	SOFT_RAMP_CH5_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[3]	SOFT_RAMP_CH4_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[2]	SOFT_RAMP_CH3_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[1]	SOFT_RAMP_CH2_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[0]	SOFT_RAMP_CH1_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative

Register 24-23: INTERRUPT MASK N

Bits	[15:8]	[7:6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	8'b00000000	2'b00	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[15:8]	RESERVED	NA
[7:6]	INPUT_DATA_TYPE_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[5]	TDM_DATA_VALID_FLAG_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[4]	CLK_AVALID_FLAG_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[3]	RWS_REFERENCE_COUNTER_FULL_FLAG_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[2]	BCK_WS_FAILED_FLAG_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[1]	RESERVED	NA
[0]	DOP_VALID_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative

Register 25: INTERRUPT VOL MIN CLEAR

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	VOL_MIN_CH8_CLEAR	Write a 1'b1 to clear the interrupt
[6]	VOL_MIN_CH7_CLEAR	Write a 1'b1 to clear the interrupt
[5]	VOL_MIN_CH6_CLEAR	Write a 1'b1 to clear the interrupt
[4]	VOL_MIN_CH5_CLEAR	Write a 1'b1 to clear the interrupt
[3]	VOL_MIN_CH4_CLEAR	Write a 1'b1 to clear the interrupt
[2]	VOL_MIN_CH3_CLEAR	Write a 1'b1 to clear the interrupt
[1]	VOL_MIN_CH2_CLEAR	Write a 1'b1 to clear the interrupt
[0]	VOL_MIN_CH1_CLEAR	Write a 1'b1 to clear the interrupt

Register 26: INTERRUPT AUTOMUTE CLEAR

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	AUTOMUTE_FLAG_CH8_CLEAR	Write a 1'b1 to clear the interrupt
[6]	AUTOMUTE_FLAG_CH7_CLEAR	Write a 1'b1 to clear the interrupt
[5]	AUTOMUTE_FLAG_CH6_CLEAR	Write a 1'b1 to clear the interrupt
[4]	AUTOMUTE_FLAG_CH5_CLEAR	Write a 1'b1 to clear the interrupt
[3]	AUTOMUTE_FLAG_CH4_CLEAR	Write a 1'b1 to clear the interrupt
[2]	AUTOMUTE_FLAG_CH3_CLEAR	Write a 1'b1 to clear the interrupt
[1]	AUTOMUTE_FLAG_CH2_CLEAR	Write a 1'b1 to clear the interrupt
[0]	AUTOMUTE_FLAG_CH1_CLEAR	Write a 1'b1 to clear the interrupt

Register 27: INTERRUPT DRE FLAG CLEAR

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	DRE_FLAG_CH8_CLEAR	Write a 1'b1 to clear the interrupt
[6]	DRE_FLAG_CH7_CLEAR	Write a 1'b1 to clear the interrupt
[5]	DRE_FLAG_CH6_CLEAR	Write a 1'b1 to clear the interrupt
[4]	DRE_FLAG_CH5_CLEAR	Write a 1'b1 to clear the interrupt
[3]	DRE_FLAG_CH4_CLEAR	Write a 1'b1 to clear the interrupt
[2]	DRE_FLAG_CH3_CLEAR	Write a 1'b1 to clear the interrupt
[1]	DRE_FLAG_CH2_CLEAR	Write a 1'b1 to clear the interrupt
[0]	DRE_FLAG_CH1_CLEAR	Write a 1'b1 to clear the interrupt

Register 28: INTERRUPT SOFT RAMP CLEAR

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	SOFT_RAMP_CH8_CLEAR	Write a 1'b1 to clear the interrupt
[6]	SOFT_RAMP_CH7_CLEAR	Write a 1'b1 to clear the interrupt
[5]	SOFT_RAMP_CH6_CLEAR	Write a 1'b1 to clear the interrupt
[4]	SOFT_RAMP_CH5_CLEAR	Write a 1'b1 to clear the interrupt
[3]	SOFT_RAMP_CH4_CLEAR	Write a 1'b1 to clear the interrupt
[2]	SOFT_RAMP_CH3_CLEAR	Write a 1'b1 to clear the interrupt
[1]	SOFT_RAMP_CH2_CLEAR	Write a 1'b1 to clear the interrupt
[0]	SOFT_RAMP_CH1_CLEAR	Write a 1'b1 to clear the interrupt

Register 30-29: INTERRUPT CLEAR

Bits	[15:8]	[7:6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	8'b00000000	2'b00	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[15:8]	RESERVED	NA
[7:6]	INPUT_DATA_CLEAR	Write a 1'b1 to clear the interrupt
[5]	TDM_DATA_VALID_CLEAR	Write a 1'b1 to clear the interrupt
[4]	CLK_AVALID_FLAG_CLEAR	Write a 1'b1 to clear the interrupt
[3]	RWS_REFERENCE_COUNTER_FULL_FLAG_CLEAR	Write a 1'b1 to clear the interrupt
[2]	BCK_WS_FAILED_FLAG_CLEAR	Write a 1'b1 to clear the interrupt
[1]	RESERVED	NA
[0]	DOP_VALID_CLEAR	Write a 1'b1 to clear the interrupt

Register 31: ANALOG CTRL CONFIG

Bits	[7:6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	2'd0	1'b0	1'b1	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7:6]	RESERVED	NA
[5]	AMP_PDB_ON_SS	DAC amp power control for soft ramp on normal mute. • 1'b0: When soft ramped to ground during normal mute, keeps DAC AMP on • 1'b1: When soft ramped to ground during normal mute allow DAC AMP to shut down for power saving (default) "normal mute" includes: automute, mute by register, mute by GPIO
[4]	AMP_PDB_CLK_INVALID	DAC amp power control for soft ramp on abnormal mute. • 1'b0: When soft ramped to ground during abnormal mute, keeps DAC AMP on • 1'b1: When soft ramped to ground during abnormal mute allow DAC AMP to shut down for power saving (default) "abnormal mute" includes: PLL unlock, BCK_WS ratio failed
[3]	RESERVED	NA
[2]	LP_DAC_REG_R	Set the low power mode for DAC regulator (Right) • 1'b0: Normal Mode (default) • 1'b1: Low power mode enabled
[1]	LP_DAC_REG_L	Set the low power mode for DAC regulator (Left) • 1'b0: Normal Mode (default) • 1'b1: Low power mode enabled
[0]	EN_FCB	Enable the fast charge for VREF_L AND VREF_R • 1'b0: Enabled (default) • 1'b1: Disable fast charge

Register 34-32: RESERVED

Register 35: OCP LDRV CTRL

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	ENB_OCP_LDRV_CH8	Line driver over current protection • 1'b0: Enable • 1'b1: Disable
[6]	ENB_OCP_LDRV_CH6	Line driver over current protection • 1'b0: Enable • 1'b1: Disable
[5]	ENB_OCP_LDRV_CH7	Line driver over current protection • 1'b0: Enable • 1'b1: Disable
[4]	ENB_OCP_LDRV_CH5	Line driver over current protection • 1'b0: Enable • 1'b1: Disable
[3]	ENB_OCP_LDRV_CH4	Line driver over current protection • 1'b0: Enable • 1'b1: Disable
[2]	ENB_OCP_LDRV_CH2	Line driver over current protection • 1'b0: Enable • 1'b1: Disable
[1]	ENB_OCP_LDRV_CH3	Line driver over current protection • 1'b0: Enable • 1'b1: Disable
[0]	ENB_OCP_LDRV_CH1	Line driver over current protection • 1'b0: Enable • 1'b1: Disable

Register 36: DAC TRIB CTRL

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b1	1'b1	1'b1	1'b1	1'b1	1'b1	1'b1	1'b1

Bits	Mnemonic	Description
[7]	TRIB_DAC_CH8	Set DAC output tri-state • 1'b0: tri-state • 1'b1: Normal operation
[6]	TRIB_DAC_CH6	Set DAC output tri-state • 1'b0: tri-state • 1'b1: Normal operation
[5]	TRIB_DAC_CH7	Set DAC output tri-state • 1'b0: tri-state • 1'b1: Normal operation
[4]	TRIB_DAC_CH5	Set DAC output tri-state • 1'b0: tri-state • 1'b1: Normal operation
[3]	TRIB_DAC_CH4	Set DAC output tri-state • 1'b0: tri-state • 1'b1: Normal operation
[2]	TRIB_DAC_CH2	Set DAC output tri-state • 1'b0: tri-state • 1'b1: Normal operation
[1]	TRIB_DAC_CH3	Set DAC output tri-state • 1'b0: tri-state • 1'b1: Normal operation
[0]	TRIB_DAC_CH1	Set DAC output tri-state • 1'b0: tri-state • 1'b1: Normal operation

Register 48-37: RESERVED

Register 49: DIGITAL CTRL OVERRIDE

Bits	[7:6]	[5:4]	[3:2]	[1:0]
Default	2'd0	2'd0	2'd0	2'd0

Bits	Mnemonic	Description
[7:6]	RESERVED	NA
[5:4]	BCK_WS_FAILED_CONFIG	When BCK/WS ratio fails: • 2'b00: No operation (default) • 2'b01: Reserved • 2'b10: Force DAC to AVCC/2 • 2'b11: Force DAC to ground
[3:2]	CLK_AVALID_CONFIG	When SYS_CLK clock fails: • 2'b00: No operation (default) • 2'b01: Force DAC power down • 2'b10: Force DAC to AVCC/2 • 2'b11: Force DAC to ground
[1:0]	RESERVED	NA

Register 50: FB_DIV TUNING CONFIG

Bits	[7]	[6]	[5:3]	[2:1]	[0]
Default	1'b0	1'b0	3'd0	2'd0	1'b0

Bits	Mnemonic	Description
[7]	RESERVED	NA
[6]	CLEAR_CLK_REF_CNT	Write 1 to clear/disable RWS_REF counter, then write 0 to start the counter. 0 by default.
[5:3]	RWS_REF_CNT_SEL	The RWS_REF counter will count for N RWS pos edges using CLK_IDAC. N is: • 3'd0: 256 (default) • 3'd1: 512 • 3'd2: 1024 • 3'd3: 2048 • 3'd4: 4096 • 3'd5: 8192 • 3'd6: 16384 • 3'd7: 32768
[2:1]	RESERVED	NA
[0]	ENABLE_FBDIV_TUNE	Enables FB_DIV tuning logic using the RWS_REF counter. • 1'b0: Disabled (default) • 1'b1: Enabled

Register 51: FORCE PLL LOCK CONFIG

Bits	[7]	[6:0]
Default	1'b0	7'd0

Bits	Mnemonic	Description
[7]	FORCE_PLL_LOCK	• 1'b0: PLL clock status is indicated by PLL_LOCKED: 0->PLL unlocked, 1->PLL locked (default) • 1'b1: Ignores PLL_LOCKED and forces PLL clock status to be locked **Note: This must be set to ensure the DAC does not mute itself**
[6:0]	RESERVED	NA

Register 52: SPDIF CONFIG

Bits	[7:6]	[5:4]	[3:0]
Default	2'd0	2'd0	4'b0000

Bits	Mnemonic	Description
[7:6]	SPDIF2_SEL	Selects 2nd SPDIF encoder input. • 2'b00: Ch1/2 • 2'b01: Ch3/4 • 2'b10: Ch5/6 • 2'b11: Ch7/8
[5:4]	SPDIF1_SEL	Selects 1st SPDIF encoder input. • 2'b00: Ch1/2 • 2'b01: Ch3/4 • 2'b10: Ch5/6 • 2'b11: Ch7/8
[3:0]	RESERVED	NA

GPIO Registers

Register 53: GPIO1/2 CONFIG

Bits	[7:4]	[3:0]
Default	4'd0	4'd0

Bits	Mnemonic	Description
[7:4]	GPIO2_CFG	Configures GPIO2 • 4'd0: output 0 - output • 4'd1: output 0 - output • 4'd2: output 1 - output • 4'd3: CLK_DATA - output • 4'd4: interrupt - output • 4'd5: mute all channel - input • 4'd6: system mode control - input • 4'd7: RESERVED • 4'd8: clk_avalid - output • 4'd9: output PWM1 - output • 4'd10: output PWM2 - output • 4'd11: output PWM3 - output • 4'd12: volume minimum - output • 4'd13: automute status - output • 4'd14: soft ramp done - output • 4'd15: SPDIF1/SPDIF2 stream - output
[3:0]	GPIO1_CFG	Configures GPIO1 • 4'd0: output 0 - output • 4'd1: output 0 - output • 4'd2: output 1 - output • 4'd3: CLK_DATA - output • 4'd4: interrupt - output • 4'd5: mute all channel - input • 4'd6: system mode control - input • 4'd7: RESERVED • 4'd8: clk_avalid - output • 4'd9: output PWM1 - output • 4'd10: output PWM2 - output • 4'd11: output PWM3 - output • 4'd12: volume minimum - output • 4'd13: automute status - output • 4'd14: soft ramp done - output • 4'd15: SPDIF1/SPDIF2 stream - output

Register 54: GPIO3/4 CONFIG

Bits	[7:4]	[3:0]
Default	4'd0	4'd0

Bits	Mnemonic	Description
[7:4]	GPIO4_CFG	Configures GPIO4 • 4'd0: output 0 - output • 4'd1: output 0 - output • 4'd2: output 1 - output • 4'd3: CLK_DATA - output • 4'd4: interrupt - output • 4'd5: mute all channel - input • 4'd6: system mode control - input • 4'd7: RESERVED • 4'd8: clk_avalid - output • 4'd9: output PWM1 - output • 4'd10: output PWM2 - output • 4'd11: output PWM3 - output • 4'd12: volume minimum - output • 4'd13: automute status - output • 4'd14: soft ramp done - output • 4'd15: SPDIF1/SPDIF2 stream - output
[3:0]	GPIO3_CFG	Configures GPIO3 • 4'd0: output 0 - output • 4'd1: output 0 - output • 4'd2: output 1 - output • 4'd3: CLK_DATA - output • 4'd4: interrupt - output • 4'd5: mute all channel - input • 4'd6: system mode control - input • 4'd7: RESERVED • 4'd8: clk_avalid - output • 4'd9: output PWM1 - output • 4'd10: output PWM2 - output • 4'd11: output PWM3 - output • 4'd12: volume minimum - output • 4'd13: automute status - output • 4'd14: soft ramp done - output • 4'd15: SPDIF1/SPDIF2 stream - output

Register 55: GPIO5/6 CONFIG

Bits	[7:4]	[3:0]
Default	4'd0	4'd0

Bits	Mnemonic	Description
[7:4]	GPIO6_CFG	Configures GPIO6 • 4'd0: output 0 - output • 4'd1: output 0 - output • 4'd2: output 1 - output • 4'd3: CLK_DATA - output • 4'd4: interrupt - output • 4'd5: mute all channel - input • 4'd6: system mode control - input • 4'd7: RESERVED • 4'd8: clk_avalid - output • 4'd9: output PWM1 - output • 4'd10: output PWM2 - output • 4'd11: output PWM3 - output • 4'd12: volume minimum - output • 4'd13: automute status - output • 4'd14: soft ramp done - output • 4'd15: SPDIF1/SPDIF2 stream - output
[3:0]	GPIO5_CFG	Configures GPIO5 • 4'd0: output 0 - output • 4'd1: output 0 - output • 4'd2: output 1 - output • 4'd3: CLK_DATA - output • 4'd4: interrupt - output • 4'd5: mute all channel - input • 4'd6: system mode control - input • 4'd7: RESERVED • 4'd8: clk_avalid - output • 4'd9: output PWM1 - output • 4'd10: output PWM2 - output • 4'd11: output PWM3 - output • 4'd12: volume minimum - output • 4'd13: automute status - output • 4'd14: soft ramp done - output • 4'd15: SPDIF1/SPDIF2 stream - output

Register 57-56: RESERVED

Register 59-58: GPIO INVERT AND OUTPUT LOGIC

Bits	[15]	[14]	[13]	[12]	[11]	[10]	[9:6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b1	1'b1	1'b1	1'b0	1'b0	1'b0	4'd0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[15]	GPIO_OR_SS_RAMP	When GPIOx_CFG=14 (output soft ramp done flag): • 1'b0: The soft ramp done flag is determined by GPIO_AND_SS_RAMP and GPIO_SEL • 1'b1: The soft ramp done flag is the "OR" of all 8ch soft ramp done flags (default)
[14]	GPIO_OR_VOL_MIN	When GPIOx_CFG=12 (output vol_min flag): • 1'b0: The vol_min flag is determined by GPIO_AND_VOL_MIN and GPIO_SEL • 1'b1: The vol_min flag is the "OR" of all 8ch vol_min flags (default)
[13]	GPIO_OR_AUTOMUTE	When GPIOx_CFG=13 (output automute status): • 1'b0: The automute status is determined by GPIO_AND_AUTOMUTE and GPIO_SEL • 1'b1: The automute status is the "OR" of all 8ch automute status (default)
[12]	GPIO_AND_SS_RAMP	When GPIOx_CFG=14 (output soft ramp done flag) and GPIO_OR_SS_RAMP is not set: • 1'b0: The soft ramp done flag is from a single channel selected by GPIO_SEL (default) • 1'b1: The soft ramp done flag is the "AND" of all 8ch soft ramp done flags
[11]	GPIO_AND_VOL_MIN	When GPIOx_CFG=12 (output vol_min flag) and GPIO_OR_VOL_MIN is not set: • 1'b0: The vol_min flag is from a single channel selected by GPIO_SEL (default) • 1'b1: The vol_min flag is the "AND" of all 8ch vol_min flags
[10]	GPIO_AND_AUTOMUTE	When GPIOx_CFG=13 (output automute status) and GPIO_OR_AUTOMUTE is not set: • 1'b0: The automute status is from a single channel selected by GPIO_SEL (default) • 1'b1: The automute status is the "AND" of all 8ch automute status
[9:6]	RESERVED	NA
[5]	INVERT_GPIO6	Inverts GPIO6 output. • 1'b0: not inverted • 1'b1: inverted
[4]	INVERT_GPIO5	Inverts GPIO5 output. • 1'b0: not inverted • 1'b1: inverted
[3]	INVERT_GPIO4	Inverts GPIO4 output. • 1'b0: not inverted • 1'b1: inverted

[2]	INVERT_GPIO3	Inverts GPIO3 output. • 1'b0: not inverted • 1'b1: inverted
[1]	INVERT_GPIO2	Inverts GPIO2 output. • 1'b0: not inverted • 1'b1: inverted
[0]	INVERT_GPIO1	Inverts GPIO1 output. • 1'b0: not inverted • 1'b1: inverted

Register 61-60: GPIO WEAK EN AND CH SEL

Bits	[15:13]	[12:10]	[9:6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	3'd0	3'b0	4'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[15:13]	RESERVED	NA
[12:10]	GPIO_SEL	When GPIOx_CFG is set to 12, 13 or 14, and the corresponding GPIO_AND and GPIO_OR are not set: • 3'd0: Outputs status/flag from ch1 • 3'd1: Outputs status/flag from ch2 • 3'd2: Outputs status/flag from ch3 • 3'd3: Outputs status/flag from ch4 • 3'd4: Outputs status/flag from ch5 • 3'd5: Outputs status/flag from ch6 • 3'd6: Outputs status/flag from ch7 • 3'd7: Outputs status/flag from ch8
[9:6]	RESERVED	NA
[5]	GPIO6_WK_EN	Weak keeper control for GPIO6. • 1'b0: GPIO6 weak keeper disabled (default) • 1'b1: GPIO6 weak keeper enabled Note: Weak keeper is a holder that can be optionally set, it maintains the previous state driver, with the GPIOx_WK_EN bit.
[4]	GPIO5_WK_EN	Weak keeper control for GPIO5. • 1'b0: GPIO5 weak keeper disabled (default) • 1'b1: GPIO5 weak keeper enabled
[3]	GPIO4_WK_EN	Weak keeper control for GPIO4. • 1'b0: GPIO4 weak keeper disabled (default) • 1'b1: GPIO4 weak keeper enabled
[2]	GPIO3_WK_EN	Weak keeper control for GPIO3. • 1'b0: GPIO3 weak keeper disabled (default) • 1'b1: GPIO3 weak keeper enabled
[1]	GPIO2_WK_EN	Weak keeper control for GPIO2. • 1'b0: GPIO2 weak keeper disabled (default) • 1'b1: GPIO2 weak keeper enabled
[0]	GPIO1_WK_EN	Weak keeper control for GPIO1. • 1'b0: GPIO1 weak keeper disabled (default) • 1'b1: GPIO1 weak keeper enabled

Register 62: GPIO INPUT ENABLE

Bits	[7:6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	2'd0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[5]	GPIO6_IE	GPIO6 input control. • 1'b0: Disables GPIO6 input (default) • 1'b1: Enables GPIO6 input
[4]	GPIO5_IE	GPIO5 input control. • 1'b0: Disables GPIO5 input (default) • 1'b1: Enables GPIO5 input
[3]	GPIO4_IE	GPIO4 input control. • 1'b0: Disables GPIO4 input (default) • 1'b1: Enables GPIO4 input
[2]	GPIO3_IE	GPIO3 input control. • 1'b0: Disables GPIO3 input (default) • 1'b1: Enables GPIO3 input
[1]	GPIO2_IE	GPIO2 input control. • 1'b0: Disables GPIO2 input (default) • 1'b1: Enables GPIO2 input
[0]	GPIO1_IE	GPIO1 input control. • 1'b0: Disables GPIO1 input (default) • 1'b1: Enables GPIO1 input

Register 63: RESERVED

Register 65-64: GPIO OUTPUT ENABLE

Bits	[15]	[14]	[13]	[12]	[11]	[10]	[9:6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	4'd0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[15]	SPDIF_SEL_GPIO6	When GPIO6_CFG=15 (output SPDIF stream): • 1'b0: Outputs SPDIF1 stream (default) • 1'b1: Outputs SPDIF2 stream
[14]	SPDIF_SEL_GPIO5	When GPIO5_CFG=15 (output SPDIF stream): • 1'b0: Outputs SPDIF1 stream (default) • 1'b1: Outputs SPDIF2 stream
[13]	SPDIF_SEL_GPIO4	When GPIO4_CFG=15 (output SPDIF stream): • 1'b0: Outputs SPDIF1 stream (default) • 1'b1: Outputs SPDIF2 stream
[12]	SPDIF_SEL_GPIO3	When GPIO3_CFG=15 (output SPDIF stream): • 1'b0: Outputs SPDIF1 stream (default) • 1'b1: Outputs SPDIF2 stream
[11]	SPDIF_SEL_GPIO2	When GPIO2_CFG=15 (output SPDIF stream): • 1'b0: Outputs SPDIF1 stream (default) • 1'b1: Outputs SPDIF2 stream
[10]	SPDIF_SEL_GPIO1	When GPIO1_CFG=15 (output SPDIF stream): • 1'b0: Outputs SPDIF1 stream (default) • 1'b1: Outputs SPDIF2 stream
[9:6]	RESERVED	NA
[5]	GPIO6_OE	GPIO6 output control. • 1'b0: Tristate GPIO6 (default) • 1'b1: GPIO6 Output Enable
[4]	GPIO5_OE	GPIO5 output control. • 1'b0: Tristate GPIO5 (default) • 1'b1: GPIO5 Output Enable
[3]	GPIO4_OE	GPIO4 output control. • 1'b0: Tristate GPIO4 (default) • 1'b1: GPIO4 Output Enable
[2]	GPIO3_OE	GPIO3 output control. • 1'b0: Tristate GPIO3 (default) • 1'b1: GPIO3 Output Enable
[1]	GPIO2_OE	GPIO2 output control. • 1'b0: Tristate GPIO2 (default) • 1'b1: GPIO2 Output Enable
[0]	GPIO1_OE	GPIO1 output control. • 1'b0: Tristate GPIO1 (default) • 1'b1: GPIO1 Output Enable

Register 67-66: GPIO READ ENABLE

Bits	[15:12]	[11]	[10]	[9:6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	4'b0000	1'b0	1'b0	4'd0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[15:12]	RESERVED	NA
[11]	GPIO_AMP_MODE	When any GPIO_CFG is set to 6 (input system mode control): • 1'b0: Power down when GPIO input is 1 • 1'b1: HIFI when GPIO input is 1 (when GPIO input is 0, system mode is determined by register AMP_MODE (register 0, bit[1]))
[10]	GPIO1_AS_DATA8	Controls DATA8 input source. • 1'b0: Gets DATA8 input from DATA8_I (default) • 1'b1: Gets DATA8 input from GPIO1_I instead of DATA8_I
[9:6]	RESERVED	NA
[5]	GPIO6_READ	GPIO6 readback control. • 1'b0: GPIO6 Readback disabled (default) • 1'b1: Allow readback of GPIO6_I
[4]	GPIO5_READ	GPIO5 readback control. • 1'b0: GPIO5 Readback disabled (default) • 1'b1: Allow readback of GPIO5_I
[3]	GPIO4_READ	GPIO4 readback control. • 1'b0: GPIO4 Readback disabled (default) • 1'b1: Allow readback of GPIO4_I
[2]	GPIO3_READ	GPIO3 readback control. • 1'b0: GPIO3 Readback disabled (default) • 1'b1: Allow readback of GPIO3_I
[1]	GPIO2_READ	GPIO2 readback control. • 1'b0: GPIO2 Readback disabled (default) • 1'b1: Allow readback of GPIO2_I
[0]	GPIO1_READ	GPIO1 readback control. • 1'b0: GPIO1 Readback disabled (default) • 1'b1: Allow readback of GPIO1_I

Register 68: PWM1 COUNT

Bits	[7:0]
Default	8'd0

Bits	Mnemonic	Description
[7:0]	PWM1_COUNT	8-bit value to set the number of SYS_CLK periods the PWM signal is high for. • 8'd1: Minimum • 8'd255: Maximum

Register 70-69: PWM1 FREQUENCY

Bits	[15:0]
Default	16'd0

Bits	Mnemonic	Description
[15:0]	PWM1_FREQ	16-bit value to set the frequency of the PWM signal in terms of SYS_CLK divisions. **Valid from 16'h0001 to 16'hFFFF** $$frequency\ (Hz) = \frac{SYS\_CLK}{PWM1\_FREQ + 1}$$ $$Duty\ Cycle\ (\%) = \left(1 - \frac{(PWM1\_FREQ + 1) - PWM1\_COUNT}{(PWM1\_FREQ + 1)}\right) \times 100$$

Register 71: PWM2 COUNT

Bits	[7:0]
Default	8'd0

Bits	Mnemonic	Description
[7:0]	PWM2_COUNT	8-bit value to set the number of SYS_CLK periods the PWM signal is high for. • 8'd1: Minimum • 8'd255: Maximum

Register 73-72: PWM2 FREQUENCY

Bits	[15:0]
Default	16'd0

Bits	Mnemonic	Description
[15:0]	PWM2_FREQ	16-bit value to set the frequency of the PWM signal in terms of SYS_CLK divisions. **Valid from 16'h0001 to 16'hFFFF** $$frequency\ (Hz) = \frac{SYS\_CLK}{PWM2\_FREQ + 1}$$ $$Duty\ Cycle\ (\%) = \left(1 - \frac{(PWM2\_FREQ + 1) - PWM2\_COUNT}{(PWM2\_FREQ + 1)}\right) \times 100$$

Register 74: PWM3 COUNT

Bits	[7:0]
Default	8'd0

Bits	Mnemonic	Description
[7:0]	PWM3_COUNT	8-bit value to set the number of SYS_CLK periods the PWM signal is high for. • 8'd1: Minimum • 8'd255: Maximum

Register 76-75: PWM3 FREQUENCY

Bits	[15:0]
Default	16'd0

Bits	Mnemonic	Description
[15:0]	PWM3_FREQ	16-bit value to set the frequency of the PWM signal in terms of SYS_CLK divisions. **Valid from 16'h0001 to 16'hFFFF** $$frequency\ (Hz) = \frac{SYS\_CLK}{PWM3\_FREQ + 1}$$ $$Duty\ Cycle\ (\%) = \left(1 - \frac{(PWM3\_FREQ + 1) - PWM3\_COUNT}{(PWM3\_FREQ + 1)}\right) \times 100$$

DAC Registers

Register 77: INPUT CONFIG

Bits	[7]	[6]	[5]	[4]	[3:2]	[1:0]
Default	1'b0	1'b0	1'b0	1'b0	2'd0	2'd0

Bits	Mnemonic	Description
[7:6]	RESERVED	NA
[5]	DSD_MASTER_MODE	DSD master mode config. • 1'b0: DSD slave mode (default) • 1'b1: DSD master mode. DSD_CLK outputs from DATA_CLK
[4]	ENABLE_MASTER_MODE	TDM master mode config. • 1'b0: TDM slave mode (default) • 1'b1: TDM master mode enabled. Master BCK and WS output from DATA_CLK and DATA1
[3:2]	INPUT_SEL	Selects input data when AUTO_INPUT_SELECT is set to 2'd0. • 2'd0: TDM (default) • 2'd1: DSD • 2'd2: DoP • 2'd3: Reserved
[1:0]	AUTO_INPUT_SELECT	Auto input data selection config. • 2'd0: Disables auto input select. Input data type is set by INPUT_SEL (default) • 2'd1: Auto select between DSD and TDM inputs. • 2'd2-2'd3: Reserved

Register 78: MASTER MODE CONFIG

Bits	[7]	[6]	[5]	[4:3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	2'd0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	RESERVED	NA
[6]	MASTER_BCK_DIV1	When enabled, master BCK is 128fs clock. Otherwise, BCK is less than or equal to 64fs. • 1'b0: BCK is not 128fs clock (default) • 1'b1: BCK is 128fs clock
[5]	MASTER_WS_IDLE	Sets the value of master WS when WS is idle. • 1'b0: WS is 0 when idle (default) • 1'b1: WS is 1 when idle
[4:3]	MASTER_FRAME_LENGTH	Selects the bit length in each TDM channel in master mode. • 2'd0: 32 bit (default) • 2'd2: 16 bit • others: Reserved
[2]	MASTER_WS_PULSE_MODE	When enabled, master WS is a pulse signal instead of a 50% duty cycle signal. The pulse width is 1 BCK cycle. • 1'b0: 50% duty cycle WS signal (default) • 1'b1: Pulse WS signal
[1]	MASTER_WS_INVERT	Inverts master WS. • 1'b0: Non-inverted (default) • 1'b1: Inverted
[0]	MASTER_BCK_INVERT	Inverts master BCK or DSD_CLK. • 1'b0: Non-inverted (default) • 1'b1: Inverted

Register 79: TDM CONFIG1

Bits	[7]	[6:4]	[3:0]
Default	1'b0	3'd0	4'd1

Bits	Mnemonic	Description
[7]	TDM_RESYNC	Force TDM decoder to resync. • 1'b0: Let decoder sync (default) • 1'b1: Force decoder not sync
[6:4]	MASTER_WS_SCALE	In TDM master mode, tunes master BCK/WS ratio by scaling master WS. It allows more TDM slots in a fixed frame. • 3'd0: No scale (default) • 3'd1: Scale down WS by 2 • 3'd2: Scale down WS by 4 • 3'd3: Scale down WS by 8 • 3'd4: Scale down WS by 16 • others: Reserved
[3:0]	TDM_CH_NUM	Total TDM slot number per frame = TDM_CH_NUM + 1.

Register 80: TDM CONFIG2

Bits	[7]	[6]	[5:0]
Default	1'b0	1'b0	6'd1

Bits	Mnemonic	Description
[7]	TDM_LJ_MODE	TDM LJ mode. • 1'b0: Standard I2S (default) • 1'b1: LJ mode
[6]	TDM_VALID_EDGE	TDM WS valid edge. • 1'b0: negative edge (default) • 1'b1: positive edge
[5:0]	TDM_VALID_PULSE_LEN	Data valid pulse length adjustment If using 8 or more TDM channels, Set to “8”, else default value

Register 81: TDM CONFIG3

Bits	[7:6]	[5]	[4:0]
Default	2'd0	1'b0	5'd0

Bits	Mnemonic	Description
[7:6]	TDM_BIT_WIDTH	Bit width of each TDM slot. • 2'b00: 32-bit (default) • 2'b01: 24-bit • 2'b10: 16-bit • 2'b11: Reserved
[5]	TDM_CHAIN_MODE	TDM daisy chain mode. • 1'b0: Disable (default) • 1'b1: Enable chain mode
[4:0]	TDM_DATA_LATCH_ADJ	Sets the position of the start bit within each TDM slot …Can be moved +ve or -ve relative to MSB

Register 82: BCK/WS MONITOR CONFIG

Bits	[7:6]	[5]	[4]	[3:0]
Default	2'd0	1'b0	1'b0	4'd0

Bits	Mnemonic	Description
[7:6]	RESERVED	NA
[5]	ENABLE_WS_MONITOR	Enable WS monitor. • 1'b0: Disable (default) • 1'b1: Enable Note: Should be set to 1'b0 when using DSD, if required then data is required to be on Channel 1
[4]	ENABLE_BCK_MONITOR	Enable BCK monitor. • 1'b0: Disable (default) • 1'b1: Enable
[3:0]	BCK_TIMER_DIV	BCK monitor counts 0 to (9'h1FF >> BCK_TIME_DIV) on MCLK. • 4'd0: Minimum (default) • 4'd15: Maximum

Register 83: TDM VALID PULSE CONFIG

Bits	[7:0]
Default	8'd0

Bits	Mnemonic	Description
[7:0]	TDM_VALID_PULSE_POS	The position of TDM valid pulse compared to WS valid edge. • 8'd0: Minimum • 8'd255: Maximum

Register 84: TDM CH1 CONFIG

Bits	[7]	[6]	[5:4]	[3:0]
Default	1'b0	1'b0	2'd0	4'd0

Bits	Mnemonic	Description
[7]	TDM_VALID_PULSE_POS_MSB	The position of TDM valid pulse compared to WS valid edge. MSB bit from TDM_VALID_PULSE_POS • 1'b0: Minimum (default) • 1'b1: Maximum
[6]	RESERVED	NA
[5:4]	TDM_CH1_LINE_SEL	CH1 data line selection. CH1 receives data from Nth line. N = TDM_CH1_LINE_SEL + 1. • 2'b00: Minimum (line1) • 2'b11: Maximum (line4)
[3:0]	TDM_CH1_SLOT_SEL	CH1 data slot selection. CH1 receives data from Mth slot. M = TDM_CH1_SLOT_SEL + 1. • 4'd0: Minimum (slot 1) • 4'd15: Maximum (slot 16)

Register 85: TDM CH2 CONFIG

Bits	[7:6]	[5:4]	[3:0]
Default	2'd0	2'd0	4'd1

Bits	Mnemonic	Description
[7:6]	RESERVED	NA
[5:4]	TDM_CH2_LINE_SEL	CH2 data line selection. CH2 receives data from Nth line. N = TDM_CH2_LINE_SEL + 1. 2'b00: Minimum (line1) 2'b11: Maximum (line4)
[3:0]	TDM_CH2_SLOT_SEL	CH2 data slot selection. CH2 receives data from Mth slot. M = TDM_CH2_SLOT_SEL + 1. • 4'd0: Minimum (slot 1) • 4'd15: Maximum (slot 16)

Register 86: TDM CH3 CONFIG

Bits	[7:6]	[5:4]	[3:0]
Default	2'd0	2'd1	4'd0

Bits	Mnemonic	Description
[7:6]	RESERVED	NA
[5:4]	TDM_CH3_LINE_SEL	CH3 data line selection. CH3 receives data from Nth line. N = TDM_CH3_LINE_SEL + 1. • 2'b00: Minimum (line1) • 2'b11: Maximum (line4)
[3:0]	TDM_CH3_SLOT_SEL	CH3 data slot selection. CH3 receives data from Mth slot. M = TDM_CH3_SLOT_SEL + 1. • 4'd0: Minimum (slot 1) • 4'd15: Maximum (slot 16)

Register 87: TDM CH4 CONFIG

Bits	[7:6]	[5:4]	[3:0]
Default	2'd0	2'd1	4'd1

Bits	Mnemonic	Description
[7:6]	RESERVED	NA
[5:4]	TDM_CH4_LINE_SEL	CH4 data line selection. CH4 receives data from Nth line. N = TDM_CH4_LINE_SEL + 1. • 2'b00: Minimum (line1) • 2'b11: Maximum (line4)
[3:0]	TDM_CH4_SLOT_SEL	CH4 data slot selection. CH4 receives data from Mth slot. M = TDM_CH4_SLOT_SEL + 1. • 4'd0: Minimum (slot 1) • 4'd15: Maximum (slot 16)

Register 88: TDM CH5 CONFIG

Bits	[7:6]	[5:4]	[3:0]
Default	2'd0	2'd2	4'd0

Bits	Mnemonic	Description
[7:6]	RESERVED	NA
[5:4]	TDM_CH5_LINE_SEL	CH5 data line selection. CH5 receives data from Nth line. N = TDM_CH5_LINE_SEL + 1. • 2'b00: Minimum (line1) • 2'b11: Maximum (line4)
[3:0]	TDM_CH5_SLOT_SEL	CH5 data slot selection. CH5 receives data from Mth slot. M = TDM_CH5_SLOT_SEL + 1. • 4'd0: Minimum (slot 1) • 4'd15: Maximum (slot 16)

Register 89: TDM CH6 CONFIG

Bits	[7:6]	[5:4]	[3:0]
Default	2'd0	2'd2	4'd1

Bits	Mnemonic	Description
[7:6]	RESERVED	NA
[5:4]	TDM_CH6_LINE_SEL	CH6 data line selection. CH6 receives data from Nth line. N = TDM_CH6_LINE_SEL + 1. • 2'b00: Minimum (line1) • 2'b11: Maximum (line4)
[3:0]	TDM_CH6_SLOT_SEL	CH6 data slot selection. CH6 receives data from Mth slot. M = TDM_CH6_SLOT_SEL + 1. • 4'd0: Minimum (slot 1) • 4'd15: Maximum (slot 16)

Register 90: TDM CH7 CONFIG

Bits	[7:6]	[5:4]	[3:0]
Default	2'd0	2'd3	4'd0

Bits	Mnemonic	Description
[7:6]	RESERVED	NA
[5:4]	TDM_CH7_LINE_SEL	CH7 data line selection. CH7 receives data from Nth line. N = TDM_CH7_LINE_SEL + 1. • 2'b00: Minimum (line1) • 2'b11: Maximum (line4)
[3:0]	TDM_CH7_SLOT_SEL	CH7 data slot selection. CH7 receives data from Mth slot. M = TDM_CH7_SLOT_SEL + 1. • 4'd0: Minimum (slot 1) • 4'd15: Maximum (slot 16)

Register 91: TDM CH8 CONFIG

Bits	[7:6]	[5:4]	[3:0]
Default	2'd0	2'd3	4'd1

Bits	Mnemonic	Description
[7:6]	RESERVED	NA
[5:4]	TDM_CH8_LINE_SEL	CH8 data line selection. CH8 receives data from Nth line. N = TDM_CH8_LINE_SEL + 1. • 2'b00: Minimum (line1) • 2'b11: Maximum (line4)
[3:0]	TDM_CH8_SLOT_SEL	CH8 data slot selection. CH8 receives data from Mth slot. M = TDM_CH8_SLOT_SEL + 1. • 4'd0: Minimum (slot 1) • 4'd15: Maximum (slot 16)

Register 92: RESYNC CONFIG

Bits	[7:5]	[4]	[3]	[2]	[1]	[0]
Default	3'd0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7:5]	RESERVED	NA
[4]	SYNC_DAC_CLK_DIV	Controls clock divider reset on negative edge of WS. • 1'b1: Clock divider will be reset at every negative edge of WS • 1'b0: Disable the FIR_RESYNC reset Note: If reset the SYNC_DAC_CLK_DIV (ie 1'b1), toggle this bit before setting any other RESYNC bits [3:0]
[3]	DOP_CLK_RESYNC	Controls Dop clock divider reset on negative edge of WS. • 1'b1: Clock divider will be reset at every negative edge of WS • 1'b0: Disable the FIR_RESYNC reset
[2]	VOL_THD_RESYNC	Controls Volume-THD block reset on negative edge of WS. • 1'b1: DoP clock generator will be reset at every negative edge of WS • 1'b0: Disable the DOP_CLK_RESYNC reset
[1]	FIR_RESYNC	Controls FIR filters reset on negative edge of WS. • 1'b1: FIR filters will be reset at every negative edge of WS • 1'b0: Disable the FIR_RESYNC reset
[0]	FS_RESYNC	Controls FS clock generator reset on negative edge of WS. • 1'b1: FS clock generator will be reset at every negative edge of WS • 1'b0: Disable the FS_RESYNC reset

Register 93: RESERVED

Register 94: VOLUME1

Bits	[7:0]
Default	8'd0

Bits	Mnemonic	Description
[7:0]	VOLUME1	DAC ch1 volume. -0dB to -127.5dB 0.5dB steps. • 8'd0: 0dB • 8'd255: -127.5 dB

Register 95: VOLUME2

Bits	[7:0]
Default	8'd0

Bits	Mnemonic	Description
[7:0]	VOLUME2	DAC ch2 volume. -0dB to -127.5dB 0.5dB steps. • 8'd0: 0dB • 8'd255: -127.5 dB

Register 96: VOLUME3

Bits	[7:0]
Default	8'd0

Bits	Mnemonic	Description
[7:0]	VOLUME3	DAC ch3 volume. -0dB to -127.5dB 0.5dB steps. • 8'd0: 0dB • 8'd255: -127.5 dB

Register 97: VOLUME4

Bits	[7:0]
Default	8'd0

Bits	Mnemonic	Description
[7:0]	VOLUME4	DAC ch4 volume. -0dB to -127.5dB 0.5dB steps. • 8'd0: 0dB • 8'd255: -127.5 dB

Register 98: VOLUME5

Bits	[7:0]
Default	8'd0

Bits	Mnemonic	Description
[7:0]	VOLUME5	DAC ch5 volume. -0dB to -127.5dB 0.5dB steps. • 8'd0: 0dB • 8'd255: -127.5 dB

Register 99: VOLUME6

Bits	[7:0]
Default	8'd0

Bits	Mnemonic	Description
[7:0]	VOLUME6	DAC ch6 volume. -0dB to -127.5dB 0.5dB steps. • 8'd0: 0dB • 8'd255: -127.5 dB

Register 100: VOLUME7

Bits	[7:0]
Default	8'd0

Bits	Mnemonic	Description
[7:0]	VOLUME7	DAC ch7 volume. -0dB to -127.5dB 0.5dB steps. • 8'd0: 0dB • 8'd255: -127.5 dB

Register 101: VOLUME8

Bits	[7:0]
Default	8'd0

Bits	Mnemonic	Description
[7:0]	VOLUME8	DAC ch8 volume. -0dB to -127.5dB 0.5dB steps. • 8'd0: 0dB • 8'd255: -127.5 dB

Register 102: DAC VOL UP RATE

Bits	[7:0]
Default	8'd150

Bits	Mnemonic	Description
[7:0]	DAC_VOL_RATE_UP	Value by which the old VOLUME value is incremented to reach the new VOLUME value. Valid from 8'd1 (slowest) to 8'd255 (fastest), where 8'd0 instantly changes the VOLUME value. Calculation of time ramp rate (in seconds): 2^14/(DAC_VOL_RATE_UP*FS) • 8'd0 : Instant change • 8'd150: Default • 8'd255: Fastest change

Register 103: DAC VOL DOWN RATE

Bits	[7:0]
Default	8'd150

Bits	Mnemonic	Description
[7:0]	DAC_VOL_RATE_DOWN	Value by which the old VOLUME value is incremented to reach the new VOLUME value. Valid from 8'd1 (slowest) to 8'd255 (fastest), where 8'd0 instantly changes the VOLUME value. Calculation of time ramp rate (in seconds): 2^14/(DAC_VOL_RATE_UP*FS) • 8'd0 : Instant change • 8'd150: Default • 8'd255: Fastest change

Register 104: DAC VOL DOWN RATE FAST

Bits	[7:0]
Default	8'd0

Bits	Mnemonic	Description
[7:0]	DAC_VOL_RATE_FAST	Value by which the old VOLUME value is decremented to reach the new VOLUME value. Valid from 8'd1 (slowest) to 8'd255 (fastest), where 8'd0 instantly changes the VOLUME value. Only used during abnormal mute (PLL unlock or BCK_WS ratio have failed) Calculation of time ramp rate (in seconds): 2^14/(DAC_VOL_RATE_UP*FS) • 8'd0: Instant change (default) • 8'd255: Fastest change

Register 105: VOLUME AND MONO CTRL

Bits	[7]	[6]	[5]	[4]	[3:0]
Default	1'b0	1'b0	1'b0	1'b0	4'b0000

Bits	Mnemonic	Description
[7]	RESERVED	NA
[6]	FORCE_VOLUME	Volume update control. • 1'b0: Updates volume when toggling RUN_VOLUME (default) • 1'b1: Updates volume immediately after changing any of VOLUME1-VOLUME8
[5]	DAC_USE_MONO_VOLUME	Defines how volume is controlled between channels. • 1'b0: Separated volume control (default) • 1'b1: Ch2/4/6/8 volumes are set by Ch1/3/5/7 volumes, respectively
[4]	RUN_VOLUME	Toggle RUN_VOLUME to update volumes set by VOLUME1-VOLUME8 • 1'b0: Separate volume control for each channel • 1'b1: Update all volumes at the same time
[3:0]	RESERVED	NA

Register 106: MUTE CTRL

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	DAC_MUTE_CH8	Channel 8 DAC mute control. • 1'b0: Normal operation (default) • 1'b1: Mute ch8
[6]	DAC_MUTE_CH7	Channel 7 DAC mute control. • 1'b0: Normal operation (default) • 1'b1: Mute ch7
[5]	DAC_MUTE_CH6	Channel 6 DAC mute control. • 1'b0: Normal operation (default) • 1'b1: Mute ch6
[4]	DAC_MUTE_CH5	Channel 5 DAC mute control. • 1'b0: Normal operation (default) • 1'b1: Mute ch5
[3]	DAC_MUTE_CH4	Channel 4 DAC mute control. • 1'b0: Normal operation (default) • 1'b1: Mute ch4
[2]	DAC_MUTE_CH3	Channel 3 DAC mute control. • 1'b0: Normal operation (default) • 1'b1: Mute ch3
[1]	DAC_MUTE_CH2	Channel 2 DAC mute control. • 1'b0: Normal operation (default) • 1'b1: Mute ch2
[0]	DAC_MUTE_CH1	Channel 1 DAC mute control. • 1'b0: Normal operation (default) • 1'b1: Mute ch1

Register 107: DATA INVERT CTRL

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	DAC_INVERT_CH8	Invert the output on Ch8 at the input to the NSMOD • 1'b0: Disable • 1'b1: Enable
[6]	DAC_INVERT_CH7	Invert the output on Ch7 at the input to the NSMOD • 1'b0: Disable • 1'b1: Enable
[5]	DAC_INVERT_CH6	Invert the output on Ch6 at the input to the NSMOD • 1'b0: Disable • 1'b1: Enable
[4]	DAC_INVERT_CH5	Invert the output on Ch5 at the input to the NSMOD • 1'b0: Disable • 1'b1: Enable
[3]	DAC_INVERT_CH4	Invert the output on Ch4 at the input to the NSMOD • 1'b0: Disable • 1'b1: Enable
[2]	DAC_INVERT_CH3	Invert the output on Ch3 at the input to the NSMOD • 1'b0: Disable • 1'b1: Enable
[1]	DAC_INVERT_CH2	Invert the output on Ch2 at the input to the NSMOD • 1'b0: Disable • 1'b1: Enable
[0]	DAC_INVERT_CH1	Invert the output on Ch1 at the input to the NSMOD • 1'b0: Disable • 1'b1: Enable

Register 108: FILTER CONFIG

Bits	[7]	[6]	[5]	[4:3]	[2:0]
Default	1'b0	1'b1	1'b0	2'b10	3'd0

Bits	Mnemonic	Description
[7]	RESERVED	NA
[6]	BYPASS_DEEMPH	De-emphasis filter control for channels 1/2. • 1'b0: Enables de-emphasis filters, for ch1/2 only • 1'b1: Disables de-emphasis filters (default)
[5]	PEAK_FILTER	DRE peak filter control. • 1'b0: Disables DRE peak filter (default) • 1'b1: Enables DRE peak filter
[4:3]	SEL_DEEMPH	Configures the de-emphasis filters for various sample rate. • 2'b00: FS=32kHz • 2'b01: FS=44.1kHz • 2'b10: FS=48kHz (default) • 2'b11: Reserved
[2:0]	FILTER_SHAPE	Selects the 8x interpolation FIR filter shape. • 3'd0: Minimum phase (default) • 3'd1: Linear phase apodizing • 3'd2: Reserved • 3'd3: Linear phase fast roll-off low ripple • 3'd4: Reserved • 3'd5: Reserved • 3'd6: Minimum phase slow roll-off • 3'd7: Minimum phase slow roll-off low dispersion Note: Chosen filter shape is the same for all channels

Register 109: IIR CONFIG

Bits	[7:6]	[5:3]	[2:0]
Default	2'd1	3'd4	3'd4

Bits	Mnemonic	Description
[7:6]	IIR_DITHER_SCALE	IIR dither scaling. IIR dither amount is IIR1_BW+IIR_DITHER_SCALE+2 bits. • 2'b01: Default • 2'b11: For Best low level linearity use this setting
[5:3]	RESERVED	NA
[2:0]	IIR1_BW	IIR1 bandwidth control. • 3'b011: Bandwidth *2 • 3'b100: Normal conditions (default) • 3'b101: Bandwidth/2 All other values are reserved

Register 110: RESERVED

Register 112-111: THD COMP C2 CH1/3/5/7

Bits	[15:0]
Default	16'd0

Bits	Mnemonic	Description
[15:0]	THD_C2_CH1357	A 16-bit signed coefficient for correcting for the CH1/3/5/7 second harmonic distortion. $$output = x + c2 * x^2 + c3 * x^3$$

Register 114-113: THD COMP C3 CH1/3/5/7

Bits	[15:0]
Default	16'd0

Bits	Mnemonic	Description
[15:0]	THD_C3_CH1357	A 16-bit signed coefficient for correcting for the CH1/3/5/7 third harmonic distortion. $$output = x + c2 * x^2 + c3 * x^3$$

Register 116-115: THD COMP C2 CH2/4/6/8

Bits	[15:0]
Default	16'd0

Bits	Mnemonic	Description
[15:0]	THD_C2_CH2468	A 16-bit signed coefficient for correcting for the CH2/4/6/8 second harmonic distortion. $$output = x + c2 * x^2 + c3 * x^3$$

Register 118-117: THD COMP C3 CH2/4/6/8

Bits	[15:0]
Default	16'd0

Bits	Mnemonic	Description
[15:0]	THD_C3_CH2468	A 16-bit signed coefficient for correcting for the CH2/4/6/8 third harmonic distortion. $$output = x + c2 * x^2 + c3 * x^3$$

Register 119: AUTOMUTE ENABLE

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	AUTOMUTE_EN_CH8	Channel 8 automute. • 1'b0: Disables ch8 automute (default) • 1'b1: Enables ch8 automute Note: Automute is available for PCM only
[6]	AUTOMUTE_EN_CH7	Channel 7 automute. • 1'b0: Disables ch7 automute (default) • 1'b1: Enables ch7 automute Note: Automute is available for PCM only
[5]	AUTOMUTE_EN_CH6	Channel 6 automute. • 1'b0: Disables ch6 automute (default) • 1'b1: Enables ch6 automute Note: Automute is available for PCM only
[4]	AUTOMUTE_EN_CH5	Channel 5 automute. • 1'b0: Disables ch5 automute (default) • 1'b1: Enables ch5 automute Note: Automute is available for PCM only
[3]	AUTOMUTE_EN_CH4	Channel 4 automute. • 1'b0: Disables ch4 automute (default) • 1'b1: Enables ch4 automute Note: Automute is available for PCM only
[2]	AUTOMUTE_EN_CH3	Channel 3 automute. • 1'b0: Disables ch3 automute (default) • 1'b1: Enables ch3 automute Note: Automute is available for PCM only
[1]	AUTOMUTE_EN_CH2	Channel 2 automute. • 1'b0: Disables ch2 automute (default) • 1'b1: Enables ch2 automute Note: Automute is available for PCM only
[0]	AUTOMUTE_EN_CH1	Channel 1 automute • 1'b0: Disables ch1 automute (default) • 1'b1: Enables ch1 automute Note: Automute is available for PCM only

Register 121-120: AUTOMUTE TIME

Bits	[15]	[14]	[13:11]	[10:0]
Default	1'b1	1'b0	3'd0	11'd0

Bits	Mnemonic	Description
[15]	AUTOMUTE_RAMP_TO_GROUND	When ramped to minimum volume during normal mute, allow soft ramp to ground for power saving. • 1'b0: Disabled • 1'b1: Enabled (default) normal mute includes: automute, mute by register, mute by GPIO
[14]	AUTOMUTE_WAIT_ON_DRE	Automute flag control. • 1'b0: Automute is flagged when automute condition is met (default) • 1'b1: Automute is flagged when automute condition is met and DRE is engaged
[13:11]	RESERVED	NA
[10:0]	AUTOMUTE_TIME	Configures the amount of time in seconds the audio must remain below AUTOMUTE_LEVEL before an automute condition is flagged. Valid from 0 (disabled) to 11'h7FF (fastest), where 11'h001 is the slowest $$Time(s) = \frac{2^{18}}{(AUTOMUTE\_TIME * FS)}$$ Where FS (s) = 1/fs (in kHz), for example if fs = 44.1kHz, FS(s) = 1/44.1e-3

Register 123-122: AUTOMUTE LEVEL

Bits	[15:0]
Default	16'd0

Bits	Mnemonic	Description
[15:0]	AUTOMUTE_LEVEL	Configures the threshold which the audio must be below before an automute condition is flagged. Valid from: 16'hFFFF (-42dB) to 16'h0001 (-132dB). Shift right 1 bit corresponds to -6dB. • 16'h0001: -132dB • 16'h0003: -126dB • 16'h3FFF: -54dB • 16'h7FFF: -48dB • 16'hFFFF: -42dB $$20 * log\left(\frac{AUTOMUTE\_LEVEL}{2^{16}}\right) - 42\ dB$$ *Note: this register works in tandem with AUTOMUTE_TIME to create the automute condition*

Register 125-124: AUTOMUTE OFF LEVEL

Bits	[15:0]
Default	16'd0

Bits	Mnemonic	Description
[15:0]	AUTOMUTE_OFF_LEVEL	Configures the threshold which the audio must be above before the automute condition is cleared (cleared immediately). Valid from: 16'hFFFF (-42dB) to 16'h0001 (-132dB). Shift right 1 bit corresponds to -6dB. • 16'h0001: -132dB • 16'h0003: -126dB • 16'h3FFF: -54dB • 16'h7FFF: -48dB • 16'hFFFF: -42dB $20 * log\left(\frac{AUTOMUTE\_OFF\_LEVEL}{2^{16}}\right) - 42\ dB$

Register 126: SOFT RAMP CONFIG

Bits	[7:6]	[5]	[4:0]
Default	2'd0	1'b0	5'd2

Bits	Mnemonic	Description
[7:6]	RESERVED	NA
[5]	SOFT_RAMP_TYPE	Sets whether the soft start ramp is linear or quadratic • 1'b0: Uses a quadratic function for the soft start ramp (default) • 1'b1: Uses the standard soft start ramp
[4:0]	SOFT_RAMP_TIME	Sets the amount of time that it takes to perform a soft start ramp. This time affects both ramp to ground and ramp to AVCC/2. Valid from 0 to 20 (inclusive). $Time[s] = \frac{4096 * 2^{(SOFT\_RAMP\_TIME+1)}}{MCLK[Hz]}$

Register 127: NSMOD DITHER SELECT

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	NSMOD_DITHER_SEL_CH8	Selects dither into ch8 NSMOD • 1'b0: out_ns_1 (default) • 1'b1: out_notch
[6]	NSMOD_DITHER_SEL_CH7	Selects dither into ch7 NSMOD • 1'b0: out_ns_1 (default) • 1'b1: out_notch
[5]	NSMOD_DITHER_SEL_CH6	Selects dither into ch6 NSMOD • 1'b0: out_ns_1 (default) • 1'b1: out_notch
[4]	NSMOD_DITHER_SEL_CH5	Selects dither into ch5 NSMOD • 1'b0: out_ns_1 (default) • 1'b1: out_notch
[3]	NSMOD_DITHER_SEL_CH4	Selects dither into ch4 NSMOD • 1'b0: out_ns_1 (default) • 1'b1: out_notch
[2]	NSMOD_DITHER_SEL_CH3	Selects dither into ch3 NSMOD • 1'b0: out_ns_1 (default) • 1'b1: out_notch
[1]	NSMOD_DITHER_SEL_CH2	Selects dither into ch2 NSMOD • 1'b0: out_ns_1 (default) • 1'b1: out_notch
[0]	NSMOD_DITHER_SEL_CH1	Selects dither into ch1 NSMOD • 1'b0: out_ns_1 (default) • 1'b1: out_notch

Register 128: NSMOD DITHER INVERT

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b1	1'b0	1'b1	1'b0	1'b1	1'b0	1'b1	1'b0

Bits	Mnemonic	Description
[7]	NSMOD_DITHER_INVERT_CH8	Invert dither into Channel 8 NSMOD. • 1'b0: Non-invert • 1'b1: Inverts dither into ch8 NSMOD (default)
[6]	NSMOD_DITHER_INVERT_CH7	Invert dither into Channel 7 NSMOD. • 1'b0: Non-invert (default) • 1'b1: Inverts dither into ch7 NSMOD
[5]	NSMOD_DITHER_INVERT_CH6	Invert dither into Channel 6 NSMOD. • 1'b0: Non-invert • 1'b1: Inverts dither into ch6 NSMOD (default)
[4]	NSMOD_DITHER_INVERT_CH5	Invert dither into Channel 5 NSMOD. • 1'b0: Non-invert (default) • 1'b1: Inverts dither into ch5 NSMOD
[3]	NSMOD_DITHER_INVERT_CH4	Invert dither into Channel 4 NSMOD. • 1'b0: Non-invert • 1'b1: Inverts dither into ch4 NSMOD (default)
[2]	NSMOD_DITHER_INVERT_CH3	Invert dither into Channel 3 NSMOD. • 1'b0: Non-invert (default) • 1'b1: Inverts dither into ch3 NSMOD
[1]	NSMOD_DITHER_INVERT_CH2	Invert dither into Channel 2 NSMOD. • 1'b0: Non-invert • 1'b1: Inverts dither into ch2 NSMOD (default)
[0]	NSMOD_DITHER_INVERT_CH1	Invert dither into Channel 1 NSMOD. • 1'b0: Non-invert (default) • 1'b1: Inverts dither into ch1 NSMOD

Register 129: NSMOD AND DITHER CONFIG

Bits	[7]	[6:4]	[3]	[2]	[1:0]
Default	1'b0	3'd0	1'b0	1'b0	2'b00

Bits	Mnemonic	Description
[7]	RESERVED	NA
[6:4]	IIR_DITHER_SEL	Selects different types of dither • 3'd0: mode_1 (default), if SELECT_IDAC_NUM = 0 • 3'd1: mode_2, if SELECT_IDAC_NUM = 1 • 3'd2: mode_3, if SELECT_IDAC_NUM = 2 • 3'd3: mode_4, if SELECT_IDAC_NUM = 3 • 3'd4: mode_6, if SELECT_IDAC_NUM = 5 • 3'd5-7: mode_8, if SELECT_IDAC_NUM>=7 **Note: Change to 3'd5 (mode_8) which is best for all sample rates**
[3]	RESERVED	NA
[2]	ENABLE_1_8TH_GAIN_MODE	Enables 1/8 gain mode in the NSMOD. • 1'b0: Disables 1/8 gain mode (default) • 1'b1: Enables 1/8 gain mode
[1:0]	RESERVED	NA

Register 130: RESERVED

Register 131: NSMOD DITHER CH12

Bits	[7:4]	[3:0]
Default	4'd0	4'd0

Bits	Mnemonic	Description
[7:4]	DITHER_SCALE_CH2	Alters the amount of dither to inject into the ch2 NS quantizer • 4'd0: Minimum (default) • 4'd15: Maximum
[3:0]	DITHER_SCALE_CH1	Alters the amount of dither to inject into the ch1 NS quantizer • 4'd0: Minimum (default) • 4'd15: Maximum

Register 132: NSMOD DITHER CH34

Bits	[7:4]	[3:0]
Default	4'd0	4'd0

Bits	Mnemonic	Description
[7:4]	DITHER_SCALE_CH4	Alters the amount of dither to inject into the ch4 NS quantizer • 4'd0: Minimum (default) • 4'd15: Maximum
[3:0]	DITHER_SCALE_CH3	Alters the amount of dither to inject into the ch3 NS quantizer • 4'd0: Minimum (default) • 4'd15: Maximum

Register 133: NSMOD DITHER CH56

Bits	[7:4]	[3:0]
Default	4'd0	4'd0

Bits	Mnemonic	Description
[7:4]	DITHER_SCALE_CH6	Alters the amount of dither to inject into the ch6 NS quantizer • 4'd0: Minimum (default) • 4'd15: Maximum
[3:0]	DITHER_SCALE_CH5	Alters the amount of dither to inject into the ch5 NS quantizer • 4'd0: Minimum (default) • 4'd15: Maximum

Register 134: NSMOD DITHER CH78

Bits	[7:4]	[3:0]
Default	4'd0	4'd0

Bits	Mnemonic	Description
[7:4]	DITHER_SCALE_CH8	Alters the amount of dither to inject into the ch8 NS quantizer • 4'd0: Minimum (default) • 4'd15: Maximum
[3:0]	DITHER_SCALE_CH7	Alters the amount of dither to inject into the ch7 NS quantizer • 4'd0: Minimum (default) • 4'd15: Maximum

Register 135: MIN PEAK

Bits	[7:1]	[0]
Default	7'd0	1'b1

Bits	Mnemonic	Description
[7:1]	RESERVED	NA
[0]	MIN_PEAK	DRE peak detector start point control. • 1'b0: DRE peak detector starts from max • 1'b1: DRE peak detector starts from min (default)

Register 136: DRE ATT EN AND THDR CTRL

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	DRE_THDR_CTRL_CH78	Allows DRE to control the THDR when ch7/8 DRE is engaged. • 1'b0: DRE does not control THDR(default) • 1'b1: DRE controls THDR
[6]	DRE_THDR_CTRL_CH56	Allows DRE to control the THDR when ch5/6 DRE is engaged. • 1'b0: DRE does not control THDR(default) • 1'b1: DRE controls THDR
[5]	DRE_THDR_CTRL_CH34	Allows DRE to control the THDR when ch3/4 DRE is engaged. • 1'b0: DRE does not control THDR(default) • 1'b1: DRE controls THDR
[4]	DRE_THDR_CTRL_CH12	Allows DRE to control the THDR when ch1/2 DRE is engaged. • 1'b0: DRE does not control THDR(default) • 1'b1: DRE controls THDR
[3]	DRE_ATT_ENABLE_CH78	Performs digital/analog gain swap when ch7/8 DRE is engaged. • 1'b0: DRE controls does not control analog attenuation (default) • 1'b1: DRE controls analog attenuation
[2]	DRE_ATT_ENABLE_CH56	Performs digital/analog gain swap when ch5/6 DRE is engaged. • 1'b0: DRE controls does not control analog attenuation (default) • 1'b1: DRE controls analog attenuation
[1]	DRE_ATT_ENABLE_CH34	Performs digital/analog gain swap when ch3/4 DRE is engaged. • 1'b0: DRE controls does not control analog attenuation (default) • 1'b1: DRE controls analog attenuation
[0]	DRE_ATT_ENABLE_CH12	Performs digital/analog gain swap when ch1/2 DRE is engaged. • 1'b0: DRE controls does not control analog attenuation (default) • 1'b1: DRE controls analog attenuation

Register 138-137: RESERVED

Register 139: DRE FORCE

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	DRE_FORCE_CH8	Force ch8 into DRE mode even if zero cross has not occurred. • 1'b0: DRE engages when signal is below DRE threshold and a signal zero cross is detected (default) • 1'b1: DRE engages when the signal is below DRE threshold, signal zero cross is ignored
[6]	DRE_FORCE_CH6	Force ch6 into DRE mode even if zero cross has not occurred. • 1'b0: DRE engages when signal is below DRE threshold and a signal zero cross is detected (default) • 1'b1: DRE engages when the signal is below DRE threshold, signal zero cross is ignored
[5]	DRE_FORCE_CH4	Force ch4 into DRE mode even if zero cross has not occurred. • 1'b0: DRE engages when signal is below DRE threshold and a signal zero cross is detected (default) • 1'b1: DRE engages when the signal is below DRE threshold, signal zero cross is ignored
[4]	DRE_FORCE_CH2	Force ch2 into DRE mode even if zero cross has not occurred. • 1'b0: DRE engages when signal is below DRE threshold and a signal zero cross is detected (default) • 1'b1: DRE engages when the signal is below DRE threshold, signal zero cross is ignored
[3]	DRE_FORCE_CH7	Force ch7 into DRE mode even if zero cross has not occurred. • 1'b0: DRE engages when signal is below DRE threshold and a signal zero cross is detected (default) • 1'b1: DRE engages when the signal is below DRE threshold, signal zero cross is ignored
[2]	DRE_FORCE_CH5	Force ch5 into DRE mode even if zero cross has not occurred. • 1'b0: DRE engages when signal is below DRE threshold and a signal zero cross is detected (default) • 1'b1: DRE engages when the signal is below DRE threshold, signal zero cross is ignored
[1]	DRE_FORCE_CH3	Force ch3 into DRE mode even if zero cross has not occurred. • 1'b0: DRE engages when signal is below DRE threshold and a signal zero cross is detected (default) • 1'b1: DRE engages when the signal is below DRE threshold, signal zero cross is ignored

[0]	DRE_FORCE_CH1	Force ch1 into DRE mode even if zero cross has not occurred. • 1'b0: DRE engages when signal is below DRE threshold and a signal zero cross is detected (default) • 1'b1: DRE engages when the signal is below DRE threshold, signal zero cross is ignored

Register 141-140: DRE GAIN CH1/3/5/7

Bits	[15:0]
Default	16'd0

Bits	Mnemonic	Description
[15:0]	DRE_GAIN1357	Sets the DRE gain for ch1/3/5/7. Shift right 1 bit corresponds to 6dB. Valid from 16'h7FFF (30dB) to 16'h03FF (0dB) • 16'h03FF: 0dB • 16'h07FF: 6dB • 16'h0FFF: 12dB • 16'h1FFF: 18dB • 16'h3FFF: 24dB • 16'h7FFF: 30dB

Register 143-142: DRE GAIN CH2/4/6/8

Bits	[15:0]
Default	16'd0

Bits	Mnemonic	Description
[15:0]	DRE_GAIN2468	Sets the DRE gain for ch2/4/6/8. Shift right 1 bit corresponds to 6dB. Valid from 16'h7FFF (30dB) to 16'h03FF (0dB) • 16'h03FF: 0dB • 16'h07FF: 6dB • 16'h0FFF: 12dB • 16'h1FFF: 18dB • 16'h3FFF: 24dB • 16'h7FFF: 30dB

Register 145-144: DRE ON THRESHOLD

Bits	[15:0]
Default	16'd0

Bits	Mnemonic	Description
[15:0]	DRE_ON_THRESH	DRE on threshold. Shift right 1 bit corresponds to -6dB. • 16'h0000: (default, invalid value for DRE) • 16'h0001: -114dB • … • 16'h0FFF: -48dB • 16'h1FFF: -42dB • 16'h3FFF: -36dB • 16'h7FFF: -30dB • 16'hFFFF: -24dB

Register 147-146: DRE OFF THRESHOLD

Bits	[15:0]
Default	16'd0

Bits	Mnemonic	Description
[15:0]	DRE_OFF_THRESH	DRE off threshold. Shift right 1 bit corresponds to -6dB. • 16'h0000: (default, invalid value for DRE) • 16'h0001: -114dB • … • 16'h0FFF: -48dB • 16'h1FFF: -42dB • 16'h3FFF: -36dB • 16'h7FFF: -30dB • 16'hFFFF: -24dB

Register 148: DRE DECAY RATE

Bits	[7]	[6:5]	[4:0]
Default	1'b0	2'd0	5'd0

Bits	Mnemonic	Description
[7]	DRE_FORCE_LEVEL	Force ch1-8 into DRE mode even if zero cross has not occurred.
[6:5]	RESERVED	NA
[4:0]	DRE_DECAY_RATE	Sets the speed at which the stored value of the DRE peak detector will decay when the input signal is below the stored value. • 5'd31 = slowest decay • 5'd0 = instant decay

Register 150-149: DC OFFSET CH1/3/5/7

Bits	[15:0]
Default	16'd0

Bits	Mnemonic	Description
[15:0]	DC_OFFSET1357	DC offset for ch1/3/5/7 $V_{OFFSET} = \frac{DC\_OFFSET_{2468}}{2^{24}-1} * V$

Register 152-151: DC OFFSET CH2/4/6/8

Bits	[15:0]
Default	16'd0

Bits	Mnemonic	Description
[15:0]	DC_OFFSET2468	DC offset for ch2/4/6/8 $V_{OFFSET} = \frac{DC\_OFFSET_{2468}}{2^{24}-1} * V$

Register 153: DC RAMP RATE

Bits	[7:0]
Default	8'd0

Bits	Mnemonic	Description
[7:0]	DC_RAMP_RATE	Value by which the old DC value is incremented/decremented per sample to reach the new dc value. Valid from 8'd0 (instant) to 8'd255 (fastest), where 8'd1 is the slowest ramp rate. • 8'd0: Instant (default) • 8'd1: Slowest • 8'd255: Fastest

Register 154: GAIN 18dB

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	GAIN_18DB_CH8	Digital +18dB gain control on channel 8. • 1'b0: No gain • 1'b1: Applies +18dB gain on ch8
[6]	GAIN_18DB_CH6	Digital +18dB gain control on channel 6. • 1'b0: No gain • 1'b1: Applies +18dB gain on ch6
[5]	GAIN_18DB_CH4	Digital +18dB gain control on channel 4. • 1'b0: No gain • 1'b1: Applies +18dB gain on ch4
[4]	GAIN_18DB_CH2	Digital +18dB gain control on channel 2. • 1'b0: No gain • 1'b1: Applies +18dB gain on ch2
[3]	GAIN_18DB_CH7	Digital +18dB gain control on channel 7. • 1'b0: No gain • 1'b1: Applies +18dB gain on ch7
[2]	GAIN_18DB_CH5	Digital +18dB gain control on channel 5. • 1'b0: No gain • 1'b1: Applies +18dB gain on ch5
[1]	GAIN_18DB_CH3	Digital +18dB gain control on channel 3. • 1'b0: No gain • 1'b1: Applies +18dB gain on ch3
[0]	GAIN_18DB_CH1	Digital +18dB gain control on channel 1. • 1'b0: No gain • 1'b1: Applies +18dB gain on ch1

Register 159-155: SPDIF1 CS

Bits	[39:0]
Default	40'd0

Bits	Mnemonic	Description
[39:0]	SPDIF1_CS	Configures SPDIF1 sub-code bits. 32 bits for S/PDIF specification channel information.

Register 164-160: SPDIF2 CS

Bits	[39:0]
Default	40'd0

Bits	Mnemonic	Description
[39:0]	SPDIF2_CS	Configures SPDIF2 sub-code bits. 32 bits for S/PDIF specification channel information.

Synchronous Slave Interface (no clock required)

Register 192: RESET & PLL REGISTER1

Bits	[7]	[6]	[5:3]	[2]	[1]	[0]
Default	1'b0	1'b0	3'd0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	AO_SOFT_RESET	Performs soft reset to clocked registers. • 1'b0: Disabled (default) • 1'b1: Enabled
[6]	PLL_SOFT_RESET	Performs soft reset to clock not required registers. • 1'b0: Disabled (default) • 1'b1: Enabled
[5:3]	RESERVED	NA
[2]	I2C_ADDR	This bit configures the I2C device address for 1 of 2 devices • 1'b0: I2C device address 0x90/0x98 (default) • 1'b1: I2C device address 0x92/0x9A See Register Overview for more information
[1]	GPIO1_SDB_AO	Configures GPIO1 SDB (Shutdown_b) When SYS_CLK is provided through GPIO1, set this bit to '1' to allow SYS_CLK input. • 1'b0: Disabled (default) • 1'b1: Enabled
[0]	PLL_CLKHV_PHASE_INV	Inverts SYS_CLK. • 1'b0: Disabled (default) • 1'b1: Enabled

Register 193: PLL REGISTER2

Bits	[7]	[6]	[5]	[4:3]	[2:1]	[0]
Default	1'b0	1'b0	1'b0	2'd0	2'd0	1'b0

Bits	Mnemonic	Description
[7]	PLL_BYP	PLL bypass mode. • 1'b0: Disabled (default) • 1'b1: Enabled
[6]	DVDD_SHUNTB	Enables digital regulator output shunt to ground (10k). Active low. • 1'b0: Enabled (default) • 1'b1: Disabled
[5]	SEL_1V_DREG	Sets digital regulator output voltage to 1V • 1'b0: Disabled (default) • 1'b1: Enabled
[4:3]	PLL_HVREG_VREF_SEL	PLL HVREG reference voltage selection • **2'b11: 1.7 V (Optimum setting, normal operation)** • Others: reserved
[2:1]	SEL_PLL_IN	Selects PLL input clock sources. • 2'd0: XTAL (default) • 2'd1: MCLK • 2'd2: XIN • 2'd3: BCK
[0]	EN_PLL_CLKIN	PLL input clocks control. • 1'b0: Disables PLL input clocks (default) • 1'b1: Enables PLL input clocks

Register 194: PLL REGISTER3

Bits	[7:3]	[2]	[1]	[0]
Default	5'd0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7:3]	RESERVED	NA
[2]	AUTO_LOCK_EN	Allows PLL to relock when PLL lock is lost and there are 256 valid PLL input clock cycles. • 1'b0: Disabled (default) • 1'b1: Enabled
[1:0]	RESERVED	NA

Register 195: PLL REGISTER4

Bits	[7:5]	[4:3]	[2]	[1]	[0]
Default	3'd0	2'd0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7:5]	PLL_CP_BIAS_SEL	Sets the Charge Pump Bias current value: • **3b'011:4u (optimum setting, for normal operation)**
[4:3]	PLL_ID_SEL	Sets the PLL Internal Delay: • **2b'11:1.5nS (optimum setting, for normal operation)** **Note: Fixed to 1.5nS, no other possible cases**
[2]	PLL_VCO_FMAX	Disables the PLL VCO's FMAX-limiting • 1'b0: Limit is set (default) • **1'b1: No limit (for normal operation)**
[1]	PLL_VCO_PDB	Enables/disables the PLL voltage-controlled oscillator (VCO). • 1'b0: Disabled (default) • 1'b1: Enabled
[0]	PLL_CP_PDB	Enables/disables the PLL charge pump. • 1'b0: Disabled (default) • 1'b1: Enabled

Register 196: PLL REGISTER5

Bits	[7:5]	[4:2]	[1:0]
Default	3'd0	3'd0	2'd0

Bits	Mnemonic	Description
[7:5]	PLL_VCO_BAND_CTRL	Selects the frequency band of the VCO. • 3'd0: Minimum (default) • 3'd10: **Optimum analog performance** • 3'd7: Maximum
[4:2]	RESERVED	NA
[1:0]	PLL_VCO_BIAS	Selects the bias current of the VCO. • 2'b00: Minimum (default) • 2'b11: **Maximum, Optimum analog performance**

Register 199-197: PLL REGISTER6

Bits	[23:0]
Default	24'd0

Bits	Mnemonic	Description
[23:0]	PLL_CLK_FB_DIV	Sets the PLL clock feedback divider. • 20'd0: Reserved • 20'dn: Divide by (2^25)/n

Register 202-200: PLL REGISTER7

Bits	[23]	[22]	[21]	[20]	[19]	[18:10]	[9:1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	9'd0	9'd0	1'b0

Bits	Mnemonic	Description
[23]	PLL_REG_PDB_HV	Power Down the HV regulator. • 1'd0: Disable the PLL HV-regulator • 1'd1: Enable the PLL HV-regulator
[22]	PLL_REG_PDB_1V2	Power Down the 1V2 regulator. • 1'd0: Disable the PLL 1V2-regulator • 1'd1: Enable the PLL 1V2-regulator
[21:20]	RESERVED	NA
[19]	PLL_LOW_BW	Adjust the PLL Bandwidth • 1'b0: Default • 1'b1: **Normal operation, optimum setting**
[18:10]	PLL_CLK_OUT_DIV	Sets the Output Division (No) of the PLL. • 9'd0: Reserved • 9'd1: Divide by 1 **(Normal Starting value)** • 9'd2: Divide by 2 • 9'dn: Divide by n
[9:1]	PLL_CLK_IN_DIV	Sets the PLL clock input divider. • 9'd0: Reserved • 9'd1: Divide by 1 **(Normal Starting value)** • 9'd2: Divide by 2 • 9'dn: Divide by n
[0]	PLL_FB_DIV_LOAD	Load PLL_CLK_FB_DIV Write 1 then write 0 to load CLK_FB_DIV.

Register 203: PLL REGISTER8

Bits	[7:6]	[5]	[4]	[3:1]	[0]
Default	2'd0	1'b0	1'b0	3'b000	1'b0

Bits	Mnemonic	Description
[7:6]	RESERVED	NA
[5]	PLL_DIG_RSTB	Resets the Digital core of the PLL. • 1'b0: PLL digital is off (default) • 1'b1: PLL digital is on
[4]	PLL_VCO_D_EN	**PLL requirement for normal operation** • 1'b0: PLL not used (default) • 1'b1: For normal PLL operation
[3:1]	RESERVED	NA
[0]	PLL_RCOSC_EN	Enables RC oscillator. • 1'b0: Disabled (default) • 1'b1: Enabled

Read Only Registers

Register 224: SYS READ

Bits	[7:2]	[1]	[0]
Default	-	-	-

Bits	Mnemonic	Description
[7:2]	RESERVED	NA
[1]	ADDR	I2C address select bit. • 1'b0 Address 0x90/0x98 • 1'b1 Address 0x92/0x9A
[0]	RESERVED	NA

Register 225: CHIP ID READ

Bits	[7:0]
Default	8'h67

Bits	Mnemonic	Description
[7:0]	CHIP_ID	CHIP ID Readback.

Register 228-227: RESERVED

Register 234-229: INTERRUPT STATE

Bits	[47:0]
Default	-

Bits	Mnemonic	Description
[47:0]	INTERRUPT_STATE	Interrupt state flags.

Register 240-235: INTERRUPT SOURCE

Bits	[47:0]
Default	-

Bits	Mnemonic	Description
[47:0]	INTERRUPT_SOURCES	Interrupt sources.

Register 244-241: RWS REF CNT STATUS

Bits	[31:27]	[26:0]
Default	-	-

Bits	Mnemonic	Description
[31:27]	RESERVED	NA
[26:0]	RWS_REF_CNT	Receiver WS Reference counter readback. • 27h'0000000: Minimum • 27h'7FFFFFF: Maximum

Register 246-245: RESERVED

Register 248-247: GPIO READ

Bits	[15:6]	[5:0]
Default	-	-

Bits	Mnemonic	Description
[15:6]	RESERVED	NA
[5:0]	GPIO_I_READ	GPIO inputs readback.

Register 249: AUTOMUTE READ

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	-	-	-	-	-	-	-	-

Bits	Mnemonic	Description
[7]	AUTOMUTE_CH8	Automute status ch8 • 1'b0: Automute not detected on channel 8 • 1'b1: Automute detected on channel 8
[6]	AUTOMUTE_CH7	Automute status ch7 • 1'b0: Automute not detected on channel 7 • 1'b1: Automute detected on channel 7
[5]	AUTOMUTE_CH6	Automute status ch6 • 1'b0: Automute not detected on channel 6 • 1'b1: Automute detected on channel 6
[4]	AUTOMUTE_CH5	Automute status ch5 • 1'b0: Automute not detected on channel 5 • 1'b1: Automute detected on channel 5
[3]	AUTOMUTE_CH4	Automute status ch4 • 1'b0: Automute not detected on channel 4 • 1'b1: Automute detected on channel 4
[2]	AUTOMUTE_CH3	Automute status ch3 • 1'b0: Automute not detected on channel 3 • 1'b1: Automute detected on channel 3
[1]	AUTOMUTE_CH2	Automute status ch2 • 1'b0: Automute not detected on channel 2 • 1'b1: Automute detected on channel 2
[0]	AUTOMUTE_CH1	Automute status ch1 • 1'b0: Automute not detected on channel 1 • 1'b1: Automute detected on channel 1

Register 250: VOL MIN READ

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	-	-	-	-	-	-	-	-

Bits	Mnemonic	Description
[7]	VOL_MIN_CH8	Volume min flag ch8 • 1'b0: Minimum volume not detected on channel 8 • 1'b1: Minimum volume detected on channel 8
[6]	VOL_MIN_CH7	Volume min flag ch7 • 1'b0: Minimum volume not detected on channel 7 • 1'b1: Minimum volume detected on channel 7
[5]	VOL_MIN_CH6	Volume min flag ch6 • 1'b0: Minimum volume not detected on channel 6 • 1'b1: Minimum volume detected on channel 6
[4]	VOL_MIN_CH5	Volume min flag ch5 • 1'b0: Minimum volume not detected on channel 5 • 1'b1: Minimum volume detected on channel 5
[3]	VOL_MIN_CH4	Volume min flag ch4 • 1'b0: Minimum volume not detected on channel 4 • 1'b1: Minimum volume detected on channel 4
[2]	VOL_MIN_CH3	Volume min flag ch3 • 1'b0: Minimum volume not detected on channel 3 • 1'b1: Minimum volume detected on channel 3
[1]	VOL_MIN_CH2	Volume min flag ch2 • 1'b0: Minimum volume not detected on channel 2 • 1'b1: Minimum volume detected on channel 2
[0]	VOL_MIN_CH1	Volume min flag ch1 • 1'b0: Minimum volume not detected on channel 1 • 1'b1: Minimum volume detected on channel 1

Register 251: SOFT RAMP UP READ

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	-	-	-	-	-	-	-	-

Bits	Mnemonic	Description
[7]	SS_RAMP_UP_CH8	Soft ramped up flag ch8 • 1'b0: Soft ramp up not detected on channel 8 • 1'b1: Soft ramp up detected on channel 8
[6]	SS_RAMP_UP_CH7	Soft ramped up flag ch7 • 1'b0: Soft ramp up not detected on channel 7 • 1'b1: Soft ramp up detected on channel 7
[5]	SS_RAMP_UP_CH6	Soft ramped up flag ch6 • 1'b0: Soft ramp up not detected on channel 6 • 1'b1: Soft ramp up detected on channel 6
[4]	SS_RAMP_UP_CH5	Soft ramped up flag ch5 • 1'b0: Soft ramp up not detected on channel 5 • 1'b1: Soft ramp up detected on channel 5
[3]	SS_RAMP_UP_CH4	Soft ramped up flag ch4 • 1'b0: Soft ramp up not detected on channel 4 • 1'b1: Soft ramp up detected on channel 4
[2]	SS_RAMP_UP_CH3	Soft ramped up flag ch3 • 1'b0: Soft ramp up not detected on channel 3 • 1'b1: Soft ramp up detected on channel 3
[1]	SS_RAMP_UP_CH2	Soft ramped up flag ch2 • 1'b0: Soft ramp up not detected on channel 2 • 1'b1: Soft ramp up detected on channel 2
[0]	SS_RAMP_UP_CH1	Soft ramped up flag ch1 • 1'b0: Soft ramp up not detected on channel 1 • 1'b1: Soft ramp up detected on channel 1

Register 252: SOFT RAMP DOWN READ

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	-	-	-	-	-	-	-	-

Bits	Mnemonic	Description
[7]	SS_RAMP_DOWN_CH8	Soft ramped down flag ch8 • 1'b0: Soft ramp down not detected on channel 8 • 1'b1: Soft ramp down detected on channel 8
[6]	SS_RAMP_DOWN_CH7	Soft ramped down flag ch7 • 1'b0: Soft ramp down not detected on channel 7 • 1'b1: Soft ramp down detected on channel 7
[5]	SS_RAMP_DOWN_CH6	Soft ramped down flag ch6 • 1'b0: Soft ramp down not detected on channel 6 • 1'b1: Soft ramp down detected on channel 6
[4]	SS_RAMP_DOWN_CH5	Soft ramped down flag ch5 • 1'b0: Soft ramp down not detected on channel 5 • 1'b1: Soft ramp down detected on channel 5
[3]	SS_RAMP_DOWN_CH4	Soft ramped down flag ch4 • 1'b0: Soft ramp down not detected on channel 4 • 1'b1: Soft ramp down detected on channel 4
[2]	SS_RAMP_DOWN_CH3	Soft ramped down flag ch3 • 1'b0: Soft ramp down not detected on channel 3 • 1'b1: Soft ramp down detected on channel 3
[1]	SS_RAMP_DOWN_CH2	Soft ramped down flag ch2 • 1'b0: Soft ramp down not detected on channel 2 • 1'b1: Soft ramp down detected on channel 2
[0]	SS_RAMP_DOWN_CH1	Soft ramped down flag ch1 • 1'b0: Soft ramp down not detected on channel 1 • 1'b1: Soft ramp down detected on channel 1

Register 253: DRE STATUS READ

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	-	-	-	-	-	-	-	-

Bits	Mnemonic	Description
[7]	DRE_SELECT_CH8	DRE is engaged ch8 • 1'b0: DRE not engaged on channel 8 1'b1: DRE engaged on channel 8
[6]	DRE_SELECT_CH6	DRE is engaged ch6 • 1'b0: DRE not engaged on channel 6 • 1'b1: DRE engaged on channel 6
[5]	DRE_SELECT_CH4	DRE is engaged ch4 • 1'b0: DRE not engaged on channel 4 • 1'b1: DRE engaged on channel 4
[4]	DRE_SELECT_CH2	DRE is engaged ch2 • 1'b0: DRE not engaged on channel 2 • 1'b1: DRE engaged on channel 2
[3]	DRE_SELECT_CH7	DRE is engaged ch7 • 1'b0: DRE not engaged on channel 7 • 1'b1: DRE engaged on channel 7
[2]	DRE_SELECT_CH5	DRE is engaged ch5 • 1'b0: DRE not engaged on channel 5 • 1'b1: DRE engaged on channel 5
[1]	DRE_SELECT_CH3	DRE is engaged ch3 • 1'b0: DRE not engaged on channel 3 • 1'b1: DRE engaged on channel 3
[0]	DRE_SELECT_CH1	DRE is engaged ch1 • 1'b0: DRE not engaged on channel 1 • 1'b1: DRE engaged on channel 1

Register 254: DRE DETECT READ

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	-	-	-	-	-	-	-	-

Bits	Mnemonic	Description
[7]	DRE_DETECT_CH8	DRE is detected ch8 • 1'b0: DRE not detected on channel 8 • 1'b1: DRE detected on channel 8
[6]	DRE_DETECT_CH6	DRE is detected ch6 • 1'b0: DRE not detected on channel 6 • 1'b1: DRE detected on channel 6
[5]	DRE_DETECT_CH4	DRE is detected ch4 • 1'b0: DRE not detected on channel 4 • 1'b1: DRE detected on channel 4
[4]	DRE_DETECT_CH2	DRE is detected ch2 • 1'b0: DRE not detected on channel 2 • 1'b1: DRE detected on channel 2
[3]	DRE_DETECT_CH7	DRE is detected ch7 • 1'b0: DRE not detected on channel 7 • 1'b1: DRE detected on channel 7
[2]	DRE_DETECT_CH5	DRE is detected ch5 • 1'b0: DRE not detected on channel 5 • 1'b1: DRE detected on channel 5
[1]	DRE_DETECT_CH3	DRE is detected ch3 • 1'b0: DRE not detected on channel 3 • 1'b1: DRE detected on channel 3
[0]	DRE_DETECT_CH1	DRE is detected ch1 • 1'b0: DRE not detected on channel 1 • 1'b1: DRE detected on channel 1

Register 255: DATA FLAG READ

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1:0]
Default	-	-	-	-	-	-	-

Bits	Mnemonic	Description
[7]	RESERVED	NA
[6]	TDM_DATA_VALID	TDM data is valid. • 1'b0: TDM data is invalid • 1'b1: TDM data is valid
[5]	DOP_VALID_CH78	Ch7/8 DoP valid flag • 1'b0: DoP is invalid on ch7/8 • 1'b1: DoP is valid on ch7/8
[4]	DOP_VALID_CH56	Ch5/6 DoP valid flag • 1'b0: DoP is invalid on ch5/6 • 1'b1: DoP is valid on ch5/6
[3]	DOP_VALID_CH34	Ch3/4 DoP valid flag • 1'b0: DoP is invalid on ch3/4 • 1'b1: DoP is valid on ch3/4
[2]	DOP_VALID_CH12	Ch1/2 DoP valid flag • 1'b0: DoP is invalid on ch1/2 • 1'b1: DoP is valid on ch1/2
[1:0]	RESERVED	NA

ES9080 Reference Schematic

Note: For some optional power savings, connect GPIO5 & GPIO6 together. This will give the option of turning off the charge pump with Automute set.

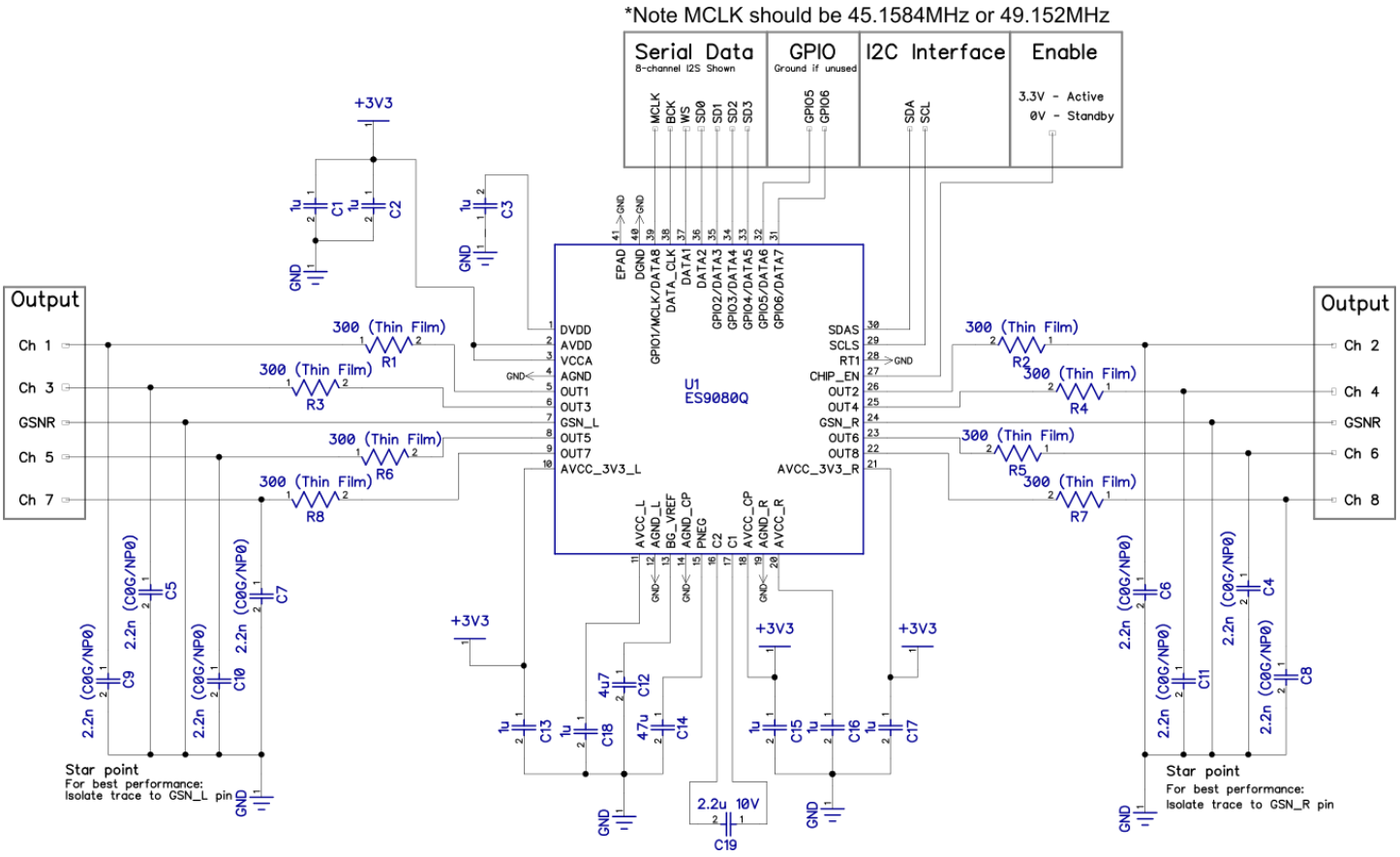
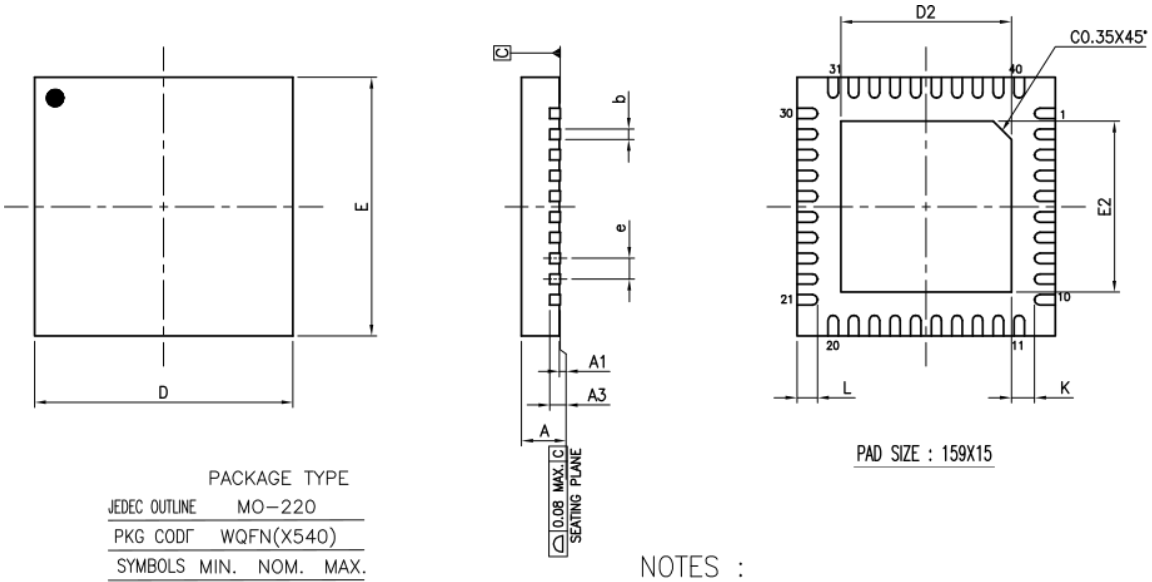


Figure 13 - Reference schematic

40 QFN Package Dimensions



PACKAGE TYPE			
JEDEC OUTLINE	MO-220		
PKG CODE	WQFN(X540)		
SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203 REF.	
b	0.15	0.20	0.25
D		5.00 BSC	
E		5.00 BSC	
e		0.40 BSC	
K	0.20	—	—

NOTES :

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

PAD SIZE	D2			E2			L		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
159X15* MIL	3.74	3.79	3.84	3.74	3.79	3.84	0.25	0.30	0.35

Figure 14 - Package dimensions

40 QFN Top View Marking

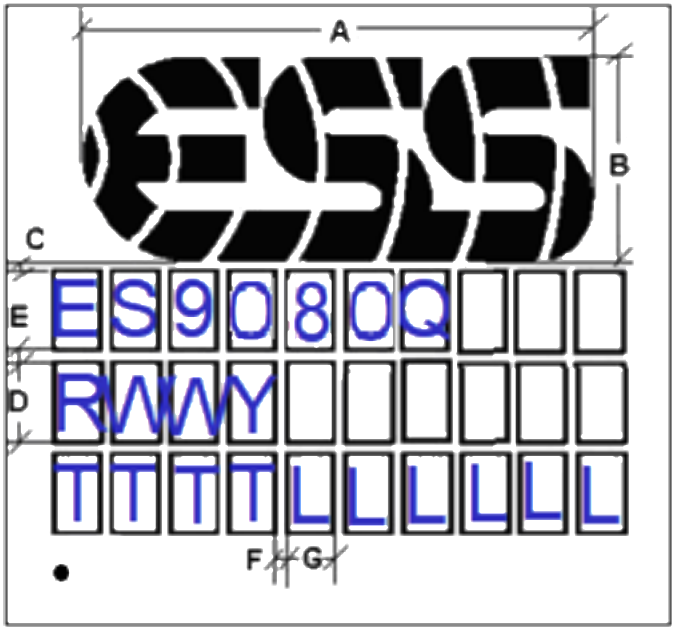


Figure 15 - Top view markings

	Dimension in mm						
Package Type	A	B	C	D	E	F	G
QFN 5mm x 5mm	4.0	1.6	0.2	0.4	0.2	0.1	0.3

T	*Tracking*
W	*Work week*
Y	*Last digit of year*
L	*Lot number*
R	*Silicon Revision*

Table 24 - Top view markings definitions

Marking is subject to change. This drawing is not to scale

Reflow Process Considerations

Temperature Controlled

For lead-free soldering, the characterization and optimization of the reflow process is the most important factor to consider.

The lead-free alloy solder has a melting point of 217°C. This alloy requires a minimum reflow temperature of 235°C to ensure good wetting. The maximum reflow temperature is in the 245°C to 260°C range, depending on the package size (RPC-2 Pb-Free Process – Classification Temperatures (Tc)). This narrows the process window for lead-free soldering to 10°C to 20°C.

The increase in peak reflow temperature in combination with the narrow process window makes the development of an optimal reflow profile a critical factor for ensuring a successful lead-free assembly process. The major factors contributing to the development of an optimal thermal profile are the size and weight of the assembly, the density of the components, the mix of large and small components, and the paste chemistry being used.

Reflow profiling needs to be performed by attaching calibrated thermocouples well adhered to the device as well as other critical locations on the board to ensure that all components are heated to temperatures above the minimum reflow temperatures and that smaller components do not exceed the maximum temperature limits (Table RPC-2).

To ensure that all packages can be successfully and reliably assembled, the reflow profiles studied and recommended by ESS are based on the JEDEC/IPC standard J-STD-020 revision D.1.

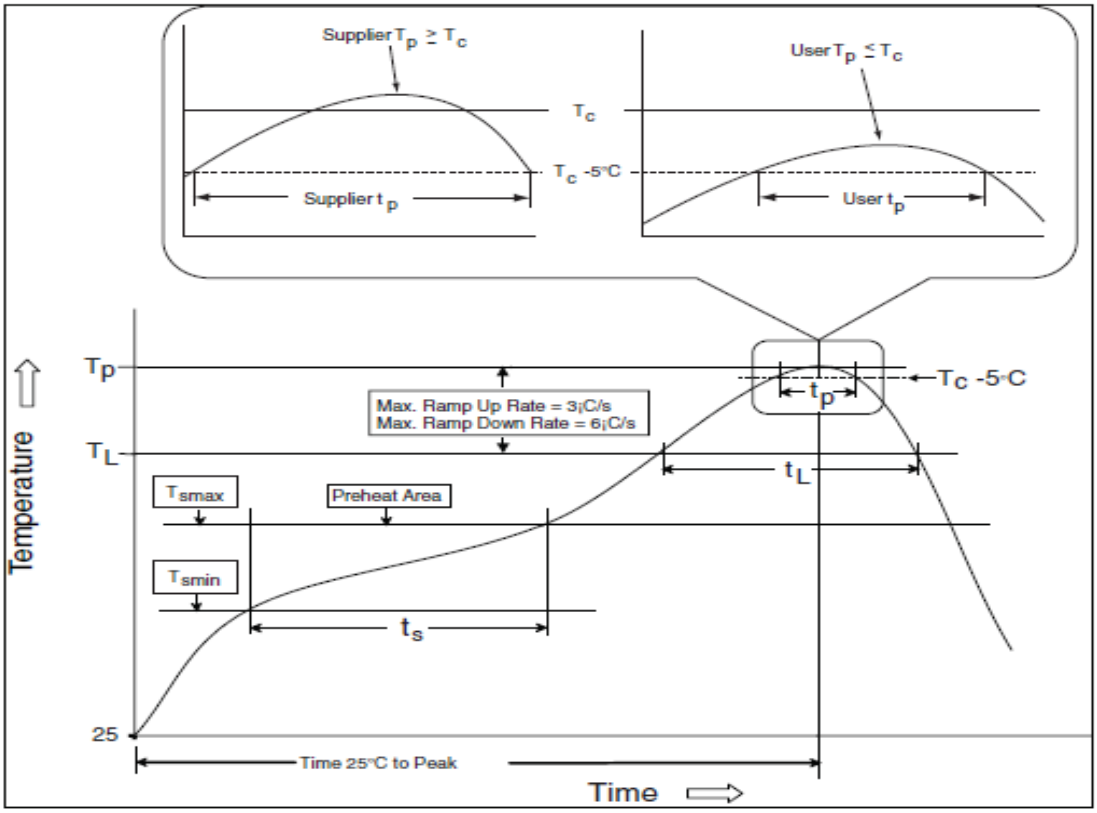


Figure 16 - IR/Convection Reflow Profile (IPC/JEDEC J-STD-020D.1)

Reflow is allowed 3 times. Caution must be taken to ensure time between re-flow runs does not exceed the allowed time by the moisture sensitivity label. If the time elapsed between the re-flows exceeds the moisture sensitivity time bake the board according to the moisture sensitivity label instructions.

Manual

Allowed up to 2 times with maximum temperature of 350°C no longer than 3 seconds.

RPC-1 Classification reflow profile

Profile Feature	Pb-Free Assembly
Preheat/Soak Temperature Min (Tsmin) Temperature Max (Tsmax) Time (ts) from (Tsmin to Tsmax)	 150°C 200°C 60-120 seconds
Ramp-up rate (TL to Tp)	3°C / second maximum
Liquidous temperature (TL) Time (tL) maintained above TL	217°C 60-150 seconds
Peak package body temperature (Tp)	For users Tp must not exceed the classification temp in Table RPC-2. For suppliers Tp must equal or exceed the Classification temp in Table RPC-2.
Time (tp)* within 5°C of the specified classification temperature (Tc), see Figure 16	30* seconds
Ramp-down rate (Tp to TL)	6°C / second maximum
Time 25°C to peak temperature	8 minutes maximum
* Tolerance for peak profile temperature (Tp) is defined as a supplier minimum and a user maximum.	

Table 25 - RPC-1 classification reflow profile data

All temperatures refer to the center of the package, measured on the package body surface that is facing up during assembly reflow (e.g., live-bug). If parts are reflowed in other than the normal live-bug assembly reflow orientation (i.e., dead-bug), Tp shall be within ±2°C of the live-bug Tp and still meet the Tc requirements, otherwise, the profile shall be adjusted to achieve the latter. To accurately measure actual peak package body temperatures, refer to JEP140 for recommended thermocouple use.

Reflow profiles in this document are for classification/preconditioning and are not meant to specify board assembly profiles. Actual board assembly profiles should be developed based on specific process needs and board designs and should not exceed the parameters in Table RPC-1.

For example, if Tc is 260°C and time tp is 30 seconds, this means the following for the supplier and the user.

For a supplier: The peak temperature must be at least 260°C. The time above 255°C must be at least 30 seconds.

For a user: The peak temperature must not exceed 260°C. The time above 255°C must not exceed 30 seconds.

All components in the test load shall meet the classification profile requirements.

RPC-2 Pb-Free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm3, <350	Volume mm3, 350 to 2000	Volume mm3, >2000
<1.6 mm	260°C	260°C	260°C
1.6 mm – 2.5 mm	260°C	250°C	245°C
>2.5 mm	250°C	245°C	245°C

Table 26 - RPC-2 Pb-free process classification temperatures

At the discretion of the device manufacturer, but not the board assembler/user, the maximum peak package body temperature (Tp) can exceed the values specified in Table RPC-2. The use of a higher Tp does not change the classification temperature (Tc).

Package volume excludes external terminals (e.g., balls, bumps, lands, leads) and/or nonintegral heat sinks.

The maximum component temperature reached during reflow depends on package thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD packages may still exist.

Ordering Information

Part Number	Description	Package
ES9080Q	SABRE 32-bit 8 Channel DAC with built in line driver & digital filters	5mm x 5mm 40 QFN
ES9080QT	SABRE 32-bit 8 Channel DAC with built in line driver & digital filters Extended temperature range -40 to 125deg Celsius	5mm x 5mm 40 QFN

Table 27 - Ordering information

Addendum

The following subsections outline the recommended configuration for common I2S and TDM modes in s2m format.

I2S Master

```
//Initialize into I2S with 4 data lines (8 channel), MCLK = 49.152MHz, fs = 48kHz, DRE
enabled, automute enabled

w 0x98 192 0x03; //Set GPIO1 (MCLK) pad to input mode, Invert CLKHV phase for better DNR

w 0x98 193 0xC3; //Set PLL Bypass, Remove 10k DVDD shunt to ground, set PLL input to MCLK,
enable the PLL clock inputs

w 0x98 202 0x40; //Set PLL Parameters


w 0x90 1 0xFF;        //Enable Interpolation and modulator clocks for all 8 channels

w 0x90 2 0x01;        //Enable the TDM decoder


//This sets the MCLK/FS rate

//w 0x90 3 0x00;         //128FS Eg, 49.152MHz/384kHz

//w 0x90 4 0x00;         //128FS Eg, 49.152MHz/384kHz

//w 0x90 3 0x01;         //256FS Eg, 49.152MHz/192kHz

//w 0x90 4 0x01;         //256FS Eg, 49.152MHz/192kHz

//w 0x90 3 0x03;         //512FS Eg, 49.152MHz/96kHz

//w 0x90 4 0x03;         //512FS Eg, 49.152MHz/96kHz

w 0x90 3 0x07;           //1024FS Eg, 49.152MHz/48kHz

w 0x90 4 0x07;           //1024FS Eg, 49.152MHz/48kHz


w 0x90 5 0xFF;   //Enable all 8 channels Analog section.

w 0x90 6 0x1F;   //Set the PNEG charge pump clock frequency to 705.6kHz or 768kHz
(depending on MCLK being 22.5792MHz or 24.576MHz)

w 0x90 7 0xBB;   //Setup automated delay sequence for analog section quietest pop

w 0x90 51 0x80;  //Force a PLL_LOCKL signal from analog since it it bypassed to prevent
muting the DAC automatically


//GPIO Registers

w 0x90 62 0x0E;  //Enable GPIO2/3/4 Inputs
```

```
//TDM/I2S Registers
w 0x90 77 0x10;  //Enable Master Mode
w 0x90 78 0x01;  //Invert Master mode BCK for I2S spec
w 0x90 79 0x01;  //Set 2 TDM slots per frame
w 0x90 80 0x01;  //Set to I2S format
w 0x90 84 0x00;  //TDM_CH1_LINE_SEL = 00 (DATA2), TDM_CH1_SLOT_SEL = 0
w 0x90 85 0x01;  //TDM_CH2_LINE_SEL = 00 (DATA2), TDM_CH2_SLOT_SEL = 1
w 0x90 86 0x10;  //TDM_CH3_LINE_SEL = 01 (DATA2), TDM_CH3_SLOT_SEL = 0
w 0x90 87 0x11;  //TDM_CH4_LINE_SEL = 01 (DATA2), TDM_CH4_SLOT_SEL = 1
w 0x90 88 0x20;  //TDM_CH5_LINE_SEL = 02 (DATA2), TDM_CH5_SLOT_SEL = 0
w 0x90 89 0x21;  //TDM_CH6_LINE_SEL = 02 (DATA2), TDM_CH6_SLOT_SEL = 1
w 0x90 90 0x30;  //TDM_CH7_LINE_SEL = 03 (DATA2), TDM_CH7_SLOT_SEL = 0
w 0x90 91 0x31;  //TDM_CH8_LINE_SEL = 03 (DATA2), TDM_CH8_SLOT_SEL = 1

w 0x90 109 0xE4; //Set Dither into the IIR filters for best low level linearity

//THD Compensation Registers
w 0x90 111 0x68; //THD C2 Coefficient for CH1/3/5/7
w 0x90 112 0x01; //THD C2 Coefficient for CH1/3/5/7
w 0x90 113 0x8D; //THD C3 Coefficient for CH1/3/5/7
w 0x90 115 0x68; //THD C2 Coefficient for CH2/4/6/8
w 0x90 116 0x01; //THD C2 Coefficient for CH2/4/6/8
w 0x90 117 0x8D; //THD C3 Coefficient for CH2/4/6/8

//Automute Registers
w 0x90 119 0xFF; //Enable Automute for 8 channels
w 0x90 120 0x0F; //Set Automute parameters
w 0x90 121 0xC0; //Set Automute parameters
w 0x90 122 0x08; //Set Automute Engage level to -120.4dB
w 0x90 124 0x0A; //Set Automute Disengage level to -118.4dB

//NSMOD Registers
```

```
w 0x90 128 0xCC; //Set the NSMOD dither phases for best performance if summing channels
together, (NOTE: not strictly needed for 8 channel mode)

w 0x90 129 0x54; //Set NSMOD dither type

w 0x90 131 0x44; //Set the Amount of dither into the NSMOD CH1/2 quantizer to best
linearity

w 0x90 132 0x44; //Set the Amount of dither into the NSMOD CH3/4 quantizer to best
linearity

w 0x90 133 0x44; //Set the Amount of dither into the NSMOD CH5/6 quantizer to best
linearity

w 0x90 134 0x44; //Set the Amount of dither into the NSMOD CH7/8 quantizer to best
linearity


//DRE Registers

w 0x90 136 0xFF; //Set the DRE to turn off the THDR at low volume for power saving, and to
swap analog and digital gain at low volume for best DNR

w 0x90 139 0xFF; //Allow DRE to still trigger if there is a small DC offset in the music.
(Some recordings have small DC offsets in them)

w 0x90 140 0x56; //Set DRE digital gain of CH1/3/5/7 to 16.37dB to match the Analog
attenuate amount when DRE turns on

w 0x90 141 0x1A; //Set DRE digital gain of CH1/3/5/7 to 16.37dB to match the Analog
attenuate amount when DRE turns on

w 0x90 142 0x56; //Set DRE digital gain of CH2/4/6/8 to 16.37dB to match the Analog
attenuate amount when DRE turns on

w 0x90 143 0x1A; //Set DRE digital gain of CH2/4/6/8 to 16.37dB to match the Analog
attenuate amount when DRE turns on

w 0x90 144 0xF1; //Set DRE ON theshold to -48dB

w 0x90 145 0x0C; //Set DRE ON theshold to -48dB

w 0x90 146 0x84; //Set DRE OFF theshold to -28dB

w 0x90 147 0x81; //Set DRE OFF theshold to -28dB

w 0x90 148 0x8F; //Set DRE decay rate (time it takes to automatically engage DRE if the
signal drops below the DRE ON threshold


//Enable Audio

w 0x90 92 0x10;  //Toggle DAC clock Resync to line up all the clocks in the DAC core for
best analog performance

w 0x90 92 0x0F;  //Toggle DAC clock Resync to line up all the clocks in the DAC core for
best analog performance
```

```
w 0x90 92 0x00;  //Toggle DAC clock Resync to line up all the clocks in the DAC core for best analog performance

w 0x90 0 0x02;   //Turn on the AMP  (This runs a state machine to gracefully turn on the DAC's)
```

I2S Slave

```
//Initialize into I2S with 4 data lines (8 channel), MCLK = 49.152MHz, fs = 48kHz, DRE
enabled, automute enabled

w 0x98 192 0x03; //Set GPIO1 (MCLK) pad to input mode, Invert CLKHV phase for better DNR

w 0x98 193 0xC3; //Set PLL Bypass, Remove 10k DVDD shunt to ground, set PLL input to MCLK,
enable the PLL clock inputs

w 0x98 202 0x40; //Set PLL Parameters


w 0x90 1 0xFF;        //Enable Interpolation and modulator clocks for all 8 channels

w 0x90 2 0x01;        //Enable the TDM decoder


//This sets the MCLK/FS rate

//w 0x90 3 0x00;         //128FS Eg, 49.152MHz/384kHz

//w 0x90 3 0x01;         //256FS Eg, 49.152MHz/192kHz

//w 0x90 3 0x03;         //512FS Eg, 49.152MHz/96kHz

w 0x90 3 0x07;           //1024FS Eg, 49.152MHz/48kHz


w 0x90 5 0xFF;   //Enable all 8 channels Analog section.

w 0x90 6 0x1F;   //Set the PNEG charge pump clock frequency to 705.6kHz or 768kHz
(depending on MCLK being 22.5792MHz or 24.576MHz)

w 0x90 7 0xBB;   //Setup automated delay sequence for analog section quietest pop

w 0x90 51 0x80;  //Force a PLL_LOCKL signal from analog since it it bypassed to prevent
muting the DAC automatically


//GPIO Registers

w 0x90 62 0x0E;  //Enable GPIO2/3/4 Inputs


//TDM/I2S Registers

w 0x90 77 0x00;  //Enable Slave Mode

w 0x90 79 0x01;  //Set 2 TDM slots per frame

w 0x90 80 0x01;  //Set to I2S format

w 0x90 84 0x00;  //TDM_CH1_LINE_SEL = 00 (DATA2), TDM_CH1_SLOT_SEL = 0

w 0x90 85 0x01;  //TDM_CH2_LINE_SEL = 00 (DATA2), TDM_CH2_SLOT_SEL = 1
```

```
w 0x90 86 0x10;  //TDM_CH3_LINE_SEL = 01 (DATA2), TDM_CH3_SLOT_SEL = 0

w 0x90 87 0x11;  //TDM_CH4_LINE_SEL = 01 (DATA2), TDM_CH4_SLOT_SEL = 1

w 0x90 88 0x20;  //TDM_CH5_LINE_SEL = 02 (DATA2), TDM_CH5_SLOT_SEL = 0

w 0x90 89 0x21;  //TDM_CH6_LINE_SEL = 02 (DATA2), TDM_CH6_SLOT_SEL = 1

w 0x90 90 0x30;  //TDM_CH7_LINE_SEL = 03 (DATA2), TDM_CH7_SLOT_SEL = 0

w 0x90 91 0x31;  //TDM_CH8_LINE_SEL = 03 (DATA2), TDM_CH8_SLOT_SEL = 1


w 0x90 109 0xE4; //Set Dither into the IIR filters for best low level linearity


//THD Compensation Registers

w 0x90 111 0x68; //THD C2 Coefficient for CH1/3/5/7

w 0x90 112 0x01; //THD C2 Coefficient for CH1/3/5/7

w 0x90 113 0x8D; //THD C3 Coefficient for CH1/3/5/7

w 0x90 115 0x68; //THD C2 Coefficient for CH2/4/6/8

w 0x90 116 0x01; //THD C2 Coefficient for CH2/4/6/8

w 0x90 117 0x8D; //THD C3 Coefficient for CH2/4/6/8


//Automute Registers

w 0x90 119 0xFF; //Enable Automute for 8 channels

w 0x90 120 0x0F; //Set Automute parameters

w 0x90 121 0xC0; //Set Automute parameters

w 0x90 122 0x08; //Set Automute Engage level to -120.4dB

w 0x90 124 0x0A; //Set Automute Disengage level to -118.4dB


//NSMOD Registers

w 0x90 128 0xCC; //Set the NSMOD dither phases for best performance if summing channels
together, (NOTE: not strictly needed for 8 channel mode)

w 0x90 129 0x54; //Set NSMOD dither type

w 0x90 131 0x44; //Set the Amount of dither into the NSMOD CH1/2 quantizer to best
linearity

w 0x90 132 0x44; //Set the Amount of dither into the NSMOD CH3/4 quantizer to best
linearity
```

```
w 0x90 133 0x44; //Set the Amount of dither into the NSMOD CH5/6 quantizer to best
linearity

w 0x90 134 0x44; //Set the Amount of dither into the NSMOD CH7/8 quantizer to best
linearity


//DRE Registers

w 0x90 136 0xFF; //Set the DRE to turn off the THDR at low volume for power saving, and to
swap analog and digital gain at low volume for best DNR

w 0x90 139 0xFF; //Allow DRE to still trigger is there is a small DC offset in the music.
(Some recordings have smal DC offsets in them)

w 0x90 140 0x56; //Set DRE digital gain of CH1/3/5/7 to 16.37dB to match the Analog
attenuate amount when DRE turns on

w 0x90 141 0x1A; //Set DRE digital gain of CH1/3/5/7 to 16.37dB to match the Analog
attenuate amount when DRE turns on

w 0x90 142 0x56; //Set DRE digital gain of CH2/4/6/8 to 16.37dB to match the Analog
attenuate amount when DRE turns on

w 0x90 143 0x1A; //Set DRE digital gain of CH2/4/6/8 to 16.37dB to match the Analog
attenuate amount when DRE turns on

w 0x90 144 0xF1; //Set DRE ON theshold to -48dB

w 0x90 145 0x0C; //Set DRE ON theshold to -48dB

w 0x90 146 0x84; //Set DRE OFF theshold to -28dB

w 0x90 147 0x81; //Set DRE OFF theshold to -28dB

w 0x90 148 0x8F; //Set DRE decay rate (time it takes to automatically engage DRE if the
signal drops below the DRE ON threshold


//Enable Audio

w 0x90 92 0x10;  //Toggle DAC clock Resync to line up all the clocks in the DAC core for
best analog performance

w 0x90 92 0x0F;  //Toggle DAC clock Resync to line up all the clocks in the DAC core for
best analog performance

w 0x90 92 0x00;  //Toggle DAC clock Resync to line up all the clocks in the DAC core for
best analog performance

w 0x90 0 0x02;   //Turn on the AMP  (This runs a state machine to gracefully turn on the
DAC's
```

TDM Master

```
//Initialize Master Mode TDM with 8 channels, MCLK = 49.152MHz, fs = 48kHz, DRE enabled, automute enabled
w 0x98 192 0x03; //Set GPIO1 (MCLK) pad to input mode, Invert CLKHV phase for better DNR
w 0x98 193 0xC3; //Set PLL Bypass, Remove 10k DVDD shunt to ground, set PLL input to MCLK, enable the PLL clock inputs
w 0x98 202 0x40; //Set PLL Parameters

w 0x90 1 0xFF;   //Enable Interpolation and modulator clocks for all 8 channels
w 0x90 2 0x01;   //Enable the TDM decoder

//Sample Rate register (MCLK/fs ratio)
//w 0x90 3 0x00;   //MCLK = 128FS Eg, 49.152MHz/384kHz
//w 0x90 3 0x01;   //MCLK = 256FS Eg, 49.152MHz/192kHz
//w 0x90 3 0x03;   //MCLK = 512FS Eg, 49.152MHz/96kHz
w 0x90 3 0x07;   //MCLK = 1024FS Eg, 49.152MHz/48kHz

//This sets BCK and WS frequency
//w 0x90 4 0x00;   //BCK & WS = 128FS, TDM512
w 0x90 4 0x01;   //BCK & WS = 256FS, TDM256
//w 0x90 4 0x03;   //BCK & WS = 512FS, TDM128
//w 0x90 4 0x07;   //BCK & WS = 1024FS, TDM64 (I2S)

w 0x90 5 0xFF;   //Enable all 8 channels Analog section.
w 0x90 6 0x1F;   //Set the PNEG charge pump clock frequency to 705.6kHz or 768kHz (depending on MCLK being 22.5792MHz or 24.576MHz)
w 0x90 7 0xBB;   //Setup automated delay sequence for analog section quietest pop
w 0x90 51 0x80;  //Force a PLL_LOCKL signal from analog since it it bypassed to prevent muting the DAC automatically

//TDM Registers
w 0x90 77 0x10;  //Enable Master Mode
w 0x90 78 0x03;  //Invert Master mode WS and BCK
w 0x90 79 0x27;  //Scale WS by 4 (WS = 4*256FS = 1024FS), set 8 TDM slots per frame
w 0x90 80 0xC8;  //Set TDM to Left Justified mode and WS positive valid edge, TDM_VALID_PULSE_LEN = 8
w 0x90 84 0x00;  //TDM_CH1_LINE_SEL = 00 (DATA2), TDM_CH1_SLOT_SEL = 0
w 0x90 85 0x01;  //TDM_CH2_LINE_SEL = 00 (DATA2), TDM_CH2_SLOT_SEL = 1
w 0x90 86 0x02;  //TDM_CH3_LINE_SEL = 00 (DATA2), TDM_CH3_SLOT_SEL = 2
w 0x90 87 0x03;  //TDM_CH4_LINE_SEL = 00 (DATA2), TDM_CH4_SLOT_SEL = 3
w 0x90 88 0x04;  //TDM_CH5_LINE_SEL = 00 (DATA2), TDM_CH5_SLOT_SEL = 4
w 0x90 89 0x05;  //TDM_CH6_LINE_SEL = 00 (DATA2), TDM_CH6_SLOT_SEL = 5
```

```
w 0x90 90 0x06;  //TDM_CH7_LINE_SEL = 00 (DATA2), TDM_CH7_SLOT_SEL = 6
w 0x90 91 0x07;  //TDM_CH8_LINE_SEL = 00 (DATA2), TDM_CH8_SLOT_SEL = 7

w 0x90 109 0xE4; //Set Dither into the IIR filters for best low level linearity

//THD Compensation Registers
w 0x90 111 0x68; //THD C2 Coefficient for CH1/3/5/7
w 0x90 112 0x01; //THD C2 Coefficient for CH1/3/5/7
w 0x90 113 0x8D; //THD C3 Coefficient for CH1/3/5/7
w 0x90 115 0x68; //THD C2 Coefficient for CH2/4/6/8
w 0x90 116 0x01; //THD C2 Coefficient for CH2/4/6/8
w 0x90 117 0x8D; //THD C3 Coefficient for CH2/4/6/8

//Automute Registers
w 119 0xFF; //Enable Automute for 8 channels
w 120 0x0F; //Set Automute parameters
w 121 0xC0; //Set Automute parameters
w 122 0x08; //Set Automute Engage level to -120.4dB
w 124 0x0A; //Set Automute Disengage level to -118.4dB

//NSMOD Registers
w 0x90 128 0xCC; //Set the NSMOD dither phases for best performance if summing channels
together, (NOTE: not strictly needed for 8 channel mode)
w 0x90 129 0x54; //Set NSMOD dither type, and use 1/8th gain parameter in the NSMOD
w 0x90 131 0x44; //Set the Amount of dither into the NSMOD CH1/2 quantizer to best
linearity
w 0x90 132 0x44; //Set the Amount of dither into the NSMOD CH3/4 quantizer to best
linearity
w 0x90 133 0x44; //Set the Amount of dither into the NSMOD CH5/6 quantizer to best
linearity
w 0x90 134 0x44; //Set the Amount of dither into the NSMOD CH7/8 quantizer to best
linearity

//DRE Registers
w 0x90 136 0xFF; //Set the DRE to turn off the THDR at low volume for power saving, and to
swap analog and digital gain at low volume for best DNR
w 0x90 139 0xFF; //Allow DRE to still trigger is there is a small DC offset in the music.
(Some recordings have small DC offsets in them)
w 0x90 140 0x56; //Set DRE digital gain of CH1/3/5/7 to 16.37dB to match the Analog
attenuate amount when DRE turns on
w 0x90 141 0x1A; //Set DRE digital gain to CH1/3/5/7 to 16.37dB to match the Analog
attenuate amount when DRE turns on
w 0x90 142 0x56; //Set DRE digital gain to CH2/4/6/8 to 16.37dB to match the Analog
attenuate amount when DRE turns on
```

```
w 0x90 143 0x1A; //Set DRE digital gain to CH2/4/6/8 to 16.37dB to match the Analog attenuate amount when DRE turns on
w 0x90 144 0xF1; //Set DRE ON threshold to -48dB
w 0x90 145 0x0C; //Set DRE ON threshold to -48dB
w 0x90 146 0x84; //Set DRE OFF threshold to -28dB
w 0x90 147 0x81; //Set DRE OFF threshold to -28dB
w 0x90 148 0x8F; //Set DRE decay rate (time it takes to automatically engage DRE if the signal drops below the DRE ON threshold

//Enable Audio
w 0x90 92 0x10;  //Toggle DAC clock Resync to line up all the clocks in the DAC core for best analog performance
w 0x90 92 0x0F;  //Toggle DAC clock Resync to line up all the clocks in the DAC core for best analog performance
w 0x90 92 0x00;  //Toggle DAC clock Resync to line up all the clocks in the DAC core for best analog performance
w 0x90 0 0x02;   //Turn on the AMP  (This runs a state machine to gracefully turn on the DAC's)
```

TDM Slave

```
//Initialize Slave Mode TDM with 8 channels, MCLK = 49.152MHz, fs = 48kHz, DRE enabled, automute enabled
w 0x98 192 0x03; //Set GPIO1 (MCLK) pad to input mode, Invert CLKHV phase for better DNR
w 0x98 193 0xC3; //Set PLL Bypass, Remove 10k DVDD shunt to ground, set PLL input to MCLK, enable the PLL clock inputs
w 0x98 202 0x40; //Set PLL Parameters

w 1 0xFF;   //Enable Interpolation and modulator clocks for all 8 channels
w 2 0x01;   //Enable the TDM decoder

//Sample Rate register (MCLK/fs ratio)
//w 3 0x00;   //MCLK = 128FS Eg, 49.152MHz/384kHz
//w 3 0x01;   //MCLK = 256FS Eg, 49.152MHz/192kHz
//w 3 0x03;   //MCLK = 512FS Eg, 49.152MHz/96kHz
w 3 0x07;   //MCLK = 1024FS Eg, 49.152MHz/48kHz

w 5 0xFF;   //Enable all 8 channels Analog section.
w 6 0x1F;   //Set the PNEG charge pump clock frequency to 705.6kHz or 768kHz (depending on MCLK being 22.5792MHz or 24.576MHz)
w 7 0xBB;   //Setup automated delay sequence for analog section quietest pop
w 51 0x80;  //Force a PLL_LOCKL signal from analog since it it bypassed to prevent muting the DAC automatically

//TDM Registers
```

```
w 77 0x00;  //Enable Slave Mode
w 79 0x07;  //Set 8 TDM slots per frame
w 80 0xC8;  //Set TDM to Left Justified mode and WS positive valid edge,
TDM_VALID_PULSE_LEN = 8
w 84 0x00;  //TDM_CH1_LINE_SEL = 00 (DATA2), TDM_CH1_SLOT_SEL = 0
w 85 0x01;  //TDM_CH2_LINE_SEL = 00 (DATA2), TDM_CH2_SLOT_SEL = 1
w 86 0x02;  //TDM_CH3_LINE_SEL = 00 (DATA2), TDM_CH3_SLOT_SEL = 2
w 87 0x03;  //TDM_CH4_LINE_SEL = 00 (DATA2), TDM_CH4_SLOT_SEL = 3
w 88 0x04;  //TDM_CH5_LINE_SEL = 00 (DATA2), TDM_CH5_SLOT_SEL = 4
w 89 0x05;  //TDM_CH6_LINE_SEL = 00 (DATA2), TDM_CH6_SLOT_SEL = 5
w 90 0x06;  //TDM_CH7_LINE_SEL = 00 (DATA2), TDM_CH7_SLOT_SEL = 6
w 91 0x07;  //TDM_CH8_LINE_SEL = 00 (DATA2), TDM_CH8_SLOT_SEL = 7

w 109 0xE4; //Set Dither into the IIR filters for best low level linearity

//THD Compensation Registers
w 111 0x68; //THD C2 Coefficient for CH1/3/5/7
w 112 0x01; //THD C2 Coefficient for CH1/3/5/7
w 113 0x8D; //THD C3 Coefficient for CH1/3/5/7
w 115 0x68; //THD C2 Coefficient for CH2/4/6/8
w 116 0x01; //THD C2 Coefficient for CH2/4/6/8
w 117 0x8D; //THD C3 Coefficient for CH2/4/6/8

//Automute Registers
w 119 0xFF; //Enable Automute for 8 channels
w 120 0x0F; //Set Automute parameters
w 121 0xC0; //Set Automute parameters
w 122 0x08; //Set Automute Engage level to -120.4dB
w 124 0x0A; //Set Automute Disengage level to -118.4dB

//NSMOD Registers
w 128 0xCC; //Set the NSMOD dither phases for best performance if summing channels
together, (NOTE: not strictly needed for 8 channel mode)
w 129 0x54; //Set NSMOD dither type, and use 1/8th gain parameter in the NSMOD
w 131 0x44; //Set the Amount of dither into the NSMOD CH1/2 quantizer to best linearity
w 132 0x44; //Set the Amount of dither into the NSMOD CH3/4 quantizer to best linearity
w 133 0x44; //Set the Amount of dither into the NSMOD CH5/6 quantizer to best linearity
w 134 0x44; //Set the Amount of dither into the NSMOD CH7/8 quantizer to best linearity

//DRE Registers
w 136 0xFF; //Set the DRE to turn off the THDR at low volume for power saving, and to swap
analog and digital gain at low volume for best DNR
```

```
w 139 0xFF; //Allow DRE to still trigger is there is a small DC offset in the music.  (Some recordings have small DC offsets in them)
w 140 0x56; //Set DRE digital gain of CH1/3/5/7 to 16.37dB to match the Analog attenuate amount when DRE turns on
w 141 0x1A; //Set DRE digital gain to CH1/3/5/7 to 16.37dB to match the Analog attenuate amount when DRE turns on
w 142 0x56; //Set DRE digital gain to CH2/4/6/8 to 16.37dB to match the Analog attenuate amount when DRE turns on
w 143 0x1A; //Set DRE digital gain to CH2/4/6/8 to 16.37dB to match the Analog attenuate amount when DRE turns on
w 144 0xF1; //Set DRE ON threshold to -48dB
w 145 0x0C; //Set DRE ON threshold to -48dB
w 146 0x84; //Set DRE OFF threshold to -28dB
w 147 0x81; //Set DRE OFF threshold to -28dB
w 148 0x8F; //Set DRE decay rate (time it takes to automatically engage DRE if the signal drops below the DRE ON threshold


//Enable Audio
w 92 0x10;  //Toggle DAC clock Resync to line up all the clocks in the DAC core for best analog performance
w 92 0x0F;  //Toggle DAC clock Resync to line up all the clocks in the DAC core for best analog performance
w 92 0x00;  //Toggle DAC clock Resync to line up all the clocks in the DAC core for best analog performance
w 0 0x02;   //Turn on the AMP  (This runs a state machine to gracefully turn on the DAC's)
```

Revision History

Current Version 0.4.3

Rev.	Date	Notes
0.1	December 10, 2020	Initial Release
0.1.1	December 20, 2020	• Added Recommended Power-Up Sequence • Removed “ESS” logo from pinout
0.2	January 25, 2021	• Removed GPIO7-10 references • Added Register Descriptions for Registers 7,50[6:3]&[0],82,109,128-129 • Added Register Descriptions for Registers 131-134,136,139 • Added Audio Interface Timing • Added APLL frequency formula and block diagram • Added Reflow Process Considerations • Added Top View Marking • Added notes on DSD automute and power savings with GPIO5/6 connection to schematic • Added PCM frequency and impulse responses for the 5 built in digital filters • Register 0[5:2] are reserved • Added note on THD compensation using differential mode
0.2.1	January 28, 2021	• Added PLL Bypass to APLL diagram
0.2.2	January 29, 2021	• Added Register Descriptions for Registers 92 & 195 • Added equations for Register 102-104
0.2.3	March 15, 2021	• Updated Registers 200-202 descriptions
0.3	April 18, 2021	• Corrected typo for registers 94-101 for 8’bxx to 8’dxx • Updated PLL section • Corrected Automute_time equation • Updated Register 202,203 Descriptions • Updated Registers 5[2:1] & 6 Descriptions • Updated Register 31 Defaults • Updated HBM & CDM values • Updated Register 200 [0] description
0.3.1	June 1, 2021	• Updated Registers 6,49,193 descriptions • Added Register 127 descriptions • Updated Register 126[4:0] with formula • Moved S/PDIF encoders to Output Formats • Updated Registers 121-120[10:0] Automute time equation • Added Register 123-122 Automute level equation • Added Register 125-124 Automute OFF level equation • Recommend change Register 129[6:4] to 3’d5 for all sample rates. • Added Register 60 Weak Keeper definition • Added Digital Filter characteristics
0.3.2	June 15, 2021	• Updated most register descriptions for clarity • Minor formatting changes • Modified Register order in APLL configuration, Register 202 to be written first. • Updated Register 136 Descriptions • Updated Register 62 mnemonic names for clarity

		• Added clock distribution section
0.4	August 25, 2021	• Added TDM timing diagram • Updated names and descriptions for registers 136 and 62 • Added THD compression calculation • Changed equations in registers 102-104 • Added soft mute, automute, and volume control sections • Added note on reserved registers to register listing section • Major formatting updates • Unreserved register 49[5:4], 8 • Updated Digital Signal Path section • Added de-emphasis filter section • Added DRE section • Added note on *SPDIF_SEL_GPIO#* registers in S/PDIF encoders section • Added Clock Distribution tables
0.4.1	October 6th, 2021	• Added PLL configurations Table • Register 154 updated for clarity, it is a digital gain • Added w/o DRE DNR performance number • Corrected Register Map table • Added note regarding DSD for Register 82[5] ENABLE_WS_MONITOR • Updated Registers 129, 203, 140-143 descriptions • Unreserved Register 80[5:0] TDM_VALID_PULSE_LEN • Added Addendum for example setup register listings • Updated some descriptions in Synchronous Slave Interface registers • Reserved Register 77[6], default is required • Corrected Register 144-147 description values • Updated Digital Signal Path diagram with DSD/DoP & SPDIF path
0.4.2	October 26th, 2021	• Updated DNR performance values w/o DRE, added 4ch[SE], stereo[Diff], mono
0.4.3	April 7th, 2022	• Removed incorrect Power Up sequence, updated Power Up and Down sequences • Updated filter characteristics with additional passband • Removed Automute reference to DSD as Automute is only available for PCM • Updated Register 31 Bit 4 Default state • Corrected Register 49 Bit configuration • Unreserved Register 51[7] FORCE_PLL_LOCK • Updated Registers 59-58, 61-60 Defaults • Updated Registers 84-91[3:0] Description 4 bits for 16 slots • Updated Register 104 Default state in description • Added Register 225 (CHIP_ID) as 8'h67 • Added Note on DRE section • Updated Registers 248-247 Bits width • Updated Registers 68-76 PWM descriptions for valid ranges • Updated Reference schematic for readability • Added Note to Register 51 FORCE_PLL_LOCK