The Sabre ES9033 High Performance Audio DAC is a 32-Bit, 2-channel audio DAC that brings professional, digital audio quality to the consumer home entertainment market.

Using ESS' patented HyperStream ® II architecture, the Sabre ES9033 delivers studio quality audio with 122dB DNR (w / DRE) and -108dB THD+N.

With the integrated line drivers, the ES9033 reduces BOM costs by eliminating the need for external amplifier to produce a line level 2Vrms output.

The Sabre ES9033 flexible input architecture accepts up to serial 32-bit serial PCM data to 768kHz sample rate & DSD512.

The Sabre DAC sets a new standard for high-quality audio performance in a cost-effective, compact, easy to use form factor for today's most demanding digital audio applications.

Feature	Description
+122dB DNR (w/ DRE) per channel -108dB THD+N per channel	Unprecedented dynamic range and ultra-low distortion
High Sample Rates	Support for up to PCM 768kHz & DSD512
2-channel DAC + Line Driver in 28-QFN	Reduced footprint and simplifies board layout
Multiple formats available	PCM, TDM, DSD, DoP input data formats.
Customizable filter characteristics	8 preset filters
I2C, SPI, and Hardware interface control	Configured by microcontroller or other I2C/SPI source, or pins through Hardware Mode
Integrated low noise DAC reference regulators	Reduced BOM cost, PCB area and improved DNR.
Low Pin Count Standardized Packaging	5mm x 5mm, 28 pin QFN
2Vrms Integrated Line Driver	Reduces BOM costs w/o required external op-amp required for line driver levels
Analog PLL (APLL)	Simplifies clocking requirements and reduces PCB size and BOM cost

APPLICATIONS

- Media Streamer Applications
- Gaming Motherboards
- Audio Receivers
- Professional Audio Equipment
- Active Speakers

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Functional Block Diagram

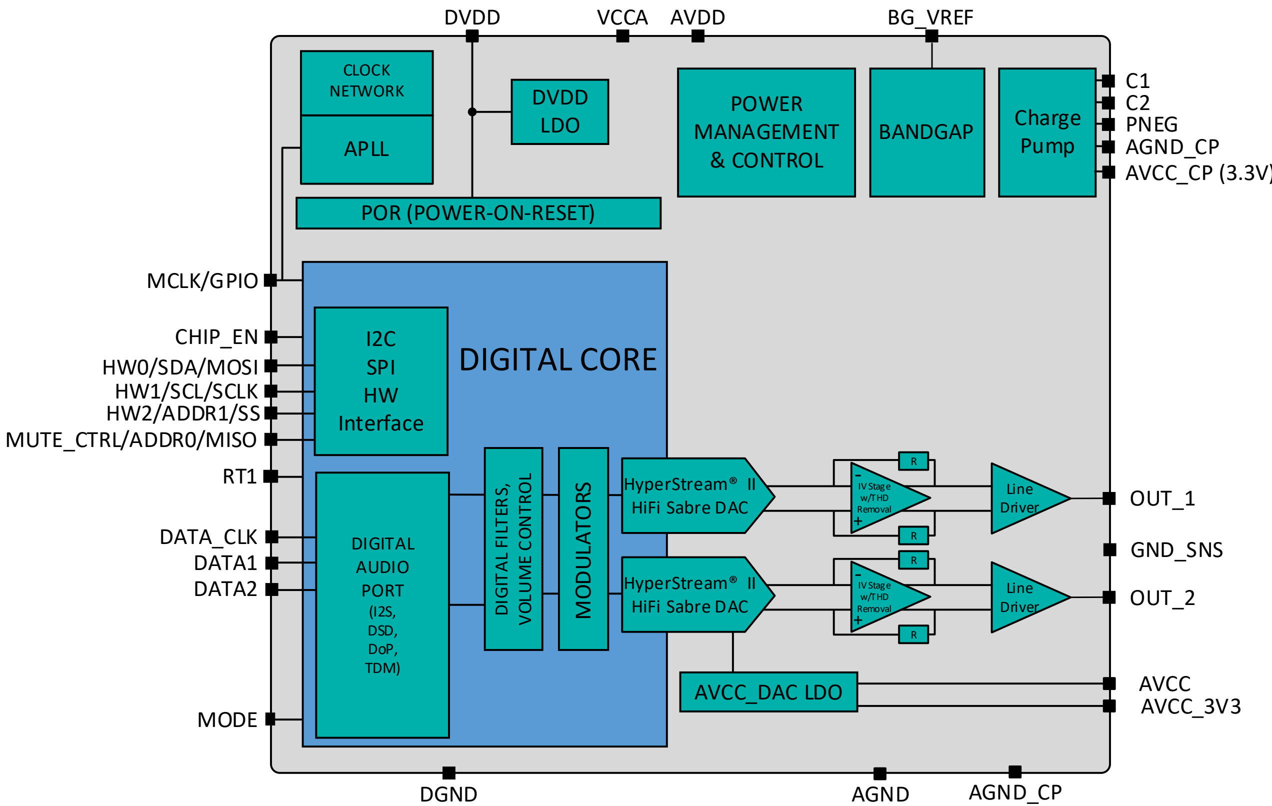


Figure 1 - ES9033 Block Diagram

ES9033Q Package

28 QFN Pinout

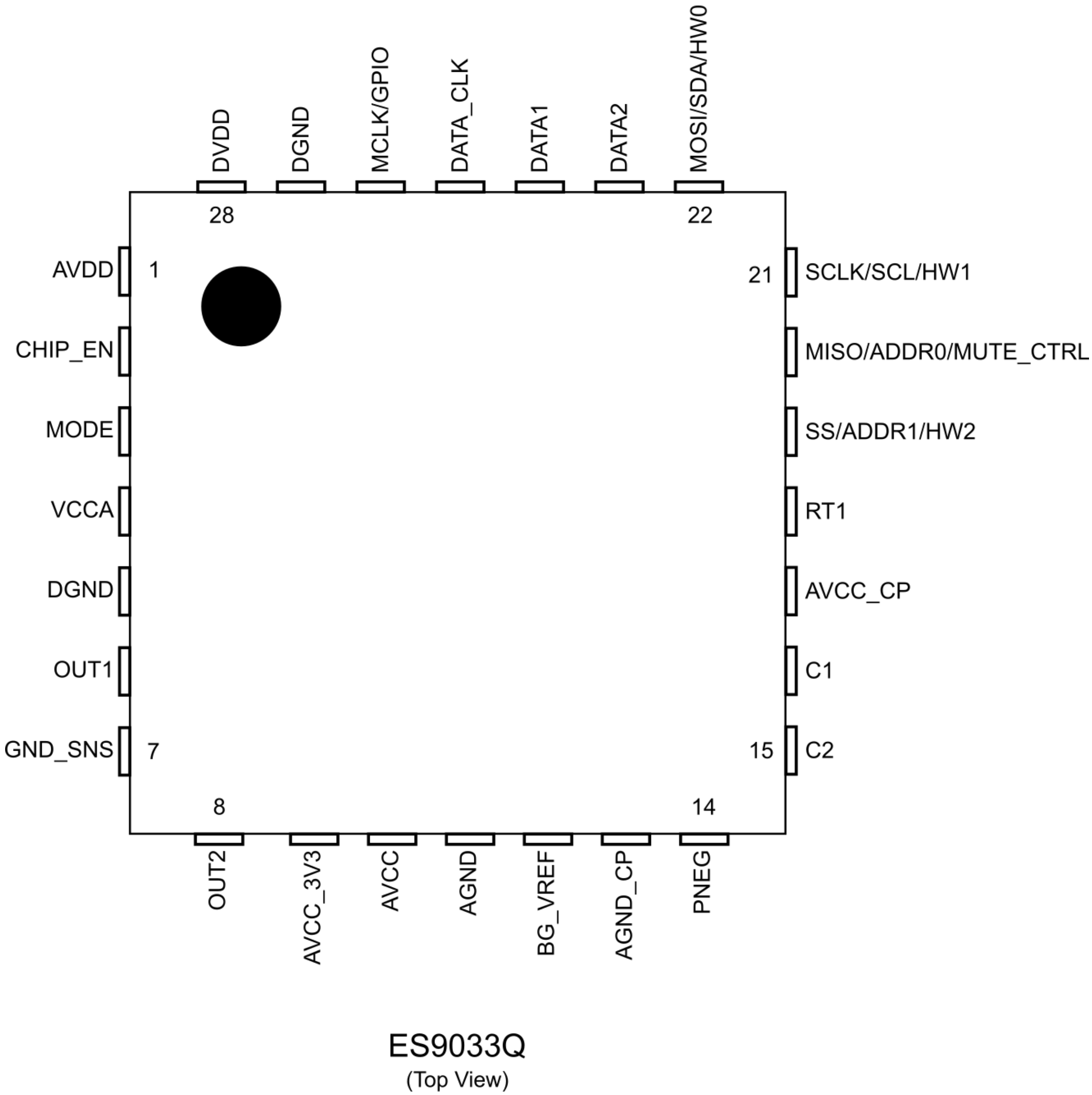


Figure 2 - 28 QFN pinout

28 QFN Pin Descriptions

Pin	Name	Pin Type	Reset State	Pin Description
1	AVDD	Power	Power	3.3V I/O supply
2	CHIP_EN	I/O	HiZ	Active-high chip enable.
3	MODE	I/O	HiZ	Control for SPI/I2C/HW modes
4	VCCA	Power	Power	Analog Supply
5	DGND	Ground	Ground	Digital ground
6	OUT1	AO	Ground	Output channel 1
7	GND_SNS	AI	Ground	Line driver load ground voltage sense
8	OUT2	AO	Ground	Output channel 2
9	AVCC_3V3	Power	Power	Analog Regulator 3.3V Supply
10	AVCC	Power	Power	Analog Regulator Output, internally supplied
11	AGND	Ground	Ground	Analog ground
12	BG_VREF	AO	Ground	Bandgap Voltage reference
13	AGND_CP	Ground	Ground	Analog Ground for charge pump
14	PNEG	Power	Ground	Integrated charge pump output. Line driver negative supply.
15	C2	-	-	Line driver negative flying capacitor
16	C1	-	-	Line driver positive flying capacitor
17	AVCC_CP	Power	Power	Analog Supply for charge Pump
18	RT1	I	HiZ	Reserved. **Must be connected to DGND for normal operation**.
19	SS/ADDR1/HW2	I/O	HiZ	Interface Signal (SPI/I2C/Hardware modes)
20	MISO/ADDR0/MUTE_CTRL	I/O	HiZ	Interface Signal (SPI/I2C/Hardware modes)
21	SCLK/SCL/HW1	I/O	HiZ	Interface Signal (SPI/I2C/Hardware modes)
22	MOSI/SDA/HW0	I/O	HiZ	Interface Signal (SPI/I2C/Hardware modes)
23	DATA2	I/O	HiZ	Serial DATA2
24	DATA1	I/O	HiZ	Serial DATA1
25	DATA_CLK	I	HiZ	Serial data clock
26	MCLK/GPIO	I/O	HiZ	MCLK input, General I/O
27	DGND	Ground	Ground	Digital core ground
28	DVDD	Power	Power	Digital core supply, internally supplied
29	Package PAD[1]	-	-	Not electrically connected, used for heat dissipation

Table 1 - 28 QFN pin descriptions

[1] Pin 29 is the package pad. See 28 QFN package dimensions for sizing

Configuration Modes

Hardware Mode

The ES9033 has 31 pre-configured modes that can be set with external pin configuration. These modes configure the DAC for different input serial data rates and set the DAC muting.

These modes are set with pins:

- MODE (Pin 3)
- HW0 (Pin 22)
- HW1 (Pin 21)
- HW2 (Pin 19)
- MUTE_CTRL (Pin 20)

Each hardware mode pin has 4 states:

- 0 – Pin directly connected to GND
- 1 – Pin directly connected to AVDD
- Pull 0 – Pin pulled to GND through 47kΩ resistor
- Pull 1 – Pin pulled to AVDD through 47kΩ resistor

Design Information

Each hardware mode pin can be configured with either a pull-up or pull-down resistor. Therefore, it is important that the pin is configured to allow for the desired hardware modes. Some guidelines include the following:

- By placing a pull-down resistor on the MODE pin, the device is limited to hardware modes with DRE. Alternatively, if a pull-up resistor is placed on the MODE pin, the device is limited to non-DRE modes.
- By placing a pull-down resistor on the HW2 pin, the device can no longer access modes 8-11 or modes 24-27. Alternatively, if a pull-up resistor is places on the HW2 pin, the device can no longer use LJ Master mode with an external MCLK.
- The HW0 and HW1 pins never require a pull up or pull-down resistor.

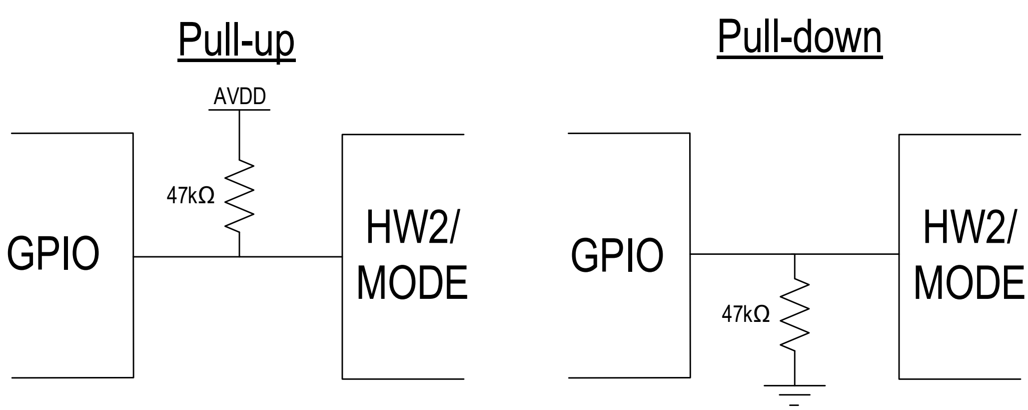


Figure 3 - Hardware mode pin configurations

Muting

MUTE_CTRL (Pin 20) is used to control the muting of the output and enabling of the Automute feature while in Hardware Mode:

- 0 – Output Muted
- 1 – Output Unmuted
- Pull 0 – Output Muted
- Pull 1 – Output Unmuted, Automute Enabled.

Hardware Mode Pin Configurations

HW Mode	FS (kHz)	BCK (MHz)	MCLK (MHz)	BCK/Channel	MODE	HW2	HW1	HW0
	I2S Master Mode, Ext MCLK (DRE)							
0	MCLK / 128	MCLK / 2	5 < MCLK < 50	32	Pull 0	0	0	0
1	MCLK / 256	MCLK / 4	5 < MCLK < 50	32	Pull 0	0	0	1
2	MCLK / 512	MCLK / 8	5 < MCLK < 50	32	Pull 0	0	1	0
3	MCLK / 1024	MCLK / 16	5 < MCLK < 50	32	Pull 0	0	1	1
	LJ Master, EXT MCLK (DRE)							
4	MCLK / 128	MCLK / 2	5 < MCLK < 50	32	Pull 0	Pull 0	0	0
5	MCLK / 256	MCLK / 4	5 < MCLK < 50	32	Pull 0	Pull 0	0	1
6	MCLK / 512	MCLK / 8	5 < MCLK < 50	32	Pull 0	Pull 0	1	0
7	MCLK / 1024	MCLK / 16	5 < MCLK < 50	32	Pull 0	Pull 0	1	1
	I2S Slave, EXT MCLK, Auto Detect (DRE)							
8	Auto (8 < FS < 384)	64FS	128FS < MCLK < 50	32	Pull 0	Pull 1	0	0
	I2S Slave, PLL from BCK (DRE)							
9	48	3.072	49.152 from PLL	32	Pull 0	Pull 1	0	1
10	96	6.144	49.152 from PLL	32	Pull 0	Pull 1	1	0
11	192	12.288	49.152 from PLL	32	Pull 0	Pull 1	1	1
	DSD Slave, EXT MCLK, Auto Detect (DRE)							
12	64FS	64FS	5 < MCLK < 50	32	Pull 0	1	0	0
	LJ Slave, PLL from BCK (DRE)							
13	48	3.072	49.152 from PLL	32	Pull 0	1	0	1
14	96	6.144	49.152 from PLL	32	Pull 0	1	1	0
15	192	12.288	49.152 from PLL	32	Pull 0	1	1	1
	I2S Master Mode, Ext MCLK (no DRE)							
16	MCLK / 128	MCLK / 2	5 < MCLK < 50	32	Pull 1	0	0	0
17	MCLK / 256	MCLK / 4	5 < MCLK < 50	32	Pull 1	0	0	1
18	MCLK / 512	MCLK / 8	5 < MCLK < 50	32	Pull 1	0	1	0
19	MCLK / 1024	MCLK / 16	5 < MCLK < 50	32	Pull 1	0	1	1
	LJ Master, EXT MCLK (no DRE)							

20	MCLK / 128	MCLK / 2	5 < MCLK < 50	32	Pull 1	Pull 0	0	0
21	MCLK / 256	MCLK / 4	5 < MCLK < 50	32	Pull 1	Pull 0	0	1
22	MCLK / 512	MCLK / 8	5 < MCLK < 50	32	Pull 1	Pull 0	1	0
23	MCLK / 1024	MCLK / 16	5 < MCLK < 50	32	Pull 1	Pull 0	1	1
	I2S Slave, EXT MCLK, Auto Detect (no DRE)							
24	Auto (8 < FS < 384)	64FS	128FS < MCLK < 50	32	Pull 1	Pull 1	0	0
	I2S Slave, PLL from BCK (no DRE)							
25	48	3.072	49.152 from PLL	32	Pull 1	Pull 1	0	1
26	96	6.144	49.152 from PLL	32	Pull 1	Pull 1	1	0
27	192	12.288	49.152 from PLL	32	Pull 1	Pull 1	1	1
	DSD Slave, EXT MCLK, Auto Detect (no DRE)							
28	64FS	64FS	5 < MCLK < 50	32	Pull 1	1	0	0
	LJ Slave, PLL from BCK (no DRE)							
29	48	3.072	49.152 from PLL	32	Pull 1	1	0	1
30	96	6.144	49.152 from PLL	32	Pull 1	1	1	0
31	192	12.288	49.152 from PLL	32	Pull 1	1	1	1

Table 2 - Hardware mode pin configurations

Recommended Hardware Mode Setup Sequence

The hardware mode setup sequence is shown below with all hardware pins being defined before and after CHIP_EN is asserted.

Note: It is recommended that MUTE_CTRL is set low until the HW mode and CHIP_EN is finalized, then asserted last.

For all HW modes (Modes 0-31):

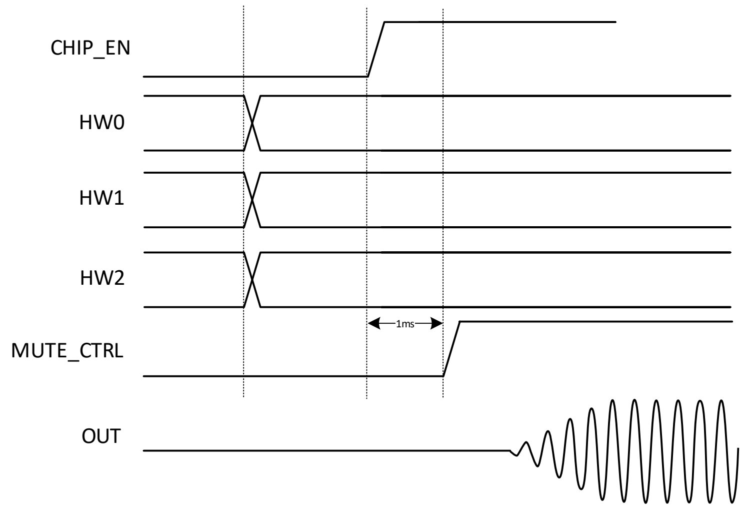


Figure 4 - Hardware mode startup sequence

Software Mode

To configure the ES9033 registers manually over I²C or SPI, connect the following pins:

I²C

- MODE (Pin 3) – ***GND***
- Connect per I²C standard
  - SDA (Pin 22)
  - SCL (Pin 21)
  - ADDR0 (Pin 20)
  - ADDR1 (Pin 19)

Available I2C Addresses for the ES9033Q:

I2C Address	ADDR1	ADDR0
0x90	***GND***	***GND***
0x92	***GND***	***AVDD***
0x94	***AVDD***	***GND***
0x96	***AVDD***	***AVDD***

Table 3 - I2C address configurations

SPI

- Mode (Pin 3) – **AVDD**
- Connect per SPI standard
  - SCLK (Pin 21)
  - SS (Pin 19)
  - MOSI (Pin 22)
  - MISO (Pin 20)

Digital Features

Digital Signal Path

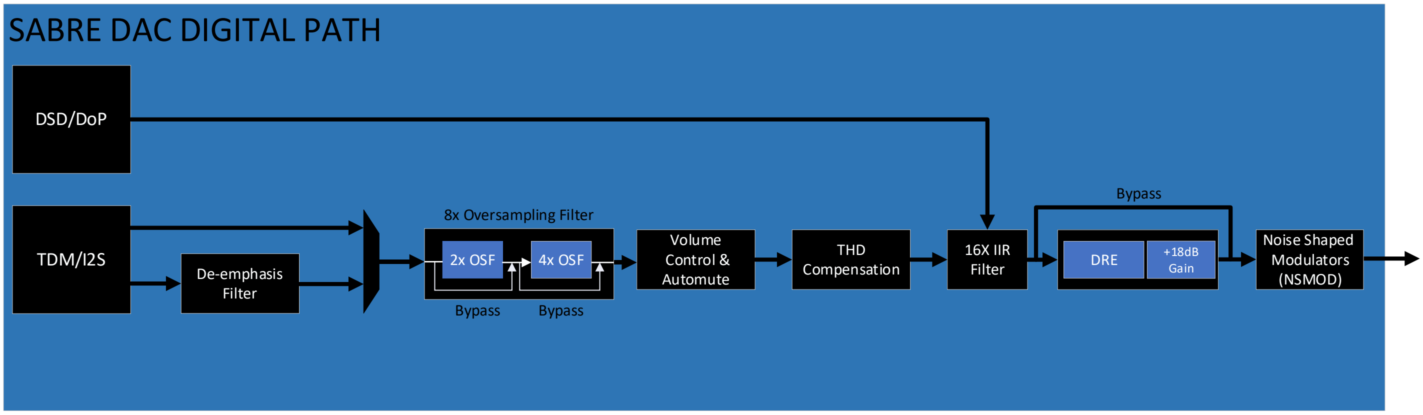


Figure 5 - Digital signal path block diagram

GPIO Configuration

GPIO_CONFIG	Function	I/O Direction
0	1'b0	Output
1	1'b0	Output
2	1'b1	Output
3	128 FS Block	Output
4	Interrupt Output	Output
5	Mute all channel	Input
6	System mode Control	Input
7	Reserved	Output
8	CLK_VALID flag	Output
9	PWM1	Output
10	PWM2	Output
11	PWM3	Output
12	Volume min	Output
13	Automute status	Output
14	Soft Ramp finished	Output
15	1'b0	Output

Table 4 – Standard GPIO Functions

For GPIO_CONFIG 12, 13, 14:

Register 26[0] (GPIO_SEL) selects which channel determines the flag status when the corresponding bits in Register 25[7:2] are set to 1'b0. See register listing for more detail.

Soft Mute

When Mute is asserted the digital signal level will be smoothly ramped to minimum. When Mute is de-asserted the digital signal level will ramp back up to the level set by the volume control register. Asserting Mute will not change the value stored in the volume control register. The volume ramp rate is controlled through registers 48-50.

Mute can be engaged through either the automute feature or by setting the mute bits for any individual channel through register 51: MUTE CTRL & CH INVERT.

Automute

Automute is disabled by default and is triggered when any one of the following conditions are met:

Mode	Detection Condition	Time
PCM	Data is lower than *automute_level* for longer than the *automute_time*	$\frac{2\hat{}18}{(automute\_time * FS)}$
DSD	Equal number of 1s and 0s in any 8 consecutive bits of data	$\frac{2\hat{}18}{(automute\_time * DCLK)}$
DoP	DSD data contains an equal number of 1s and 0s in any 8 consecutive bits of data	$\frac{2\hat{}18}{(automute\_time * DCLK)}$

Table 5 - Automute conditions

The automute feature is enabled for both channels individually through the AUTOMUTE_EN_CH2 and AUTOMUTE_EN_CH1 bits (register 64-63[12:11]). The thresholds that trigger and disable automute can be configured through registers 65-68.

Volume Control

This volume control is intended for use during audio playback. Each channel can be digitally attenuated from 0dB to –127.5dB. When a new volume level is set, the attenuation circuit will ramp softly to the new level.

Volume of both channels individually is configured through registers 46-47.

By default, channel volumes are updated as soon as the volume registers are written. However the volume control can be configured to only change once the RUN_VOLUME bit (register 51[5]) is toggled. This feature can be enabled or disabled through the FORCE_VOLUME bit (register 51[7]).

Both output channels have an independent volume control. The attenuation for the channels can be independent or synchronized in pairs by setting the DAC_USE_MONO_VOLUME bit (register 51[6]).

THD Compensation

THD Compensation can be used to minimize distortion from external PCB components and layout through the generation of inverse second and third harmonic components matching the target system distortion profile.

The coefficients are stored in Registers 56 – 61.

Audio Input Formats

For configuring TDM and I2S, use Registers 36-40

Time-division multiplexing (TDM)

The ES9033 supports up to 32 channels TDM modes.

I2S

Data is latched on the positive edge of BCK

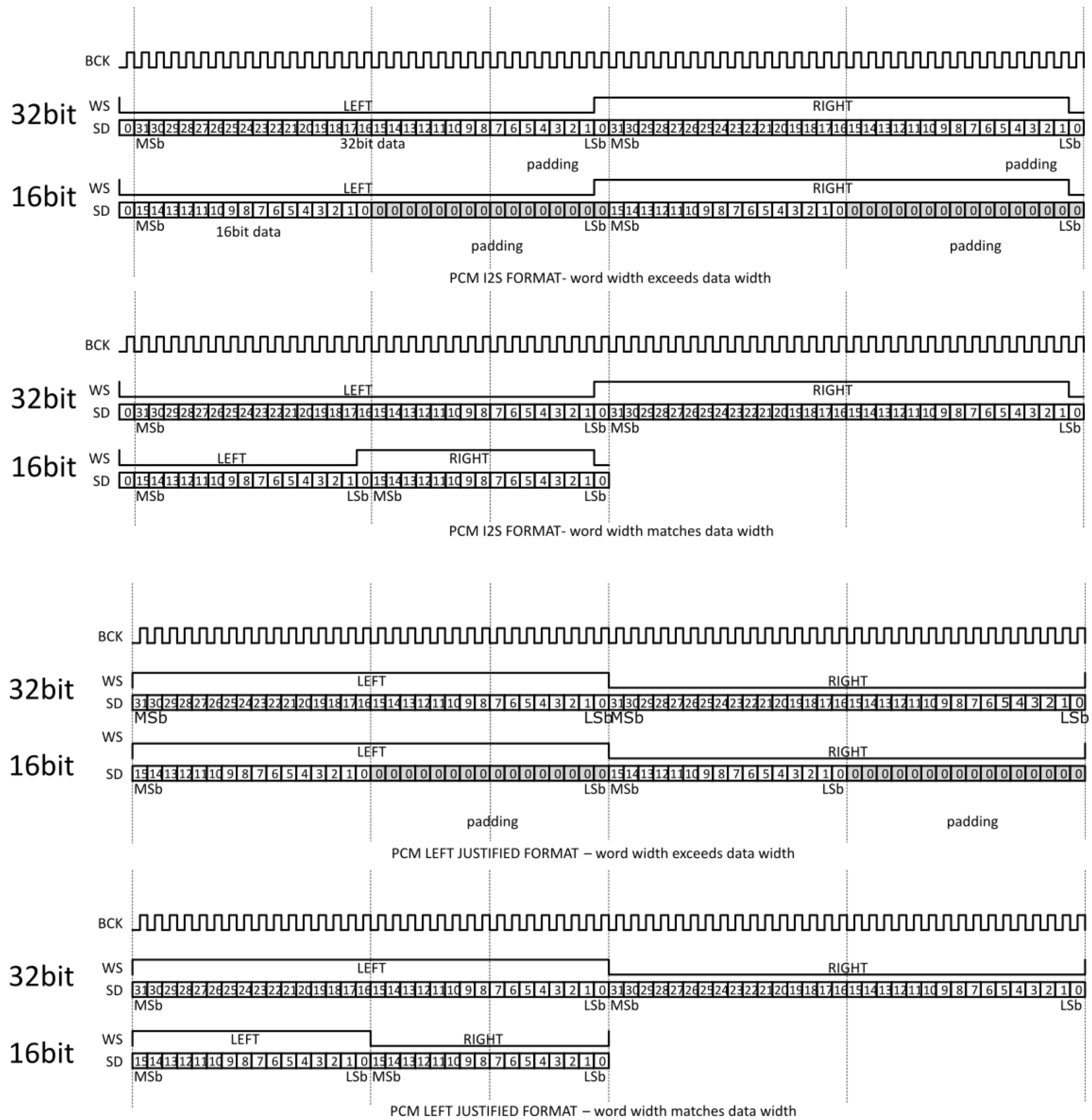


Figure 2 - I2S & LJ Output Format

DSD[2]

Data is latched on the positive edge of DCLK.

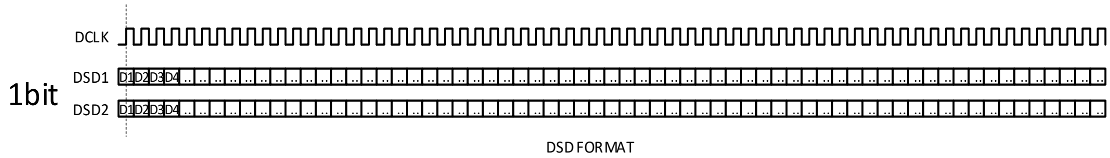


Figure 6 - DSD format

Pre-Programmed Digital Filters

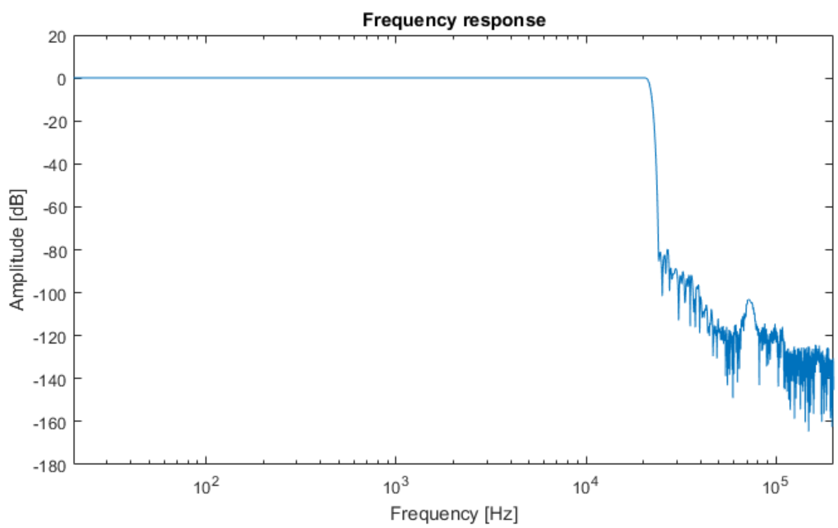
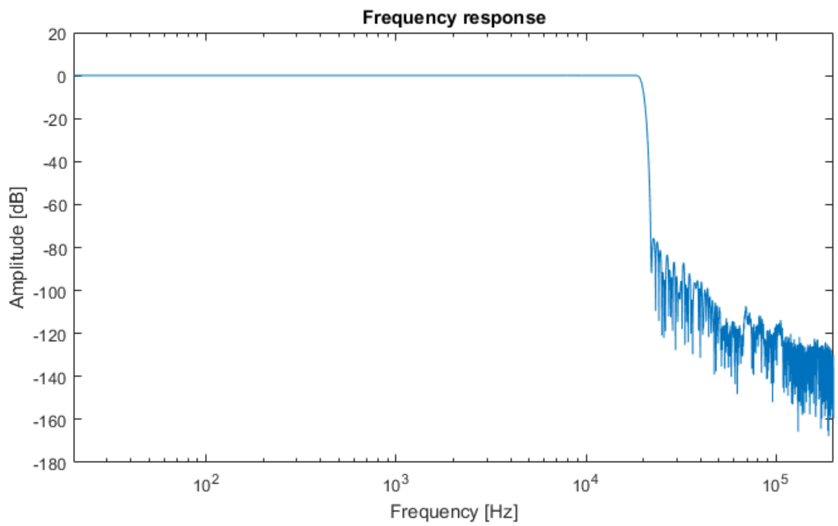
The ES9033 has 8 pre-programmed digital filters. The latency for each filter reduces (scales) with increasing sample rates.

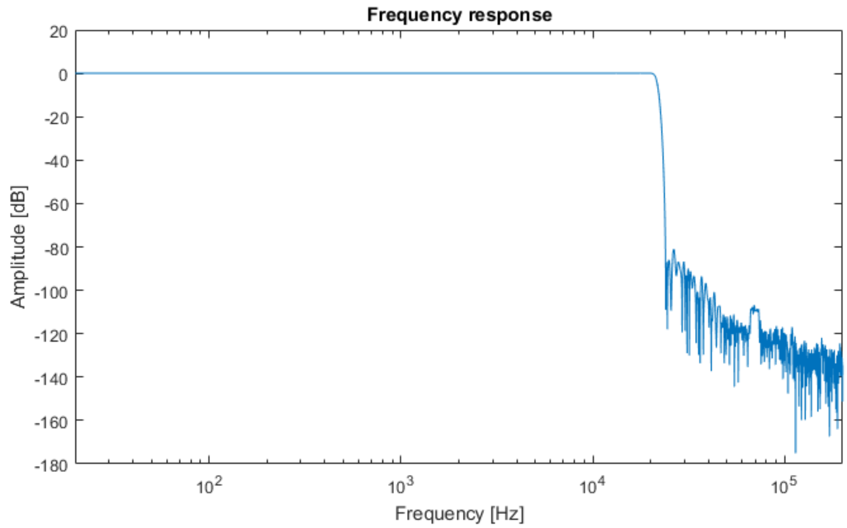
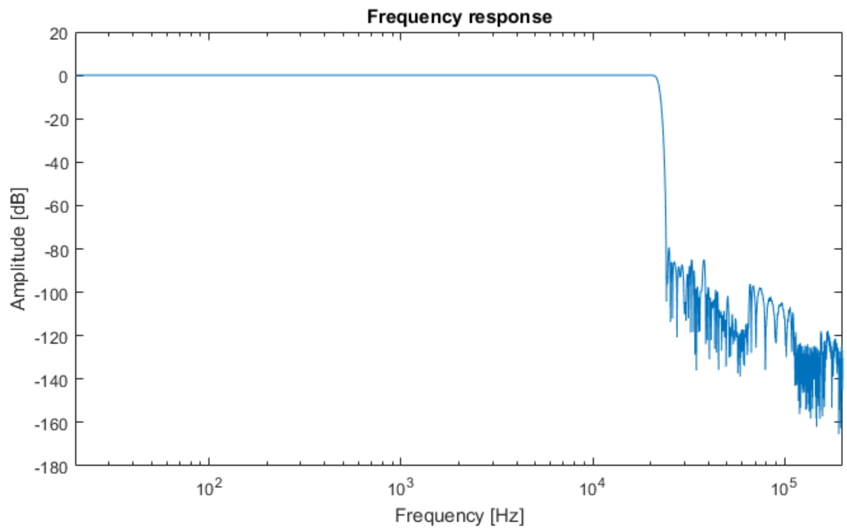
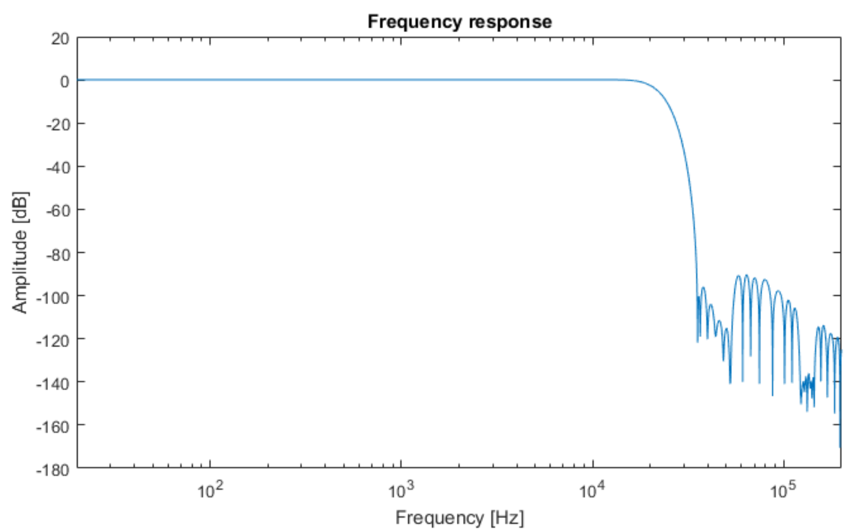
- Minimum Phase
- Linear Phase Apodizing
- Linear Phase Fast Roll-off
- Linear Phase Fast Roll-off Low Ripple
- Linear Phase Slow Roll-off
- Minimum Phase Fast Roll-off
- Minimum Phase Slow Roll-off
- Minimum Phase Slow Roll-off Low Dispersion

[2] The Automute Feature is not available when using DSD mode

PCM Filter Frequency Response

The following frequency responses were obtained from software simulations of these filters. Simulation sample rate is 44.1kHz.

Filter	Frequency Response
Minimum Phase	
Linear Phase Apodizing	

Linear Phase Fast Roll-off	
Linear Phase Fast Roll-off Low Ripple	
Linear Phase Slow Roll-off	

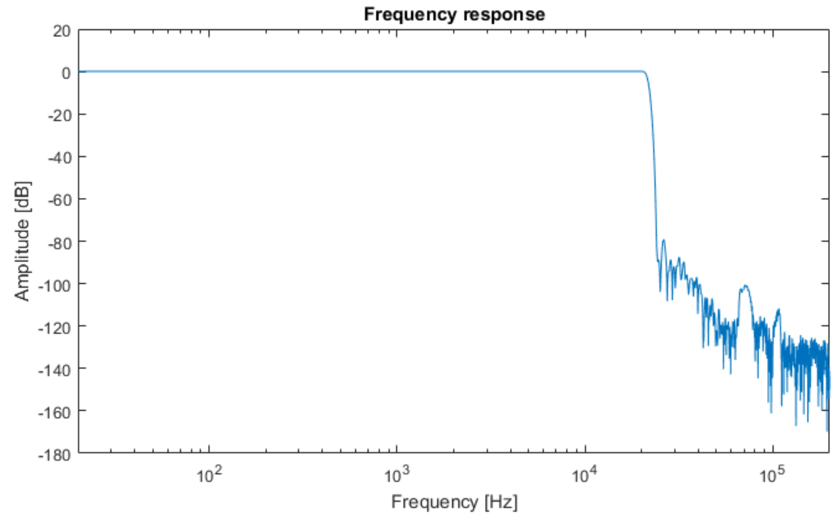
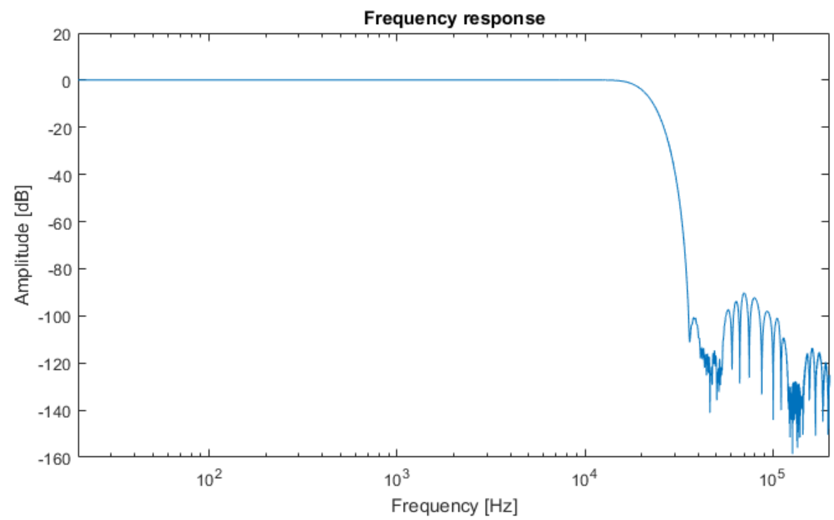
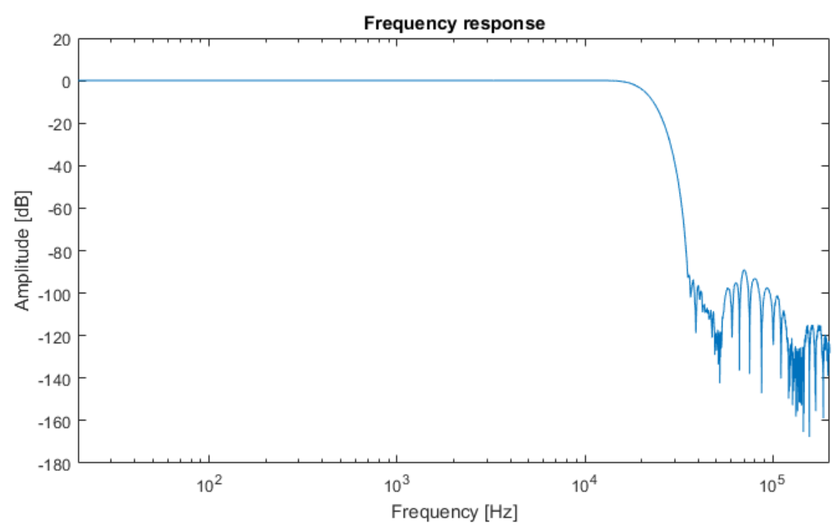
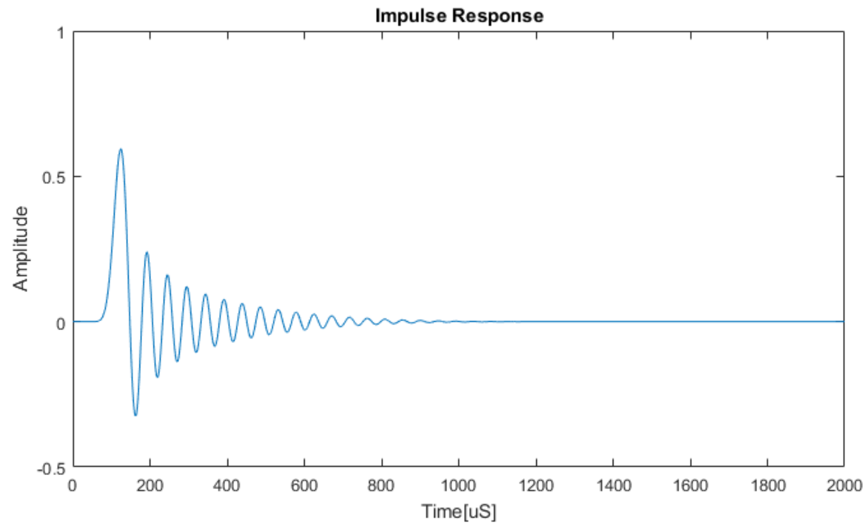
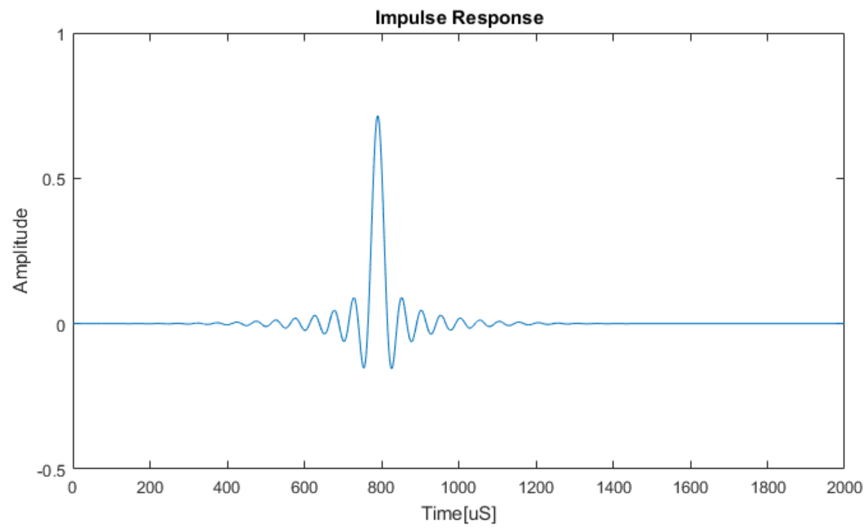
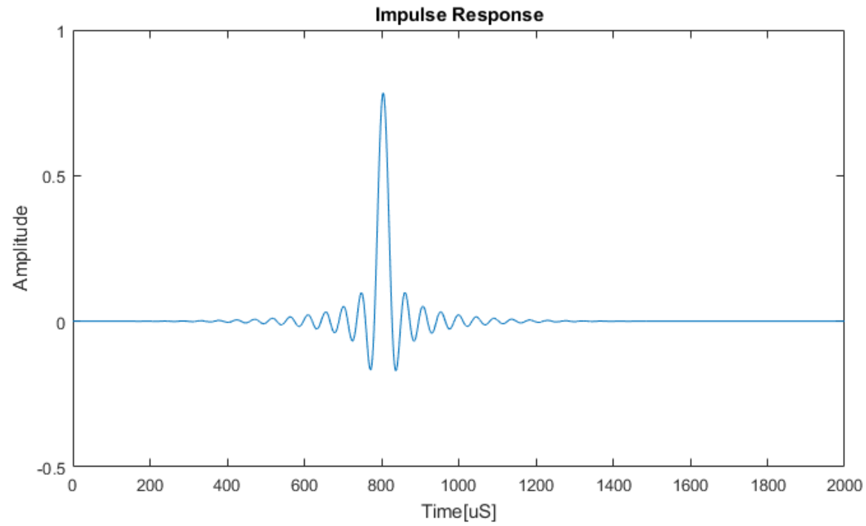
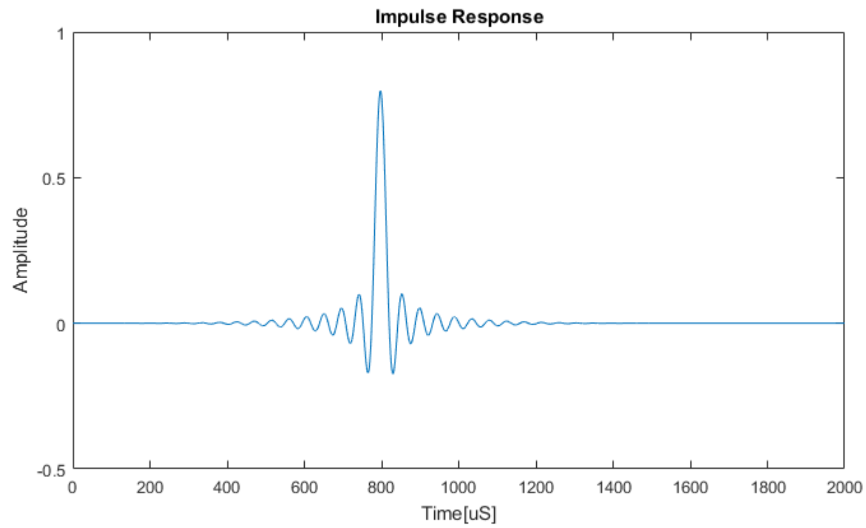
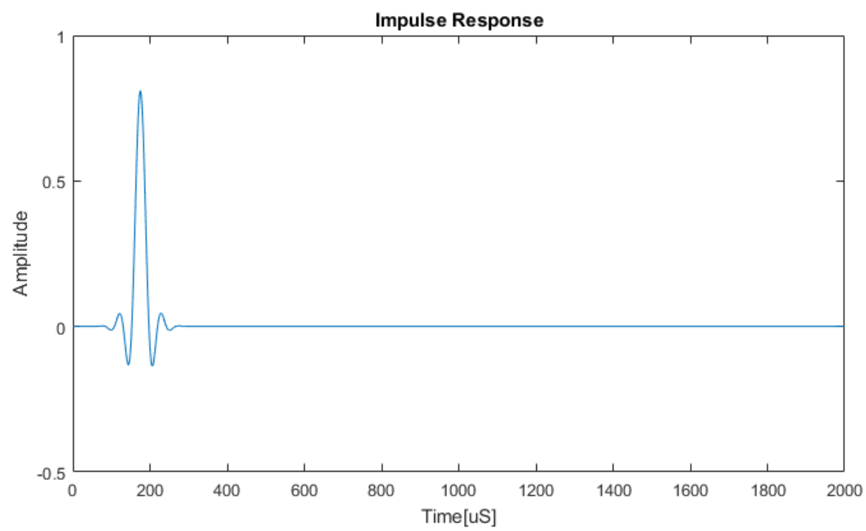
Minimum Phase Fast Roll-off	
Minimum Phase Slow Roll-off	
Minimum Phase Slow Roll-off Low Dispersion	

Table 6 - Frequency response of PCM filters

PCM Filter Impulse Response

The following impulse responses were obtained from software simulations of these filters. Simulation sample rate is 44.1kHz.

Filter	Impulse Response
Minimum Phase	
Linear Phase Apodizing	

Linear Phase Fast Roll-off	
Linear Phase Fast Roll-off Low Ripple	
Linear Phase slow roll-off	

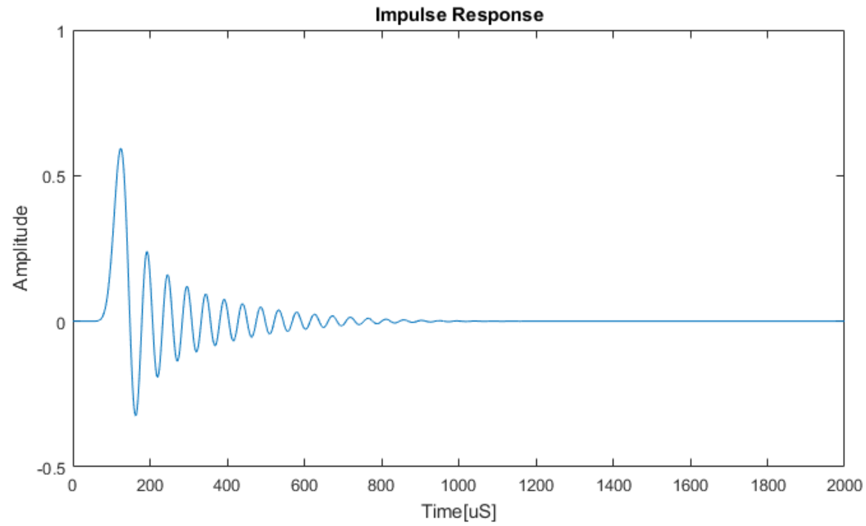
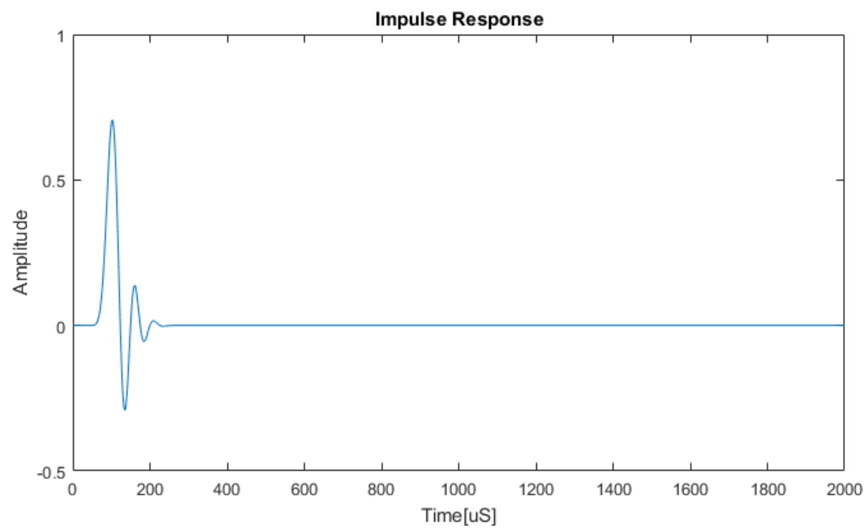
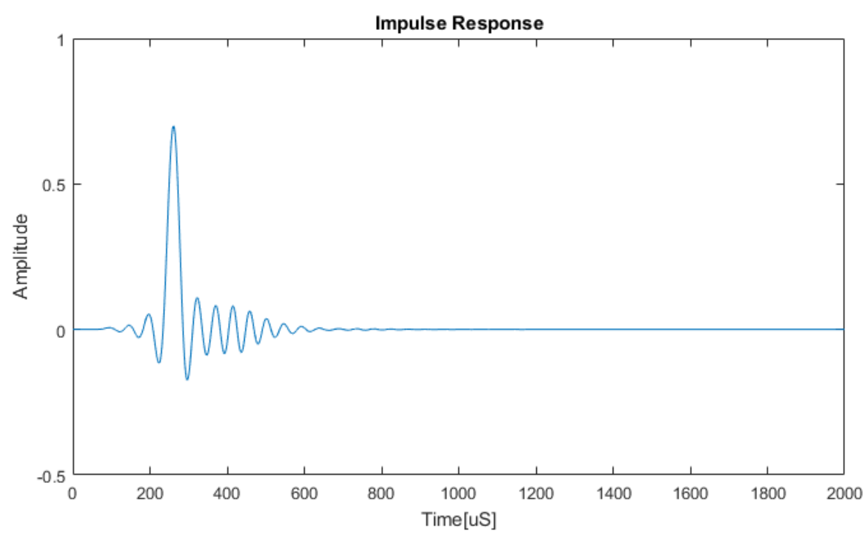
Minimum phase fast roll-off	
Minimum phase slow roll-off	
Minimum phase slow roll-off low dispersion	

Table 7 - Impulse response of PCM filters

Clock Distribution

The ES9033 includes features for selecting and manipulating the input clock source.

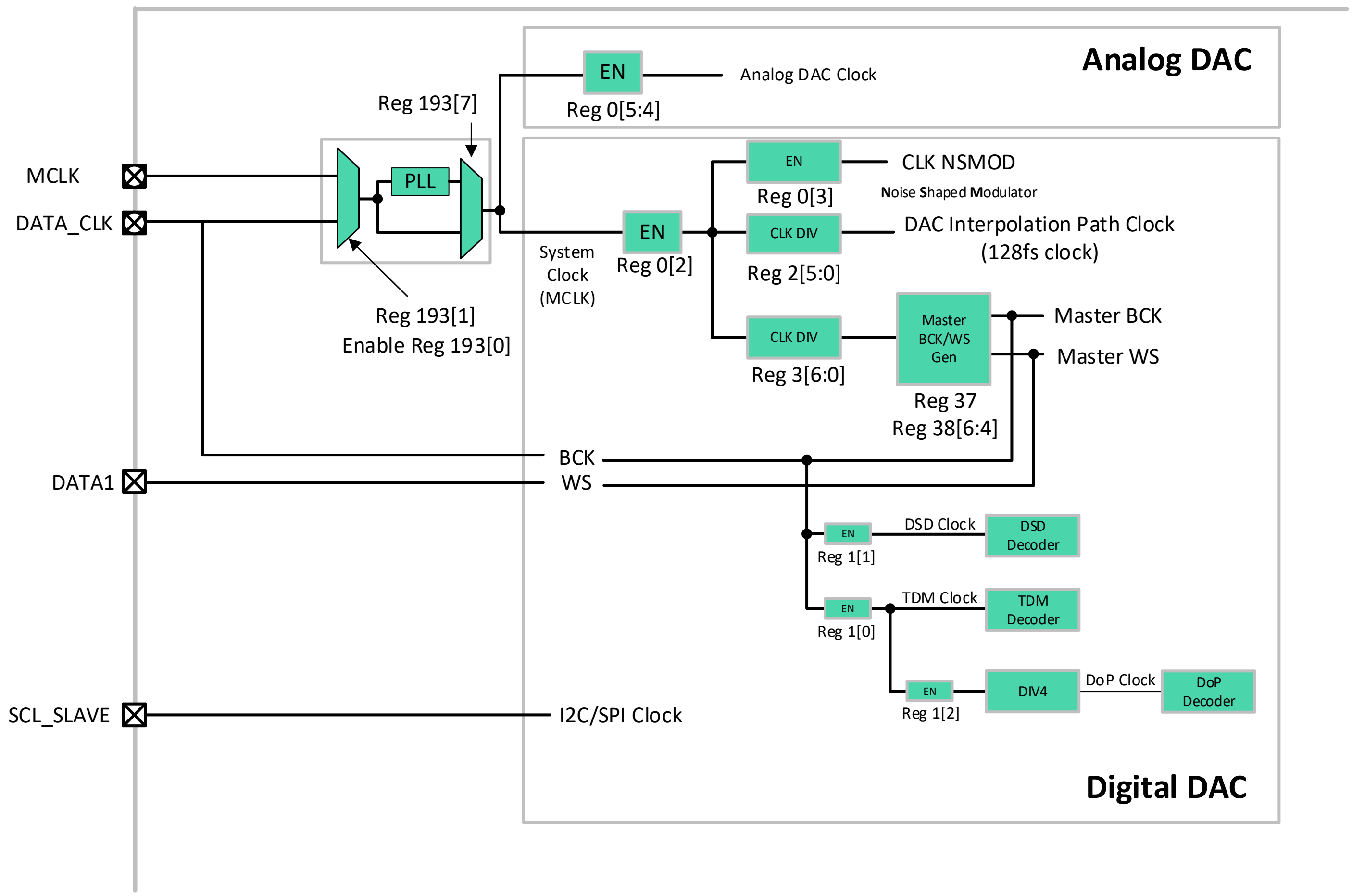


Figure 7 - ES9033 Clock Distribution

The following list shows the various clocks of the ES9033 and the associated registers for configuration.

Analog DAC Clock

- Reg 0[5] (ENABLE_ANALOG_DAC_CH2)
- Reg 0[4] (ENABLE_ANALOG_DAC_CH1)
- Reg 193[7] (PLL_BYP)
- Reg 193[1] (SEL_PLL_IN)
- Reg 193[0] (EN_PLL_CLKIN)

NSMOD Clock

The NSMOD clock is utilized by the HyperStream® II **N**oise **S**haped **MOD**ulators.

- Reg 0[3] (ENABLE_NSMOD)
- Reg 0[2] (ENABLE_DAC)
- Reg 193[7] (PLL_BYP)
- Reg 193[1] (SEL_PLL_IN)
- Reg 193[0] (EN_PLL_CLKIN)

DAC Interpolation Path Clock

- Reg 2[5:0] (SELECT_IDAC_NUM)
- Reg 0[2] (ENABLE_DAC)
- Reg 193[7] (PLL_BYP)
- Reg 193[1] (SEL_PLL_IN)
- Reg 193[0] (EN_PLL_CLKIN)

Master BCK and WS

- Reg 37 (MASTER MODE CONFIG)
- Reg 38[6:4] (MASTER_WS_SCALE)
- Reg 3[6:0] (SELECT_MENC_NUM)
- Reg 0[2] (ENABLE_DAC)
- Reg 193[7] (PLL_BYP)
- Reg 193[1] (SEL_PLL_IN)
- Reg 193[0] (EN_PLL_CLKIN)

DSD Clock

- Reg 1[1] (ENABLE_DSD_DECODE)

TDM Clock

- Reg 1[0] (ENABLE_TDM_DECODE)

DoP Clock

- Reg 1[2] (ENABLE_DOP_DECODE)
- Reg 1[0] (ENABLE_TDM_DECODE)

I2S Master Clock Rate Configurations

WS can be scaled down further than shown via Register 38 [6:4] *MASTER_WS_SCALE*.

MCLK Frequency	WS [kHz]	BCK [MHz]	Bits	Channels	Register 2 [5:0] SELECT_IDAC_NUM		Register 3 [6:0] SELECT_MENC_NUM		Register 40 [4:0] TDM_BIT_WIDTH	
					value	divider	value	divider	value	length
22.579 MHz	44.1	2.822	32	2	5'd3	4	7'd3	4	1'b0	32
	88.2	5.645		2	5'd1	2	7'd1	2	1'b0	32
	176.4	11.290		2	5'd0	1	7'd0	1	1'b0	32
	44.1	1.411	16	2	5'd3	4	7'd3	4	1'b1	16
	88.2	2.822		2	5'd1	2	7'd1	2	1'b1	16
	176.4	5.645		2	5'd0	1	7'd0	1	1'b1	16
24.576 MHz	48	3.072	32	2	5'd3	4	7'd3	4	1'b0	32
	96	6.144		2	5'd1	2	7'd1	2	1'b0	32
	192	12.288		2	5'd0	1	7'd0	1	1'b0	32
	48	1.536	16	2	5'd3	4	7'd3	4	1'b1	16
	96	3.072		2	5'd1	2	7'd1	2	1'b1	16
	192	6.144		2	5'd0	1	7'd0	1	1'b1	16
45.158 MHz	44.1	2.822	32	2	5'd7	8	7'd7	8	1'b0	32
	88.2	5.645		2	5'd3	4	7'd3	4	1'b0	32
	176.4	11.290		2	5'd1	2	7'd1	2	1'b0	32
	352.8	22.579		2	5'd0	1	7'd0	1	1'b0	32
	44.1	1.411	16	2	5'd7	8	7'd7	8	1'b1	16
	88.2	2.822		2	5'd3	4	7'd3	4	1'b1	16
	176.4	5.645		2	5'd1	2	7'd1	2	1'b1	16
	352.8	11.290		2	5'd0	1	7'd0	1	1'b1	16
49.152 MHz	48	3.072	32	2	5'd7	8	7'd7	8	1'b0	32
	96	6.144		2	5'd3	4	7'd3	4	1'b0	32
	192	12.288		2	5'd1	2	7'd1	2	1'b0	32
	384	24.576		2	5'd0	1	7'd0	1	1'b0	32
	48	1.536	16	2	5'd7	8	7'd7	8	1'b1	16
	96	3.072		2	5'd3	4	7'd3	4	1'b1	16
	192	6.144		2	5'd1	2	7'd1	2	1'b1	16
	384	12.288		2	5'd0	1	7'd0	1	1'b1	16

Table 8 - I2S Master Clock Rate Configurations

I2S Slave Clock Rate Configurations

MCLK Frequency	WS [kHz]	BCK	Channels	Register 2 [5:0] SELECT_IDAC_NUM		Register 0 [6] ENABLE_2X_MODE	
				value	divider	value	multiplier
22.579 MHz	44.1	64FS	2	7'd3	4	1'b0	1x
	88.2		2	7'd1	2	1'b0	1x
	176.4		2	7'd0	1	1'b0	1x
	352.8		2	7'd0	1	1'b1	2x
24.576 MHz	48		2	7'd3	4	1'b0	1x
	96		2	7'd1	2	1'b0	1x
	192		2	7'd0	1	1'b0	1x
	384		2	7'd0	1	1'b1	2x
45.158 MHz	44.1		2	7'd7	8	1'b0	1x
	88.2		2	7'd3	4	1'b0	1x
	176.4		2	7'd1	2	1'b0	1x
	352.8		2	7'd0	1	1'b0	1x
49.152 MHz	48		2	7'd7	8	1'b0	1x
	96		2	7'd3	4	1'b0	1x
	192		2	7'd1	2	1'b0	1x
	384		2	7'd0	1	1'b0	1x

Table 9 - I2S Slave Clock Rate Configurations

TDM Slave Clock Rate Configurations

All configurations are 32-bit.

MCLK Frequency	WS [kHz]	BCK [MHz]	TDM Mode	Chan-nels	Register 2 [5:0] SELECT_IDAC_NUM	
					value	divider
22.579 MHz	44.1	5.645	TDM 128	4	5'd3	4
	88.2	11.290		4	5'd1	2
	176.4	22.579		4	5'd0	1
	44.1	11.290	TDM 256	8	5'd3	4
	88.2	22.579		8	5'd1	2
	44.1	22.579	TDM 512	16	5'd3	4
24.576 MHz	48	6.144	TDM 128	4	5'd3	4
	96	12.288		4	5'd1	2
	192	24.576		4	5'd0	1
	48	12.288	TDM 256	8	5'd3	4
	96	24.576		8	5'd1	2
	48	24.576	TDM 512	16	5'd3	4
45.158 MHz	44.1	5.645	TDM 128	4	5'd7	8
	88.2	11.290		4	5'd3	4
	176.4	22.579		4	5'd1	2
	44.1	11.290	TDM 256	8	5'd7	8
	88.2	22.579		8	5'd3	4
	44.1	22.579	TDM 512	16	5'd7	8
49.152 MHz	48	6.144	TDM 128	4	5'd7	8
	96	12.288		4	5'd3	4
	192	24.576		4	5'd1	2
	48	12.288	TDM 256	8	5'd7	8
	96	24.576		8	5'd3	4
	48	24.576	TDM 512	16	5'd7	8

Table 10 - TDM Slave Clock Rate Configurations

TDM Master Clock Rate Configurations

When using left justified mode (Register 10) remember to enable Reg 33 – sync positive edge of frame to correct for phase differences.

MCLK Frequency	WS [kHz]	BCK [MHz]	TDM Mode	Chan-nels	Register 2 [5:0] SELECT_IDAC_NUM		Register 3 [6:0] SELECT_MENC_NUM		Register 38 [6:4] MASTER_WS_SCALE		Register 37 [6] MASTER_BCK_DIV1	
					value	divider	value	divider	value	divider	value	divider
22.579 MHz	44.1	5.645	TDM 128	4	5'd3	4	7'd1	2	3'd1	2	1'b0	2
	88.2	11.290		4	5'd1	2	7'd0	1	3'd1	2	1'b0	2
	176.4	22.579		4	5'd0	1	7'd0	1	3'd0	1	1'b1	1
	44.1	11.290	TDM 256	8	5'd3	4	7'd0	1	3'd2	4	1'b0	2
	88.2	22.579		8	5'd1	2	7'd0	1	3'd1	2	1'b1	1
	44.1	22.579	TDM 512	16	5'd3	4	7'd0	1	3'd2	4	1'b1	1
24.576 MHz	48	6.144	TDM 128	4	5'd3	4	7'd1	2	3'd1	2	1'b0	2
	96	12.288		4	5'd1	2	7'd0	1	3'd1	2	1'b0	2
	192	24.576		4	5'd0	1	7'd0	1	3'd0	1	1'b1	1
	48	12.288	TDM 256	8	5'd3	4	7'd0	1	3'd2	4	1'b0	2
	96	24.576		8	5'd1	2	7'd0	1	3'd1	2	1'b1	1
	48	24.576	TDM 512	16	5'd3	4	7'd0	1	3'd2	4	1'b1	1
45.158 MHz	44.1	5.645	TDM 128	4	5'd7	8	7'd3	4	3'd1	2	1'b0	2
	88.2	11.290		4	5'd3	4	7'd1	2	3'd1	2	1'b0	2
	176.4	22.579		4	5'd1	2	7'd0	1	3'd1	2	1'b0	2
	44.1	11.290	TDM 256	8	5'd7	8	7'd1	2	3'd2	4	1'b0	2
	88.2	22.579		8	5'd3	4	7'd0	1	3'd2	4	1'b0	2
	44.1	22.579	TDM 512	16	5'd7	8	7'd0	1	3'd3	8	1'b0	2
49.152 MHz	48	6.144	TDM 128	4	5'd7	8	7'd3	4	3'd1	2	1'b0	2
	96	12.288		4	5'd3	4	7'd1	2	3'd1	2	1'b0	2
	192	24.576		4	5'd1	2	7'd0	1	3'd1	2	1'b0	2
	48	12.288	TDM 256	8	5'd7	8	7'd1	2	3'd2	4	1'b0	2
	96	24.576		8	5'd3	4	7'd0	1	3'd2	4	1'b0	2
	48	24.576	TDM 512	16	5'd7	8	7'd0	1	3'd3	8	1'b0	2

Table 11 - TDM Master Clock Rate Configurations

Audio Interface Timing

Audio data on DATA1-2 are sampled at the rising edges of DATA_CLK and must satisfy the setup and hold time requirements relative to the rising edge of DATA_CLK.

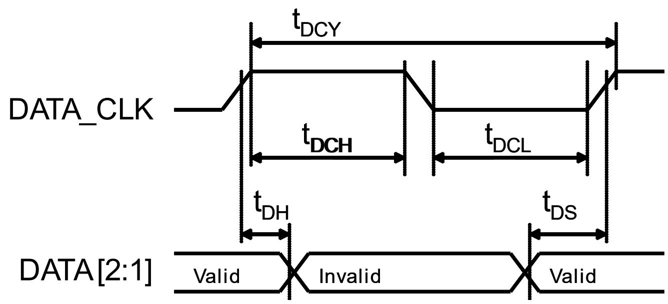


Figure 8 - Audio interface timing

Parameter	Symbol	Min	Max	Unit
DATA_CLK pulse width high	t_{DCH}	9.0		ns
DATA_CLK pulse width low	t_{DCL}	9.0		ns
DATA_CLK cycle time	t_{DCY}	20		ns
DATA_CLK duty cycle		45:55	55:45	
DATAx set-up time to DATA_CLK rising edge	t_{DS}	4.1		ns
DATAx hold time to DATA_CLK rising edge	t_{DH}	2.0		ns

Table 9 - Audio interface timing definitions

Analog Features

APLL

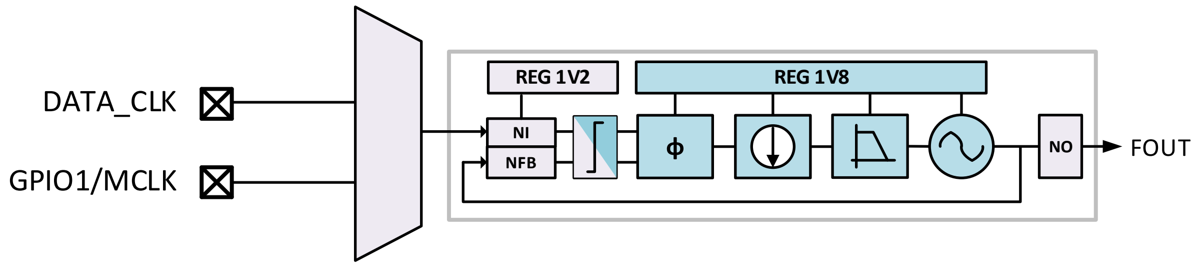


Figure 9 - Functional Block Diagram of ES9033 APLL

The ES9033 has a built in Analog PLL (APLL) for generating frequencies that are unavailable externally.

For calculation of the PLL frequency output, use the following formula:

$$Fout = \left(\frac{FIN}{NI}\right) * \frac{NFB}{NO}$$

$$NFB = \frac{(2^{25})}{FBDIV}$$

Where:

a. FBDIV is a 24-bit number
b. Fvco = Fout * NO, where Fvco must be between 90MHz and 100MHz
c. NI = input dividing ratio,
    - Accessible from Reg 202-200[9:1], **PLL_CLK_IN_DIV**
d. NO = output dividing ratio
    - Accessible from Reg 202-200[13:10], **PLL_CLK_OUT_DIV**
e. NFB = feedback dividing ratio,
    - Accessible from Reg 199-197[23:0], **PLL_CLK_FB_DIV**

PLL Registers

- NI – Register 200-202[9:1] PLL_CLK_IN_DIV
- NO – Register 200-202[13:10] PLL_CLK_OUT_DIV
- FBDIV – Register 197-199[23:0] PLL_CLK_FB_DIV

Absolute Maximum Ratings

PARAMETER	RATING
Positive Supply Voltage • AVCC_3V3 • AVCC_CP • VCCA • AVDD • DVDD	 • +3.7V with respect to Ground • +3.7V with respect to Ground • +3.7V with respect to Ground • +3.7V with respect to Ground • +1.4V with respect to Ground
Storage temperature	–65°C to +150°C
Operating Junction Temperature	+125°C
Voltage range for digital input pins	–0.3V to AVDD(nom)+0.3V
ESD Protection Human Body Model (HBM) Charge Device Model (CDM)	 2kV 500V

Table 12 - Absolute maximum ratings

WARNING: Stresses beyond those listed under here may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied.

WARNING: Electrostatic Discharge (ESD) can damage this device. Proper procedures must be followed to avoid ESD when handling this device.

IO Electrical Characteristics

PARAMETER	SYMBOL	MINIMUM	MAXIMUM	UNIT	COMMENTS
High-level input voltage	VIH	(AVDD / 2) + 0.4		V	
Low-level input voltage	VIL		0.4	V	
High-level output voltage	VOH	AVDD – 0.2		V	IOH = ((AVDD / 2) +1.4) mA
Low-level output voltage	VOL		0.2	V	IOL = ((AVDD / 2) + 1.7) mA

Table 13 - IO electrical characteristics

Recommended Operating Conditions

These are the recommended operating conditions for the ES9033:

PARAMETER	SYMBOL	CONDITIONS
Operating temperature	T_A	–20°C to +85°C
DVDD		Internally Generated
AVDD		3.3V
VCCA		3.3V
AVCC		Internally Generated
AVCC_CP		3.3V
AVCC_3V3		3.3V

Table 14 - Recommended operating conditions

Power Consumption

Power numbers are given when the device is in slave mode.

Test Conditions 1 (unless otherwise noted)

T_A = 25ºC, AVCC_3V3 = AVCC_CP = VCCA = AVDD = **+3.3V**, fs = **48kHz**, **MCLK = 49.152MHz**, I2S 2Vrms 1kHz sine full scale

Parameter		*Min*	*Typ*	*Max*	*Unit*
Hardware Mode: 3					
AVCC_3V3			11.4		mA
AVCC_CP			7.2		mA
VCCA			0.3		mA
AVDD			11.2		mA
Standby (CHIP_EN = 0V)					
AVCC			<1		uA
AVDD			<1		uA

Table 15 - Power consumption with test conditions 1

Test Conditions 2 (unless otherwise noted)

T_A = 25ºC, AVCC_3V3 = AVCC_CP = VCCA = AVDD = **+3.3V**, fs = **48kHz**, **MCLK = 49.152MHz**, I2S streaming zeros

Parameter		*Min*	*Typ*	*Max*	*Unit*
Hardware Mode: 3					
AVCC_3V3			<1		uA
AVCC_CP			0.5		mA
VCCA			0.3		mA
AVDD			9.8		mA
Standby (CHIP_EN = 0V)					
AVCC			***<1***		uA
AVDD			***<1***		uA

Table 16 - Power consumption with test conditions 2

Test Conditions 3 (unless otherwise noted)

T_A = 25ºC, AVCC_3V3 = AVCC_CP = VCCA = AVDD = **+3.3V**, fs = **192kHz**, **MCLK = 24.576MHz**, I2S 2Vrms 1kHz sine full scale

Parameter		*Min*	*Typ*	*Max*	*Unit*
Hardware Mode: 8					
AVCC_3V3			10.4		mA
AVCC_CP			7.0		mA
VCCA			0.2		mA
AVDD			10.4		mA
Standby (CHIP_EN = 0V)					
AVCC			***<1***		uA
AVDD			***<1***		uA

Table 17 - Power consumption with test conditions 3

Performance

Test Conditions 1 (unless otherwise noted)

T_A = 25ºC, AVDD = AVCC_CP = AVCC_3V3 = VCCA = +3.3V, **fs = 48kHz**, **MCLK = 49.152MHz**, 1kHz tone

Parameter			Min	Typ	Max	Unit
Resolution				32		Bit
THD+N Ratio @ fs=48kHz, BW=20Hz-20kHz				-108	-105	dB
DNR A-weighted (w/ DRE)	-60dBFS		120	122		dB
DNR A-weighted (w/o DRE)	-60dBFS		112	115		dB
Interchannel Mismatch				±0.02	±0.05	dB
Output Amplitude	0dBFS			2.1		Vrms

Table 18 - Performance data

Recommended Power-Up Sequence

The recommended power-up sequence is shown in the following diagram.

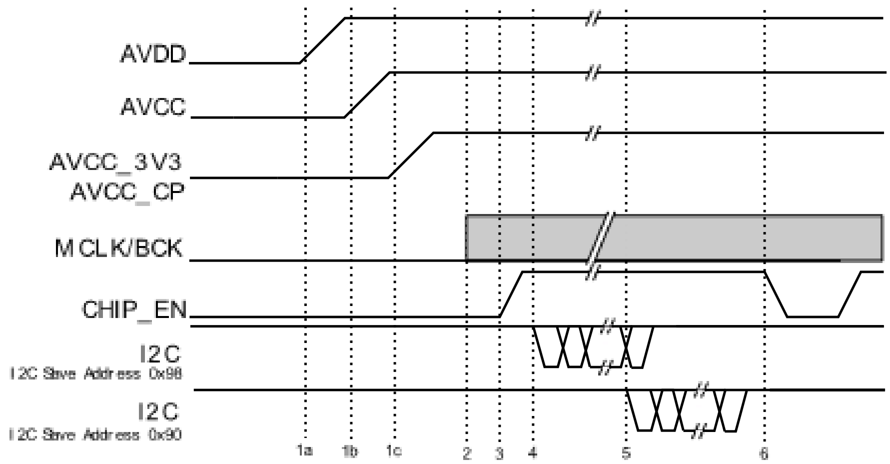


Figure 10 - Recommended power-up sequence

1. Supplies:
   a. AVDD
   b. AVCC
   c. AVCC_3V3, AVCC_CP
2. Enable MCLK
3. Set CHIP_EN high after MCLK is stable
4. Configure the clock setup through I2C address 0x98
   a. Must wait 100ms after CHIP_EN is set HIGH
5. I2C address 0x90 can be written/read after clock setup has been established
6. Any reset operation must keep CHIP_EN low for at least 20ns

Recommended Power-Down Sequence

The recommended power-down sequence is shown in the following diagram.

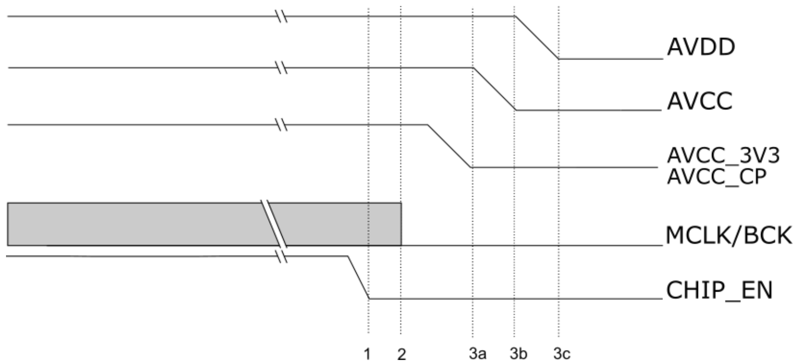


Figure 11 - Recommended power-down sequence

1. Set CHIP_EN to 0V
2. Disable MCLK
3. Supplies
    a. AVCC_3V3, AVCC_CP
    b. AVCC
    c. AVDD

Register Overview

I²C Slave Interface (Device Address 0x90, 0x92, 0x94, 0x96)

This interface contains Read/Write and Read-only registers. A system clock must be present.

Multi-byte registers must be written from LSB to MSB. Data is latched when MSB is written.
Multi-byte registers must be read from LSB to MSB. Data is latched when LSB is read.
MSB is always stored in the highest register address.

Read/Write Register Addresses

Registers 0–88 (0x00 – 0x58) are read/write registers

Read-only Register Addresses

Registers 224 – 241 (0xE0 – 0xF1) are read only registers.

I²C Synchronous Slave Interface (Device Address 0x98, 0x9A, 0x9C, 0x9E)

This interface contains Write-only registers. These registers can be written even when there is no system clock present.

When the device is inactive, all peripherals are automatically disabled and all clocks are stopped. A reset can wake the ES9033.

Write-only Register Addresses.

Registers 192 – 203 (0xC0 – 0xCB) are write only registers.

Multi-Byte Registers

Multi-byte registers must be written from LSB to MSB. Data is latched when MSB is written.
MSB is always stored in the highest register address.

I²C Slave/Synchronous Slave Interface Timing

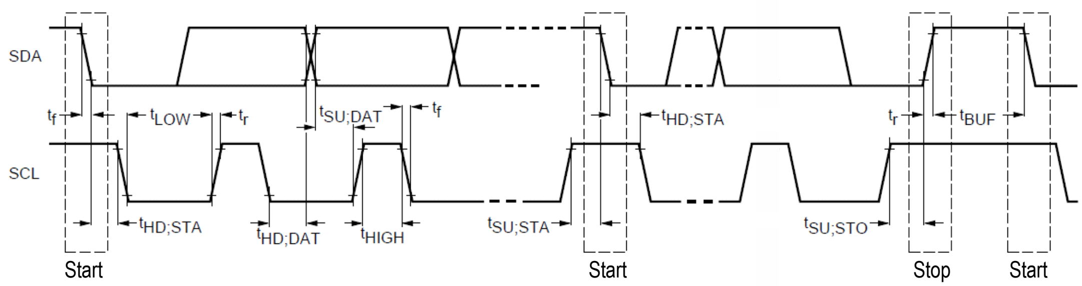


Figure 12 - I2C Slave Control Interface Timing

Parameter	Symbol	CLK Constraint	Standard-Mode		Fast-Mode		Unit
			MIN	MAX	MIN	MAX	
SCL Clock Frequency	f_{SCL}	< CLK/20	0	100	0	400	kHz
START condition hold time	$t_{HD;STA}$		4.0	-	0.6	-	µs
LOW period of SCL	t_{LOW}	>10/CLK	4.7	-	1.3	-	µs
HIGH period of SCL (>10/CLK)	t_{HIGH}	>10/CLK	4.0	-	0.6	-	µs
START condition setup time (repeat)	$t_{SU;STA}$		4.7	-	0.6	-	µs
SDA hold time from SCL falling - All except NACK read - NACK read only	$t_{HD;DAT}$		0 2/CLK	-	0 2/CLK	-	µs s
SDA setup time from SCL rising	$t_{SU;DAT}$		250	-	100	-	ns
Rise time of SDA and SCL	t_r		-	1000		300	ns
Fall time of SDA and SCL	t_f		-	300		300	ns
STOP condition setup time	$t_{SU;STO}$		4	-	0.6	-	µs
Bus free time between transmissions	t_{BUF}		4.7	-	1.3	-	µs
Capacitive load for each bus line	C_b		-	400	-	400	pF

Table 19 - I2C slave/synchronous slave interface timing definitions

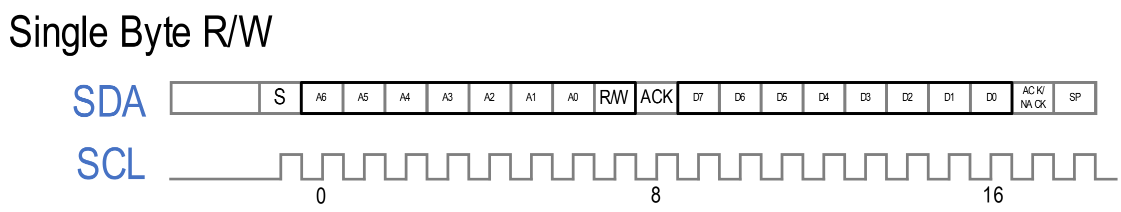


Figure 13 - I2C single byte R/W

SPI Slave Interface

The SPI slave interface is used when the MODE pin (pin 3) is pulled high.

- The SPI Slave interface can be accessed using the Pins 25-28
    - Pin 22 MOSI
    - Pin 21 SCLK
    - Pin 19 SS
    - Pin 20 MISO

The 4-wire SPI data format is: Command (1 byte) + Address (1 byte) + Data

SPI commands

- 0x01: Read
- 0x03: Write
- 0x07: Write-only Register Addresses 192-194 (0xC0 – 0xC2)

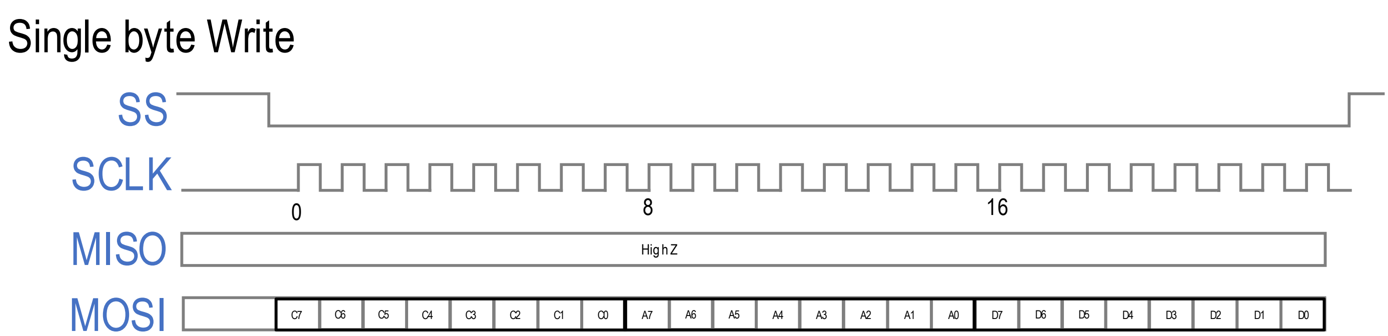


Figure 14 - SPI single byte write

Single byte Read

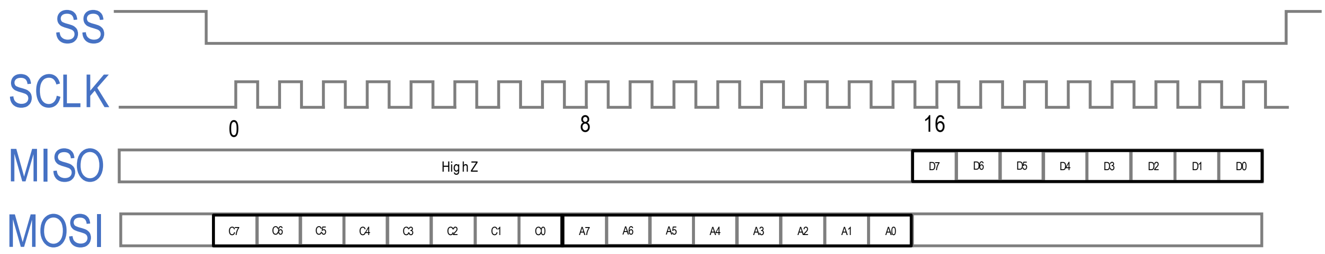


Figure 15 - SPI single byte Read

Multi-byte Read

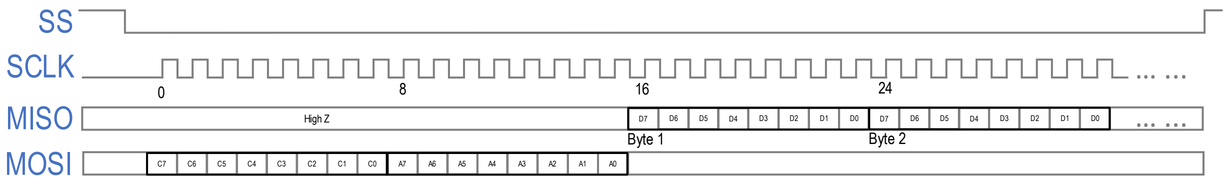


Figure 16 - SPI multi-byte read

Register Map

Addr (Hex)	Addr (Dec)	Register	7	6	5	4	3	2	1	0
0x0	0	SYSTEM CONFIG	SOFT_RESET	ENABLE_2X_MODE	ENABLE_ANALOG_DAC_CH2	ENABLE_ANALOG_DAC_CH1	ENABLE_NSMOD	ENABLE_DAC	AMP_MODE_REG	RESERVED
0x1	1	SYS MODE CONFIG	RESERVED					ENABLE_DOP_DECODE	ENABLE_DSD_DECODE	ENABLE_TDM_DECODE
0x2	2	DAC CLOCK CONFIG	RESERVED	SELECT_IDAC_HALF	SELECT_IDAC_NUM					
0x3	3	MASTER CLOCK CONFIG	SELECT_MENC_HALF	SELECT_MENC_NUM						
0x4	4	CP CLOCK DIV	CP_CLK_DIV							
0x5	5	RESERVED	RESERVED							
0x6	6	RESERVED	RESERVED							
0x7	7	RESERVED	RESERVED							
0x8	8	RESERVED	RESERVED							
0x9	9	INTERRUPT MASK P	SOFT_RAMP_CH2_MASKP	SOFT_RAMP_CH1_MASKP	DRE_FLAG_CH2_MASKP	DRE_FLAG_CH1_MASKP	AUTOMUTE_FLAG_CH2_MASKP	AUTOMUTE_FLAG_CH1_MASKP	VOL_MIN_CH2_MASKP	VOL_MIN_CH1_MASKP
0xA	10	INTERRUPT MASK P	INPUT_DATA_TYPE_MASKP		TDM_DATA_VALID_FLAG_MASKP	CLK_AVALID_FLAG_MASKP	RWS_REFERENCE_COUNTER_FULL_FLAG_MASKP	BCK_WS_FAILED_FLAG_MASKP	RESERVED	DOP_VALID_MASKP
0xB	11	INTERRUPT MASK N	SOFT_RAMP_CH2_MASKN	SOFT_RAMP_CH1_MASKN	DRE_FLAG_CH2_MASKN	DRE_FLAG_CH1_MASKN	AUTOMUTE_FLAG_CH2_MASKN	AUTOMUTE_FLAG_CH1_MASKN	VOL_MIN_CH2_MASKN	VOL_MIN_CH1_MASKN
0xC	12	INTERRUPT MASK N	INPUT_DATA_TYPE_MASKN		TDM_DATA_VALID_FLAG_MASKN	CLK_AVALID_FLAG_MASKN	RWS_REFERENCE_COUNTER_FULL_FLAG_MASKN	BCK_WS_FAILED_FLAG_MASKN	RESERVED	DOP_VALID_MASKN
0xD	13	INTERRUPT CLEAR	SOFT_RAMP_CH2_CLEAR	SOFT_RAMP_CH1_CLEAR	DRE_FLAG_CH2_CLEAR	DRE_FLAG_CH1_CLEAR	AUTOMUTE_FLAG_CH2_CLEAR	AUTOMUTE_FLAG_CH1_CLEAR	VOL_MIN_CH2_CLEAR	VOL_MIN_CH1_CLEAR
0xE	14	INTERRUPT CLEAR	INPUT_DATA_CLEAR		TDM_DATA_VALID_CLEAR	CLK_AVALID_FLAG_CLEAR	RWS_REFERENCE_COUNTER_FULL_FLAG_CLEAR	BCK_WS_FAILED_FLAG_CLEAR	RESERVED	DOP_VALID_CLEAR
0xF	15	ANALOG CTRL CONFIG	RESERVED	AMP_PDB_ON_SS	AMP_PDB_CLK_INVALID	RESERVED			LP_DAC_REG	EN_FCB
0x10	16	LDRV CTRL	ENB_OCP_LDRV_CH2	ENB_OCP_LDRV_CH1	RESERVED					
0x11	17	RESERVED	RESERVED							
0x12	18	RESERVED	RESERVED							
0x13	19	ANALOG CONTROL OVERRIDE2	TRIB_DAC_CH2	TRIB_DAC_CH1	RESERVED					
0x14	20	RESERVED	RESERVED							
0x15	21	RESERVED	RESERVED							
0x16	22	RESERVED	RESERVED							
0x17	23	RESERVED	RESERVED							
0x18	24	GPIO CONFIG	INVERT_GPIO1	GPIO1_WK_EN	GPIO1_SDB	GPIO1_OE	GPIO1_CFG			
0x19	25	GPIO CONFIG2	GPIO_OR_SS_RAMP	GPIO_OR_VOL_MIN	GPIO_OR_AUTOMUTE	GPIO_AND_SS_RAMP	GPIO_AND_VOL_MIN	GPIO_AND_AUTOMUTE	RESERVED	GPIO1_READ
0x1A	26	GPIO INPUT ENABLE	RESERVED						GPIO_AMP_MODE	GPIO_SEL
0x1B	27	PWM1 COUNT	PWM1_COUNT							
0x1C	28	PWM1 FREQUENCY	PWM1_FREQ							
0x1D	29	PWM1 FREQUENCY	PWM1_FREQ							
0x1E	30	PWM2 COUNT	PWM2_COUNT							
0x1F	31	PWM2 FREQUENCY	PWM2_FREQ							
0x20	32	PWM2 FREQUENCY	PWM2_FREQ							
0x21	33	PWM3 COUNT	PWM3_COUNT							
0x22	34	PWM3 FREQUENCY	PWM3_FREQ							
0x23	35	PWM3 FREQUENCY	PWM3_FREQ							
0x24	36	INPUT CONFIG	AUTO_FS_DETECT	DSD_NEGEDGE	DSD_MASTER_MODE	ENABLE_TDM_MASTER_MODE	ENABLE_PDM	INPUT_SEL		AUTO_INPUT_SELECT
0x25	37	MASTER MODE CONFIG	AUTO_FS_DETECT_BLOCK_2XMODE	MASTER_BCK_DIV1	MASTER_WS_IDLE	MASTER_FRAME_LENGTH		MASTER_WS_PULSE_MODE	MASTER_WS_INVERT	MASTER_BCK_INVERT
0x26	38	TDM CONFIG1	TDM_RESYNC	MASTER_WS_SCALE			TDM_CH_NUM			
0x27	39	TDM CONFIG2	TDM_LJ_MODE	TDM_VALID_EDGE	TDM_VALID_PULSE_LEN					
0x28	40	TDM CONFIG3	PDM_NEG_FIRST	TDM_BIT_WIDTH		TDM_DATA_LATCH_ADJ				

0x29	41	RESERVED	RESERVED							
0x2A	42	TDM SLOT CONFIG	TDM_CH2_SLOT_SEL				TDM_CH1_SLOT_SEL			
0x2B	43	RESERVED	RESERVED							
0x2C	44	RESYNC CONFIG	RESERVED	CP_PDB_ON_MUTE	RESERVED					
0x2D	45	DSD 2DB DOWN	DSD_2DB_DOWN	RESERVED						
0x2E	46	VOLUME1	VOLUME1							
0x2F	47	VOLUME2	VOLUME2							
0x30	48	DAC VOL UP RATE	DAC_VOL_RATE_UP							
0x31	49	DAC VOL DOWN RATE	DAC_VOL_RATE_DOWN							
0x32	50	DAC VOL DOWN RATE FAST	DAC_VOL_RATE_FAST							
0x33	51	MUTE CTRL	FORCE_VOLUME	DAC_USE_MONO_VOLUME	RUN_VOLUME	RESERVED	DAC_INVERT_CH2	DAC_INVERT_CH1	DAC_MUTE_CH2	DAC_MUTE_CH1
0x34	52	FILTER CONFIG	AUTO_CH_DETECT	BYPASS_DEEMPH	PEAK_FILTER	SEL_DEEMPH		FILTER_SHAPE		
0x35	53	RESERVED	RESERVED							
0x36	54	DATAPATH CONTROL	RESERVED						BYPASS_FIR 4X	BYPASS_FIR 2X
0x37	55	THD COMP C2 CH1	THD_C2_CH1							
0x38	56	THD COMP C2 CH1	THD_C2_CH1							
0x39	57	THD COMP C3 CH1	THD_C3_CH1							
0x3A	58	THD COMP C3 CH1	THD_C3_CH1							
0x3B	59	THD COMP C2 CH2	THD_C2_CH2							
0x3C	60	THD COMP C2 CH2	THD_C2_CH2							
0x3D	61	THD COMP C3 CH2	THD_C3_CH2							
0x3E	62	THD COMP C3 CH2	THD_C3_CH2							
0x3F	63	AUTOMUTE TIME	AUTOMUTE_TIME							
0x40	64	AUTOMUTE TIME	AUTOMUTE_RAMP_TO_GROUND	AUTOMUTE_WAIT_ON_DRE	RESERVED	AUTOMUTE_EN_CH2	AUTOMUTE_EN_CH1	AUTOMUTE_TIME		
0x41	65	AUTOMUTE LEVEL	AUTOMUTE_LEVEL							
0x42	66	AUTOMUTE LEVEL	AUTOMUTE_LEVEL							
0x43	67	AUTOMUTE OFF LEVEL	AUTOMUTE_OFF_LEVEL							
0x44	68	AUTOMUTE OFF LEVEL	AUTOMUTE_OFF_LEVEL							
0x45	69	SOFT RAMP CONFIG	GAIN_18DB_CH2	GAIN_18DB_CH1	SOFT_RAMP_TYPE	SOFT_RAMP_TIME				
0x46	70	RESERVED	RESERVED							
0x47	71	RESERVED	RESERVED							
0x48	72	RESERVED	RESERVED							
0x49	73	DRE FORCE	DRE_FORCE_CH2	DRE_FORCE_CH1	RESERVED					
0x4A	74	DRE GAIN CH1	DRE_GAIN1							
0x4B	75	DRE GAIN CH1	DRE_GAIN1							
0x4C	76	DRE GAIN CH2	DRE_GAIN2							
0x4D	77	DRE GAIN CH2	DRE_GAIN2							
0x4E	78	DRE ON THRESHOLD	DRE_ON_THRESH							
0x4F	79	DRE ON THRESHOLD	DRE_ON_THRESH							
0x50	80	DRE OFF THRESHOLD	DRE_OFF_THRESH							
0x51	81	DRE OFF THRESHOLD	DRE_OFF_THRESH							
0x52	82	DRE DECAY RATE	DRE_FORCE_LEVEL	RESERVED	MIN_PEAK	DRE_DECAY_RATE				
0x53	83	DC OFFSET CH1	DC_OFFSET1							
0x54	84	DC OFFSET CH1	DC_OFFSET1							
0x55	85	DC OFFSET CH2	DC_OFFSET2							
0x56	86	DC OFFSET CH2	DC_OFFSET2							
0x57	87	DC RAMP RATE	DC_RAMP_RATE							
0x58	88	MASTER TRIM	MASTER_TRIM							
0xC0	192	RESET & PLL REGISTER1	AO_SOFT_RESET	PLL_SOFT_RESET	PLL_VCO_CMP_ISET			RESERVED	GPIO1_SDB_AO	PLL_CLKHV_PHASE
0xC1	193	PLL REGISTER2	PLL_BYP	DVDD_SHUNTB	SEL_1V_DREG	PLL_HVREG_VREF_SEL			SEL_PLL_IN	EN_PLL_CLKIN
0xC2	194	PLL REGISTER3	RESERVED				RESERVED	AUTO_LOCK_EN	VREF_HOLD_REG	VREF_HOLD_ENABLE
0xC3	195	PLL REGISTER4	PLL_CP_BIAS_SEL			PLL_PFD_DELAY_SEL		PLL_VCO_FLIMIT_PD	PLL_VCO_PDB	PLL_CP_PDB
0xC4	196	PLL REGISTER5	PLL_VCO_BAND_CTRL			PLL_VCO_KVCO_CTRL			PLL_VCO_IB_AMP_CTRL	
0xC5	197	PLL REGISTER6	PLL_CLK_FB_DIV							
0xC6	198	PLL REGISTER6	PLL_CLK_FB_DIV							
0xC7	199	PLL REGISTER6	PLL_CLK_FB_DIV							
0xC8	200	PLL REGISTER7	PLL_FB_DIV_LOAD PLL_FB_DIV_LOAD							
0xC9	201	PLL REGISTER7	PLL_CLK_OUT_DIV_PHASE		PLL_CLK_OUT_DIV				PLL_CLK_IN_DIV	
0xCA	202	PLL REGISTER7	PLL_REG_PDB_HV	PLL_REG_PDB_1V2	PLL_REG_BYP_HV	PLL_REG_BYP_1V2	PLL_LOW_BW	PLL_CLK_OUT_DIV_PHASE_EN	PLL_CLK_OUT_DIV_PHASE	
0xCB	203	PLL REGISTER8	PLL_VCO_FLIMIT_CTRL		PLL_DIG_RSTB	PLL_VCO_DIODE_EN	RESERVED			
0xE0	224	SYS READ	RESERVED			MODES		ADDR1	ADDR0	RESERVED

0xE1	225	CHIP ID READ	CHIP_ID							
0xE2	226	RESERVED	RESERVED							
0xE3	227	RESERVED	RESERVED							
0xE4	228	RESERVED	RESERVED							
0xE5	229	INTERRUPT STATE	SS_FULL_RAMP_INTSTATE		DRE_SELECT2_INTSTATE	DRE_SELECT1_INTSTATE	AUTOMUTE_INTSTATE		VOL_MIN_INTSTATE	
0xE6	230	INTERRUPT STATE	INPUT_SELECT_OVERRIDE_INTSTATE		TDM_DATA_VALID_INTSTATE	CLK_AVALID_INT_INTSTATE	RWS_REF_CNT_FULL_INTSTATE	BCK_WS_FAIL_INTSTATE	PLL_LOCKED_R_INTSTATE	DOP_VALID_INTSTATE
0xE7	231	INTERRUPT SOURCE	SS_FULL_RAMP_INTSOURCE		DRE_SELECT2_INTSOURCE	DRE_SELECT1_INTSOURCE	AUTOMUTE_INTSOURCE		VOL_MIN_INTSOURCE	
0xE8	232	INTERRUPT SOURCE	INPUT_SELECT_OVERRIDE_INTSOURCE		TDM_DATA_VALID_INTSOURCE	CLK_AVALID_INT_INTSOURCE	RWS_REF_CNT_FULL_INTSOURCE	BCK_WS_FAIL_INTSOURCE	PLL_LOCKED_R_INTSOURCE	DOP_VALID_INTSOURCE
0xE9-0xEE	233-238	RESERVED	RESERVED							
0xEF	239	AUTO TUNING READ	RATIO_VALID	IDAC_DIV_HALF_REG	IDAC_DIV_REG					
0xF0	240	GPIO READ	RESERVED							GPIO1_I_READ
0xF1	241	DAC STATUS READ	SS_RAMP_DOWN_CH2	SS_RAMP_DOWN_CH1	SS_RAMP_UP_CH2	SS_RAMP_UP_CH1	AUTOMUTE_CH2	AUTOMUTE_CH1	VOL_MIN_CH2	VOL_MIN_CH1
0xF2	242	DRE STATUS READ	TDM_DATA_VALID	DOP_VALID	RESERVED		DRE_DETECT_CH2	DRE_DETECT_CH1	DRE_SELECT_CH2	DRE_SELECT_CH1

Table 20 – Register map

Register Listings

System Registers

Register 0: SYSTEM CONFIG

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b1	1'b1	1'b1	1'b1	1'b0	1'b0

Bits	Mnemonic	Description
[7]	SOFT_RESET	Performs soft reset to digital core except for the PLL Registers
6]	ENABLE_2X_MODE	Enables 2x mode for 768k sample rate. • 1'b0: 2x mode disabled (default) • 1'b1: 2x mode enabled
[5]	ENABLE_ANALOG_DAC_CH2	Enables ch2 analog DAC. • 1'b0: Disabled • 1'b1: Enabled (default)
[4]	ENABLE_ANALOG_DAC_CH1	Enables ch1 analog DAC. • 1'b0: Disabled • 1'b1: Enabled (default)
[3]	ENABLE_NSMOD	Enables nsmod clock. • 1'b0: Clock disabled • 1'b1: Clock enabled (default)
[2]	ENABLE_DAC	Enables DAC interpolation path clock. • 1'b0: Clock disabled • 1'b1: Clock enabled (default)
[1]	AMP_MODE_REG	Sets system mode. • 1'b0: Power Down (default) • 1'b1: HIFI
[0]	RESERVED	NA

Register 1: SYS MODE CONFIG

Bits	[7:3]	[2]	[1]	[0]
Default	5'b00001	1'b0	1'b0	1'b1

Bits	Mnemonic	Description
[7:3]	RESERVED	NA
[2]	ENABLE_DOP_DECODE	Enables DoP decoding. • 1'b0: Disabled (default) • 1'b1: Enabled
[1]	ENABLE_DSD_DECODE	Enables DSD decoding. • 1'b0: Disabled (default) • 1'b1: Enabled
[0]	ENABLE_TDM_DECODE	Enables TDM decoding. • 1'b0: Disabled • 1'b1: Enabled (default)

Register 2: DAC CLOCK CONFIG

Bits	[7]	[6]	[5:0]
Default	1'b0	1'b0	6'd7

Bits	Mnemonic	Description
[7]	RESERVED	NA
[6]	SELECT_IDAC_HALF	Specifies whether to half CLK_IDAC divider. • 1'b0: Divide by SELECT_IDAC_NUM + 1 (default) • 1'b1: Divide by half of SELECT_IDAC_NUM + 1 Note: Can only produce half of an odd number divide
[5:0]	SELECT_IDAC_NUM	CLK_IDAC divider. Whole number divide value + 1 for CLK_IDAC (SYS_CLK/divide_value). • 6'd0: Whole number divide value + 1 = 1 • 6'd1: Whole number divide value + 1 = 2 • 6'd63: Whole number divide value + 1 = 64

Register 3: MASTER CLOCK CONFIG

Bits	[7]	[6:0]
Default	1'b0	7'd7

Bits	Mnemonic	Description
[7]	SELECT_MENC_HALF	Master Encoder (MENC) • 1'b0: Divide by SELECT_MENC_NUM + 1 (default) • 1'b1: Divide by half of SELECT_MENC_NUM + 1 Note: Can only produce half of an odd number divide
[6:0]	SELECT_MENC_NUM	Master mode clock divider. Whole number divide value + 1 for CLK_Master (SYS_CLK/divide_value). • 7'd0: Whole number divide value + 1 = 1 • 7'd1: Whole number divide value + 1 = 2 • 7'd127: Whole number divide value + 1 = 128

Register 4: CP CLOCK DIV

Bits	[7:0]
Default	8'd31

Bits	Mnemonic	Description
[7:0]	CP_CLK_DIV	Specifies the clk divider for the CP clock source. Valid from 8'd0 to 8'd255. 8'dX: CP clock is SYS_CLK/((X+1)*2) • 8'd0: Minimum • 8'd31: Defaults • 8'd255: Maximum

Register 8-5: RESERVED

Register 10- 9: INTERRUPT MASK P

Bits	[15:14]	[13]	[12]	[11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	2'b00	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[15:14]	INPUT_DATA_TYPE_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[13]	TDM_DATA_VALID_FLAG_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[12]	CLK_AVALID_FLAG_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[11]	RWS_REFERENCE_COUNTER_FULL_FLAG_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[10]	BCK_WS_FAILED_FLAG_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[9]	RESERVED	NA
[8]	DOP_VALID_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[7]	SOFT_RAMP_CH2_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive

[6]	SOFT_RAMP_CH1_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[5]	DRE_FLAG_CH2_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[4]	DRE_FLAG_CH1_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[3]	AUTOMUTE_FLAG_CH2_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[2]	AUTOMUTE_FLAG_CH1_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[1]	VOL_MIN_CH2_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[0]	VOL_MIN_CH1_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive

Register 12-11: INTERRUPT MASK N

Bits	[15:14]	[13]	[12]	[11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	2'b00	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[15:14]	INPUT_DATA_TYPE_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[13]	TDM_DATA_VALID_FLAG_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[12]	CLK_AVALID_FLAG_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[11]	RWS_REFERENCE_COUNTER_FULL_FLAG_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[10]	BCK_WS_FAILED_FLAG_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[9]	RESERVED	NA
[8]	DOP_VALID_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[7]	SOFT_RAMP_CH2_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative

[6]	SOFT_RAMP_CH1_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[5]	DRE_FLAG_CH2_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[4]	DRE_FLAG_CH1_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[3]	AUTOMUTE_FLAG_CH2_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[2]	AUTOMUTE_FLAG_CH1_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[1]	VOL_MIN_CH2_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[0]	VOL_MIN_CH1_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative

Register 14-13: INTERRUPT CLEAR

Bits	[15:14]	[13]	[12]	[11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	2'b00	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[15:14]	INPUT_DATA_CLEAR	Write a 1'b1 to clear the interrupt
[13]	TDM_DATA_VALID_CLEAR	Write a 1'b1 to clear the interrupt
[12]	CLK_AVALID_FLAG_CLEAR	Write a 1'b1 to clear the interrupt
[11]	RWS_REFERENCE_COUNTER_FULL_FLAG_CLEAR	Write a 1'b1 to clear the interrupt
[10]	BCK_WS_FAILED_FLAG_CLEAR	Write a 1'b1 to clear the interrupt
[9]	RESERVED	NA
[8]	DOP_VALID_CLEAR	Write a 1'b1 to clear the interrupt
[7]	SOFT_RAMP_CH2_CLEAR	Write a 1'b1 to clear the interrupt
[6]	SOFT_RAMP_CH1_CLEAR	Write a 1'b1 to clear the interrupt
[5]	DRE_FLAG_CH2_CLEAR	Write a 1'b1 to clear the interrupt
[4]	DRE_FLAG_CH1_CLEAR	Write a 1'b1 to clear the interrupt
[3]	AUTOMUTE_FLAG_CH2_CLEAR	Write a 1'b1 to clear the interrupt
[2]	AUTOMUTE_FLAG_CH1_CLEAR	Write a 1'b1 to clear the interrupt
[1]	VOL_MIN_CH2_CLEAR	Write a 1'b1 to clear the interrupt
[0]	VOL_MIN_CH1_CLEAR	Write a 1'b1 to clear the interrupt

Register 15: ANALOG CTRL CONFIG

Bits	[7]	[6]	[5]	[4:2]	[1]	[0]
Default	1'd0	1'b1	1'b1	3'b000	1'b0	1'b0

Bits	Mnemonic	Description
[7]	RESERVED	NA
[6]	AMP_PDB_ON_SS	DAC amp power control for soft ramp on normal mute. • 1'b0: When soft ramped to ground during normal mute, keeps DAC AMP on • 1'b1: When soft ramped to ground during normal mute allow DAC AMP to shut down for power saving (default) "normal mute" includes: 54utomate, mute by register, mute by GPIO
[5]	AMP_PDB_CLK_INVALID	DAC amp power control for soft ramp on abnormal mute. • 1'b0: When soft ramped to ground during abnormal mute, keeps DAC AMP on • 1'b1: When soft ramped to ground during abnormal mute allow DAC AMP to shut down for power saving (default) "abnormal mute" includes: PLL unlock, BCK_WS ratio failed
[4:2]	RESERVED	NA
[1]	LP_DAC_REG	Set the low power mode for DAC regulator (Left) • 1'b0: Normal Mode • 1'b1: Low power mode enabled
[0]	EN_FCB	Enable the fast charge for VREF_L AND VREF_R • 1'b0: Enabled (default) • 1'b1: Disable fast charge

Register 16: LDRV CTRL

Bits	[7]	[6]	[5:0]
Default	1'b0	1'b0	6'b000011

Bits	Mnemonic	Description
[7]	ENB_OCP_LDRV_CH2	Line driver over current protection • 1'b0: Enable • 1'b1: Disable
[6]	ENB_OCP_LDRV_CH1	Line driver over current protection • 1'b0: Enable • 1'b1: Disable
[5:0]	RESERVED	NA

Register 17: RESERVED

Register 19-18: ANALOG CONTROL OVERRIDE2

Bits	[15]	[14]	[13:0]
Default	1'b1	1'b1	14'b00000000000000

Bits	Mnemonic	Description
[15]	TRIB_DAC_CH2	Set DAC output tri-state • 1'b0: tri-state • 1'b1: Normal operation
[14]	TRIB_DAC_CH1	Set DAC output tri-state • 1'b0: tri-state • 1'b1: Normal operation
[13:0]	RESERVED	NA

Register 23-20: RESERVED

GPIO Registers

Register 24: GPIO CONFIG

Bits	[7]	[6]	[5]	[4]	[3:0]
Default	1'b0	1'b0	1'b0	1'b0	4'd0

Bits	Mnemonic	Description
[7]	INVERT_GPIO1	Invert GPIO1 • 1'b1: Inverts GPIO1 output.
[6]	GPIO1_WK_EN	Enables GPIO1 weak keeper. • 1'b0: GPIO1 weak keeper disabled (default) • 1'b1: GPIO1 weak keeper enabled Note: Weak keeper is a holder that can be optionally set, it maintains the previous state driver, with the GPIOx_WK_EN bit.
[5]	GPIO1_SDB	Enables GPIO1 input. • 1'b0: Disables GPIO1 input (default) • 1'b1: Enables GPIO1 input
[4]	GPIO1_OE	Enables GPIO1 output. • 1'b0: Tristate GPIO1 (default) • 1'b1: GPIO1 Output Enable
[3:0]	GPIO1_CFG	Configures GPIO1 • 4'd0: output 0 – output • 4'd1: output 0 – output • 4'd2: output 1 – output • 4'd3: CLK_DATA – output • 4'd4: interrupt – output • 4'd5: mute all channel – input • 4'd6: system mode control – input • 4'd7: Reserved • 4'd8: clk_avalid – output • 4'd9: output PWM1 – output • 4'd10: output PWM2 – output • 4'd11: output PWM3 – output • 4'd12: volume minimum – output • 4'd13: 56utomate status – output • 4'd14: soft ramp done – output • 4'd15: output 0 – output

Register 25: GPIO CONFIG2

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b1	1'b0	1'b0

Bits	Mnemonic	Description
[7]	GPIO_OR_SS_RAMP	When GPIOx_CFG=14 (output soft ramp done flag): • 1'b0: The soft ramp done flag is determined by GPIO_AND_SS_RAMP and GPIO_SEL (default) • 1'b1: The soft ramp done flag is the "OR" of both channel soft ramp done flags
[6]	GPIO_OR_VOL_MIN	When GPIOx_CFG=12 (output vol_min flag): • 1'b0: The vol_min flag is determined by GPIO_AND_VOL_MIN and GPIO_SEL (default) • 1'b1: The vol_min flag is the "OR" of both channel vol_min flags
[5]	GPIO_OR_AUTOMUTE	When GPIOx_CFG=13 (output 57utomate status): • 1'b0: The 57utomate status is determined by GPIO_AND_AUTOMUTE and GPIO_SEL (default) • 1'b1: The 57utomate status is the "OR" of both channel 57utomate status
[4]	GPIO_AND_SS_RAMP	When GPIOx_CFG=14 (output soft ramp done flag) and GPIO_OR_SS_RAMP is not set: • 1'b0: The soft ramp done flag is from a single channel selected by GPIO_SEL (default) • 1'b1: The soft ramp done flag is the "AND" of both channel soft ramp done flags
[3]	GPIO_AND_VOL_MIN	When GPIOx_CFG=12 (output vol_min flag) and GPIO_OR_VOL_MIN is not set: • 1'b0: The vol_min flag is from a single channel selected by GPIO_SEL (default) • 1'b1: The vol_min flag is the "AND" of both channel vol_min flags
[2]	GPIO_AND_AUTOMUTE	When GPIOx_CFG=13 (output 57utomate status) and GPIO_OR_AUTOMUTE is not set: • 1'b0: The 57utomate status is from a single channel selected by GPIO_SEL • 1'b1: The 57utomate status is the "AND" of both channel 57utomate status (default)
[1]	RESERVED	NA
[0]	GPIO1_READ	• 1'b0: GPIO1 Readback disabled (default) • 1'b1: Allow readback of GPIO1_I

Register 26: GPIO INPUT ENABLE

Bits	[7:3]	[1]	[0]
Default	5’d0	1’b0	1’b0

Bits	Mnemonic	Description
[7:3]	RESERVED	NA
[1]	GPIO_AMP_MODE	When any GPIO_CFG is set to 6 (input system mode control): • 1’b0: Power down when GPIO input is 1 (default) • 1’b1: HIFI when GPIO input is 1 (when GPIO input is 0, system mode is determined by register AMP_MODE (register 0, bit[1]))
[0]	GPIO_SEL	When GPIOx_CFG is set to 12, 13 or 14, and the corresponding GPIO_AND and GPIO_OR are not set: • 1’d0: Outputs status/flag from ch1 • 1’d1: Outputs status/flag from ch2

Register 27: PWM1 COUNT

Bits	[7:0]
Default	8’d0

Bits	Mnemonic	Description
[7:0]	PWM1_COUNT	8-bit value to set the number of SYS_CLK periods the PWM signal is high for. Valid from 8’d0 to 8’d255 • 8’d0: minimum • 8’d255: maximum

Register 29-28: PWM1 FREQUENCY

Bits	[15:0]
Default	16'd0

Bits	Mnemonic	Description
[15:0]	PWM1_FREQ	16-bit value to set the frequency of the PWM signal in terms of SYS_CLK divisions. Valid from 16'h0000 to 16'hFFFF $frequency\ (Hz) = \frac{SYS\_CLK}{PWM1\_FREQ}$ $Duty\ Cycle\ (\%) = \left(1 - \frac{PWM1\_FREQ - PWM1\_COUNT}{PWM1\_FREQ}\right) \times 100$

Register 30: PWM2 COUNT

Bits	[7:0]
Default	8'd0

Bits	Mnemonic	Description
[7:0]	PWM2_COUNT	8-bit value to set the number of SYS_CLK periods the PWM signal is high for. Valid from 8'd0 to 8'd255 • 8'd0: minimum • 8'd255: maximum

Register 32-31: PWM2 FREQUENCY

Bits	[15:0]
Default	16'd0

Bits	Mnemonic	Description
[15:0]	PWM2_FREQ	16-bit value to set the frequency of the PWM signal in terms of SYS_CLK divisions. Valid from 16'h0000 to 16'hFFFF $frequency\ (Hz) = \frac{SYS\_CLK}{PWM3\_FREQ}$ $Duty\ Cycle\ (\%) = \left(1 - \frac{PWM3\_FREQ - PWM3\_COUNT}{PWM3\_FREQ}\right) \times 100$

Register 33: PWM3 COUNT

Bits	[7:0]
Default	8'd0

Bits	Mnemonic	Description
[7:0]	PWM3_COUNT	8-bit value to set the number of SYS_CLK periods the PWM signal is high for. Valid from 8'd0 to 8'd255 • 8'd0: minimum • 8'd255: maximum

Register 35-34: PWM3 FREQUENCY

Bits	[15:0]
Default	16’d0

Bits	Mnemonic	Description
[15:0]	PWM3_FREQ	16-bit value to set the frequency of the PWM signal in terms of SYS_CLK divisions. Valid from 16’h0000 to 16’hFFFF $frequency\ (Hz) = \frac{SYS_{CLK}}{PWM3\_FREQ}$ $Duty\ Cycle\ (\%) = \left(1 - \frac{PWM3\_FREQ - PWM3\_COUNT}{PWM3\_FREQ}\right) \times 100$

DAC Registers

Register 36: INPUT CONFIG

Bits	[7]	[6]	[5]	[4]	[3]	[2:1]	[0]
Default	1'b1	1'b0	1'b0	1'b0	1'b0	2'd0	1'b0

Bits	Mnemonic	Description
[7]	AUTO_FS_DETECT	Enables automatic tuning of CLK_DAC/CLK_IDAC ratio according to detected FS. • 1'b0: Auto tune Disabled • 1'b1: Auto tune CLK_DAC/CLK_IDAC ratio according to detected FS (default)
[6]	DSD_NEGEDGE	Changes DSD latching edge polarity. • 1'b0: Latch DSD data at positive edge of DSD_CLK (default) • 1'b1: Latch DSD data at negative edge of DSD_CLK
[5]	DSD_MASTER_MODE	DSD master mode config. • 1'b0: DSD slave mode (default) • 1'b1: DSD master mode. DSD_CLK outputs from DATA_CLK
[4]	ENABLE_TDM_MASTER_MODE	TDM master mode config. • 1'b0: TDM slave mode (default) • 1'b1: TDM master mode enabled. Master BCK and WS output from DATA_CLK and DATA1
[3]	ENABLE_PDM	Enable PDM playback. If not using AUTO_INPUT_SELECT for DSD streaming, assert ENABLE_PDM (1b'1) and use INPUT_SEL 2'd1. • 1'b0: TDM mode (default) • 1'b1: PDM mode
[2:1]	INPUT_SEL	Selects input data when AUTO_INPUT_SELECT is set to 2'd0. • 2'd0: TDM (default) • 2'd1: DSD • 2'd2: DoP • 2'd3: Reserved
[0]	AUTO_INPUT_SELECT	Auto input data selection configuration • 2'd0: Disables auto input select. Input data type is set by INPUT_SEL (default) • 2'd1: Auto select between DSD and TDM inputs.

Register 37: MASTER MODE CONFIG

Bits	[7]	[6]	[5]	[4:3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	2'd0	1'b0	1'b0	1'b1

Bits	Mnemonic	Description
[7]	AUTO_FS_DETECT_BLOCK_2XMODE	Automatic 2x mode enable. • 1'b0: Set 2x mode when the detected CLK_DAC/CLK_IDAC ratio is 64 (default) • 1'b1: Do not set 2x mode when the detected CLK_DAC/CLK_IDAC ratio is 64
[6]	MASTER_BCK_DIV1	When enabled, master BCK is 128fs clock. Otherwise, BCK is less than or equal to 64fs. • 1'b0: BCK is not 128fs clock (default) • 1'b1: BCK is 128fs clock
[5]	MASTER_WS_IDLE	Sets the value of master WS when WS is idle. • 1'b0: WS is 0 when idle (default) • 1'b1: WS is 1 when idle
[4:3]	MASTER_FRAME_LENGTH	Selects the bit length in each TDM channel in master mode. • 2'd0: 32 bit (default) • 2'd2: 16 bit • others: Reserved
[2]	MASTER_WS_PULSE_MODE	When enabled, master WS is a pulse signal instead of a 50% duty cycle signal. The pulse width is 1 BCK cycle. • 1'b0: 50% duty cycle WS signal (default) • 1'b1: Pulse WS signal
[1]	MASTER_WS_INVERT	Inverts master WS. • 1'b0: Non-inverted (default) • 1'b1: Inverted
[0]	MASTER_BCK_INVERT	Inverts master BCK or DSD_CLK. • 1'b0: Non-inverted • 1'b1: Inverted (default)

Register 38: TDM CONFIG1

Bits	[7]	[6:4]	[3:0]
Default	1'b0	3'd0	4'd1

Bits	Mnemonic	Description
[7]	TDM_RESYNC	Force TDM decoder to resynchronize (RESYNC) • 1'b0: Let decoder sync (default) • 1'b1: Force decoder not sync
[6:4]	MASTER_WS_SCALE	In TDM master mode, tunes master BCK/WS ratio by scaling master WS. It allows more TDM slots in a fixed frame. • 3'd0: No scale (default) • 3'd1: Scale down WS by 2 • 3'd2: Scale down WS by 4 • 3'd3: Scale down WS by 8 • 3'd4: Scale down WS by 16 • others: Reserved
[3:0]	TDM_CH_NUM	Total TDM slot number per frame = TDM_CH_NUM + 1. • 4'd0: Minimum • 4'd1: Default • 4'd15: Maximum

Register 39: TDM CONFIG2

Bits	[7]	[6]	[5:0]
Default	1'b0	1'b0	6'd1

Bits	Mnemonic	Description
[7]	TDM_LJ_MODE	TDM LJ mode. • 1'b0: Standard I2S (default) • 1'b1: LJ mode
[6]	TDM_VALID_EDGE	TDM WS valid edge. • 1'b0: negative edge (default) • 1'b1: positive edge
[5:0]	TDM_VALID_PULSE_LEN	Data valid pulse length adjustment. • 6'd1: Default

Register 40: TDM CONFIG3

Bits	[7]	[6:5]	[4:0]
Default	1'd0	2'd0	5'd0

Bits	Mnemonic	Description
[7]	PDM_NEG_FIRST	PDM data edge polarity control. • 2'b0: PDM data ch1/2 are on positive/negative edges of PDM clock (default) • 2'b1: PDM data ch1/2 are on negative/positive edges of PDM clock
[6:5]	TDM_BIT_WIDTH	Bit width of each TDM slot. • 2'b00: 32-bit (default) • 2'b01: 24-bit • 2'b10: 16-bit • 2'b11: Reserved
[4:0]	TDM_DATA_LATCH_ADJ	Sets the position of the start bit within each TDM slot Can be moved +ve or -ve relative to MSB. • 5'd00: Default • 5'd16: Start bit shifted 16 bits towards LSB • 5'd31: Start bit shifted 16 bits towards MSB

Register 41: RESERVED

Register 42: TDM SLOT CONFIG

Bits	[7:4]	[3:0]
Default	4'd1	4'd0

Bits	Mnemonic	Description
[7:4]	TDM_CH2_SLOT_SEL	CH2 data slot selection. CH2 receives data from Mth slot. M = TDM_CH2_SLOT_SEL + 1. • 4'd00: Minimum (M=1) • 4'd15: Maximum (M=16)
[3:0]	TDM_CH1_SLOT_SEL	CH1 data slot selection. CH1 receives data from Mth slot. M = TDM_CH1_SLOT_SEL + 1. • 4'd00: Minimum (M=1) • 4'd15: Maximum (M=16)

Register 43: RESERVED

Register 44: RESYNC CONFIG

Bits	[7]	[6]	[5:0]
Default	1'b0	1'b1	6'b000000

Bits	Mnemonic	Description
[7]	RESERVED	NA
[6]	CP_PDB_ON_MUTE	Charge pump state control when mute • 1'b0: Keep charge pump on when mute • 1'b1: Turn off charge pump when mute (default)
[5]	RESERVED	NA
[4]	SYNC_DAC_CLK_DIV	Controls clock divider reset on negative edge of WS. • 1'b1: Clock divider will be reset at every negative edge of WS • 1'b0: Disable the FIR_RESYNC reset Note: If reset the SYNC_DAC_CLK_DIV (ie 1'b1), toggle this bit before setting any other RESYNC bits [3:0]
[3]	DOP_CLK_RESYNC	Controls DoP clock divider reset on negative edge of WS. • 1'b1: Clock divider will be reset at every negative edge of WS • 1'b0: Disable the FIR_RESYNC reset
[2]	VOL_THD_RESYNC	Controls Volume-THD block reset on negative edge of WS. • 1'b1: DoP clock generator will be reset at every negative edge of WS • 1'b0: Disable the DOP_CLK_RESYNC reset
[1]	FIR_RESYNC	Controls FIR filters reset on negative edge of WS. • 1'b1: FIR filters will be reset at every negative edge of WS • 1'b0: Disable the FIR_RESYNC reset
[0]	FS_RESYNC	Controls FS clock generator reset on negative edge of WS. • 1'b1: FS clock generator will be reset at every negative edge of WS • 1'b0: Disable the FS_RESYNC reset

Register 45: DSD 2DB DOWN

Bits	[7]	[6:0]
Default	1'b1	7'd64

Bits	Mnemonic	Description
[7]	DSD_2DB_DOWN	Scales down DSD data by 2dB to match PCM data. • 1'b1: Scale (default) • 1'b0: No scale **Note: DSD_2DB_DOWN requires RUN_VOLUME to be toggled in order to take effect.**

[6:0]	RESERVED	NA

Register 46: VOLUME1

Bits	[7:0]
Default	8'd0

Bits	Mnemonic	Description
[7:0]	VOLUME1	DAC ch1 volume. -0dB to -127.5dB 0.5dB steps. • 8'd0: 0dB • 8'd255: -127.5dB

Register 47: VOLUME2

Bits	[7:0]
Default	8'd0

Bits	Mnemonic	Description
[7:0]	VOLUME2	DAC ch2volume. -0dB to -127.5dB 0.5dB steps. • 8'd0: 0dB • 8'd255: -127.5dB

Register 48: DAC VOL UP RATE

Bits	[7:0]
Default	8'd150

Bits	Mnemonic	Description
[7:0]	DAC_VOL_RATE_UP	Value by which the old VOLUME value is incremented to reach the new VOLUME value Valid from 8'd0 (instant) to 8'd255 (fastest), where 8'd0 instantly changes the VOLUME value Calculation of time ramp rate(in seconds): • 8'd0: Instant change • 8'd150: Default • 8'd255: Fastest change

Register 49: DAC VOL DOWN RATE

Bits	[7:0]
Default	8'd150

Bits	Mnemonic	Description

[7:0]	DAC_VOL_RATE_DOWN	Value by which the old VOLUME value is incremented to reach the new VOLUME value Valid from 8'd0 (instant) to 8'd255 (fastest), where 8'd0 instantly changes the VOLUME value Calculation of time ramp rate(in seconds): • 8'd0: Instant change • 8'd150: Default • 8'd255: Fastest change

Register 50: DAC VOL DOWN RATE FAST

Bits	**[7:0]**
Default	8’d0

Bits	**Mnemonic**	**Description**
[7:0]	DAC_VOL_RATE_FAST	Value by which the old VOLUME value is incremented to reach the new VOLUME value Valid from 8’d0 (instant) to 8’d255 (fastest), where 8’d0 instantly changes the VOLUME value Only used during abnormal mute (PLL unlock or BCK_WS ratio failed) Calculation of time ramp rate(in seconds): • 8’d0: Instant change • 8’d150: Default • 8’d255: Fastest change

Register 51: MUTE CTRL

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	FORCE_VOLUME	Volume update control. • 1'b0: Updates volume when toggling RUN_VOLUME (default) • 1'b0: Updates volume when toggling RUN_VOLUME (default)
[6]	DAC_USE_MONO_VOLUME	Defines how volume is controlled between channels. • 1'b0: Separated volume control (default) • 1'b1: Ch2 volume is set by Ch1 volume setting
[5]	RUN_VOLUME	Toggle RUN_VOLUME to update volumes set by VOLUME1-VOLUME8 • 1'b0: Disabled (default) • 1'b1: Enabled
[4]	RESERVED	NA
[3]	DAC_INVERT_CH2	Invert the output on Ch2 at the input to the NSMOD • 1'b0: Disabled (default) • 1'b1: Enabled
[2]	DAC_INVERT_CH1	Invert the output on Ch1 at the input to the NSMOD • 1'b0: Disabled (default) • 1'b1: Enabled
[1]	DAC_MUTE_CH2	DAC channel 2 mute control. • 1'b0: Normal operation (default) • 1'b1: Mute ch2
[0]	DAC_MUTE_CH1	DAC channel 1 mute control. • 1'b0: Normal operation (default) • 1'b1: Mute ch1

Register 52: FILTER CONFIG

Bits	[7]	[6]	[5]	[4:3]	[2:0]
Default	1'b0	1'b1	1'b0	2'b01	3'd0

Bits	Mnemonic	Description
[7]	AUTO_CH_DETECT	Auto detect BCK/FRAME ratio to determine the number of TDM channels. • 1'b0: Disabled (default) • 1'b1: Enabled
[6]	BYPASS_DEEMPH	De-emphasis filter control for ch1/2 only. • 1'b0: Enabled • 1'b1: Disables de-emphasis filters (default)
[5]	PEAK_FILTER	DRE peak filter control. • 1'b0: Disabled (default) • 1'b1: Enabled
[4:3]	SEL_DEEMPH	Configures the de-emphasis filters for various sample rate. • 2'b00: FS=32kHz • 2'b01: FS=44.1kHz (default) • 2'b10: FS=48kHz • 2'b11: Reserved
[2:0]	FILTER_SHAPE	Selects the 8x interpolation FIR filter shape. • 3'd0: Minimum phase (default) • 3'd1: Linear phase apodizing • 3'd2: Linear phase fast roll-off • 3'd3: Linear phase fast roll-off low ripple • 3'd4: Linear phase slow roll-off • 3'd5: Minimum phase fast roll-off • 3'd6: Minimum phase slow roll-off • 3'd7: Minimum phase slow roll-off low dispersion

Register 53: RESERVED

Register 54: DATAPATH CONTROL

Bits	[7:2]	[1]	[0]
Default	6'd0	1'b0	1'b0

Bits	Mnemonic	Description
[7:2]	RESERVED	NA
[1]	BYPASS_FIR4X	Bypass of the FIR 4x oversampling filter. • 1'b0: Normal Operation (default) • 1'b1: Bypass FIR 4x oversampling filter
[0]	BYPASS_FIR2X	Bypass of the FIR 2x oversampling filter. • 1'b0: Normal Operation (default) • 1'b1: Bypass FIR 2x oversampling filter

Register 56-55: THD COMP C2 CH1

Bits	[15:0]
Default	16'd360

Bits	Mnemonic	Description
[15:0]	THD_C2_CH1	A 16-bit signed coefficient for correcting for the CH1 second harmonic distortion. $output = x + c2 * x^2 + c3 * x^3$

Register 58-57: THD COMP C3 CH1

Bits	[15:0]
Default	16'd141

Bits	Mnemonic	Description
[15:0]	THD_C3_CH1	A 16-bit signed coefficient for correcting for the CH1 third harmonic distortion. $output = x + c2 * x^2 + c3 * x^3$

Register 60-59: THD COMP C2 CH2

Bits	[15:0]
Default	16'd360

Bits	Mnemonic	Description
[15:0]	THD_C2_CH2	A 16-bit signed coefficient for correcting for the CH2 second harmonic distortion. $output = x + c2 * x^2 + c3 * x^3$

Register 62-61: THD COMP C3 CH2

Bits	[15:0]
Default	16'd141

Bits	Mnemonic	Description
[15:0]	THD_C3_CH2	A 16-bit signed coefficient for correcting for the CH2 third harmonic distortion. $output = x + c2 * x^2 + c3 * x^3$

Register 64-63: AUTOMUTE TIME

Bits	[15]	[14]	[13]	[12]	[11]	[10:0]
Default	1'b1	1'b1	1'b0	1'b1	1'b1	11'd15

Bits	Mnemonic	Description
[15]	AUTOMUTE_RAMP_TO_GROUND	When ramped to minimum volume during normal mute, allow soft ramp to ground for power saving. • 1'b0: Disabled • 1'b1: Enabled (default) Note: Normal mute includes 74utomate, mute by register and mute by GPIO.
[14]	AUTOMUTE_WAIT_ON_DRE	Automute flag control. • 1'b0: Automute is flagged when 74utomate condition is met • 1'b1: Automute is flagged when 74utomate condition is met and DRE is engaged (default)
[13]	RESERVED	NA
[12]	AUTOMUTE_EN_CH2	Channel 2 automute. • 1'b0: Disables ch2 automute • 1'b1: Enables ch2 automute (default) Note: Automute is available for PCM only
[11]	AUTOMUTE_EN_CH1	Channel 1 automute. • 1'b0: Disables ch1 automute • 1'b1: Enables ch1 automute (default) Note: Automute is available for PCM only
[10:0]	AUTOMUTE_TIME	Configures the amount of time in seconds the audio must remain below AUTOMUTE_LEVEL before an 74utomate condition is flagged. Valid from 0 (disabled) to 11'h7FF (fastest), where 11'h001 is the slowest $Time\ in\ Seconds\ =\ 128fs * \frac{2^{18}}{AUTOMUTE\_TIME}$

Register 66-65: AUTOMUTE LEVEL

Bits	[15:0]
Default	16’d8

Bits	Mnemonic	Description
[15:0]	AUTOMUTE_LEVEL	Configures the threshold which the audio must be below before an 75utomate condition is flagged. • 16’h0000: Reserved • 16’h0001: Minimum (-132dB) • 16’hFFFF: Maximum (-42dB) Note: this register works in tandem with AUTOMUTE_TIME to create the 75utomate condition

Register 68-67: AUTOMUTE OFF LEVEL

Bits	[15:0]
Default	16’d10

Bits	Mnemonic	Description
[15:0]	AUTOMUTE_OFF_LEVEL	Configures the threshold which the audio must be above before the 75utomate condition is cleared (cleared immediately). • Valid from: 16’hFFFF (-42dB) to 16’h0001 (-132dB) • Shift right 1 bit corresponds to -6dB

Register 69: SOFT RAMP CONFIG

Bits	[7]	[6]	[5]	[4:0]
Default	1’b0	1’b0	1’b0	5’d2

Bits	Mnemonic	Description
[7]	GAIN_18DB_CH2	Applies +18dB digital gain on channel 2. • 1’b0: Disabled (default) • 1’b1: Enabled
[6]	GAIN_18DB_CH1	Applies +18dB digital gain on channel 1. • 1’b0: Disabled (default) • 1’b1: Enabled
[5]	SOFT_RAMP_TYPE	Sets whether the soft start ramp is linear or quadratic • 1’b0: Uses a quadratic function for the soft start ramp (default) • 1’b1: Uses the standard soft start ramp
[4:0]	SOFT_RAMP_TIME	Sets the amount of time that it takes to perform a soft start ramp. Valid from 0 to 20 (inclusive). • 5’d00: Minimum • 5’d02: Default • 5’d20: Maximum

Register 72-70: RESERVED

Register 73: DRE FORCE

Bits	[7]	[6]	[5:0]
Default	1'b1	1'b1	6'b000011

Bits	Mnemonic	Description
[7]	DRE_FORCE_CH2	Force CH2 into DRE mode even if zero cross has not occurred. • 1'b0: DRE engages when signal is below DRE threshold and a signal zero cross is detected(default). • 1'b1: DRE engages when signal is below DRE threshold and a signal zero cross is ignored.
[6]	DRE_FORCE_CH1	Force CH1 into DRE mode even if zero cross has not occurred. • 1'b0: DRE engages when signal is below DRE threshold and a signal zero cross is detected(default). • 1'b1: DRE engages when signal is below DRE threshold and a signal zero cross is ignored.
[5:0]	RESERVED	NA

Register 75-74: DRE GAIN CH1

Bits	[15:0]
Default	16'h1A34

Bits	Mnemonic	Description
[15:0]	DRE_GAIN1	Sets the DRE gain for CH1. Shift right 1 bit corresponds to -6dB. • 16'h07FF (0dB): Minimum • 16'h1A34 (16.33dB): Default • 16'h7FFF (30dB): Maximum

Register 77-76: DRE GAIN CH2

Bits	[15:0]
Default	16’h1A34

Bits	Mnemonic	Description
[15:0]	DRE_GAIN2	Sets the DRE gain for CH2. Shift right 1 bit corresponds to -6dB. • 16’h07FF (0dB): Minimum • 16’h1A34 (16.33dB): Default • 16’h7FFF (30dB): Maximum

Register 79-78: DRE ON THRESHOLD

Bits	[15:0]
Default	16’h0CF1

Bits	Mnemonic	Description
[15:0]	DRE_ON_THRESH	DRE on threshold. Shift right 1 bit corresponds to -6dB. • 16’h0CF1 (-48dB): Default • 16’hFFFF (-24dB): Maximum

Register 81-80: DRE OFF THRESHOLD

Bits	[15:0]
Default	16’h8184

Bits	Mnemonic	Description
[15:0]	DRE_OFF_THRESH	DRE off threshold. Shift right 1 bit corresponds to -6dB. • 16’h8184 (-28dB): Default • 16’hFFFF (-24dB): Maximum

Register 82: DRE DECAY RATE

Bits	[7]	[6]	[5]	[4:0]
Default	1’b1	1’b0	1’b1	5’d15

Bits	Mnemonic	Description
[7]	DRE_FORCE_LEVEL	Force CH1 + CH2 into DRE mode even if zero cross has not occurred. • 1’b0: Disabled • 1’b1: CH1 + CH2 forced into DRE mode
[6]	RESERVED	NA
[5]	MIN_PEAK	DRE peak detector starting point control. • 1’b0: DRE peak detector starts from max • 1’b1: DRE peak detector starts from min (default)
[4:0]	DRE_DECAY_RATE	Sets the speed at which the stored value of the DRE peak detector will decay when the input signal is below the stored value. • 5’d31 = slowest decay • 5’d0 = instant decay

Register 84-83: DC OFFSET CH1

Bits	[15:0]
Default	16’d0

Bits	Mnemonic	Description
[15:0]	DC_OFFSET1	DC offset for ch1 $V_{offset} = \frac{DC\_OFFSET1}{2^{24} - 1} * Vref$

Register 86-85: DC OFFSET CH2

Bits	[15:0]
Default	16’d0

Bits	Mnemonic	Description
[15:0]	DC_OFFSET2	DC offset for ch2 $V_{offset} = \frac{DC\_OFFSET2}{2^{24} - 1} * Vref$

Register 87: DC RAMP RATE

Bits	[7:0]
Default	8'd0

Bits	Mnemonic	Description
[7:0]	DC_RAMP_RATE	Value by which the old DC value is incremented/decremented per sample to reach the new DC value. • 8'd0: Instant (default) • 8'd1: Slowest • 8d'255: Fastest

Register 88: MASTER TRIM

Bits	[7:0]
Default	8'd0

Bits	Mnemonic	Description
[7:0]	MASTER_TRIM	Master trim volume. Unsigned, range 0dB(8'hFF) to -42dB(8'h01), 0 is bypass. • 8'h00: Bypass (default) • 8'h01 (-42dB): Minimum • 8'hFF (0dB): Maximum

PLL Registers

Note: some registers have an implied value that is recommended for normal and optimized operation.

Register 192: RESET & PLL REGISTER1

Bits	[7]	[6]	[5:3]	[2]	[1]	[0]
Default	1'b0	1'b0	3'd0	1'b0	1'b0	1'b1

Bits	Mnemonic	Description
[7]	AO_SOFT_RESET	Performs soft reset to Slave Registers. • 1'b0: Disabled (default) • 1'b1: Enabled
[6]	PLL_SOFT_RESET	Performs soft reset to Synchronous Slave Registers. • 1'b0: Disabled (default) • 1'b1: Enabled
[5:3]	PLL_VCO_I	Set Current in PLL VCO • Must set to 3'b110, for normal operation
[2]	RESERVED	NA
[1]	GPIO1_SDB_SYNC	Configures GPIO1 SDB (Shutdown_b). When SYS_CLK is provided through GPIO1, set this bit to '1' to allow SYS_CLK input. • 1'b0: Disabled (default) • 1'b1: Enabled
[0]	PLL_CLKHV_PHASE	Digital/analog DAC clock phase control. • 1'b0: Digital/analog DAC clocks have inverted phase • 1'b1: Digital/analog DAC clocks have the same phase (default)

Register 193: PLL REGISTER2

Bits	[7]	[6]	[5]	[4:2]	[1]	[0]
Default	1'b0	1'b0	1'b0	2'd0	1'd0	1'b0

Bits	Mnemonic	Description
[7]	PLL_BYP	PLL bypass mode. • 1'b0: Disabled (default) • 1'b1: Enabled
[6]	DVDD_SHUNTB	Enables digital regulator output shunt to ground (10k). Active low. • 1'b0: Enabled (default) • 1'b1: Disabled
[5]	SEL_1V_DREG	Sets digital regulator output voltage to 1V • 1'b0: Disabled (default) • 1'b1: Enabled
[4:2]	PLL_HVREG_VREF_SEL	PLL HVREG reference voltage selection • 3'b001: 1.6V **(optimum setting, normal operation)** • others: Reserved
[1]	SEL_PLL_IN	Selects PLL input clock sources. • 1'd0: MCLK (default) • 1'd1: BCK
[0]	EN_PLL_CLKIN	Controls PLL input clocks. • 1'b0: Disables PLL input clocks (default) • 1'b1: Enables PLL input clocks

Register 194: PLL REGISTER3

Bits	[7:4]	[3]	[2]	[1]	[0]
Default	4'd0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7:3]	RESERVED	NA
[2]	AUTO_LOCK_EN	Allows PLL to relock when PLL lock is lost and there are 256 valid PLL input clock cycles. • 1'b0: Disabled (default) • 1'b1: Enabled
[1:0]	RESERVED	NA

Register 195: PLL REGISTER4

Bits	[7:5]	[4:3]	[2]	[1]	[0]
Default	3'd0	2'd0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7:5]	PLL_CP_BIAS_SEL	Sets the PLL Charge Pump BIAS current value: • **3b'011:4u (optimum setting, for normal operation)**
[4:3]	PLL_ID_SEL	Sets the PLL **I**nternal **D**elay: • **2b'11:1.5nS (optimum setting, for normal operation)** **Note: Fixed to 1.5nS, no other possible cases**
[2]	PLL_VCO_FMAX	Disables the PLL VCO's FMAX-limiting • 1'b0 (default): Limit is set • **1'b1: No limit (for normal operation)**
[1]	PLL_VCO_PDB	Enables/disables the PLL voltage-controlled oscillator (VCO). • 1'b0: Disabled (default) • 1'b1: Enabled
[0]	PLL_CP_PDB	Enables/disables the PLL charge pump. • 1'b0: Disabled (default) • 1'b1: Enabled

Register 196: PLL REGISTER5

Bits	[7:5]	[4:2]	[1:0]
Default	3'd0	3'd0	2'd0

Bits	Mnemonic	Description
[7:5]	PLL_VCO_BAND_CTRL	Selects the frequency band of the VCO. • 3'b011 (for optimum operation)
[4:2]	RESERVED	NA
[1:0]	PLL_VCO_IB_AMP_CTRL	Selects the V to I Amplifier's bias current: • 2'b10 (for optimum operation)

Register 199-197: PLL REGISTER6

Bits	[23:0]
Default	24’d0

Bits	Mnemonic	Description
[23:0]	PLL_CLK_FB_DIV	Sets the PLL clock feedback divider. • 20’d0: Reserved • 20’dn: Divide by (2^25)/n

Register 202-200: PLL REGISTER7

Bits	[23]	[22]	[21]	[20]	[19]	[18]	[17:14]	[13:10]	[9:1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	4'd0	4'd0	9'd0	1'b0

Bits	Mnemonic	Description
[23]	PLL_REG_PDB_HV	Power Down the regulators. • 1'b0: Disable the PLL HV-regulator (default) • 1'b1: Enable the PLL HV-regulator
[22]	PLL_REG_PDB_1V2	Power Down the regulators. • 1'b0: Disable the PLL 1V2-regulator (default) • 1'b1: Enable the PLL 1V2-regulator
[21:20]	RESERVED	NA
[19]	PLL_LOW_BW	PLL low bandwidth mode. • 1'b0: (default) • 1'b1: **Normal operation, optimum setting**
[18]	PLL_CLK_OUT_DIV_PHASE_EN	• 1'b0: Disabled (default) • 1'b1: Tune the PLL clock output divider phase according to PLL_CLK_OUT_DIV_PHASE
[17:14]	PLL_CLK_OUT_DIV_PHASE	Sets the PLL clock output divider phase
[13:10]	PLL_CLK_OUT_DIV	Sets the Output Division (No) of the PLL. • 9'd0: Divide by 1 (default) • 9'd1: Divide by 2 • 9'd2: Divide by 3 • 9'dn: Divide by n+1
[9:1]	PLL_CLK_IN_DIV	Sets the PLL clock input divider. • 9'd0: Divide by 1 (default) • 9'd1: Divide by 2 • 9'd2: Divide by 3 • 9'dn: Divide by n+1
[0]	PLL_FB_DIV_LOAD	Writes 1 then write 0 to load CLK_FB_DIV.

Register 203: PLL REGISTER8

Bits	[7:6]	[5]	[4]	[3:0]
Default	2'd0	1'b0	1'b0	4'b0000

Bits	Mnemonic	Description
[7:6]	RESERVED	NA
[5]	PLL_DIG_RSTB	Resets the Digital core of the PLL. • 1'b0 (default): PLL digital is off • 1b1: PLL digital is on
[4]	PLL_VCO_D_EN	PLL requirement for normal operation • 1'b0 (default): PLL not used • 1'b1: For normal PLL operation
[3:0]	RESERVED	NA

Read Only Registers

Register 224: SYS READ

Bits	[7:5]	[4:3]	[2]	[1]	[0]
Default	-	-	-	-	-

Bits	Mnemonic	Description
[7:5]	RESERVED	NA
[4:3]	MODES	Device mode readback. Based off MODE Pin (Pin 3) • 1'd1: I2C • 1'd2: HW_SERIAL • 1'd3: Reserved • 1'd4: SPI
[2]	ADDR1	I2C address select bit2.
[1]	ADDR0	I2C address select bit1.
[0]	RESERVED	NA

Register 225: CHIP ID READ

Bits	[7:0]
Default	-

Bits	Mnemonic	Description
[7:0]	CHIP_ID	CHIP ID.

Register 228-227: RESERVED

Register 230-229: INTERRUPT STATE

Bits	[15:14]	[13]	[12]	[11]	[10]	[9]	[8]	[7:6]	[5]	[4]	[3:2]	[1:0]
Default	-	-	-	-	-	-	-	-	-	-	-	-

Bits	Mnemonic	Description
[15:14]	INPUT_SELECT_OVERRIDE_INTSTATE	Input select override interrupt state • 2'b00: TDM select • 2'b01: DSD select • 2'b10: DoP select • 2'b11: RESERVED
[13]	TDM_DATA_VALID_INTSTATE	TDM data valid interrupt state. • 1'b0: Inactive • 1'b1: Active
[12]	CLK_AVALID_INT_INTSTATE	Clock A valid interrupt state. • 1'b0: Inactive • 1'b1: Active
[11]	RWS_REF_CNT_FULL_INTSTATE	Receiver WS reference counter full interrupt state. • 1'b0: Inactive • 1'b1: Active
[10]	BCK_WS_FAIL_INTSTATE	BCK WS fail interrupt state. • 1'b0: Inactive • 1'b1: Active
[9]	PLL_LOCKED_R_INTSTATE	PLL locked interrupt status. • 1'b0: Inactive • 1'b1: Active
[8]	DOP_VALID_INTSTATE	DOP valid interrupt state. • 1'b0: Inactive • 1'b1: Active
[7:6]	SS_FULL_RAMP_INTSTATE	SS full ramp interrupt state • 1'b0: Inactive • 1'b1: Active
[5]	DRE_SELECT2_INTSTATE	DRE select 2 interrupt state • 1'b0: Inactive • 1'b1: Active
[4]	DRE_SELECT1_INTSTATE	DRE select 1 interrupt state • 1'b0: Inactive • 1'b1: Active
[3:2]	AUTOMUTE_INTSTATE	Automute interrupt state • 1'b0: Inactive • 1'b1: Active

[1:0]	VOL_MIN_INTSTATE	Minimum volume interrupt state • 1'b0: Inactive • 1'b1: Active

Register 232-231: INTERRUPT SOURCE

Bits	[15:14]	[13]	[12]	[11]	[10]	[9]	[8]	[7:6]	[5]	[4]	[3:2]	[1:0]
Default	-	-	-	-	-	-	-	-	-	-	-	-

Bits	Mnemonic	Description
[15:14]	INPUT_SELECT_OVERRIDE_INTSOURCE	Input select override interrupt source
[13]	TDM_DATA_VALID_INTSOURCE	Valid TDM data interrupt source
[12]	CLK_AVALID_INT_INTSOURCE	Valid clock interrupt source
[11]	RWS_REF_CNT_FULL_INTSOURCE	RWS_REF_CNT interrupt source
[10]	BCK_WS_FAIL_INTSOURCE	BCK WS fail interrupt source
[9]	PLL_LOCKED_R_INTSOURCE	Locked PLL interrupt source
[8]	DOP_VALID_INTSOURCE	Valid DoP interrupt source
[7:6]	SS_FULL_RAMP_INTSOURCE	SS full ramp interrupt source
[5]	DRE_SELECT2_INTSOURCE	DRE select 2 interrupt source
[4]	DRE_SELECT1_INTSOURCE	DRE select 1 interrupt source
[3:2]	AUTOMUTE_INTSOURCE	Automute interrupt source
[1:0]	VOL_MIN_INTSOURCE	Minimum volume interrupt source

Register 233-238: RESERVED

Register 239: AUTO TUNING READ

Bits	[7]	[6]	[5:0]
Default	-	-	-

Bits	Mnemonic	Description
[7]	RATIO_VALID	A 1 indicates the CLK_DAC/CLK_IDAC ratio is valid (N or N.5) • 1'b0: Invalid • 1'b1: Valid
[6]	IDAC_DIV_HALF_REG	Result of auto FS tuning divider for IDAC_HALF flag
[5:0]	IDAC_DIV_REG	Result of auto FS tuning divider for CLK_DAC/CLK_IDAC ratio

Register 240: GPIO READ

Bits	[7:1]	[0]
Default	-	-

Bits	Mnemonic	Description
[7:1]	RESERVED	NA
[0]	GPIO1_I_READ	GPIO1 input readback. • 1'b0: Low • 1'b1: High

Register 241: DAC STATUS READ

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	-	-	-	-	-	-	-	-

Bits	Mnemonic	Description
[7]	SS_RAMP_DOWN_CH2	Channel 2 soft ramped down flag readback. • 1'b0: Soft ramp down not detected on channel 2 • 1'b1: Soft ramp down detected on channel 2
[6]	SS_RAMP_DOWN_CH1	Channel 1 soft ramped down flag readback. • 1'b0: Soft ramp down not detected on channel 1 • 1'b1: Soft ramp down detected on channel 1
[5]	SS_RAMP_UP_CH2	Channel 2 soft ramped up flag readback. • 1'b0: Soft ramp up not detected on channel 2 • 1'b1: Soft ramp up detected on channel 2
[4]	SS_RAMP_UP_CH1	Channel 1 soft ramped up flag readback. • 1'b0: Soft ramp up not detected on channel 1 • 1'b1: Soft ramp up detected on channel 1
[3]	AUTOMUTE_CH2	Channel 2 automute status readback. • 1'b0: Automute not detected on channel 2 • 1'b1: Automute detected on channel 2
[2]	AUTOMUTE_CH1	Channel 1 automute status readback. • 1'b0: Automute not detected on channel 1 • 1'b1: Automute detected on channel 1
[1]	VOL_MIN_CH2	Channel 2 minimum volume flag readback. • 1'b0: Minimum volume not detected on channel 2 • 1'b1: Minimum volume detected on channel 2
[0]	VOL_MIN_CH1	Channel 1 minimum volume flag readback. • 1'b0: Minimum volume not detected on channel 1 • 1'b1: Maximum volume detected on channel 1

Register 242: DRE STATUS READ

Bits	[7]	[6]	[5:4]	[3]	[2]	[1]	[0]
Default	-	-	-	-	-	-	-

Bits	Mnemonic	Description
[7]	TDM_DATA_VALID	TDM data valid flag • 1b'0: TDM data Not valid • 1b'1: TDM data Valid
[6]	DOP_VALID	DoP valid flag • 1b'0: Not valid • 1b'1: Valid
[5:4]	RESERVED	NA
[3]	DRE_DETECT_CH2	Cannel 2 DRE detection status. • 1b'0: DRE not detected on channel 2 • 1b'1: DRE detected on channel 2
[2]	DRE_DETECT_CH1	DRE is detected ch1 • 1b'0: DRE not detected on channel 1 • 1b'1: DRE detected on channel 1
[1]	DRE_SELECT_CH2	Channel 2 DRE engage status. • 1b'0: DRE not engaged on channel 2 • 1b'1: DRE engaged on channel 2
[0]	DRE_SELECT_CH1	Channel 1 DRE engage status. • 1b'0: DRE not engaged on channel 1 • 1b'1: DRE engaged on channel 1

Reference Schematic

Hardware Mode

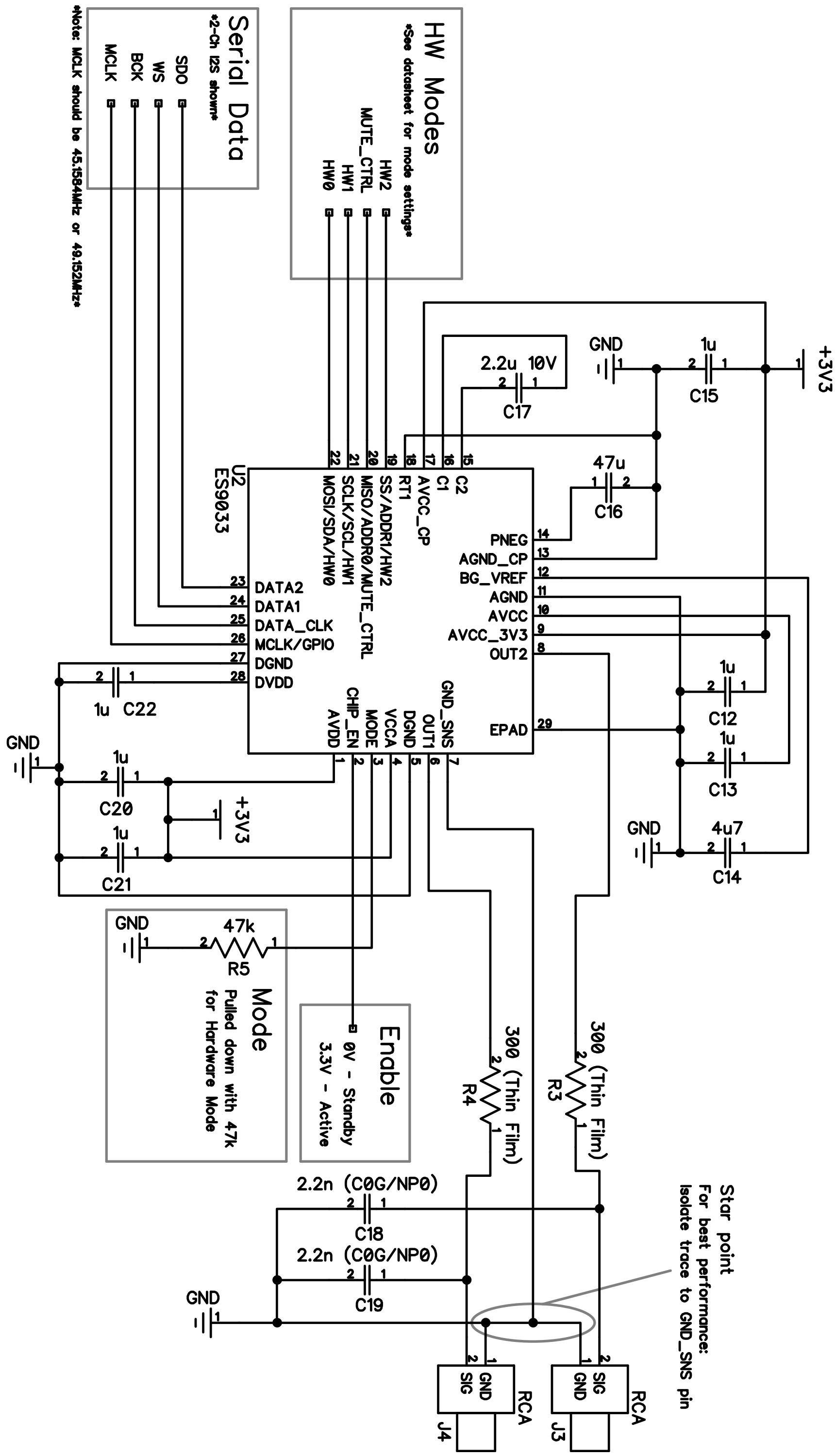


Figure 17 – Hardware mode reference schematic

Software Mode

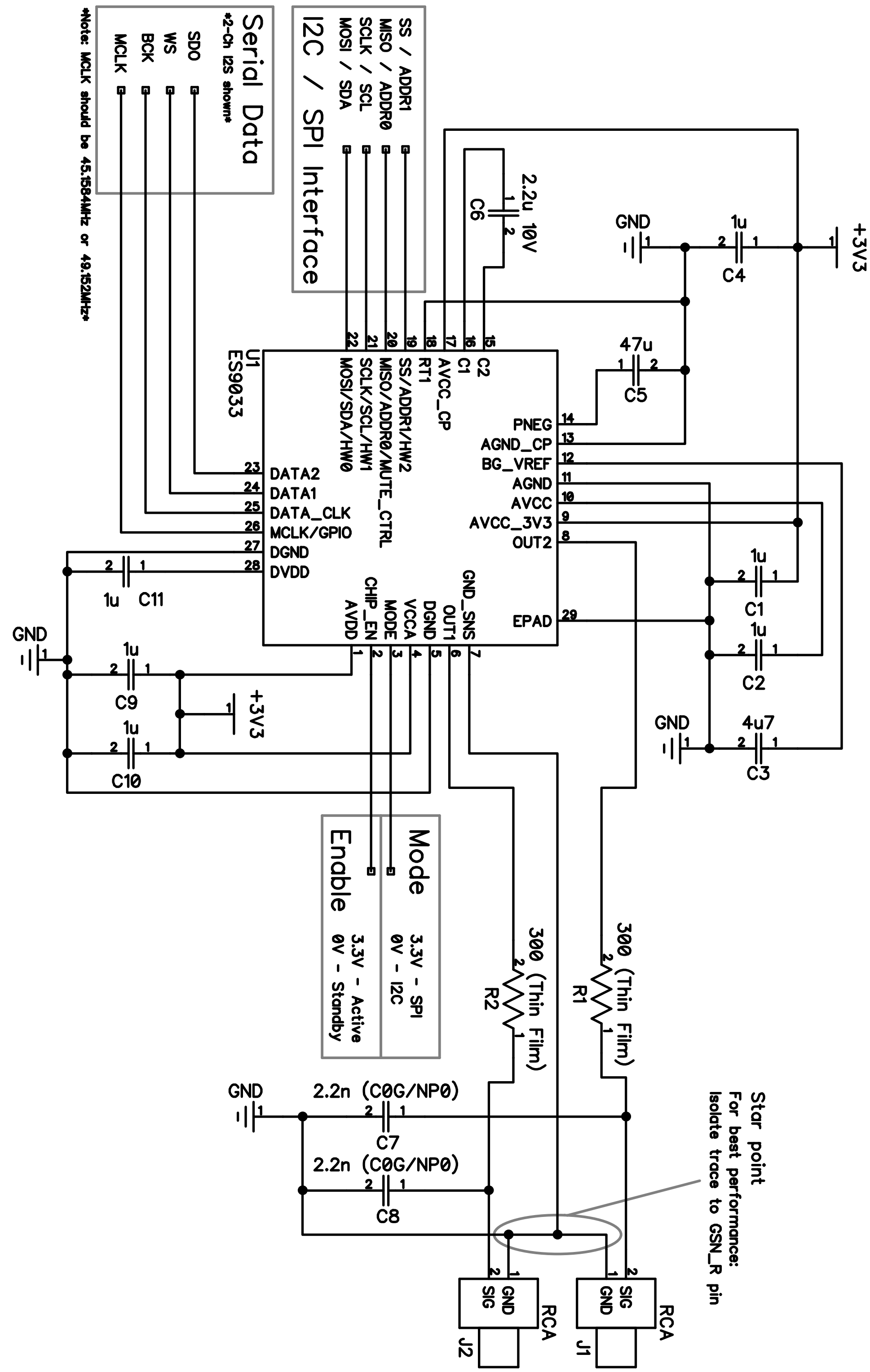
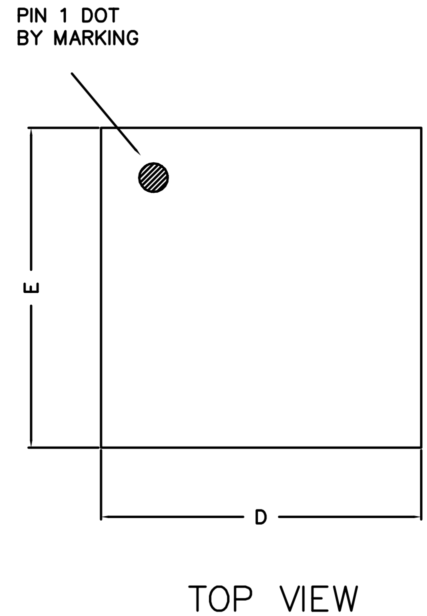
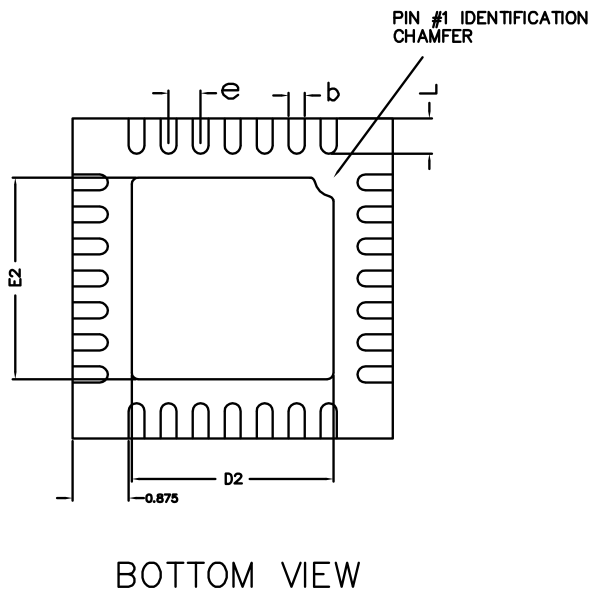
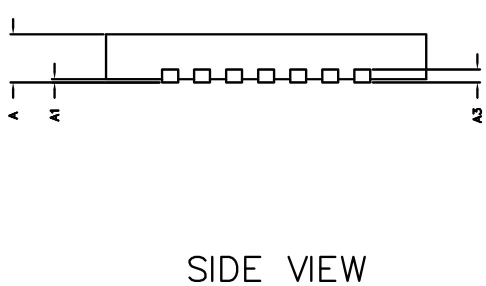


Figure 18 – Software mode reference schematic

28 QFN Package Dimensions







COMMON DIMENSIONS(MM)			
PKG.	W: VERY VERY THIN		
REF.	MIN.	NOM.	MAX
A	0.70	0.75	0.80
A1	0.00	–	0.05
A3	0.2 REF.		
D	4.95	5.00	5.05
E	4.95	5.00	5.05
b	0.18	0.23	0.30
L	0.45	0.55	0.65
D2	3.00	3.15	3.25
E2	3.00	3.15	3.25
e	0.5 BSC		

Figure 19 – QFN package dimensions

28 QFN Top View Marking

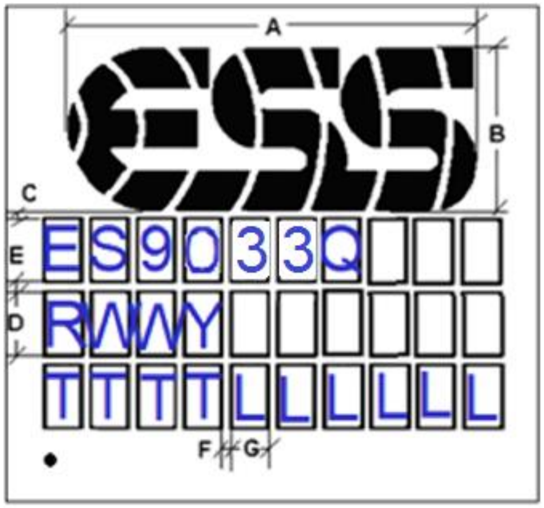


Figure 20 – 28 QFN top view markings

	Dimension in mm						
Package Type	A	B	C	D	E	F	G
QFN 5mm x 5mm	4.0	1.6	0.2	0.4	0.2	0.1	0.3

Table 21 – 28 QFN top view markings dimensions

T	*Tracking*
W	*Work week*
Y	*Last digit of year*
L	*Lot number*
R	*Silicon Revision*

Table 22 – 28 QFN top view markings definitions

Marking is subject to change. This drawing is not to scale

Reflow Process Considerations

Temperature Controlled

For lead-free soldering, the characterization and optimization of the reflow process is the most important factor to consider.

The lead-free alloy solder has a melting point of 217°C. This alloy requires a minimum reflow temperature of 235°C to ensure good wetting. The maximum reflow temperature is in the 245°C to 260°C range, depending on the package size (RPC-2 Pb-Free Process – Classification Temperatures (Tc)). This narrows the process window for lead-free soldering to 10°C to 20°C.

The increase in peak reflow temperature in combination with the narrow process window makes the development of an optimal reflow profile a critical factor for ensuring a successful lead-free assembly process. The major factors contributing to the development of an optimal thermal profile are the size and weight of the assembly, the density of the components, the mix of large and small components, and the paste chemistry being used.

Reflow profiling needs to be performed by attaching calibrated thermocouples well adhered to the device as well as other critical locations on the board to ensure that all components are heated to temperatures above the minimum reflow temperatures and that smaller components do not exceed the maximum temperature limits (Table RPC-2).

To ensure that all packages can be successfully and reliably assembled, the reflow profiles studied and recommended by ESS are based on the JEDEC/IPC standard J-STD-020 revision D.1.

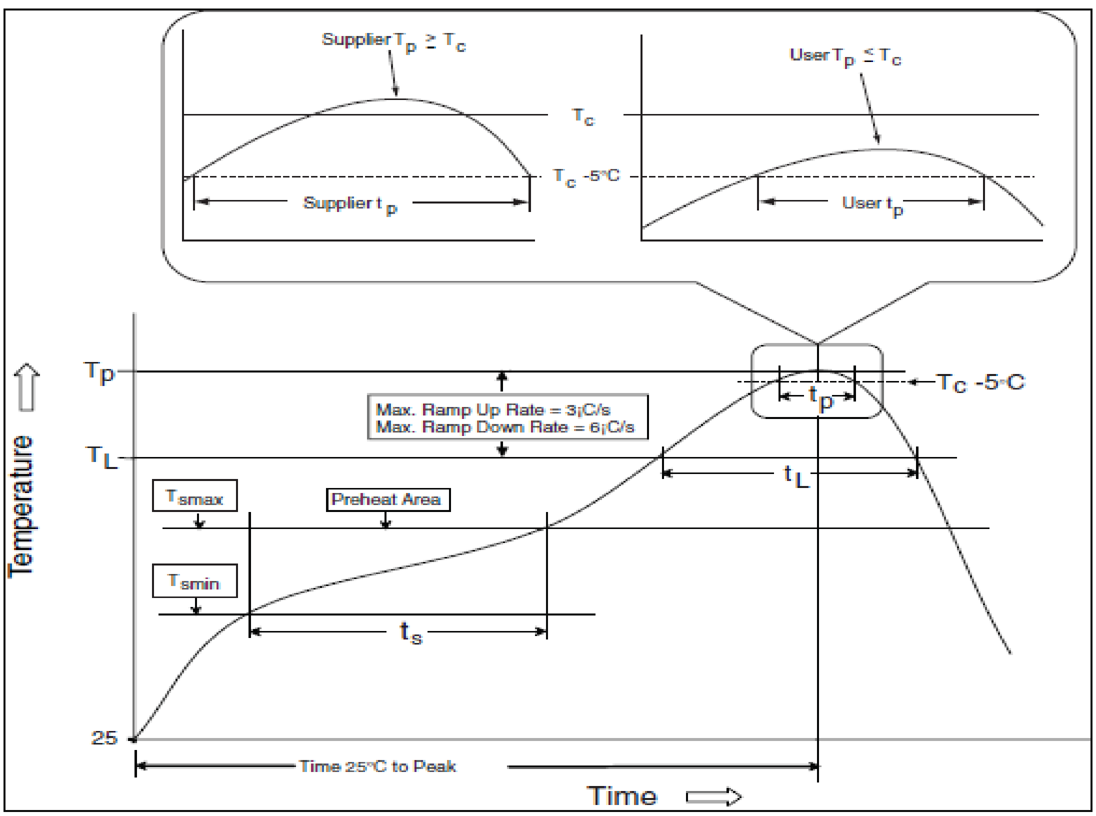


Figure 21 – IR/Convection Reflow Profile (IPC/JEDEC J-STD-020D.1)

Reflow is allowed 3 times. Caution must be taken to ensure time between re-flow runs does not exceed the allowed time by the moisture sensitivity label. If the time elapsed between the re-flows exceeds the moisture sensitivity time bake the board according to the moisture sensitivity label instructions.

Manual

Allowed up to 2 times with maximum temperature of 350°C no longer than 3 seconds.

RPC-1 Classification reflow profile

Profile Feature	Pb-Free Assembly
Preheat/Soak Temperature Min (Tsmin) Temperature Max (Tsmax) Time (ts) from (Tsmin to Tsmax)	 150°C 200°C 60-120 seconds
Ramp-up rate (TL to Tp)	3°C / second maximum
Liquidous temperature (TL) Time (tL) maintained above TL	217°C 60-150 seconds
Peak package body temperature (Tp)	For users Tp must not exceed the classification temp in Table RPC-2. For suppliers Tp must equal or exceed the Classification temp in Table RPC-2.
Time (tp)* within 5°C of the specified classification temperature (Tc), see **Error! Reference source not found.**	30* seconds
Ramp-down rate (Tp to TL)	6°C / second maximum
Time 25°C to peak temperature	8 minutes maximum
* Tolerance for peak profile temperature (Tp) is defined as a supplier minimum and a user maximum.	

Table 23 – RPC-1 Classification reflow profile

All temperatures refer to the center of the package, measured on the package body surface that is facing up during assembly reflow (e.g., live-bug). If parts are reflowed in other than the normal live-bug assembly reflow orientation (i.e., dead-bug), Tp shall be within ±2°C of the live-bug Tp and still meet the Tc requirements, otherwise, the profile shall be adjusted to achieve the latter. To accurately measure actual peak package body temperatures, refer to JEP140 for recommended thermocouple use.

Reflow profiles in this document are for classification/preconditioning and are not meant to specify board assembly profiles. Actual board assembly profiles should be developed based on specific process needs and board designs and should not exceed the parameters in Table RPC-1.

For example, if Tc is 260°C and time tp is 30 seconds, this means the following for the supplier and the user.

For a supplier: The peak temperature must be at least 260°C. The time above 255°C must be at least 30 seconds.

For a user: The peak temperature must not exceed 260°C. The time above 255°C must not exceed 30 seconds.

All components in the test load shall meet the classification profile requirements.

RPC-2 Pb-Free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm3, <350	Volume mm3, 350 to 2000	Volume mm3, >2000
<1.6 mm	260°C	260°C	260°C
1.6 mm – 2.5 mm	260°C	250°C	245°C
>2.5 mm	250°C	245°C	245°C

Table 24 – Classification Temperatures

At the discretion of the device manufacturer, but not the board assembler/user, the maximum peak package body temperature (Tp) can exceed the values specified in Table RPC-2. The use of a higher Tp does not change the classification temperature (Tc).

Package volume excludes external terminals (e.g., balls, bumps, lands, leads) and/or nonintegral heat sinks.

The maximum component temperature reached during reflow depends on package thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD packages may still exist.

Ordering Information

Part Number	Description	Package
ES9033Q	SABRE 32-bit 2 Channel DAC with built in line driver & digital filters	5mm x 5mm 28 QFN
ES9033QT • **Inquire for availability**	SABRE 32-bit 2 Channel DAC with built in line driver & digital filters Extended temperature range -40 to 125deg Celsius	5mm x 5mm 28 QFN

Table 25 – Ordering information

Revision History

Current Version [Status]

Rev.	Date	Notes
0.1	April 5, 2021	Initial Release
0.2	April 7, 2021	• Added digital filter frequency and impulse response diagrams • Corrected block diagram • Added register list and register map
0.2.1	April 13, 2021	• Made some register names more descriptive • Changed references to “Serial Configuration Mode” simplified to “Software Mode” • Clarified “0” and “1” in Software Mode section to “GND” and “AVDD” respectively.
0.2.2	June 15, 2021	• Updated formatting in most registers and improved descriptiveness. • Added weak keeper definition to register 24. • Added register information and TDM to Audio Input Format. • Added hardware APLL mode startup sequence. • Added hardware modes 16-31 • Added coloring to register listings
0.2.3	July 22, 2021	• Added HW design information to configuration modes • Added SPI timing diagram • Added I2C timing diagram • Added w/o DRE performance numbers • Added ESD protection ratings • Minor formatting updates
0.3	October 1, 2021	• Unreserved registers 196[7:5][1:0], 203[5:4], 195[7:2], 192[5:3], 193[6] & [4:2], and 200-202[0]. • Updated Register 194, 202-200 descriptions • Added clock configuration tables for I2S and TDM modes • Corrected DRE ON/OFF_THRESHOLD descriptions for Registers 78-81
0.3.1	April 20, 2022	• Updated Register 44 bit descriptions • Updated Register 36 [4:0] descriptions • Removed AVDD pin description reference to 1.8V, ES9033 is a 3.3V device • Added Register 54[1:0] • Updated the Digital Signal Path diagram • Updated BCK column for I2S Slave Clock Rate Configurations table • Minor typing corrections • Reserved Registers 233-236 • Added note for register 45[7] DSD_2DB_DOWN regarding RUN_VOLUME • Updated Register 202-200[13:1] descriptions • Removed APLL modes section