Analog Reinvented

ES9018S
Reference 32-bit Audio DAC
Product Datasheet

The ***SABRE[32] Reference*** audio DAC series is the world's highest performance 32-bit audio DAC solution targeted for consumer applications such as Blu-ray players, audio pre-amplifiers, A/V receivers and professional applications such as recording systems, mixer consoles and digital audio workstations.

Part Number	Description	Package	DNR (dB)	THD (dB)	32-bit DAC	I²S / DSD Input	SPDIF Input	Jitter Reduction
ES9018	***SABRE[32] Reference 8-Channel* Audio DAC**	64-LQFP	135 (mono) 129 (8-Ch)	–120	Yes	Yes	Yes	Yes

With ESS' patented 32-bit HyperStream™ DAC architecture and Time Domain Jitter Eliminator, the ***SABRE[32] Reference Stereo DAC*** delivers an unprecedented DNR of up to 135dB and THD+N of –120dB, the industry's highest performance level that will satisfy the most demanding audio enthusiasts.

The ***SABRE[32] Reference*** audio DAC's 32-bit HyperStream™ architecture can handle full 32-bit PCM data via I²S input, as well as DSD or SPDIF data. The ***SABRE[32] Reference*** supports up to 1.536MHz input sampling rates and consumes less than 100mW.

The ***SABRE[32] Reference DACs*** set the standard for HD audio performance, **SABRE SOUND™**, in a cost-effective, easy-to-use form factor for today's most demanding digital-audio applications.

Feature	Description
Patented 32-bit HyperStream™ DAC ○ Up to 135dB DNR –120dB THD+N	Industry's highest performance 32-bit audio DAC with unprecedented dynamic range and ultra-low distortion
Patented Time Domain Jitter Eliminator	Unmatched audio clarity free from input clock jitter
64-bit accumulator and 32-bit processing	Distortion free signal processing
Universal digital input for up to 1.536MHz[1] sampling rate	Supports SPDIF, PCM (I²S, MSB / LSB justified 16-32-bit) or DSD input with DVD Audio and SACD compatibility.
Integrated DSP functions	Click-free soft mute and volume control Programmable filter characteristics for PCM / DSD Programmable Zero detect De-emphasis for 32kHz, 44.1kHz, and 48kHz sampling
Customizable output configuration	Mono, stereo, 8-channel output in current- or voltage-mode based on performance criterion
Customizable filter characteristics	User-programmable filter allowing custom roll-off response
100mW power consumption	Simplifies power supply design

APPLICATIONS

- Blu-ray / SACD / DVD-Audio player
- A/V processor
- Digital audio workstation
- Audio preamplifier and receiver
- Professional audio recording systems and mixing consoles

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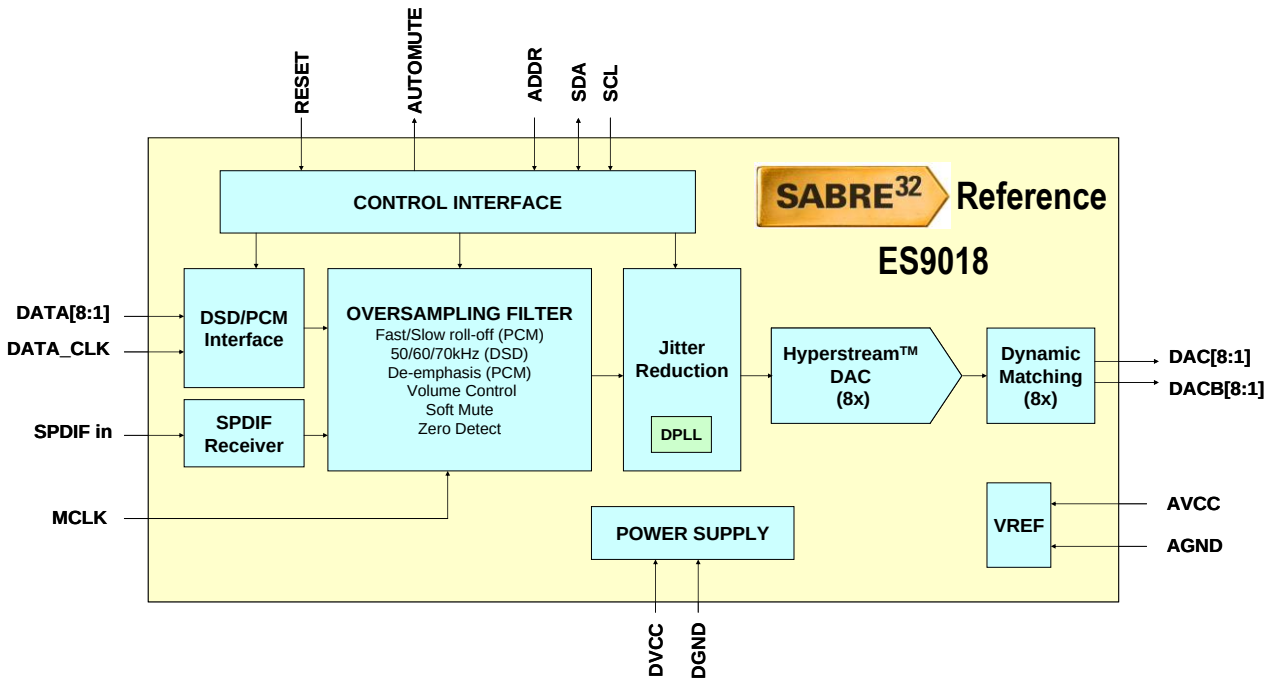


Figure 1 - Functional Block Diagram

Application Diagram

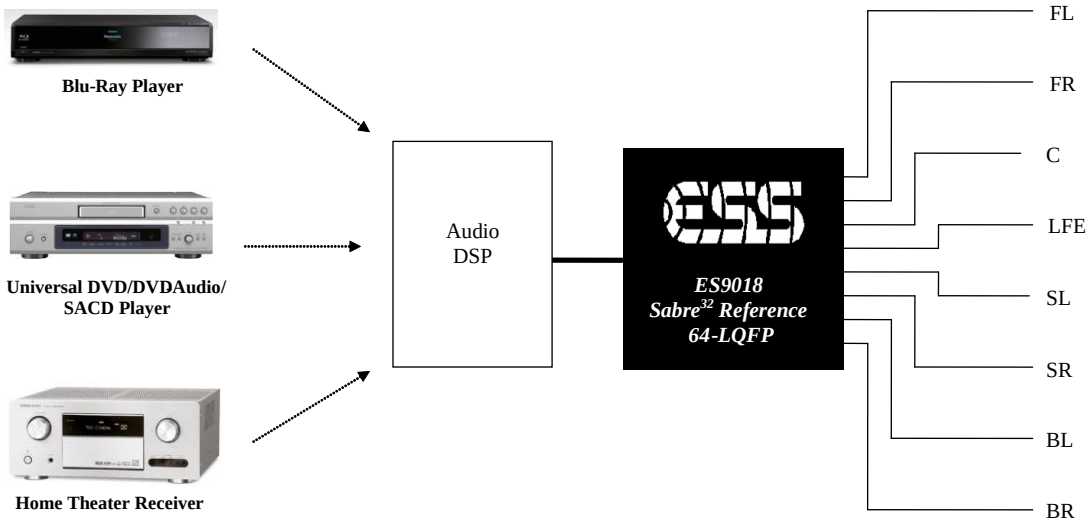


Figure 2 - Application Diagram

Pin Layout

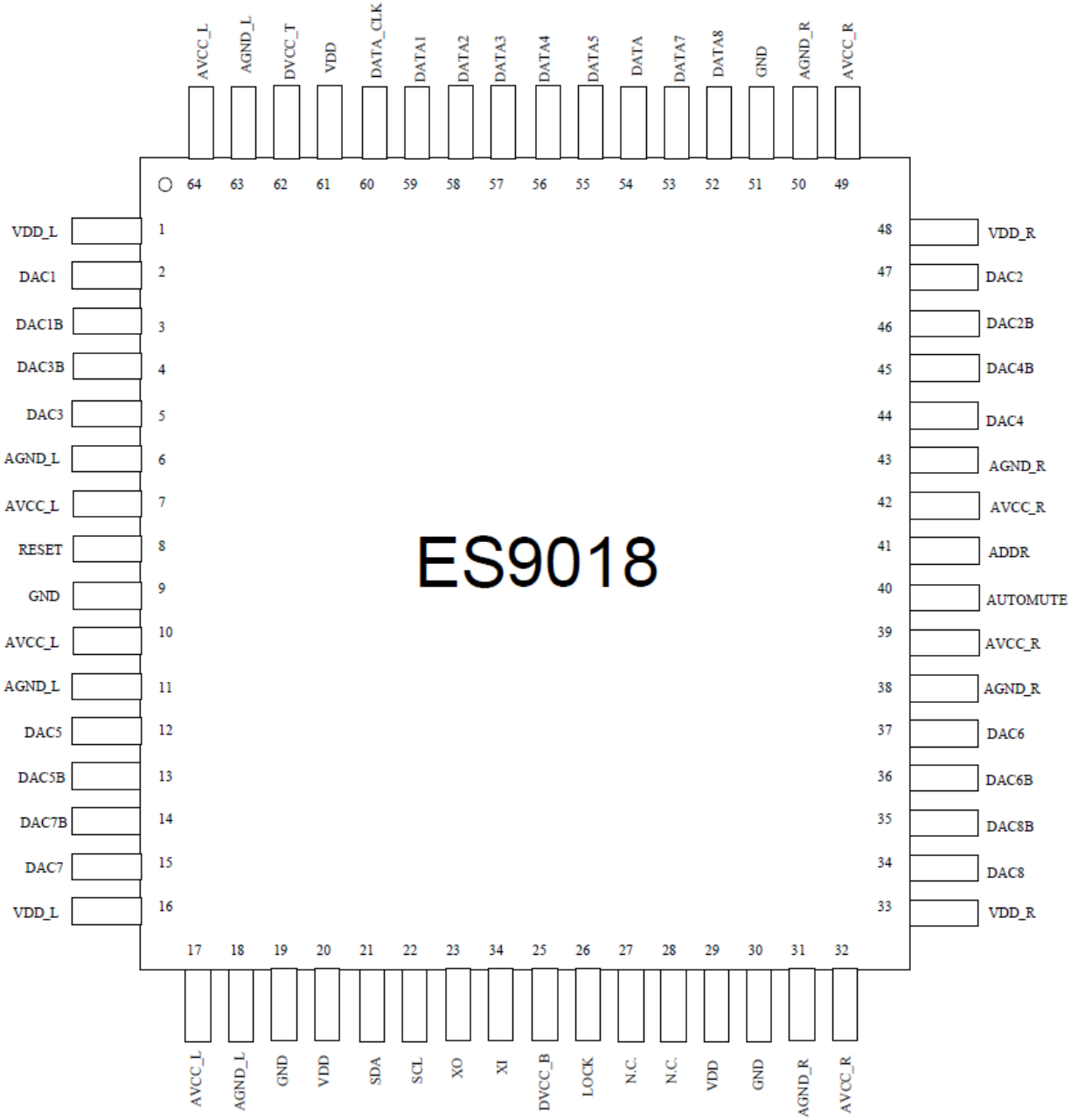


Figure 3 – Pin Layout

Pin Descriptions

Pin	Name	I/O	Description
1	VDD_L	-	Analog Power (+1.2V) for Left channels
2	DAC1	O	Differential Positive Analog Output 1
3	DAC1B	O	Differential Negative Analog Output 1
4	DAC3B	O	Differential Negative Analog Output 3
5	DAC3	O	Differential Positive Analog Output 3
6	AGND_L	-	Analog Ground for Left channels
7	AVCC_L	-	Analog Power (+3.3V) for Left channels
8	RESET	I	Global Reset Input, Active High
9	GND	-	Digital Ground
10	AVCC_L	-	Analog Power (+3.3V) for Left channels
11	AGND_L	-	Analog Ground for Left channels
12	DAC5	O	Differential Positive Analog Output 5
13	DAC5B	O	Differential Negative Analog Output 5
14	DAC7B	O	Differential Negative Analog Output 7
15	DAC7	O	Differential Positive Analog Output 7
16	VDD_L	-	Analog Power (+1.2V) for Left channels
17	AVCC_L	-	Analog Power (+3.3V) for Left channels
18	AGND_L	-	Analog Ground for Left channels
19	GND	-	Digital Ground
20	VDD	-	Digital Power (+1.2V) for core of chip
21	SDA	I/O	I^2C Serial Data Input / Output
22	SCL	I	I^2C Serial Clock Input
23	XO	O	Crystal oscillator output
24	XI (MCLK)	I	Crystal oscillator input (Note: can also just be a clock input)
25	DVCC_B	-	Digital Power (+3.3V) for bottom pad ring of chip
26	LOCK	O	Lock output
27	N.C.		Not connected (leave open)
28	N.C.		Not connected (leave open)
29	VDD	-	Digital Power (+1.2V) for core of chip
30	GND	-	Digital Ground
31	AGND_R	-	Analog Ground for Right channels
32	AVCC_R	-	Analog Power (+3.3V) for Right channels
33	VDD_R	-	Analog Power (+1.2V) for Right channels
34	DAC8	O	Differential Positive Analog Output 8
35	DAC8B	O	Differential Negative Analog Output 8
36	DAC6B	O	Differential Negative Analog Output 6
37	DAC6	O	Differential Positive Analog Output 6
38	AGND_R	-	Analog Ground for Right channels
39	AVCC_R	-	Analog Power (+3.3V) for Right channels
40	AUTMOMUTE	O	Automute
41	ADDR	I	Chip Address Select

42	AVCC_R	-	Analog Power (+3.3V) for Right channels
43	AGND_R	-	Analog Ground for Right channels
44	DAC4	O	Differential Positive Analog Output 4
45	DAC4B	O	Differential Negative Analog Output 4
46	DAC2B	O	Differential Negative Analog Output 2
47	DAC2	O	Differential Positive Analog Output 2
48	VDD_R	-	Analog Power (+1.2V) for Right channels
49	AVCC_R	-	Analog Power (+3.3V) for Right channels
50	AGND_R	-	Analog Ground for Right channels
51	GND	-	Digital Ground
52	DATA8	I	DSD Data8 OR SPDIF Input8
53	DATA7	I	DSD Data7 OR SPDIF Input7
54	DATA6	I	DSD Data6 OR SPDIF Input6
55	DATA5	I	DSD Data5 OR PCM Data CH7/CH8 OR SPDIF Input5
56	DATA4	I	DSD Data4 OR PCM Data CH5/CH6 OR SPDIF Input4
57	DATA3	I	DSD Data3 OR PCM Data CH3/CH4 OR SPDIF Input3
58	DATA2	I	DSD Data2 OR PCM Data CH1/CH2 OR SPDIF Input2
59	DATA1	I	DSD Data1 OR PCM Frame Clock OR SPDIF Input1
60	DATA_CLK	I	PCM Bit Clock OR DSD Bit Clock
61	VDD	-	Digital Power (+1.2V) for core of chip
62	DVCC_T	-	Digital Power (+3.3V) for top pad ring of chip
63	AGND_L	-	Analog Ground for Left channels
64	AVCC_L	-	Analog Power (+3.3V) for Left channels

Table 1 - Pin Descriptions

5V Tolerant Pins

The following pins are 5V tolerant:

- DATA_CLK
- DATA 1-8
- SCL
- SDA
- ADDR
- RESET

Functional Descriptions

Notations for Sampling Rates

Mode	fs	Fs
DSD	DATA_CLK / 64	DSD data rate
Serial (PCM) Normal Mode	DATA_CLK / 64	DATA_CLK / 64
Serial (PCM) OSF Bypass Mode	DATA_CLK / 8	DATA_CLK / 8
SPDIF	SPDIF Sampling Rate	SPDIF Sampling Rate

Table 2 - Notations for Sampling Rates

PCM, SPDIF and DSD Pin Connections

The following tables show how the pins are used for PCM and DSD audio formats.

PCM Audio Format

Notes:

- *XI clock (MCLK) must be > 192 x Fs (for Fs ≤ 200kHz) when using PCM input (normal mode)*
- *XI clock (MCLK) must be > 256 x Fs (200kHz < Fs ≤ 384kHz) when using PCM input (normal mode)*
- *XI clock (MCLK) must be > 24 x Fs (Fs ≤ 1.536MHz) when using PCM input (OSF bypass mode)*

Pin Name	Description
DATA1	Frame clock
DATA[2:5]	8-channel PCM serial data
DATA_CLK	Bit clock for PCM audio format

Table 3 - PCM pin connections

SPDIF Audio Formant

Note: XI clock (MCLK) must be > 386 x Fs (for Fs ≤ 200kHz) when using SPDIF input

Pin Name	Description
DATA[1:8]	Up to 8 SPDIF inputs can be connected to an 8-to-1 mux internal to ***SABRE[32] Reference***, selectable via register SPDIF Source

Table 4 - SPDIF pin connections

DSD Audio Format

Note: XI clock (MCLK) must be > 3 x Fs (Fs = 2.8224MHz x1, x2, or x4) when using DSD input

Pin Name	Description
DATA[1:8]	8-channel DSD data input
DATA_CLK	Bit clock for DSD data input

Table 5 - DSD pin connections

Feature Descriptions

Soft Mute

When Mute is asserted the output signal will ramp to the –∞ level. When Mute is reset the attenuation level will ramp back up to the previous level set by the volume control register. Asserting Mute will not change the value of the volume control register. The ramp rate is 0.0078125 x fs dB/s, where fs = DATA_CLK / 64 in PCM serial or DSD modes, or SPDIF sampling rate in SPDIF mode.

Automute

During an automute condition the ramping of the volume of each DAC to –∞ can now be programmatically enabled or disabled.

- In PCM serial mode, "AUTOMUTE" will become active once the audio data is continuously below the threshold set by <Register Automute_lev>, for a length of time defined by 2096896 / (<Register#9> x DATA_CLK) Seconds.
- In SPDIF mode, "AUTOMUTE" will become active once the audio data is continuously below the threshold set by <Register Automute_lev>, for a length of time defined by 2096896 / (<Register#9> x (64 x Fs) Seconds, where Fs is the SPDIF sampling rate.
- In the DSD Mode, "AUTOMUTE" will become active when any 8 consecutive values in the DSD stream have as many 1's and 0's for a length of time defined by 2096896 / (<Register Automute_time> x DATA_CLK) Seconds. The following table summarizes the conditions.

Mode	Detection Condition	Time
PCM	Data is continuously lower than <Register Automute_lev>	2096896 / (<Register Automute_time > x DATA_CLK)
SPDIF	Data is continuously lower than <Register Automute_lev>	2096896 / (<Register Automute_time > x (64 x Fs)) where Fs is the SPDIF sampling rate
DSD	Equal number of 1s and 0s in every 8 bits of data	2096896 / (<Register Automute_time > x DATA_CLK)

Table 6 - Automute configurations

Volume Control

Each output channel has its own attenuation circuit. The attenuation for each channel is controlled independently. Each channel can be attenuated from 0dB to –127dB in 0.5dB steps.

Each 0.5dB step transition takes 64 intermediate levels. The result being that the level changes are done using small enough steps so that no switching noise occurs during the transition of the volume control. When a new volume level is set, the attenuation circuit will ramp softly to the new level.

Master Trim

The master trim sets the 0dB reference level for the volume control of each DAC. The master trim is programmable via registers 20-23 and is a 32bit signed number. Therefore it should never exceed 32'h7FFFFFFF (as this is full-scale signed).

All Mono Mode

The SABRE32 can be put into an all mono mode where all eight DACs are driven from the same source. This can be useful for high-end audio applications. The source data for all eight DACs can be programmatically configured to be either PCM CH1 or CH2.

De-emphasis

The de-emphasis feature is included for audio data that has utilized the 50/15μs pre-emphasis for noise reduction. There are three de-emphasis filters, one for 32kHz, one for 44.1kHz, and one for 48kHz.

The de-emphasis filter can automatically be applied when an SPDIF stream sets the de-emphasis flag. It will auto detect the sample rate (32k, 44.1k, 48k) in either consumer or professional formats and then apply the correct de-emphasis filter. The automatic enabling of the de-emphasis filter can be disabled in Register 17 <en_auto>.

OSF Bypass

The oversampling FIR filter can be bypassed, sourcing data directly into the IIR filter. ESS recommends using 8 x Fs as the input. For example, an external signal at 44.1kHz can be oversampled externally to 8 x 44.1kHz = 352.8kHz and then applied to the serial decoder in either I²S, LJ or RJ format. The maximum sample rate that can be applied is 1.536MHz (8 x 192kHz).

SPDIF Data Select

An SPDIF source multiplexer allows for up to eight SPDIF sources to be connected to the data pins on the ***SABRE[32] Reference***. The ***SABRE[32] Reference*** uses an internal programmable register to select the appropriate data pin to decode.

SPDIF input can be automatically decoded when there is valid SPDIF data if Register 17 <spdif_autodetect> is enabled.

Programmable Filter

The FIR filter can be programmed with custom coefficients to achieve an arbitrary frequency response that suits the needs of the product. The two stage interpolated filter exploits the symmetry of the coefficients to achieve a very sharp frequency response while using only 64 coefficients for the stage one filter and 14 coefficients for the stage two filter. Custom coefficients can be enabled via register 37 <prog_coeff_enabled> and can be programmed via the method explained in the FIR Programmable Filters section.

The length of the stage 2 filter is configurable to either 27 or 28 coefficients via register 17 <fir_length>.

System Clock (XI / MCLK)

A system clock is required for proper operation of the digital filters and modulation circuitry. Maximum MCLK frequency is 100MHz. The system clock must also satisfy:

Data Type	Valid MCLK Frequencies
DSD Data	100MHz > MCLK > 3 x Fs, Fs = 2.8224MHz (x 1, 2, or 4)
Serial Normal Mode	100MHz > MCLK > 192 x Fs, Fs ≤ 200kHz, or 100MHz > MCLK > 256 x Fs, 200kHz < Fs ≤ 384kHz
Serial OSF Bypass Mode	100MHz > MCLK > 24 x Fs, Fs ≤ 1.536MHz
SPDIF Data	100MHz > MCLK > 386 x Fs, Fs ≤ 200kHz

Table 7 - MCLK configurations

Data Clock

DATA_CLOCK must be 64 x Fs for SERIAL, Fs for DSD modes, and is not required for SPDIF mode. This pin should be pulled low if not used.

Built-in Digital Filters

There are numerous applications for a stereo DAC so for added flexibility; two digital filter settings are possible, sharp roll-off and a slow roll-off for PCM mode. For DSD mode, there are four available filters with cutoffs at 47kHz, 50kHz, 60kHz, and 70kHz.

Sample Rate Calculation

The DPLL number can be read back from the ***SABRE^{32} Reference***, allowing for calculation of the sample rate. The sample rate can be calculated using: $F_{in} = (DPLL\_NUM \times F_{crystal}) / 2^{32}$. F_{in} must be divided by 64 for I^2S data.

DAC-bar Phase

Each DAC-bar phase can be configured to be in phase with DAC. This allows for the outputs of the DAC to be summed to drive an amplifier.

DPLL Lock Reset

The DPLL can be forced to relock, which is useful when the sample rate has been changed. This can be done by setting Register 17 <dpll_lock_rst_reg> high to force the reset, and then low to resume normal operation.

DPLL Frequency Phase Flip

The DPLL can be set to lock to either the rising or falling edge of the clock. This can be set using Register 17 <fin_phase_flip>.

PCM Audio Interface Formats

Several interface formats are provided so that direct connection to common audio processors is possible. The available formats and their accompanying diagrams are listed in the following table. The audio interface format can be set by programming the registers.

Format	Description	Figure
0	MSB First, Left Justified, up to 32-bit data	1A
1	I^2S, up to 32-bit data	3A
2	MSB First, Right Justified, 32-bit data	2A
3	MSB First, Right Justified, 24-bit data	2B
4	MSB First, Right Justified, 20-bit data	2C
5	MSB First, Right Justified, 16-bit data	2D
6	DSD Normal Mode	4A
7	DSD Phase Mode	4B

Table 8 - PCM Audio Interface Formats

Audio Interface Formats

Several interface formats are provided so that direct connection to common audio processors is possible. The available formats are shown in the following diagrams. The audio interface format can be set by programming the registers.

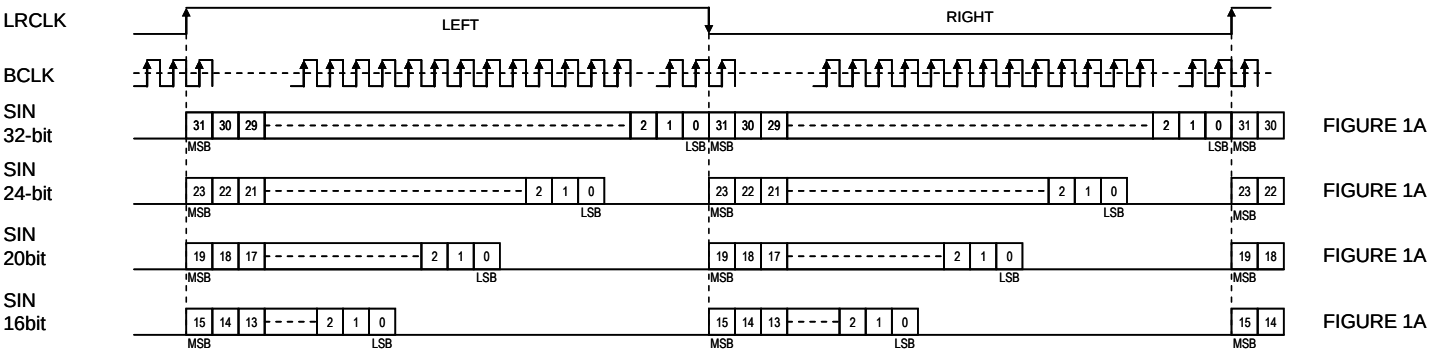


FIGURE 1A

LEFT JUSTIFIED FORMAT

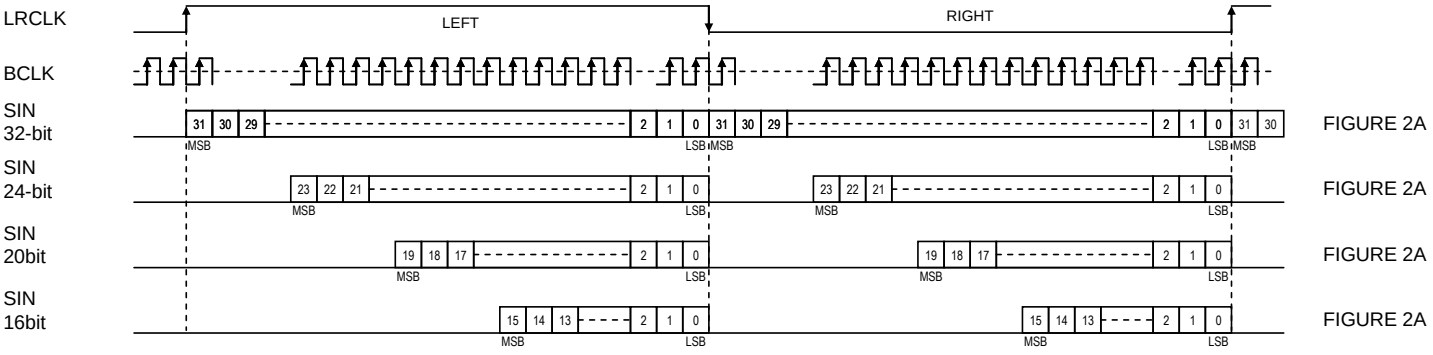


FIGURE 2A

RIGHT JUSTIFIED FORMAT

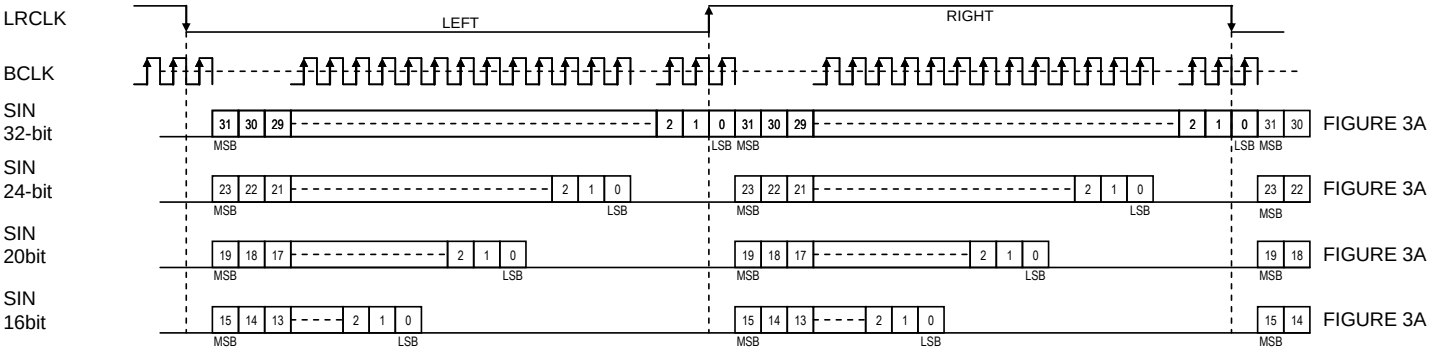


FIGURE 3A

I2S FORMAT

FIGURE 4A

DSD NORMAL MODE

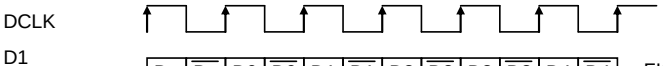


FIGURE 4B

DSD PHASE MODE

Figure 4 - Audio Interface Formats

Serial Control Interface

The registers inside the chip are programmed via an I²C interface. The diagram below shows the timing for this interface. The chip address can be set to 2 different settings via the "ADDR" pin. Table 7 below summarizes this.

ADDR	CHIP ADDRESS
0	0x90
1	0x92

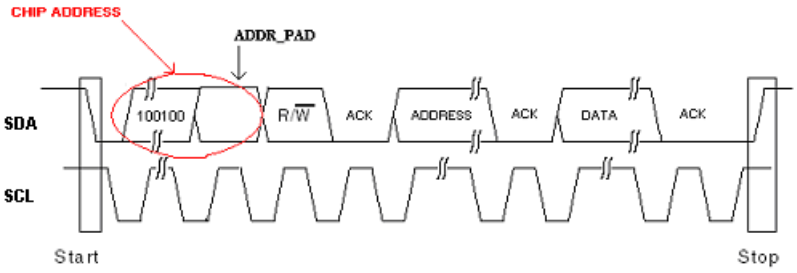
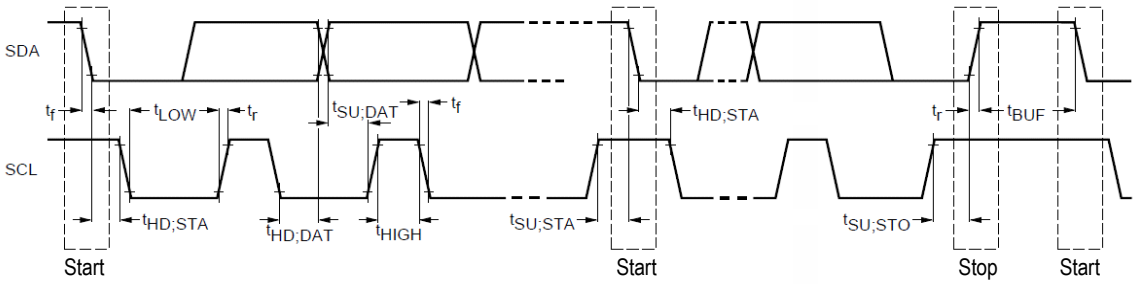


Figure 5 - I2C Addresses

Notes:
The "ADDR" pin is used to create the CHIP ADDRESS. (0x90, 0x92)
The first byte after the chip address is the "ADDRESS" this is the register address.
The second byte after the CHIP ADDRESS is the "DATA" this is the data to be programmed into the register at the previous "ADDRESS".
Compatible with I²C-bus specification version 2.1 Standard-mode/Fast-mode.



Parameter	Symbol	Standard-Mode		Fast-Mode		Unit
		MIN	MAX	MIN	MAX	
SCL Clock Frequency	f_{SCL}	0	100	0	400	kHz
START condition hold time	$t_{HD,STA}$	4.0	-	0.6	-	µs
LOW period of SCL	t_{LOW}	4.7	-	1.3	-	µs
HIGH period of SCL	t_{HIGH}	4.0	-	0.6	-	µs
START condition setup time (repeat)	$t_{SU,STA}$	4.7	-	0.6	-	µs
SDA hold time from SCL falling	$t_{HD,DAT}$	0.3	-	0.3	-	µs
SDA setup time from SCL rising	$t_{SU,DAT}$	250	-	100	-	ns
Rise time of SDA and SCL	t_r	-	1000		300	ns
Fall time of SDA and SCL	t_f	-	300		300	ns
STOP condition setup time	$t_{SU,STO}$	4	-	0.6	-	µs
Bus free time between transmissions	t_{BUF}	4.7	-	1.3	-	µs
Capacitive load for each bus line	C_b	-	400	-	400	pF

Figure 6 - I2C timing

Register Map

Addr (Hex)	Addr (Dec)	Register	7	6	5	4	3	2	1	0
0x0	0	VOLUME OF DAC 0	VOLUME_DAC0							
0x1	1	VOLUME OF DAC 1	VOLUME_DAC1							
0x2	2	VOLUME OF DAC 2	VOLUME_DAC2							
0x3	3	VOLUME OF DAC 3	VOLUME_DAC3							
0x4	4	VOLUME OF DAC 4	VOLUME_DAC4							
0x5	5	VOLUME OF DAC 5	VOLUME_DAC5							
0x6	6	VOLUME OF DAC 6	VOLUME_DAC6							
0x7	7	VOLUME OF DAC 7	VOLUME_DAC7							
0x8	8	AUTOMUTE LEVEL	SPDIF_ENABLE	AUTOMUTE_LEVEL						
0x9	9	AUTOMUTE TIME	AUTOMUTE_TIME							
0xA	10	MODE CONTROL 1	SERIAL_DATA_LENGTH		SERIAL_DATA_MODE		RESERVED	JITTER_REDUCTION_ENABLE	BYPASS_DEEMPHASIS_FILTER	MUTE_DAC
0xB	11	MODE CONTROL 2	RESERVED			DPLL_BANDWIDTH			DE_EMPHASIS_SELECT	
0xC	12	RESERVED	RESERVED							
0xD	13	DAC POLARITY	POLARITY_DAC8	POLARITY_DAC7	POLARITY_DAC6	POLARITY_DAC5	POLARITY_DAC4	POLARITY_DAC3	POLARITY_DAC2	POLARITY_DAC1
0xE	14	IIR BANDWIDTH AND FIR ROLLOFF	SOURCE_DAC8	SOURCE_DAC7	SOURCE_DAC4	SOURCE_DAC3	RESERVED	IIR_BANDWIDTH		FIR_ROLLOFF_SPEED
0xF	15	RESERVED	RESERVED							
0x10	16	AUTOMUTE LOOPBACK	RESERVED				AUTOMUTE_LOOPBACK	RESERVED		
0x11	17	MODE CONTROL 5	MONO_CH_SEL	OSF_BYPASS	DPLL_LOCK_RST_REG	AUTO_DEEMPH	SPDIF_AUTODETECT	FIR_LENGTH	FIN_PHASE_FLIP	ALL_MONO
0x12	18	SPDIF SOURCE	SPDIF_SOURCE							
0x13	19	DACB POLARITY	POLARITY_DAC8B	POLARITY_DAC7B	POLARITY_DAC6B	POLARITY_DAC5B	POLARITY_DAC4B	POLARITY_DAC3B	POLARITY_DAC2B	POLARITY_DAC1B
0x14	20	MASTER TRIM	MASTER_TRIM							
0x15	21	MASTER TRIM	MASTER_TRIM							
0x16	22	MASTER TRIM	MASTER_TRIM							
0x17	23	MASTER TRIM	MASTER_TRIM							
0x18	24	PHASE SHIFT	RESERVED				PHASE_SHIFT			
0x19	25	DPLL MODE CONTROL	RESERVED						DPLL_BW_DEFAULTS	DPLL_BW_128X
0x1A	26	RESERVED	RESERVED							
0x1B	27	STATUS	RESERVED				DSD_PCM	SPDIF_VALID	SPDIF_EN	LOCK
0x1C	28	DPLL NUM	DPLL_NUM							
0x1D	29	DPLL NUM	DPLL_NUM							
0x1E	30	DPLL NUM	DPLL_NUM							
0x1F	31	DPLL NUM	DPLL_NUM							
0x25	37	FIR COEFFICIENTS	RESERVED		STAGE1_PROG_COEFF_ENABLED	STAGE1_PROGRAMMING_ENABLED	RESERVED		STAGE2_PROG_COEFF_ENABLED	STAGE2_PROGRAMMING_ENABLED
0x26	38	STAGE 1 FIR COEFFICIENTS	STAGE1_FIR_COEFFICIENTS							
0x27	39	STAGE 1 FIR COEFFICIENTS	STAGE1_FIR_COEFFICIENTS							
0x28	40	STAGE 1 FIR COEFFICIENTS	STAGE1_FIR_COEFFICIENTS							
0x29	41	STAGE 1 FIR COEFFICIENTS	STAGE1_FIR_COEFFICIENTS							
0x2A	42	RESERVED	RESERVED							
0x2B	43	RESERVED	RESERVED							
0x2C	44	RESERVED	RESERVED							
0x2D	45	RESERVED	RESERVED							
0x30	48	SPDIF CHANNEL STATUS DATA	SPDIF_CHANNEL_STATUS_DATA							
0x31	49	SPDIF CHANNEL STATUS DATA	SPDIF_CHANNEL_STATUS_DATA							
0x32	50	SPDIF CHANNEL STATUS DATA	SPDIF_CHANNEL_STATUS_DATA							
0x33	51	SPDIF CHANNEL STATUS DATA	SPDIF_CHANNEL_STATUS_DATA							
0x34	52	SPDIF CHANNEL STATUS DATA	SPDIF_CHANNEL_STATUS_DATA							
0x35	53	SPDIF CHANNEL STATUS DATA	SPDIF_CHANNEL_STATUS_DATA							
0x36	54	SPDIF CHANNEL STATUS DATA	SPDIF_CHANNEL_STATUS_DATA							
0x37	55	SPDIF CHANNEL STATUS DATA	SPDIF_CHANNEL_STATUS_DATA							
0x38	56	SPDIF CHANNEL STATUS DATA	SPDIF_CHANNEL_STATUS_DATA							
0x39	57	SPDIF CHANNEL STATUS DATA	SPDIF_CHANNEL_STATUS_DATA							

0x3A	58	SPDIF CHANNEL STATUS DATA	SPDIF_CHANNEL_STATUS_DATA
0x3B	59	SPDIF CHANNEL STATUS DATA	SPDIF_CHANNEL_STATUS_DATA
0x3C	60	SPDIF CHANNEL STATUS DATA	SPDIF_CHANNEL_STATUS_DATA
0x3D	61	SPDIF CHANNEL STATUS DATA	SPDIF_CHANNEL_STATUS_DATA
0x3E	62	SPDIF CHANNEL STATUS DATA	SPDIF_CHANNEL_STATUS_DATA
0x3F	63	SPDIF CHANNEL STATUS DATA	SPDIF_CHANNEL_STATUS_DATA
0x40	64	SPDIF CHANNEL STATUS DATA	SPDIF_CHANNEL_STATUS_DATA
0x41	65	SPDIF CHANNEL STATUS DATA	SPDIF_CHANNEL_STATUS_DATA
0x42	66	SPDIF CHANNEL STATUS DATA	SPDIF_CHANNEL_STATUS_DATA
0x43	67	SPDIF CHANNEL STATUS DATA	SPDIF_CHANNEL_STATUS_DATA
0x44	68	SPDIF CHANNEL STATUS DATA	SPDIF_CHANNEL_STATUS_DATA
0x45	69	SPDIF CHANNEL STATUS DATA	SPDIF_CHANNEL_STATUS_DATA
0x46	70	SPDIF CHANNEL STATUS DATA	SPDIF_CHANNEL_STATUS_DATA
0x47	71	SPDIF CHANNEL STATUS DATA	SPDIF_CHANNEL_STATUS_DATA

Register Listing

Read Write Registers

Register 0: VOLUME OF DAC 0

Bits	[7:0]
Default	8'd0

Bits	Mnemonic	Description
[7:0]	VOLUME_DAC0	Volume in dBs = -REG_VALUE/2

Register 1: VOLUME OF DAC 1

Bits	[7:0]
Default	8'd0

Bits	Mnemonic	Description
[7:0]	VOLUME_DAC1	Volume in dBs = -REG_VALUE/2

Register 2: VOLUME OF DAC 2

Bits	[7:0]
Default	8'd0

Bits	Mnemonic	Description
[7:0]	VOLUME_DAC2	Volume in dBs = -REG_VALUE/2

Register 3: VOLUME OF DAC 3

Bits	[7:0]
Default	8'd0

Bits	Mnemonic	Description
[7:0]	VOLUME_DAC3	Volume in dBs = -REG_VALUE/2

Register 4: VOLUME OF DAC 4

Bits	[7:0]
Default	8'd0

Bits	Mnemonic	Description
[7:0]	VOLUME_DAC4	Volume in dBs = -REG_VALUE/2

Register 5: VOLUME OF DAC 5

Bits	[7:0]
Default	8'd0

Bits	Mnemonic	Description
[7:0]	VOLUME_DAC5	Volume in dBs = -REG_VALUE/2

Register 6: VOLUME OF DAC 6

Bits	[7:0]
Default	8'd0

Bits	Mnemonic	Description
[7:0]	VOLUME_DAC6	Volume in dBs = -REG_VALUE/2

Register 7: VOLUME OF DAC 7

Bits	[7:0]
Default	8'd0

Bits	Mnemonic	Description
[7:0]	VOLUME_DAC7	Volume in dBs = -REG_VALUE/2

Register 8: AUTOMUTE LEVEL

Bits	[7]	[6:0]
Default	1'b0	7'd104

Bits	Mnemonic	Description
[7]	SPDIF_ENABLE	SPDIF input select. • 1'b0: Use either I2S or DSD input • 1'b1: Use SPDIF input
[6:0]	AUTOMUTE_LEVEL	Automute trigger point select. Automute trigger point in dB's = -REG_VALUE

Register 9: AUTOMUTE TIME

Bits	[7:0]
Default	8'd4

Bits	Mnemonic	Description
[7:0]	AUTOMUTE_TIME	Automute time control. • 8’d0: Longest time • 8’d4: Default • 8’d255: Shortest time •

Register 10: MODE CONTROL 1

Bits	[7:6]	[5:4]	[3]	[2]	[1]	[0]
Default	2'b11	2'b00	1'b1	1'b1	1'b1	1'b0

Bits	Mnemonic	Description
[7:6]	SERIAL_DATA_LENGTH	Serial data length control. • 2'b00: 24 Bit • 2'b01: 20 Bit • 2'b10: 16 Bit • 2'b11: 32 Bit
[5:4]	SERIAL_DATA_MODE	Serial data mode select. • 2'b00: I2S • 2'b01: LJ • 2'b10: RJ • 2'b11: I2S
[3]	RESERVED	NA
[2]	JITTER_REDUCTION_ENABLE	Jitter reduction enable. 1'b0: Bypass and stop JITTER_REDUCTION 1'b1: Use JITTER_REDUCTION
[1]	BYPASS_DEEMPHASIS_FILTER	De-emphasize filter enable. 1'b0: Use De-emphasize filter 1'b1: Bypass De-emphasize filter
[0]	MUTE_DAC	DAC mute control. • 1'b0: Unmute all DACs • 'b1: Mute all DACs

Register 11: MODE CONTROL 2

Bits	[7:5]	[4:2]	[1:0]
Default	3'b100	3'b001	2'b01

Bits	Mnemonic	Description
[7:5]	RESERVED	NA
[4:2]	DPLL_BANDWIDTH	DPLL bandwidth control. • 3'b000: No Bandwidth • 3'b001: Lowest Bandwidth • 3'b010: Low Bandwidth • 3'b011: Med-Low Bandwidth • 3'b100: Medium Bandwidth • 3'b101: Med-High Bandwidth • 3'b110: High Bandwidth • 3'b111: Highest Bandwidth
[1:0]	DE_EMPHASIS_SELECT	De-emphasis frequency select • 2'b00: 32 kHz • 2'b01: 44.1 kHz • 2'b10: 48 kHz • 2'b11: RESERVED

Register 12: RESERVED

Register 13: DAC POLARITY

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	POLARITY_DAC8	Polarity control for DAC 8. • 1'b0: In-Phase • 1'b1: Anti-Phase
[6]	POLARITY_DAC7	Polarity control for DAC 7. • 1'b0: In-Phase • 1'b1: Anti-Phase
[5]	POLARITY_DAC6	Polarity control for DAC 6. • 1'b0: In-Phase • 1'b1: Anti-Phase
[4]	POLARITY_DAC5	Polarity control for DAC 5. • 1'b0: In-Phase • 1'b1: Anti-Phase
[3]	POLARITY_DAC4	Polarity control for DAC 4. • 1'b0: In-Phase • 1'b1: Anti-Phase
[2]	POLARITY_DAC3	Polarity control for DAC 3. • 1'b0: In-Phase • 1'b1: Anti-Phase
[1]	POLARITY_DAC2	Polarity control for DAC 2. • 1'b0: In-Phase • 1'b1: Anti-Phase
[0]	POLARITY_DAC1	Polarity control for DAC 1. • 1'b0: In-Phase • 1'b1: Anti-Phase

Register 14: IIR BANDWIDTH AND FIR ROLLOFF

Bits	[7]	[6]	[5]	[4]	[3]	[2:1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b1	2'b01	1'b1

Bits	Mnemonic	Description
[7]	SOURCE_DAC8	DAC 8 source control. • 1'b0: DAC8 • 1'b1: DAC6
[6]	SOURCE_DAC7	DAC 7 source control. • 1'b0: DAC7 • 1'b1: DAC5
[5]	SOURCE_DAC4	DAC 4 source control. • 1'b0: DAC4 • 1'b1: DAC2
[4]	SOURCE_DAC3	DAC 3 source control. • 1'b0: DAC3 • 1'b1: DAC1
[3]	RESERVED	NA
[2:1]	IIR_BANDWIDTH	IRR bandwidth control. • 2'b00: Normal (for least in-band ripple for PCM data set to Normal) • 2'b01: 50k • 2'b10: 60k • 2'b11: 70k
[0]	FIR_ROLLOFF_SPEED	FIR roll off speed control • 1'b0: Slow Rolloff • 1'b1: Fast Rolloff

Register 15: RESERVED

Register 16: AUTOMUTE LOOPBACK

Bits	[7:4]	[3]	[2:0]
Default	4'd0	1'b0	3'b000

Bits	Mnemonic	Description
[7:4]	RESERVED	NA
[3]	AUTOMUTE_LOOPBACK	Automute volume ramp down control. • 1'b1: Ramp volume to -infinity upon automute condition • 1'b0: Do not ramp volume down upon automute condition
[2:0]	RESERVED	NA

Register 17: MODE CONTROL 5

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b1	1'b1	1'b1	1'b0	1'b0

Bits	Mnemonic	Description
[7]	MONO_CH_SEL	Channel select when ALL_MONO mode is enabled. • 1'b1: Use the right channel when ALL_MONO mode is enabled • 1'b0: Use the left channel when ALL_MONO mode is enabled
[6]	OSF_BYPASS	Polarity control for DAC 7. • 1'b0: Use the OSF filter (normal operation) • 1'b1: Send data directly from the I2S receiver to the IIR filter at 8x. Note: Setting to 1 will cause the signal to bypass the FIR filters as well as the de-emphasis… filter but will still apply to the volume controls.
[5]	DPLL_LOCK_RST_REG	DPLL_LOCK manual override. • 1'b0: Normal Operation • 1'b1: Manually override the DPLL_LOCK. This will force the Jitter Eliminator to relock the signal.
[4]	AUTO_DEEMPH	SPDIF automatic de-emphasis control. • 1'b0: De-emphasis filter is not automatically applied • 1'b1: De-emphasis in SPDIF mode is automatically applied with the correct frequency if 44.1k/48k/32k are detected in the SPDIF channel status bits.
[3]	SPDIF_AUTODETECT	Automatic SPDIF input detection control. • 1'b0: Must manually select SPDIF input. • 1'b1: Automatically detect SPDIF input Note: This should only be set if I2S data will not be applied to the pins
[2]	FIR_LENGTH	2nd stage FIR filter coefficient length control. • 1'b1: 2nd stage FIR filter is 28 coefficients in length • 1'b0: 2nd stage FIR filter is 27 coefficients in length
[1]	FIN_PHASE_FLIP	DPLL phase invert • 1'b0: Do not invert the phase to the DPLL • 1'b1: Invert the phase to the DPLL
[0]	ALL_MONO	Overall DAC true mono source enable. • 1'b0: Normal 8 channel mode • 1'b1: All 8 DACs are sourced from one source for true mono. Note: The channel to use as the source is selected by the MONO_CH_SELECT register.

Register 18: SPDIF SOURCE

Bits	[7:0]
Default	8'd1

Bits	Mnemonic	Description
[7:0]	SPDIF_SOURCE	This register chooses the SPDIF source. The Sabre32 Reference has an 8-to-1 multiplexer which allows up to 8 SPDIF inputs to be connected to the data pins. • 8'd1: data1 • 8'd2: data2 • 8'd4: data3 • 8'd8: data4 • 8'd16: data5 • 8'd32: data6 • 8'd64: data7 • 8'd128: data8

Register 19: DACB POLARITY

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	POLARITY_DAC8B	DAC8 polarity control. • 1'b0: Anti-phase (normal operation) • 1'b1: In-phase
[6]	POLARITY_DAC7B	DAC7 polarity control. • 1'b0: Anti-phase (normal operation) • 1'b1: In-phase
[5]	POLARITY_DAC6B	DAC6 polarity control. • 1'b0: Anti-phase (normal operation) • 1'b1: In-phase
[4]	POLARITY_DAC5B	DAC5 polarity control. • 1'b0: Anti-phase (normal operation) • 1'b1: In-phase
[3]	POLARITY_DAC4B	DAC4 polarity control. • 1'b0: Anti-phase (normal operation) • 1'b1: In-phase
[2]	POLARITY_DAC3B	DAC3 polarity control. • 1'b0: Anti-phase (normal operation) • 1'b1: In-phase
[1]	POLARITY_DAC2B	DAC2 polarity control. • 1'b0: Anti-phase (normal operation) • 1'b1: In-phase
[0]	POLARITY_DAC1B	DAC1 polarity control. • 1'b0: Anti-phase (normal operation) • 1'b1: In-phase

Register 23-20: MASTER TRIM

Bits	[31:0]
Default	32'h7FFFFFFF

Bits	Mnemonic	Description
[31:0]	MASTER_TRIM	This is a 32 bit value that sets the 0dB level for all volume controls. This is a signed number, so it should never exceed 32'h7FFFFFFF (which is 2^31-1). • 32'h00000000: Minimum • 32'h7FFFFFFF: Maximum Note: Register 23 contains the MSBs, Register 20 contains the LSBs

Register 24: PHASE SHIFT

Bits	[7:4]	[3:0]
Default	4'd3	4'd0

Bits	Mnemonic	Description
[7:4]	RESERVED	NA
[3:0]	PHASE_SHIFT	Phase shift control. • 4'd0: default • 4'd1: default + 1/clk delay • 4'd2: default + 2/clk delay • 4'd3: default + 3/clk delay • 4'd4: default + 4/clk delay • 4'd5: default + 5/clk delay • 4'd6: default + 6/clk delay • 4'd7: default + 7/clk delay • 4'd8: default + 8/clk delay • 4'd9: default + 9/clk delay • 4'd10: default + 10/clk delay • 4'd11: default + 11/clk delay • 4'd12: default + 12/clk delay • 4'd13: default + 13/clk delay • 4'd14: default + 14/clk delay • 4'd15: default + 15/clk delay

Register 25: DPLL MODE CONTROL

Bits	[7:2]	[1]	[0]
Default	6'd0	1'b1	1'b0

Bits	Mnemonic	Description
[7:2]	RESERVED	NA
[1]	DPLL_BW_DEFAULTS	DPLL default bandwidth settings. • 1'b1: Use the best DPLL_BANDWIDTH settings. • 1'b0: Allow all settings
[0]	DPLL_BW_128X	• 1'b1: Multiply the DPLL_BANDWIDTH setting by 128 • 1'b0: Use the DPLL_BANDWIDTH setting • 1'b1: Multiply the DPLL_BANDWIDTH setting by 128

Register 26: RESERVED

Read Only Registers

Register 27: STATUS

Bits	[7:4]	[3]	[2]	[1]	[0]
Default	-	-	-	-	-

Bits	Mnemonic	Description
[7:4]	RESERVED	NA
[3]	DSD_PCM	DSD or PCM status bit. • 1'b1: DSD mode • 1'b0: I2S or SPDIF mode
[2]	SPDIF_VALID	Valid SPDIF data status bit. • 1'b1: The SPDIF data is valid • 1'b0: The SPDIF data is invalid
[1]	SPDIF_EN	SPDIF enabled status bit. • 1'b0: SPDIF mode is currently disabled. • 1'b1: SPDIF mode is currently enabled. Note: This can be done manually by setting SPDIF_EN_R (Register 8) or by having SPDIF_AUTODETECT enabled with valid SPDIF data on the input.
[0]	LOCK	Jitter Eliminator lock status bit. • 1'b1:The Jitter Eliminator is locked to an incoming signal • 1'b0: The Jitter Eliminator is not locked to an incoming signal

Register 31-28: DPLL NUM

Bits	[31:0]
Default	-

Bits	Mnemonic	Description
[31:0]	DPLL_NUM	This is a read-only 32 bit value that can be used to calculate the sample rate. The sample rate can be calculated using: Note: Fin must be divided by 64 for I2S data. $F_{in} = \frac{DPLL\_NUM * F_{crystal}}{2^{32}}$

Read Write Registers

Register 37: FIR COEFFICIENTS

Bits	[7:6]	[5]	[4]	[3:2]	[1]	[0]
Default	2'b00	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7:6]	RESERVED	NA
[5]	STAGE1_PROG_COEFF_ENABLED	Stage 1 FIR filter custom coefficient control. • 1'b1: The stage 1 interpolating FIR filter will use the downloaded (custom) coefficients. • 1'b0: The stage 1 interpolating FIR filter will use the built-in coefficients
[4]	STAGE1_PROGRAMMING_ENABLED	Stage 1 coefficients write enable. • 1'b1: The stage 1 coefficients are set for writing. This bit must be enabled prior to programming the stage 1 FIR coefficients. • 1'b0: The stage 1 coefficients are not set for writing
[3:2]	RESERVED	NA
[1]	STAGE2_PROG_COEFF_ENABLED	Stage 2 FIR filter custom coefficient control. • 1'b1: The stage 2 FIR filter will use the downloaded (custom) coefficients. • 1'b0: The stage 2 FIR filter will use the built-in coefficients.
[0]	STAGE2_PROGRAMMING_ENABLED	Stage 2 coefficients write enable. • 1'b1: The stage 2 coefficients are set for writing. This bit must be enabled prior to programming the RESERVED. • 1'b0: The stage 2 coefficients are not set for writing.

Register 41-38: STAGE 1 FIR COEFFICIENTS

Bits	[31:0]
Default	-

Bits	Mnemonic	Description
[31:0]	STAGE1_FIR_COEFFICIENTS	These 32 bits are used for writing the stage 1 FIR coefficients. See the programming section for more information.

Register 45-42: STAGE 2 FIR COEFFICIENTS

Bits	[31:0]
Default	-

Bits	Mnemonic	Description
[31:0]	STAGE2_FIR_COEFFICIENTS	These 32 bits are used for writing the stage 1 FIR coefficients. See the programming section for more information.

Register 71-48: SPDIF CHANNEL STATUS DATA

Bits	[191: 0]
Default	-

Bits	Mnemonic	Description
[191: 0]	SPDIF_CHANNEL_STATUS_DATA	These registers allow read back of the SPDIF channel status. The status definition is different for the customer configuration (Table 7) and professional configuration (Table 8)

SPDIF CHANNEL STATUS - Consumer configuration (Base Address = 48)								
Address Offset	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	Reserved	Reserved	0: 2Channel 1: 4Channel	Reserved	0: No-Preemph 1: Pre-emphasis	0: Copyright 1: Non-Copyright	0: Audio 1: Data	**0: Consumer** 1: Professional
1	Category Code 0x00: General 0x01: Laser-Optical 0x02: D/D Converter 0x03: Magnetic 0x04: Digital Broadcast 0x05: Musical Instrument 0x06: Present A/D Converter 0x08: Solid State Memory 0x16: Future A/D Converter 0x19: DVD 0x40: Experimental							
2	Channel Number 0x0: Don't Care 0x1: A (Left) 0x2: B (Right) 0x3: C 0x4: D 0x5: E 0x6: F 0x7: G 0x8: H 0x9: I 0xA: J 0xB: K 0xC: L 0xD: M 0xE: N 0xF: O				Source Number 0x0:Don't Care 0x1: 1 0x2: 2 0x3: 3 0x4: 4 0x5: 5 0x6: 6 0x7: G 0x8: 8 0x9: 9 0xA: 10 0xB: 11 0xC: 12 0xD: 13 0xE: 14 0xF: 15			
3	Reserved	Reserved	Clock Accuracy 0x0:Level 2 ±1000ppm 0x1:Level 1 ±50ppm 0x2:Level 3 variable pitch shifted		Sample Frequency 0x0: 44.1k 0x2: 48k 0x3: 32k 0x4: 22.05k 0x6: 24k 0x8: 88.2k 0xA: 96k 0xC: 176.4k 0xE: 192k			
4	Reserved	Reserved	Reserved	Reserved	Word Length: If Word Field Size=0 |If Word Field Size = 1 000=Not indicated |000=Not indicated 100 = 23bits |100 = 19bits 010 = 22bits |010 = 18bits 110 = 21bits |110 = 17bits 001 = 20bits |001 = 16bits 101 = 24bits |101 = 20bits			Word Field Size 0: Max 20bits 1: Max 24bits
5-23	Reserved							

SPDIF CHANNEL STATUS - Professional configuration (Base Address = 48)								
Address Offset	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	sampling frequency: 00: not indicated (or see byte 4) 10: 48kHz 01: 44.1kHz 11: 32kHz		lock: 0: locked 1: unlocked	emphasis: 000: Emphasis not indicated 001: No emphasis 011: CD-type emphasis 111: J-17 emphasis			0: Audio 1: Non-audio	0: Consumer **1: Professional**
1	User bit management: 0000: no indication 1000: 192-bit block as channel status 0100: As defined in AES18 1100: user-defined 0010: As in IEC60958-3 (consumer)				Channel mode: 0000: not indicated (default to 2 channel) 1000: 2 channel 0100: 1 channel (monophonic) 1100: primary / secondary 0010: stereo 1010: reserved for user applications 0110: reserved for user applications 1110: SCDSR (see byte 3 for ID) 0001: SCDSR (stereo left) 1001: SCDSR (stereo right) 1111: Multichannel (see byte 3 for ID)			
2	alignment level: 00: not indicated 10: –20dB FS 01: –18.06dB FS		Source Word Length: If max=20bits |If max=24bits 000=Not indicated |000=Not indicated 100 = 23bits |100 = 19bits 010 = 22bits |010 = 18bits 110 = 21bits |110 = 17bits 001 = 20bits |001 = 16bits 101 = 24bits |101 = 20bits			Use of aux sample word: 000: not defined, audio max 20 bits 100: used for main audio, max 24 bits 010: used for coord, audio max 20 bits 110: reserved		
3	Channel identification: if bit 7 = 0 then channel number is 1 plus the numeric value of bits 0-6 (bit reversed). if bit 7 = 1 then bits 4–6 define a multichannel mode and bits 0–3 (bit reversed) give the channel number within that mode.							
4	fs scaling: 0: no scaling 1: apply factor of 1 / 1.001 to value		Sample frequency (fs): 0000: not indicated 0001: 24kHz 0010: 96kHz 1001: 22.05kHz 1010: 88.2kHz 1011: 176.4kHz 0011: 192kHz 1111: User defined			Reserved	DARS (Digital audio reference signal): 00: not a DARS 01: DARS grade 2 (±10ppm) 10: DARS grade 1 (±1ppm) 11: Reserved	
5	Reserved							
6-9	alphanumerical channel origin: four-character label using 7-bit ASCII with no parity. Bits 55, 63, 71, 79 = 0.							
10-13	alphanumerical channel destination: four-character label using 7-bit ASCII with no parity. Bits 87, 95, 103, 111 = 0.							
14-17	local sample address code: 32-bit binary number representing the sample count of the first sample of the channel status block.							
18-21	time of day code: 32-bit binary number representing time of source encoding in samples since midnight							
22	reliability flags 0: data in byte range is reliable 1: data in byte range is unreliable							
23	CRCC 00000000: not implemented X: error check code for bits 0–183							

FIR Programmable Filters

The ***SABRE[32] Reference*** has a two-stage interpolating filter with both built-in and programmable coefficients. Each stage can be programmed and enabled independently. Each channel can also have a different filter per stage.

Each stage of the FIR filter either uses the built-in coefficients, or the programmable coefficients. Register 37 bits 5 and 1 are used for setting the filter coefficient sources.

Programming the filter requires passing every coefficient for all 8 channels to the ***SABRE[32] Reference*** via I²C. Stage 1 and Stage 2 must be programmed independently. Programming starts by enabling the appropriate enable_programming bit in register 37.

The FIR can only be programmed when DATA_CLK is available and when the DAC is locked.

To program stage 1, bit 4 of register 37 must be set high. Then the 32bit coefficients are written to registers 41 (Bits [31:24]), 40 (Bits[23:16]), 39 (Bits[15:8]), 38 (Bits[7:0]) in that order. The first write to these 4 consecutive register is the 32-bit value for Channel1, coefficient1. The next write to these 4 consecutive registers is the 32-bit value for Channel2, coefficient1. After 8 writes to these 4 consecutive registers, coefficient 2 for all 8 filters is ready to be input. There are 64 coefficients to write for Stage 1. So that is 4 bytes per coefficient, 8 channels and 64 coefficients for a total of 2048 bytes to program the stage 1. Once complete, zero must be written to register 38. Bit 4 of register 37 must then be set low to finalize the programming.

To program stage 2, bit 0 of register 37 must be set high. Then the 32bit coefficients are written to registers 45 (Bits [31:24]), 44 (Bits [23:16]), 43 (Bits [15:8]), 42 (Bits [7:0]), in that order. The first write to these 4 consecutive register is the 32-bit value for Channel1, coefficient1. The next write to these 4 consecutive registers is the 32-bit value for Channel2, coefficient1. After 8 writes to these 4 consecutive registers, coefficient 2 for all 8 filters is ready to be input. There are 16 coefficients to write for Stage 2. So that is 4 bytes per coefficient, 8 channels and 16 coefficients for a total of 512 bytes to program the stage 1. Once complete, zero must be written to register 42. Bit 0 of register 37 must then be set low to finalize the programming.

C++ Sample Code for writing custom coefficients to either stage.

```
 void CLoadCoeffDlg::ProgramStage(int nStage)
{
	BYTE WE;
	BYTE WritePort[4];
	BYTE WriteData[4];
	int nTotal;
	if(nStage==0){		//programming stage 1
		WE=0x10;
		WritePort[0]=41;
		WritePort[1]=40;
		WritePort[2]=39;
		WritePort[3]=38;
		nTotal=64;
	}
	else{			//programming stage 2
		WE=0x01;
		WritePort[0]=45;
		WritePort[1]=44;
		WritePort[2]=43;
		WritePort[3]=42;
		nTotal=16;
	}
	if(!m_pParent->WriteRegisters(1, 37, &WE))
		return;
	for(int nCIndex=0; nCIndex<nTotal; nCIndex++){
		for(int nCh=0; nCh<8; nCh++){
			DWORD nCoeff;
			if(nStage==0)
				nCoeff=CoeffCh[nCh].CoeffStage1[nCIndex];
			else
				nCoeff=CoeffCh[nCh].CoeffStage2[nCIndex];
			WriteData[0]=(BYTE)(nCoeff>>24)&0xff;
			WriteData[1]=(BYTE)((nCoeff>>16)&0xff);
			WriteData[2]=(BYTE)((nCoeff>>8)&0xff);
			WriteData[3]=(BYTE)((nCoeff)&0xff);
			if(!m_pParent->WriteRegisters(4, WritePort, WriteData))
				return;
		}
	}
	WE=0x00;
	if(nStage == 0) WriteRegisters(1, 38, &WE);
	else if(nStage == 1) WriteRegisters(1, 42, &WE);
	if(!m_pParent->WriteRegisters(1, 37, &WE));
}
```

Application Diagrams

Recommended Differential, Current-Mode External Op-Amp Circuit

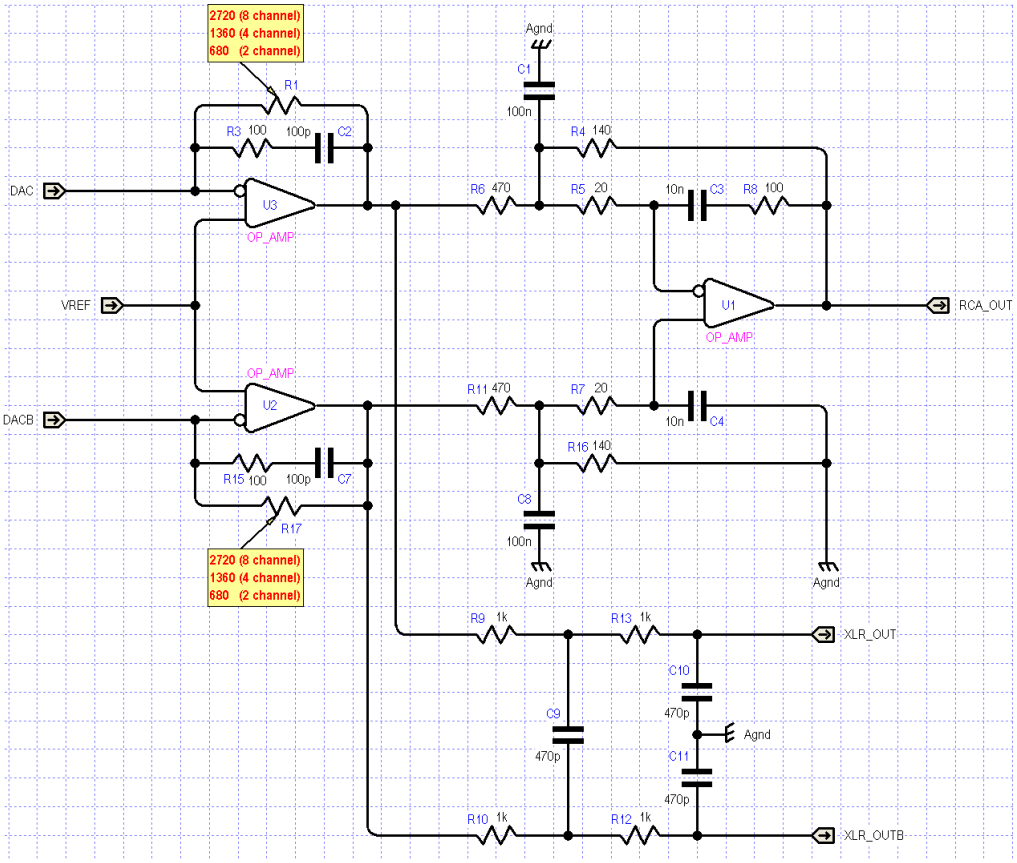


Figure 7 - Recommended Differential, Current-Mode External Op-Amp Circuit

ES9018 Stereo Quad-differential Current Mode

(DNR: 133dB, THD: –120dB)

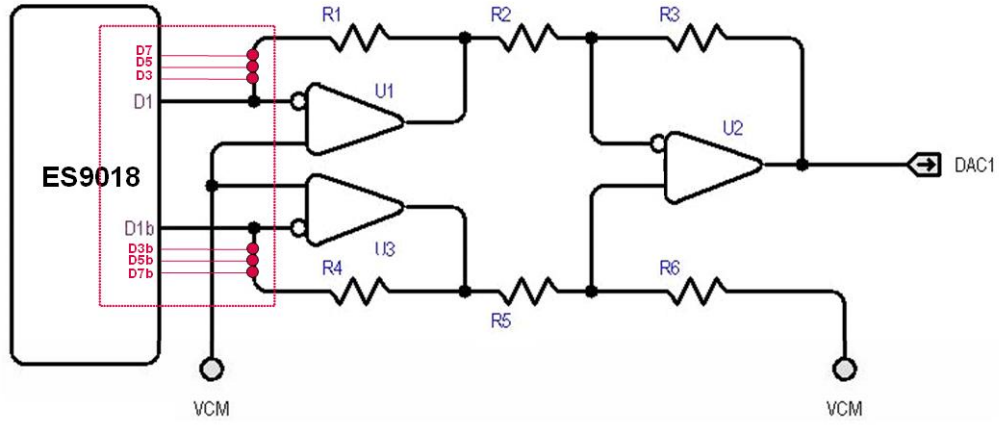


Figure 8 - Sabre 32 Reference DAC in stereo "quad-differential" current mode

(DNR: 129dB, THD: –120dB)

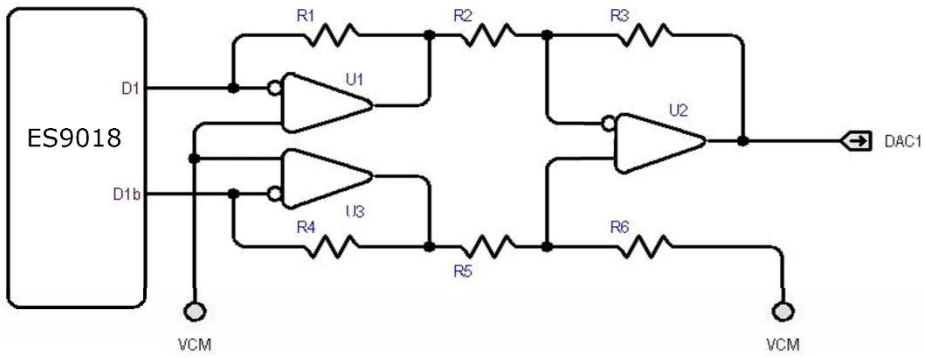


Figure 9 - Sabre32 Reference DAC in 8-Channel differential current mode

Absolute Maximum Ratings

PARAMETER	RATING
Storage temperature	–65°C to +105°C
Voltage range for 5V tolerant pins	–0.5V to +5.5V
Voltage range for all other pins	–0.5V to (DVCC_T+0.5V) or –0.5V to (DVCC_B+0.5V)

Table 9 – Absolute Maximum Ratings

WARNING: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

WARNING: Electrostatic Discharge (ESD) can damage this device. Proper procedures must be followed to avoid ESD when handling this device.

Recommended Operating Conditions

PARAMETER	SYMBOL	CONDITIONS
Operating temperature	T_A	0°C to 70°C
Digital core supply voltage	VDD	1.2V ± 5%, 37mA nominal (Note 1)
Digital power supply voltage	DVCC_T, DVCC_B	3.3V ± 5%, 7mA nominal (Note 1)
Analog power supply voltage	AVCC_L, AVCC_R	3.3V ± 5%, 25mA nominal (Note 1)

Table 10 - Recommended Operating Conditions

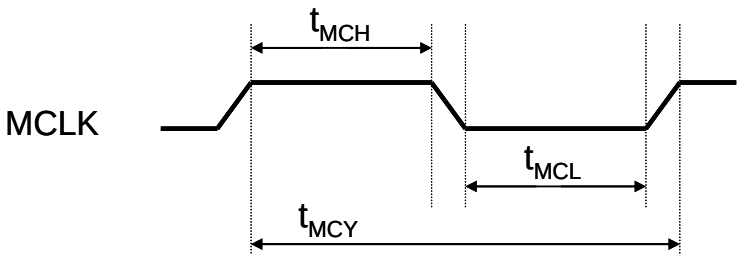
Note: fs = 48kHz, MCLK = 40MHz, I²S input, output unloaded

DC Electrical Characteristics

SYMBOL	PARAMETER	MIN	MAX	UNIT	COMMENTS
V_{IH}	High-level input voltage	2.0	DVCC_T or DVCC_B	V	All inputs TTL levels except CLK and 5V tolerant input pins
		2.0	5.5	V	All 5V tolerant inputs
V_{IL}	Low-level input voltage	–0.3	0.8	V	All input TTL levels except CLK
V_{CLKH}	CLK high-level input	2.0	DVCC_B+0.25	V	TTL level input
V_{CLKL}	CLK low-level input	–0.3	0.8	V	
V_{OH}	High-level output voltage	3.0		V	I_{OH} = 1mA
V_{OL}	Low-level-output voltage		0.45	V	I_{OL} = 4mA
I_{LI}	Input leakage current		±15	µA	
I_{LO}	Output leakage current		±15		
C_{IN}	Input capacitance		10	pF	fc = 1MHz
C_O	Input/output capacitance		12		
C_{CLK}	CLK capacitance		5	pF	fc = 1MHz

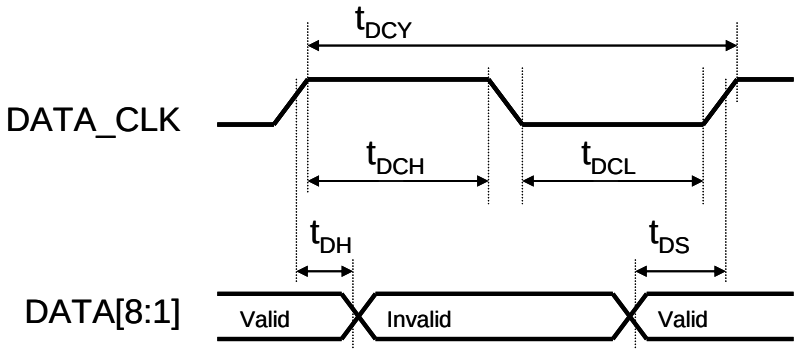
Table 11 - DC Electrical Characteristics

MCLK Timing



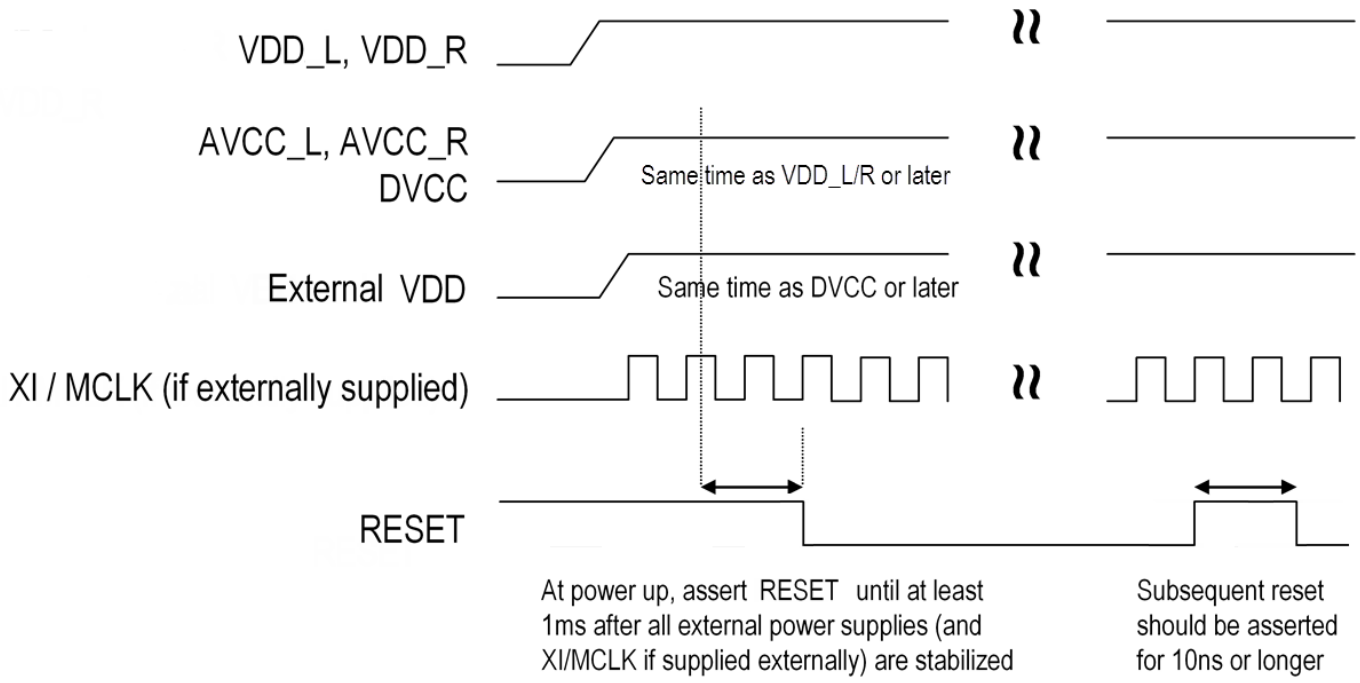
Parameter	Symbol	Min	Max	Unit
MCLK pulse width high	T_{MCH}	4.5		ns
MCLK pulse width low	T_{MCL}	4.5		ns
MCLK cycle time	T_{MCY}	10		ns
MCLK duty cycle		45:55	55:45	

Audio Interface Timing



Parameter	Symbol	Min	Max	Unit
DATA_CLK pulse width high	t_{DCH}	4.5		ns
DATA_CLK pulse width low	t_{DCL}	4.5		ns
DATA_CLK cycle time	t_{DCY}	10		ns
DATA_CLK duty cycle		45:55	55:45	
DATA set-up time to DATA_CLK rising edge	t_{DS}	2		ns
DATA hold time to DATA_CLK rising edge	t_{DH}	2		ns

Recommended Power-Up Sequence



The ES9018S must be reset after power-up to ensure correct operation. Reset can be performed using a reset controller in some configurations or via a system software reset. The active-HI reset pin provides a high input-impedance with no internal pull-up or pull-down. To reset the ES9018S, the reset input should be pulled high for a minimum of 1ms after all external power supplies (and XI/MCLK if supplied externally) are stabilized. Following the reset signal, the input can be held low indefinitely.

Analog Performance

Test Conditions (unless otherwise stated)

1. T_A = 25°C, AVCC = +3.3V, DVCC = +1.2V, fs = 44.1kHz, MCLK = 27MHz and 32-bit data
2. SNR/DNR: A-weighted over 20Hz-20kHz in averaging mode
3. THD+N: un-weighted over 20Hz-20kHz bandwidth

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Resolution			32		Bits
MCLK (PCM normal mode)			> 192 x Fs (for Fs ≤ 200kHz) > 256 x Fs (200kHz < Fs ≤ 384kHz)		Hz
MCLK (PCM OSF bypass mode)			> 24 x Fs		Hz
MCLK (DSD mode)			> 3 x Fs		Hz
MCLK (SPDIF mode)			> 386 x Fs		Hz
DYNAMIC PERFORMANCE					
DNR (mono differential current mode)	–60dBFS		135		dB-A
DNR (stereo differential current mode)	–60dBFS		133		dB-A
DNR (8-Ch differential current mode)	–60dBFS		129		dB-A
DNR (8-Ch differential voltage mode)	–60dBFS		120		dB-A
THD+N (differential current mode)	0dBFS		–120		dB
THD+N (differential voltage mode)	0dBFS		–108		dB
PCM sampling freq (Fs, normal mode)	MCLK > 192 x Fs MCLK > 256 x Fs			200 384	kHz
PCM sampling freq (Fs, OSF bypass)	MCLK > 24 x Fs			1.536	MHz
ANALOG OUTPUT					
Differential (+ or –) voltage output range	Full-scale out		3.05 (0.924 x AVCC)		Vp-p
Differential (+ or –) voltage output offset	Bipolar zero out		1.65 (AVCC / 2)		V
Differential (+ or –) current output range (Note *1)	Full-scale out		3.903		mAp-p
Differential (+ or –) current output offset (Note *1)	Bipolar zero out to virtual ground at voltage Vg (V)		2.112 – (1000 x Vg) / 834		mA
Digital Filter Performance					
De-emphasis error				±0.2	dB
Mute Attenuation			127		dB

PCM Filter Characteristics (Sharp Roll Off)						
Pass band		±0.003dB			0.454 x fs	Hz
		–3dB			0.49 x fs	Hz
Stop band		< –115dB	0.546 x fs			Hz
Group Delay				35 / fs		s
PCM Filter Characteristics (Slow Roll Off)						
Pass band		±0.05dB			0.308 x fs	Hz
		–3dB			0.454 x fs	Hz
Stop band		< –100dB	0.814 x fs			Hz
Group Delay				6.25 / fs		s
DSD Filter Characteristics						
Pass band		–3dB		50 / 60 / 70		kHz
Stop band attenuation				18		dB/oct

Table 12 - Analog Performance

Note

*1. Differential (+ or –) current output is equivalent to a differential (+ or –) voltage source in series with an 834Ω ±11% resistor. The differential (+ or –) voltage source has a peak-to-peak output range of (0.924 x AVCC) = 3.05V and an output offset of (AVCC / 2) = 1.65V with a 3.3V AVCC.

PCM DE-EMPHASIS FILTER RESPONSE (32kHz)

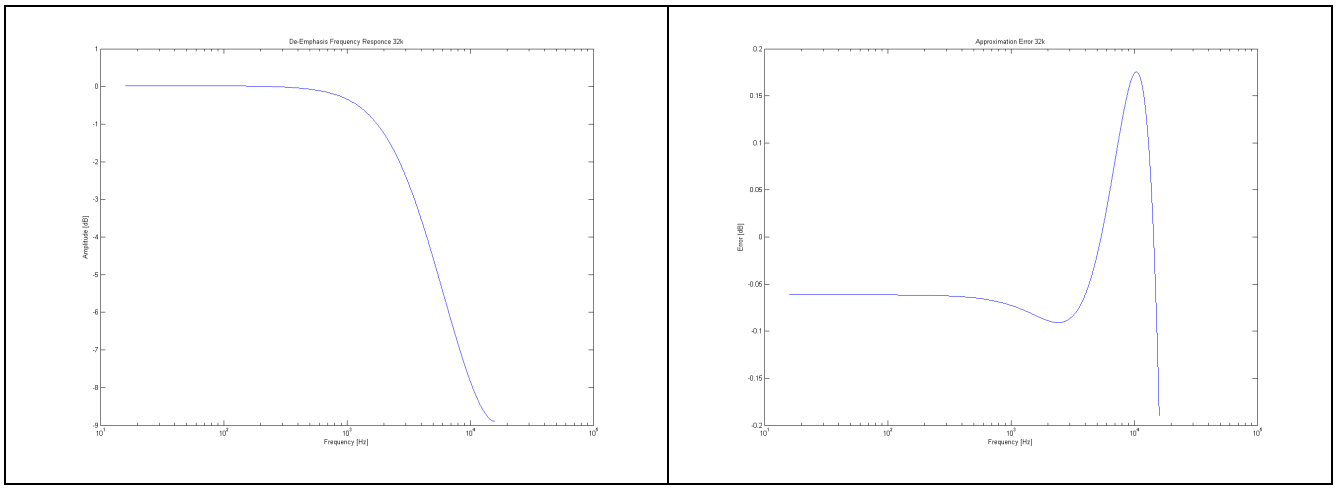


Table 13 - PCM DE-EMPHASIS FILTER RESPONSE (32kHz)

PCM DE-EMPHASIS FILTER RESPONSE (44.1kHz)

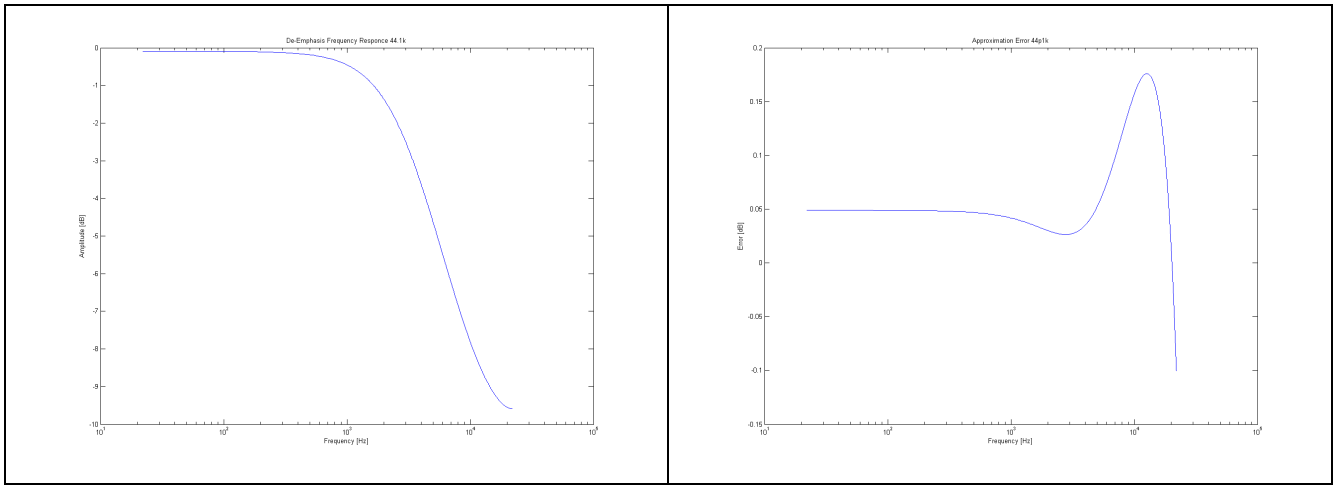


Table 14 - PCM DE-EMPHASIS FILTER RESPONSE (44.1kHz)

PCM DE-EMPHASIS FILTER RESPONSE (48kHz)

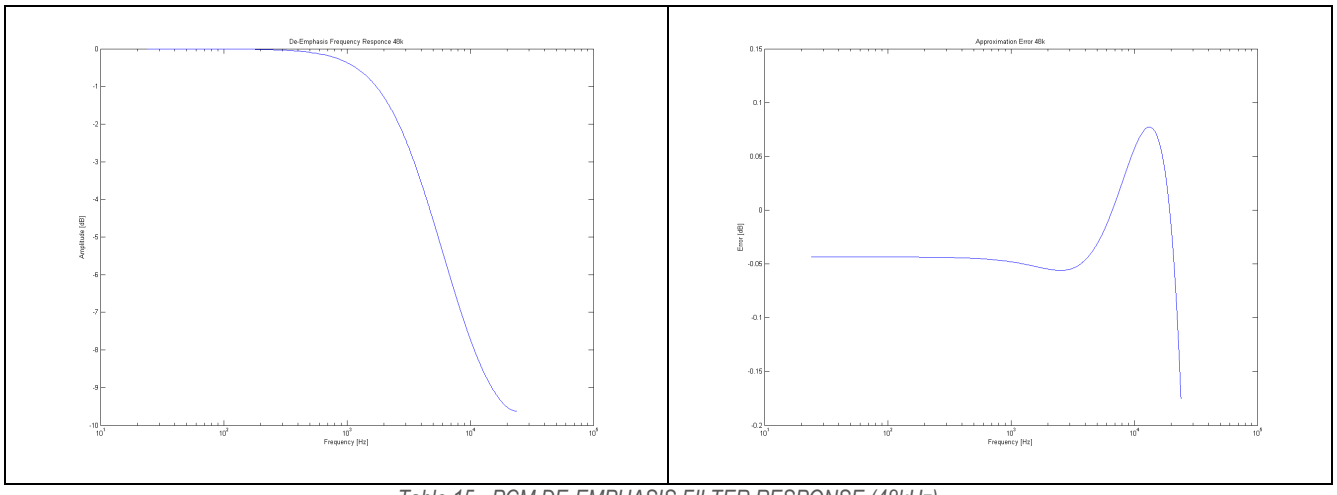


Table 15 - PCM DE-EMPHASIS FILTER RESPONSE (48kHz)

PCM Sharp Roll-Off Filter Response

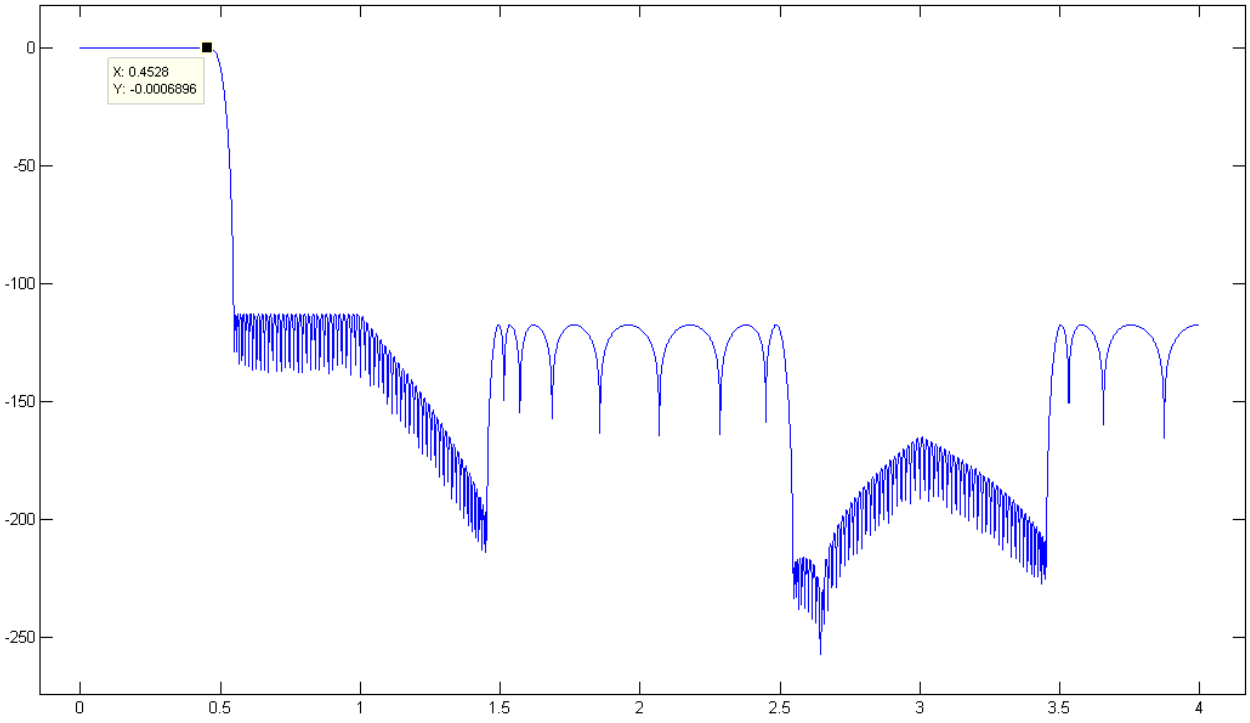


Figure 10 - PCM Sharp Roll-Off Filter Response

PCM Slow Roll-Off Filter Response

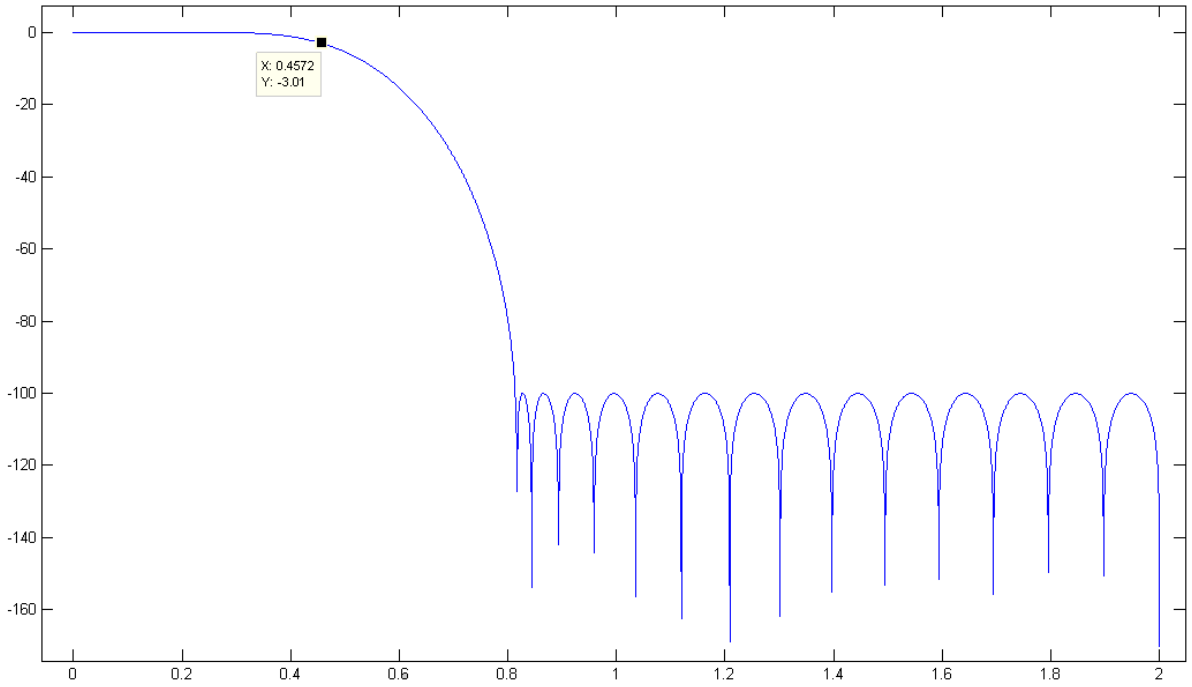


Figure 11 - PCM Slow Roll-Off Filter Response

DSD Filter Response

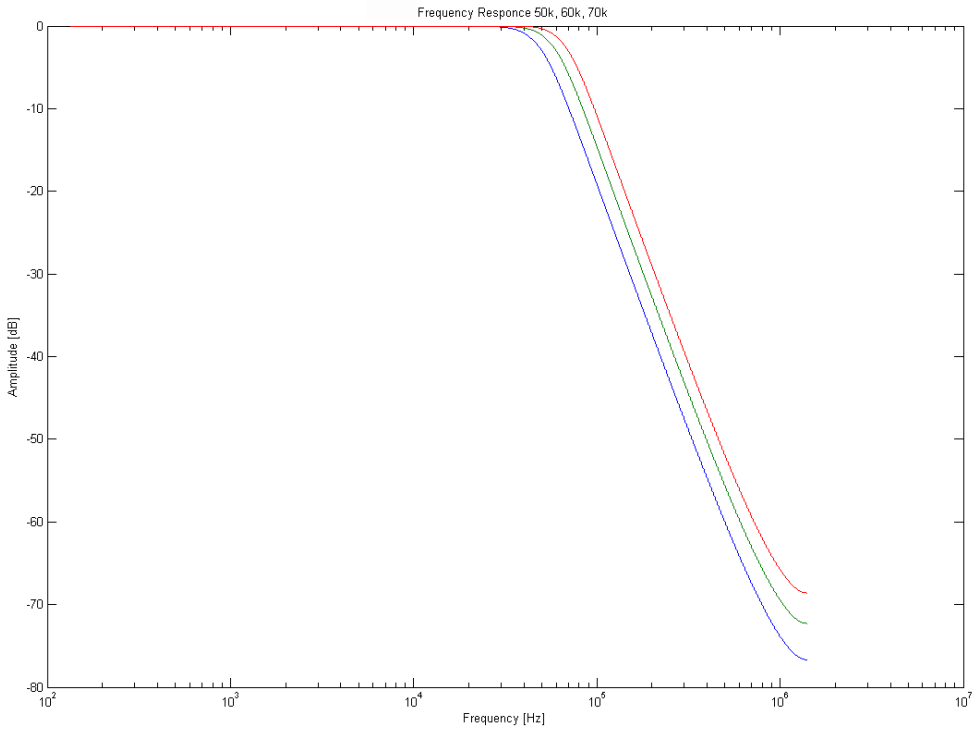
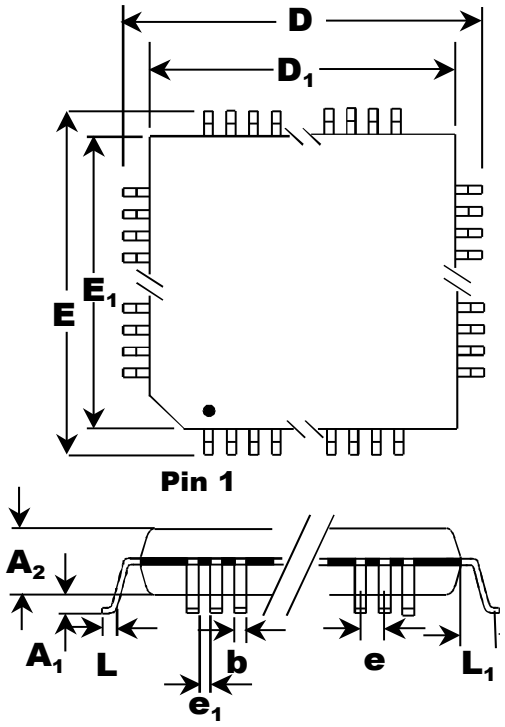


Figure 12 - DSD Filter Response

64-Pin LQFP Mechanical Dimensions



		MILLIMETERS		
Symbol	Description	Min.	Nom.	Max.
D	Lead-to Lead, X-axis	11.75	12.00	12.25
D1	Package's Outside, X-axis	9.90	10.00	10.10
E	Lead-to Lead, Y-axis	11.75	12.00	12.25
E1	Package's Outside, Y-axis	9.90	10.00	10.10
A1	Board Standoff	0.05	0.10	0.15
A2	Package Thickness	1.35	1.40	1.45
b	Lead Width	0.17	0.22	0.27
e	Lead Pitch		0.50 BSC	
e_1	Lead Gap	0.23	0.28	0.33
L	Foot Length	0.45	0.60	0.75
L1	Lead Length		1.00	
	Co-planarity			0.102
	Foot Angle	0°		7°
	No. of Leads in X-axis		16	
	No. of Leads in Y-axis		16	
	No. of Leads Total		64	
	Package Type		LQFP	

Figure 13 - 64-Pin LQFP Mechanical Dimensions

Reflow Process Considerations

For lead-free soldering, the characterization and optimization of the reflow process is the most important factor you need to consider.

The lead-free alloy solder has a melting point of 217°C. This alloy requires a minimum reflow temperature of 235°C to ensure good wetting. The maximum reflow temperature is in the 245°C to 260°C range, depending on the package size *(Table RPC-2)*. This narrows the process window for lead-free soldering to 10°C to 20°C.

The increase in peak reflow temperature in combination with the narrow process window makes the development of an optimal reflow profile a critical factor for ensuring a successful lead-free assembly process. The major factors contributing to the development of an optimal thermal profile are the size and weight of the assembly, the density of the components, the mix of large and small components, and the paste chemistry being used.

Reflow profiling needs to be performed by attaching calibrated thermocouples well adhered to the device as well as other critical locations on the board to ensure that all components are heated to temperatures above the minimum reflow temperatures and that smaller components do not exceed the maximum temperature limits *(Table RPC-2)*.

To ensure that all packages can be successfully and reliably assembled, the reflow profiles studied and recommended by ESS are based on the JEDEC/IPC standard J-STD-020 revision D.1.

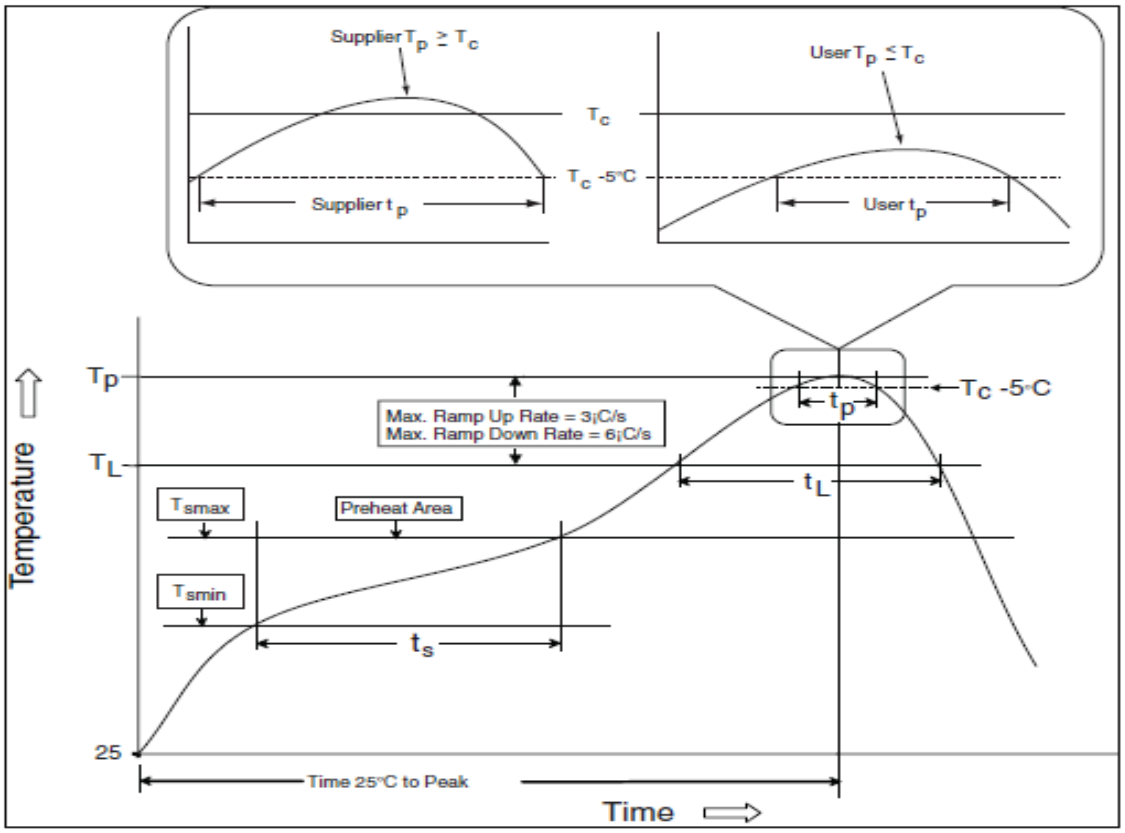


Figure 14 - IR/Convection Reflow Profile (IPC/JEDEC J-STD-020D.1)

Note: Reflow is allowed 3 times. Caution must be taken to ensure time between re-flow runs does not exceed the allowed time by the moisture sensitivity label. If the time elapsed between the re-flows exceeds the moisture sensitivity time bake the board according to the moisture sensitivity label instructions.

Manual Soldering

Allowed up to 2 times with maximum temperature of 350 degrees no longer than 3 seconds.

RPC-1 Classification reflow profile

Profile Feature	Pb-Free Assembly
Preheat/Soak Temperature Min (Tsmin) Temperature Max (Tsmax) Time (ts) from (Tsmin to Tsmax)	 150°C 200°C 60-120 seconds
Ramp-up rate (TL to Tp)	3°C / second max.
Liquidous temperature (TL) Time (tL) maintained above TL	217°C 60-150 seconds
Peak package body temperature (Tp)	For users Tp must not exceed the classification temp in Table RPC-2. For suppliers Tp must equal or exceed the Classification temp in Table RPC-2.
Time (tp)* within 5°C of the specified classification temperature (Tc), see Figure RPC-1	30* seconds
Ramp-down rate (Tp to TL)	6°C / second max.
Time 25°C to peak temperature	8 minutes max.
* Tolerance for peak profile temperature (Tp) is defined as a supplier minimum and a user maximum.	

Table 16 - RPC-1 Classification reflow profile

Note 1: All temperatures refer to the center of the package, measured on the package body surface that is facing up during assembly reflow (e.g., live-bug). If parts are reflowed in other than the normal live-bug assembly reflow orientation (i.e., dead-bug), Tp **shall** be within ±2°C of the live-bug Tp and still meet the Tc requirements, otherwise, the profile **shall** be adjusted to achieve the latter. To accurately measure actual peak package body temperatures refer to JEP140 for recommended thermocouple use.

Note 2: Reflow profiles in this document are for classification/preconditioning and are not meant to specify board assembly profiles. Actual board assembly profiles should be developed based on specific process needs and board designs and should not exceed the parameters in Table RPC-1.

For example, if Tc is 260°C and time tp is 30 seconds, this means the following for the supplier and the user.

For a supplier: The peak temperature must be at least 260°C. The time above 255°C must be at least 30 seconds.

For a user: The peak temperature must not exceed 260°C. The time above 255°C must not exceed 30 seconds.

RPC-2 Pb-Free Process - Classification Temperatures (Tc)

Package Thickness	Volume mm3, <350	Volume mm3, 350 to 2000	Volume mm3, >2000
<1.6 mm	260°C	260°C	260°C
1.6 mm - 2.5 mm	260°C	250°C	245°C
>2.5 mm	250°C	245°C	245°C

Table 17 - RPC-2 Pb-Free Process - Classification Temperatures (Tc)

Note 1: At the discretion of the device manufacturer, but not the board assembler/user, the maximum peak package body temperature (Tp) can exceed the values specified in Table RPC-2. The use of a higher Tp does not change the classification temperature (Tc).

Note 2: Package volume excludes external terminals (e.g., balls, bumps, lands, leads) and/or non-integral heat sinks.

Note 3: The maximum component temperature reached during reflow depends on package thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD packages may still exist.

Ordering Information

Part Number	Description	Package
ES9018S	Sabre[32] Reference 8-channel Audio DAC	64-pin LQFP

The letter S at the end of the part number identifies the package type LQFP.

Table 18 - Ordering Information

Revision History

Revision	Date	Notes
Initial	January 21, 2009	Initial version
1.0	January 23, 2009	Update Register #15 default value Update Audio Interface Timing Update Level Linearity Error Performance Add details to FIR Programmable Filters and Registers sections
1.1	March 13, 2009	Add ES9012
1.2	February 11, 2010	Corrected Sample Rate Calculation formula
1.21	July 26, 2012	Update feature table
1.22	December 12, 2012	Update Analog Performance table – Maximum PCM sampling frequency Update I^2C compatible modes Update 5V tolerant pins. Update pinout. Update PCM Audio Interface Diagram
1.23	April 11, 2013	Correct I2C description
1.3	July 16, 2013	Add reflow profile
1.31	September 19, 2013	Correct typos and timing diagrams
1.4	June 6, 2014	Added SABRE SOUND™ trademark
1.5	July 15, 2014	Updated ESS' FAX number. Added medical liabilities disclaimer. Clarified polarity of RESET input, pin 8, on page 4. Updated supported sampling rates. ES2012 removed. Recommended power-up sequence, timing diagram added to page 27
1.6	July 22, 2014	Pages 23 and 24, corrected the polarity of U2 on two circuit diagrams
1.7	September 16, 2014	Updated DAC output resistance from 781.25Ω to 834Ω ±11%
1.8	January 22, 2015	Cleaned up formatting and corrected typos.
1.9	February 18, 2015	Corrected formulae on Analog Performance table.
1.91	March 18, 2015	Removed incorrect note from cover page. Updated ESS Technology contact information.
2.0	February 16, 2016	Added I^2C interface timing table
2.1	March 16, 2016	Changed C_{CLK} input capacitance from 20pF max. to 5pF max.
2.2	May 4, 2016	Pin 24 on the pin layout diagram was erroneously marked as pin 34
2.3	August 9, 2021	Formatting changes