

The **Crescendo VII** is a 7th-generation SoC that integrates all soundbar audio processing functions in a Low Profile Quad Flat Pack (LQFP) package. The Crescendo VII offers a reduction in both operating and standby power consumption from the previous generations. The lower standby-power operation allows for system makers to meet the demands of green product approvals. The lower operating power eliminates the need for a heatsink in standard applications.

For lowest system BOM, the **Crescendo VII** integrates a 32-bit RISC and a 32-bit media processor for audio decoding, post-processing, lip-synchronization and sound effects such as virtual surround and bass enhancement, a software parametric equalizer (PEQ) for speaker equalization, a user-programmable 32-bit Audio Coprocessor for custom sound algorithms, stereo ADC for connection to line input sources, an 8 channel I2S input, a 4 input SPDIF/ARC receiver for connection to coaxial, optical, HDMI and ARC input sources, a 4-channel system ADC for analog status measurement, a 3-channel key ADC for multi-key support, and a high speed USB host controller for firmware upgrade or music playback.

The Crescendo VII features improved USB and UART speeds that allow for support of improved Bluetooth connectivity, higher bit rate audio, and increased number of supported channels.

FEATURE	BENEFIT
System <ul style="list-style-type: none"> High Speed USB 2.0 Host Low Operating Power/Low Standby Power Fast UART interface 	<ul style="list-style-type: none"> High Bit Rate Audio Green Certification, no heat sink required Improved compatibility with Bluetooth modules
<ul style="list-style-type: none"> 128-LQFP (14mm x14 mm) 	<ul style="list-style-type: none"> Small PCB footprint
Enhanced System Controller <ul style="list-style-type: none"> 4-input System Monitor ADC SPI M/S, I2C, UART, GPIO IR, 3x Key ADC, VFD ASRC Direct APLL CEC 	Eliminate external MCU <ul style="list-style-type: none"> System event monitoring Analog voltage generation System control & status monitoring User interface, multiple keys/pin ASRC for 2ch input source Improves BT / SPDIF performance and supports software ARSC HDMI CEC control
Comprehensive Sound Bar Processing <ul style="list-style-type: none"> Decode MP3/DD/DTS, AAC, FLAC, etc. Sound effects Audio Coprocessor w/ 144kB SRAM 	Eliminate external DSP <ul style="list-style-type: none"> Playback all legacy audio formats Virtual Surround Speaker, AV sync, Dolby ProLogic, etc. Supports custom algorithms
Versatile Audio Input <ul style="list-style-type: none"> 2-input enhanced ADC (50kΩ impedance) 4-input SPDIF/ARC receiver 8-ch I2S input 	Eliminate external SPDIF receiver & ADC <ul style="list-style-type: none"> CD quality analog audio input Connect to optical/coax/HDMI SPDIF or Audio Return Channel Take HDMI high resolution audio in compressed or PCM formats
OpenRISC CPU	Add flexibility for adding custom features



LICENSING REQUIREMENTS

Depending on the features supported, system manufacturers will need to obtain the necessary licenses. Some details are provided below.

Dolby Digital

Dolby Digital audio enabling software is provided with the Crescendo VII SoC. Dolby is a trademark of the Dolby Laboratories. Supply of this implementation of Dolby Technology does not convey a license or imply a right under any patent, or any other Industrial or Intellectual Property Right of Dolby Laboratories, to use this implementation in any end-user or ready-to-use final product. Companies planning to use this implementation in products must obtain a license from Dolby Laboratories Licensing Corporation before designing such products. Additional per-chip royalties may be required and are to be paid by the purchaser to Dolby Laboratories, Inc. Details of the OEM Dolby Digital license may be obtained by writing to:

Dolby Laboratories, Inc.
Dolby Laboratories Licensing Corporation
Attn.: Intellectual Property Manager
100 Potrero Avenue
San Francisco, CA 94103-4813
<http://www.dolby.com>

DTS 2.0 / DTS Virtual X

Details on licensing or membership can be obtained at <http://www.dtsonline.com>

MP3

Details on licensing or membership can be obtained at <http://www.mp3licensing.com>

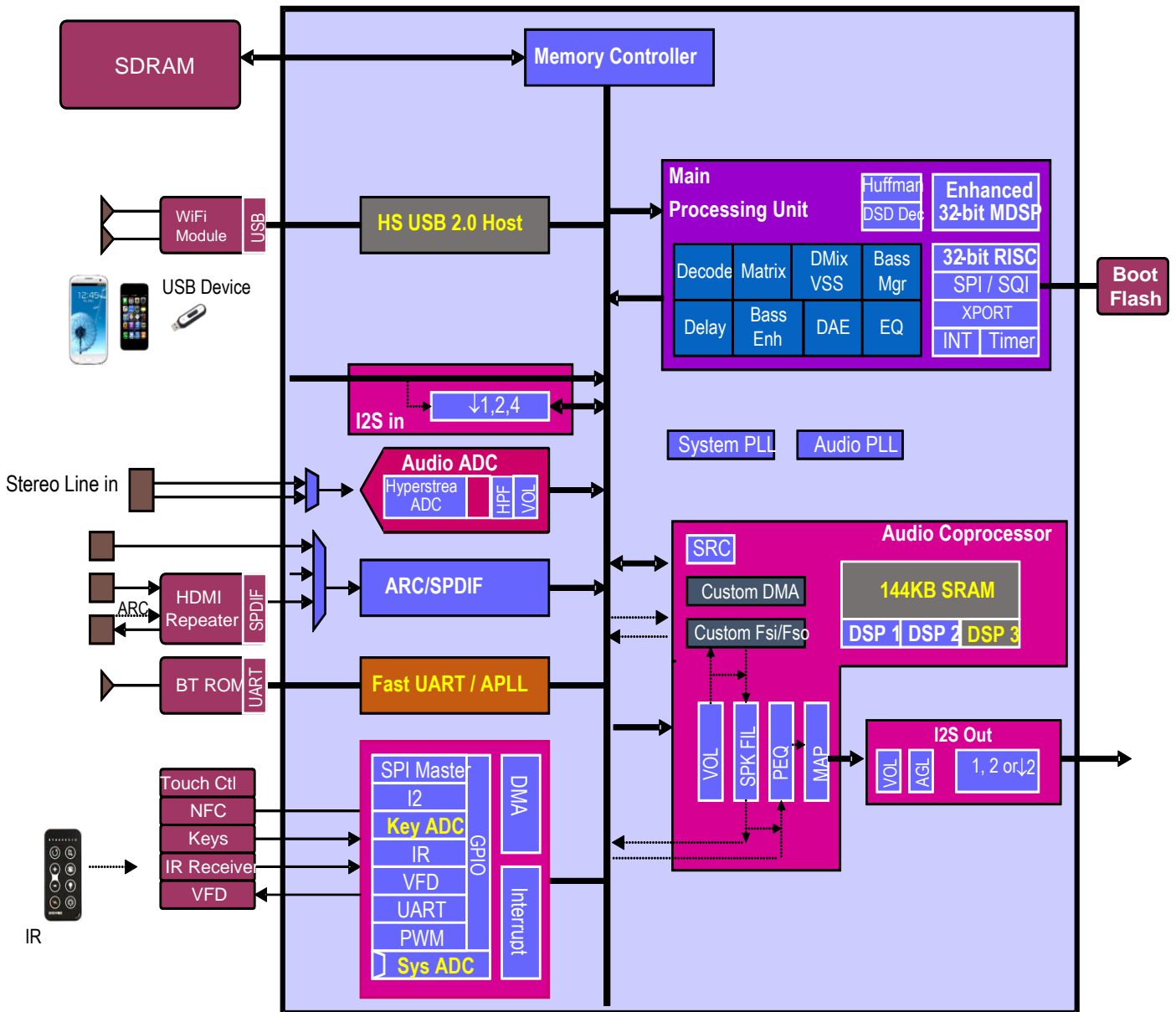
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Details on licensing or membership can be obtained at <http://www.vialicensing.com>

Crescendo VII SoundBar Product Brief



FUNCTIONAL BLOCK DIAGRAM





Crescendo VII SoundBar Datasheet

System Interfaces

The Crescendo VII SoundBar employs a unified memory architecture to ensure the lowest possible system memory cost.

Feature	Description
Memory	<ul style="list-style-type: none"> Serial flash interface via SPI
Control/Status	<ul style="list-style-type: none"> High Speed USB host controller I2C Master GPIO / IR remote control 4-input system monitor ADC

Core Audio DSP

The Crescendo VII SoundBar audio DSP is built on the ESS proprietary dual CPU Programmable Multimedia Processor (PMP) core consisting of a 32-bit RISC and a 64-bit Media Processor that deliver the best sound bar feature set.

Feature	Description
Audio Decode	<ul style="list-style-type: none"> Dolby Digital, DTS, LPCM, MP2 MP3, AAC
Audio Matrix	<ul style="list-style-type: none"> Dolby ProLogic and ProLogic II
Audio Effect	<ul style="list-style-type: none"> Graphic EQ, Reverb, Bass enhancement, Stereo expansion
Audio Spatialization	<ul style="list-style-type: none"> Virtual speaker
Speaker Compensation	<ul style="list-style-type: none"> Parametric EQ

Note: Not all features are available with all Crescendo VII SoundBar parts. For more information, please consult your ESS Sales Representative.

Audio Input and Output

The Crescendo VII SoundBar incorporates powerful audio post-processing DSPs to enable custom algorithms, as well as audio ADCs for connection to multiple line-in sources, and a 12-ch I2S interface.

Feature	Description
Custom Audio Post-processing	<ul style="list-style-type: none"> Dedicated Audio DSP with 144kB SRAM for custom algorithms Hardware speaker filters for custom crossover characteristics Hardware parametric equalizer (up to 16 band/channel)
Audio Output	<ul style="list-style-type: none"> 12-channel I2S interface
Audio Input	<ul style="list-style-type: none"> 4-input SPDIF receiver 2-input Stereo ADC 8-channel I2S interface

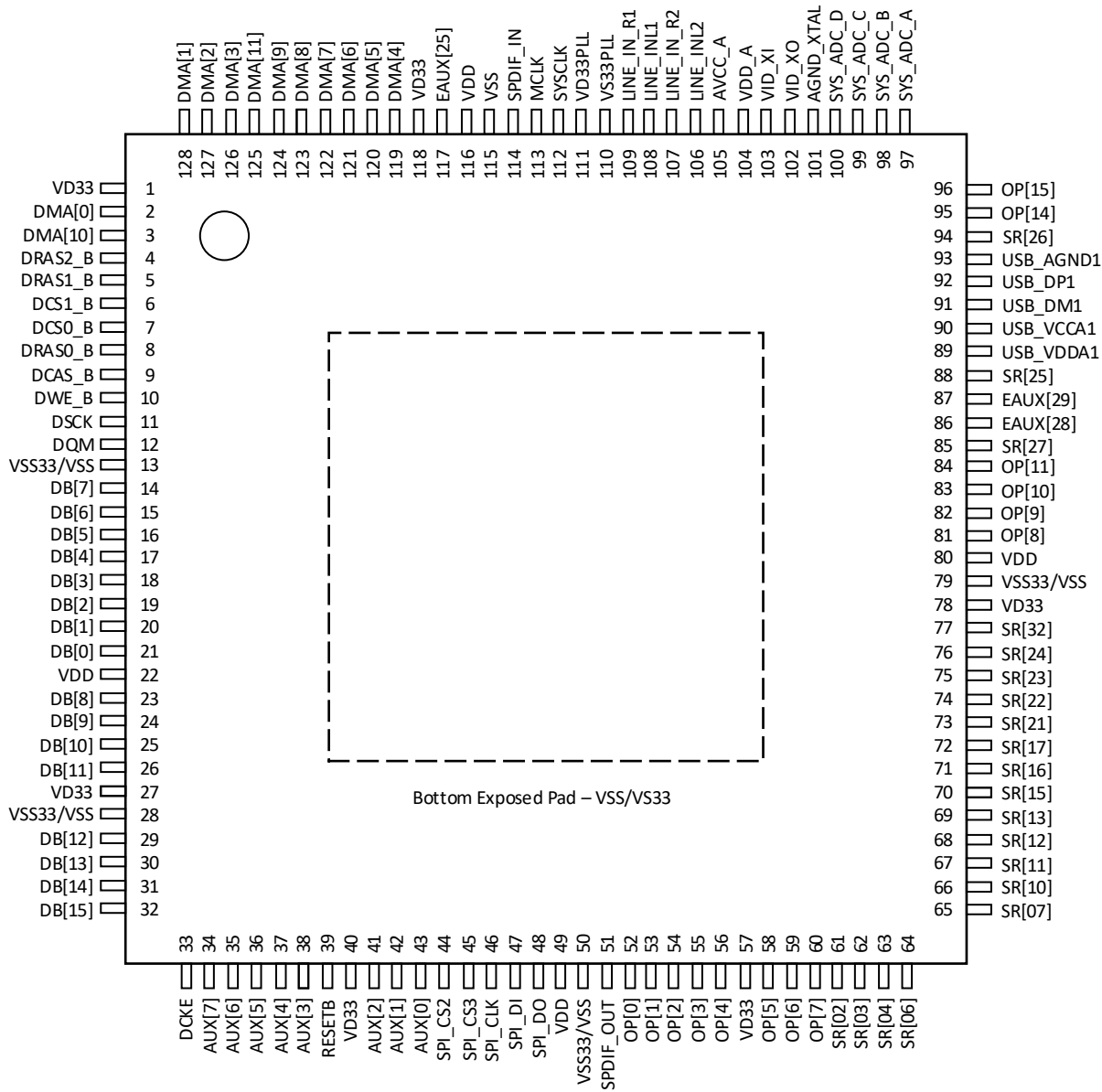
High Speed USB Host Controller

USB high-speed host controller are built-in to allow field upgrade of system firmware and connection to thumb drives for playback of music files.

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PIN LAYOUT





Crescendo VII SoundBar Datasheet

PIN DESCRIPTION

Pin #	Name	Type	ResetState	Pin Description
1	VD33	Power		3.3V Power Supply
2	DMA [0]	O	0	DRAM Address Bus
3	DMA [10]	O	0	DRAM Address Bus
4	DRAS2_B	I/O	1	SDRAM Bank Select 1 / E AUX[13]
5	DRAS1_B	I/O	1	SDRAM Bank Select 0 / E AUX[14] / DCS1_B
6	DCS1_B	I/O	0	DRAM Bank Sel/DRAM Chip Sel / E AUX[12] / DMA[12] / TDMFS / RWS / HW_mute
7	DCS0_B	I/O	0	SDRAM Chip Select
8	DRAS0_B	I/O	1	DRAM RAS 0
9	DCAS_B	I/O	1	DRAM CAS
10	DWE_B	I/O	1	DRAM WE_B
11	DSCK	O	0	DRAM Clock
12	DQM	I/O	1	DRAM DQM
13	VSS33/VSS	Power		Common ground for exposed pad L/F
14	DB [7]	I/O	1	DRAM Data Bus
15	DB [6]	I/O	1	DRAM Data Bus
16	DB [5]	I/O	1	DRAM Data Bus
17	DB [4]	I/O	1	DRAM Data Bus
18	DB [3]	I/O	1	DRAM Data Bus
19	DB [2]	I/O	1	DRAM Data Bus
20	DB [1]	I/O	1	DRAM Data Bus
21	DB [0]	I/O	1	DRAM Data Bus
22	VDD			1.3V Core Power Supply
23	DB [8]	I/O	1	DRAM Data Bus
24	DB [9]	I/O	1	DRAM Data Bus
25	DB [10]	I/O	1	DRAM Data Bus
26	DB [11]	I/O	1	DRAM Data Bus
27	VD33			3.3V Power Supply
28	VSS33/VSS			Common ground for exposed pad L/F
29	DB [12]	I/O	1	DRAM Data Bus
30	DB [13]	I/O	1	DRAM Data Bus
31	DB [14]	I/O	1	DRAM Data Bus
32	DB [15]	I/O	1	DRAM Data Bus
33	DCKE		i	DRAM Clock Enable
34	AUX [7]	I/O	1	AUX [7] / U2_SIN
35	AUX [6]	I/O	1	AUX [6] / U2_SOUT
36	AUX [5]	I/O	1	AUX [5] / SPDIF_IN2/PWM_CTRL1
37	AUX [4]	I/O	1	AUX [4] / IR
38	AUX [3]	I/O	1	AUX [3] / Block_Rst
39	RESET_B	I	1	Chip Reset (active low)
40	VD33			3.3V Power Supply
41	AUX [2]	I/O	1	AUX [2] / SIN_2
42	AUX [1]	I/O	1	AUX [1] / I2C_CLK / S_SPI_CLK
43	AUX [0]	I/O	1	AUX [0] / I2C_DATA / S_SPI_MOSI
44	SPI_CS2	I/O	1	SPI_ROM / GPIO_Mute / E AUX [16] / drv_enable / S_SPI_CS
45	SPI_CS3	O	1	SPI_ROM / SPI_pinstrap_swap_bank23
46	SPI_CLK	O	1	SPI_ROM
47	SPI_DI	I/O	1	SPI_ROM (IO_0)
48	SPI_DO	I/O	1	SPI_ROM (IO_1)

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Pin #	Name	Type	ResetState	Pin Description
49	VDD	Power		1.3V Core Power Supply
50	VSS33/VSS	Ground		Common ground for exposed pad L/F
51	SPDIF_OUT	I/O	I	SPDI_OUT / EAUX [7] / SOUT_2
52	OP [0]	I/O	I	SIN_4 / SDIO_CD / SPDIF_IN3
53	OP [1]	I/O	I	TSD0_2 / SDIO_LED
54	OP [2]	I/O	I	TSD1_2 / DCLK_DOE
55	OP [3]	I/O	I	TSD2_2 / OR_boot
56	OP [4]	I/O	I	TSD3_2 / THM_W / S_SPI_MISO / OR1200_SIN
57	VD33	Power		3.3V Power Supply
58	OP[5]	I/O	I	TWS_2/KEY_ADC3
59	OP [6]	I/O	I	TBCK_2 / HDMI_CEC
60	OP [7]	I/O	I	SOUT_4 / SDIO_WP / SPDIF_IN4
61	SR [02]	I/O	I	TSD0_3 / SDIO_LED_2
62	SR [03]	I/O	I	TSD1_3 / SDIO_CD_2
63	SR [04]	I/O	I	TSD2_3 / SDIO_D0_2
64	SR [06]	I/O	I	SDIO_WP_2
65	SR [07]	I/O	I	TSD3_3 / SDIO_D1_2
66	SR [10]	I/O		TDMR / SDIO_D0 / RSD [0]
67	SR [11]	I/O		TDMFS / SDIO_D1 / RSD [1]
68	SR [12]	I/O	I	TDMCLK / SDIO_CLK / RBCK
69	SR [13]	I/O	I	TSD4_2 / SDIO_D3 / RSD [3] / PWM_CTRL0
70	SR [15]	I/O	I	p_dwn_drv / EAUX [1] / TWS_3 / SDIO_CMD
71	SR [16]	I/O	I	TSD4_3 / SDIO_D2_2
72	SR [17]	I/O	I	TSD5_3 / SDIO_D3_2
73	SR [21]	I/O	I	TSD5_2 / SDIO_D2 / RSD [2] / KEY_ADC2
74	SR [22]	I/O	I	PWM_CTRL0_2
75	SR [23]	I/O	I	TWS / SDIO_CMD_2
76	SR [24]	I/O	I	TBCK / SDIO_CLK_2
77	SR [32]	I/O	I	RWS_2 / TMDMR_1 / KEY_ADC1
78	VD33	Power		3.3V Power Supply
79	VSS33/VSS	Ground		Common Ground for Exposed Pad L/F
80	VDD	Power		1.3V Core Power Supply
81	OP [8]	I/O	I	I2C_A_CLK / S_SPI_CLK_2
82	OP [9]	I/O	I	I2C_A_DATA / S_SPI_MOSI_2
83	OP [10]	I/O	I	I2C_B_CLK / S_SPI_MISO_2
84	OP [11]	I/O	I	I2C_B_DATA / S_SPI_CS_2
85	SR[27]	O	I	PWM_CTRL1_2 / PLL_SEL[3]
86	EAUX[28]	I/O	I	PLL_SEL[1]
87	EAUX[29]	I/O	I	TDMFS_2
88	SR[25]	I/O	I	SPDIF_IN6
89	SR[26]	I/O	I	SPDIF_IN5
90	OP[14]	I/O	I	TDMCLK_2 / OR1200_SOUT
91	OP[15]	I/O	I	TMDMR_2
92	USB_VDDA1			Analog USB1 ID Pin
93	USB_VCCA1			Analog USB1 VBUS Pin
94	USB_DM1			Analog USB1 Signal 0 (minus)
95	USB_DP1			Analog USB1 Signal 0 (plus)
96	USB_AGND1			Analog Ground for USB1
97	VD33PLL			3.3V Power Supply for PLLs
98	SYS_ADC_A			System Monitor ADC input / OP[20]
99	SYS_ADC_B			System Monitor ADC input / OP[21]
100	SYS_ADC_C			System Monitor ADC input / OP[22]



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Pin #	Name	Type	ResetState	Pin Description
101	SYS_ADC_D			System Monitor ADC Input / OP[23]
102	AGND_XTAL	Ground		Analog Ground for XTAL and SYS_ADC
103	VID_XO	O	O	Crystal Output
104	VID_XI	I	I	Crystal Input
105	VDD_A	Power		Analog 1.3V Analog Power Supply for Audio ADC
106	LINE_IN_L2	I	I	ADC Line In
107	LINE_IN_R2	I	I	ADC Line In
108	LINE_IN_L1	I	I	ADC Line In
109	LINE_IN_R1	I	I	ADC Line In
110	AVCC_A	Power		Analog 3.3V Power Supply for XTAL / ADC / SYS_ADC
111	AGND_ADC	Ground		Analog Ground for ADC
112	SYSCLK	I/O	I	EAUX[11] / TDMCLK / RBCK
113	MCLK	I/O	I	Audio Master Clock / EAUX[10] / TBCK
114	SPDIF_IN	I/O	I	SPDIF_In / SPDIF_Out
115	VSS	Ground		Common Ground for Exposed Pad L/F
116	VDD	Power		1.3V Core Power Supply
117	EAUX [25]	I/O	I	EXT_PWM_CLK
118	VD33	Power		3.3V Power Supply
119	DMA [4]	O	O	DRAM Address Bus
120	DMA [5]	O	O	DRAM Address Bus
121	DMA [6]	O	O	DRAM Address Bus
122	DMA [7]	O	O	DRAM Address Bus
123	DMA [8]	O	O	DRAM Address Bus
124	DMA [9]	O	O	DRAM Address Bus
125	DMA [11]	O	O	DRAM Address Bus
126	DMA [3]	O	O	DRAM Address Bus
127	DMA [2]	O	O	DRAM Address Bus
128	DMA [1]	O	O	DRAM Address Bus
Exposed Pad	VSS/VS33	Ground		

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REVISION HISTORY

Current Version 0.5

Revision	Date	Notes
0.1	August 30, 2017	Initial version
0.2	October 11, 2017	<ul style="list-style-type: none"> Updated front page features, Pin Layout, Pin Description,
0.3	October 12, 2017	<ul style="list-style-type: none"> Updated Functional Block Diagram and Pin Layout
0.5	August 26, 2022	<ul style="list-style-type: none"> Updated to data sheet spec

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