Precise Measurement of the Accuracy of 24 bit ADC by AC Josephson effect

Haruo YOSHIDA 1), Tuneoki KOZAKAI 2), Eiichi YADA 3), Yasushi MURAYAMA 4)
1) Advantest Laboratories Ltd. 48-2 Mastuhara, Kamiayashi, Aoba-ku, Sendai, Miyagi, 989-31 Japan
2) Advantest Ltd., Gunnma Factory. Shinozuka 54-1, Oura-machi, Oura-gun, Gunnma, 370-06 Japan
3) Advantest ADC Ltd. Miyako 77-1, Namekawa-cho, Hiki-gun, Saitama, 355 Japan
4) Electrotechnical Laboratory. 1-1-4 Umezono, Tsukuba, Ibaraki, 305 Japan

Abstract

This paper reports precise measurement of the offset error voltage and non-linearity error voltage of 24 bit analog to digital converter (ADC) from -10 V to +10 V on the basis of 10-V Josephson junction array voltage standard system (10-V JJAVS). Characteristics of the ADC has improved with correcting detected localized raggedness of those errors.

Introduction

Analog to digital converters (ADCs) are classified into three large groups, that is, high speed flash-type ADC, conventional successively-comparison-type ADC and high resolution integrating-type ADC. There are many technical items which provide for the characteristics of ADC, such as resolution, accuracy, conversion time etc. Generally speaking, inferior coordination among the components cause those errors. Though precise DC voltage calibrator is required to verify the accuracy of the ADC, the best accuracy of commercial available DC voltage calibrator based on Zener diode and PWM (Pulse Width Modulation) technique is 1 to 2 ppm (x 10^{-6}) at present.

We discuss the verification of the accuracy of the 24 bit multi-slope ADC based on the results of offset error and non-linearity error (linearity deviation) measured by using the new 10-V JJAVS [1], [2] in this paper. As the accuracy of the Josephson step voltage is determined by the uncertainty of millimeter-wave frequency of $1x10^{-10}$ and leakage resistance uncertainty of $1x10^{-10}$, it become a suitable voltage reference for precise linearity measurement of the ADC.

Block diagram of 24 bit ADC and its characteristics

A block diagram of integrating type 24 bit ADC for 8 digit DVM which is developed by Advantest is shown in Fig.-1. The ADC is designed for compatible with high resolution and high speed measurement of the DVM. In order to obtain those compatibility, it has multi-slope mechanism, 12 MHz clock rate and -10 V reference. Nominal main specification is listed in Table-1.

Table-1

* Resolution :
  0.01 ppm at 10 PLC (200 msec.), 0.1 ppm at 1PLC (20 msec.), 1 ppm at 2 msec.
* Input analog voltage : +/- 12 V (Bipolar)
* Input Impedance : 20 kΩ
* Non-linearity error : 0.2 ppm
* Total drift : 0.38 ppm/degree C

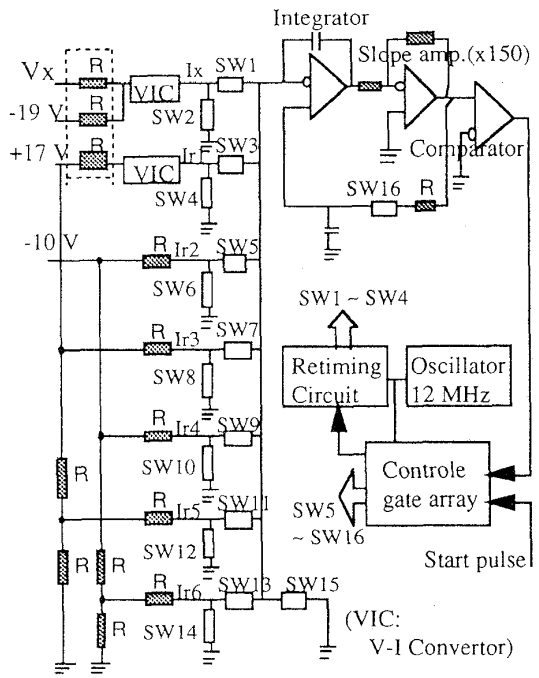

Fig.-1 Block diagram of the integrating 24 bit ADC

Measurement of the offset error and non-linearity error of the ADC

Based on the recently developed technique to capture the desired Josephson voltage step [2], the offset error of the ADC is measured as a difference between the reading value of the ADC (average of 10 data obtained with each 50 PLC (1 sec.) integrating time and same auto zero adjusting time) and the selected Josephson step voltage.

Measured offset error voltages and calculated non-linearity error voltages of the ADC between - 10 V to + 10 V are shown in Fig.-2(a) and (b). Non-linearity error is defined by the difference between each offset error and linear fitting regression line. (There is another " non-linearity error " defined by the difference between each error and end-point line.)

As there was obvious localized raggedness between 0 V to +10 V as shown in Fig.-2(a) and (b), we adjusted those characteristics based on the measured data to be straighten, the results is shown in Fig.-3(a) and (b). In order to measure the characteristics on + and - polarity, we do not use polarity reversing technique which eliminate thermal EMF. produced on the signal

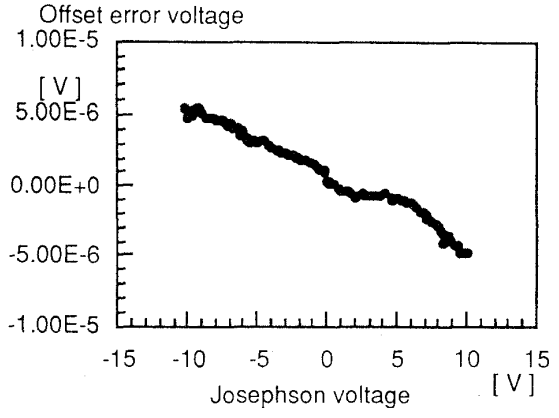

Fig.-2(a) Offset error voltage of the ADC

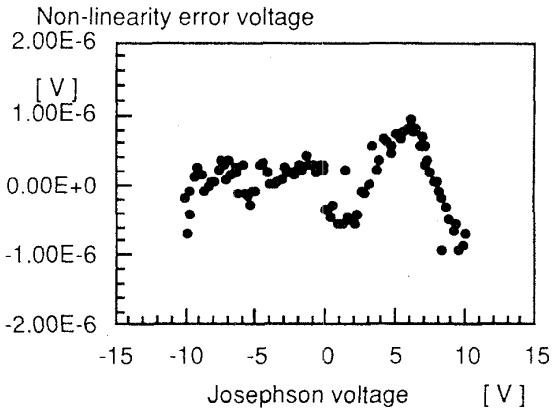

Fig.-2(b) Non-linearity error voltage of the ADC

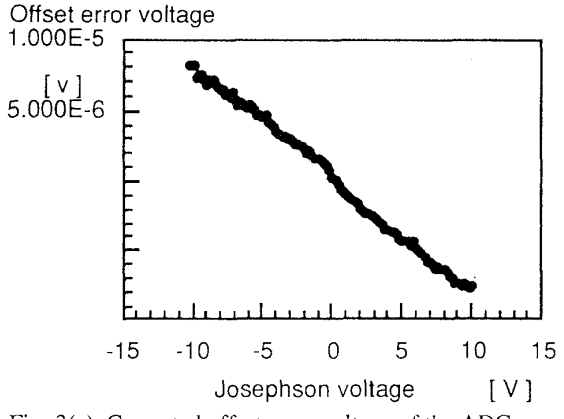

Fig.-3(a) Corrected offset error voltage of the ADC

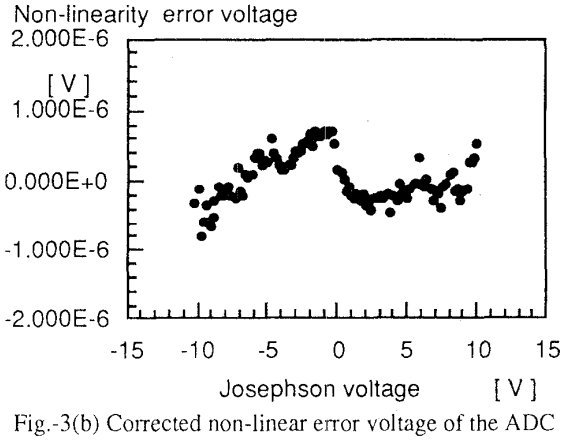

Fig.-3(b) Corrected non-linear error voltage of the ADC

line, so that the thermal EMF. is included as an error in each measured data. Measured thermal EMF. is about 20 to 60 nV as shown Fig.-4.

Though the localized raggedness has revised, linearity gap around 0 V is still remained. This problem is caused by the control pulse width which determine the antipodal condition to compromise high resolution and high speed of the ADC, so that it is not easy to solve soon, but we expect that this problem will be solved with acquiring newly developed precise measuring tool.

Conclusion

Based on the AC Josephson effect, offset error and non-linearity error characteristics of the 24 bit multi-slope ADC for 8 digit DVM had measured precisely. As a result of the precise measurement, detected localized raggedness has revised. Acquiring the precise measuring tool based on the quantum effect, we expect the total accuracy of the ADC and digital to analog converter (DAC) will be improved drastically.

Acknowledgment

The authors would like to thank Dr. Yasuhiko SAKAMOTO and Dr. Tadashi ENDO/ETL for their helpful discussions for applying AC Josephson effect on accuracy check of the ADC.

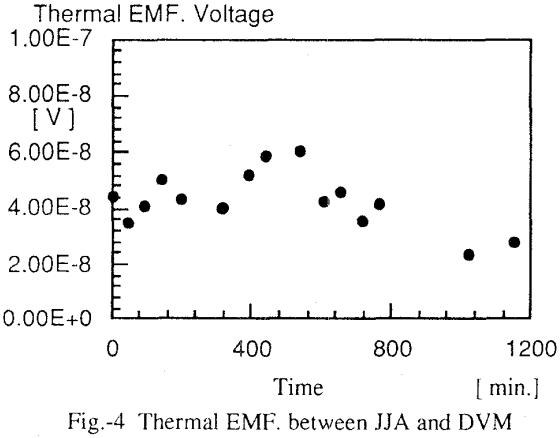

Fig.-4 Thermal EMF. between JJA and DVM

References

[1] Y. Murayama et al., " Ten-Volt Josephson Junction Array Voltage Standard at ETL", submitted to this issue.

[2] H. Yoshida et al., " Precise Null Balancing Technique for 10-V Josephson Junction Array Voltage Standard", submitted to this issue.