CMOS-6
1.0 Micron CMOS Gate Array

Description

CMOS-6 is NEC's well-established channelless gate array family. The CMOS-6 family comprises 17 masters, which are available in a wide variety of package types including thin packages (T-QFP), QFP with heatspreader and PGA.

The CMOS-6 family is designed for cost effective solutions in low end, low gate count applications to be used in all market segments. In addition, specific master steps are tuned for low gate count in combination with high pin count.

The CMOS-6 libraries give immediate access to over 300 functions, a wide set of interface blocks, RAM, ROM and commonly used mega macros like UART and DMA controller. The standard library has been characterised also for extended operation voltage starting at 2.7 V. Therefore this 5 V technology can be used also in the field of typical 3 V applications.

Features

- ❍ 1.0 µm (drawn) CMOS process
- ❍ Sea-of-gates
- ❍ Extended voltage range (2.7 V ~ 5.5 V)
- ❍ Extensive block library
- ❍ Mega macro support
- ❍ High Speed / High Density RAM, ROM
- ❍ Variable output drive (4.5 to 24 mA)
- ❍ Supports scan test methodology
- ❍ High pin count
- ❍ Wide range of package options

Product Outline

Family		CMOS-6A/6S	CMOS-6
Metalization layers (Al.)		2 metal layers	3 metal layers
Gate Count Range (raw)		2k - 70k	42k - 177k
Utilisation (Minimum)		65% for 2 metal layers, 80% for 3 metal layers	
Toggle Frequency (Min.)		120 MHz	
Delay time	Internal gate	0.27 ns (F/O = 1, l = 0 mm); 0.40 ns (F/O = 2, l = 2 mm) Note1	
	Input buffer	1.0 ns (F/O = 2, l = 2 mm)	
	Output buffer	2.0 ns (C L = 15 pF)	
Consumed Power	Internal gate	8 µW/MHz/Cell	
	Input buffer	46 µW/MHz/Cell (CMOS, normal buffer)	
	Output buffer	0.78 mW/MHz/Cell (C_L = 15 pF)	
Power supply voltage		5V ±10% (CMOS), 5V ±5% (TTL), extended voltage range starting at 2.7V	
Operating temperature		-40 to +85°C	
Interface level		CMOS level, TTL level	
Technology		Channelless (Sea-of-Gates) 1.0 µm Silicon gate CMOS	

Note1 : 2-input NAND power gate

Document No. A10013EE2V0DS00
Date Published April 1996
Printed in Germany

Master Line-Up

This 1.0µ sea-of-gates technology offers 17 masters starting at 2k up to 177k raw gates, achieving a utilisation of minimum 65% for two-layer and 80% for three-layer devices. The 13 masters of CMOS-6A/6S are using two metal layers. The CMOS-6 family provides four masters with high gate count and three metal layers.

CMOS-6 Master Table

Sub-Family	CMOS-6				CMOS-6S				
Metal Layers	3				2				
Master Name	65658	65664	65672	65676	65611	65621	65625	65643	65653
Raw Gates	42240	72576	119232	177408	1836	3484	5312	13416	25488
PAD Count*	220	288	368	448	80	100	120	176	236

Sub-Family	CMOS-6A							
Metal Layers	2							
Master Name	65630	65636	65640	65646	65650	65654	65656	65662
Raw Gates	5376	8000	11520	16240	21120	30720	40480	70272
PAD Count*	84	100	120	140	160	192	220	288

Note: * = 16 Pads are reserved for VDD/GND pins. Please refer to detailed master/package description in Design Manual.

Design Tool Support

NEC supports its ASIC products with a comprehensive CAD system that significantly reduces the time and expense usually associated with the development of semicustom devices.

NEC's OpenCAD™ Design System - a unified design package for front-to-back-end - allows designers to combine tools from the CAE industry's most popular third-party vendors and from NEC's offer of powerful proprietary software tools.

The OpenCAD™ integration system supports tools for schematic capture, logic synthesis, floorplanning, automatic test pattern generation (ATPG), full timing simulation, accelerated fault-grading and advanced place-and-route algorithms. These advanced CAD tools help ensure accurate designs.

Placement and Routing is performed in the European headquarter in Düsseldorf (Germany), which allows quick and flexible handling of specific design demands leading to significantly reduced turn-around-times.

Macrofunctions

The CMOS-6 Gate Array family offers an extensive library of primitives, complex functions and RAM/ROM blocks. In addition to these macros the following mega macros are available or under development:

Function	Compatible Device
DMA Controller	µPD71037
Serial Control Unit (USART)	µPD71051
µPD71051 Programmable Timer / Counter	µPD71054
Parallel Interface Unit	µPD71055
Interrupt Control Unit	µPD71059
UART	NS16C450
UART with FIFO	NS16550A
I^2C-Bus Interface	I^2C

The usage of these macrofunctions is fully supported by NEC's OpenCAD™ Design System.

Block Library

The CMOS-6 family offers a variety of blocks, among others combination gates, counters, shift registers and scan macros which can be used for scan path design. In addition, memory blocks such as RAM and ROM are provided. The usage of RAM can be optimised for density or speed. The low-power blocks are designed for gate count reduction; the number of cells are fewer than that of the standard block, contributing to lower power consumption and higher efficiency. Many combinations of

different buffers and interface types are available to optimise for system requirements. Special clock drivers can be used for clock distribution.

I/O Buffer

Buffer Type	Options and possible combinations
Input Buffer	Pull-Up 50 kΩ, 5 kΩ / Pull-Down 50 kΩ Schmitt Trigger Input / TTL Level / High Fanout (Clock Driver)
Output Buffer, Bidirectional I/O-Buffer	Drive Ability: 4.5, 9, 13.5, 18, 24 mA / TTL Level (note 1) / Open Drain / Pull-Up 50 kΩ, 5 kΩ/ Pull-Down 50 kΩ / Tri-State / Low Noise / Oscillator Buffer / Osc. Buffer 32 kHz

(note 1) TTL Output buffers are only available in CMOS-6 and CMOS-6A, but not in CMOS-6S

Memory Blocks

Type (Function)	Operation	Bit range	Word range
High density single port RAM	Asynchronous	4 to 40	128 to 4k
High speed single port RAM	Asynchronous	4 to 40	32 to 512
High speed dual port RAM	Asynchronous	4 to 40	32 to 512
Standard ROM	Asynchronous	4 to 32	128 to 8k

Replacement of CMOS-6V/6X

The new introduced CMOS-6S masters cover a range of 1836 raw gates at 64 I/O signals up to 25488 raw gates providing 220 signal pins The new masters can be seen as a shrinked version of the former CMOS-6V/6X masters. The combination of small masters using a high pad count is realised in CMOS-6S using a 100 µm pad pitch. As a result, this new family provides smaller die sizes at a higher pin count than the former families CMOS-6V/6X.

Packaging

The CMOS-6 Family supports a variety of different master package combinations. The wide range of packages includes also thin packages (T-QFP, L-QFP) and QFP with heatspreader, to improve the thermal characteristics. Pin restricted designs with small gate count can be realised by the suitable choice of master and package. For information concerning mounting, quality and reliability please refer to NEC's dedicated documentation.

CMOS-6 Package Availability (Note: ❍ = Under development ✔ = Available)

Sub-Family			CMOS-6				CMOS-6S				
Package Type	No. of Pins	Pitch [mm]	65658	65664	65672	65676	65611	65621	65625	65643	65653
QFP	44	0.80					✔	✔	✔		
	52	1.00					✔	✔	✔		
	64	1.00					✔	✔	✔		
	80	0.80						✔	✔		
	100	0.65	✔						✔		
	120	0.80	✔	✔	✔						
	136	0.65	✔	✔	✔					✔	
	160	0.65	✔	✔	✔	✔				✔	
	184	0.65	✔	✔	✔	✔					❍
QFP (FP)	100	0.50	✔						✔		
	120	0.50	✔	✔	✔						
	144	0.50	✔	✔	✔					✔	

Sub-Family			CMOS-6				CMOS-6S				
Package Type	No. of Pins	Pitch [mm]	65658	65664	65672	65676	65611	65621	65625	65643	65653
QFP (FP)	160	0.50	✔	✔	✔	✔				✔	
	176	0.50	✔	✔	✔	✔				✔	✔
	208	0.50	✔	✔	✔	✔					✔
	240	0.50		✔	✔	✔					
	304	0.50			✔	✔					
QFP (HSP)	160	0.65	✔	✔	✔						
QFP-FP (HSP)	208	0.50	✔	✔	✔	✔					❍
	304	0.50			✔						
TQFP (FP)	48	0.50					❍	❍			
	64	0.50					❍	❍	❍		
	80	0.50						❍	❍		
	100	0.50	✔						❍		
	120	0.40	✔								
LQFP (FP)	144	0.50	✔		✔					❍	
PLCC	68		✔								
	84		✔								
PGA	132		✔	✔	✔	✔					
	176		✔	✔	✔	✔					
	208		✔	✔	✔	✔					
	280			✔	✔	✔					
	364				✔	✔					
B/L PGA	528					✔					

Sub-Family			CMOS-6A							
Package Type	No. of Pins	Pitch [mm]	65630	65636	65640	65646	65650	65654	65656	65662
QFP	44	0.80	✔	✔	✔	✔	✔			
	52	1.00	✔	✔	✔	✔	✔	✔		
	64	1.00	✔	✔	✔	✔	✔	✔		
	80	0.80	✔	✔	✔	✔	✔	✔		
	100	0.65	✔	✔	✔	✔	✔	✔	✔	
	120	0.80	✔		✔	✔	✔	✔	✔	✔
	136	0.65				✔	✔	✔	✔	✔
	160	0.65					✔	✔	✔	✔
	184	0.65						✔	✔	✔
QFP (FP)	100	0.50		✔	✔	✔	✔	✔	✔	
	120	0.50			✔	✔	✔	✔	✔	✔
	144	0.50				✔			✔	✔
	160	0.50					✔	✔	✔	✔
	176	0.50					✔	✔	✔	✔
	208	0.50							✔	✔
	240	0.50								✔
QFP (HSP)	160	0.65							✔	✔
	160	0.50							❍	❍
	176	0.50							❍	❍
	208	0.50							✔	✔
TQFP (FP)	48	0.50	✔							
	64	0.50	✔	✔	✔	✔				
	80	0.50	✔	✔	✔	✔				
	100	0.50		❍	✔	✔	❍	✔	✔	
	120	0.40			❍	❍	❍	❍	✔	
LQFP (FP)	144	0.50				✔	✔	❍	✔	❍
PLCC	84						✔			
PGA	72				✔	✔	✔	✔		
	132					✔	✔	✔	✔	✔
	176							✔	✔	✔
	208								✔	✔
	280									✔

Absolute Maximum Ratings

Power supply voltage, V_{DD}	-0.5 to 6.5 V
Input voltage, V_I	-0.5 to V_{DD}+ 0.5 V
Output voltage, V_O	-0.5 to V_{DD}+ 0.5 V
Output current I_O	
@ $I_{OL(MIN)}$ = 4.5 mA	< 10 mA
@ $I_{OL(MIN)}$ = 9.0 mA	< 20 mA
@ $I_{OL(MIN)}$ = 13.5 mA	< 30 mA
@ $I_{OL(MIN)}$ = 18.0 mA	< 40 mA
@ $I_{OL(MIN)}$ = 24.0 mA	< 60 mA
Operating temperature, T_{OPT}	-40 to +85°C
Storage temperature, T_{STG}	-65 to +150°C

Input/Output Capacitance

V_{DD}=V_I=0 V; f=1 Mhz ; T_A = +25 °C.

Terminal	Symbol	Typ	Max	Unit
Input	C_{IN}	10	20	pF
Output	C_{OUT}	10	20	pF
I/O	$C_{I/O}$	10	20	pF

Note:
(1) Values do not include package pin capacitance.

Power Consumption

Description	Limits	Unit
Internal Cell (@ 5 V supply voltage)	8	µW/MHz
Input block (FI01)	46	µW/MHz
Output block (F002 @ 15 pF)	780	µW/MHz

Recommended Operating Conditions

		CMOS Level		TTL-Level (1)		TTL-Level (2)		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Power supply voltage	V_{DD}	4.5	5.5	4.75	5.25	4.5	5.5	V
Ambient temperature	T_A	-40	+85	0	70	-40	+85	°C
Low-level input voltage	V_{IL}	0	0.3 V_{DD}	0	0.8	-0.5	0.77	V
High-level input voltage	V_{IH}	0.7 V_{DD}	V_{DD}	2.2	V_{DD}	2.29	V_{DD}	V
Input rise or fall time	t_R, t_F	0	200	0	200	0	200	ns
Input rise or fall time, Schmitt	t_R, t_F	0	10	0	10	0	10	ms
Positive trigger voltage	V_P	1.8	4.0	1.2	2.4	1.15	2.54	V
Negative trigger voltage	V_N	0.6	3.1	0.6	1.8	0.59	1.85	ms
Hysteresis voltage	V_H	0.3	1.5	0.3	1.5	0.27	1.5	ms

(1) ± 5% supply voltage tolerance and 0..70° ambient temperature

(2) ± 10% supply voltage tolerance and -40..85° ambient temperature

AC Characteristics

V_{DD} = 5 V ± 0.5 V; T_j = -40 to +125°C

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Toggle frequency	f_{TOG}	120			MHz	D-F/F; F/O = 2
Delay time						
2-input NAND (F322)	t_{PD}		270		ps	F/O = 1; L = 0 mm
	t_{PD}		500		ps	F/O = 2; L = 2mm
Input buffer (FI01)	t_{PD}		1000		ps	F/O = 2; L = 2mm
Output buffer (FO01)	t_{PD}		2000		ps	C_L = 15 pF
Output rise time (FO01)	t_R		1.54		ns	C_L = 15 pF; 10-90%
Output fall time (FO01)	t_F		1.42		ns	C_L = 15 pF; 10-90%

DC Characteristics

(V_{DD} = 5 V ± 0.5 V; T_a = -40 to +85°C) and (V_{DD} = 5 V ± 0.25 V; T_a = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Quiescent current						
CMOS-6	I_{DDS}		0.1	280	µA	$V_I = V_{DD}$ or GND
CMOS-6A	I_{DDS}		0.1	100	µA	$V_I = V_{DD}$ or GND
CMOS-6S	I_{DDS}		0.1	tbd.	µA	$V_I = V_{DD}$ or GND
Off-state output leakage current	I_{OZ}			±10	µA	$V_O = V_{DD}$ or GND
Output sink short circuit current	I_{OS}			-250	mA	V_O = GND

DC Characteristics

V_{DD} = 5 V ± 0.5 V; T_a = -40 to +85°C

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Input leakage current						
Regular	I_I		$\pm 10^{-5}$	±10	µA	$V_I = V_{DD}$ or GND
50 kΩ pull-up	I_I	-45	-131	-320	µA	V_I = GND
5 kΩ pull-up	I_I	-0.35	-1.0	-2.20	mA	V_I = GND
50 kΩ pull-down	I_I	45	131	320	µA	$V_I = V_{DD}$
Pull-up resistor						
50 kΩ pull-up	R_{PU}	17.2	38.2	100.0	kΩ	
5 kΩ pull-up	R_{PU}	2.5	5.0	12.9	kΩ	
50 kΩ pull-down	R_{PD}	17.2	38.2	100.0	kΩ	
Low-level output current						
4.5 mA (CMOS)	I_{OL}	4.50			mA	V_{OL} = 0.4 V
9.0 mA (CMOS)	I_{OL}	9.00			mA	V_{OL} = 0.4 V
13.5 mA (CMOS)	I_{OL}	13.50			mA	V_{OL} = 0.4 V
18.0 mA (CMOS)	I_{OL}	18.00			mA	V_{OL} = 0.4 V
24.0 mA (CMOS)	I_{OL}	24.00			mA	V_{OL} = 0.4 V
Low-level output voltage	V_{OL}			0.1	V	I_{OL} = 0 mA
High-level output current						
4.5 mA (CMOS)	I_{OL}	-2.50			mA	$V_{OH} = V_{DD}$ - 0.4 V
9.0 mA (CMOS)	I_{OL}	-5.00			mA	$V_{OH} = V_{DD}$ - 0.4 V
13.5 mA (CMOS)	I_{OL}	-7.50			mA	$V_{OH} = V_{DD}$ - 0.4 V
18.0 mA (CMOS)	I_{OL}	-10.00			mA	$V_{OH} = V_{DD}$ - 0.4 V
24.0 mA (CMOS)	I_{OL}	-14.00			mA	V_{OH} = 2.4 V
High-level output voltage	V_{OH}	V_{DD}-0.1			V	I_{OH} = 0 mA

DC Characteristics

V_{DD} = 5 V ± 0.25 V; T_a = 0 to +70°C

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Input leakage current						
Regular	I_I		$\pm10^{-5}$	±10	µA	$V_I = V_{DD}$ or GND
50 kΩ pull-up	I_I	-55	-131	-238	µA	V_I = GND
5 kΩ pull-up	I_I	-0.42	-1.0	-1.72	mA	V_I = GND
50 kΩ pull-down	I_I	55	131	238	µA	$V_I = V_{DD}$
Pull-up resistor						
50 kΩ pull-up	R_{PU}	22.1	38.2	86.4	kΩ	
5 kΩ pull-up	R_{PU}	3.1	5.0	11.3	kΩ	
50 kΩ pull-down	R_{PD}	22.1	38.2	86.4	kΩ	
Low-level output current						
4.5 mA (CMOS)	I_{OL}	4.98			mA	V_{OL} = 0.4 V
9.0 mA (CMOS)	I_{OL}	9.96			mA	V_{OL} = 0.4 V
13.5 mA (CMOS)	I_{OL}	14.94			mA	V_{OL} = 0.4 V
18.0 mA (CMOS)	I_{OL}	19.92			mA	V_{OL} = 0.4 V
9.0 mA (TTL)	I_{OL}	9.0			mA	V_{OL} = 0.4 V
18.0 mA (TTL)	I_{OL}	18.0			mA	V_{OL} = 0.4 V
Low-level output voltage						
CMOS buffers	V_{OL}			0.1	V	I_{OL} = 0 mA
TTL buffers	V_{OL}			0.1	V	I_{OL} = 0 mA
High-level output current						
4.5 mA (CMOS)	I_{OL}	-2.63			mA	$V_{OH} = V_{DD}$ - 0.4 V
9.0 mA (CMOS)	I_{OL}	-5.27			mA	$V_{OH} = V_{DD}$ - 0.4 V
13.5 mA (CMOS)	I_{OL}	-7.90			mA	$V_{OH} = V_{DD}$ - 0.4 V
18.0 mA (CMOS)	I_{OL}	-10.53			mA	$V_{OH} = V_{DD}$ - 0.4 V
9.0 mA (TTL)	I_{OL}	-0.50			mA	V_{OH} = 2.4 V
18.0 mA (TTL)	I_{OL}	-1.00			mA	V_{OH} = 2.4 V
High-level output voltage						
CMOS buffers	V_{OH}	V_{DD}-0.1			V	I_{OH} = 0 mA
TTL buffers	V_{OH}	2.6			V	I_{OH} = 0 mA

Publications

This data sheet contains specifications, package information, and operational data for the CMOS-6 gate array family. Additional design information is available in NEC's ASIC selection guide, CMOS-6 block library and design manual. Please ask your local NEC Design Center.