

TOSHIBA BIPOLAR DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

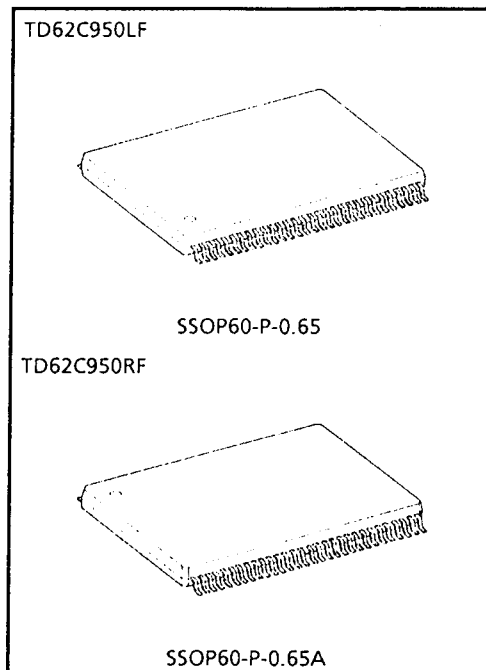
TD62C950RF, TD62C950LF

**TD62C950RF : 40BIT SHIFT REGISTER
/ LATCHES DRIVER (RIGHT SHIFT)**

**TD62C950LF : 40BIT SHIFT REGISTER
/ LATCHES DRIVER (LEFT SHIFT)**

FEATURES

- Low Power Consumption
- High Speed Operation : $f_{CK} = 4\text{MHz}$
- High Voltage Output : 70V
- Push/Pull Output : $-40\text{mA} / +2\text{mA}$
- 40bit Shift Register / Latches / Outputs
- Both Right-direction Shift type (RF) and Left-direction type (LF) are available.
- CMOS Interface
- Compact 60 Leads Plastic Package

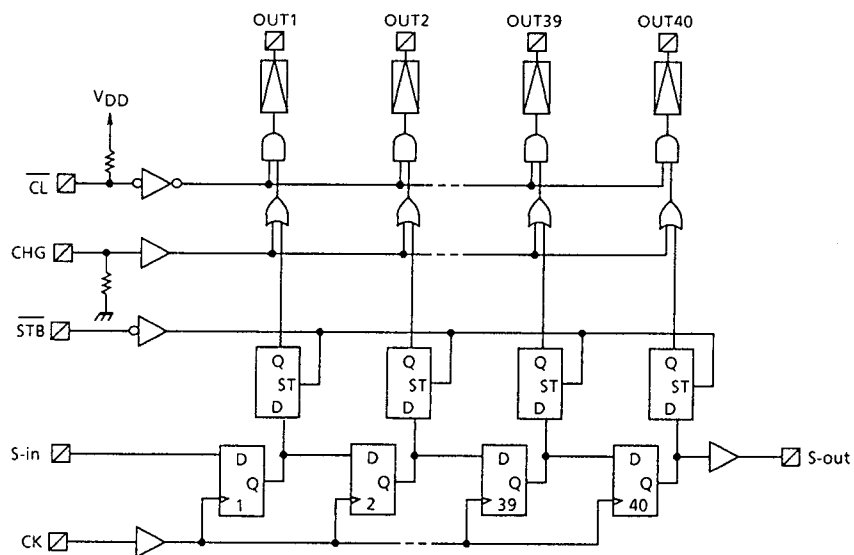


Weight SSOP60-P-0.65 : 1.47g (Typ.)
SSOP60-P-0.65A : 1.47g (Typ.)

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BLOCK DIAGRAM



PIN CONNECTION (TOP VIEW)


TD62C950LF

OUT40	1	60	OUT1
OUT39	2	59	OUT2
OUT38	3	58	OUT3
OUT37	4	57	OUT4
OUT36	5	56	OUT5
OUT35	6	55	OUT6
OUT34	7	54	OUT7
OUT33	8	53	OUT8
OUT32	9	52	OUT9
OUT31	10	51	OUT10
OUT30	11	50	OUT11
OUT29	12	49	OUT12
OUT28	13	48	OUT13
OUT27	14	47	OUT14
OUT26	15	46	OUT15
OUT25	16	45	OUT16
OUT24	17	44	OUT17
OUT23	18	43	OUT18
OUT22	19	42	OUT19
OUT21	20	41	OUT20
HVCC	21	40	HVCC
P-GND	22	39	P-GND
L-GND	23	38	L-GND
NC	24	37	CL
CHG	25	36	NC
NC	26	35	STB
CK	27	34	NC
NC	28	33	NC
S-out	29	32	S-in
VDD	30	31	VDD



TD62C950RF

OUT1	60	1	OUT40
OUT2	59	2	OUT39
OUT3	58	3	OUT38
OUT4	57	4	OUT37
OUT5	56	5	OUT36
OUT6	55	6	OUT35
OUT7	54	7	OUT34
OUT8	53	8	OUT33
OUT9	52	9	OUT32
OUT10	51	10	OUT31
OUT11	50	11	OUT30
OUT12	49	12	OUT29
OUT13	48	13	OUT28
OUT14	47	14	OUT27
OUT15	46	15	OUT26
OUT16	45	16	OUT25
OUT17	44	17	OUT24
OUT18	43	18	OUT23
OUT19	42	19	OUT22
OUT20	41	20	OUT21
HVCC	40	21	HVCC
P-GND	39	22	P-GND
L-GND	38	23	L-GND
CL	37	24	NC
NC	36	25	CHG
STB	35	26	NC
NC	34	27	CK
NC	33	28	NC
S-in	32	29	S-out
VDD	31	30	VDD

PIN FUNCTION

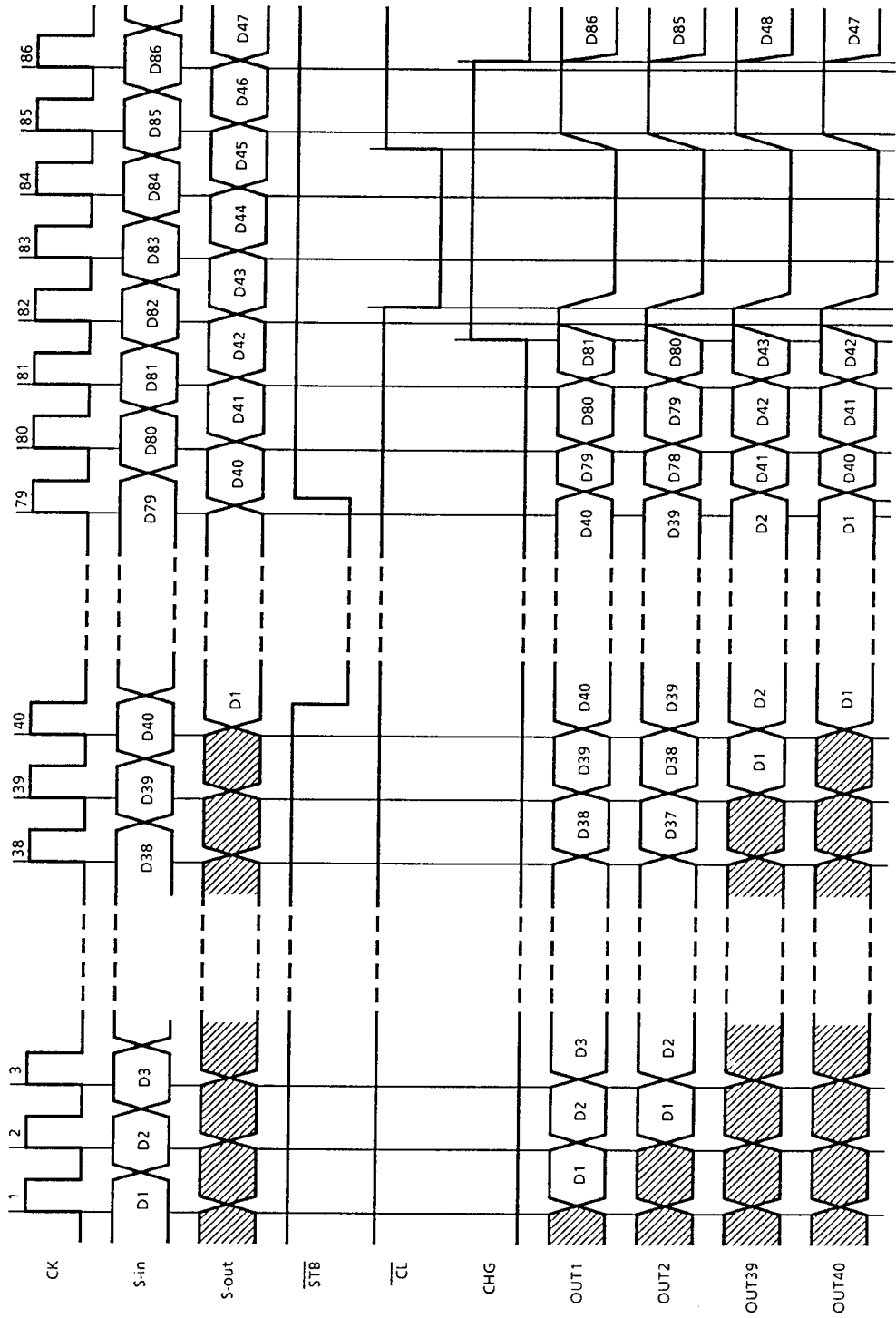
PIN No.	PIN NAME	FUNCTION
1~20 41~60	OUTn	Output terminal
21, 40	HV _{CC}	Supply voltage terminal for driver
22, 39	P-GND	Power GND (GND terminal for driver)
23, 38	L-GND	Logic GND (GND terminal for control)
37	\overline{CL}	"L" : All outputs "L" Pull up register equipped
35	\overline{STB}	"L" : Data latch "H" : Data through
32	S-in	Serial data input terminal for shift register
30, 31	V _{DD}	Supply voltage terminal for control logic
29	S-out	Serial data output terminal for shift register
27	CK	"  ": Data shift
25	CHG	If \overline{CL} = "H" at CHG = "L" input, it make all output "H". Pull down register equipped

TRUTH TABLE

CK	INPUT				OUTPUT			
	CHG	\overline{CL}	\overline{STB}	S-in	OUT1	OUTm	OUT40	S-out
	H	H	(*)	Dn	ALL H			Dn-39
	L	H	H	Dn	Dn	Dm-1	Dn-39	Dn-39
	L	H	L	Dn	Dn-1	Dn-m	Dn-40	Dn-39
	(*)	L	(*)	Dn	ALL L			Dn-39
	H	H	(*)	Dn	ALL H			Dn-40
	L	H	(*)	Dn	Dn-1	Dn-m	Dn-40	Dn-40
	(*)	L	(*)	Dn	ALL L			Dn-40

(*) "H" or "L"

TIMING CHART



MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Output Driver Supply Voltage	HVCC	70	V
Supply Voltage	VDD	7	V
Output Voltage	VOUT	GND - 2.0 ~ HVCC + 2.0	V
Input Voltage	VIN	GND - 0.5 ~ VDD + 0.5	V
Power Dissipation	PD	1.0	W
		1.3 (Note)	
Operating Temperature	Topr	-40 ~ 85	°C
Storage Temperature	Tstg	-55 ~ 150	°C

(Note) Mounted on a 60×60×1.6mm Cu 24% glass epoxy PCB.

RECOMMENDED OPERATING CONDITION (Ta = -40~85°C)

CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Driver Supply Voltage		HVCC	—	—	—	70	V
		VDD	—	4.5	5.0	5.5	
Output Current	"H" Level	S-out OUTn	IOH	—	—	-0.5	mA
				—	—	-40	
	"L" Level	S-out OUTn	IOL	—	—	0.5	
				—	—	2.0	
Input Voltage		VIN	—	GND	—	VDD	V
Operating Clock Frequency		fCK	—	—	4	8	MHz
Clock Pulse Width		tWCK	—	75	—	—	ns
Data Set Up Time		tsetup	—	50	—	—	ns
Data Hold Time		t hold	—	50	—	—	ns
Power Dissipation		PD	(*)	—	—	0.57	W

(*) On glass epoxy PCB (60×60×1.6mm Cu 24%)

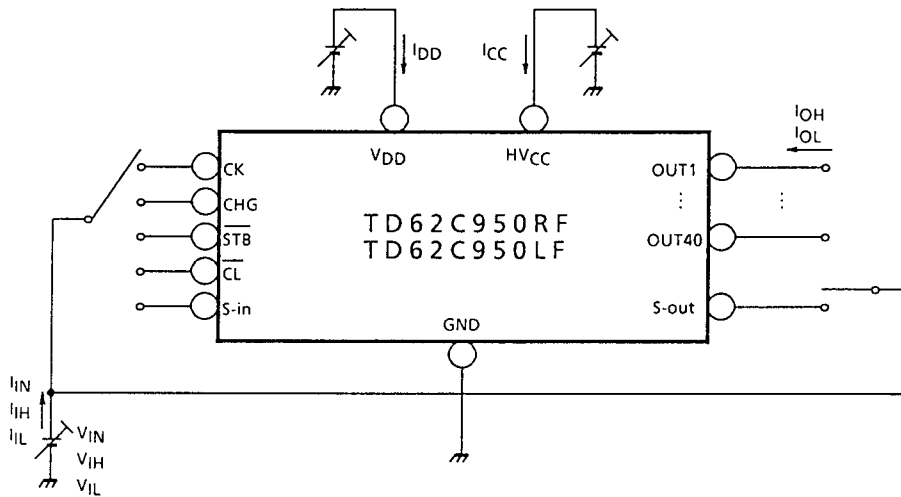
ELECTRICAL CHARACTERISTICS (Ta = 25°C)

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT		
Input Voltage	"H" Level	V _{IH}	—	—	70% V _{DD}	—	V _{DD}	V		
	"L" Level	V _{IL}	—	—	GND	—	30% V _{DD}			
Input Current		I _{IN}	—	CL = H, CHG = L	V _{DD} = 5.0V	—	—	± 1	μA	
				CL = L, CHG = L	V _{IN} = GND or V _{DD}	—	—	- 100		
				CL = H, CHG = H	V _{DD}	—	—	100		
Output Voltage	"H" Level	S-out	—	V _{DD} = 5V HV _{CC} = 70V	I _{OH} = - 20μA	4.9	4.95	—	V	
		OUTn			I _{OH} = - 40mA	65.0	66.5	—		
		OUTn			I _{OH} = - 10μA	68.0	68.5	—		
	"L" Level	S-out	I _{OL} = 20μA		—	0.01	0.1			
		OUTn	I _{OL} = 2mA		—	2.0	3.0			
		OUTn	I _{OL} = 10μA		—	0.8	1.0			
Quiescent Current		I _{CCH}	—	HV _{CC} = 70V V _{DD} = 5V	All output "H"	—	5.0	6.5	mA	
		I _{CCL}			All output "L"	—	—	10		μA
		I _{DD}			—	—	10			
Operating Supply Current		I _{CC} opr.	—	HV _{CC} = 70V V _{DD} = 5V	f _{CK} = 100MHz Duty = 50% CL = 0	—	6.0	7.0	mA	
		I _{DD} opr.			f _{CK} = 1MHz CL = 0	—	0.8	1.0		

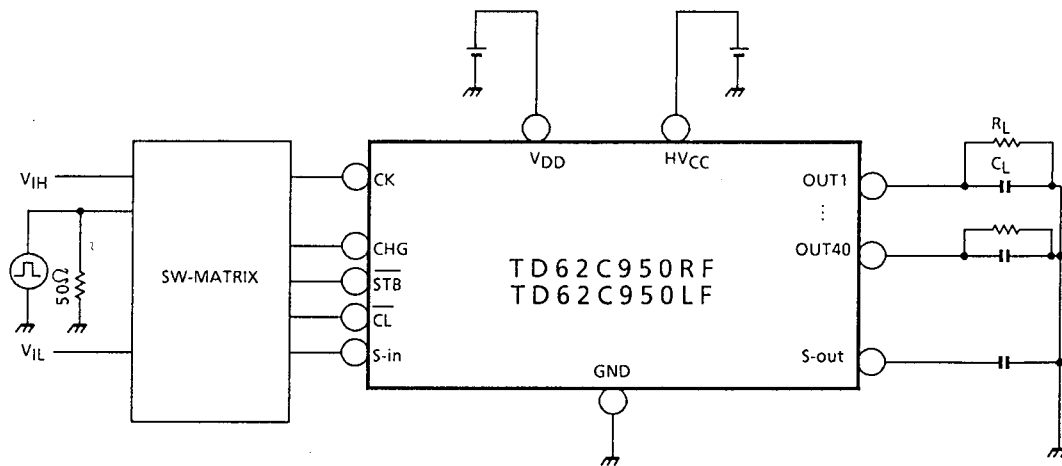
SWITCHING CHARACTERISTICS (Ta = 25°C)

CHARACTERISTIC		SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
Maximum Operating Clock Frequency		f (max)	—	HVCC = 70V VDD = 5V VIH = VDD VIL = GND CL (OUTn) = 50pF RL (OUTn) = 1.5kΩ CL (S-out) = 15pF	9	17	—	MHz	
Propagation Delay Time	"H" Level	CK-S-out	t _{pLH}		—	50	100	ns	
		CK-OUTn			—	0.6	1.2	μs	
		CL-OUTn			—	0.6	1.2		
		STB-OUTn			—	0.6	1.2		
	"L" Level	CK-S-out	t _{pHL}		—	50	100	ns	
		CK-OUTn			—	0.1	0.5	μs	
		CL-OUTn			—	0.1	0.5		
		STB-OUTn			—	0.1	0.5		
Minimum Pulse Width		CK	t _{w min}		—	70	—	—	ns
		STB			—	70	—	—	
Data Set Up Time		t _{setup}	—		20	—	—	ns	
CK-STB Set Up Time		t _{setup (STB)}	—		50	—	—	ns	
Data Hold Time		t _{hold}	—		20	—	—	ns	
Maximum Rise Time		t _r	—	—	—	1.0	μs		
Maximum Fall Time		t _f	—	—	—	1.0			
Output Rise Time	S-out	t _{or}	—	—	20	45	ns		
	OUTn		—	—	0.6	1.2	μs		
Output Fall Time	S-out	t _{of}	—	—	20	45	ns		
	OUTn		—	—	0.07	0.3	μs		

DC CHARACTERISTIC TEST CIRCUIT

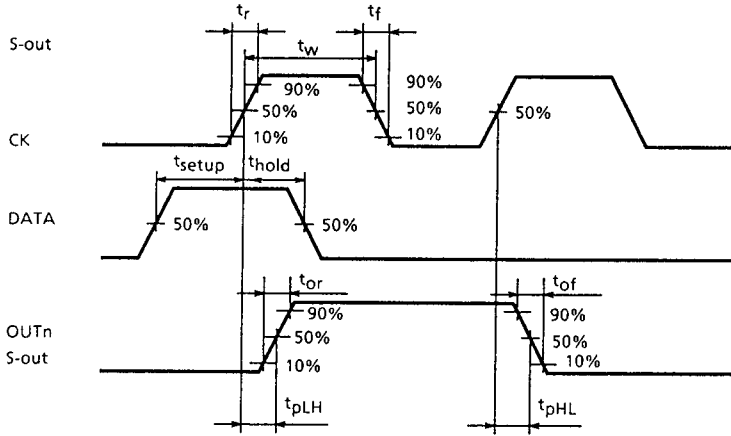


AC CHARACTERISTIC TEST CIRCUIT

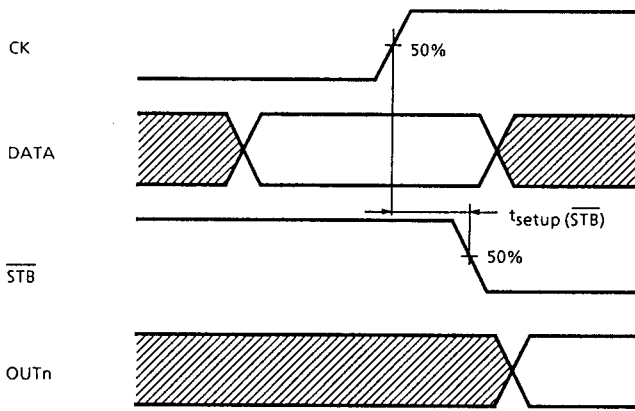


TIMING WAVEFORM

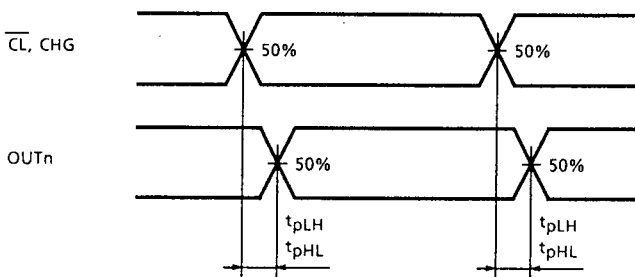
1. CK-OUTn



2. CK-STB

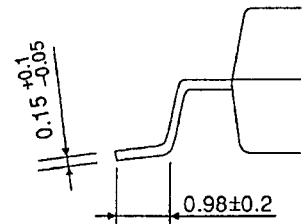
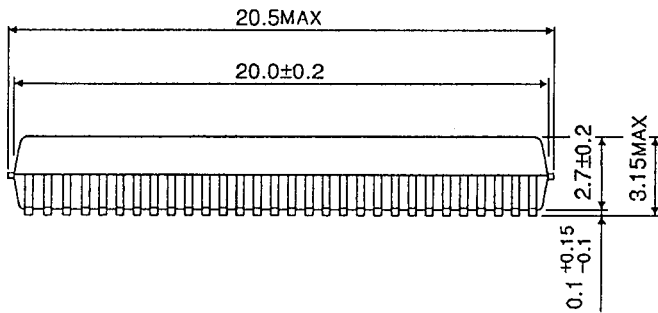
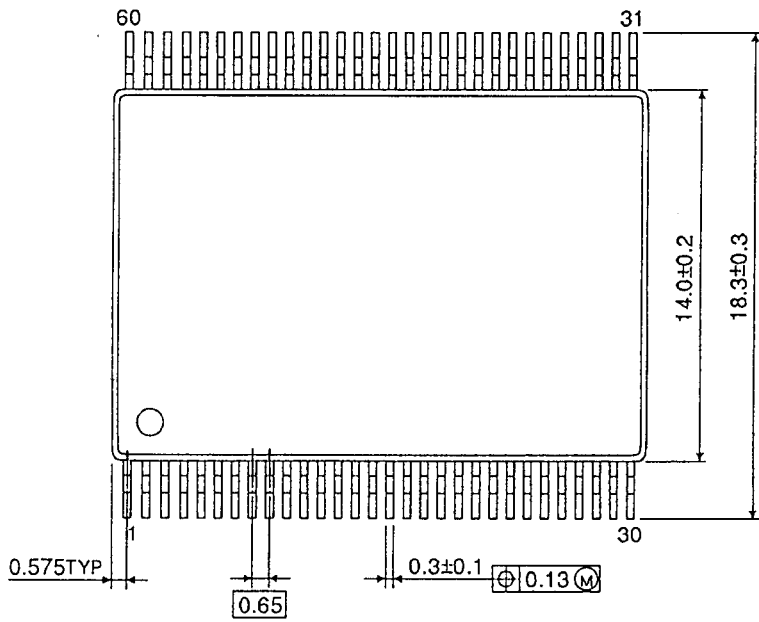


3. CHG, \overline{CL} -OUTn



OUTLINE DRAWING
SSOP60-P-0.65

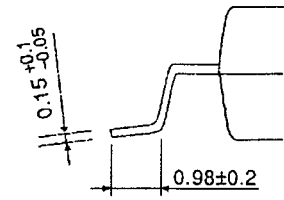
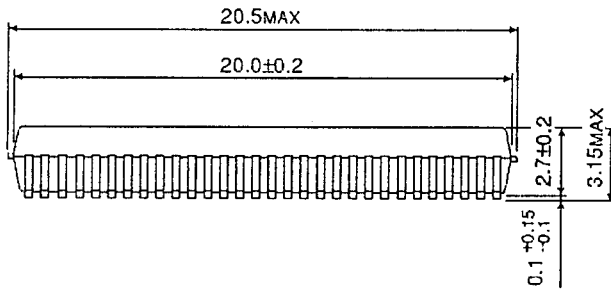
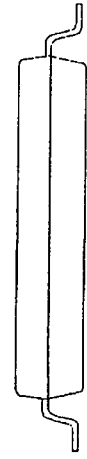
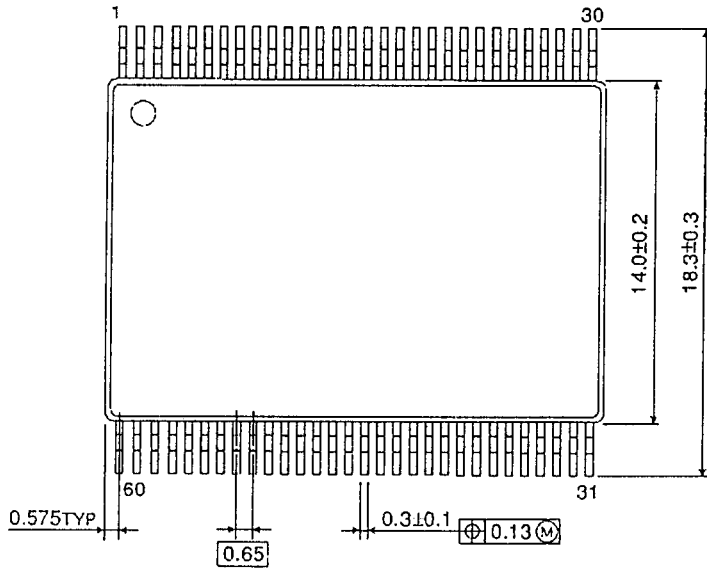
Unit : mm



Weight : 1.47g (Typ.)

OUTLINE DRAWING
SSOP60-P-0.65A

Unit : mm



Weight : 1.47g (Typ.)