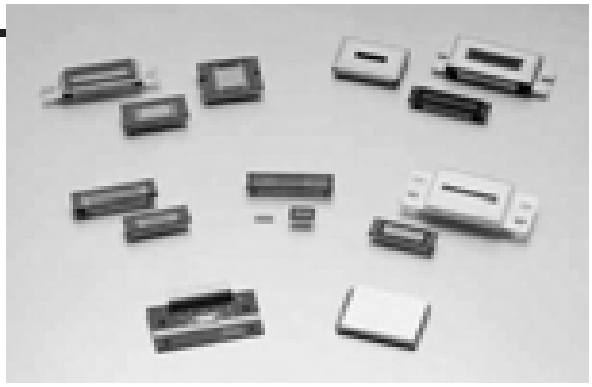
CHAPTER 04

Image sensors

Image sensors



For many years HAMAMATSU has developed image sensors for measurement in broad wavelength and energy regions from infrared to visible light, to ultraviolet, vacuum ultraviolet, soft X-rays, and hard X-rays. We provide a wide range of image sensors for diverse applications and meticulously respond to customer needs such as for different window materials, filter combinations, and optical fiber couplings. We also supply driver circuits that are optimized for sensor evaluation or installation in equipment, as well as easy-to-use multichannel detector heads.

Back-thinned CCD area image sensors are suitable for low-level light detection because of their high UV sensitivity, high S/N, and wide dynamic range. These sensors are extensively used in scientific and industrial fields such as DNA analysis, spectrophotometry, and semiconductor inspection systems, as well as in the medical field.

Front-illuminated CCD area image sensors are used for imaging and measurement in the visible and near infrared region. Their applications have been recently expanded to include high-resolution X-ray imaging by coupling them to an FOP (fiber optic plate) with scintillator for use in medical equipment such as for dental diagnosis and in industrial non-destructive inspection.

NMOS linear image sensors are suitable for precision spectrophotometry because of their high UV sensitivity and superb linearity. CMOS linear image sensors are well suited for industrial applications that require small, low-cost, and low-power consumption image sensors. We also provide photodiode arrays with amplifiers, which have a unique hybrid structure comprised of a photodiode array with a freely changeable pitch and a CMOS amplifier array chip. These photodiode arrays serve as sensors for identifying paper money. When combined with a scintillator, these photodiode arrays are also used for non-destructive X-ray inspection of food and industrial materials.

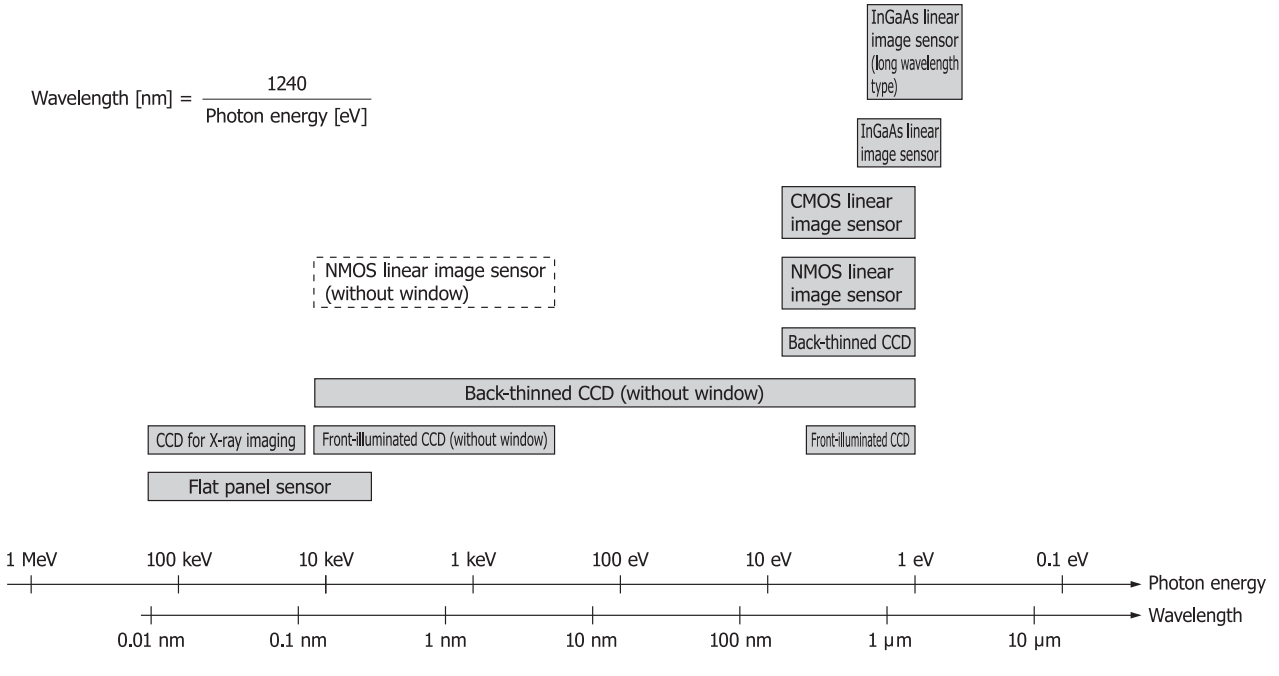
InGaAs linear image sensors consisting of an InGaAs photodiode array and CMOS charge amplifier array are used as sensors for near infrared spectrometry and DWDM monitoring.

HAMAMATSU also provides flat panel sensors developed for X-ray detection, which combine a scintillator with a large-area CMOS image sensor made from monocrystalline silicon. (See Chapter 8, “X-ray detectors.”)

HAMAMATSU image sensors

Type	Lineup	Features
CCD area image sensor	● Front-illuminated type (for spectrophotometry, long integration type, large area type, for X-ray imaging) ● Back-thinned type (for spectrophotometry, large full well type, high-speed type)	Image sensors with high S/N optimized for low-light-level detection. In particular, the back-thinned type offers high quantum efficiency down to the vacuum UV region (90% or more at peak). Sensitivity stability is excellent over a wide spectral range from visible light to X-rays.
NMOS linear image sensor	● Current output type (infrared-enhanced type, fiber optic window type, for X-ray detection) ● Voltage output type	Image sensors that feature large pixel size, high UV sensitivity, and low noise. Dedicated driver circuits and pulse generators are also available.
CMOS linear image sensor	● Standard type ● High-speed readout type ● Digital output type ● UV-enhanced type ● Plastic package	Self-scanning photodiode arrays with an internal signal processing circuit. Since a timing generator is already included for generating various types of drive clock pulses, these operate simply by supplying clock pulses, start pulses, and 5 V.
Photodiode array with amplifier	● Long and narrow area type ● For X-ray detection	Sensors combining a Si photodiode array and a signal processing IC. A long, narrow image sensor can also be configured by arranging multiple arrays in a row.
InGaAs linear image sensor	● For NIR spectrometry ● For DWDM monitor	Image sensors for near infrared region. Built-in readout circuit allows easy handling.
Flat panel sensor	● For radiography ● For X-ray non-destructive inspection	Sensors for capturing X-ray images in real time.

Energy/spectral range detectable by image sensors (e ample)



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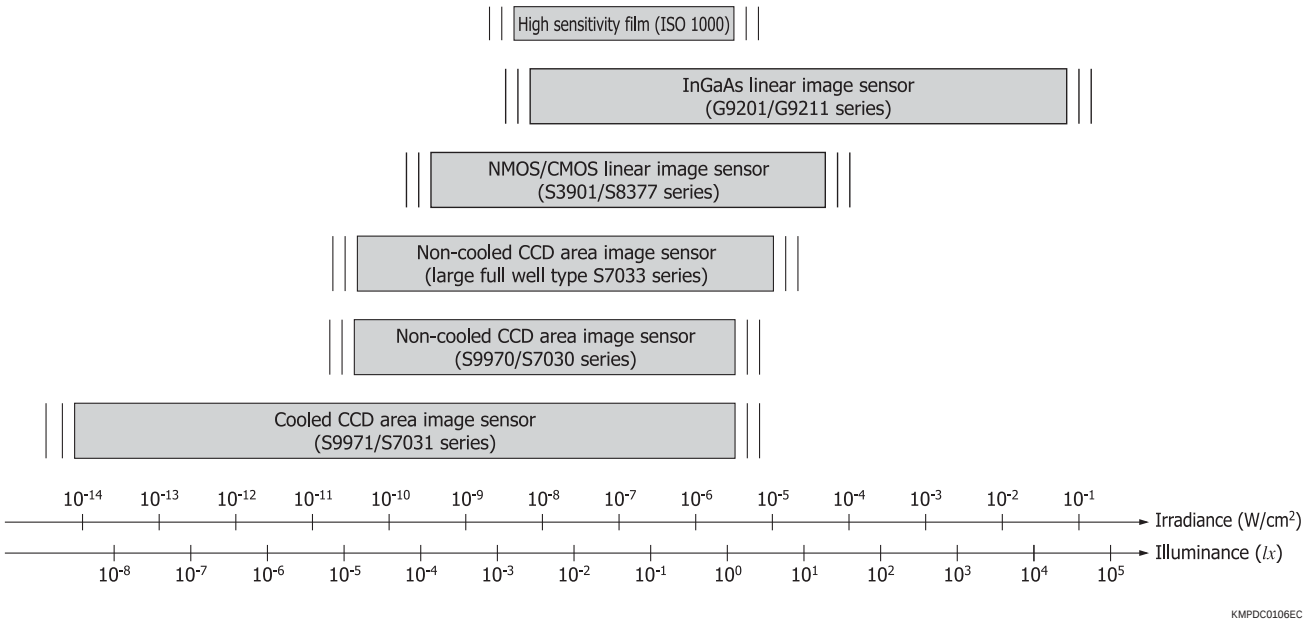
Light level range detectable by image sensors (e ample)



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1. CCD area image sensors

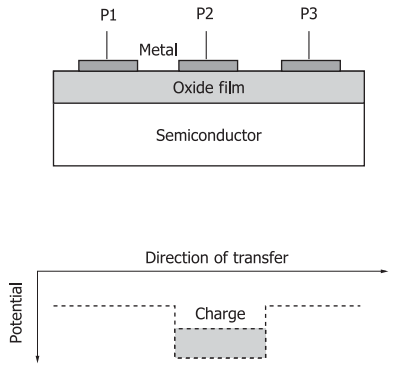
1-1 Structure and operating principle

CCD area image sensors (referred to simply as CCD from now on) are semiconductor devices invented by Willard Boyle and George Smith at the AT&T Bell Laboratories in 1970. CCDs are image sensors grouped within a family of charge transfer devices (CTD) that transfer charges through the semiconductor by using potential wells. Most current CCDs have a buried channel CCD (BCCD) structure in which the charge transfer channels are embedded inside the substrate.

As shown in Figure 1-1, a CCD potential well is made by supplying one of multiple MOS (metal oxide semiconductor) structure electrodes with a voltage which is different from that supplied to the other electrodes. The signal charge packed in this potential well is sequentially transferred through the semiconductor toward the output section. Because of this, the CCD is also called an analog shift register.

CCDs are essentially semiconductor devices through which a signal charge is transferred. Currently, however, the term "CCD" has come to signify image sensors and video cameras since CCDs are widely used as image sensors.

Figure 1-1 CCD basic structure and potential well



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CCD types

Currently used CCDs are grouped by their transfer method into the following five types.

(1) FT (frame transfer) type
(2) FFT (full frame transfer) type
(3) IT (interline transfer) type
(4) FIT (frame interline transfer) type
(5) One-dimensional type

Types except for the FFT and one-dimensional types are widely used in general-purpose video cameras. FFT and one-dimensional types are not suitable for use in video cameras because of their operating principle, and are mainly used in measurement and analysis applications.

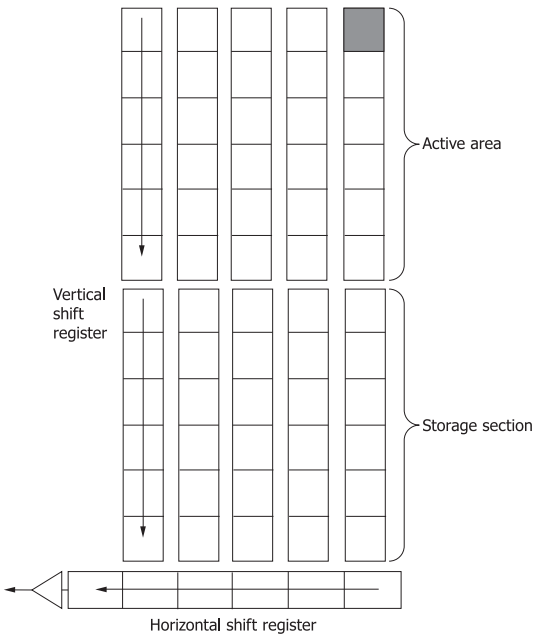
(1) FT type

The FT type CCD (FT-CCD) is comprised of two vertical shift registers for the active area and storage section, one horizontal shift register, and an output section. Vertical shift registers are also referred to as parallel registers, while the horizontal register is called the serial register or readout register. Transparent electrodes such as made from poly-silicon are generally employed as the electrodes for the active area.

When light comes through a transparent electrode into the CCD semiconductor, photoelectric conversion occurs and a signal charge is generated. This signal charge is collected into the potential well beneath the electrode. By utilizing the vertical blanking period, this signal charge is transferred at high speed to the storage section for each frame. Therefore in the FT type, the vertical shift register in the active area acts as a photoelectric converter device during the integration time.

The signal charge in the storage section is transferred to the output section through the horizontal shift register, while photoelectric conversion and signal accumulation take place in the active area. The signal charge is transferred to the horizontal shift register for each line in the storage section during the horizontal blanking period. In the FT type, all areas other than the active areas are covered with an opaque metal such as aluminum that prevents light from entering.

Figure 1-2 Structure of FT type



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(2) FFT type

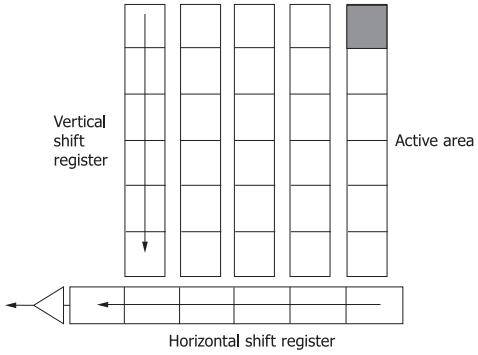
The FFT type CCD (FFT-CCD) basically has the same structure as the FT type except that there is no storage section. Because there is no storage section, the FFT type is usually used along with some type of external shutter mechanism. This limitation

makes it difficult to use the FFT type in video cameras.

The operating principle of the FFT type is similar to that of the FT. The signal charge is collected in a potential well in the active area during the integration time and then transferred to the output section via the horizontal shift register during the external shutter closed period, etc.

Since there is no storage section, the FFT type can be fabricated with a larger number of pixels or with a larger pixel size while using the same chip size, so the FFT type is mainly used for measurement camera systems with a slow frame rate. Most HAMAMATSU CCDs are the FFT type.

Figure 1-3 Structure of FFT type



(3) IT type

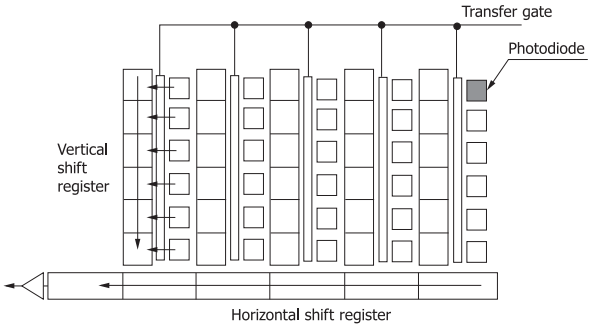
The IT type CCD (IT-CCD) has an active area consisting of photodiodes or MOS structure diodes formed separately from the transfer section. Recent IT types use buried photodiodes with a low dark current. Vertical shift registers are arranged along photodiodes, and horizontal shift registers and output sections are also configured.

The signal charge produced by photoelectric conversion in a photodiode is stored in the junction capacitance of the photodiode itself and others. This charge is then transferred to the vertical shift register during the vertical blanking period through the transfer gate which is provided as a switch between the photodiode and the vertical shift register. This operation differs from the FT type in that the charge transfer from the photodiode to the vertical shift register is performed for all pixels simultaneously.

Subsequent operations are exactly the same as the FT type operation following “signal transfer to the storage section,” so the signal charge is transferred to the horizontal shift register for every line during the horizontal blanking period.

Figure 1-4 shows a simplified structure of the IT type. As with the FT type, areas other than the photodiodes are light-shielded with aluminum, etc. In the IT type, the signal charge is transferred from the storage section to the output section by using the period in which the charge is accumulated in the photodiode. This tends to cause a phenomenon called “smear” due to the signal charge leaking into the vertical shift register.

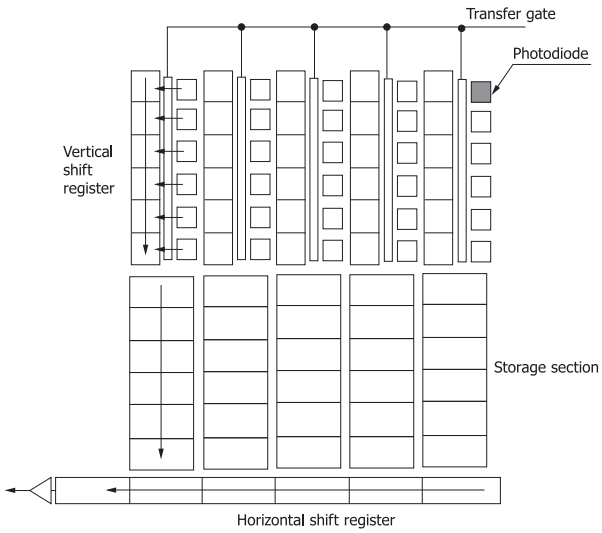
Figure 1-4 Structure of IT type



(4) FIT type

The FIT type CCD (FIT-CCD) was developed to solve the problems of the IT type CCD. The FIT type is configured basically by adding a storage section to the IT type. In the FIT type, as soon as a signal charge is transferred from the photodiodes to the vertical shift registers, the charge is transferred to the storage section at high speeds. The FIT type therefore ensures reduced smear compared to the IT type.

Figure 1-5 Structure of FIT type



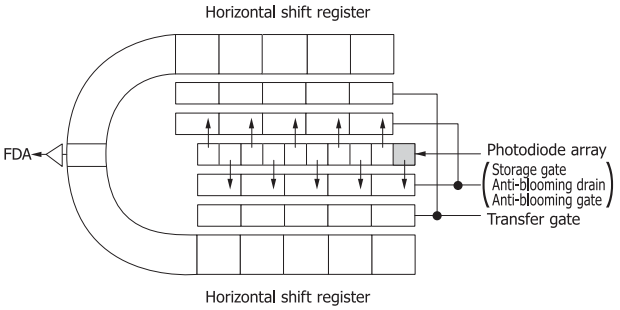
(5) One-dimensional type

In a one-dimensional type CCD, the signal charge generated by photoelectric conversion in a photodiode is collected in the adjacent storage gate. The signal charge is then transferred to the horizontal shift register through the transfer gate provided as a switch between the storage gate and the horizontal shift register. Charge transfer from the storage gate to the horizontal shift register is performed for all pixels simultaneously.

Figure 1-6 shows the structure of a one-dimensional type CCD. Signal charges from odd pixels in the photodiode array are transferred to the upper horizontal shift register, and signal charges from even pixels are transferred to the lower horizontal shift register. Those signal charges are alternately detected by a single FDA (floating diffusion amplifier). Transferring the odd pixel signal charges and even pixel signal charges to the

separate horizontal shift registers makes it possible to fabricate a photodiode array with a small pitch and to form anti-blooming and electronic shutter structures.

Figure 1-6 Structure of one-dimensional type



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Charge transfer operation

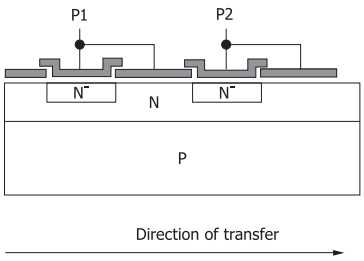
CCDs using two electrodes (gates) for one pixel are called two-phase (drive) CCDs or two-gate CCDs. Figure 1-7 shows the operating principle of a 2-phase CCD in which the signal charge is transferred by applying two clock pulses with different voltage levels (high level and low level). See Figure 1-7 (c).

In a 2-phase CCD, the signal charge is transferred in the direction determined by the difference in potential created in the semiconductor process. The signal charge is stored beneath the storage electrode. In Figure 1-7 for example, the signal charge is stored beneath the storage electrode for electrode P1 by setting electrode P1 to high level (setting electrode P2 to low level) at time t1.

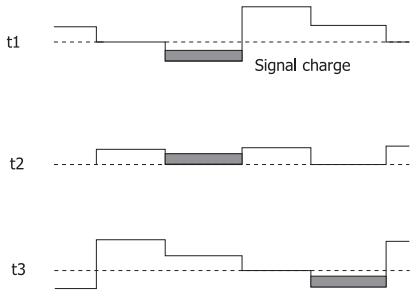
It is important in 2-phase CCDs to optimize the overlapping of clock pulses. As shown in the timing chart of Figure 1-7 (c), clock pulses must cross each other (at time t2) at a level higher than the midpoint of the high and low levels for P1 and P2 (for example, if the high level is V and the low level is 0, the cross point should be higher than V/2). The signal charges can be transferred by setting the clock phase so that P1 alternately goes high and low, while P2 goes low and high.

Figure 1-7 Operating principle of 2-phase CCD

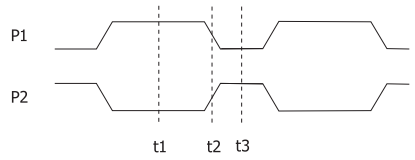
(a) Structure



(b) Potential



(c) Timing chart



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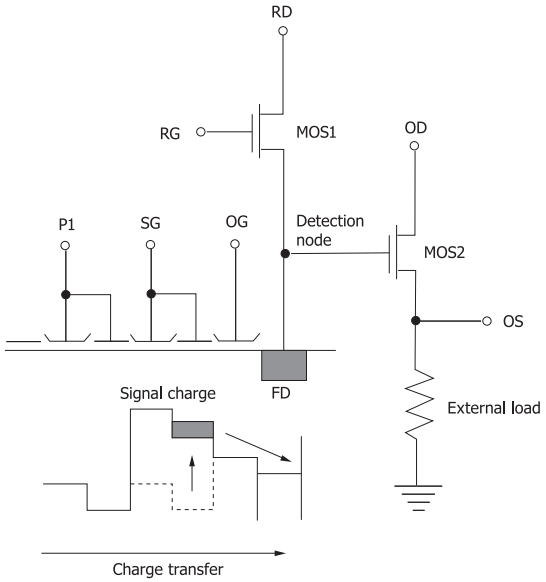
FDA

FDA is the most popular method for detecting the signal charge of a CCD. As shown in Figure 1-8, the FDA consists of a node for detecting charges and two MOSFETs (MOS1 for reset and MOS2 for charge-to-voltage conversion) connected to the node. The charge transferred to the detection node is converted into a voltage by MOS2 via the relation Q = C V. The detection node is reset by MOS1 to the reference level (voltage on RD) in order to read the next signal.

Noise accompanying the charge detection by FDA is determined by the capacitance of the node but can be almost entirely eliminated by CDS (correlated double sampling).

The signal charge output timing is synchronized with the timing at which the summing gate (SG) goes from high level to low level, which is the last clock gate for the shift register.

Figure 1-8 CCD output section using FDA



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Binning of signal charges

During CCD operation, a signal charge accumulates in the potential well of every pixel during the integration time. In FFT-CCDs, this means that the charge information is stored in two dimensions at the end of the integration time as shown in Figure 1-9 (a).

Since clock pulses can be input separately to the vertical shift register and horizontal shift register, an operation called “binning” can be performed. Binning is an operation unique to CCDs, and can be grouped into line (vertical) binning and pixel (horizontal) binning, depending on the direction that the signal charge is added.

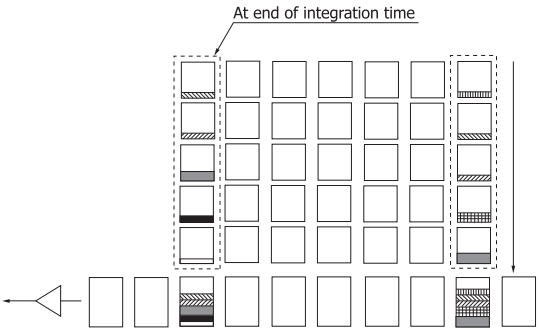
(1) Line binning

In line binning, the signal of each pixel is summed in the vertical direction. As shown in Figure 1-9 (b), the signal charge of each vertical pixel is sequentially transferred and added to one corresponding pixel of the horizontal shift register by applying a specified number of clock pulses P1V and P2V to the vertical shift register while the horizontal shift register clock pulse P1H is halted.

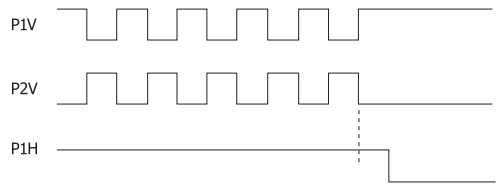
Line binning allows obtaining a signal which is equivalent to that obtained from a one-dimensional sensor having a very long active area in the vertical direction. Noise intrusion resulting from signal readout can be minimized since signal readout from the output section is performed at one time.

Figure 1-9 Line binning

(a) Signal charge ow



(b) Timing chart



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(2) Pixel binning

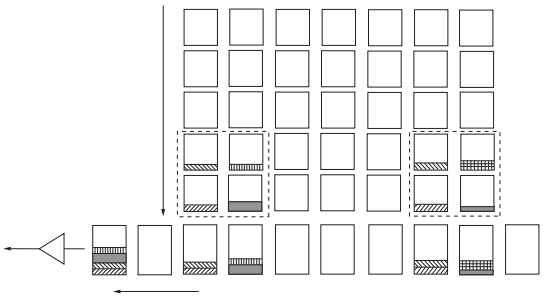
The last gate of the horizontal shift register in a CCD is an independent gate called the summing gate (SG). During operation not using pixel binning, the SG terminal is directly shorted to P2H (or the same clock pulses as P2H may be input to SG without shorting SG to P2H). Pixel binning can be performed by supplying a different clock pulse to SG.

When used in combination with line binning, signals from 2 × 2 pixels for example can be summed as shown in Figure 1-10. In this case, the signals of two vertical lines are first summed by line binning into the pixels of the horizontal shift register. Next, in the signal charge readout by the horizontal shift register, the signals of the two horizontal pixels can be transferred and summed by applying just one clock pulse to the SG terminal during each period of two P1H clock pulses.

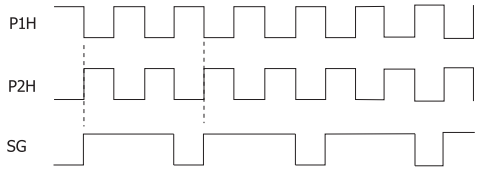
This method is effective in detecting low level light. For example, when the incident light level is too low to detect with a CCD having 1024 × 1024 pixels, operating it as a sensor having 512 × 512 pixels will acquire an image with higher contrast, although the spatial resolution will be lower.

Figure 1-10 Pi el binning

(a) Signal charge ow



(b) Timing chart



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Signal charge injection

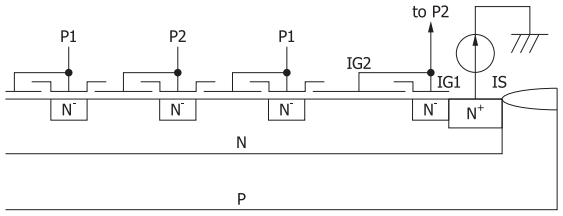
CCDs have input sources (ISV, ISH) and input gates (IGV, IGH) each arranged at the respective heads of the vertical shift register and horizontal shift register as the signal input terminals for electrical tests. In normal operation, a specified bias (see datasheets) should be applied to these test terminals. However, by applying a bias and clock pulses other than the specified values to these input sources and gates, a signal charge can be injected into the shift registers. This will reduce radiation-induced degradation of the CCD charge transfer efficiency. These terminals can also make quantitative evaluations of the full well capacity and the FDA linearity. A signal charge can also be injected into the shift registers by connecting a current source to the input sources and shorting the input gates to P2 for clock pulse input [Figure 1-11]. The signal charge injected by this method equals the product of the injection current value from the current source and the injection time (reciprocal of

CCD drive frequency).

$$Qinj = Iinj \times t \cdots\cdots (1)$$

Qinj: injection charge [C]
Iinj : injection current [A]
t : injection time [s]

Figure 1-11 Structure of signal charge injection section connected to current source



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Comparison with NMOS image sensor

The structure of CCD image sensors differs from NMOS image sensors, so their specifications and performance are also quite different from each other.

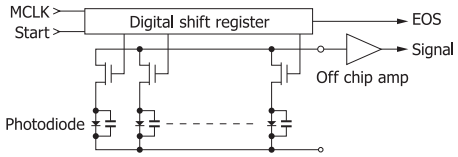
In NMOS image sensors, the signal charge accumulated in each photodiode is output to the signal line through a MOSFET switch by sequentially addressing the signal charge by a digital shift register. The operation at this point is performed by supplying TTL level clock pulses at a constant timing to the digital shift register, so that NMOS image sensors operate with just a single 5 V supply, except for the power to external signal processing sections.

On the other hand, CCD image sensors (IT type and one-dimensional type) transfer the signal charge accumulated in each photodiode to the analog shift register by turning on the MOSFET switch. The signal charge is then sequentially transferred by the analog shift register to the FDA in the final stage and is output. Operating a CCD image sensor requires more than one power supply, and the clock pulse amplitude must match the specified value. CCD image sensors exhibit a low readout noise level from a few to a dozen electrons (e^- rms). They also allow a high-speed readout at a pixel rate of 10 MHz or more depending on the amplifier bandwidth for the FDA.

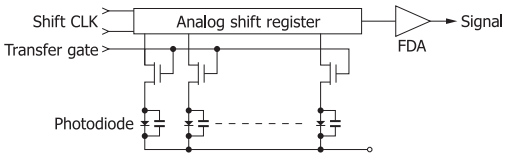
Although the noise level of NMOS image sensors runs as high as 3000 electrons (e^- rms), they can handle a signal charge over 100 times higher than CCD image sensors that typically handle several hundred thousand electrons (e^- rms). In general, if the light level to be detected is sufficiently high, using an NMOS image sensor is preferable because it simplifies the measurement system. In contrast, CCD image sensors have low noise and ensure an adequate S/N even at light levels that cannot be detected with NMOS image sensors. CCD image sensors are therefore suitable for low-light-level detection.

Figure 1-12 Comparison of NMOS and CCD image sensors

(a) NMOS image sensor



(b) CCD image sensor (IT type and one-dimensional type)



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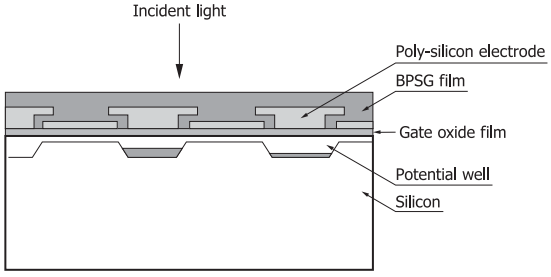
Front-illuminated type and back-thinned type

In general, CCDs are designed to receive light from the front side where circuit patterns are formed. This type of CCD is called the front-illuminated CCD. The light input surface of front-illuminated CCDs is formed on the front surface of the silicon substrate where a BPSG film, poly-silicon electrodes, and gate oxide film are deposited. Light entering the front surface is largely reflected away and absorbed by those components [Figure 1-13 (a)]. The quantum efficiency is therefore limited to approx. 40% at the highest in the visible region, and there is no sensitivity in the ultraviolet region.

Back-thinned CCDs [1] were developed to solve such problems. Back-thinned CCDs also have a BPSG film, poly-silicon electrodes, and gate oxide film on the surface of the silicon substrate, but they receive light from the backside of the silicon substrate [Figure 1-13 (b)]. Because of this structure, back-thinned CCDs deliver high quantum efficiency over a wide spectral range. Besides having high sensitivity and low noise which are the intrinsic features of CCDs, back-thinned CCDs are also sensitive to electron beams, soft X-rays, ultraviolet, visible, and near infrared light.

Figure 1-13 Schematic of CCDs

(a) Front-illuminated type



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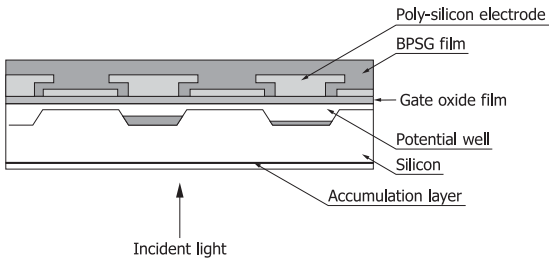
(b) Back-thinned type



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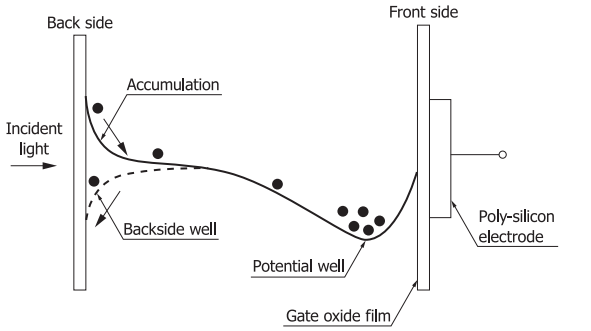
In order for back-thinned CCDs to achieve high sensitivity, it is essential to thin the silicon substrate and to activate the active area. The active area is activated by forming an internal potential (accumulation) so that signal charges generated near the backside light input surface are smoothly carried to the CCD potential wells without recombining.[2, 3] The internal potential in an accumulation state is shown in Figure 1-14.

Figure 1-14 Internal potential of back-thinned CCD



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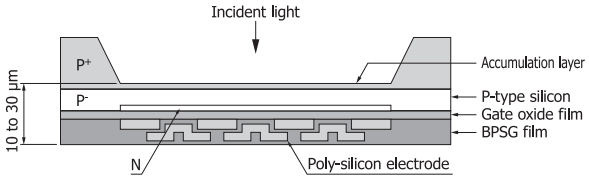
Fully-depleted back-illuminated CCD

Back-thinned CCDs have high quantum efficiency in the ultraviolet to visible region. However, since the silicon substrate is about 15 to 30 µm thick, the quantum efficiency in the near infrared (NIR) region is low. For example, the quantum efficiency at a wavelength of 1 µm is approx. 20%. Thickening the silicon substrate improves sensitivity in the near infrared region, but the resolution decreases due to diffusion of charges that are generated when the input photons are absorbed in the neutral region (undepleted region) near the backside light input surface.

Fully-depleted back-illuminated CCDs were developed to solve such problems. These fully-depleted back-illuminated CCDs use an ultra-high resistance N-type wafer to form a thick depletion layer. When the silicon resistivity is the same, the dopant concentration in N-type wafers can be reduced lower than that in P-type wafers, so the depletion layer can be thickened even when the same bias voltage is applied. On the other hand, MPP operation (see “Dark current” in section 1-2, “Characteristics”) is not possible because the bias voltage is applied to the backside (Vbb). Using a thick silicon substrate also causes the dark current to increase, so the CCD must be cooled to -70 to -100 °C. Since the silicon substrate thickness for back-thinned CCDs is about 10 to 30 µm, it is difficult to fabricate large-area devices. However, fully-depleted back-illuminated CCDs use a silicon substrate whose thickness is 100 to 300 µm over the entire area, so large-area devices can be easily fabricated.

Figure 1-15 Internal structure of back-illuminated CCD

(a) Back-thinned type



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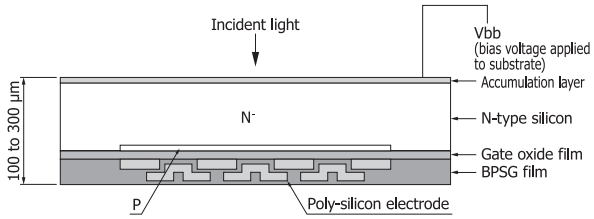
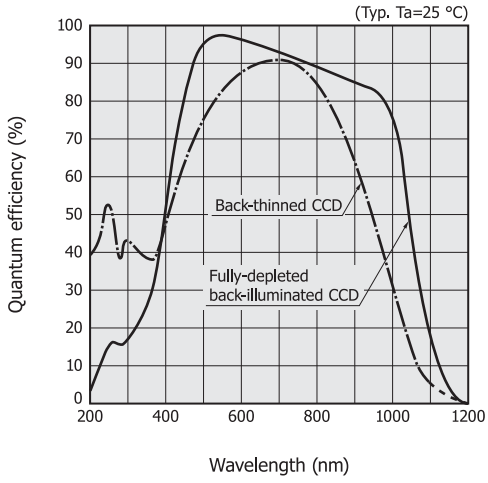
(b) Fully-depleted type



KMPDC0282EA

Figure 1-16 Spectral response (without window)



KMPDB0295EA

Multiport CCD

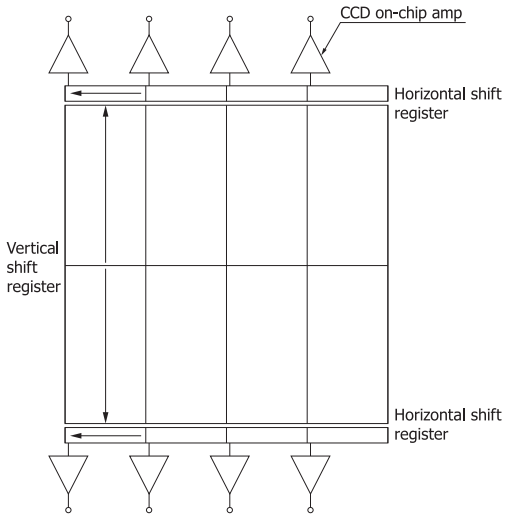
The readout time of a CCD is determined by the number of pixels and readout frequency, and readout usually takes a long time. For example, when reading out signals from 1024 × 1024 pixels at a readout frequency of 100 kHz, the readout time will be 10 seconds or longer.

There is a trade-off between the readout frequency and readout noise. Increasing the readout frequency shortens the readout time but increases the readout noise [Figure 1-39].

Using multiple CCD amplifiers (multiport configuration) allows

parallel readout of pixels and improves the frame rate (number of frames acquired per second).

Figure 1-17 Multiport CCD con guration



Thermoelectrically cooled CCD

CCD dark current varies with temperature; namely dark current is reduced by approx. one-half for every 5 to 7 °C decrease in temperature. As with MPP operation, cooling a CCD is an effective way to reduce the dark current and enhance the detection limit.

Thermoelectrically cooled CCDs contain a thermoelectric cooler (Peltier element) in the package, which efficiently cools the CCD. The cooling temperature is determined by heat absorption and heat dissipation capacities of the thermoelectric cooler. The following parameters differ depending on the thermoelectric cooler.

· Maximum current (Imax)
· Maximum voltage (Vmax)
· Maximum heat absorption (Qmax)

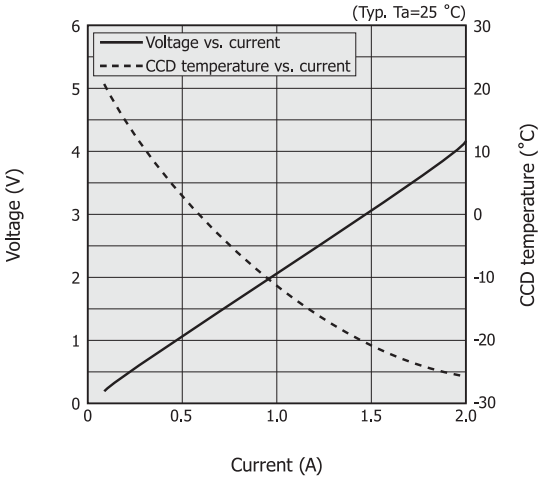
To avoid damaging a thermoelectric cooler and CCD, always operate them within the ratings specified in the datasheets. Heat dissipation methods are important when using a thermoelectric cooler. The cooling might be inadequate unless the heat is sufficiently dissipated. This is because the power consumption suddenly increases, and the temperature on the hot side of the thermoelectric cooler becomes high. In those cases, an optimal heatsink or forced air/water cooling, etc. is required. Thermoelectric coolers are designed to cool a CCD most efficiently when used at about 60% of the maximum current.

As a rough guide, CCDs are cooled to the following temperatures when the ambient temperature is 25 °C.

· One-stage thermoelectrically cooled type: approx. 0 to -10 °C
· Two-stage thermoelectrically cooled type: approx. -20 to -30 °C
· Four-stage thermoelectrically cooled type: approx. -50 to -70 °C

To ensure stable and reliable operation, the thermoelectric cooler current and heat dissipation condition should be determined according to the surrounding environment.

Figure 1-18 Cooling characteristics of one-stage thermoelectrically cooled type (S7171-0909)



TDI-CCD

Back-thinned TDI-CCDs allow acquiring high S/N images even under low-light conditions during high-speed imaging. TDI operation yields dramatically enhanced sensitivity by integrating the exposure of a moving object. The back-thinned structure ensures high quantum efficiency over a wide spectral range from the ultraviolet to the near infrared region (200 to 1100 nm).

TDI operation

In CCD operation, a signal charge is transferred to the output section while being held in potential wells so as not to mix with other individual charges. TDI operation makes good use of this CCD charge transfer principle, and it is an effective technique for detecting weak light and for imaging a moving object or a still object while scanning it with a CCD sensor that is itself being moved.

Normally, an image focused on the CCD sensor is output as a signal corresponding to the focused position. This means that the image focused within the integration time must stay in the same position on the CCD sensor. If, for some reason, the focused position is shifted, then the image S/N will deteriorate. When an object is moving, the focused position will shift, causing the image to blur or, in some cases, no image to appear. The TDI operation, in contrast, is a unique operation that captures images of a moving object. In FFT-CCD, signal charges in each column are vertically transferred during charge readout. TDI operation synchronizes this vertical transfer timing with the movement of the object, so signal charges are

integrated by a number of times equal to the number of vertical stages of the CCD pixels.
In TDI operation, the signal charges must be transferred in the same direction at the same speed as those of the object to be imaged. These speeds are expressed by equation (2).

$$v = f \times d \cdots\cdots (2)$$

v : object speed, charge transfer speed
f : vertical transfer frequency
d : pixel size (transfer direction)

In Figure 1-19, when the charge accumulated in the first stage is transferred to the second stage, another charge produced by photoelectric conversion is simultaneously accumulated in the second stage. Repeating this operation continuously until reaching the last stage M (number of vertical stages) results in a charge accumulation M times greater than the initial charge. This shows that the TDI operation enhances sensitivity up to M times higher than ordinary linear image sensors. (If the number of vertical stages is 128, the sensitivity will be 128 times higher than ordinary linear image sensors.) Since the accumulated signal charges are output for each column from the CCD horizontal shift register, a two-dimensional continuous image can be obtained. TDI operation also improves sensitivity variations compared to two-dimensional operation mode.

Figure 1-19 Schematic of integrated e posure in TDI operation

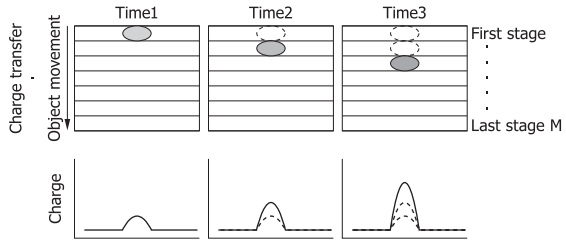


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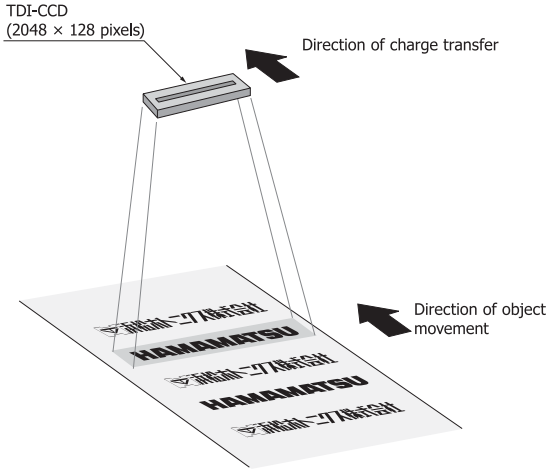
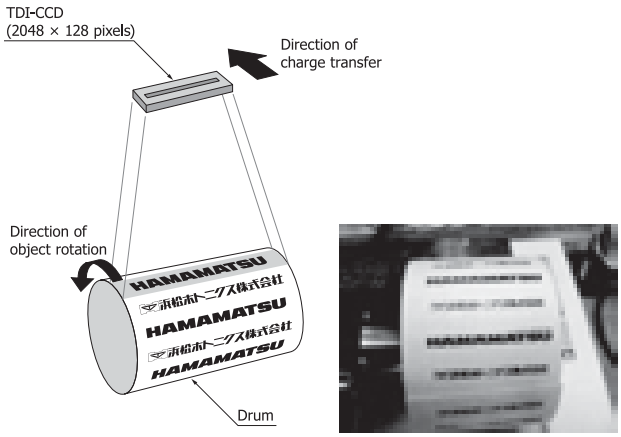
Figure 1-20 Imaging e ample in TDI operation
(a) Imaging of fast moving object



KMPDC0266EB

(b) Imaging of fast rotating object



KMPDC0267EA

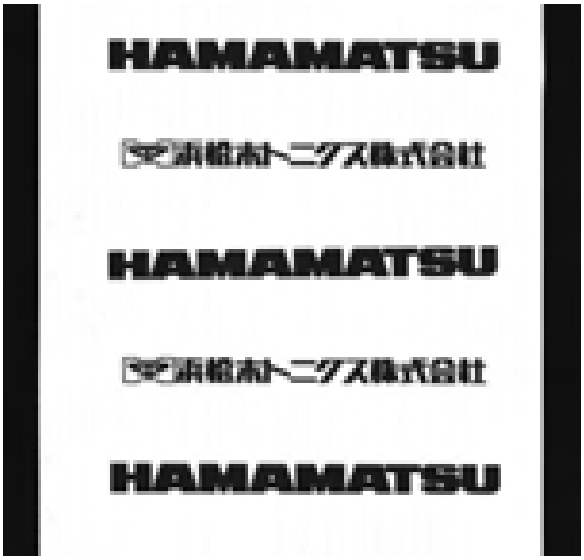
In Figure 1-20 (b), when the drum is imaged while in idle, a clear image with no blurring is obtained as shown in Figure 1-21 (a). However, when the drum is rotating, the image is blurred as shown in Figure 1-21 (b). Shortening the shutter time captures an unblurred image, but the image becomes dark as shown in Figure 1-21 (c). Using a TDI-CCD acquires clear, continuous images with no blurring since charge transfer is performed in the same direction at the same speed as those of the rotating drum.

Figure 1-21 Imaging in two-dimensional operation
(a) hen drum is in idle

(b) hen drum is rotating

(c) hen drum is rotating (with shutter time shortened)

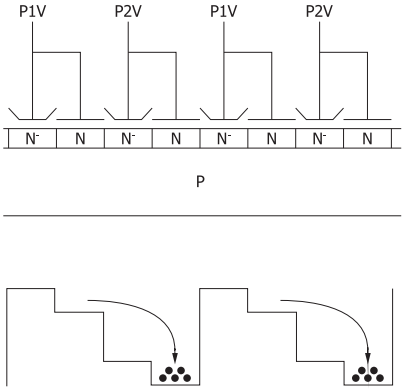
Figure 1-22 Imaging in TDI operation (continuous image during drum rotation)



Resistive gate structure

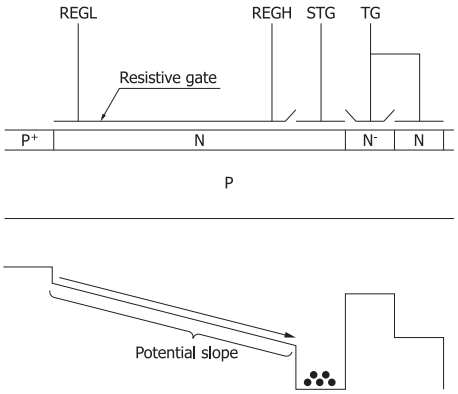
In ordinary CCDs, one pixel contains multiple electrodes and a signal charge is transferred by applying different clock pulses to those electrodes [Figure 1-23]. In resistive gate structures, a single high-resistance electrode is formed in the active area, and a signal charge is transferred by means of a potential slope that is created by applying different voltages across the electrode [Figure 1-24]. Compared to a CCD area image sensor which is used as a linear sensor by line binning, a one-dimensional CCD having a resistive gate structure in the active area offers higher speed transfer, allowing readout that leaves behind fewer unread charges even if the pixel height is large.

Figure 1-23 Schematic diagram and potential of ordinary 2-phase CCD



KMPDC0320EA

Figure 1-24 Schematic diagram and potential of resistive gate structure



KMPDC0321EB

1 - 2 Characteristics

Conversion factor

The conversion factor is the charge-to-voltage conversion ratio of an FDA.
The FDA converts a signal charge into a voltage, which is output from the output end OS as the voltage ΔVout.

$$\Delta Vout = Av \times Q / Cfd \cdots\cdots (3)$$

Av : voltage gain of charge-to-voltage conversion MOSFET
Q : signal charge [C]
Cfd: node capacitance [F]

The conversion factor (Sv) is expressed by equation (4).

$$Sv = q \times \Delta Vout / Q \ [V/e^-] \cdots\cdots (4)$$

q: electron charge
When S9970 series is used: Sv=2.0 μV/e⁻

The node capacitance (Cfd) is expressed by equation (5).

$$Cfd = q \times Av / Sv \ [F] \cdots\cdots (5)$$

When S9970 series is used: Cfd=44 fF

Spectral response

Figure 1-25 shows the spectral response of front-illuminated CCDs and back-illuminated CCDs. Front-illuminated CCDs have no sensitivity in the ultraviolet region, and the maximum quantum efficiency in the visible region is approx. 40%. In contrast, back-thinned CCDs deliver very high quantum efficiency, which is approx. 40% in the ultraviolet region and approx. 90% at a peak wavelength in the visible region. The fully-depleted back-illuminated CCDs use a thick silicon substrate which allows higher sensitivity in the wavelength range from 800 to 1200 nm than back-thinned CCDs. The fully-depleted back-illuminated CCDs also have high sensitivity in the visible region from 400 to 700 nm due to use of a special

AR (anti-reflection) coating process; however the ultraviolet sensitivity is low.

The spectral response range is determined on long wavelengths by the silicon substrate thickness and on short wavelengths by the sensor structure on the light input surface side. Front-illuminated FFT-CCDs require that poly-silicon gate electrodes be formed on the effective active area because of their structure, which makes the CCD almost insensitive to ultraviolet light at wavelengths shorter than 400 nm. To make it sensitive to ultraviolet light, a scintillator material called “Lumogen” is coated on the CCD surface of some front-illuminated types. Back-thinned CCDs, on the other hand, deliver a high quantum efficiency from ultraviolet to near infrared and also exhibit excellent stability even during exposure to ultraviolet light.

In the near infrared region at wavelengths longer than 700 nm, the quantum efficiency of standard front-illuminated CCDs is not so high (this depends on the depletion layer thickness), but the HAMAMATSU S9975 fully-depleted front-illuminated CCD delivers high quantum efficiency even in the near infrared region [Figure 1-26].

When a CCD is cooled during use, it should be noted that the sensitivity drops at wavelengths longer than approx. 800 nm [Figure 1-26].

Figure 1-25 Spectral response (without window)

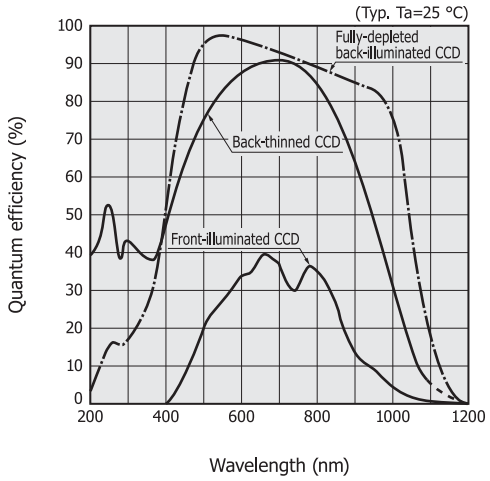


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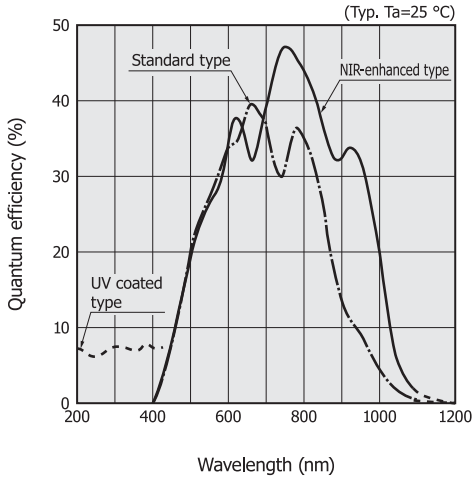
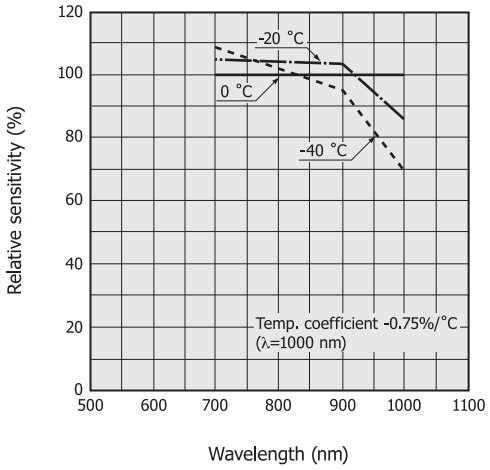
Figure 1-26 Spectral response of front-illuminated CCDs (without window)



KMPDB0205EB

Figure 1-27 Temperature characteristics of sensitivity (S9974-1007)



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Lumogen-coated front-illuminated CCD

The active area of front-illuminated CCDs is covered with poly-silicon electrodes. Ultraviolet light is almost totally absorbed by the poly-silicon, so the quantum efficiency in the ultraviolet region is nearly zero. To make the front-illuminated CCDs sensitive to ultraviolet light, a scintillator material “Lumogen” is sometimes used. Lumogen is directly coated on the CCD effective active area by vacuum sublimation.

Lumogen absorbs light at wavelengths shorter than 480 nm and emits light whose center wavelength is around 530 nm. In other words, ultraviolet light striking the CCD surface is converted to visible light which is then detected by the CCD.

Care should be taken when using a Lumogen-coated front-illuminated CCD because its life under ultraviolet light is extremely short and its sensitivity is highly dependent on temperature when compared to back-thinned CCDs.

Selecting window materials

Back-thinned CCDs provide high quantum efficiency over 90% at the peak sensitivity wavelength around 700 nm, but this is a value measured without a window.

The quantum efficiency of CCDs is affected by the window material. HAMAMATSU mainly uses three types of windows for CCDs: AR (anti-reflection) coated sapphire (S type), quartz (Q type), and windowless (N type).

Sapphire is mechanically strong and scratch-resistant compared to quartz and is stable in high humidity environments. In addition, since the thermal conductivity of sapphire is close to that of metal, it is less likely to cause moisture condensation and can be hermetically sealed within a metal package, making it an excellent choice as window material. The transmittance of sapphire having no AR coating is not so high, but AR coated sapphire has good transmittance which is higher than quartz in the visible region. HAMAMATSU thermoelectrically cooled CCDs such as the S9971/S7031 series use sapphire as a standard window material.

Quartz is available in two types: synthetic quartz and fused quartz. Synthetic quartz is more frequently used as the window for CCDs since it contains fewer metallic impurities. Even if there is no AR coating, quartz has high transmittance which is approx. 94% in the visible region, and the transmittance of AR coated quartz is more than 99%. Quartz transmits light down to a wavelength of 200 nm or shorter and so is suitable as a window material, especially when detecting ultraviolet light. However, compared to sapphire, quartz is less rugged and has lower thermal conductivity and can only be used with resin adhesives, so the usage environment must be taken into account when using it as a window material for cooled CCDs.

Naturally, CCDs not having a window exhibit the highest quantum efficiency. Windowless CCDs are sometimes used especially in the vacuum ultraviolet region at wavelengths shorter than 160 nm because appropriate window materials are not available in that region.

Other window materials include borosilicate glass which is less expensive than quartz. Borosilicate glass is mainly used to detect visible and longer wavelength light since its transmittance sharply drops from wavelengths around 300 nm. To detect X-rays, aluminum or beryllium is used as the window material which allows X-rays to transmit through but blocks out light (use caution since beryllium is toxic).

Figure 1-28 Spectral transmittance of window materials

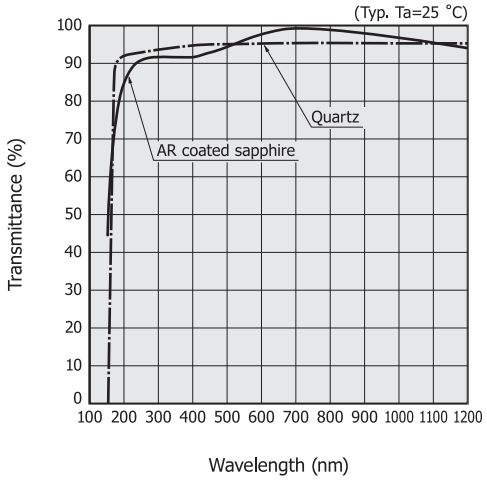

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Photo response non-uniformity

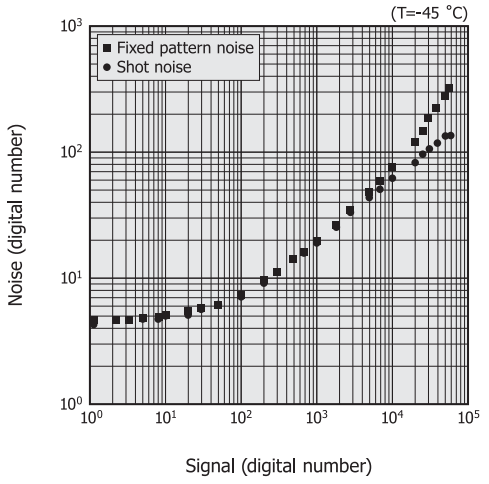
Photo response non-uniformity specifies the variations in sensitivity between pixels of a CCD, and is caused by variations in the light input window and the wafer process. Noise accompanying the photo response non-uniformity is proportional to the signal level.

A photon transfer curve [Figure 1-29], which plots the relationship between the noise and the input signal level varying with light exposure, is acquired by illuminating the effective active area with uniform light and setting a measurement area of about 50 × 50 pixels. Photo response non-uniformity (PRNU) is then defined by equation (6).

$$PRNU = \frac{Noise}{Signal} \times 100\ [\%] \cdots\cdots (6)$$

Here, noise is a statistical value indicating the standard deviation of pixel signals. The signal is the average signal of each pixel in the effective active area. When the signal level is low, the PRNU is affected by fixed pattern noise (see “Noise” in section 1-2, “Characteristics”). However, when the signal level is sufficiently high, the PRNU becomes a constant value regardless of the signal level. The PRNU specified in our datasheets was measured at a signal level that is 50% of the full well capacity (saturation charge). A PRNU of typical FFT-CCDs is approx. 1% rms or ±3% (peak to peak).

Figure 1-29 Photon transfer curve (S9974-1007)



Full well capacity

The full well capacity for a CCD indicates the number of signal electrons that can be transferred by a potential well. This full well capacity is expressed in units of e^-.
The full well capacity for CCDs is determined by the following four factors:

- Vertical shift register full well capacity (vertical full well capacity)
- Horizontal shift register full well capacity (horizontal full well capacity)
- Summing full well capacity
- Output section full well capacity

In two-dimensional operation mode, the signal charge of each pixel is output individually, so the full well capacity is determined by the vertical shift register. On the other hand, the horizontal full well capacity is designed to saturate at a higher level than the vertical full well capacity so as to enable line binning. The summing full well capacity formed by the summing gate, which is the last clock gate, is designed to be greater than the horizontal full well capacity in order to add signals from the horizontal shift register (pixel binning).
The saturation voltage (Vsat) of an output signal is given by equation (7).

$$Vsat = FW \times Sv \quad \cdots\cdots\cdots (7)$$

FW : full well capacity
Sv : conversion coefficient

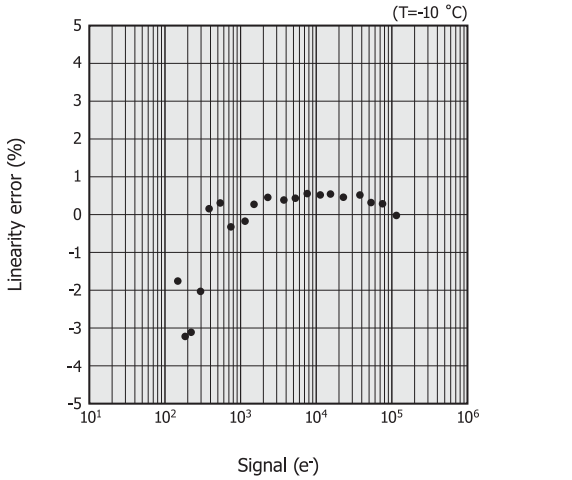
Linearity

The linearity of CCD output characteristics deviates slightly from the ideal line γ=1. The cause of this deviation is related to the output stage and results from capacitive variations in the reverse-biased PN junction constituting the FDA and from fluctuations of the MOSFET transconductance.
The extent of linearity deviation is expressed in terms of "linearity residual" (LR) as defined by equation (8).

$$LR = \left(1 - \frac{Sm/Tm}{S/T}\right) \times 100\ [\%] \quad \cdots\cdots\cdots (8)$$

Sm: signal level at one-half the full well capacity
Tm: exposure time at one-half the full well capacity
S : signal
T : exposure time

Figure 1-30 Linearity (S9970-1007 in two-dimensional operation mode)



Charge transfer efficiency

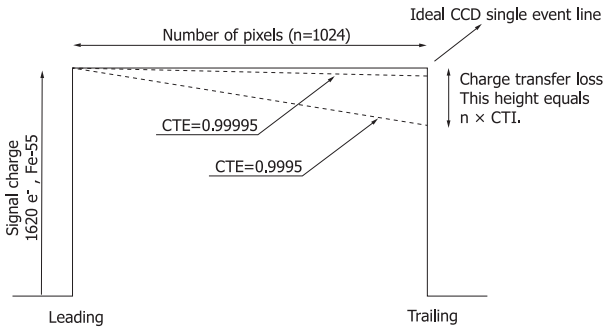
Ideally, there is no loss in the charge transfer process of CCDs. In actual operation, however, 100% charge transfer is not attained due to traps resulting from the semiconductor materials and wafer process. A very small amount of charge is not transferred and is left behind.
Charge transfer efficiency (CTE) is defined as the ratio of charge that is transferred from one pixel to the adjacent pixel. (In a 2-phase CCD, 2 charge transfers are required in gate units in order to transfer the signal charge per pixel, but those two transfers are specified as one transfer.)
An X-ray stimulation method is effective in measuring the transfer efficiency of a small charge because X-ray incident on the CCD causes an ideal spot charge to input in a pixel without using electrical means.
In this measurement, the signal of each line in the horizontal direction is stacked (horizontal stacking). By means of this horizontal stacking, the CCD output depicts a single event line according to the X-ray energy as shown in Figure 1-31. In an ideal CCD with a CTE equal to 1, the signal height of the leading and trailing edges should be the same. In actual use, however, the CTE is less than 1, so a loss of the signal charge transfer occurs at the trailing edge. If we let the signal charge at the leading edge be 1, then the charge transfer loss is expressed by equation (9).

Charge transfer loss = n × CTI ····· (9)

n: number of pixels
CTI (charge transfer inefficiency): 1 - CTE

HAMAMATSU standard CCDs have a typical CTE of 0.99999.

Figure 1-31 CTE evaluation method by Fe-55 stacking



KMPDC0046EA

Table 1-1 Charge transfer ef ciency and lag in line binning

CTE	S9971-0906	S9971-0907
0.99995	0.0032	0.0064
0.99999	0.00064	0.00128
0.999995	0.00032	0.00064

Dark current

Dark current is an output current that flows when no light is input. This is generally expressed in units of A (ampere), A/cm^2, and V (volt). In CCDs for measurement applications, e$^-$/pixel/s or e$^-$/pixel/h units are generally used, which indicate the number of electrons generated in one pixel per unit time. Dark current nearly doubles for every 5 to 7 °C increase in temperature.

Three major causes that generate CCD dark current are as follows:

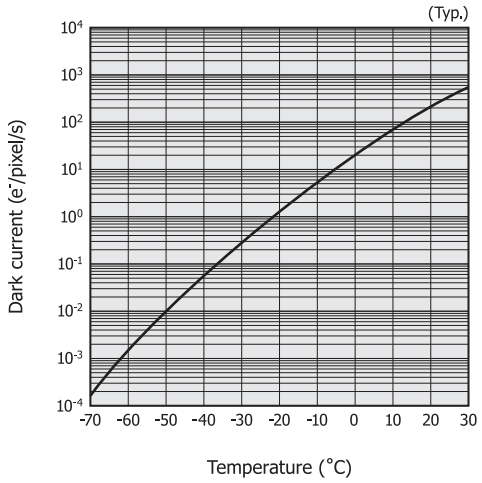
① Thermal excitation and diffusion in undepleted region
② Thermal excitation in depletion layer
③ Thermal excitation by surface level

Among these three causes, item ③ is most dominant.

MPP (multi-pinned phase) operation reduces the dark current and is also referred to as inverted operation. MPP operation is performed by setting the portions under all MOS structure gates, which constitute the CCD electrodes, to the inverted state.

The dark current can be significantly lowered by MPP operation since it suppresses the effect of ③.

Figure 1-32 Dark current vs. temperature (S9970/S9971 series)



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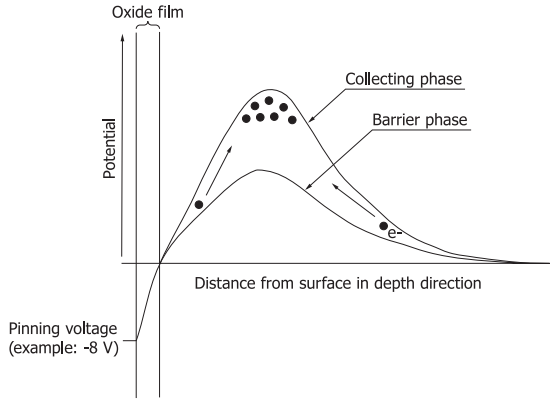
In a 2-phase CCD, a potential difference is applied between the barrier phase and the signal charge collecting phase by way of ion implantation, etc. The 2-phase CCD therefore provides the potential wells for accumulating charges even when all gates are set to the same voltage. MPP operation can be performed by applying a bias to invert all phases of the CCD.

When the dark current must be reduced, using the MPP operation and cooling the CCD are very effective.

Figure 1-33 Potential distribution in MPP operation

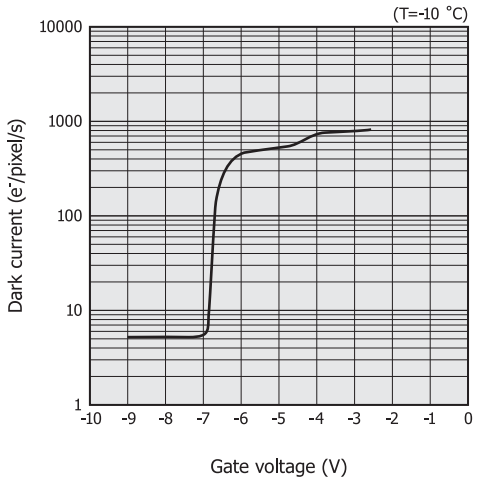


KMPDB0055EB

As shown in Figure 1-33, both the collecting phase and barrier phase are pinned in the inverted state. In the pinned state, the CCD surface is inverted by holes supplied from the channel stop region. The potential at the oxide film interface is fixed at the same potential as the substrate, even if a further negative voltage is applied.

In the state where the oxide film interface is inverted by holes, the generation of thermally excited electrons is drastically suppressed. This therefore allows attaining a state with low dark current.

Figure 1-34 Dark current vs. gate voltage (S9974-1007)



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In MPP operation, the dark current can be greatly reduced by applying the optimum pinning voltage. However, if the voltage does not reach the optimum pinning voltage, the inverted layer is not fully formed by holes, so the dark current cannot be minimized. In contrast, if the voltage is increased as a negative value in excess of the optimum pinning voltage, not only is extra clock amplitude required, but the dark current may also increase due to excessive charges called spurious charges. Dark current can be minimized by adjusting the voltage to an optimum value near the gate voltage listed in the datasheet.

Noise

CCD noise is classified into the following four factors:

(1) Fixed pattern noise (Nf)

This noise is caused by variations in sensitivity between CCD pixels (variations in sensitivity between pixels is caused by non-uniformities in the aperture area and film thickness). When the signal is large, the fixed pattern noise is proportional to the amount of exposure (number of signal electrons). The fixed pattern noise Nf can be regarded as zero based on the noise from one pixel.

(2) Shot noise (Ns)

Shot noise is the noise generated by statistical changes in the number of photons incident on a CCD. Shot noise is expressed by equation (10) according to the Poisson distribution.

$$Ns = \sqrt{S} \quad \cdots\cdots\cdots \quad (10)$$

S: number of signal electrons [e^-]

For example, if a CCD receives photons that generate a signal electron quantity of 10000 e^- inside the CCD, then the shot noise will be 100 e^- rms.

(3) Dark shot noise (Nd)

Dark shot noise is caused by dark current and is proportional to the square root of the number of electrons generated in a dark state. To reduce the dark shot noise, the dark current itself must be reduced. The variation in dark current between each pixel is larger than variations in the sensitivity.

(4) Readout noise (Nr)

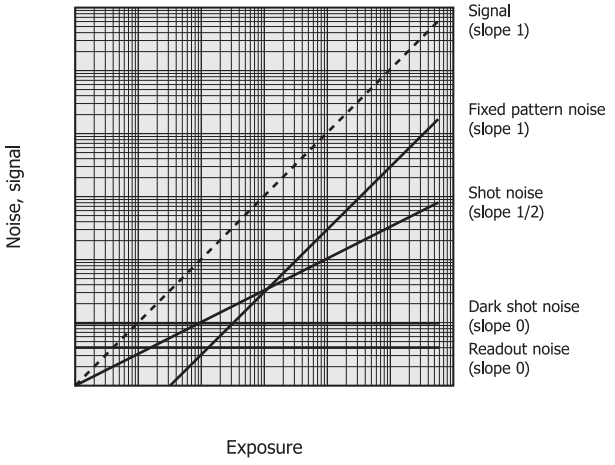
This is electrical noise from thermal noise caused by the MOSFET used as the amplifier in the CCD output section. It also comes from the readout circuit and eventually determines the lower detection limit of the CCD. Readout noise is determined by the CCD output method and is not affected by the amount of exposure. Readout noise is also frequency-dependent [Figure 1-39].

Total noise (Nt) is expressed by equation (11).

$$Nt = \sqrt{Nf^2 + Ns^2 + Nd^2 + Nr^2} \quad \cdots\cdots\cdots \quad (11)$$

Figure 1-35 shows the interrelation between these four factors and the amount of exposure. The CCD detection limit is determined by the dark shot noise and readout noise. This means that the CCD detection limit can be lowered to the readout noise level by reducing the dark current and lowering the shot noise below the readout noise.
The S/N is mainly determined by the fixed pattern noise when the amount of exposure is high, and it is determined by the shot noise when the amount of exposure is low.

Figure 1-35 Noise vs. e posure



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Dynamic range

Dynamic range generally specifies the measurable range of a detector and is defined as the ratio of the maximum level to the minimum level (detection limits).
The CCD dynamic range is a value obtained by dividing the full well capacity by the readout noise.

$$\text{Dynamic range} = \frac{\text{Full well capacity}}{\text{Readout noise}} \quad \cdots\cdots\cdots \quad (12)$$

Dynamic range is also given by equation (13).

$$\text{Dynamic range} = 20 \times \log\left(\frac{\text{Full well capacity}}{\text{Readout noise}}\right) \text{[dB]} \cdots (13)$$

The dynamic range varies with operating conditions such as temperature and integration time. At around room temperature, the dark shot noise determines the lower detection limit. Under operating conditions where the dark shot noise can be ignored (by cooling the CCD sufficiently), the readout noise determines the dynamic range.

In two-dimensional operation, the full well capacity will equal the charge that can be transferred by the vertical shift register. In one-dimensional operation by line binning, the full well capacity will equal the charge that can be transferred by the horizontal shift register.

Table 1-2 CCD specification examples

Parameter	S9736 series	S7170-0909
Type	Front-illuminated type	Back-thinned type
Number of pixels	512 × 512	512 × 512
Pixel size [µm]	24	24
Full well capacity (vertical) [ke⁻]	300	300
Conversion factor [µV/e⁻]	3.5	2.2
Readout noise [e⁻ rms]	4	8
Dynamic range	75000	37500
Dark current (0 °C) [e⁻/pixel/s]	10	10

Resolution

The ability of an image sensor to reproduce the contrast at a spatial frequency in an image is called the spatial resolution and is quantified by the MTF (modulation transfer function) for sine waves. Since the pixels of a CCD are individually separated, there is a limiting resolution determined by the Nyquist limit due to the discrete sampling theorem. For example, when a black-and-white stripe pattern is viewed with a CCD, the difference between the black and white signal levels decreases as the stripe pattern becomes finer, and finally reaches a point at which the stripe pattern cannot be resolved. The ideal MTF of CCDs is expressed by equation (14).

$$\text{MTF} = \text{sinc}\{(\pi \times f) / (2 \times fn)\} \cdots\cdots (14)$$

f : spatial frequency of image
fn: spatial Nyquist frequency

Because optical sine waves are difficult to generate, a test chart having square wave patterns is commonly used. The spatial frequency response measured using this test pattern is called the contrast transfer function (CTF) which is different from the MTF. (The CTF can be converted into the MTF by Fourier transform.)

The actual CCD resolution is determined by the extent of diffusion occurring when the signal charge is collected inside the silicon. Since the incident photons are absorbed within the depletion layer, the generated electrons do not diffuse and is collected by the corresponding pixels, so the resolution does not deteriorate. The resolution also varies depending on the depth in the silicon where the incident photons are absorbed. The longer the incident photon wavelength, the deeper the position where the photons are absorbed, causing the resolution to deteriorate.

Figure 1-36 MTF vs. spatial frequency at different wavelengths of input photons (S9970/S9917 series calculated values)

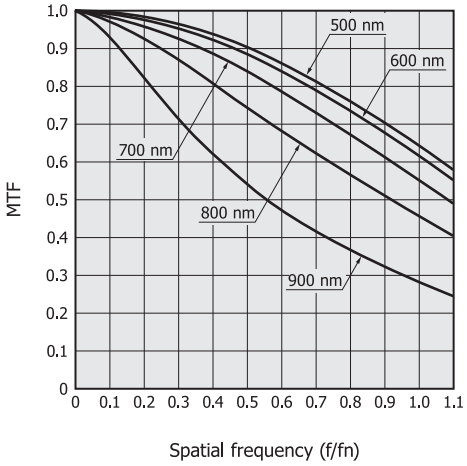

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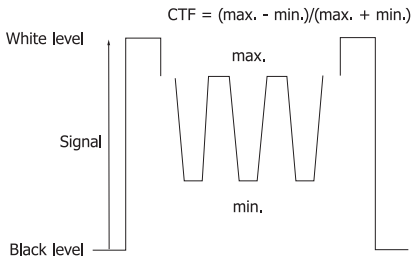
Figure 1-37 CTF calculation method



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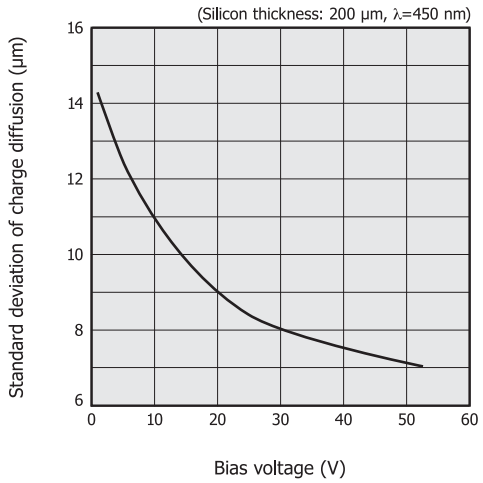
Point spread function

The standard deviation (σ_D) of charge diffusion is defined as shown in equation (15). Here, σ_D is proportional to the square root of the depletion layer thickness and also of the absolute temperature in the silicon, and is inversely proportional to the square root of the bias voltage applied to the backside.

$$\sigma_D = \sqrt{\frac{2 \times Xdep^2 \times k\,T}{Vbb \times q}} \cdots\cdots (15)$$

Xdep: depletion layer thickness
k : Boltzmann's constant
T : absolute temperature
Vbb : bias voltage applied to backside
q : electron charge

Figure 1-38 Standard deviation of charge diffusion vs. bias voltage



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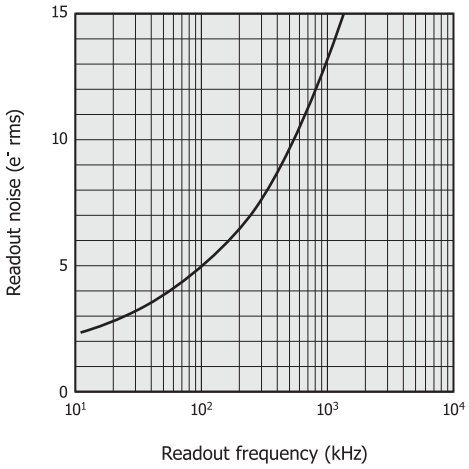
Frequency characteristics of noise

When dark current and spurious charges are sufficiently small, the readout noise determines the eventual number of noise electrons generated in a CCD. The readout noise is determined by the thermal noise of the MOSFET comprising the FDA in the readout section. MOSFET thermal noise includes white noise and 1/f noise, both of which should be reduced to achieve low noise. White noise can be reduced by increasing the MOSFET mutual conductance (gm). In MOSFET built into CCDs for measurement applications, the corner frequency of 1/f noise is reduced to as low as a few kilohertz.

MOSFET thermal noise depends greatly on the bias conditions. To achieve the readout noise specified in our CCD image sensor datasheet, the bias must be applied according to the recommended operating conditions. Even when the recommended bias conditions have been set, the signal processing circuit still has a great effect on CCD readout noise. Since a CDS circuit is commonly used for CCD signal processing, optimizing the transfer functions for the CDS circuit and the LPF (low-pass filter) installed in the preceding stage of the CDS circuit will result in reduced CCD readout noise. Therefore, if the effect of the 1/f noise corner frequency can be reduced versus CCD readout frequency, then the output noise of the CCD system including the signal processing circuit will be determined by the white noise and noise bandwidth.

To summarize the above, CCD readout noise depends on the readout frequency. The readout frequency must be low (less than 100 kHz) to achieve a readout noise of a few electrons (e^- rms) which is a noise level required in measurement applications. If the signal readout frequency becomes higher, the readout noise increases sharply.

Figure 1-39 Readout noise vs. readout frequency (S9737-01)



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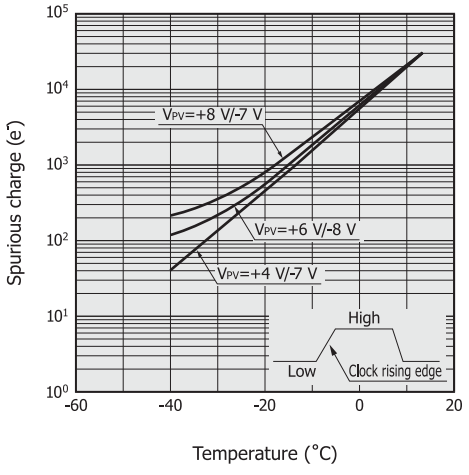
Spurious charge

Spurious charges are generated by clock pulses during operation such as in MPP mode and do not result from signals produced by the incident light. In MPP operation, the vertical clock is set to low, and during this low period, the region under the gate of each pixel is in an inverted state. In this state, holes move from the channel stop region to a point under the gate, and the surface potential in that region is pinned at the substrate potential. At this point, some holes are trapped along the oxide film interface, and their phase becomes a non-inverted state when the clock pulse goes to high level. The trapped holes have high energy after being released and generate a spurious charge which is then collected in a potential well. The CCD output is the sum of the signal, dark current, and this spurious charge.

Spurious charges can be reduced by delaying the rising edge of clock pulses or decreasing the voltage difference between high and low clock levels. When a CCD is cooled to a sufficiently low temperature where the signal level approaches readout noise level, it is important to set the clocking conditions by taking the spurious charge into account.

Figure 1-40 Spurious charge vs. temperature (typical e ample)



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Anti-blooming

Blooming (overflow) is a phenomenon that occurs when high-intensity light enters the active area and the resulting signal charge exceeds a specific level. This excess charge then overflows into adjacent pixels and transfer region. A technique to prevent this is called anti-blooming which provides a drain to carry away the excess charge.

Anti-blooming structures for CCDs are roughly divided into a lateral type and a vertical type. The lateral type structure has an overflow drain formed along the pixels or charge transfer channels. This structure has the drawback that the fill factor is reduced when used for front-illuminated CCDs. However, this problem can be avoided when used for back-thinned CCDs. Our CCDs use the lateral type. The vertical type structure is designed so as to carry away the excess charge into the inside of the substrate. The fill factor is not reduced, but there is a problem in that the sensitivity drops at longer wavelengths.

When controlling the anti-blooming function by means of the overflow voltage (V_{OFD}) and overflow gate voltage (V_{OFG}), these applied voltages may decrease the full well capacity.

Figure 1-41 Schematic diagram of anti-blooming

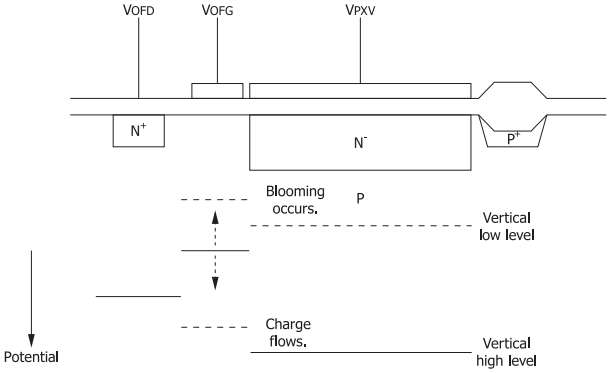

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Figure 1-42 Anti-blooming structure and potential (lateral type)

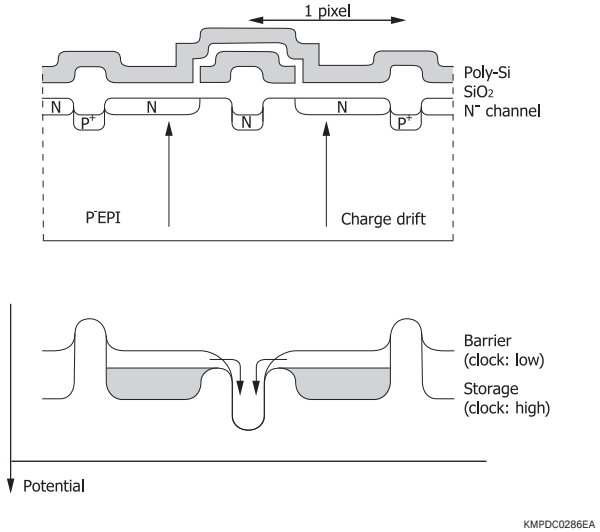

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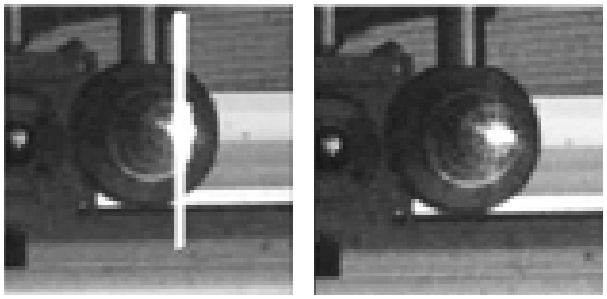
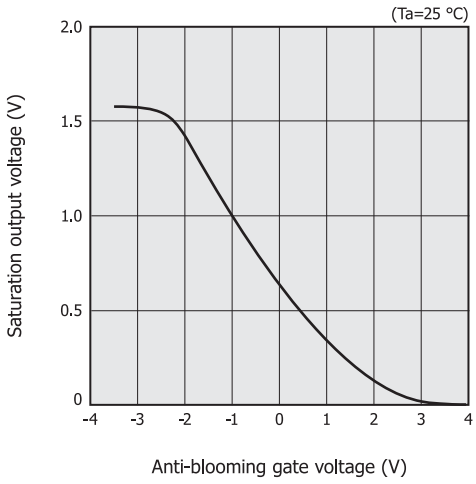
Figure 1-43 E ample of acquired images
(a) ithout anti-blooming (b) ith anti-blooming



Anti-blooming function for one-dimensional CCD

In one-dimensional CCDs, an anti-blooming drain and anti-blooming gate are formed in the vicinity of the storage gate. The anti-blooming function works by setting the anti-blooming voltage to an appropriate value. The anti-blooming voltage also controls the saturation output voltage. Moreover, when the anti-blooming voltage is set high, all signal charges generated in the photodiodes can be removed to make the output zero. This function is used to activate the electronic shutter described next.

Figure 1-44 Saturation output voltage vs. anti-blooming gate voltage



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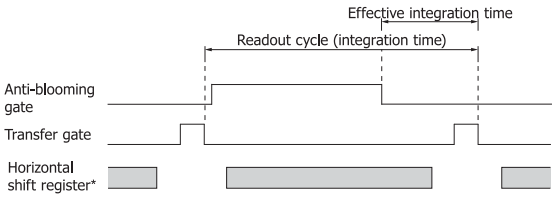
Electronic shutter

In general, the integration time for one-dimensional CCDs is equivalent to the interval between clock pulses to the transfer gate. Using an electronic shutter function allows setting an effective integration time that is shorter than the transfer gate clock pulse interval. When the anti-blooming gate voltage is set high, all signal charges generated in the photodiodes are carried away into the anti-blooming drain. It is therefore possible to set an effective integration time shorter than the normal integration time by providing a period during which the anti-blooming gate voltage is high and a period during which the anti-blooming gate voltage is low.

Figure 1-45 Timing chart for one-dimensional CCD (electronic shutter function)



* Indicates readout period.

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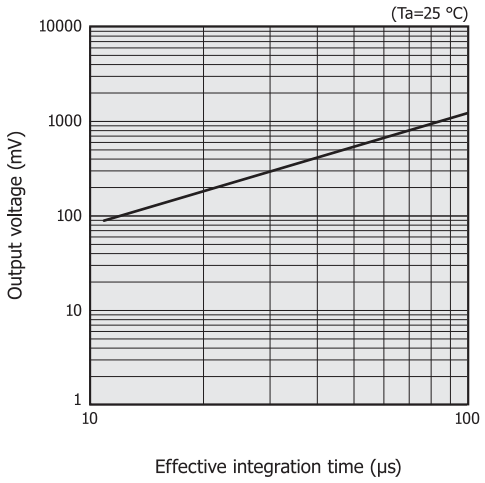
Figure 1-46 Output voltage vs. effective integration time (one-dimensional CCD)



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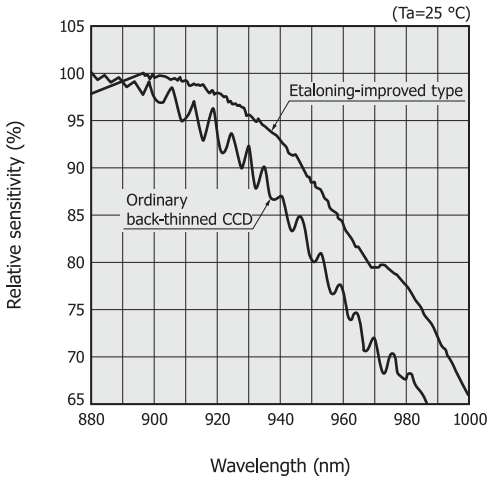
Etaloning

Etaloning is an interference phenomenon that occurs while the light incident on a CCD repeatedly undergoes reflection and attenuation between the front and back surfaces of the CCD, and causes alternately high and low sensitivity. An etalon commonly refers to an optical element consisting of two parallel planes facing each other and whose inner surfaces are coated with a highly reflective film. The light entering a CCD repeatedly undergoes imperfect reflection, transmission, and absorption within the CCD as if the light has entered an etalon. This phenomenon is therefore called “etaloning.” When long-wavelength light enters a back-thinned CCD, etaloning occurs due to the relationship between the silicon substrate thickness and the absorption length [Figure 1-47]. Using our advanced device technology, we have succeeded in producing back-thinned CCDs that offer reduced etaloning. Note that etaloning is a phenomenon unique to back-thinned CCDs and does not occur in front-illuminated CCDs.

Figure 1-47 Etaloning characteristics (typical e ample)



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Cosmetics

The term “cosmetics” refers to the extent of CCD defects (blemishes and scratches). Blemishes and scratches are divided into two categories: “white spots” that appear bright in a dark state and “black spots” that appear dark when light is incident on a CCD. These white and black spots are also called pixel defects.

White spots are usually caused by lattice defects or metal impurities in the substrate material or by pattern failures from mechanical damage or dust during the wafer process. Black spots are mainly caused by irregular reflections due to dust on the CCD surface during the wafer process or partial defects of the surface insulation film, or by contamination such as dust on the device surface or window. It is difficult to completely eliminate these white and black spots. The larger the active area and the smaller the pixel, the more obvious the effects from these white and black spots become.

HAMAMATSU defines white and black spot specifications and inspects every CCD to check the number of these spots.

Cosmetic specifications are defined as described below. These definitions may vary depending on the manufacturer, so use caution when comparing specifications.

(1) Point defect

- White spot

White spots are pixels that generate dark current in excess of 3% of the full well capacity after charge integration for 1 second at a cooling temperature of 0 °C.

- Black spot

Black spots are pixels that provide an output of less than 50% of the average output value calculated when the CCD is illuminated with uniform light so as to generate a charge equal to 50 to 90% of the full well capacity. We usually perform this test using uniform light that generates a charge equal to 50% of

the full well capacity.

(2) Cluster defect

A cluster consisting of two to nine continuous pixel defects is called a cluster defect and is distinguished from point defects. Cluster defects appear vertically in most cases, but appear as a two-dimensional cluster if originating from black spots of back-thinned CCDs or front-illuminated CCDs coupled to an FOS (fiber optic plate with scintillator).

(3) Column defect

A cluster consisting of ten or more continuous pixel defects (larger than a cluster defect) is called a column defect and is viewed as different from cluster defects. As with cluster defects, column defects also appear vertically in most cases, but may appear as a two-dimensional cluster if originating from black spots of back-thinned CCDs or front-illuminated CCDs coupled to an FOS.

Front-illuminated CCDs with a small active area, such as HAMAMATSU S9970/S9971 series, have no point defects, cluster defects, or column defects. When CCDs are coupled to an FOP (fiber optic plate) or FOS, defects might occur due to other factors not originating in the CCDs, so the shape and number of defects will differ from those occurring only in CCDs.

1-3 How to use

Timing

Operating a CCD requires seven types of signals: 2-phase clock pulses (P1V, P2V) for the vertical shift register, a transfer gate pulse (TG), another 2-phase clock pulses (P1H, P2H) for the horizontal shift register, a summing gate pulse (SG), and a reset pulse (RG). The TG electrode utilizes a part of the last P2V electrode but is recommended to be used as a separate terminal where the clock pulse should be input at the same timing as P2V. However, operation is also possible by shorting the TG and P2V terminals. To find timing charts of pulses needed to operate a CCD, refer to our datasheet.
FFT-CCDs can be operated in any of four modes: line binning, two-dimensional operation, pixel binning, or TDI operation. The desired operation mode can be chosen by simply adjusting the timing of each clock pulse.

(1) Line binning

The number of bits that should be "binned" is first transferred in the vertical direction. This permits signal charges to be added to the corresponding horizontal shift register. Then all horizontal signal charges are transferred. The summing gate pulse should be exactly the same as the clock pulse (P2H) for the horizontal shift register.

(2) Two-dimensional operation (area scan)

This operation transfers all horizontal signal charges each time one bit is transferred in the vertical direction. When the transfer in the vertical direction is fully complete, a frame transfer has been completed. At this point, the summing gate pulse should be set exactly as the clock pulse (P2H) for the horizontal shift register.

(3) Pixel binning

One bit is first transferred in the vertical direction. Then all the horizontal signal charges are transferred. At this point, by halting the summing gate pulse for a period equal to the number of bits required for summing, the signal charges are added to the summing well.

Note: Line binning and pixel binning can be performed at the same time.

(4) TDI operation

As explained in "TDI-CCD" in section 1-1, "Structure and operating principle," TDI operation allows imaging of a moving object. To do this, the CCD vertical transfer clock pulse must be synchronized with the speed at which the object moves along the active area surface of the CCD.

Clock pulse and DC bias adjustment

The clock pulse and DC bias must be adjusted properly to make fullest use of CCD performance.

(1) Transfer clock pulse

The low level of the clock voltage for the vertical shift register affects the CCD dark current. If it is set to a voltage higher than the pinning voltage that initiates MPP operation, the dark current will not lower as expected. The pinning voltage differs according to the individual CCD due to variations in device production. Ideally, it should be adjusted for each product.
After determining the low level of the vertical clock voltage, adjust the high level. The clock pulse amplitude should be large enough to maintain the desired full well capacity. However, if the clock pulse amplitude is set too large, the spurious charges become large, causing the dark current (Nb) during the readout time to increase and resulting in an offset that appears in the entire output signal. Normally, the spurious charges cannot be distinguished from the dark current at around room temperature, but they may cause problems when the CCD is cooled. Therefore, the vertical clock pulse amplitude should be adjusted to a minimum as long as other characteristics are not impaired.

(2) Reset clock pulse

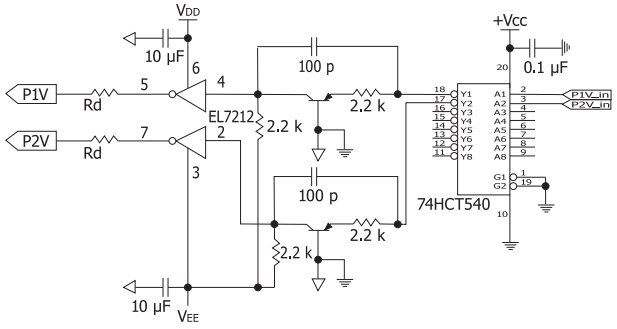
The reset clock pulse is applied to the reset gate (RG) to periodically reset the signal charge flowing into the FD (floating diffusion) to the reference voltage (V_{RD}). Adjusting the low and high levels of this clock pulse changes the saturation charge

level of the output section. When these are properly adjusted, the saturation charge level of the output section is sufficiently larger than the CCD full well capacity. If the low level voltage of the reset clock pulses becomes high, the charge that can be stored in the FD decreases because the potential has not lowered sufficiently while in a state where the reset switch is off. This may cause an overflow before all transfer charges are converted into voltage. For this reason, the low level of the reset clock pulses must be set to a voltage low enough not to affect the saturation charge level of the output section.
Set the pulse width of the reset clock pulses to about 10 ns to 100 ns (there will be no problem if longer than 100 ns).

(3) Transfer clock pulse generator

Figure 1-48 shows an example of a transfer clock pulse generator. As stated above, clock pulses with high and low levels of voltage amplitude are required to operate a CCD. These clock pulses must drive the vertical shift register and horizontal shift register at high speeds, which have an input capacitance of several hundred picofarads to several nanofarads. For this purpose, MOS driver IC is commonly used to drive a CCD since it is capable of driving a capacitive load at high speeds.
Normally, the timing signal generator circuit uses a TTL or CMOS logic level IC. The operating voltage for these ICs is +3.3 V or +5.0 V, so a level converter circuit must be connected to the MOS driver IC.
In 2-phase CCD operation, the clock pulses for driving the vertical and horizontal shift registers must overlap with each other (see “Charge transfer operation” in section 1-1, “Structure and operating principle”). For this reason, a resistor Rd with an appropriate value (dumping resistor: a few to several dozen ohms) should be placed between the MOS driver IC and the CCD in order to adjust the rise time and fall time of the clock pulses.
To minimize noise intrusion to the CCD from digital circuits, it is recommended that the analog ground and digital ground be set to the same potential by the transfer clock pulse generator.

Figure 1-48 E ample of transfer clock pulse generator



VDD: high level voltage of clock pulse
VEE: low level voltage of clock pulse
Rd : damping resistor (a few to several dozen ohms)

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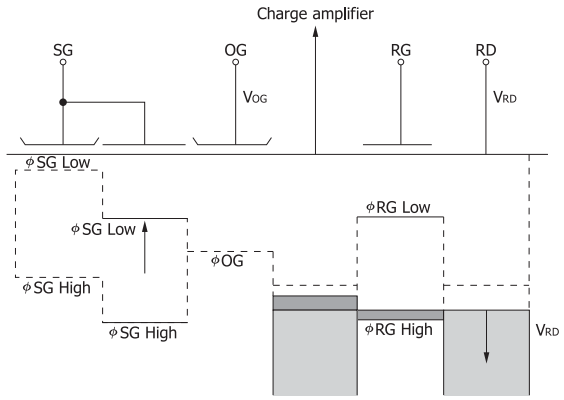
Figure 1-49 Potentials in CCD output section



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(4) DC bias

- Bias (V_{OD}) applied to OD

V_{OD} is the bias voltage applied to the output transistor. When using a one-stage source follower output amplifier, apply approx. 20 V as V_{OD}. In a source follower circuit using a load resistance of about 20 kΩ connected to the MOSFET source, the source DC level is about 15 V. Therefore, although several volts are applied across the source and drain of the MOSFET via the voltage applied to the OD, the following phenomena will occur unless this voltage is sufficiently high.

① Voltage gain (Av) in the source follower circuit is lowered.
② MOSFET does not operate in the saturation region.

These phenomena adversely affect CCD performance. For example, they may cause a decrease in the conversion factor (unit: µV/e$^-$), an increase in the readout noise, or deterioration in the linearity.
When using a multi-stage amplifier such as a two-stage source follower output type, set V_{OD} to approx. +15 V, which is lower than V_{OD} for a one-stage type. As in the case of one-stage type, phenomena ① and ② occur in the two-stage source follower output type.

- Bias (V_{RD}) applied to RD

V_{RD} is the bias voltage applied to the reset drain. It determines the reset level of the output section and also serves as the gate voltage of the output transistor. The V_{RD} determines the voltage gain and MOSFET operating region the same as with V_{OD} and also affects the saturation charge level of the output section. Increasing the V_{RD} also raises the potential in the FD and the amount of signal increases. However, it must be set to an optimum value in consideration of phenomena ① and ② which may occur in the output transistor.

- Bias (V_{OG}) applied to OG

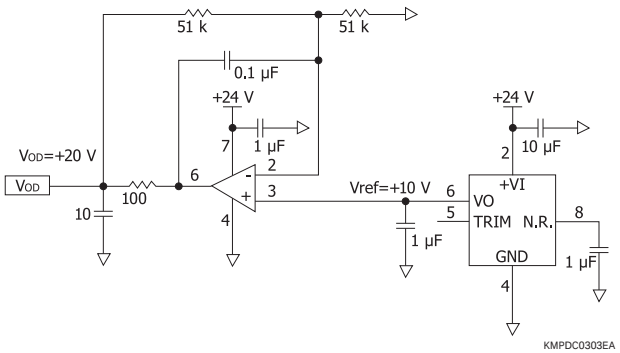
V_{OG} is the bias voltage applied to OG that separates the FD arranged at the last stage of the horizontal shift register from the last clocking gate (summing gate). The signal charge is output to the FD in synchronization with the falling edge to

the low level of the summing gate pulse (SG) which is the last clocking gate. The OG potential therefore becomes smaller than the SG potential at low level, and the difference between the OG potential and the potential at reset becomes the factor that determines the amount of signal charge that can be handled. As seen from Figure 1-49, the amount of signal charge is limited by either the potential under OG or the potential of the reset gate at low level. Since V_{OG} is set lower, the saturation charge level of the output section becomes larger. If V_{OG} is too low, however, the signal charge is unable to flow into the FD during the low level of SG, so V_{OG} must be adjusted to an appropriate value.

- Bias generator circuit

The bias voltage is mainly applied to the peripheral section of the CCD output amplifier, so use a stable power supply with relatively low noise. It is also important to note the voltage accuracy, voltage fluctuation, ripple, and output current.
Figure 1-50 shows an example of a bias voltage generator circuit for the OD terminal. The reference voltage is generated from the reference power supply IC and is set to a specified voltage value by the amplifier making up the low-pass filter. This allows obtaining a highly stable and accurate voltage with low noise.

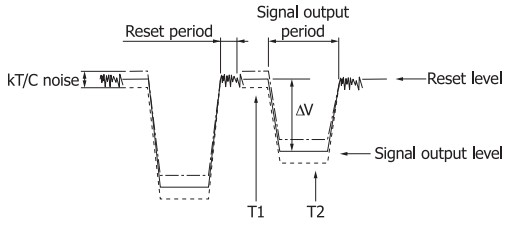
Figure 1-50 E ample of bias voltage generator circuit



Signal processing circuit

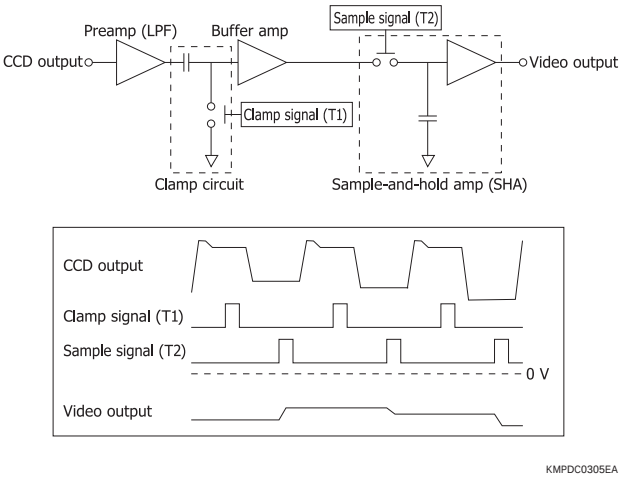
Major sources of noise from a CCD are the well-known kT/C noise and 1/f noise. The kT/C noise is generated by a discharge (reset operation) in the FDA (see “FDA” in section 1-1, “Structure and operating principle”). This noise is inversely proportional to the square root of the node capacitance (Cfd) of the FDA and makes up a large percentage of the total noise of a CCD. The 1/f noise is generated by the MOSFET constituting the FDA and is inversely proportional to the frequency.
These noises degrade the S/N in the CCD system and therefore should be reduced as much as possible in the signal processing circuit. A typical circuit for this purpose is a CDS circuit.
The operating principle of the CDS circuit is described below. Figure 1-51 shows an output waveform from a CCD. As stated above, kT/C noise occurs during a reset period in the FDA. At the point where the reset period has ended, the voltage level varies due to kT/C noise. Therefore, if data is acquired at time T2, the S/N deteriorates by an amount equal to the kT/C noise variation. In contrast, acquiring data at times T1 and T2 on the output waveform and then obtaining the difference between them will extract only a signal component ΔV with the kT/C noise removed. DC components such as the offset voltage component and reset feedthrough are removed at the same time.

Figure 1-51 CCD output waveform



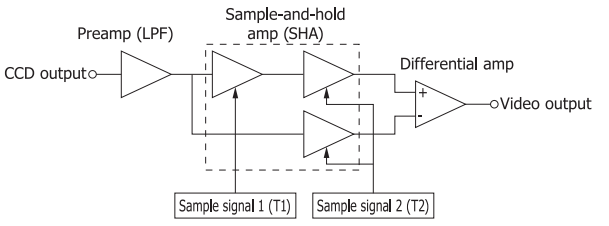
There are two types of CDS circuits: “Type 1” that uses a clamp circuit in combination with a sample-and-hold amplifier (SHA), and “Type 2” that uses a SHA in combination with a differential amplifier. Type 1 has a very simple circuit configuration [Figure 1-52]. But if the ON resistance of the switch used in the clamp circuit is large, the amount of noise that can be removed will be small or a DC voltage error will occur. Ideally, the ON resistance should be 0 Ω.

Figure 1-52 CDS circuit block diagram (using clamp circuit and SHA)



Type 2 uses a larger number of components but removes noise more effectively than Type 1. However, since Type 2 makes an analog calculation of the SHA output, the noise of the SHA itself may be added, resulting in increased noise in some cases. The SHA noise should be small enough so that the kT/C noise can be ignored.

Figure 1-53 CDS circuit block diagram (using SHA and differential ampli er)



A circuit example of Type 1 is shown in Figure 1-54.

The preamp gain should be set high in order to sufficiently amplify the CCD output signal. Since the CCD output signal contains DC voltage components, a capacitor is used for AC coupling. Note that this capacitor can cause a DC voltage error if the preamp bias current is large. Therefore, a preamp with a small bias current must be selected. A JFET or CMOS input amplifier is generally used. It is also necessary to select a low-noise amplifier with a bandwidth wide enough to amplify the CCD output waveform.

The clamp circuit is made up of capacitors and an analog switch. As the analog switch, we recommend using a high-speed type having low ON resistance and small charge injection amount.

As with the preamp, the last-stage amplifier is AC-coupled via a capacitor, so a JFET or CMOS input amplifier should be selected. In addition, a non-inverted amplifier must be configured to allow high input impedance.

Incidentally the CCD provides a negative-going output while the last-stage amplifier gives a positive-going output to facilitate analog-to-digital conversion. For this reason, an inverted amplifier is connected after the preamp.

Correction

Image sensors generally have two non-uniformities: 1) photo response non-uniformity (PRNU) that is variations in sensitivity to photons between pixels, and 2) dark current non-uniformity (DCNU) that occurs under the set operating conditions. At least these two non-uniformities must be corrected to collect highly accurate data. Since these non-uniformities vary with temperature, the correction must take the temperature into account.

(1) Dark current correction

Dark current differs from pixel to pixel and must therefore be considered in pixel units to make accurate corrections. When no light is incident on the CCD, the dark current (Nt) is expressed as in equation (16).

$$Nt(x, y, t, T) = Nd(x, y, T) \times t + Nb(x, y, T) \cdots\cdots (16)$$

x : horizontal direction address
y : vertical direction address
t : integration time
T : CCD temperature
Nd(x, y, T): dark current of each pixel [e⁻/pixel/s]
Nb(x, y, T): dark current when integration time is zero

When the integration time is zero, the dark current Nb(x, y, T) is also called the offset or bias. This value varies with the operating conditions. The dark current values listed in our datasheets are the dark current of Nd(x, y, T) averaged over a certain region and are different from the dark current actually output from the CCD. To correct the dark current, both Nd and Nb must be acquired. Nd and Nb can be acquired from one readout data, but more accurate correction image data that excludes the effect of disturbing noise can be obtained by acquiring a few or up to a dozen images and taking their average.

(2) Flat field correction

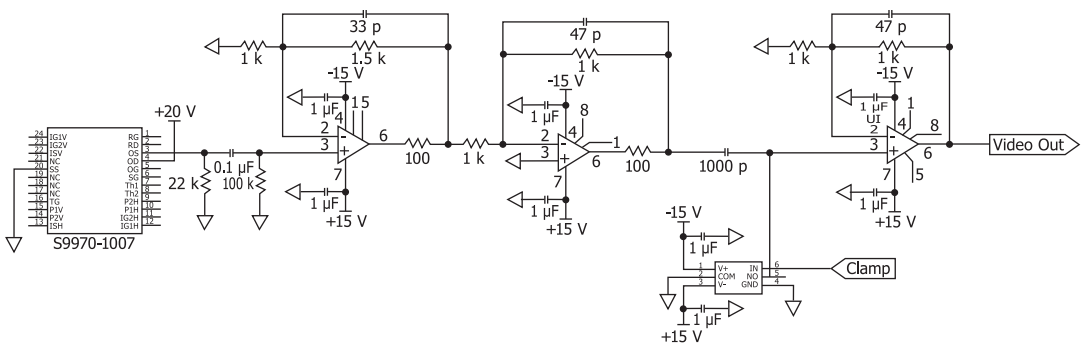
As described in “Photo response non-uniformity” in section 1-2 “Characteristics,” the sensitivity of each pixel in a CCD is not uniform, so it must be corrected in pixel units just as with the dark current. An uncorrected output I(x, y) measured under certain exposure conditions is given by equation (17).

$$I(x, y) = Nt(x, y, t, T) + i(x, y) \times r(x, y) \cdots\cdots (17)$$

i(x, y): original image output
r(x, y): sensitivity of each pixel

To acquire the original image output i(x, y), not only the dark current (Nt) but also r(x, y) must be known. Normally, the sensitivity r(x, y) can be acquired by illuminating a CCD with extremely uniform light and measuring the output. However, uniformly illuminating the entire surface of a CCD is difficult.

Figure 1-54 CDS circuit e ample (using clamp circuit and SHA)



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Moreover, the sensitivity may vary with wavelength depending on the position of the CCD active area. To accurately correct this within 1% or less, it is necessary to acquire correction data while paying attention to the optical systems and temperature, etc. The sensitivity r(x, y) can be acquired from one readout data, but more accurate calibration data can be obtained by acquiring a few or up to a dozen images and taking their average.

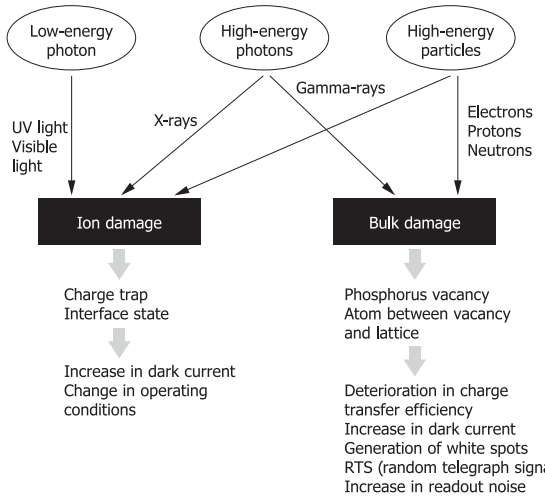
Coupling to FOS

Coupling an FOS (fiber optic plate with scintillator) to a front-illuminated CCD allows detecting X-rays up to several dozen keV or higher. See section 2 “CCD area image sensors” in Chapter 8 “X-ray detectors” for more information.

Damage by radiation

Ion damage and bulk damage can occur in a CCD due to radiation, the same as with other devices made of silicon. This must be considered before attempting to use a CCD for X-ray detection or in space environments.

Figure 1-55 Effects of radiation on CCDs



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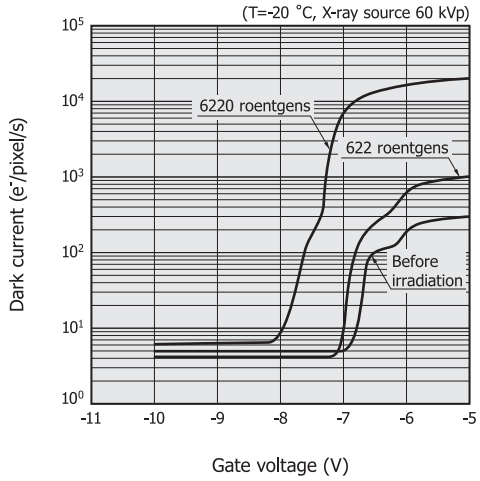
Ion damage occurs when photons with energy higher than a certain level (energy levels roughly higher than ultraviolet light) enter a CCD and the resulting electron-hole pairs are generated in the gate oxide film. Most electron-hole pairs generated by photons will recombine and disappear. However, some of the holes with less mobility than electrons are trapped in the oxide film and produce a voltage that can shift the CCD operating gate voltage. This causes the CCD pinning voltage to shift toward the negative side (amount of shift may be up to several volts in some cases). When high energy electrons or photons enter, both ion damage and bulk damage occur. On the other hand, heavy particles such as protons and neutrons also generate charges in the gate insulation film. Electrons and photons generate a new interface state at the oxide film interface. Since the energy level of that new interface state is within the band gap, the dark current will increase.

Bulk damage occurs when energized charged particles like protons interact with the silicon atoms. If protons have enough energy, they displace the silicon atoms from their lattice positions to interstitial locations (energy of approx. 100 eV is required to cause this). The displaced silicon atoms then collide with other silicon atoms to further displace more atoms. The resulting defects serve as electron traps. If many electron traps are created inside the charge transfer channels of the CCD, the charge transfer efficiency (CTE) will deteriorate. Those defects will become pixels with a large dark current.

Figure 1-56 Damage by X-rays (S9970-0907)



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Electrostatic and surge measures

CCDs may become damaged or deteriorate if subjected to static electrical charges and voltage surges. Take the following precautions to avoid trouble.

(1) Handling precautions

When taking a CCD out of the packing box, always do so in locations where anti-electrostatic measures are provided. For example, lay a grounded conductive sheet (1 MΩ to 100 MΩ) on the work bench or work floor.

When handling CCD sensors, always wear a wrist strap and also anti-static clothing, gloves, and shoes, etc. The wrist strap should have a protective resistor (about 1 MΩ) on the side closer to the body and be grounded properly. Using a wrist strap having no protective resistor is hazardous because you may receive an electrical shock if electric leakage occurs.

Always ground the soldering iron so no leakage voltage is applied to the device.

Do not bring charged objects (VDT for a PC or insulator materials such as plastics and vinyl) close to the CCD. The CCD may become electrically charged just by being brought close to a charged object, causing ESD (electrostatic discharge) damage.

(2) Usage precautions

Measurement devices and jig tools must be properly grounded so no surges are applied to the CCD by a leakage voltage. Do not allow a voltage exceeding the absolute maximum rating to be applied to the CCD from the measurement device or tester, etc. (This tends to occur during ON/OFF switching of power sources, so use caution.) If there is the possibility of a surge voltage, insert a filter (made up of a resistor or capacitor) to protect the CCD.

When installing the CCD, be extremely careful to avoid reverse insertions, wrong insertions, or shorts between terminals.

Do not attach or detach any connector, etc. that are connected to the power supply line or output line during operation.

(3) Carrying precautions

When carrying a CCD, place it on a conductive mat by inserting the lead pins into the mat (for shorting lead pins) and then put it in a conductive case. The PC board for mounting the CCD should also be put in a conductive case for carrying. Avoid using plastic or styrofoam boxes since they may generate static electricity due to vibration during shipping and cause device deterioration or breakdowns.

(4) Storage precautions

When storing a CCD, place it on a conductive mat by inserting the lead pins into the mat (for shorting the lead pins) and then put it into a conductive case. The PC board for mounting the CCD should also be put in a conductive case.

Avoid placing CCDs near equipment that may generate high voltage or high magnetic fields.

It is not always necessary to provide all the electrostatic and surge measures stated above. Implement these measures according to the extent of deterioration or damage that may occur.

1 - 4 New approaches

Among our CCDs, back-thinned CCD devices offer outstanding features such as high sensitivity in the ultraviolet to near infrared region. In addition to this technology, we are constantly at work developing new CCD devices with even higher speeds and higher sensitivity.

- Higher speed

  We are also at work developing multiport devices containing from a few up to several hundred fast-readout amplifiers capable of parallel readout. Multiport devices will allow fast readout in the order of gigapixels per second.
- Higher sensitivity

  We are also working hard to create electron multiplication (EM) technology that multiplies signal charges more than 100 times within CCD chips as well as “full depletion” technology to attain high sensitivity in the near infrared range (quantum efficiency of more than 70% in 1 µm band).
- Others

  A CCD with an electronic shutter function allowing a very short integration time of just a few microseconds is also under development. Our work also involves CCDs with fine pixel size (6 µm × 6 µm).

We are applying these advanced technologies to develop new CCD devices that meet demands in various fields including spectrophotometry, scientific measurement, medical diagnosis, DNA analysis, and industrial measurement.

2. NMOS linear image sensors

NMOS linear image sensors are self-scanning photodiode arrays designed as detectors for multichannel spectrophotometers. The scanning circuit of these image sensors is made up of N-channel MOS transistors and operates at low power consumption, making them easy to use. Each photodiode has a large active area and high UV sensitivity, yet the noise is extremely low so high S/N signals can be obtained even at low light levels. Current output type NMOS linear image sensors also deliver excellent output linearity and wide dynamic range.

2 - 1 Features

- Wide active area
- High UV sensitivity and stable characteristics under UV light irradiation
- Low dark current and large saturation charge

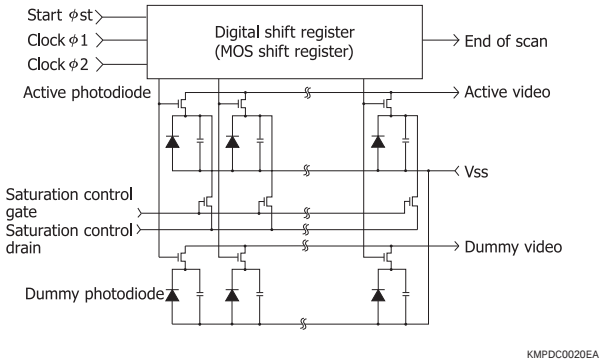
Allows a long integration time and wide dynamic range at room temperature.

- Excellent output linearity and sensitivity uniformity
- Low power consumption
- CMOS logic compatible start pulse and clock pulse
- Infrared-enhanced type: high sensitivity in infrared and soft X-ray regions
- Thermoelectrically cooled type: highly reliable package sealed with sapphire window

2 - 2 Structure

NMOS linear image sensors consist of a photodiode array that performs photoelectric conversion and stores the resulting charges, address switches connected to each photodiode, and a digital shift register. Each address switch is a MOS switch with the source connecting to a photodiode, the gate handling the address pulses from the shift register, and the drain connecting to the video line (common output line). Figure 2-1 shows an equivalent circuit of a current output type NMOS linear image sensor (S3901 to S3904 series).

Figure 2-1 Equivalent circuit (S3901 to S3904 series)



2 - 3 Operating principle

Photodiodes are initialized to a certain potential from an external circuit when their address switches turn on. When light enters a photodiode, a photocurrent proportional to the light level flows in the photodiode, and a charge (Qout = I_L × Ts) equal to the product of the photocurrent (I_L) and the integration time (Ts) is stored in the junction capacitance (Cj) of the photodiode. The integration time is the period between the times that the photodiode address switch turns on. It corresponds to the time interval between the start pulses applied to the shift register. This photodiode operation is called the charge integration mode and allows acquiring a large signal even from image sensors with small pixels by integrating the charge. In low-light-level detection, making the integration time longer yields a large output.

The shift register starts scanning when a start pulse is input with a clock pulse train applied to the shift register. The address switch connected to the first pixel photodiode first turns on in synchronization with the clock pulse and the charge stored

Table 2-1 HAMAMATSU NMOS linear image sensors

Type	Type no.	Number of pixels	Pixel size [μm (H) × mm (V)]
Standard type	S3901 series	128, 256, 512, 1024	50 × 2.5
	S3904 series	256, 512, 1024, 2048	25 × 2.5
	S3902 series	128, 256, 512	50 × 0.5
	S3903 series	256, 512, 1024	25 × 0.5
Standard type (thermoelectrically cooled type)	S5930 series	256, 512	50 × 0.5
	S5931 series	512, 1024	25 × 0.5
Infrared-enhanced type	S8380 series	128, 256, 512	50 × 0.5
	S8381 series	256, 512, 1024	25 × 0.5
Infrared-enhanced type (thermoelectrically cooled type)	S8382 series	256, 512	50 × 0.5
	S8383 series	512, 1024	25 × 0.5

in the first pixel photodiode is output to the external circuit via the video line. The first pixel address pulse then turns off, and the second pixel address pulse turns on, allowing the charge stored in the second pixel photodiode to be read out to the external circuit in the same way. By sequentially repeating this operation until the last pixel is scanned, the position information of light irradiated onto the linearly arranged photodiode array is read out to the external circuit as time-series signals including a time differential.

The minimum integration time is the product of the readout time per pixel and the number of pixels. In NMOS linear image sensors, the address switch on/off operation determines the integration time of the photodiode, and its timing shifts for each photodiode. So even though the integration time is the same for all pixels, the integration start time and end time for each pixel will differ. The next start pulse cannot be input until the last pixel is scanned.

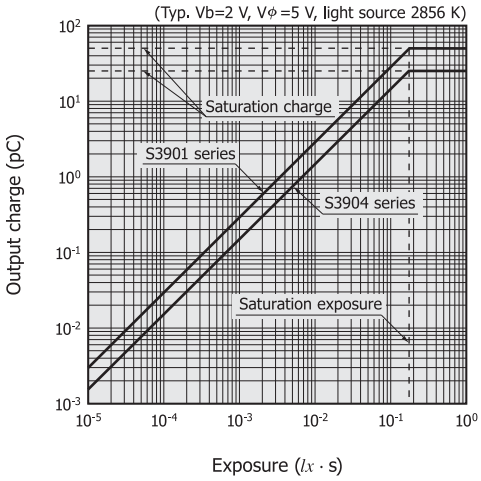
2 - 4 Characteristics

Input / output characteristics

Figure 2-2 shows input/output characteristics of current output type NMOS linear image sensors (S3901/S3904 series). The horizontal axis indicates the exposure amount which is the product of the incident light level and the integration time. Since no photodiode can store a charge larger than its junction capacitance, there is an upper limit on the output charge. This upper limit on the output charge is referred to as the saturation charge, and the exposure at this point is referred to as the saturation exposure.

In an over-saturated state, an excess charge flows into the overflow drain connected to the photodiode and will not affect other pixels. When a charge amplifier is used to read out the signal, the actual output deviation from the ideal line γ=1 is within 1% which indicates satisfactory input/output characteristics.

Figure 2-2 Output charge vs. e posure (S3901/S3904 series)



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Spectral response

Figure 2-3 shows spectral response characteristics of standard type and IR-enhanced type NMOS linear image sensors. Both types have sensitivity ranging from 200 nm to 1000 nm. Sensitivity varies linearly with temperature. At wavelengths shorter than the peak sensitivity wavelength, however, sensitivity is stable and is not significantly dependent on temperature. The longer the light wavelength, the larger the temperature dependence, and these types exhibit a temperature coefficient of approx. 0.7%/°C at 1000 nm.

HAMAMATSU NMOS linear image sensors provide stable operation even during ultraviolet light measurement because their structure is designed to prevent sensitivity from deteriorating due to ultraviolet light.

Figure 2-3 Spectral response (typical e ample)

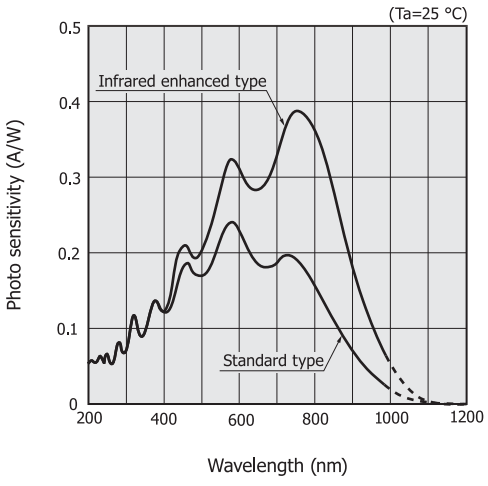

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Photo response non-uniformity

Image sensors contain a large number of photodiodes in arrays, and each photodiode is different from the others in terms of sensitivity. This may be due to crystalline defects in the silicon

substrate or variations in processing and diffusion during the manufacturing process. In HAMAMATSU NMOS linear image sensors, these variations are evaluated in terms of photo response non-uniformity (PRNU) by illuminating the image sensor with uniform light emitted from a tungsten lamp and measuring variations in the output from all pixels. PRNU is given by equation (18).

$$PRNU = (\Delta X/Xave) \times 100\ [\%] \cdots\cdots\cdots\cdots (18)$$

Xave: average output of all pixels
ΔX : difference between Xave and maximum or minimum pixel output

Our NMOS linear image sensor datasheets specify ±3% as the maximum PRNU.

Dark output

Dark output is an output that is generated even when no light strikes the image sensor. This is caused by recombination current within the photodiode depletion layer and the photodiode surface. Although the magnitude of dark output differs from pixel to pixel, it is a fixed pattern so that the dark output component can be removed by measuring “dark state” and “light state” data and obtaining the difference between them by means of software. Dark output is temperature-dependent, so it nearly doubles for every 5 °C increase in temperature. The dark output will increase during a long exposure but can be reduced by cooling the image sensor.

Noise and dynamic range

Noise is random output fluctuations over time and determines the detection limit in the low-light-level region. Noise includes dark current shot noise, incident light shot noise, charge amplifier reset noise, and amplifier noise. The charge amplifier reset noise can be reduced by using a clamp circuit. In NMOS linear image sensors, amplifier noise is predominant and increases as the video line capacitance becomes larger. Noise is defined by the standard deviation of the output. In HAMAMATSU S3901-128Q NMOS linear image sensor, noise is 3000 e^- rms when measured in the number of electrons and 0.5 fC rms in the charge. When defining the dynamic range as the ratio of the saturation charge (upper limit) to the noise (lower limit), the S3901-128Q dynamic range is 10^5 since the saturation charge is 50 pC and the noise is 0.5 fC. Effective methods for reducing the noise are to insert a low-pass filter in the signal processing circuit, perform low-speed readout, and average the data after acquiring ten or more data.

2-5 How to use

An external driver circuit for NMOS linear image sensors includes a digital circuit for generating input clock pulses and an analog circuit for converting output charges into voltage signals. The digital circuit consists of a clock oscillator circuit and a timing control circuit. Clock pulse signals should be input at CMOS logic levels. The analog circuit consists of an output processing circuit and an amplifier circuit. The output processing circuit normally uses a charge integration circuit including a charge amplifier. This method has the advantages that signal detection accuracy is high and it produces easy-to-process boxcar waveforms. Figure 2-4 shows a recommended block diagram of an external current integration method, and Figure 2-5 shows the timing chart.

Figure 2-4 Recommended block diagram (e ternal current integration method)

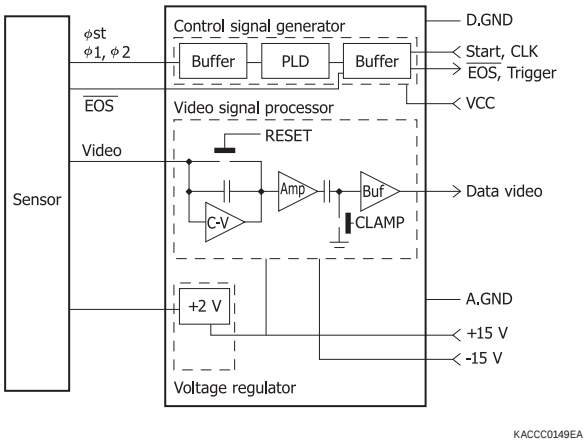
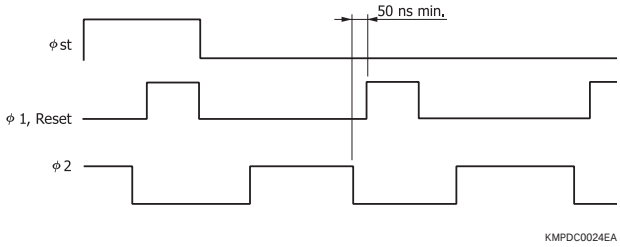


Figure 2-5 Timing chart



Immediately before the address switch connected to a photodiode turns on, a reset pulse discharges the feedback capacitance in the charge amplifier. When the address switch turns on, the charge stored in the photodiode is stored in the feedback capacitor. The relationship between the output voltage (Vout) of the charge amplifier and the stored charge (Qout) of the photodiode and the feedback capacitance (Cf) is expressed by equation (19).

$$Vout = Qout/Cf \cdots\cdots\cdots\cdots (19)$$

A capacitor of about 10 pF is used as the feedback capacitance. A clamp circuit is connected to the latter stage of the charge amplifier. The output of the clamp circuit should be connected to ground in the period immediately after the feedback capacitance is reset. This drastically reduces noise components generated when the feedback capacitance is reset.

Precautions when building the driver circuit

- Separate the analog circuit ground and the digital circuit ground.
- Connect the video output terminal to the amplifier input terminal in the shortest possible distance.
- Avoid crossing of analog and digital signals as much as possible.
- Use a series power supply having only small voltage fluctuations.

3. CMOS linear image sensors

In the CMOS process, unlike NMOS process technology, digital and analog circuits can be fabricated onto the chip. CMOS linear image sensors have signal processing and timing control circuits fabricated on the image sensor chip and so need only a simple external driver circuit. Functions difficult to implement in external circuits can be built into the image sensor to make it more sophisticated. A/D converters, for example, can be fabricated on the chip to output video data as digital signals. We also welcome requests for custom devices, so feel free to consult us for special orders.

3 - 1 Features

Incorporating a signal processing circuit into the sensor chip to match the required specifications integrates the following features into the sensor. This allows downsizing the photo-sensing systems and upgrading their functions.

- High-speed response
- High gain
- Low noise
- Digital output mode (with built-in A / D converter)
- Low voltage drive (3.3 V drive)

Table 3-1 CMOS linear image sensors

Type	Type no.	Number of pixels	Pixel size [µm (H) × mm (V)]	Video data rate max.
Standard type	S8377 series	128	50 × 0.5	500 kHz
		256		
		512		
	S8378 series	256	25 × 0.5	500 kHz
		512		
		1024		
	S9226-03	1024	7.8 × 0.125	200 kHz
High-speed type	S9227-03	512	12.5 × 0.25	5 MHz
	S10453 series	512	25 × 0.5	10 MHz
		1024		
Digital output type	S10077	1024	14 × 0.05	1 MHz

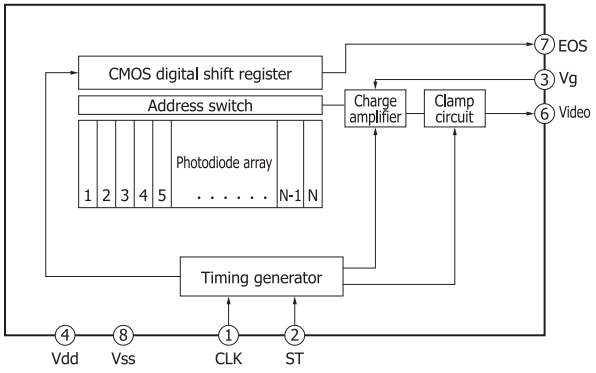
3-2 Operating principle and characteristics

Here we introduce the following three types among our CMOS linear image sensors.

Standard type S8377 / S8378 series

The S8377/S8378 series CMOS linear image sensors have on-chip circuits that are built in an external circuit section for NMOS linear image sensors. A block diagram is shown in Figure 3-1. Like NMOS linear image sensors, these CMOS linear image sensors consist of photodiodes, address switches, and shift registers. A timing generator is formed on the input side, and a signal processing circuit made up of a charge amplifier and clamp circuit forms the readout circuit on the output side.

Figure 3-1 Block diagram (S8377/S8378 series)



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The S8377/S8378 series operate only on a single 5 V power supply, ground, a clock pulse, and a start pulse. All pulses necessary to operate the shift register, charge amplifier, and clamp circuit are generated by the timing generator. An analog video output with boxcar waveform and an end-of-scan pulse are the output signals. The charge-to-voltage conversion gain can be adjusted in two steps by switching the charge amplifier's feedback capacitance via the input voltage to the gain selection terminal.

The peak sensitivity wavelength is 500 nm, which is shorter than NMOS linear image sensors. Since CMOS linear image sensors operate on a single 5 V power supply, their dynamic range is narrow compared to NMOS linear image sensors that operate on ±15 V supply. However, there is almost no difference in basic characteristics such as linearity accuracy and dark output compared to NMOS linear image sensor. CMOS linear image sensors are suitable for use in compact measurement systems since they need only a simple external driver circuit.

The S8377/S8378 series are available in six types with different pixel pitches and number of pixels. A variant type, S9226-03, is also available having the same block configuration but a different pixel format with 7.8 µm pitch, 0.125 mm active area height, and 1024 pixels.

In the S8377/S8378 series, since the signals are read out by a single charge amplifier in the last stage, the charge amplifier must be reset each time one pixel is read out. The maximum video data rate of the S8377/S8378 series is 500 kHz.

High-speed type S10453 series

The S10453 series CMOS linear image sensors have a simultaneous charge integration function for high-speed readout. The maximum video data rate is 10 MHz. The active area consists of 512 or 1024 pixels, each 0.5 mm in height and arrayed at a 25 µm pitch. In NMOS linear image sensors and S8377/S8378 series CMOS linear image sensors, a lag occurs in the pixel charge integration start/end times. However, the S10453 series has simultaneous integration and variable integration time functions (shutter function) controlled by an internal CMOS signal processing circuit, so charge integration in all pixels can start and end simultaneously.

The S10453 series has a CMOS amplifier array to convert charges to voltages. The conversion gain is determined by the charge amplifier's feedback capacitance. A small feedback capacitance of 0.1 pF allows a high output voltage.

Each photodiode pixel is connected to a charge amplifier. There is no switch between the photodiode and a charge amplifier. Since the photodiodes act as a current source, the generated signal charge is not stored in the photodiodes but is stored in the charge amplifier's feedback capacitance. The output voltage from the charge amplifier changes in proportion to the incident light level during the integration time. A hold circuit is connected following the charge amplifier of each pixel. The charge amplifiers of all pixels are simultaneously reset. By inputting a hold pulse to each hold circuit immediately before the charge amplifiers are reset, the charge amplifier outputs from all pixels are simultaneously held in their respective hold circuits. The time from when the reset switch for each charge amplifier is turned off to when the hold pulse is input to each hold circuit is the integration time. Charge integration therefore starts and ends simultaneously for all pixels. An address pulse from the shift register is next input to the latter-stage switch of each hold circuit, and the output signals held in the hold circuits are sequentially read out as a time-series signal from the video output terminal. Since this signal readout from the hold circuits is performed in a circuit separate from the operation for integrating the photodiode charges, the photodiodes and charge amplifiers can start the next charge integration while video output readout is in progress.

Figure 3-2 Block diagram (S10453 series)

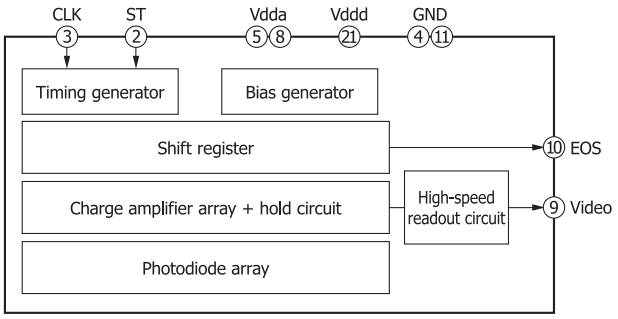

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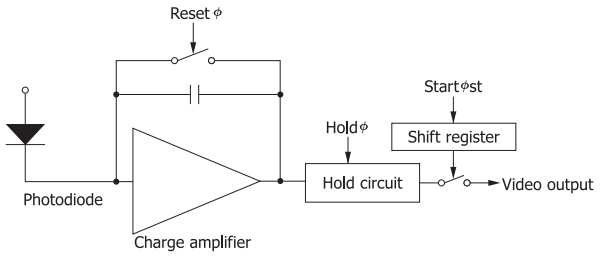
Figure 3-3 Equivalent circuit (S10453 series)



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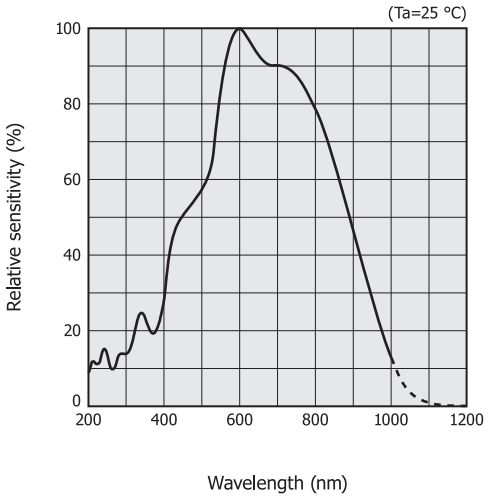
Two types of input pulses consisting of a clock pulse and a start pulse are required to operate the S10453 series. The reset pulses for the charge amplifiers, hold pulses for the hold circuits, and a start pulse for the shift register are all generated by the internal timing generator. Switching the start pulse from high to low initializes the timing generator which then sequentially generates the various control pulses. First, hold pulses are generated to hold the charge amplifier outputs in the hold circuits. Next, the reset pulses for the charge amplifiers are switched on to reset the charge amplifiers. No signal charges are integrated while the charge amplifiers are in a reset state. A start pulse is then input to the shift register to sequentially read out the video output as a time-series signal from the first pixel. When the start pulse changes from low to high, the reset pulses for the charge amplifiers are switched off, or in other words, charge integration starts. When the start pulse again changes from high to low, the timing generator is initialized as described above, and one cycle of operation is complete. Strictly speaking, charge integration starts 0.5 clocks after the start pulse has changed from low to high, and ends 0.5 clocks after the start pulse has changed from high to low. Therefore, the integration time is equal to the high period of the start pulse. If the length of one cycle is fixed, then the integration time can be adjusted by changing the ratio of high to low periods.

Figure 3-5 shows the S10453 series spectral response. The spectral response ranges from 200 to 1000 nm and displays a relatively smooth curve. The S10453 series allow stable measurement of ultraviolet light because their structure is designed to minimize sensitivity deterioration caused by ultraviolet light.

Figure 3-5 Spectral response (S10453 series typical e ample)



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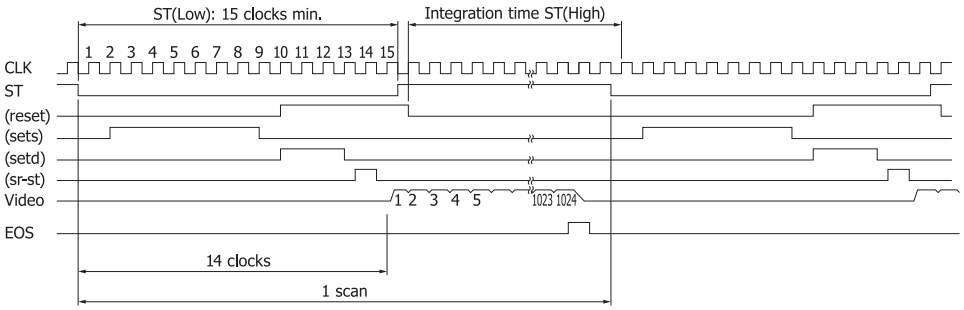
We also provide the S9227-03 linear image sensor that uses the same block configuration as the S10453 series but has a different pixel format with 12.5 µm pitch, 0.25 mm active area height, and 512 pixels. Although the S9227-03 is not sensitive to the ultraviolet region and the maximum video data rate is 5 MHz, it is better suited for compact systems since it utilizes a small package.

Digital output type S10077

The S10077 is a low power consumption CMOS linear image sensor incorporating a simultaneous integration function and internal A/D converter. It provides an 8-bit or 10-bit digital

Figure 3-4 Timing chart (S10453 series)



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output which is switchable. The maximum data rate is 1 MHz, and the S10077 can operate from a single supply voltage of 3.3 V at a power consumption of 30 mW. The active area consists of 1024 pixels at a height of 0.05 mm, arrayed at a 14 µm pitch. The simultaneous integration and variable integration time functions (shutter function) are controlled by an internal CMOS signal processing circuit.

Figure 3-6 Block diagram (S10077)

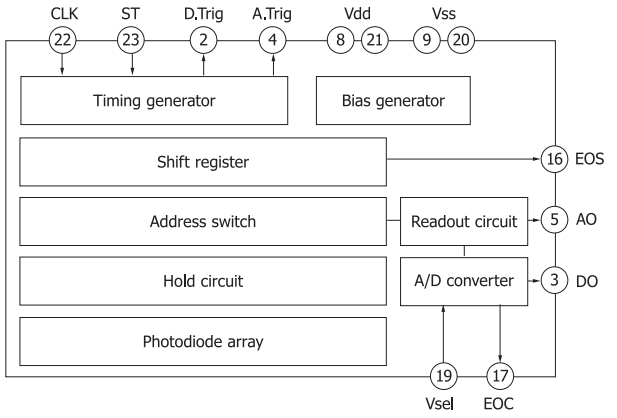
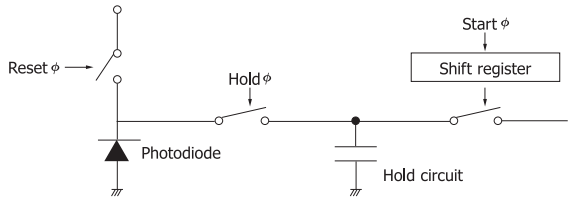


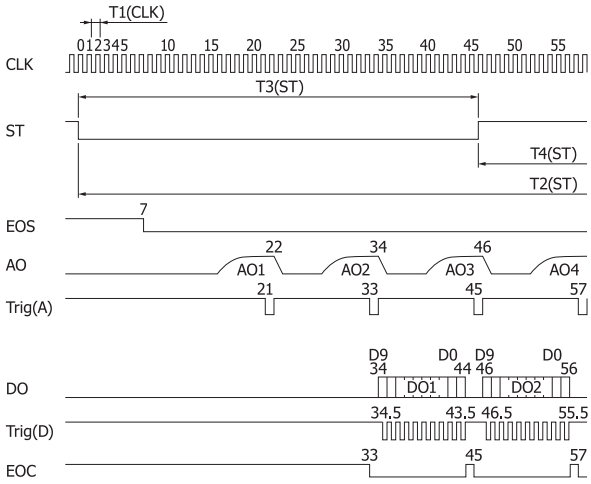
Figure 3-7 Equivalent circuit (S10077)



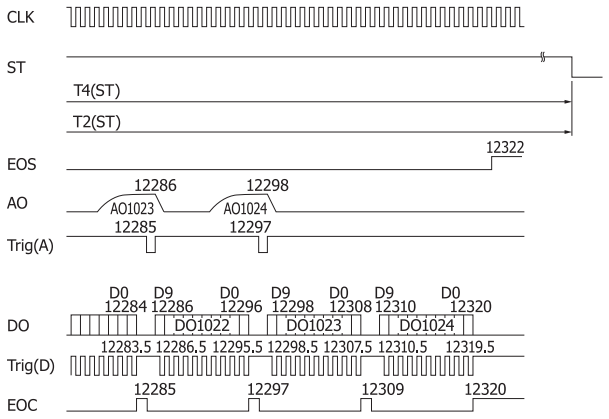
In the S10077, the signal charge stored in each photodiode is transferred to the hold circuit, and the resulting analog voltage is then sent from the readout circuit to the A/D converter via the address switch. The A/D converter converts the analog signal into a digital signal which is serially output from the MSB (most significant bit). Even though it has a small active area size, it delivers a high output voltage since the charge amplifier's feedback capacitance in the readout circuit is set to a small value of 0.05 pF. A switch and a hold circuit are connected to each photodiode pixel. During the integration time, the signal charge of each photodiode, which is proportional to the incident light level, is transferred to the hold circuit and held there. The photodiodes of all pixels are simultaneously reset. The integration time is from when the reset switch for each photodiode is turned off to when the hold pulse is turned on and then off. Charge integration therefore starts and ends simultaneously for all pixels. An address pulse from the shift register is next input to each hold circuit to allow the output signals being held to be sequentially read out as a time-series signal from the video output terminal. Since this signal readout from the hold circuits is performed in a circuit separate from the operation for integrating the photodiode charges, the photodiodes can start the next charge integration while video output readout is in progress.

Two types of input pulses consisting of a clock pulse and start pulse are required to operate the S10077 series. The reset pulses for the photodiodes, hold pulses for the hold circuits, and a start pulse for the shift register are all generated by the internal timing generator. Switching the start pulse from high to low initializes the timing generator which then sequentially generates the various control pulses. First, hold pulses are generated to hold the photodiode charges in the hold circuits. Next, the reset pulses for the photodiodes are switched on to reset the photodiodes. No signal charges are integrated while the photodiodes are in a reset state. A start pulse is then input to the shift register to sequentially read out the video output as a time-series signal from the first pixel. At the timing when the start pulse changes from low to high, the reset pulses for the photodiodes are switched off, or in other words, charge integration starts. When the start pulse again changes from high to low, the timing generator is initialized as described above, and one cycle of operation is complete. Strictly speaking, charge integration starts 0.5 clocks after the start pulse has changed from low to high, and ends 7.5 clocks after the start pulse has changed from high to low. Therefore, the integration time is equal to the sum of the high period of the start pulse and the period of 7 clock pulses. Within one cycle, the integration time can be adjusted by changing the ratio of high to low periods.

Figure 3-8 Timing chart (S10077 10-bit mode)
(a) icinity of start pi el



(b) icinity of last pi el



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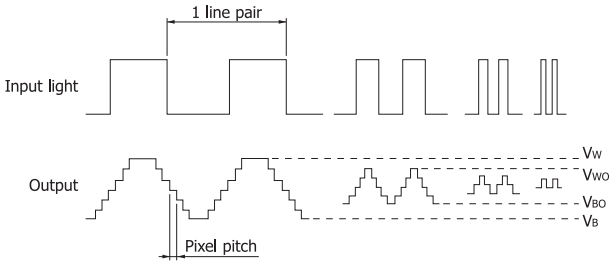
The contrast transfer function is described below to indicate the resolution of the S10077. Resolution is a measure of the degree of detail to which image sensors can reproduce an input pattern. The active area of an image sensor consists of a number of regularly arrayed photodiodes. As shown in Figure 3-9, when an image pattern of alternating black and white lines is input, an output corresponding to the input pattern appears. As the pulse width of the input pattern becomes narrower, the difference (contrast) between the black and white level outputs becomes smaller. A contrast transfer function (CTF) is used to express this relation and is given by equation (20).

$$CTF = \frac{V_{WO} - V_{BO}}{V_W - V_B} \cdots\cdots\cdots (20)$$

V_{WO}: output white level
V_{BO} : output black level
V_W : output white level (when input pattern pulse width is wide)
V_B : output black level (when input pattern pulse width is wide)

Figure 3-9 Contrast transfer function characteristics



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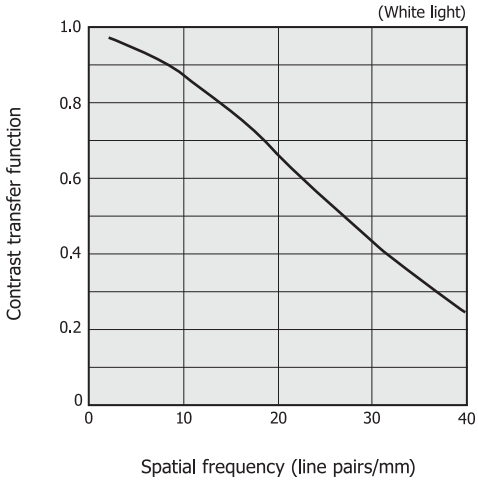
The fineness of the black and white lines for input pattern is given by the spatial frequency of the input image. The spatial frequency is the number of black and white line pairs per unit length. The higher this spatial frequency, the finer the input pattern, causing a drop in the contrast transfer function. Figure 3-10 shows an example of the S10077 contrast transfer function measurement.

Figure 3-10 Contrast transfer function vs. spatial frequency (S10077 typical e ample)



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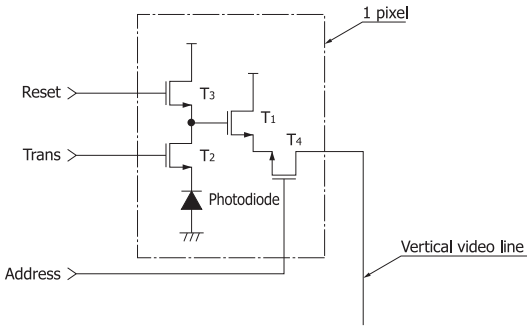
3 - 3 New approaches

HAMAMATSU is constantly striving to improve CMOS image sensors to achieve higher speeds, higher sensitivity, and more sophisticated functions.

One example of this effort is a high-speed CMOS linear image sensor with a video data rate of 50 MHz max. currently under development for industrial applications.

To achieve higher sensitivity, we are developing an active pixel sensor (APS). The CMOS image sensors we have been mainly manufacturing are passive pixel sensors whose structure uses a charge amplifier to read out the charges generated in each pixel according to their light levels. In contrast, active pixel sensors perform voltage conversion and amplification in each pixel. This will extend the lower limits of light detection to achieve a wider dynamic range.

Figure 3-11 Circuit of active pi el sensor



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We are also developing image sensors with more sophisticated functions by using our own silicon process technology and analog CMOS technology developed over the years for applications such as analytical instruments and medical equipment. By designing analog and digital circuits that meet current market needs into the same chip as the active area, we contribute to the functional enhancement and cost reduction of systems. Here, as

one example, we introduce an infrared-enhanced CMOS area image sensor. This image sensor has 384 × 256 pixels whose size is 12.2 × 12.2 µm. Our unique silicon process technology realized high sensitivity in the near infrared region [Figure 3-12]. A 12-bit A/D converter is included to allow signal readout at 60 frames max. per second. This image sensor also includes a timing generator and has a structure capable of selecting from a global shutter mode (simultaneous all-pixel integration format) and a rolling shutter mode (integration period differs for each line).

Figure 3-12 Spectral response (IR-enhanced CMOS area image sensor typical e ample)

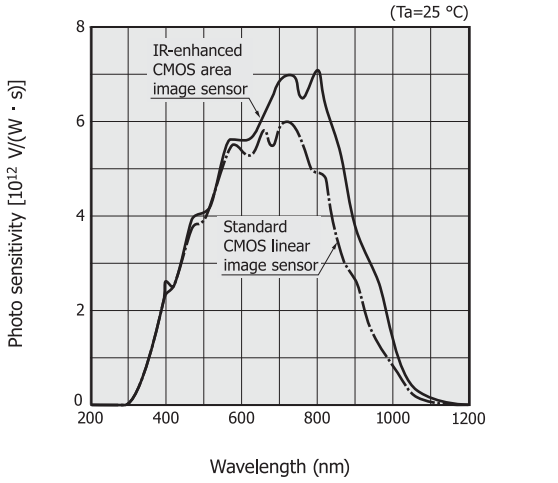
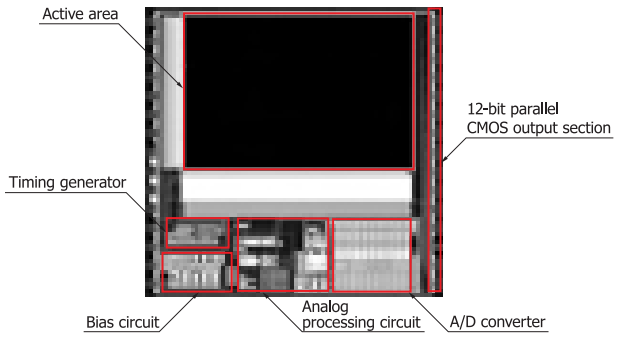


Figure 3-13 Enlarged view of chip (IR-enhanced CMOS area image sensor)



4. Photodiode arrays with ampli ers

Photodiodes with amplifiers are a type of CMOS linear image sensor designed for long and narrow area detection systems using an equal-magnification optical system. These devices combine a Si photodiode array with a CMOS signal processing IC. The CMOS signal processing IC contains a timing generator, shift register, hold circuit, and charge amplifier array, so only a simple external circuit is needed. A long and narrow image sensor can be configured by arranging multiple devices in a row. For X-ray detection applications, we also offer photodiode array/amplifier devices with a phosphor screen attached directly to their active area.

4 - 1 Features

- Long and narrow sensor can be configured by placement of multiple devices.
- 5 V operation
- Simultaneous integration by charge amplifier
- Time-series readout by shift register (data rate: 500 kHz max.)
- Low dark current due to zero-bias photodiode operation
- Internal clamp circuit achieves low noise and wide dynamic range.
- Internal timing generator allows operation with two types of input pulses (reset and clock).
- X-ray detection type available with a phosphor screen attached to the active area
- Usable with wide variety of photodiode specs (custom order item)

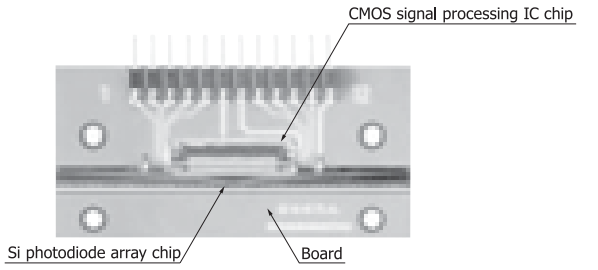
Table 4-1 HAMAMATSU photodiode arrays with ampli ers

Type	Type no.	Number of pixels	Pixel height (mm)	Pixel pitch (mm)	Effective area length (mm)	Line rate (lines/s)
Standard type (for industrial inspection)	S8865-64	64	0.8	0.8	51.2	7339
	S8865-128	128	0.6	0.4		3784
	S8865-256	256	0.3	0.2		1922
	S8866-64	64	1.6	1.6	102.4	6838
	S8866-128	128	0.8	0.8		3784
Phosphor screen type (for non-destructive inspection)	S8865-64G	64	0.8	0.8	51.2	7339
	S8865-128G	128	0.6	0.4		3784
	S8865-256G	256	0.3	0.2		1922
	S8866-64G-02	64	1.6	1.6	102.4	6838
	S8866-128G-02	128	0.8	0.8		3784

4 - 2 Structure

As shown in Figure 4-1, a photodiode array with amplifier consists of two chips: a Si photodiode array chip for light detection and a CMOS signal processing IC chip.

Figure 4-1 Chip layout on board (S8865 series)



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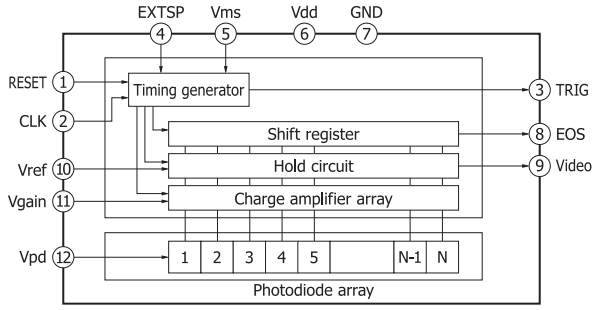
Signals from 64 pixels or 128 pixels at a time are handled by the CMOS signal processing IC. This makes the entire system configuration very simple compared to conventional methods that connect each pixel on the photodiode array to an external signal processing circuit.

Sensor devices with a phosphor screen attached to the active area are intended for X-ray detection. When X-rays irradiate a sensor device, the phosphor screen converts the X-rays into visible light which is then detected by the photodiode array. These devices are used as line sensors for X-ray non-destructive inspection tasks requiring long X-ray detectors.

4 - 3 Operating principle

The CMOS signal processing IC chip consists of a timing generator, shift register, hold circuit, and charge amplifier array [Figure 4-3]. Each pixel of the photodiode array is connected by wire bonding to the charge amplifier in the CMOS signal processing IC. The light-generated charge (Qout) in a photodiode, which is expressed by the product of the photocurrent (I_L) and the integration time (Ts), is converted into an output voltage (Vout = Qout/Cf) by the charge amplifier feedback capacitance (Cf). The output signal, which is sent to the hold circuit before the charge amplifier is reset, is read out by the shift register as time-series voltage signals. In the S8865/S8866 series, signals from all pixels are read out by the simultaneous integration method. The S8865/S8866 series also have a shutter function capable of adjusting the integration time. The maximum video data rate is 500 kHz.

Figure 4-3 Block diagram (S8865/S8866 series)



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4 - 4 Characteristics

Figure 4-4 shows the S8865 series spectral response.

Figure 4-4 Spectral response (S8865/S8866 series typical e ample)

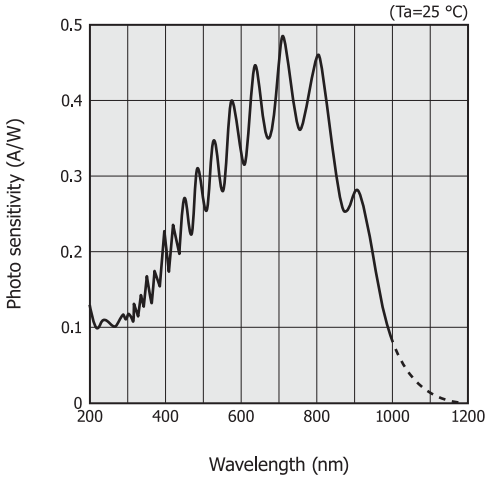

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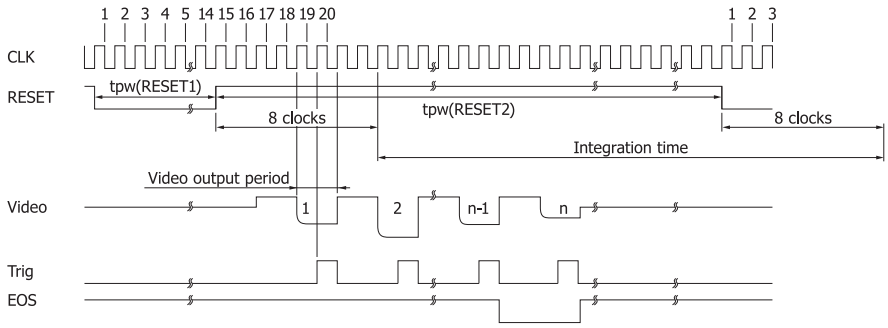
Figure 4-2 Timing chart (S8865 series)



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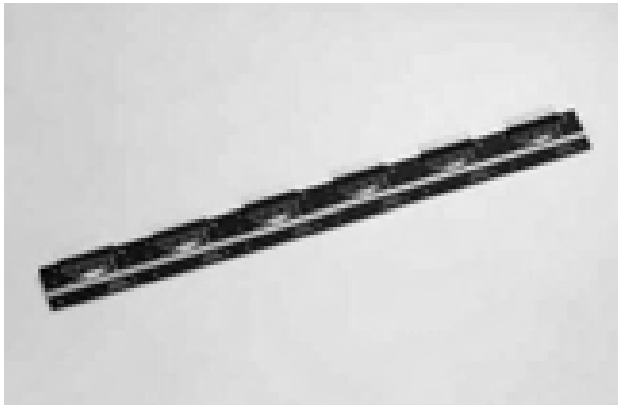
4 - 5 How to use

The S8865/S8866 series are designed so that the effective area length equals the board length. This allows easily configuring a long and narrow, one-dimensional detector system by arranging multiple sensors in a row. This type of system is difficult to create with normal image sensors. When multiple sensors are arrayed, the output signal from each sensor can be read out in parallel using multiple external circuits or read out serially using a single circuit. To read out signals serially, set the external voltage so that the preceding-stage end-of-scan signal is used as the next-stage start signal.

Besides fabricating image sensors with a long detection length, photodiode arrays with amplifiers also allow downsizing of detection systems. Using our standard CMOS signal processing IC chips makes it easy to create custom image sensors by just changing the Si photodiode array chips to a desired shape.

Figure 4-5 Long and narrow image sensor assembled by placement of multiple photodiode arrays with ampli ers



5. InGaAs linear image sensors

InGaAs linear image sensors are designed specifically for near infrared detection. These image sensors successfully minimize adverse effects from dark current by driving the InGaAs photodiode array at zero bias, and they deliver a wide dynamic range in the near infrared region.

Table 5-1 HAMAMATSU InGaAs linear image sensors

Type	Spectral response range (μm)	Number of pixels	Pixel size [μm (H) × μm (V)]
Standard type	0.9 to 1.7	256	50 × 250
			50 × 500
		512	25 × 250
			25 × 500
High-speed type		256	50 × 50
		512	25 × 25
		1024	25 × 100, 25 × 500
Long wavelength type	0.9 to 1.85	256	50 × 250
	0.9 to 2.05		
	0.9 to 2.25		
	0.9 to 2.55		

5 - 1 Features

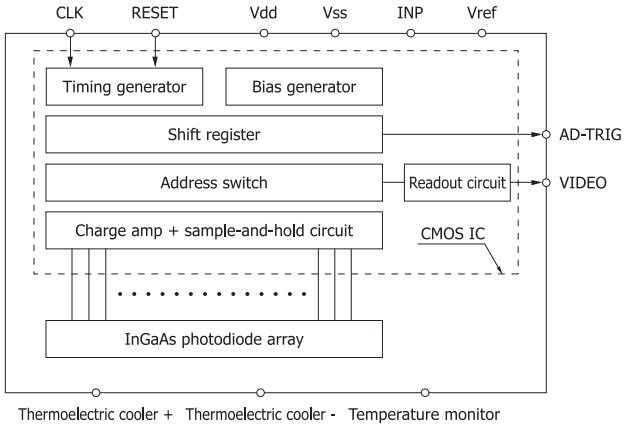
- Wide dynamic range
- Low dark current due to zero bias operation
- Wide spectral response range
- High gain due to charge amplifier
- Low noise due to CDS circuit
- Internal saturation control circuit
- Internal timing generator allows simple operation.
- Low crosstalk
- Selectable gain

5 - 2 Structure

InGaAs linear image sensors consist of an InGaAs photodiode array and a CMOS IC including a charge amplifier array, sample-and-hold circuit, shift register, readout circuit, and timing generator. The InGaAs photodiode array is connected to the CMOS IC by wire bonding or via bumps. Available packages include a ceramic package for room temperature operation and a metal package with a built-in thermoelectric cooler, which are selectable according to application. A typical block diagram for InGaAs linear image sensors is shown in Figure 5-1. An analog video output (VIDEO) and a digital output (AD-TRIG) for sample-and-hold can be obtained by

supplying analog inputs of +5 V (Vdd), GND (Vss), a charge amplifier reset voltage (INP), and a readout circuit reset voltage (Vref), as well as digital inputs of master clock pulse (CLK) and integration time control pulse (RESET).

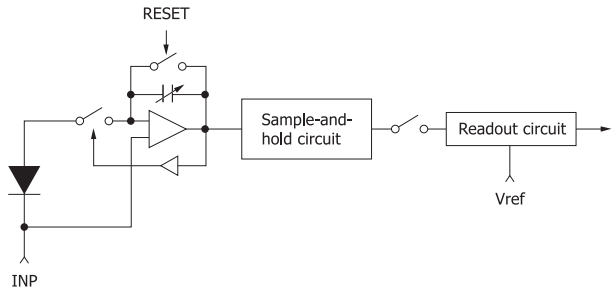
Figure 5-1 Block diagram



5-3 Operating principle

In the CMOS IC for InGaAs linear image sensors, a "charge amplifier and sample-and-hold circuit" array is formed and connected one-to-one to each pixel on the InGaAs photodiode array. Figure 5-2 shows an equivalent circuit for one pixel.

Figure 5-2 Equivalent circuit (for one pi el)



When light enters the photodiodes of an InGaAs linear image sensor, electric charges are generated and flow into the feedback capacitance of the differential-input charge amplifier. This differential-input charge amplifier can operate photodiodes at nearly zero bias, which suppresses the dark current. In actual operation, however, the amplifier has an offset voltage and the supply voltage to each pixel varies by about ±2 mV, so the video output of some pixels goes positive versus the reset level, while that of other pixels goes negative. Therefore, when no light is incident on the image sensor, extending the integration time increases the output on both the positive and negative sides. However, this output caused by the dark current is a fixed pattern, so the output signal resulting from light input can be extracted by subtracting the output due to the dark current from the output signal obtained with light incident on the image sensor. Since InGaAs photodiodes are made from a compound semiconductor, there are lattice defects and the dark current has relatively large absolute values and variations compared to Si photodiodes. The maximum integration time (integration time needed to reach saturation due to dark current) of InGaAs photodiodes therefore varies among the pixels. If a pixel with high dark current becomes saturated yet the charge integration still continues, then the charges that are no longer stored in the charge amplifier's feedback capacitance will flow out to the adjacent pixels, degrading the purity of the signal output (this is known as "blooming"). To avoid this blooming, each pixel has a circuit for stopping the charge integration by sensing whether the charge amplifier's feedback capacitance is saturated.

To extract continuous signals, the integration capacitance of the CMOS charge amplifier must be reset. A drawback of this, however, is that a large reset noise occurs. This reset noise must be removed to make measurements with high accuracy. In the CDS circuit for InGaAs linear image sensors, the integration start output is held in the signal processing circuit immediately after reset and the integration end output is then held to obtain the difference between the two outputs to eliminate the reset switching noise.

Incidentally, high-speed type image sensor circuitry gives priority to high-speed readout while standard type image sensor circuitry gives priority to a wide dynamic range.

5-4 Characteristics

Input / output characteristics

The relation between the light level incident to the image sensor and the signal output is referred to as the input/output characteristics. Since InGaAs linear image sensors operate in charge amplifier mode, the incident light exposure (unit: J) is expressed by the product of light level (unit: W) and integration time (unit: s).

The output from an InGaAs linear image sensor is represented in voltage. Figure 5-3 shows a schematic graph of input/output characteristics. The rising straight line portion in the figure can be expressed by equation (21).

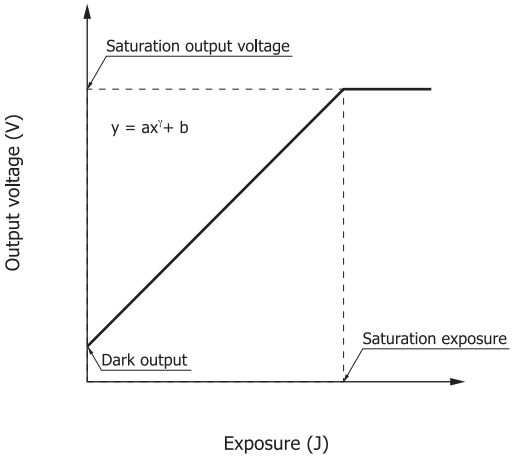
$$y = ax^{\gamma} + b \quad \cdots\cdots\cdots\cdots (21)$$

y: output voltage
x: light exposure
a: sensitivity (ratio of output to exposure)
b: dark output (output at exposure=0)
γ: slope coefficient

Since the upper limit of the output voltage is determined by the output voltage range of the charge amplifier, the input/output characteristics will have an inflection point even if the incident light exposure is increased linearly. The incident light exposure at this inflection point is referred to as the saturation

exposure, the output voltage as the saturation output voltage, and the amount of charge stored in the charge amplifier as the saturation charge.

Figure 5-3 Schematic graph of input/output characteristics (log graph)



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In our InGaAs linear image sensor datasheets, the saturation output voltage (Vsat) is defined as the saturated output voltage from light input minus the voltage at reset. Under the condition that no light is incident on the sensor (dark state), extending the integration time causes the output to increase on the positive and negative sides. The voltage going negative becomes saturated at approx. 0.5 V.

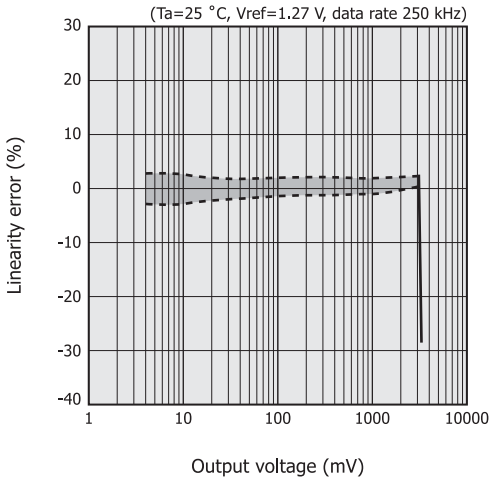
The saturation charge is calculated from the equation Q = C V based on the saturation output voltage. If the integration capacitance (Cf) is 10 pF and the saturation output voltage is 3.2 V, then the saturation charge will be 32 pC.

Linearity error

The slope coefficient (γ) of input/output characteristics shown in the preceding section corresponds to the slope plotted on the logarithmic graph. This γ value is 1, but during actual measurement, the input/output characteristics will slightly deviate from this. This deviation is known as the linearity error and is expressed in percentage.

Figure 5-4 shows the linearity error of the G9204-512S InGaAs linear image sensor obtained by random sampling. A linearity error at 95% or below the saturation exposure is within ±3%, which is quite small.

Figure 5-4 Linearity error (G9204-512S)



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Spectral response

When light energy incident on the active area formed with a PN junction is greater than the InGaAs band gap energy, the electrons in the valence band are excited into the conduction band, generating electron/hole pairs. This generated charge diffuses toward the photodiode depletion layer where the electric field accelerates the charge to pass through the PN junction, resulting in a signal for readout. If the light energy is smaller than the band gap energy, it cannot be detected. The cut-off wavelength (λc) is given by equation (22).

$$\lambda c = \frac{1.24}{Eg} \ [\mu m] \cdots\cdots\cdots (22)$$

Eg: band gap energy [eV]

The band gap energy for InxGa1-xAs (x=0.53) is 0.73 eV at room temperature, so the cut-off wavelength will be 1.7 µm. On the long wavelength type InxGa1-xAs (x=0.82), the band gap energy is 0.48 eV at room temperatures, so the cut-off wavelength will be 2.6 µm.

The light absorption coefficient for InGaAs differs depending on the light wavelength. The longer the light wavelength, the smaller the light absorption coefficient, and near the cut-off wavelength it decreases abruptly. The incident light at longer wavelengths penetrates deeper into the InGaAs substrate, generating carriers in deep positions within it. Since these carriers have a limited life, they can only diffuse a certain distance (diffusion length) after being generated. This means that, even when the same amount of light enters the InGaAs linear image sensor, the probability that the generated carriers can reach the depletion layer and eventually be detected as an output signal depends on the wavelength. Moreover, how the incident light undergoes interference, reflection, and absorption on the surface passivation film of the photodiode (such as the insulation film) depends on the wavelength and affects the sensitivity.

Figures 5-5 and 5-6 show examples of spectral response. The spectral response varies with the temperature. This is because the band gap energy is temperature-dependent. The InGaAs band gap energy increases as the temperature drops, causing the peak sensitivity wavelength and cut-off wavelength to shift to the short wavelength side.

Figure 5-5 Spectral response

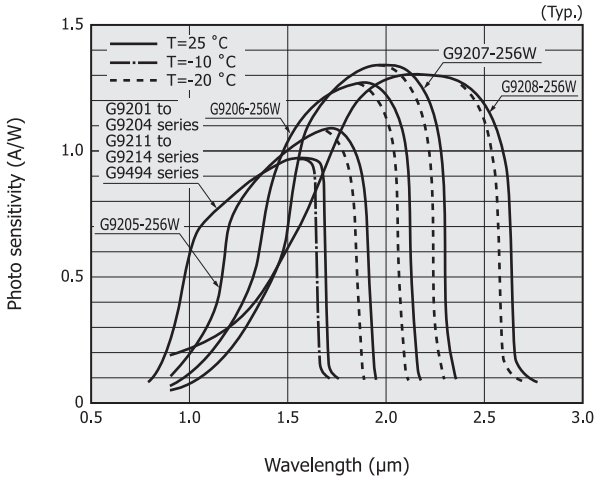


Figure 5-6 Spectral response (quantum ef ciency G9204-512S)

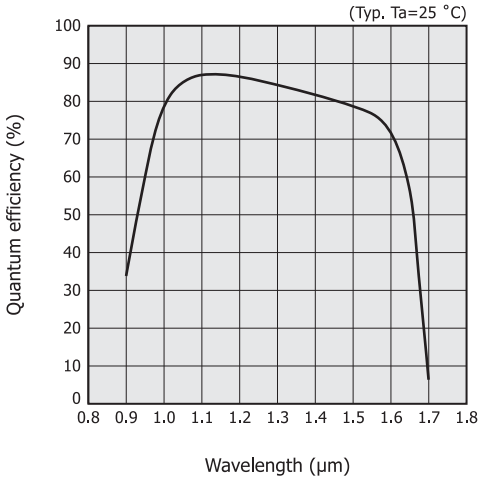


Photo response non-uniformity

InGaAs linear image sensors contain a large number of InGaAs photodiodes arranged in an array, yet sensitivity of each photodiode (pixel) is not uniform. This may result from crystal defects in the InGaAs substrate and/or variations in the processing and diffusion in the manufacturing process. For our InGaAs linear image sensors, variations in the outputs from all pixels measured when the effective active area of each photodiode is uniformly illuminated are referred to as photo response non-uniformity (PRNU) and defined as shown in equation (23).

$$PRNU = (\Delta X / X) \times 100\ [\%] \cdots\cdots\cdots (23)$$

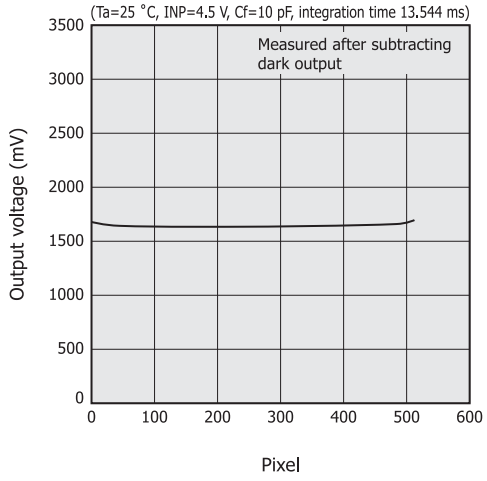
X : average output of all pixels
ΔX: absolute value of the difference between the average output X and the output of the maximum (or minimum) output pixel

In our outgoing product inspection for photo response non-uniformity, the output is adjusted to approx. 50% of the saturation output and a halogen lamp is used as the light source. Since InGaAs linear image sensors use a compound semiconductor crystal for light detection, the photodiode array may contain crystal defects, resulting in abnormal output signals from some of the pixels (defect pixels). Maximum photo response non-uniformity is specified as being within ±5% for the G9201 series and G9211 series and within ±10% for the G9205 to G9208 series.

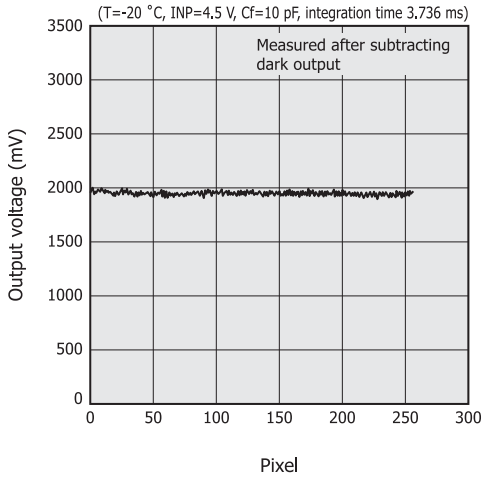
Scratches and dust on the light input window may also cause the sensitivity uniformity to deteriorate. So caution should be exercised on this point when handling image sensors. Figure 5-7 shows typical examples of photo response non-uniformity. These data were obtained by random sampling.

Figure 5-7 Photo response non-uniformity (typical e ample)

(a) G9204-512S



(b) G9207-256



Dark output

The dark output is the output generated even when no incident light is present. This output is caused by the dark current (sum of diffusion current, recombination current, and surface leakage current) within the photodiode depletion layer, which flows to charge the charge amplifier and is converted into a voltage output. Since the upper limit of the output is determined by the saturation charge, a large dark output narrows the dynamic range of the output signal. The output signal is the sum of the output generated by light and the dark output, so the purity of the output signal can be improved by using signal processing to subtract the dark output from each pixel.

The dark output is given by equation (24). The integration time significantly affects the dark output and must therefore be determined by taking the magnitude of the dark output into account.

$$Vd = I_D \times Ts / Cf \quad \cdots\cdots\cdots\cdots (24)$$

Vd: dark output voltage [V]
I_D : dark current [pA]
Ts: integration time [s]
Cf : integration capacitance [pF]

When rewriting the above equation in terms of integration time (Ts) by substituting the saturation output voltage (Vsat) for the dark output voltage (Vd), the maximum integration time (Tsmax) is expressed by equation (25).

$$Tsmax = Cf \times Vsat / I_D \quad \cdots\cdots\cdots\cdots (25)$$

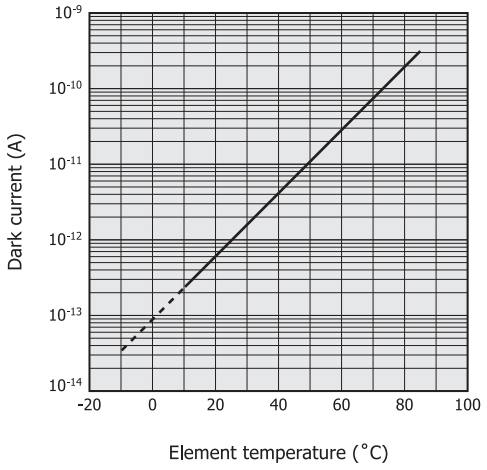
The band gap widens as the temperature decreases, so the number of carriers thermally excited into the valence band from the conduction band decreases, causing the dark current to reduce exponentially with the temperature. In our InGaAs linear image sensors, the temperature coefficient β of the dark current is 1.06 to 1.1. If the dark current at temperature T_1 (unit: °C) is I_{DT1} (unit: A), then the dark current I_{DT} at temperature T is given by equation (26).

$$I_{DT} = I_{DT1} \times \beta^{(T - T_1)} \text{ [A]} \quad \cdots\cdots\cdots\cdots (26)$$

When extending the integration time, equation (26) is used to determine the temperature setting.

Figure 5-8 shows the temperature characteristic of the G9204-512S dark current (random sampling).

Figure 5-8 Dark current vs. element temperature (G9204-512S typical e ample)



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Noise

InGaAs linear image sensor noise can be largely divided into fixed pattern noise and random noise.

Fixed pattern noise includes photodiode dark current which is current noise from the DC component. The magnitude of the fixed pattern noise is constant even if readout conditions are changed, so it can be canceled by using an external signal processing circuit.

Random noise, on the other hand, results from fluctuations in voltage, current, or charge that are caused in the signal output process in the sensor. When the fixed pattern noise has been canceled by external signal processing, the random noise will then determine the InGaAs linear image sensor's lower detection limit or lower limit of dynamic range.

Random noise includes the following four components:

① Dark current shot noise (Nd)
② Signal current shot noise at light input (Ns)
③ Charge amplifier reset noise (Nr)
④ CMOS charge amplifier readout noise (N_R)

In general, the reset noise③ that occurs when the charge amplifier is reset is predominant. This reset noise can be greatly reduced with a CDS circuit, so the dark current shot noise ① and CMOS charge amplifier readout noise ④ become significant sources of noise. Dark current shot noise results from erratic generation of the output charge due to dark current. This noise becomes larger as the output charge due to dark current increases, and therefore varies depending on operating conditions such as integration time and temperature.

Signal current shot noise ② is caused by fluctuations due to incident photons arriving randomly at the sensor.

The total noise (N) is expressed by equation (27).

$$N = \sqrt{Nd^2 + Ns^2 + N_R^2} \quad \cdots\cdots\cdots\cdots (27)$$

The dark current shot noise (Nd) and signal current shot noise

at light input (Ns) can be expressed as the root square of the generated charge by representing them as an “equivalent input noise charge” which is a value converted to a charge quantity for input to the image sensor.

$$Nd = \sqrt{\frac{2 \cdot I_D}{q}} \times T_S \ [e^- \text{ rms}] \quad \cdots\cdots\cdots\cdots (28)$$

$$Ns = \sqrt{\frac{2 \cdot I_S}{q}} \times T_S \ [e^- \text{ rms}] \quad \cdots\cdots\cdots\cdots (29)$$

Is: signal current by light input
q : electron charge

We specify the noise level in InGaAs linear image sensors as fluctuations in the output voltage of each pixel by using root-mean-square noise voltage (V rms) units. Converting equations (28) and (29) into voltage therefore gives equations (30) and (31), respectively.

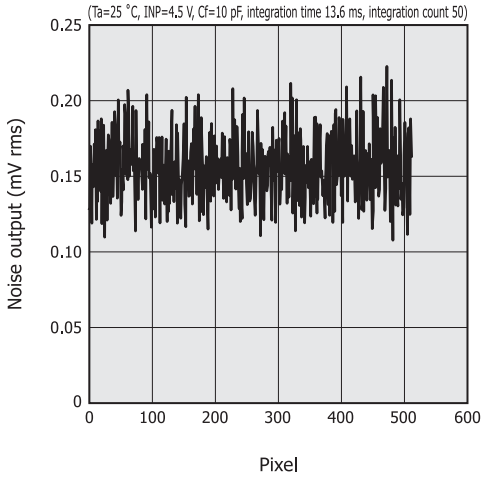
$$Nd = \sqrt{2 \cdot q \cdot I_D} \times \frac{Ts}{Cf} \ [\text{V rms}] \quad \cdots\cdots\cdots\cdots (30)$$

$$Ns = \sqrt{2 \cdot q \cdot I_S} \times \frac{Ts}{Cf} \ [\text{V rms}] \quad \cdots\cdots\cdots\cdots (31)$$

When the CMOS charge amplifier readout noise (N_R) is measured at 25 °C using an integration time of 1 ms, a data rate of 31.25 kHz, and an integration count of 50, the standard deviation in the G9201 series is calculated to be 180 µV rms at Cf=10 pF and 400 µV rms at Cf=0.5 pF. The noise levels listed for the G9201/G9211 series in our datasheet are measured at 25 °C using an integration time of 10 to 20 ms, data rate of 31.25 kHz, and integration count of 50 in order to calculate the standard deviation. In the G9205 to G9208 series, this measurement is made at -20 °C using an integration time of 1 ms or less, data rate of 31.25 kHz, and integration count of 50. Figure 5-9 shows output noise fluctuations measured with the G9204-512S and G9207-256W with no incident light. These data were obtained by random sampling.

Figure 5-9 Noise output uctuations

(a) G9204-512S



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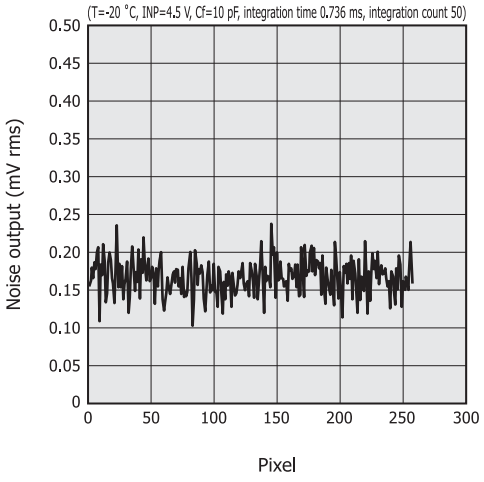
(b) G9207-256



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5 - 5 How to use

This section explains how to use and operate InGaAs linear image sensors including handling precautions and setting operating conditions.

Setups

There are two types of InGaAs linear image sensors: a thermoelectrically cooled type that contains a thermoelectric cooler and thermistor, and a non-cooled type. Both types basically operate with the same drive method except for cooling operation.

(1) Terminal description

Make connections by referring to Figures 5-10 and 5-11 and to Table 5-2.

Figure 5-10 Pin connections (G9201 to G9204 series top view)

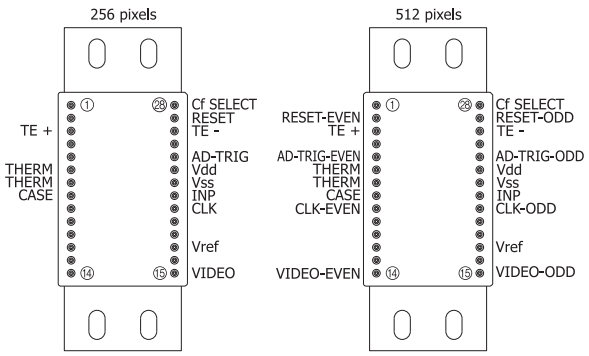

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Table 5-2 Terminal function and recommended connection

Terminal name	Input/output	Function and recommended connection
CLK	Input (CMOS logic compatible)	Clock pulse for operating the CMOS shift register
RESET	Input (CMOS logic compatible)	Reset pulse for initializing the feedback capacitance in the charge amplifier formed in the CMOS chip. The width of the reset pulse is the integration time.
Vdd	Input	Supply voltage for operating the signal processing circuit in the CMOS chip
Vss	Input	Ground for the signal processing circuit in the CMOS chip
INP	Input	Reset voltage for the charge amplifier array in the CMOS chip
Cf SELECT	Input	Voltage that determines the conversion efficiency in the CMOS chip
CASE	-	This terminal is electrically connected to the package.
THERM	Output	Thermistor for monitoring temperature inside the package
TE+, TE-	Input	Power supply terminal for the thermoelectric cooler that cools the photodiode array. No connection for room temperature operation type.
AD-TRIG	Output	Digital signal for A/D conversion; positive polarity
VIDEO	Output	Analog video signal; positive polarity
Vref	Input	Reset voltage for the offset compensation circuit in the CMOS chip

Figure 5-11 Setup and wiring

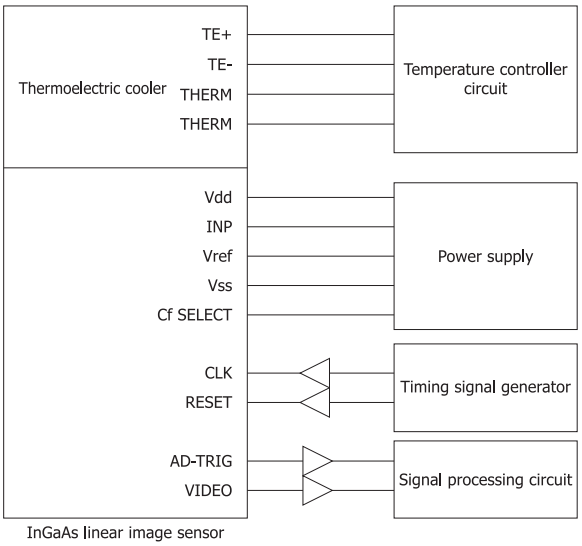

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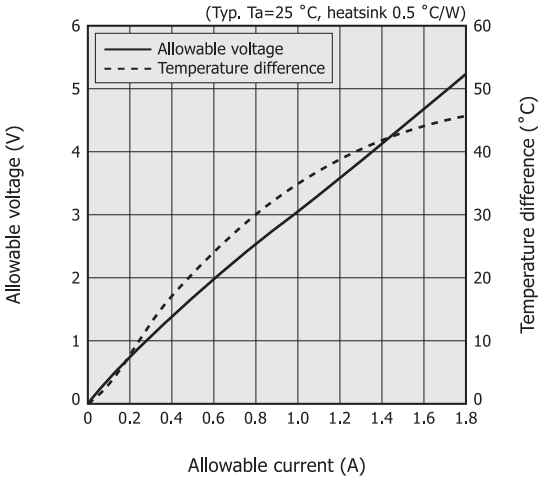
Figure 5-12 Temperature characteristics of one-stage thermoelectrically cooled device



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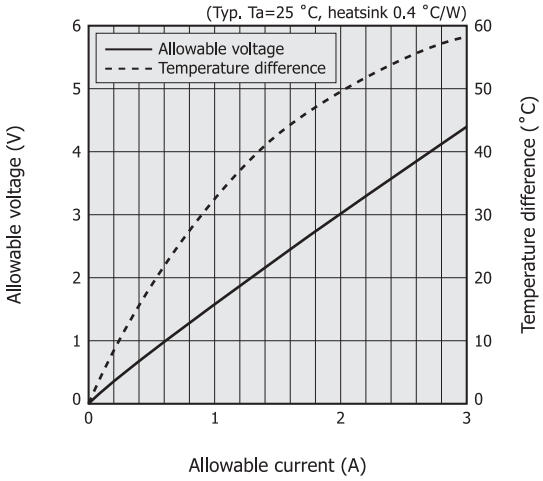
(2) Heatsink

- Selecting a heatsink

When cooling a one-stage thermoelectrically cooled device to -10 °C, select a heatsink of 0.5 °C/W or less including a safety margin. When cooling a two-stage thermoelectrically cooled device to -20 °C, select a heatsink of 0.4 °C/W or less.
Equipment should be carefully designed so that the heatsink is not placed where heat builds up. Provide good air ventilation to allow heat emitted from the heatsink to sufficiently dissipate by installing air fans and ventilation ducts. Note that the heatsink thermal resistance varies according to forced air cooling.

Figure 5-13 Temperature characteristics of two-stage thermoelectrically cooled device



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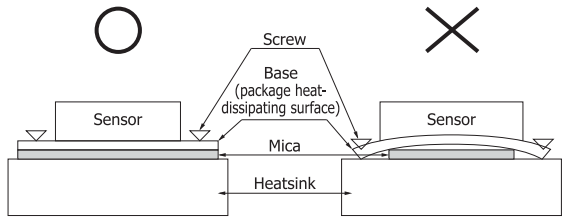
• Heatsink mounting method

To allow the thermoelectric cooler to exhibit fullest cooling capacity, the heatsink must be mounted correctly onto the sensor package. Mount the heatsink while taking the following precautions.

- Check that the heatsink attachment surface and the heat-dissipating surface of the InGaAs image sensor package are clean and flat.
- Mount the heatsink so that it makes tight contact with the entire heat-dissipating surface of the package. The heat-dissipating surface area should be large to improve the cooling efficiency and prevent possible damage.
- Apply a thin coat of heat-conductive grease uniformly over the attachment surface in order to lower thermal resistance between the package heat-dissipating surface and the heatsink. Fasten the sensor package to the heatsink with screws so that the grease spreads more uniformly. When a mica sheet is used, it must also make contact with the entire heat-dissipating surface of the package. The cooling efficiency will degrade if the sensor package is fastened to the heatsink with screws while the mica sheet is still too small to cover the screw positions. This may also warp the package base, causing cracks between the sensor and the package base [Figure 5-14 (a)].
- Do not press on the upper side of the package when fastening the sensor package to the heatsink or printed circuit board. If stress is applied to the glass faceplate bonding point, this may cause the faceplate to come off or may impair airtightness of the package [Figure 5-14 (b)].

Figure 5-14 Sensor mounting method

(a) Example 1



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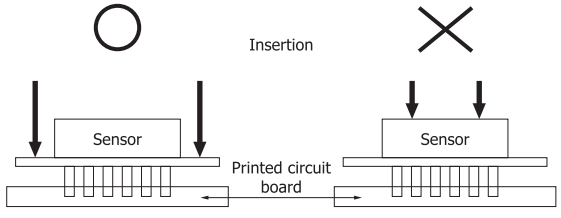
(b) Example 2



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(3) VIDEO signal monitoring

The image sensor output end does not have a drive capability, so in order to monitor the VIDEO signal, the sensor output should be amplified by a buffer amplifier and then fed to an oscilloscope.

Drive method

Sensor operation should be checked in a dark state. Block the light falling on the active area before checking operation.

(1) Turning on power to the driver circuit

First check that the power supplies provide correct voltage outputs for Vdd, INP, and Vref, and then turn the power on. At this point, also check that the current values are correct. If excessive current is flowing, the power supply line might be shorted so immediately turn off the power and check the power supply line.

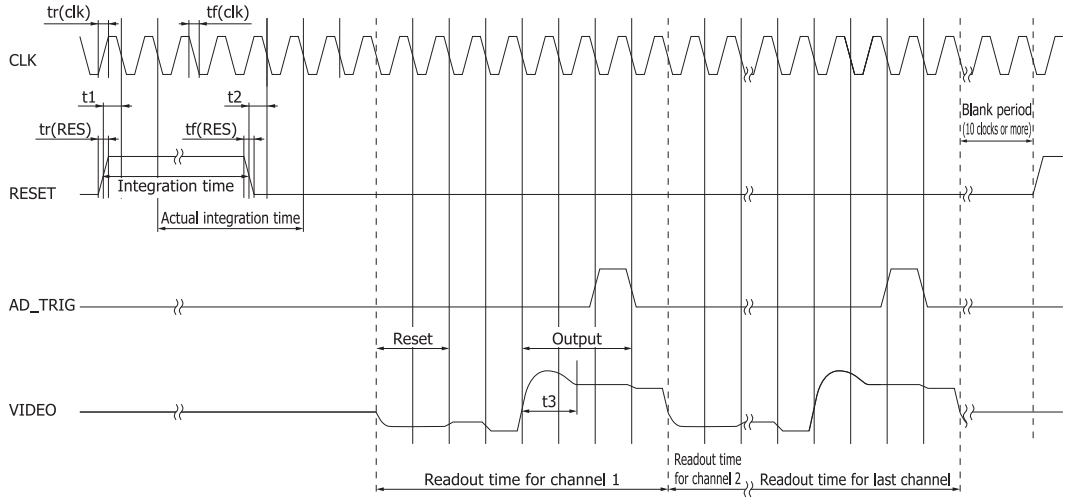
(2) Inputting control signals from the pulse generator

While referring to the timing chart shown in Figure 5-15, input the control signals from the pulse generator to the InGaAs linear image sensor (G9201/G9494 series). Two control signals (CLK and RESET) are input to the image sensor and must be H-CMOS level inputs. The image sensor may malfunction if other control signal levels are used. In the G9201/G9494 series, set the RESET signal pulse width to at least 6 µs. The CLK signal frequency determines the VIDEO signal readout frequency, and the RESET pulse interval determines the integration time.

Normal operation is performed whether the CLK and RESET signals are synchronized or not. When the RESET pulse rising edge is synchronized with the CLK pulse falling edge, the integration starts at the falling edge of the CLK pulse following the RESET pulse rising edge. When not synchronized, the integration starts at the falling edge of the second CLK pulse from the RESET pulse rising edge. When the RESET pulse falling edge is synchronized with the CLK pulse falling edge, the integration ends with the falling edge of the CLK pulse following the RESET pulse falling edge. If not synchronized, the integration ends with the falling edge of the second CLK pulse from the RESET pulse falling edge.

Figure 5-15 Timing chart

(a) G9201 series



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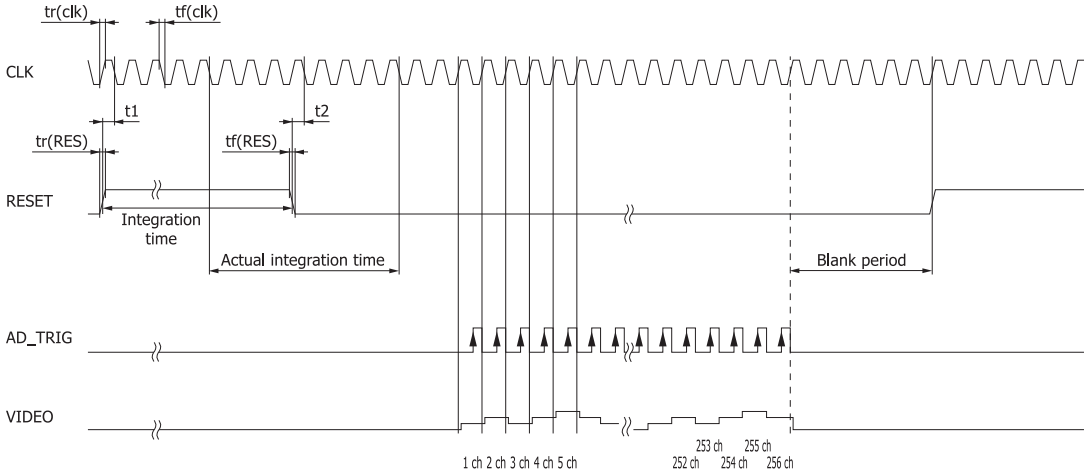
Parameter	Symbol	Min.	Typ.	Max.	Unit
Clock pulse frequency	-	0.1	-	4	MHz
Clock pulse width	tpw(clk)	100	-	-	ns
Clock pulse rise/fall times	tr(clk), tf(clk)	0	20	100	ns
Reset pulse width	tpw(RES)	6000	-	-	ns
Reset pulse rise/fall times	tr(RES), tf(RES)	0	20	100	ns
Reset (rise) timing	t1	50	-	-	ns
Reset (fall) timing	t2	50	-	-	ns
Output settling time	t3	-	-	600	ns

(b) G9494 series



Note: At least 3 µs are required from the last pixel to the RESET pulse rising edge.

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Parameter	Symbol	Min.	Typ.	Max.	Unit
Clock pulse frequency	-	0.1	2	4	MHz
Clock pulse width	tpw(clk)	100	-	-	ns
Clock pulse rise/fall times	tr(clk), tf(clk)	0	20	100	ns
Reset pulse width*	tpw(RES)	6/f	-	-	µs
Reset pulse rise/fall times	tr(RES), tf(RES)	0	20	100	ns
Reset timing	t1, t2	50	-	-	ns
Video delay time	tvd	100	-	-	ns

* Reset pulse width must be 6 µs or more.

(3) Setting the integration time

- Example 1: When operating an InGaAs linear image sensor G9201-256S at a CLK frequency of 1 MHz

Since the VIDEO signal readout frequency is 1/8 of the CLK signal frequency, the readout time (tr) per pixel is 8 µs. The time required for one scan (tscan) is therefore given by equation (32).

$$tscan = (tc \times 10) + (tr \times N) \cdots\cdots (32)$$
$$= 1\ [\mu s] \times 10 + 8\ [\mu s] \times 256$$
$$= 2058\ [\mu s]$$

tc: CLK period
N: number of pixels

In this case, the reset time [low period of RESET in Figure 5-15 (a)] must be longer than the time required for one scan, so set the scan time (tscan) longer than 2058 µs. Note that the scan time becomes slightly longer depending on the RESET pulse width and the synchronization with the CLK signal.

- Example 2: When operating an InGaAs linear image sensor G9494-256D at a CLK frequency of 2 MHz

Since the VIDEO signal readout frequency equals the CLK signal frequency, the readout time (tr) per pixel is 0.5 µs. The time required for one scan (tscan) is therefore given by equation (33).

$$tscan = (tc \times 6) + (tr \times N) \cdots\cdots (33)$$
$$= 0.5\ [\mu s] \times 6 + 0.5\ [\mu s] \times 256$$
$$= 131\ [\mu s]$$

tc: CLK period
N: number of pixels

The reset time must be longer than the scan time, so set the reset time longer than 131 µs. Note that the scan time becomes slightly longer depending on the RESET signal pulse width and the synchronization with the CLK signal.

(4) Turning on the power supply for the thermoelectric cooler

Use extra caution to avoid damaging the image sensor when turning on the power to the thermoelectric cooler. Take the following precautions when designing a power supply circuit for the thermoelectric cooler.

- Never exceed the absolute maximum ratings for the thermoelectric cooler.
- Make sure that the power supply voltage and connection polarity are correct. Turning on the power supply with the wrong voltage or polarity will damage the image sensor.
- Use a power supply having as low a noise and low ripple as possible, and also use power supply wires thick enough to keep resistance as low as possible. The TE+ and TE- wires in particular must be sufficiently thick.
- Be sure to provide an over-current safeguard circuit to protect the thermoelectric cooler from being damaged.
- Provide a protection circuit that monitors the temperature on the heat-emitting side of the heatsink to prevent the heatsink temperature from exceeding the specified level due to excessive cooling.
- While referring to Figures 5-12 and 5-13, set the optimum voltage and current values that maintain the target temperature.

5-6 New approaches

InGaAs image sensors are widely used for near infrared spectrophotometry. When a sample is irradiated with near infrared light, it reflects or transmits the light. A characteristic spectrum is obtained by separating the reflecting or transmitting diffused light into individual wavelengths. This spectrum contains multiple pieces of information regarding the components of the sample, so measuring this spectrum allows for rapid, non-destructive quantitative/qualitative analysis. Near infrared spectrometers have been downsized and are widely used not only in laboratories but also on production lines or in outdoor locations.

Near infrared image sensor applications are spreading from spectrophotometry to optical communications and are likely to expand to include more fields than ever. Near infrared image sensors will prove especially useful in biological activity measurement in the region from 900 to 1300 nm which exhibits high transmission properties and is less affected by water. As one example, in fundus (back of the eye) examinations using optical coherent tomography (OCT) technology, near infrared light at 1060 nm has higher transmission property through the eyeballs compared to 830 nm light used in current inspection light sources, making it possible to observe images at a deeper position. HAMAMATSU is developing high-speed InGaAs

linear image sensors optimized for this application. These image sensors employ a multiport readout format that reads out the data in parallel by dividing the pixels into multiple ports.

Figure 5-16 Multiport e ample
(8-port high-speed InGaAs linear image sensor)

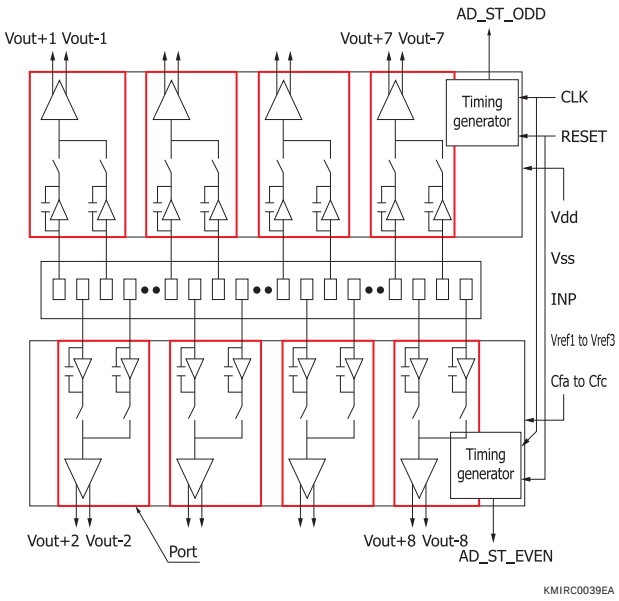


Table 5-3 Speci cation e amples for high-speed InGaAs linear image sensor

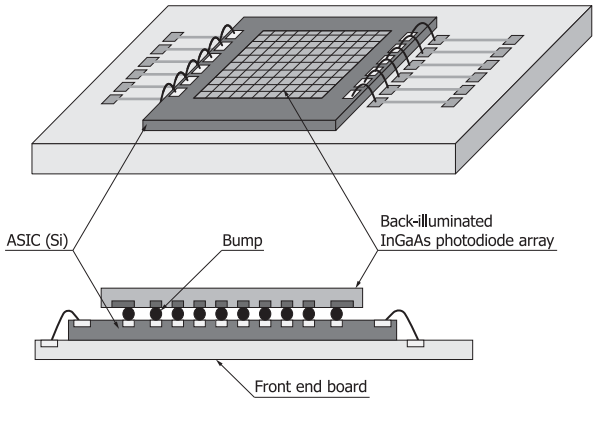
Parameter	Value	Unit
Number of pixels	1024	pixels
Pixel pitch	25	µm
Pixel size (H × V)	25 × 100	µm
Spectral response range	0.9 to 1.7	µm
Line rate	41000 max.	lines/s
Data rate	5 typ., 6.3 max.	MHz

Recently, there is an increasing demand for multichannel photometry in the visible region along with the near infrared region. These measurements utilize both Si and InGaAs image sensors. By applying our InGaAs photodiode process technology for enhancing short-wavelength sensitivity, we are now developing short-wavelength enhanced InGaAs image sensors that cover a wide spectral range from 500 to 1700 nm with a single sensor.

This expanded field of applications means that infrared image sensors will need higher cost performance. Meeting this requirement will require fabricating larger wafers and smaller chips in order to yield a greater number of chips from one wafer.

To solve this challenging problem, back-illuminated structures will help reduce the chip size as well as decrease the wiring capacitance to achieve higher speeds. Moreover, integrating a narrow-pitch charge amplifier array into a single chip offers the advantage that output variations caused by differences in the video line of each chip, which have long been a problem with conventional devices, can be suppressed. Manufacturing back-illuminated structures will also lead to development of two-dimensional devices. We are also working hard to develop an InGaAs area image sensor by combining an InGaAs photodiode array with an ASIC (application-specific integrated circuit) to meet specific applications.

Figure 5-17 Schematic representation of InGaAs area image sensor



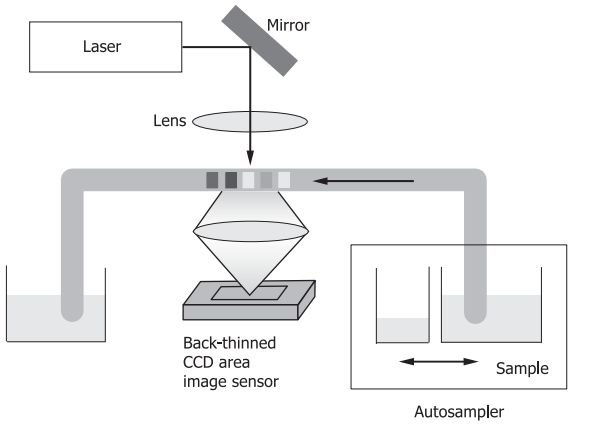
6. Applications

6 - 1 DNA sequencer

Here we introduce the DNA sequencer, which is one typical application for back-thinned CCDs. The DNA sequencer uses laser light to excite DNA fragments labeled with fluorescent dye and separated according to molecular weight, and then sequentially reads out their base sequence by detecting the resulting fluorescent light.

The DNA sequencer must be able to detect the faint fluorescent light representing the four DNA bases (adenine, thymine, cytosine, and guanine) with good accuracy, and it utilizes back-thinned CCDs having high sensitivity close to the detection limit in the visible light range.

Figure 6-1 Schematic of DNA sequencer



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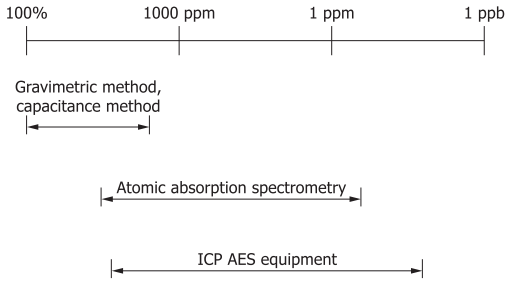
6 - 2 ICP AES equipment

The ICP AES (inductively coupled plasma atomic emission spectroscopy) equipment performs qualitative and quantitative analysis of trace metals within a liquid. ICP AES equipment is currently in high demand for making environmental measurements and analysis.

ICP AES equipment requires high detection sensitivity and accuracy, and therefore uses back-thinned CCDs with low noise and high sensitivity. The spectral range to be detected partly includes ultraviolet light, so our back-thinned CCDs with high ultraviolet sensitivity are found beneficial in enhancing the sensitivity of ICP AES equipment.

Figure 6-2 Sensitivity comparison between various types of analytical technique



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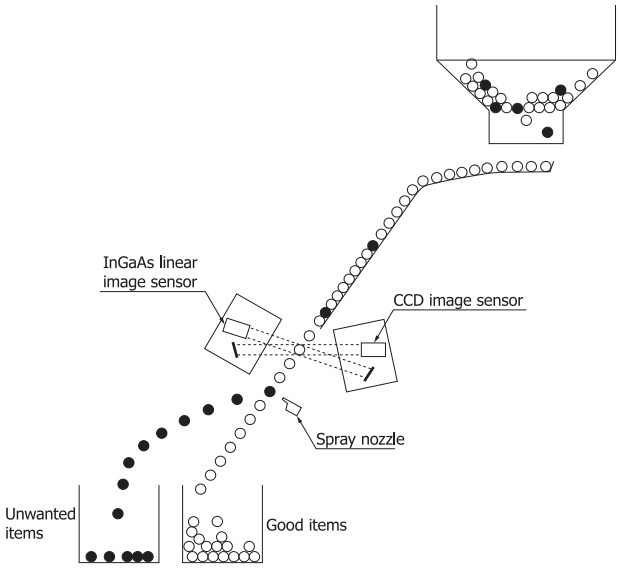
6 - 3 Spectrophotometers

The S9971 series of front-illuminated CCD image sensors with an internal thermoelectric cooler has a Lumogen coating and is therefore used in spectrophotometry over a broad spectral range (200 to 1200 nm). The S9971 series is low cost compared to back-thinned CCDs with the same active area size, making it suitable as a sensor in compact spectrophotometers. We also provide PMA (photonic multichannel analyzer) and mini-spectrometers that incorporate our CCD image sensors and InGaAs linear image sensors.

6 - 4 Grain sorters

Grain sorters irradiate light onto the falling grain, identify unwanted items from the reflected or transmitted light, and then remove those from the grain by high-pressure air spray. Using InGaAs linear image sensors in the grain sorter allows simultaneously identifying multiple grain types while analyzing grain components.

Figure 6-3 Schematic of grain sorter

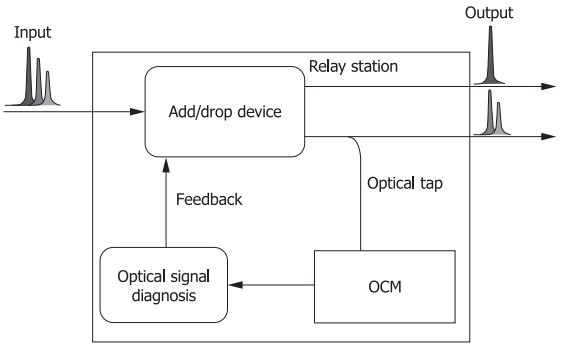


KMIRC0037EA

6 - 5 Optical channel monitors

Devices called optical channel monitors (OCM) fulfill an important role in monitoring the signal wavelength and power on wavelength division multiplexing (WDM) networks that carry huge quantities of information. InGaAs linear image sensors used in the OCM detect light spatially separated by spectral-dispersion elements.

Figure 6-4 Schematic of optical channel monitor



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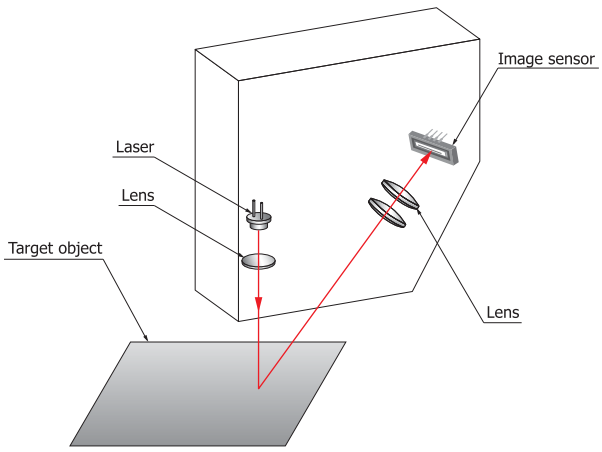
6 - 6 Displacement meters

Displacement meters measure the distance to a target object by using the triangulation principle. More specifically, they irradiate a laser beam onto the target object, and a CMOS linear image sensor captures the light reflecting from the target object. Using our lengthwise long CMOS linear image sensor in the light receiving section makes the optical design simple. Besides distance measurement, this displacement meter can be used to investigate irregularities on products such as tires and wafers.

Figure 6-5 Schematic of displacement meter



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