Design for NIL foundry using Wire Grid Polarizer volume production release methodologies on 200mm Full Wafer NIL

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In recent years, major advancements in NanoImprint Lithography (NIL) research and development have been demonstrated. However, moving NIL to volume manufacturing has been less obvious as improvements were needed in defect reduction, critical dimension uniformity (CDU) and stamp life to make a robust process [1]. To address these challenges, we will be offering a glimpse at the full wafer imprint process, fully released and utilized in 200mm wafer fabrication. Over 10,000 wafers have been processed in Moxtek's manufacturing line using an automated Substrate Conformal Imprint Lithography (SCIL) system with 94.2% up time [2]. Here, we present data producing Wire Grid Polarizer (WGP) as the baseline and related qualification methodology. We have shown stamp life well in to the 500 to 750 print ranges with some life time test up to 1300 prints (Table 1 and Figure 1). Quality control measures include critical dimension (CD) measures (Figure 2) and remaining breakthrough thickness monitored with statistical process control (SPC) along with WGP performance/yield assessments. As with all NIL processing, defect reduction is a constant focus and area for improvement.

The goal of this paper is to provide insight for the transition of optical products from design to volume NIL manufacturing in relation to WGP processing as highlighted above. New product development projects begin with master making, which is often a significant expense. Therefore, it is important to understand critical processing information related to making good masters, especially when many thousand duplicates of identical nano-structures are made. Keeping this in mind, a rough set of NIL design guidelines derived from WGP experience are listed in Table 2. This represents our best interpretation of experimental results from processing thousands of wafers.

The next step involves cycles of learning in stamp making and print optimization. Setting a process for making a good quality repeatable stamp for a new design can take at least a couple iterations. Then optimizing print involves stamp fill fraction related to resist spin coat thickness. Next is identifying and measuring the CD's of the intended structure. All of these are then incorporated in to a statistical process control methodology. Optical products can have vastly different performance measure methods requiring application specific metrology equipment. In this unique foundry situation, in house performance measure may not be possible. Therefore SPC monitoring of post print CD repeatability is critical for quality control. From this point either subsequent etch steps are optimized or imprinted wafers are delivered.

[1] Sreenivasan, S V. (2017). Nanoimprint lithography steppers for volume fabrication of leading-edge semiconductor integrated circuits. Microsystems & Nanoengineering. 3. micronano201775. 10.1038/micronano.2017.75.

[2] Verschuuren, Marc & Megens, Mischa & Ni, Yongfeng & van Sprang, Hans & Polman, Albert. (2017). Large area nanoimprint by substrate conformal imprint lithography (SCIL). Advanced Optical Technologies. 6. 243-264. 10.1515/aot-2017-0022.

Table 1. Stamp Life

Stamp ID	Pitch/CD (nm)	Failure Mode	Prints to Fail
B1.1	144/45	Release Force Limit	750
B1.2	144/45	Release Force Limit	500
L00-144	144/45	Release Force Limit	745
WGP14428	144/45	Release Force Limit	1300
WGP14430	144/45	Release Force Limit	611
NS1831-01	100/32	Damaged	652
NS1835-01	100/32	High Defects	501
NS1914-02	100/32	Damaged	285
NS196-01	100/32	Damaged	256

Figure 1. Performance Trend Chart for Stamp up to 745 Prints

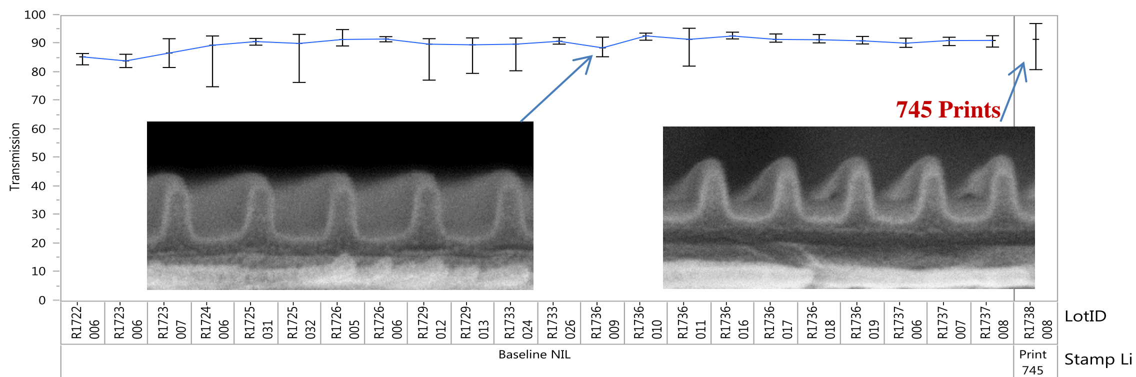

Figure 2. Initial CD Repeatability (2 Stamps, Same Master)

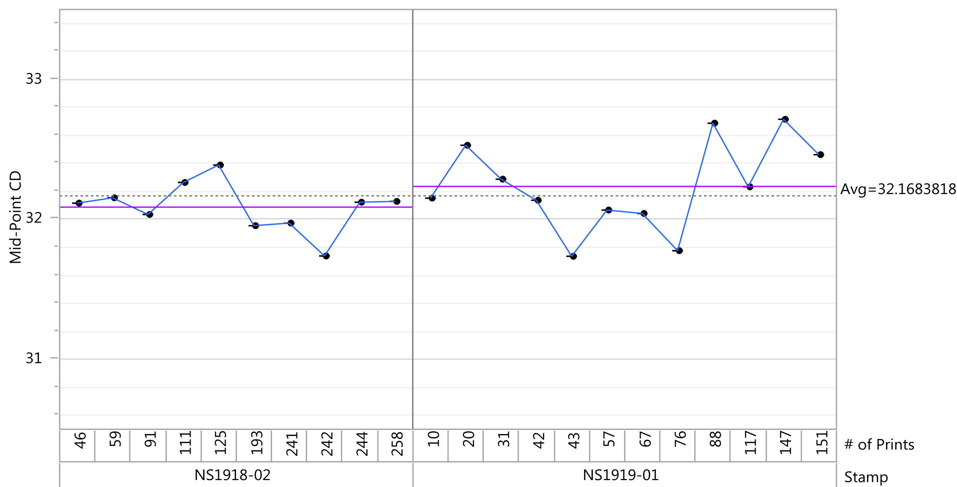

Table 2. NIL Foundry Design Guidelines (Proven Repeatable Processing)

Parameter	Guidance
Master Aspect Ratio	≤ 2 (CD Height/Width)
Minimum CD	30nm
Master Wafer Type	Silicon (Preferred)
Master Wafer Size	300mm, 200mm (Preferred) 150mm (Acceptable)
Master Release Surface Prep	In House (Preferred)
Breakthrough Remaining Thickness	≈ 25nm
Processing Substrates	200mm Glass or Silicon, 0.7mm to 1.8mm
Resist Mask	Oxide Based Sol Gel
Cut and Dice	Alignment Marks on Master