

Operation of 3- and 4-Terminal JFET

Application Note 1002

Introduction

Moxtek ultra-low noise JFETs are ideal for a variety of applications including microanalysis, Energy Dispersive X-ray Fluorescence (EDXRF), and X-ray Diffraction (XRD). Moxtek manufactures 3- and 4-pin n-channel JFETs. Moxtek ultra-low noise JFETs have low leakage current, low input capacitance (C_{gs}), and high transconductance (g_m). Each packaged JFET is tested and guaranteed.

A junction gate field-effect transistor (JFET) is the simplest type of field effect transistor. This device can be used as an electronically-controlled switch or as a voltage-controlled resistor.

In a JFET, current flows through a semiconducting channel between the “drain” terminal and the “source” terminal. Moxtek’s JFETs have n-type channels (there is an abundance of negative charge carriers—electrons). As the drain voltage increases relative to the source, the current through the channel increases.

Moxtek JFETs have a p-type gate. A depletion region exists between the channel and the gate (see Figure 1). This depletion region is essentially free of electrons. When a negative bias is applied to the gate, the size of depletion region increases and the width of the channel decreases. The larger the negative bias on the gate, the larger the depletion region and the narrower the channel. With a negative bias on the gate, current is unable to flow through the depletion region, so no current flows through the gate terminal. In practice, a very tiny “leakage current” does flow through the depletion region. Moxtek JFETs have very low leakage current (about 1 picoamp at room temperature).

Voltages applied to the gate and to the drain are commonly expressed with reference to the source. Hence, V_{ds} means the voltage applied to the drain relative to the source. Likewise, V_{gs} means the voltage applied to the gate relative to the source. The current flowing through the channel (between the drain and the source) is referred to as the “drain current” and is written I_d .

Channel Pinch-off

For a given drain voltage V_{ds} , the drain current I_d decreases as V_{gs} becomes more negative. At some voltage (known as the “pinch-off” or the “cutoff” voltage), the depletion region extends all the way through channel. As long as V_{ds} is small, the depletion region extends over the entire length of the channel and I_d becomes zero (see Figure 2).

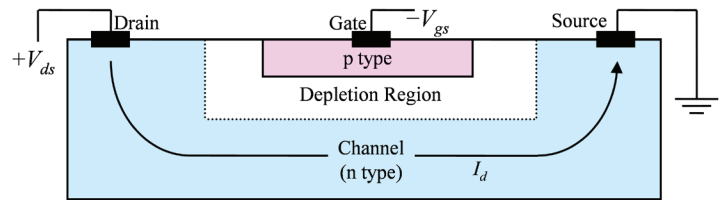
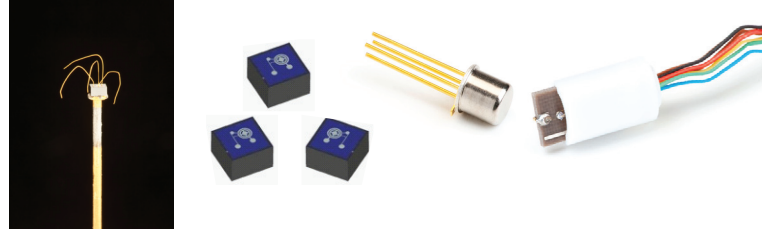


Figure 1: Operation of a 3-Terminal JFET

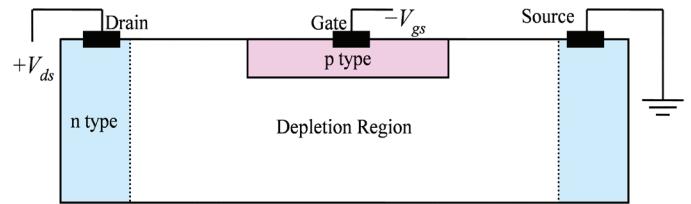


Figure 2: Channel Pinch-off

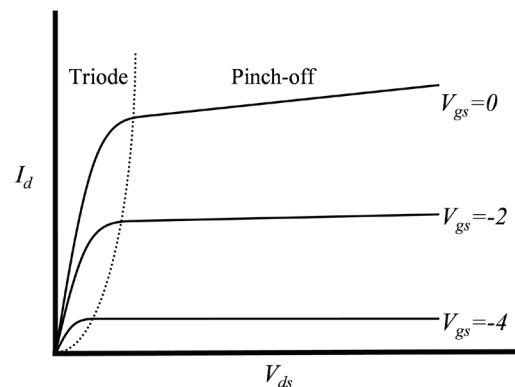


Figure 3: IV Curves for a 3-Terminal JFET

I-V Curves for a 3-Terminal JFET

For a given gate voltage V_{gs} , the drain current I_d increases quickly with drain voltage V_{ds} at first (see Figure 3). This is known as the “triode” region. Beyond a certain V_{ds} , I_d levels off and becomes almost constant. This is known as the “pinch-off” (or “active”) region. The drain current I_d in the pinch-off region when $V_{gs} = 0$ is the maximum possible drain current through the device, and is often referred to as the “drain saturation current” I_{dss} . This “leveling-off” occurs because the relative bias between the drain and the gate increases while the relative bias between the gate and the source remains small, causing the depletion region near the drain to extend farther into the channel than the depletion region near the source. Eventually, the channel pinches off near the drain end (see Figure 4). Unlike the small V_{ds} case discussed earlier (in which the entire channel disappears), there is still a non-depleted channel region near the source where current can flow. This current can drift through the small pinched-off region near the drain so that the current can still flow through the channel.

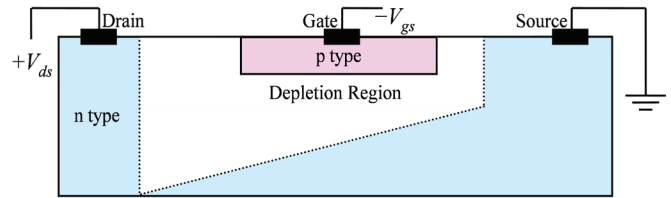


Figure 4: Entering the “Pinch-off” Region

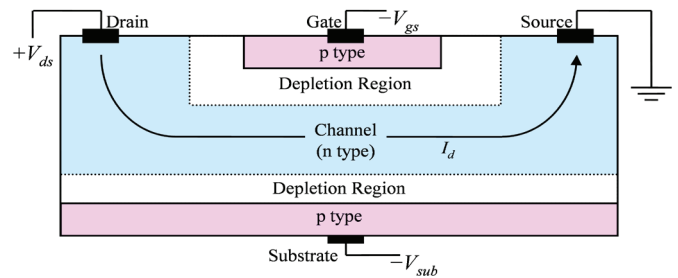


Figure 5: A 4-Terminal JFET

Advantages of a 4-Terminal JFET

Typically V_{ds} and I_d are fixed operating values which depend on the circuit in which the JFET is incorporated. In a 3-terminal JFET, V_{gs} must be adjusted for a given V_{ds} to obtain the desired I_d . Many applications are optimized when the gate bias is very small (nearly zero). For example, in an x-ray detector pre-amplifier, a maximum transconductance is desirable, and this condition occurs when V_{gs} is zero (or nearly zero). The 4-terminal device has two independently-biased gates (see Figure 5). The lower gate (substrate) can be adjusted to obtain the desired I_d and V_{ds} condition while the upper gate is maintained at a near-zero bias.

As the voltage applied to the substrate (V_{sub}) becomes increasingly negative, the drain current at a given V_{ds} and V_{gs} becomes smaller. The drain saturation current I_{dss} is adjustable in a 4-terminal device, the maximum drain current when $V_{gs} = 0$ is dependent upon the V_{sub} bias. The drain saturation current I_{dss} for a 4-terminal device is maximized when $V_{sub} = 0$ (see Figure 6).

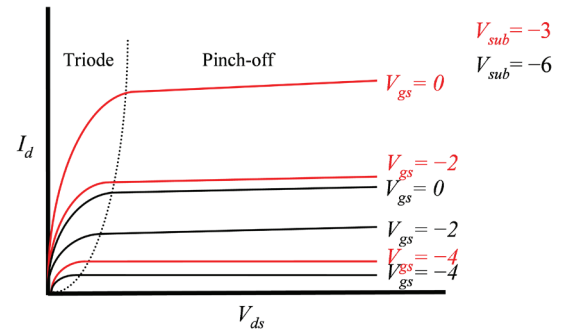


Figure 6: IV Curves for a 4-Terminal JFET

Circuit Symbols for 3-Terminal and 4-Terminal JFETs

The circuit symbol typically used for a 3-terminal JFET is shown in Figure 7a. Although the drain and source are technically interchangeable, the design of the device often favors a particular choice. The circuit symbol for a 4-terminal JFET is similar to that of a 3-terminal JFET, except that a second arrow is added to represent the voltage applied to the second gate (the substrate).

Moxtek JFETs

Moxtek JFETs are available as bare die and in a variety of standard and custom packages. For more information about standard JFET packages and performance please see the Moxtek data sheet. For price and delivery information please contact Moxtek.

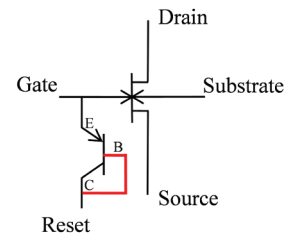


Figure 9: Current Flows Away From Gate During Reset Event