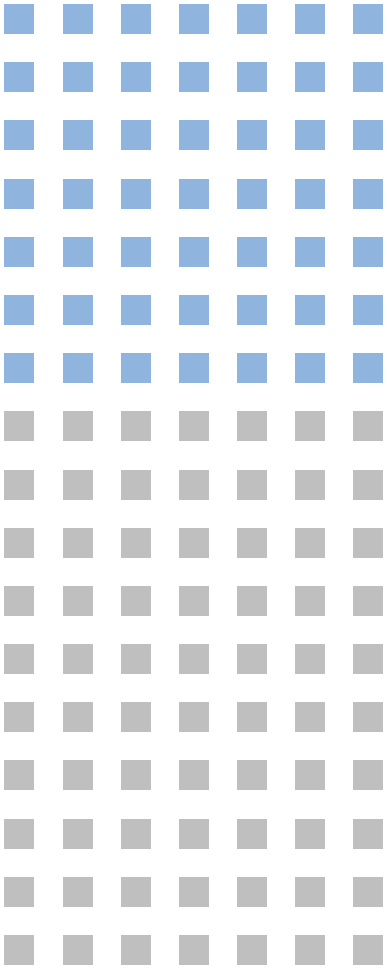
SOLID STATE DIVISION

TECHNICAL INFORMATION
SD-26

Characteristic and use of

NMOS linear image sensors



HAMAMATSU

Contents

Characteristic and use of NMOS linear image sensors

1. Introduction

The NMOS linear image sensor is a self-scanning photodiode array designed specifically for detectors used in multichannel spectroscopy. The NMOS linear image sensor offers a number of features, for example, a large photosensitive area, high UV sensitivity, stable performance against UV exposure, wide dynamic range due to low dark current and high saturation charge, superior output linearity and uniformity, and also low power consumption. In addition to standard types with a quartz window, devices with a fiber optic plate are available allowing efficient optical coupling to other imaging devices. Applications include not only spectroscopy but also a diverse range of image readout systems.

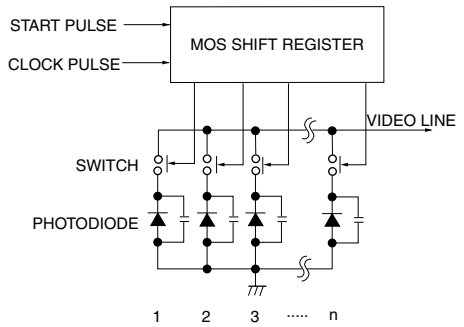
2. Structure and basic operation

This section explains the structure and operations of NMOS linear image sensors.

2-1. Structure

An NMOS linear image sensor, as shown in Figure 2-1, consists of a photosensitive section constructed with a photodiode array, a switch section that reads out the signal from the photodiode array, and a shift register that addresses these switches.

Figure 2-1 NMOS linear image sensor equivalent circuit



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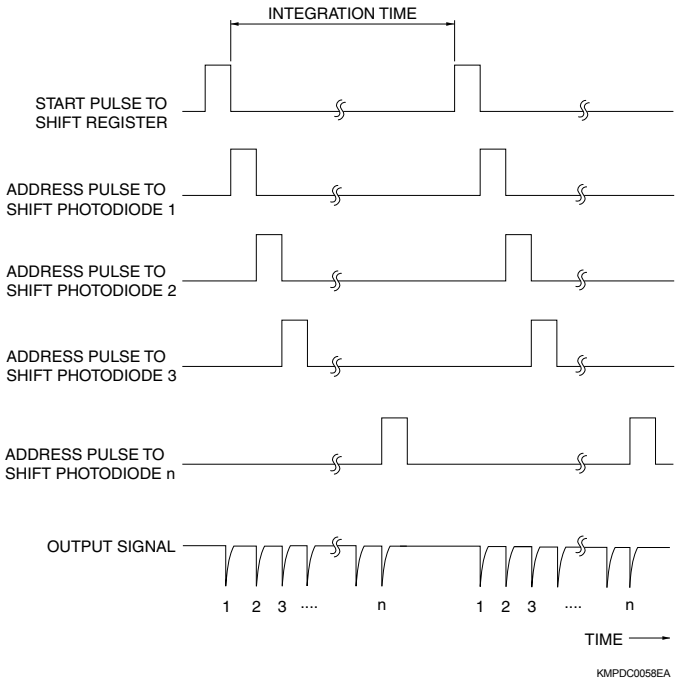
In contrast to the real-time signal readout method used for most photodiodes, the NMOS linear image sensor uses a charge integration method to read out the signal. In this method, an electrical charge generated by photoelectric conversion at the photodiode array is temporarily stored in the junction capacitance of each photodiode. The signal stored in each photodiode is read out through an output line (video line) by sequentially turning on the address switch connected to each photodiode at a delayed timing with respect to the preceding signal. The MOS shift register is used to produce the address pulses that turn on these switches. A typical output timing diagram is shown in Figure 2-2.

Figure 2-2 Output timing diagram



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2-2. Charge integration method

In the real-time readout method used for most photodiodes, the signal output is proportional only to the incident light intensity. In the charge integration method, however, the signal output is obtained in proportion to the product of light intensity and integration time, that is, the signal output is proportional to the amount of light exposure. This means that the signal output level can be increased by making the integration time longer, enabling low-light-level detection even with a photodiode with small photosensitive area.

In NMOS linear image sensor operation, the integration time of each photodiode is the time interval between when one switch is turned on for signal readout, and the time at which the same switch is turned on for the next readout. This is equal to the time interval between each start pulse signal for the MOS shift register. If the incident light level changes within this integration time, the change cannot be read out. Strictly speaking, the start time for integration does shift slightly because the switch for each photodiode is time-sequentially turned on as the signal is read out. Therefore, if the light level varies with time, the signal output from each photodiode does not become constant even though the entire image sensor is uniformly illuminated.

There is an upper limit on the output charge since the junction capacitance in which a signal charge is stored is finite. This is called the saturation charge above which the signal output will not increase with excessive light.

2-3. Signal readout by shift register

As stated above, NMOS linear image sensors use the charge integration method in which the signal from each photodiode is time-sequentially read out through one output line. It is not therefore necessary to connect an individual readout circuit to each photodiode. This means the external circuit configuration is made simple.

When an external start pulse is applied to the shift register while a two-phase clock pulse is being input, an address pulse is sequentially sent to turn on the address switch of the 1st channel photodiode and thus the signal stored in each photodiode is read out. If the next start pulse is introduced to the shift register before the signals of all channels are read out, then two address switches turn on at the same time, resulting in erroneous operation. Accordingly, the start pulse interval (integration time) must be set longer than the readout time required for all channels.

NMOS linear image sensors use a different readout method than for normal photodiodes. It is essential that the user understand these distinctions to make optimum settings to match operating conditions such as incident light level and integration time length.

3. Sensor types and operation

This section explains the types and configurations of Hamamatsu NMOS linear image sensors as well as their operating principles.

3-1. Types of NMOS linear image sensors

Hamamatsu NMOS linear image sensors are available in the following two readout methods.

1. Current output type S3901 to S3904 series, etc.
2. Voltage output type S3921 to S3924 series

The current output type offers superior linearity when used with an external signal readout circuit operating in the current integration mode, making it ideally suited for use in applications where high accuracy is particularly needed. The current output type also gives a high-speed readout when used with the current-to-voltage conversion method.

The voltage output type NMOS linear image sensors use the same output section as the current output type, but further in-

Table 3-1 Quick reference for Hamamatsu NMOS linear image sensors

Current output type

Type No.	Number of pixels	Pixel size (pixel pitch × height) (μm)	Active area [mm (H) × mm (V)]	Feature
S3901-128Q	128	50 × 2500	6.4 × 2.5	• Low power consumption • Superior output linearity • Wide dynamic range
S3901-256Q, F	256		12.8 × 2.5	
S3901-512Q, F	512		25.6 × 2.5	
S3904-256Q	256	25 × 2500	6.4 × 2.5	
S3904-512Q, F	512		12.8 × 2.5	
S3904-1024Q, F	1024		25.6 × 2.5	
S3902-128Q	128	50 × 500	6.4 × 0.5	
S3902-256Q	256		12.8 × 0.5	
S3902-512Q	512		25.6 × 0.5	
S3903-256Q	256	25 × 500	6.4 × 0.5	
S3903-512Q	512		12.8 × 0.5	
S3903-1024Q	1024		25.6 × 0.5	

Voltage output type

Type No.	Number of pixels	Pixel size (pixel pitch × height) (μm)	Active area [mm (H) × mm (V)]	Feature
S3921-128Q	128	50 × 2500	6.4 × 2.5	• Boxcar output waveform • Simple external readout circuit • Wide dynamic range
S3921-256Q	256		12.8 × 2.5	
S3921-512Q, F	512		25.6 × 2.5	
S3924-256Q	256	25 × 2500	6.4 × 2.5	
S3924-512Q, F	512		12.8 × 2.5	
S3924-1024Q	1024		25.6 × 2.5	
S3922-128Q	128	50 × 500	6.4 × 0.5	
S3922-256Q	256		12.8 × 0.5	
S3922-512Q	512		25.6 × 0.5	
S3923-256Q	256	25 × 500	6.4 × 0.5	
S3923-512Q	512		12.8 × 0.5	
S3923-1024Q	1024		25.6 × 0.5	

clude a signal processing circuit that consists of a current integration circuit utilizing video line capacitance and an impedance conversion circuit. Although the linearity accuracy is slightly lower than the current output type operated in the current integration mode, the voltage output type can internally produce a low-impedance output signal with boxcar waveform. This allows signal readout with a simple external circuit.

Table 3-1 gives the major product line of Hamamatsu NMOS linear image sensors. Suffix “Q” of the type number means the image sensors have a quartz window, while suffix “F” indicates a fiber optic plate is used. The quartz window types ensure high sensitivity in the UV range and also provide stable operation for dark current and sensitivity performance even after extended periods of UV exposure. Image sensors having a fiber optic plate can be easily fiber-coupled to another optical element such as an image intensifier. For detection of X-rays from 10 keV to 100 keV, semi-custom devices (“FX” type) having a phosphor-coated fiber optic plate are also available in each family of current output and voltage output type NMOS linear image sensors. Furthermore, S8380/S8381 series devices with enhanced near infrared sensitivity are provided.

3-2. Current output type NMOS linear image sensors

3-2-1. Configurations

The current output type NMOS linear image sensor consists of a photosensitive section, readout switch section and shift register, integrated into a single chip. In addition, dummy photodiodes and anti-blooming switches are formed on the same chip. Figure 3-1 shows the equivalent circuit for the current output type and Figure 3-2 shows the pinout configurations. The pin designations and their functions are listed in Table 3-2.

Figure 3-1 Equivalent circuit (current output type)

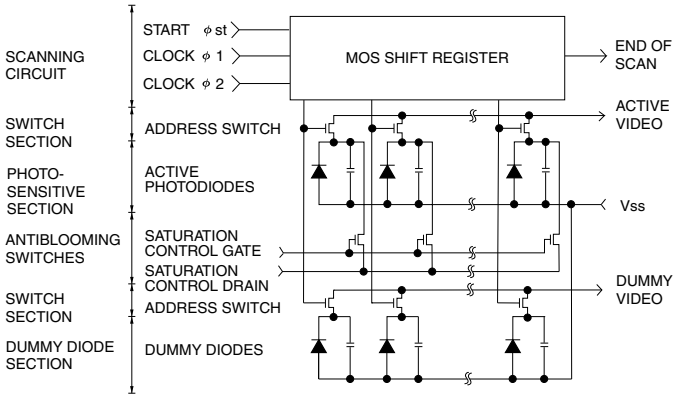

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Figure 3-2 Pinout (current output type)

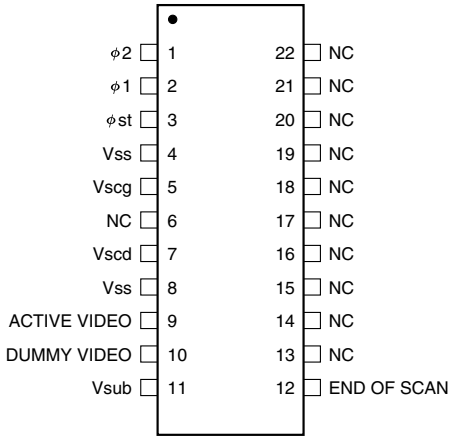

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Table 3-2 Pin description (current output type)

Terminal		Function
Input	φ1	Clock pulse 1
	φ2	Clock pulse 2
	φst	Start pulse
	Vscd	Saturation control drain
	Vscg	Saturation control gate
Ground	Vss	Ground (anode potential)
	Vsub	Substrate potential
	NC	No connection
Output	Active video	Signal output
	Dummy video	Switching noise output
	EOS	End of scan

1) Shift register

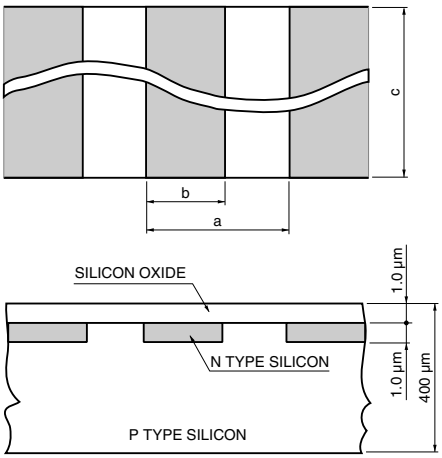
The shift register is comprised of N-channel MOS transistors. Pins φ1, φ2 and φst in Figure 3-2 are input pulse terminals used to operate the shift register. When an external start pulse φst is supplied to the shift register with the two-phase clock pulse φ1 and φ2 being applied, the shift register begins operation and generates a train of address pulses to sequentially turn on the address switch beginning with the 1st channel. The shift register is designed for low power consumption to minimize temperature rise in the sensor elements. When one scan for all pixels is completed, an end-of-scan (EOS) pulse is output at a timing immediately after the last pixel is readout.

(2) Photosensitive section

The photosensitive section is constructed with P-N junction photodiodes consisting of an N-type diffusion layer formed on a P-type silicon substrate. This section serves as a photoelectric converter that transforms light signals into electrical signals, and also temporarily stores the signal charge obtained. Pin Vss is connected to the anode (P-type silicon) of each photodiode.

The photodiode is designed and processed to provide high UV sensitivity yet low dark current. The structure of the photosensitive section is shown in Figure 3-3, in which “a” is the photodiode pitch, “b” is the width of the photodiode diffusion layer and “c” is the photodiode height.

Figure 3-3 Active area structure (current output type)



S3901 SERIES: a=50 µm b=45 µm c=2.5 mm
S3904 SERIES: a=25 µm b=20 µm c=2.5 mm
S3902 SERIES: a=50 µm b=45 µm c=0.5 mm
S3903 SERIES: a=25 µm b=20 µm c=0.5 mm

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(3) Dummy photodiode

Dummy photodiodes generate a spike noise signal used for external cancellation of spike noise in the current-to-voltage conversion readout method. These photodiodes are shielded with aluminum so that they are impervious to light.

(4) Readout switch

The readout switch section consists of an address switch array made up of N-channel MOS transistors, with the source of each transistor connected to the cathode of a photodiode or dummy photodiode while the drain and gate are connected respectively, to the video line and address pulse input. Each photodiode in the photosensitive section is connected to the video line via the individual address switch. When an address pulse is applied from the shift register, the two address switches turn on at the same time, and the output signal including spike noise is derived from the active video line, while the spike noise signal is output from the dummy video line. When the image sensor is operated in the current-to-voltage conversion method, the output signal can be obtained with low spike noise, by performing external differential amplification of each signal from the two video lines. The spike noise appears via floating capacitance between the gate and drain of each address switch at the time that the address pulse is introduced.

(5) Anti-blooming switch

The anti-blooming switch section comprises a switch array constructed with N-channel MOS transistors, with the source of each transistor connected to the cathode of a photodiode while the drain and gate are connected respectively, to the saturation control drain Vscd and saturation control gate Vscg.

When a light higher than the saturation exposure enters a photodiode, the photodiode cannot store a signal charge in excess of the saturation charge. Without saturation control, this causes the excess signal charge to overflow and diffuse into the adjacent photodiodes and the video line, resulting in deterioration of signal purity, so-called “blooming”.

An anti-blooming switch is provided in Hamamatsu NMOS linear image sensors for each photodiode separately from the normal signal output line connected to the video line, in order to allow the excess charge to bleed off.

3-2-2. Operating principle of current output type

Figure 3-4 shows the structure of one pixel comprised of a photodiode and a readout switch, and Figure 3-5 shows its equivalent circuit. Specific operations are described below.

Figure 3-4 Readout section structure

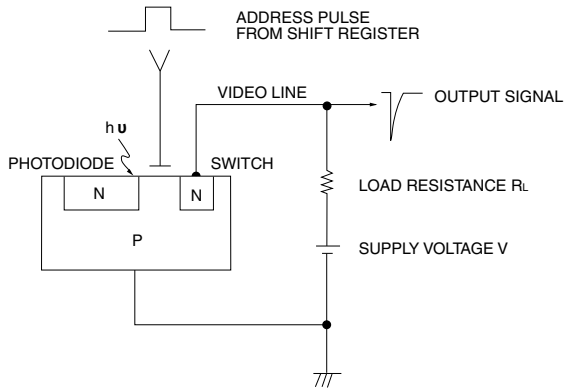

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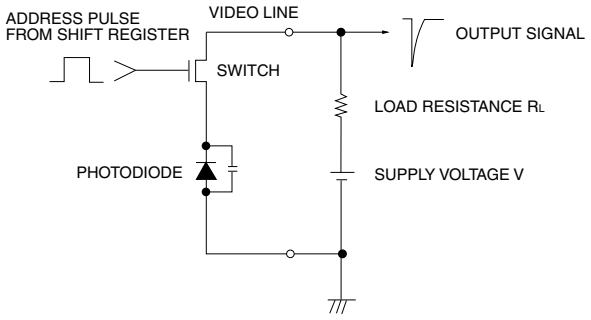
Figure 3-5 Equivalent circuit of current-to-voltage conversion method



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The photodiode is a P-N junction photodiode consisting of an N-type diffusion area formed on a P-type silicon substrate. The readout switch consists of an N-channel MOS transistor, with its source connected to the cathode of a photodiode while the drain and gate are respectively connected to the video line and the address pulse input part from the shift register. The photodiode anode (silicon substrate) is connected to GND, and the video line is biased at the positive potential Vb.

When an address pulse from the shift register is input to the gate of the readout switch, the switch turns on. As a result, the photodiode cathode sets to the same potential as that of the video line and the photodiode is initialized and reverse-biased. Thus the photodiode junction capacitance Cj is fed with a charge, Qj=Cj

× Vb, from the power supply. When the readout switch is off (open circuit) and the signal charge begins to accumulate, the charge stored in the photodiode junction capacitance Cj is discharged when the charge generated by light (photocurrent) occurs. As shown in Figure 3-6, the slope of the potential across the photodiode is a function of incident light. That is, the greater the light intensity the more electron-hole pairs are created and the faster the charge accumulates on Cj. Therefore photodiode potential approaches GND potential. The amount of this discharge increases in proportion to the incident light level, but the maximum amount is limited by the amount of charge initially stored. This corresponds to the saturation charge.
When an address pulse from the shift register is then input and the readout switch turns on, a charge equal to that discharged during the integration time is fed from the power supply through the load resistance RL, so that the photodiode is initialized again. At this point, a potential difference resulting from the charge current is developed across the load resistor RL, and is detected as an output voltage. This output has a differential waveform with a negative polarity with respect to the video line bias voltage Vb. This signal readout method is known as the current-to-voltage conversion and its simplified operating diagram is shown in Figure 3-6. In some cases, a feedback circuit using an operational amplifier is used, as shown in Figure 3-7.

Figure 3-6 Operation of current-to-voltage conversion method

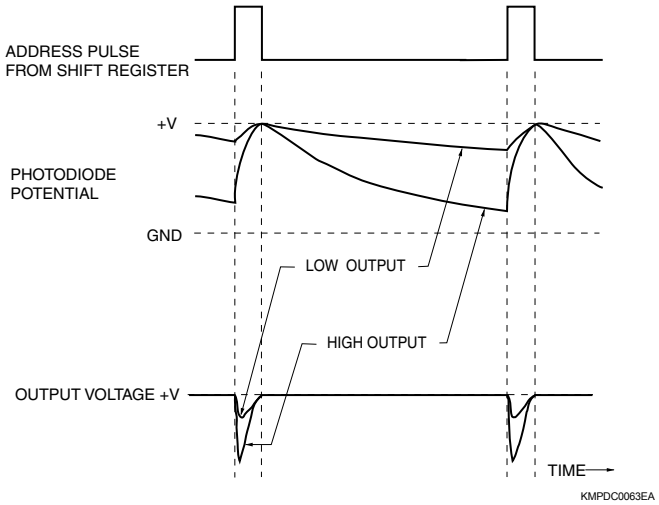
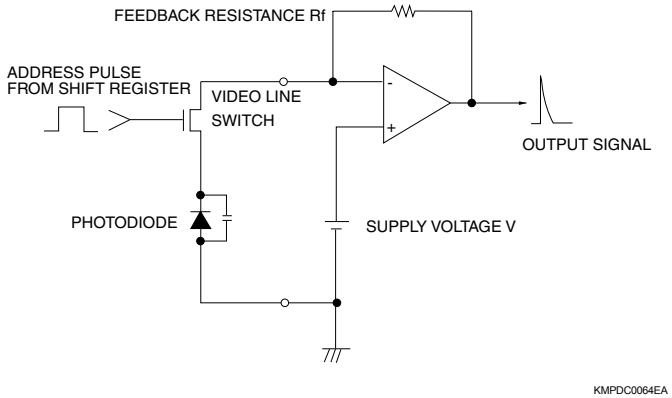


Figure 3-7 Equivalent circuit of current-to-voltage conversion method using op-amp



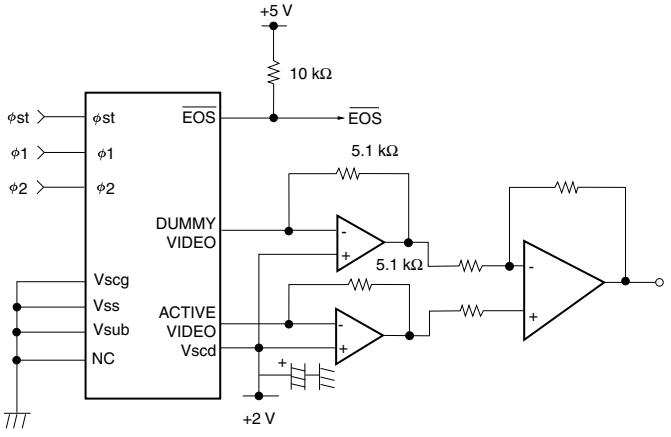
In actual operation, the charge current gradually discharges due to the re-combination current in the depletion layer and the surface leakage current as well as the photocurrent described above. These currents which are unrelated to the illumination of light are referred to as the dark current and its output is called the dark output. (See section 4-5.)

3-2-3. Readout method for the current output types

(1) Current-to-voltage conversion method

The previous section described signal readout operating principle, using current-to-voltage conversion as one example of light detection. In this method, the peak value of a differential output waveform is read out as a signal output. However, the output waveform taken at low output will not be identical pulse shape to that taken at a high output. The lower the amplitude of the output, the longer the time required to reach peak value. As a result, the ratio of peak value to the area of the differential waveform decreases. Since the amount of charge to be read out corresponds to the differential waveform area, when measuring the input/output characteristics by the current-to-voltage conversion method, its slope at low output is larger than that at high output. For this reason, this signal readout method is not suited for light detection where high accuracy at low output levels is required. This method does however offer the advantages of high-speed readout and simplified circuitry.
Figure 3-8 shows a recommended readout circuit. In order to eliminate spike noise, after performing current-to-voltage conversion, this circuit extracts the differential output between signals from the video line and dummy video line.

Figure 3-8 Recommended readout circuit for current-to-voltage conversion method



(2) Current integration method

There is another signal readout method in which the charged current is integrated in an external circuit to measure the amount of charge. This method enables high-precision signal detection even at low output levels. Figure 3-9 shows a typical current-integration circuit diagram using a charge amplifier. In this circuit, the feedback capacitance Cf in the charge amplifier is discharged by applying an external reset pulse immediately before the readout switch turns on. When the readout switch

has turned on, a charge which corresponds to the discharge during the integration time is supplied to the photodiode junction capacitance from the power supply, so that the photodiode is initialized. At the same time, the feedback capacitance Cf is also charged by this current. This, allows an integration waveform with positive polarity to be derived from the output terminal of the integration circuit. This output voltage Vout is proportional to the amount of charge Q, and expressed as Vout=Q/Cf. The output is a boxcar waveform, which facilitates signal processing. However, since this output waveform response is determined by the discharge time constant of the feedback capacitance Cf, the maximum readout frequency will be around 100 kHz.

Figure 3-10 shows a recommended readout circuit. For an evaluation circuit using this method, Hamamatsu provides C7884 series driver circuits. C7884 series includes a clamping circuit connected to the latter stage in order to reduce random noise components.

Figure 3-9 Equivalent circuit of current-integration circuit using a charge amplifier

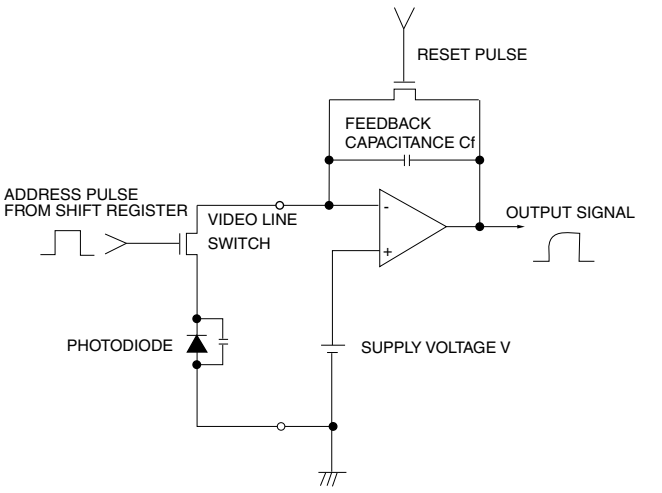
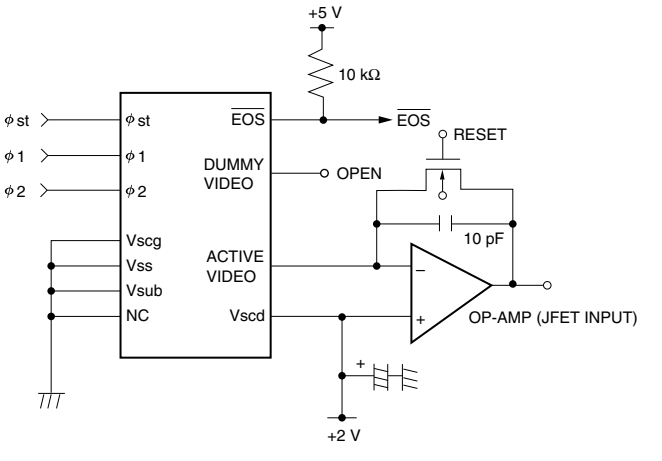


Figure 3-10 Recommended readout circuit for current integration method



3-2-4. Terminal voltage for current output types

The recommended terminal voltage for a current output type NMOS linear image sensor is listed in Table 3-3.

The two-phase clock pulses $\phi 1$ and $\phi 2$ have positive polarity. Their recommended amplitude voltage $V\phi$ is 5 V, with a minimum of 4.5 V and a maximum of 10 V. The start pulse ϕst also has positive polarity and its amplitude voltage $V\phi st$ should be equal to the clock pulse voltage $V\phi$. No DC voltage is required for driving the shift register. The Vss, Vsub and NC terminals should be all grounded.

As explained in section 3-2-2, a positive bias voltage Vb should be applied to the video line. This corresponds to the voltage applied to the non-inverting input terminal of the operational amplifier in the current-to-voltage conversion or current integration method. The recommended voltage for Vb is the clock pulse voltage minus 3 V. For example, Vb should be 2 V when $V\phi$ is 5 V. The maximum voltage for Vb is $V\phi$-2.5 V and the minimum voltage is 1.5 V.

The settable voltage range for Vb with respect to $V\phi$ is shown in Figure 3-11. Using a higher voltage for $V\phi$ widens the settable range for Vb. When Vb is set higher, the saturation charge will increase accordingly. This is accompanied by an increase in the dark current, which is however smaller than the increase in saturation charge. Conversely, when Vb is set to a lower value, the output waveform response is faster. These tendencies are shown in Figures 3-12 and 3-13. Figure 3-12 shows the characteristic dependence of the saturation charge and dark output on Vb, measured when $V\phi$ is set to 10 V and normalized for the value at Vb=2 V. Figure 3-13 shows how Vb affects the time required for a differential waveform to reach the peak after input of a clock pulse, which is measured when S3901-512Q is driven with $V\phi$ of 5 V and 10 V by the current-to-voltage conversion method. These facts indicate that the clock pulse voltage $V\phi$ and video bias voltage Vb should be set to their optimum values depending on the ambient operating conditions.

It is recommended that the saturation control drain voltage Vscd, be the same value as for the video bias line voltage Vb. The saturation control gate Vscg should be grounded. When incident light intensity is so high that blooming occurs even with this setting, then setting Vcg at positive potential will enhance the blooming suppression effect. But note that the saturation charge lowers at the same time. This relation between the saturation control gate voltage Vscg and the saturation output charge is shown in Figure 3-14.

The end-of-scan signal is available as a negative polarity signal with respect to 5 V by connecting a 10 kΩ pull-up resistor to the EOS terminal, at $\phi 2$ timing immediately after the last pixel output is derived.

Table 3-3 Recommended terminal voltage (current output type)

Input voltage		Symbol	Min.	Typ.	Max.	Unit
Clock pulse voltage	High	Vϕ1, Vϕ2 (H)	4.5	5	10	V
	Low	Vϕ1, Vϕ2 (L)	0	-	0.4	
Start pulse voltage	High	Vϕst (H)	4.5	Vϕ	10	
	Low	Vϕst (L)	0	-	0.4	
Video bias voltage		Vb	1.5	Vϕ-3.0	Vϕ-2.5	
Saturation control drain voltage		Vscd	-	Vb	-	
Saturation control gate voltage		Vscg	-	0	-	

Figure 3-11 Video bias voltage margin (current output type)

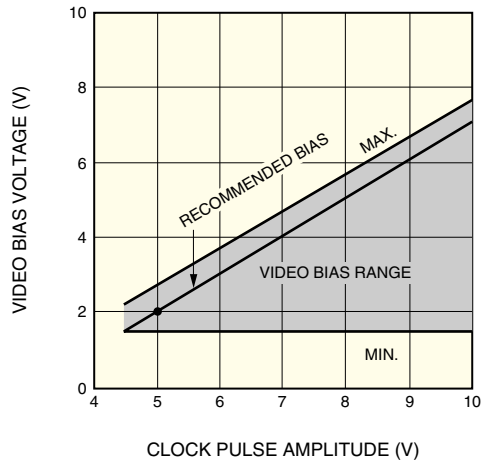


Figure 3-12 Saturated charge and dark output vs. video bias

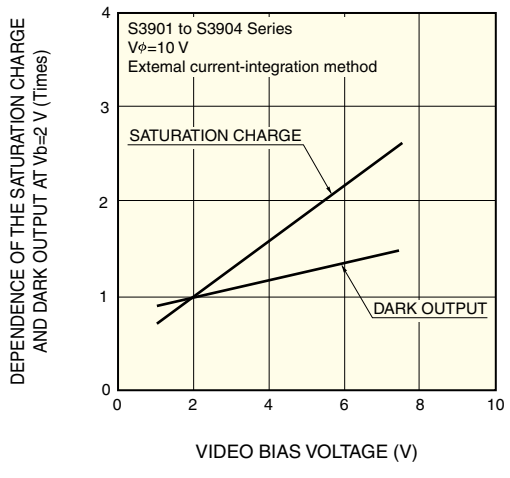


Figure 3-13 Output response time vs. video bias voltage

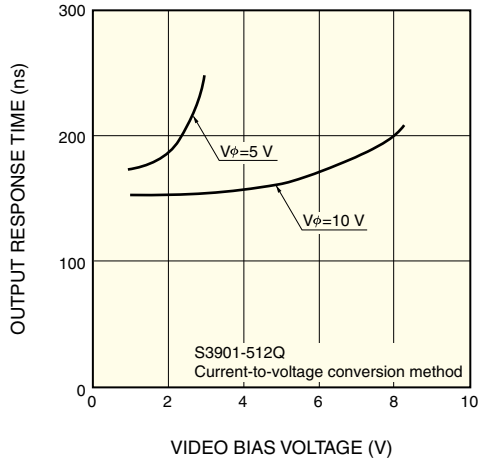
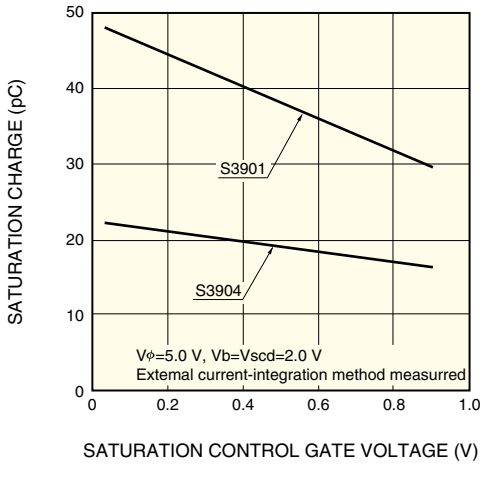


Figure 3-14 Saturated charge vs. saturation control gate



3-2-5. Input/output pulse timing for current output type

Figure 3-15 shows the input/output pulse timing diagram for a current output type image sensor. The clock and waveform conditions are listed in Tables 3-4 and 3-5, respectively.

The two-phase clock pulses ϕ1 and ϕ2 can be either in a completely separate or complementary relation. However, do not allow both pulses to turn "High" at the same time.

If the rise time and fall time of ϕ1 and ϕ2 are longer than 20 ns, insert clock spaces X1 and X2 which are longer than "rise time/fall time - 20" (ns). The pulse width of ϕ1 and ϕ2 requires at least 200 ns for stable operation of the shift register. Since the video output signal is obtained at each rising edge of ϕ2, the clock pulse frequency equals the signal readout frequency (data rate).

The start pulse ϕst has the same amplitude as ϕ1 and ϕ2. The shift register starts operating when the start pulse ϕst sets to "High" level, so the ϕst pulse interval determines the signal integration time. As with two-phase clock pulses, the start pulse also requires a pulse width of at least 200 ns, and must overlap with ϕ2 for at least 200 ns. Furthermore, ϕ2 must be changed only once from "High" to "Low" level during the "High" level of ϕst, in order to initiate correct shift register operation.

The photodiode potential of a current output type NMOS linear image sensor is reset within the readout period in which the address switch is turned on. This means that if the pulse width of ϕ2 synchronized with the address pulse is too short, a lag phenomenon may occur. Because ϕ1 is used only for scanning operation, it has advantageous characteristics in that the pulse width of ϕ2 can be set longer than that of ϕ1. However, the duty ratio of ϕ1 and ϕ2 should be set to 1:1 when the image sensor is operated in the high-speed readout mode at 1 MHz or higher.

Table 3-4 Clock characteristics (current output type)

Parameter			Symbol	Min.	Typ.	Max.	Unit
Operating frequency (Vb=2 V, Vϕ=5 V)			f	0.1	-	2000	kHz
Clock pulse line capacitance (at 5 V bias)	S3901 S3902	-128Q	Cϕ	-	21	-	pF
		-256Q		-	36	-	
		-512Q		-	67	-	
	S3903 S3904	-256Q		-	27	-	pF
		-512Q		-	50	-	
		-1024Q		-	100	-	
Saturation control gate capacitance (at 5 V bias)	S3901 S3902	-128Q	Cscg	-	12	-	pF
		-256Q		-	20	-	
		-512Q		-	35	-	
	S3903 S3904	-256Q		-	14	-	pF
		-512Q		-	24	-	
		-1024Q		-	45	-	
Video line capacitance (at 2 V bias)	S3901 S3902	-128Q	Cv	-	7	-	pF
		-256Q		-	11	-	
		-512Q		-	20	-	
	S3903 S3904	-256Q		-	10	-	pF
		-512Q		-	16	-	
		-1024Q		-	30	-	

Table 3-5 Pulse waveform conditions (current output type)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Start pulse rise time / fall time		trϕs, tfϕs	-	20	-	ns
Start pulse width		tpws	200	-	-	
Clock pulse rise time / fall time		trϕ1, trϕ2 tfϕ1, tfϕ2	-	20	-	
Clock pulse width		tpwϕ1, tpwϕ2	200	-	-	
Start pulse to clock pulse 2 overlap time		tϕov	200	-	-	
Clock pulse space		X1, X2	trf - 20	-	-	
Video delay time (50 % of saturation) Vb = 2 V, Vϕ = 5 V	S3901-128Q	tvd	-	80	-	
	S3901-256Q		-	120	-	
	S3901-512Q		-	160	-	
	S3902-128Q		-	70	-	
	S3902-256Q		-	110	-	
	S3902-512Q		-	140	-	
	S3903-256Q		-	80	-	
	S3903-512Q		-	120	-	
	S3903-1024Q		-	160	-	
	S3904-256Q		-	100	-	
	S3904-512Q		-	150	-	
	S3904-1024Q		-	200	-	

When the signal from a current output type image sensor is read out with an external current integration circuit, a reset pulse ϕreset is required in addition to the above clock pulses in order to reset the integration capacitance. However, it is possible to share the ϕ1 and ϕreset by using a timing pulse as shown in Figure 3-16, without impairing the above pulse conditions. To maintain a constant photodiode reset potential, the rise of ϕreset must be separated from the fall of ϕ2 for at least 50 ns. In this case, it is also essential that the photodiode potential reset time and readout time have the pulse width of ϕ2 set longer than that of ϕ1. Note however, if the ϕreset pulse width is too short, the integration capacitance does not completely reset and conversely, a lag resulting from the external circuit will occur.

Figure 3-15 Pulse timing diagram (current output type)

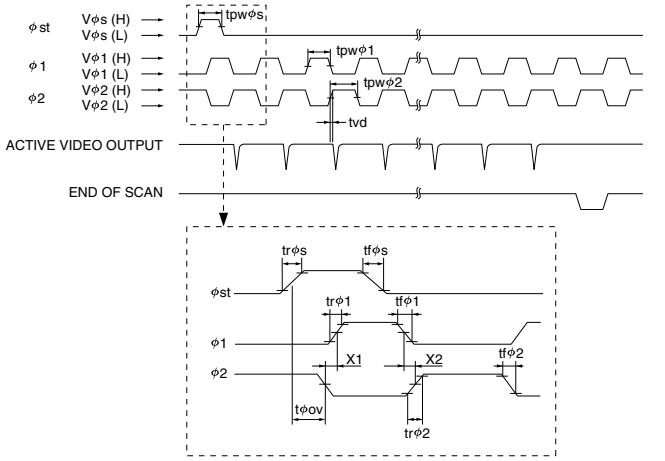


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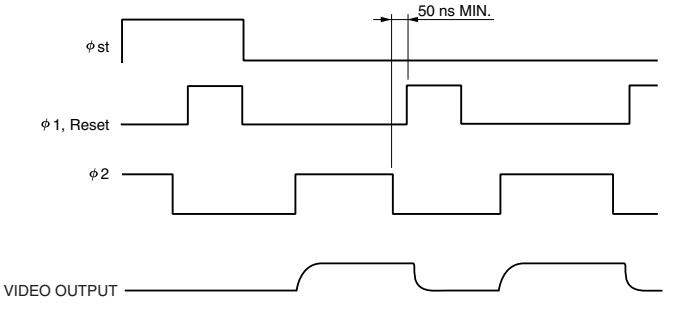
Figure 3-16 Pulse timing example for external current-integration method



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3-3. Voltage output type NMOS linear image sensors

3-3-1. Configurations of the voltage output types

The voltage output type NMOS linear image sensor consists of a photosensitive section, readout switch section, shift register and output signal processing section, all integrated into a single chip. This type of image sensor provides an output with boxcar waveform. Figure 3-17 shows the equivalent circuit of the voltage output type. Figures 3-18 and 3-19 respectively show the structure of the photosensitive section and the pinout configurations. The pin designations and their functions are listed in Table 3-6.

The structure and configurations are identical to the current output type except for the output signal processing section. The pin designations for the input/output terminals such as ϕst, ϕ1, ϕ2, Vscd, Vscg, Vss, Vsub, NC and EOS, and their functions are exactly the same for the current output type. The Vdd and Reset V terminals are for voltage input to the output signal circuit, and Resetϕ is a pulse input terminal. The output signal processing section consists of a switching transistor array for reset connected to the video line and a source follower circuit for impedance conversion. Both are comprised of N-channel MOS transistors. The Vscd and Reset V terminals are common since they are internally connected in the chip.

Figure 3-17 Equivalent circuit (voltage output type)

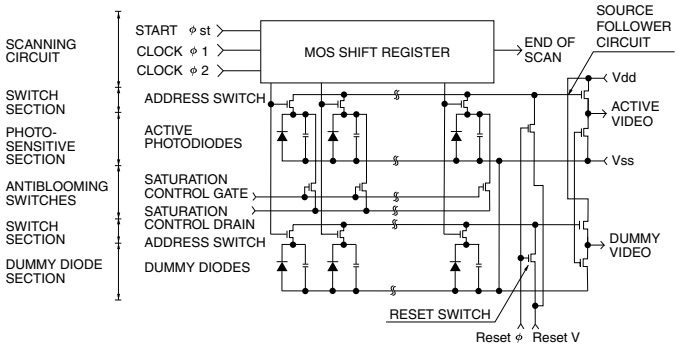

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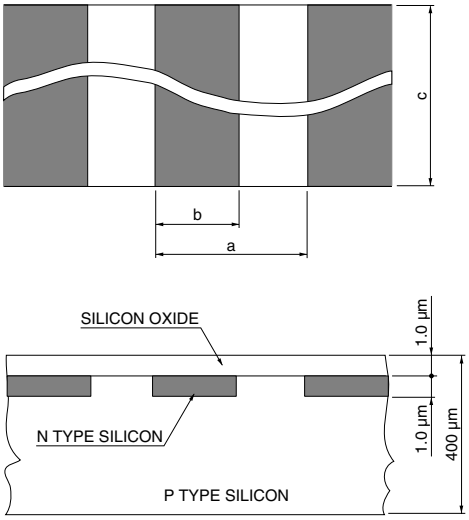
Figure 3-18 Active area structure (voltage output type)



S3921 SERIES: a=50 µm b=45 µm c=2.5 mm
S3924 SERIES: a=25 µm b=20 µm c=2.5 mm
S3922 SERIES: a=50 µm b=45 µm c=0.5 mm
S3923 SERIES: a=25 µm b=20 µm c=0.5 mm

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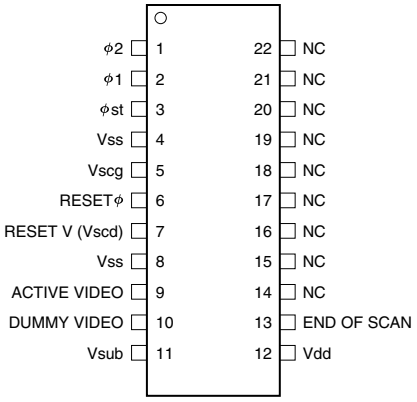
Figure 3-19 Pinout (voltage output type)



Vss, Vsub and NC should be grounded.

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Table 3-6 Pin description (voltage output type)

Terminal		Function
Input	ϕ1	Clock pulse 1
	ϕ2	Clock pulse 2
	ϕst	Start pulse
	Vscd	Saturation control drain
	Vscg	Saturation control gate
	Reset V	Reset voltage
	Reset ϕ	Reset pulse
	Vdd	Source follower drain voltage
Ground	Vss	Ground (anode potential)
	Vsub	Substrate potential
	NC	No connection
Output	Active video	Signal output
	Dummy video	Switching noise output
	EOS	End of scan

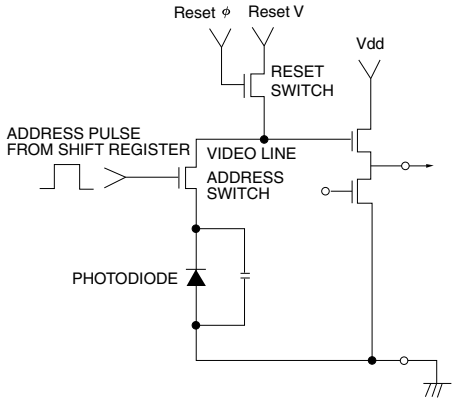
3-3-2. Operating principle of the voltage output types

Figures 3-20 shows the structure of one pixel comprised of a photodiode, a readout switch, and its equivalent circuit. This section describes specific readout operations using these figures.

When the address and reset switches simultaneously turn on at a certain time, the video line and photodiode potential are initialized. This reset switch consists of an MOS transistor, with its source connected to the Reset V terminal, its gate to the Resetϕ terminal and the drain to the video line. Each time an output signal from one pixel is read out, a reset pulse is input to the Resetϕ terminal so that the video line and photodiode potentials are initialized to the reset voltage Vr which is applied to the Reset V terminal. Both the address and reset switches then turn off, and the stored charge in the photodiode is discharged from the light output and dark output during the integration time. Next, when only the address switch turns on, charge redistribution occurs by capacitive dividing between the video line and photodiode. This supplies a charge into the photodiode from the video line until the photodiode and video line potentials are equalized. This change in the video line potential is input to the gate of the source follower circuit, causing a change in the current flowing through the transistor used as a load. As a result, a voltage signal is read out from the output terminal. After this, the reset switch turns on while the address switch stays on, and the video line and photodiode potentials are again initialized.

This readout method is referred to as video line integration since it uses the video line capacitance. The dummy video line operates in the same manner. A constant voltage is applied, inside the chip, to the gate of the transistor used as a load. The output is available in negative polarity with respect to a certain constant voltage (approx. 1.5 V) which is determined by the source follower circuit characteristics and the reset voltage.

Figure 3-20 Readout section structure



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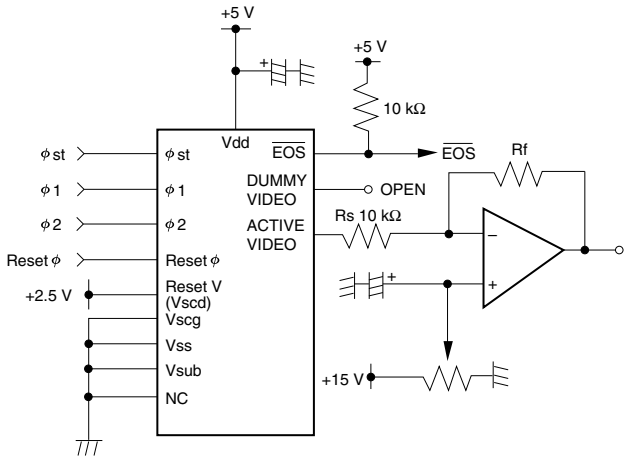
3-3-3. Readout method for the voltage output types

The voltage output type provides an output signal with boxcar waveform of negative polarity with respect to the positive potential, so an external circuit is used to perform inverting amplification and offset cancellation.

A recommended readout circuit is shown in Figure 3-21. The gain of this circuit is Rf/Rs. To prevent loading of the internal source follower a resistor of 10 kΩ or more should be used. Offset cancellation is performed by adjusting the variable resistor on the non-inverting input side of the operational amplifier.

Figure 3-21 Recommended readout circuit (voltage output type)



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3-3-4. Terminal voltage for the voltage output types

The recommended terminal voltage for a voltage output type NMOS linear image sensor is listed in Table 3-7.

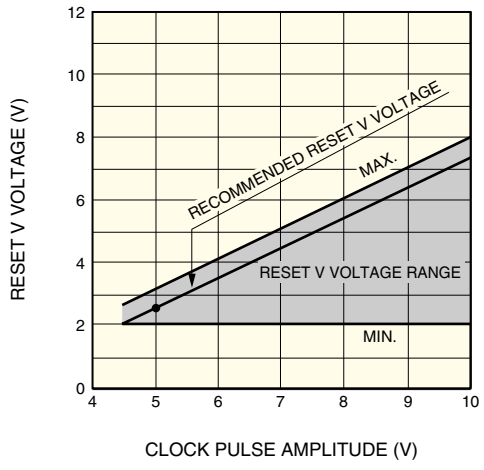
Table 3-7 Recommended terminal voltage (voltage output type)

Input voltage		Symbol	Min.	Typ.	Max.	Unit
Clock pulse voltage	High	Vϕ1, Vϕ2(H)	4.5	5	10	V
	Low	Vϕ1, Vϕ2(L)	0	-	0.4	
Start pulse voltage	High	Vϕst(H)	4.5	Vϕ	10	
	Low	Vϕst(L)	0	-	0.4	
Reset pulse voltage	High	Vrϕ (H)	4.5	Vϕ	10	
	Low	Vrϕ (L)	0	-	0.4	
Source follow drain voltage		Vdd	4.5	Vϕ	10	
Reset voltage		Vr	2.0	Vϕ-2.5	Vϕ-2.0	
Saturation control drain voltage		Vscd	-	Vb	-	
Saturation control gate voltage		Vscg	-	0	-	

As with the current output type, the recommended amplitude voltage of ϕ1 and ϕ2, Vϕ1 and Vϕ2 is 5 V, with a maximum value of 10 V and a minimum value of 4.5 V. The amplitude voltage of ϕst and Vϕst should be equal to the clock pulse voltage Vϕ. The Vss, Vsub and NC terminals should all be grounded.

Each photodiode of voltage output type image sensors is initialized via the reset switch connected to the Reset V terminal voltage Vr. This voltage corresponds to the video bias Vb for the current output type. The recommended reset voltage Vr for voltage output type equals a value obtained by subtracting 2.5 V from the clock pulse voltage Vϕ. For example, Vr should be 2.5 V when Vϕ is 5 V. The maximum voltage for Vr is Vϕ-2.5 V and the minimum voltage is 2 V. The settable voltage range for Vr with respect to Vϕ is shown in Figure 3-22. As with the current output type, using a higher voltage for Vϕ widens the settable range for Vr. When Vr is set higher, the saturation charge will increase accordingly. Conversely, when Vr is set to a lower value, the output response is faster. These facts indicate that the clock pulse voltage Vϕ and reset voltage Vr should be set to their optimum values depending upon the ambient operating conditions. The reset pulse should be CMOS compatible with positive polarity and its amplitude voltage Vrϕ should be equal to the clock pulse voltage Vϕ.

Figure 3-22 Reset voltage margin (voltage output type)



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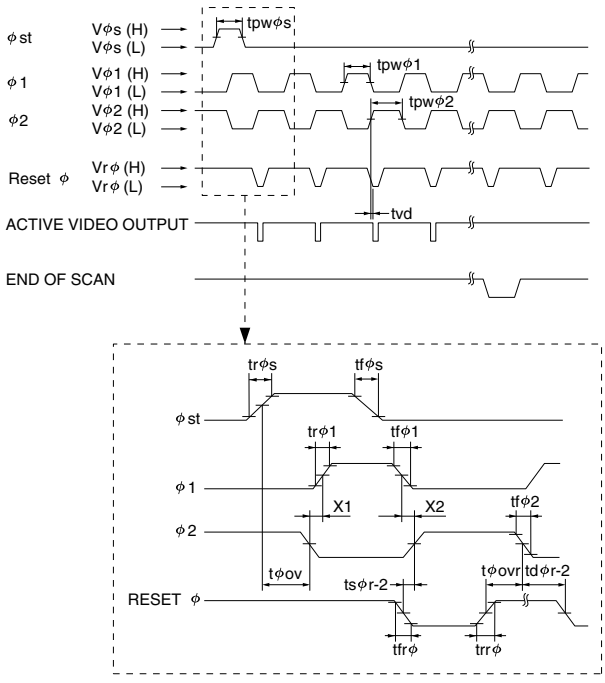
A constant voltage should be applied to the drain of the source follower circuit in the output signal processing section, from the Vdd terminal. The voltage Vdd should be equal to the clock pulse voltage Vϕ. The saturation control drain voltage Vscd should be equal to the reset voltage Vr, and the saturation control gate voltage Vscg should be grounded.

3-3-5. Input/output pulse timing for voltage output type

Figure 3-23 shows the input/output pulse timing for a voltage output type NMOS linear image sensor. The clock characteristics and waveform conditions are listed in Tables 3-8 and 3-9, respectively.

Figure 3-23 Pulse timing diagram (voltage output type)



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The timing for clock pulses ϕ1 and ϕ2 and the start pulse ϕst are exactly the same as those for the current output type. The signal is obtained during the period from the rise of ϕ2 to the rise of ϕr. Unlike the current output type, the reset operation of the voltage output type is done during the period when the address and reset switches are simultaneously turned on. For this reason, the reset pulse must overlap with the clock pulse ϕ2. More specifically, the reset pulse should rise during the "High" level of ϕ2 and fall during the "Low" level of ϕ2.

If this overlap time is too short, the photodiode reset is not complete, resulting in occurrence of lag. Because ϕ1 is used only for scanning operation, it has advantageous characteristics in that the pulse width of ϕ2 can be set longer than that of ϕ1 as shown in the timing diagram of Figure 3-24, just as with the current output type NMOS linear image sensors. However, the pulse width of ϕ1 and ϕ2 should be set to at least 200 ns. In order to maintain a constant photodiode reset potential, the rise of ϕ2 must be delayed at least 50 ns from the fall of the reset pulse.

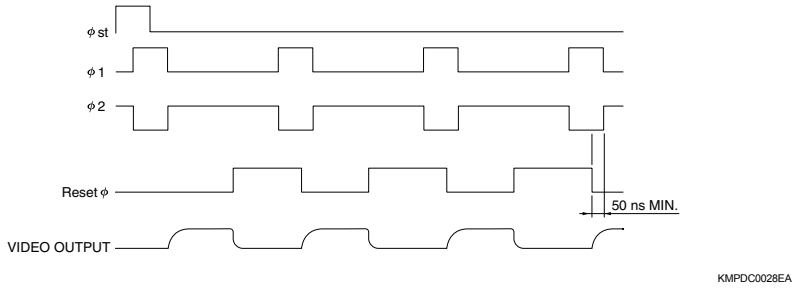
Table 3-8 Clock characteristics (voltage output type)

Parameter			Symbol	Min.	Typ.	Max.	Unit
Operating Frequency (Vr=2.5 V, Vϕ=Vdd=5 V)			f	0.1	-	500	kHz
Clock pulse line capacitance (5 V bias)	S3921 S3922	-128Q	Cϕ	-	21	-	pF
		-256Q		-	36	-	
		-512Q		-	67	-	
	S3923 S3924	-256Q		-	27	-	pF
		-512Q		-	50	-	
		-1024Q		-	100	-	
Reset pulse line capacitance (5 V bias)			Cr	-	6		pF
Saturation control gate capacitance (5 V bias)	S3921 S3922	-128Q	Cscg	-	12	-	pF
		-256Q		-	20	-	
		-512Q		-	35	-	
	S3923 S3924	-256Q		-	14	-	pF
		-512Q		-	24	-	
		-1024Q		-	45	-	

Table 3-9 Pulse waveform conditions (voltage output type)

Parameter			Symbol	Min.	Typ.	Max.	Unit
Start pulse rise time / fall time			trϕs, tfϕs	-	20	-	ns
Start pulse width			tpws	200	-	-	
Clock pulse rise time / fall time			trϕ1, trϕ2 tfϕ1, tfϕ2	-	20	-	
Clock pulse width			tpwϕ1, tpwϕ2	200	-	-	
Reset pulse rise time / fall time			trrϕ, tfrϕ	-	20	-	
Start pulse to clock pulse overlap time			tϕov	200	-	-	
Clock pulse 2 to reset pulse overlap time			tϕovr	660	-	-	
Clock pulse 2 to reset pulse delay time			tdϕr-2	50	-	-	
Clock pulse space			X1, X2	trf -20	-	-	
Clock pulse to reset pulse space			tsϕr-2	0	-	-	
Video delay time (50 % of Saturation) Vr = 2.5 V, Vϕ = Vdd = 5 V	S3921 S3922	-128Q	tvd	-	100	-	
		-256Q		-	150	-	
		-512Q		-	200	-	
	S3923 S3924	-256Q		-	100	-	
		-512Q		-	150	-	
		-1024Q		-	200	-	

Figure 3-24 Pulse timing example (recommended circuit for voltage output type)



4. Characteristics

This section explains the basic characteristics of NMOS linear image sensors as well as typical data actually measured. These measurements are made with driver circuits specifically designed for NMOS linear image sensors, which are introduced in Section 6.

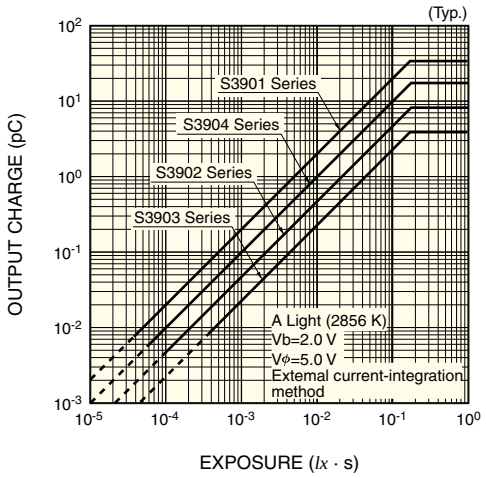
4-1. Input/output characteristics

The relation between the light level incident to the image sensor and the signal output is referred to as the input/output characteristics. As stated in Section 2, NMOS linear image sensors are operated by the charge integration readout method, so the incident light level can be expressed as incident light exposure ($lx \cdot s$), which is a product of illuminance (lx) and integration time (s).

4-1-1. Input/output characteristics (current output type)

The output signal from a current output type NMOS linear image sensor can be represented in units of charge (pC). Figure 4-1 shows a graph of input/output characteristics for S3901 to S3904 series NMOS linear image sensors, plotted on a logarithmic scale. Since the upper limit of the output charge is determined by the amount of charge that can be stored in the photodiode junction capacitance, the input/output characteristics are saturated as the output charge reaches the upper limit or break point, even though the incident light level is excessively increased. The incident light level at that point is called the saturation exposure, and the output charge is called the saturation charge. The light source used is a tungsten lamp operated at 2856 K (standard "A" light source). Note that sensitivity is wavelength-dependent and therefore differs depending on the light source used. The output will not vary even if the number of pixels or the video line capacitance is changed.

Figure 4-1 Input/output characteristics (current output type)



4-1-2. Input/output characteristics (voltage output type)

The output signal from a voltage output type NMOS linear image sensor can be represented in units of voltage (mV). As is the case with the current output type, there is a saturation point or break point in the input/output characteristics. The incident light level at that point is called the saturation exposure, and the output voltage is called the saturation output voltage. As explained in Section 3-3-2, the output voltage is determined by charge redistribution between the photodiode and video line when the address switch turns on. Therefore, the sensitivity and saturation output voltage differ, depending on the video line capacitance (the number of pixels), even though the photodiode size is identical. In addition, the source follower circuit has an upper limit in the output voltage, which also affects the final saturation output voltage. When an image sensor is operated under the recommended conditions (reset voltage=2.5 V, Vdd=Vϕ=5 V), the upper limit in the output of the source follower circuit will be about 1.3 V.

Typical input/output characteristics of S3921/S3922 series and S3924/S3923 series are shown in Figures 4-2 and 4-3. The output voltage is measured at the output terminal of the image sensor and the standard A light source is used.

Figure 4-2 Input/output characteristics [voltage output type (50 µm pitch photodiode)]

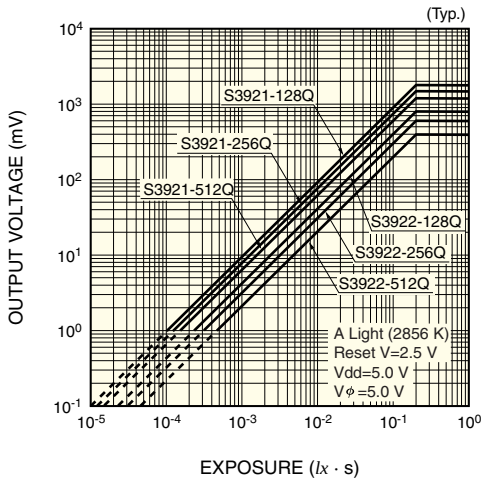
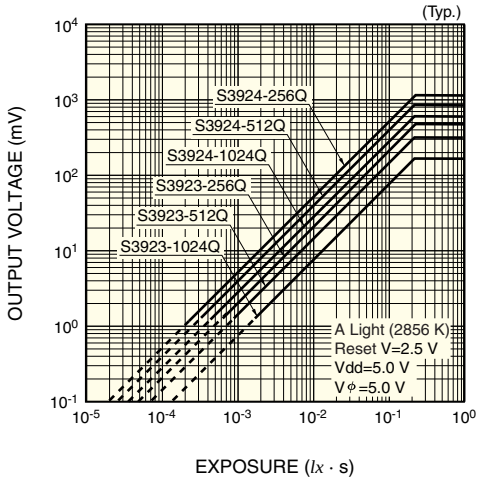


Figure 4-3 Input/output characteristics [voltage output type (25 µm pitch photodiode)]



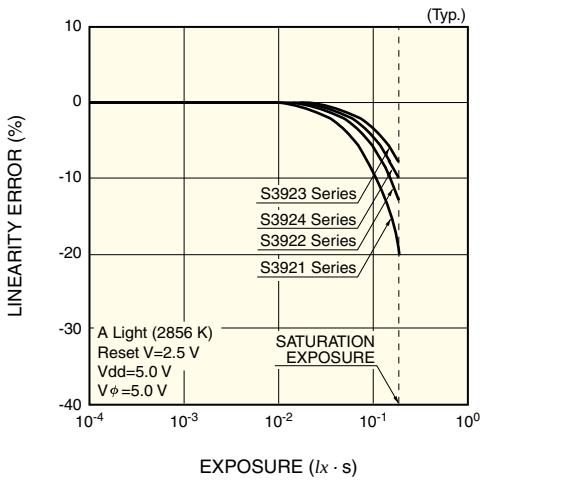
4-2. Linearity error

The slope of the input/output characteristics, the γ value, plotted on the logarithmic graph in the preceding section is approximately 1. But in actual measurement, the input/output characteristics slightly deviate from the linearity (γ=1). This deviation is known as the linearity error. The deviation from γ=1, ΔX, at a certain point, is expressed as a percentage with the deviation divided by the output X.

In the case of the current output type image sensors, as long as the output is within 95 % of the saturation charge, the linearity error can be held to a small value by using an external circuit in the current-integration readout mode, making it well suited in applications requiring high accuracy. At an output larger than 95 % of the saturation charge, part of the output begins to flow into the anti-blooming switch. The resultant output becomes smaller than γ=1 and the resulting linearity error is more than -1 %.

The output from a voltage output type image sensor is determined by the video line capacitance and photodiode junction capacitance. However, the junction capacitance is voltage-dependent and therefore increases as the output reaches saturation. As a result, the output drops below γ=1, causing a larger linearity error. Figure 4-4 shows typical linearity error in the voltage output type NMOS linear image sensor. This reveals that the linearity error is -2 % at a light exposure which is 10 % of the saturation level, and that above this, the linearity error increases ranging from -2 % to more than -50 %. The voltage output type offers ease of use yet has the disadvantage that linearity error becomes larger as the output reaches saturation.

Figure 4-4 Linearity error (voltage output type)



4-3. Spectral response characteristics

When light strikes a photosensitive section having with P-N junctions, the electrons within the valence band are stimulated. If the light energy is greater than the band gap Eg of silicon, the electrons are pulled into the conduction band, generating electron/hole pairs or carriers. These generated carriers diffuse toward the depletion layer of the photodiode. In the depletion layer the electric field accelerates the carriers to pass through the P-N junction, resulting in an accumulated signal to be read out. If the light energy is smaller than the band gap energy Eg, it cannot be detected. This limiting wavelength λ (nm) can be given by: λ=1239.5/Eg (eV)

The band gap energy Eg for silicon is 1.12 eV at room temperatures, so that the limiting wavelength will be approximately 1100 nm. This means that the silicon photodiode cannot detect light wavelengths longer than 1100 nm.

The light absorption coefficient for silicon differs depending on light wavelength. The longer the light wavelength, the smaller the absorption coefficient. In other words, incident light at longer wavelengths penetrates deeper into the silicon substrate, generating carriers in deep positions within it. Since these carriers have a limited life, they can only diffuse a certain distance after being generated. This means that, even when the same amount of light enters the image sensor, the probability that the generated carriers will reach the depletion layer and eventually be detected as an output signal varies with the depth of the carrier generation or with the incident light wavelength. In addition, how the incident light undergoes interference, reflection and absorption on the surface protective coating of the photodiode such as the silicon oxide layer, also depends on the wavelength and affects the sensitivity.

The relation between the incident light wavelength and the sensitivity is known as the spectral response characteristic. Even among silicon sensors, the spectral characteristics differ depending on the silicon substrate used and the depth of the P-N junction formed. Figure 4-5 shows typical spectral response characteristics of S3904-1024Q and S3904-1024F NMOS image sensors. The peak and valley positions in the spectral response are slightly different from process lot to lot. Hamamatsu NMOS image sensors are uniquely processed to form a junction capacitance that enhances UV sensitivity. Types with suffix “Q” have a quartz window for high sensitivity in the UV range. Furthermore, in order to reduce the adverse effect of infrared light on spatial resolution and to minimize the sensitivity ratio between short wavelength and long wavelength, Hamamatsu NMOS image sensors use a well structure capable of suppressing sensitivity on the long wavelength side. This type of NMOS image sensor provides peak response at a wavelength of near 600 nm.

The spectral response varies with the sensor element temperature. This is mainly because light absorption coefficient increases with a rise in temperature, so sensitivity varies linearly with respect to the temperature. Figure 4-6 shows the rate of change in sensitivity per °C (temperature coefficient) in NMOS image sensors, as a function of wavelength. If we let the temperature coefficient at a certain wavelength be Cλ (%/°C), then the sensitivity drops by Cλ ΔT each time temperature lowers by ΔT (°C). The longer the wavelength, the larger the change of sensitivity. This tendency is more noticeable at wavelengths longer than the peak response wavelength.

Figure 4-5 Spectral response

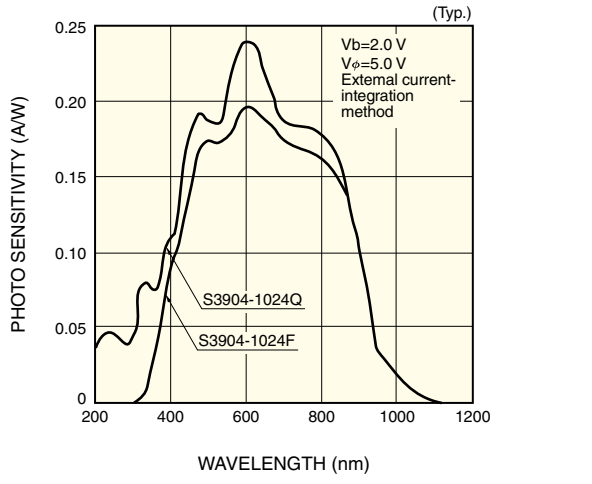
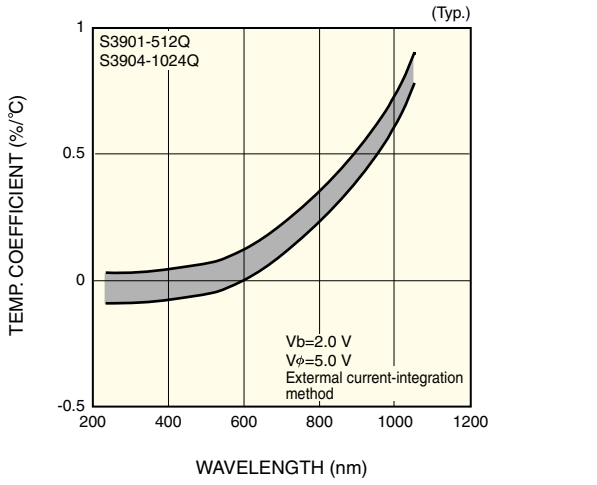


Figure 4-6 Temperature dependence of spectral response



4-4. Photoresponse non-uniformity

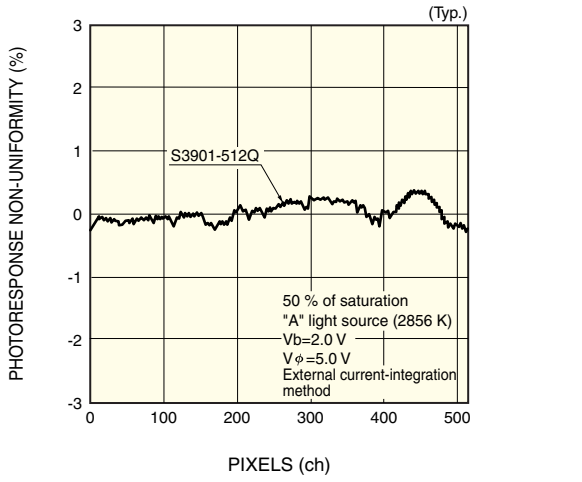
Each of the photodiodes arrayed in an image sensor is carefully fabricated to provide uniform performance, but each also exhibits some small non-uniformity in terms of sensitivity. This may be due to crystal flaws in the silicon substrate, variations in the wafer process and diffusion in the manufacturing process. This non-uniformity is often called the photoresponse non-uniformity (PRNU) and, for Hamamatsu NMOS image sensors, it is defined in the equation below by measuring the outputs of all pixels when the entire photosensitive area of each photodiode is uniformly illuminated.

$$PRNU = (\Delta X/\overline{X}) \square 100 (\%)$$

Where X is the average output of all pixels, $\Delta\overline{X}$ is the absolute value of the difference between the average output and the maximum (or minimum) output. The average output in this measurement is adjusted to 50 % of the saturation output, and a standard "A" light source is used. The outputs from the first and the last pixels are excluded from this PRNU measurement because their pixel arrangement and input pulse continuity differ from other intermediate pixels. Figure 4-7 is an example of PRNU in all pixels of S3901-512Q which has a photodiode height of 2.5 mm. It shows that the PRNU with respect to the normal average output is within ±1 %, achieving good output uniformity. The maximum non-uniformity for Hamamatsu NMOS image sensors is specified as being within ±3 %.

In addition to the element properties, scratches and dust on the faceplate may reduce the light transmission to certain pixels, causing output uniformity to deteriorate. So sufficient care concerning these points is needed when handling image sensors.

Figure 4-7 Non-uniformity



4-5. Dark output

Like other types of light sensors, NMOS image sensors exhibit a small output even when no incident light is present. This is known as the dark output (dark current), and is chiefly caused by discharge of the stored charge in each photodiode due to the recombination current within the photodiode depletion layer and/or the surface leakage current. Because the upper limit of the output is determined by the saturation charge, a large dark output narrows the output range of light detection. As with sensitivity, the dark output is non-uniform and is derived together with the light output. This means it is important to reduce the dark output to a minimal level compared to the light output unless performing signal processing that subtracts the dark output from each pixel.

The dark output charge is expressed as the product of dark current and integration time, and thereby increases in proportion to the integration time. The integration time must be determined by taking the magnitude of the dark output into account. When the signal of a current output type NMOS linear image sensor is read out with an external current-integration circuit, if we let the dark output be Vd (V) and the integration capacitance be Cf (pF), then the dark output charge Qd (pC) is given by Cf·Vd. While, if we let the integration time be Ts (s), the dark current Id (pA) is given as follows:

$$ID = Cf \cdot Vd/Ts$$

As the temperature rises, the number of carriers thermally excited into the valence band from the conduction band increase, causing dark current to increase exponentially with the element

temperature. In Hamamatsu NMOS image sensors for example, the dark current doubles for every 5 °C increase in temperature. This equals a temperature dependence of 1.15 times per °C, in other words if the temperature varies by ΔT (°C), then the dark current will be $(1.15)^{\Delta T}$ times. Accordingly, the upper limit of the image sensor operating temperature is restricted by the magnitude of the dark output. In applications requiring high measurement accuracy, temperature control of the image sensor is necessary. For instance, cooling the image sensor with a thermoelectirc cooling element will effectively reduce the dark current and allow longer integration time, thus allowing measurements at even lower light levels.

Figure 4-8 Dark current vs. temperature (current output type)

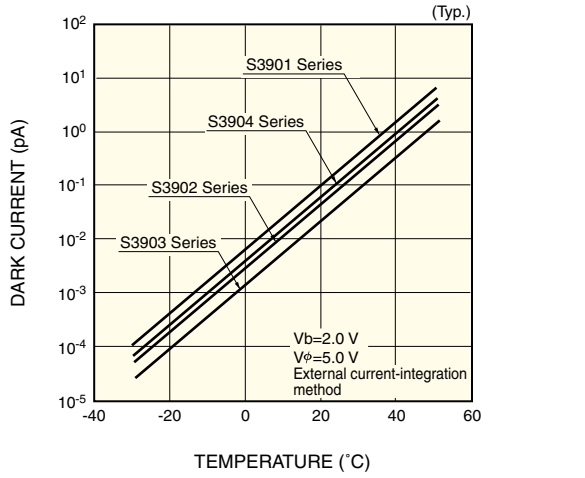


Figure 4-9 Dark output charge vs. integration time (S3901 Series)

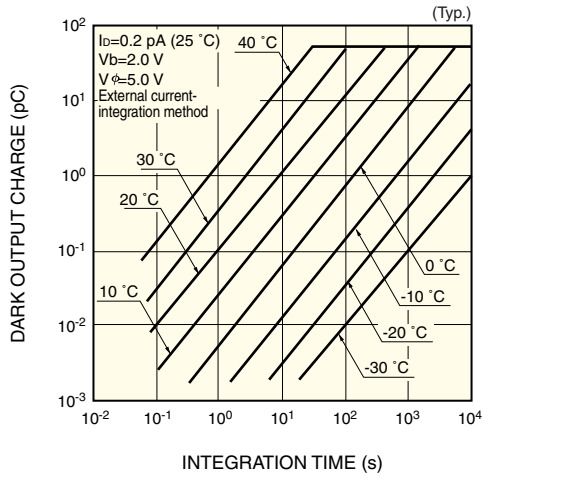


Figure 4-8 shows typical dark current temperature characteristics of S3901 to S3904 series. Their specified dark current values (typical and maximum values) at 25 °C are listed in Table 4-1. Figure 4-9 and Figure 4-10 show the dependence of dark charge as a function of integration time for various temperatures for S3901 and S3904 series respectively. Figure 4-11 shows an example of dark current uniformity in S3904-1024Q. Hamamatsu NMOS image sensors are designed to minimize the dark output as well as its non-uniformity. But dark output uniformity is usually not as good as photoresponse uniformity, and some slight erratic data may appear in some cases.

Figure 4-10 Dark output charge vs. integration time (S3904 Series)

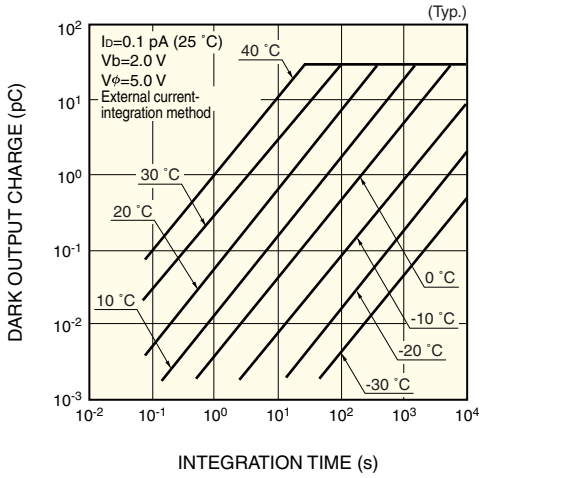


Figure 4-11 Dark current uniformity (S3904-1024Q)

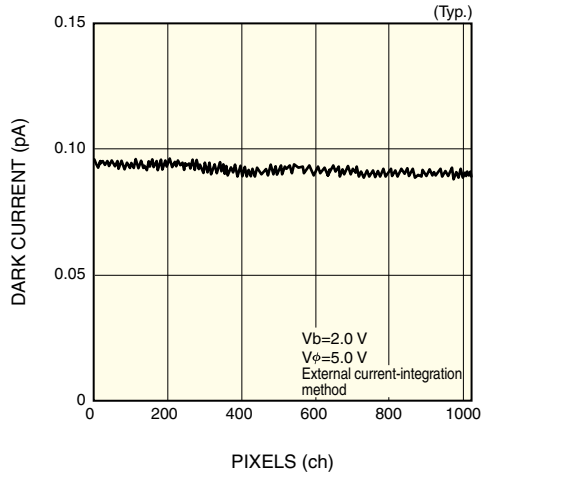


Table 4-1 Dark current (current output type)

Type No.	Dark current Ta=25 °C (pA)	
	Typ.	Max.
S3901 Series	0.2	0.6
S3902 Series	0.08	0.15
S3903 Series	0.04	0.08
S3904 Series	0.1	0.3

External current-integration method
Measured with C7884 at Vb=2 V and Vφ=5 V

4-6. Resolution

Resolution is the ability of an image sensor to discern and reproduce the details of an incident pattern. Since the photosensitive area of NMOS image sensors is not continuous but consists of many discrete pixels regularly arranged, the output of an incident image is derived as separate pixels. Therefore, when a test pattern having a series of black-and-white square wave stripes at progressively smaller spacing is viewed with an NMOS image sensor, the difference between the black and white signal levels in the output gets smaller as the stripe spacing decreases. The extent of this output modulation versus the incident pattern is called the contrast transfer function (CTF) and is defined as follows:

$$CTF = \frac{V_{WO} - V_{BO}}{V_W - V_B} \times 100 \ (\%)$$

where VW and VB are the black and white image outputs, and VWO and VBO are respectively the actual outputs of the white level and black level. As stated, the CTF is measured with a square wave pattern. On the other hand, the ratio of the output modulation versus the input from a sine wave pattern is defined as the modulation transfer function (MTF).

The fineness or detail existing between black-and-white stripes of the incident pattern is expressed in spatial frequency of the incident image. The spatial frequency is the number of stripes per unit length and is equivalent to the reciprocal of the length from one white pattern to another white pattern in Figure 4-12. Usually, the spatial frequency is expressed in units of “line pairs per millimeters (lp/mm)”. As seen in the figure, the finer the incident pattern or the higher the spatial frequency, the lower the CTF (or contrast transfer function) will be.

Resolution of Hamamatsu NMOS image sensors is defined by the MTF (or modulation transfer function). In our actual MTF measurements, the output of a certain pixel is measured while light is passed through a slit to scan the photosensitive area, and this is then converted to obtain the relation between the spatial frequency and MTF by means of Fourier transform. Figures 4-13 and 4-14 respectively show the output response of S3901-512Q and S3904-1024Q, measured when the photosensitive area is scanned with a slitted light. The abscissa indicates the distance of movement of the slitted light with respect to the center of the photodiode under measurement, so “0” means that the slitted light is striking the center of the photodiode. Figures 4-15 and 4-16 show the MTF characteristics of the output response obtained in Figures 4-13 and 4-14 respectively.

It can be seen from the figures that the resolution is wavelength-dependent. The longer the wavelength, the poorer the resolution or MTF. This is because photoelectric conversion at longer wavelengths occurs in deeper positions inside the substrate and thus the distance of diffusion in the horizontal direction is made longer, so that the generated charge may leak into the adjacent pixels until it reaches the depletion layer of the P-N junction. To suppress these effects and minimize deterioration in the resolution at longer wavelengths, Hamamatsu NMOS image sensors use a well structure in which the carriers generated in deep positions inside the substrate are captured by the substrate. Figures 4-13 and 4-14 prove that the half-width of the output response is 80 % of the photodiode pitch when the photosensitive area is scanned with a slit of light at 600 nm.

Figure 4-12 CTF characteristics

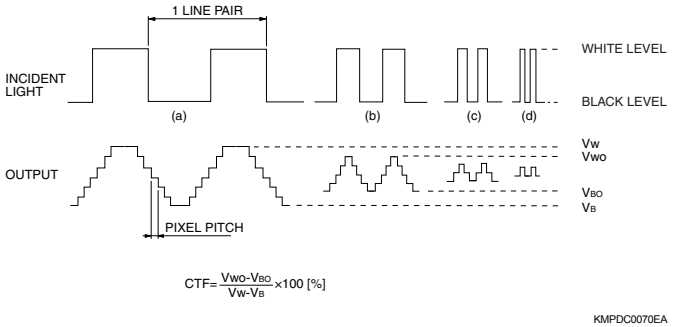


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Figure 4-13 Output response to slitted incident light (S3901-512Q)

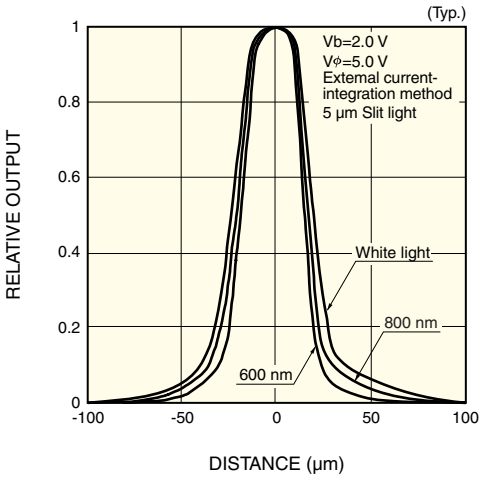

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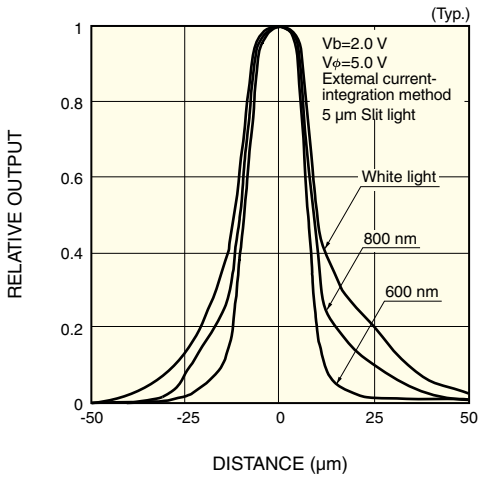
Figure 4-14 Output response to slitted incident light (S3904-1024Q)



KMPDB0076EA

Figure 4-15 MTF (S3901-512Q)

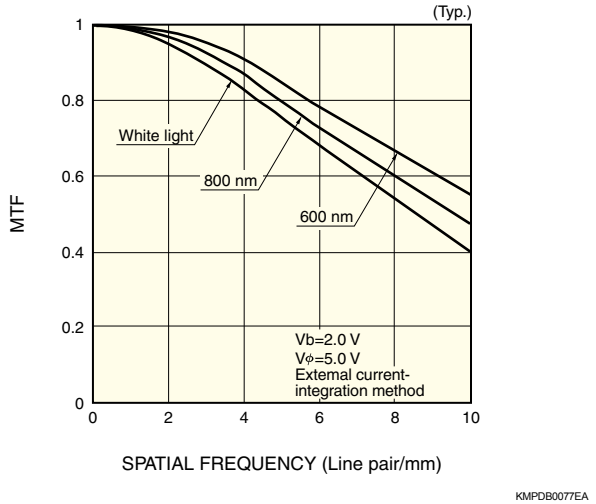
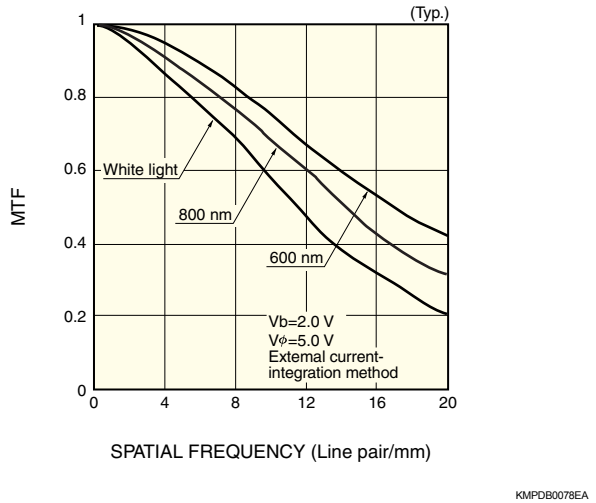


Figure 4-16 MTF (S3904-1024Q)

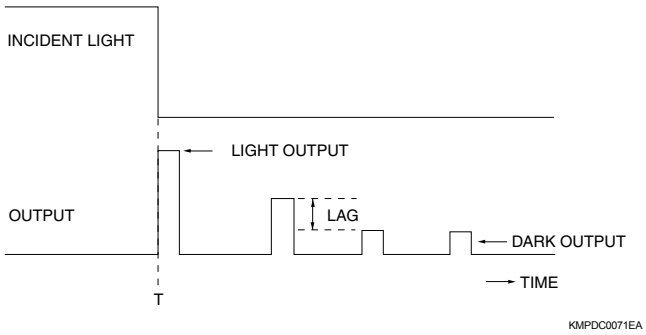


4-7. Lag

Lag is a phenomenon in which part of the signal persists in the next scan after an output signal has been read out by one scan. This is also called the time lag. A specific example is shown in Figure 4-17. When the incident light is switched from “on” to “off” at time T, the output signal is read out by the first scan after time T as the image sensor has been illuminated during the integration time. At the second scan ideally, no output signal should be read out, since the image sensor has not been illuminated during the preceding integration time. But, unless all the output signals are completely read out at the first scan, the unread signal will be read out at the next scan. In this way, lag occurs since the signal readout cannot follow a steep change in incident light, thus degrading the signal accuracy with respect to time.

Lag is caused by incomplete initialization of photodiodes. As stated in Section 2, the reset of a photodiode is performed by charging the photodiode capacitance from the power supply while the address switch is turned on and by setting the photodiode potential to a certain positive potential. Since the charging constant is determined by the photodiode capacitance Cp and the ON resistance Ron of the address switch, the charge cannot be completely injected if the address time is too short, so that the photodiode is set to a voltage lower than its correct reset potential. A charge is then fed to reach the actual reset potential from this low potential even if no incident light is present. Consequently, a signal is derived due to the stored charge at the next readout.

Figure 4-17 Lag



Due to this, the lag is closely related to the reset time, so the higher the readout speed, the larger the amount of lag. Figure 4-18 shows examples of the relation between lag and reset time, measured when the outputs of S3901/S3904 series are read out in the current-to-voltage conversion method. In this measurement, incident light is switched from “on” to “off” and the output of a certain channel is readout, then the subsequent output of the same channel at the next scan is measured. The amount of lag is defined as the rate of the output at the second scan divided by the output that should be ideally obtained with the first scan, and is usually expressed as a percentage. The amount of lag decreases exponentially as the reset time is set longer. Figure 4-18 proves that, even for S3901 series with its large photodiode area, the amount of lag decreases below 0.1 % when the reset time is set to 2.5 µs or longer.

As stated above, the reset time for the current output type image sensors corresponds to the time that the address switch is turned on (or the time that clock pulse ϕ2 is being fed in). To the contrary, the reset operation for the voltage output type image sensors is performed while the address switch is turned on and also an external reset pulse is applied to the reset switch. Thus reset time corresponds to the overlap time of the clock pulse ϕ2 and reset pulse. Figure 4-19 shows an example of how the amount of lag relates to the overlap time of ϕ2 and reset pulse for S3921/S3924 series. The figure shows that the amount of lag decreases exponentially as the overlap time lengthens, for example the amount of lag for S3921-512Q decreases to below 0.1 % when the reset time is set to 2 µs or longer.

The discussion above refers to a situation that the incident light level steeply has decreased. When the incident light conversely increases, a similar phenomenon occurs producing a signal output which is smaller than the ideal output. If the amount of unread signal is too large, a lag may appear in not only the first scan but also the subsequent scans, so that several scans may be required before reaching a normal output state. At this point,

when there is sufficient time for signal processing with respect to a change in the incident light, a dummy scan is effective in eliminating lag effects. In this method, after the signal has changed, dummy scans are repeated until the output reaches the normal steady state, and data is then read out.

Figure 4-18 Lag (current output type)

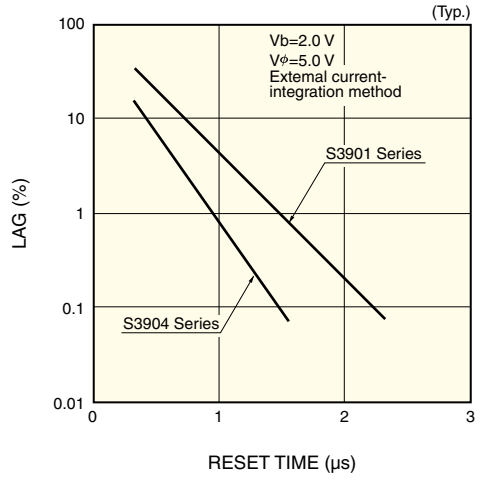
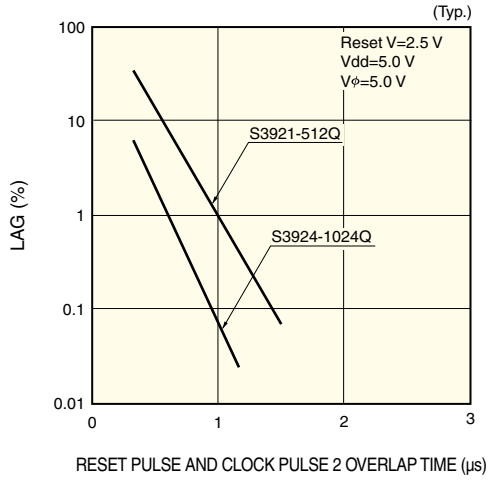


Figure 4-19 Lag (voltage output type)



4-8. Noise

NMOS image sensor noise is largely divided into fixed pattern noise and random noise.

Fixed pattern noise includes spike noise and dark current. Spike noise is a switching noise occurring on the video line via the drain to gate capacitance of the MOS switch when an address pulse is input. The magnitude of these noises is constant when the readout conditions are specified, so they can be subtracted from each pixel on signal processing software.

In contrast, random noise is traceable to erroneous fluctuations of voltage, current or electrical charge which are caused in the signal output process. This random noise may occur inside the image sensor and also in the readout circuit. When the fixed pattern noise is subtracted by an external circuit, random noise determines the lower limit of light detection of the image sensor, or the lower limit of dynamic range. Taking performance during actual operation into account, Hamamatsu NMOS image sensors are tested and evaluated by measuring the total random noise derived from the readout circuit, not from the image sensor only. The following sections discuss random noise of the current output type and voltage output type NMOS image sensors, evaluated with the recommended driver/amplifier circuits available from Hamamatsu. The noise level is expressed in equivalent input noise or ENI, which is a value converted into input charge units to the image sensor. These units are the root-mean-square value for the number of electrons (electrons r.m.s.).

4-8-1. Random noise in current output type

When a current output type NMOS linear image sensor is read out by the external current-integration method, the following 5 types of random noise components may be included in the output.

(1) Dark current shot noise
(2) Photodiode reset noise
(3) Reset noise due to readout circuit integration capacitance
(4) Readout circuit current noise
(5) Readout circuit voltage noise

Figure 4-20 shows a typical noise level when the signal of a current output type NMOS image sensor is read out by an external current-integration circuit. Here the abscissa indicates the sum of the photodiode capacitance and video line capacitance. This noise measurement is made at a readout speed of 64 µs per pixel, an integration time of 100 ms and a sensor element temperature of 15 °C. The noise level is 2000 to 3500 (electrons r.m.s.) depending on the pixel size and the number of pixels.

In general, reset noise (3) occurring when the integration capacitance is reset, is predominant in current-integration circuits. However, this component can be greatly reduced by introduction of a clamping circuit that holds the signal at a constant potential immediately after reset has been performed. Consequently, the readout circuit voltage noise (5) and photodiode reset noise (2) become significant sources of random noise. The readout circuit voltage noise increases in proportion to the sum of the video line capacitance and photodiode capacitance, while the photodiode reset noise increases in proportion to the square root of the photodiode capacitance. The reset noise component makes up a large portion of the total noise, especially for S3901/S3904 series NMOS image sensors which have a large photodiode area.

The dark current shot noise (1) results from fluctuations due to erratic generation of the dark output charge. This noise level is small under the above conditions, but increases with increasing dark output charge. Therefore, it differs depending on operating conditions such as integration time and temperature (dark current value). Figure 4-22 shows the noise level (theoretical value) of S3904-1024Q as a function of the dark output charge.

The dark current shot noise component makes up a larger portion of the noise, and as the dark output charge increases, resulting in more total noise. In addition to the above noise sources, there is shot noise due to photon-excited charges produced when light strikes the image sensor. This is caused by fluctuations due to the random arrival of photons. Consequently, the noise level as shown in Figure 4-20 may not be attained depending on the actual operating environment.
Since the upper limit of the dynamic range is determined by the saturation output charge while the lower limit depends on the charge equal to the noise level shown in Figure 4-20, the dynamic range can be figured out from these values. Table 4-2 shows the dynamic range for the current output type image sensors.

Figure 4-20 Noise level (Current output types)

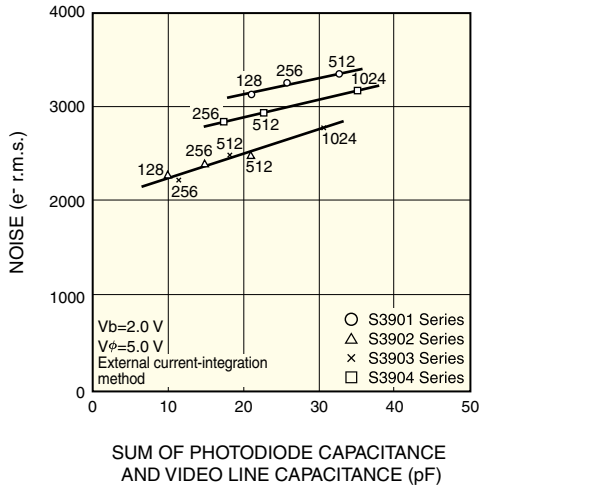


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Figure 4-21 Noise level vs. dark output charge (Theoretical value for S3904-1024Q)

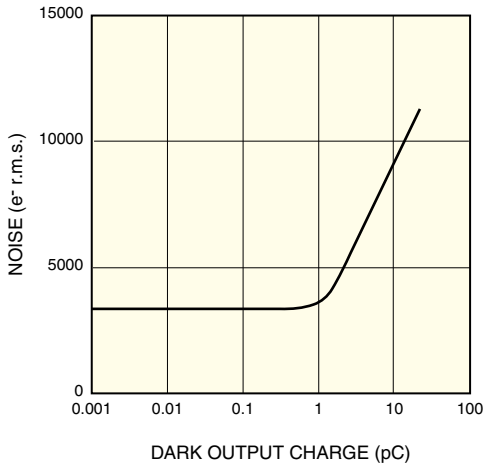

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Table 4-2 Dynamic range of current output types

Type No.	DR	ADC
S3901-128	9.5×10^4	16
-256	9.1×10^4	
-512	8.7×10^4	
S3902-128	2.5×10^4	15
-256	2.4×10^4	
-512	2.3×10^4	
S3903-256	1.2×10^4	14
-512	1.0×10^4	
-1024	0.9×10^4	
S3904-256	4.4×10^4	15
-512	4.2×10^4	
-1024	4.0×10^4	

4-8-2. Random noise (voltage output type)

When the signal of a voltage output type NMOS linear image sensor is read out by the external inverting amplification method, the following 6 types of random noise components may be included in the output.

(1) Dark current shot noise
(2) Photodiode reset noise
(3) Video line reset noise
(4) Readout circuit current noise
(5) Readout circuit voltage noise
(6) Johnson noise of resistors used in inverting amplifier of readout circuit

Figure 4-22 shows a typical noise level when the signal of a voltage output type NMOS linear image sensor is read out by an external inverting amplification circuit. Here the abscissa indicates the sum of the photodiode capacitance and video line capacitance. This noise measurement is made at a readout speed of 64 µs per pixel, an integration time of 100 ms and a sensor element temperature of 15 °C. The noise level is proportional to the sum of the photodiode capacitance and video line capacitance, and ranges from 2000 to 5500 (electrons r.m.s.).
The dominate noise sources are, readout circuit current noise (4), Johnson noise (6), and video line reset noise (3). The readout circuit voltage noise and Johnson noise are proportional to the sum of the photodiode capacitance and video line capacitance. The video line reset noise is proportional to the square root of the video line capacitance. Just as with current output type image sensors, dark current shot noise of (1) and photon-induced shot noise will vary depending on the operating conditions.
Since the upper limit of the dynamic range is determined by the saturation output charge while the lower limit depends on the charge equal to the noise level shown in Figure 4-22, the dynamic range can be figured out from these values. Table 4-3 shows the dynamic range for the voltage output type image sensors.

Figure 4-22 Noise level (voltage output type)

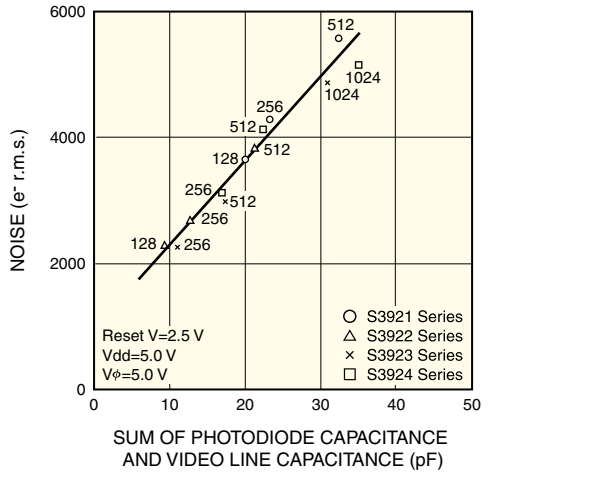


Table 4-3 Dynamic range (voltage output type)

Type No.	DR	ADC
S3921-128	4.7×10^4	15
-256	4.5×10^4	
-512	4.1×10^4	
S3922-128	2.4×10^4	15
-256	2.1×10^4	
-512	1.7×10^4	
S3923-256	1.4×10^4	14
-512	1.1×10^4	
-1024	0.7×10^4	
S3924-256	3.9×10^4	15
-512	3.0×10^4	
-1024	2.7×10^4	

4-9. Shift register frequency characteristics

The shift register of NMOS linear image sensors consists of N-channel MOS transistors and operates when an external start pulse and two-phase clock pulses are applied. The clock pulse must have an amplitude higher than a certain voltage. This is because a voltage higher than the threshold voltage Vth must be applied to the gate of MOS transistors which constitute the shift register, in order to turn on the MOS transistors. This minimum clock pulse voltage required for shift register operation varies with the operating frequency, so the maximum operating frequency exists according to the clock pulse voltage. This limitation of the operating frequency occurs because, as the operating frequency increases, the pulse response in the scanning circuit required for shift register operation does not end within the clock time and disables normal operation of the shift register. At this point, increasing the clock pulse voltage lowers the ON resistance of MOS transistors and makes the pulse response faster, thus enabling proper operation. In this way, the higher the clock pulse voltage, the higher the maximum operating frequency will be. The maximum operating frequency for Hamamatsu current output type NMOS image sensors is specified as a 2 MHz data rate (readout frequency) at a clock pulse voltage of 5 V.

The frequency characteristics of the minimum operating clock pulse voltage also vary with the sensor element temperature. The threshold voltage Vth and pulse response that determine the lower limit of the operating clock voltage vary with temperature, but in different manners. The threshold voltage Vth for MOS transistors drops with increasing temperature and the minimum clock pulse voltage required to turn on MOS transistors drops. In contrast, the pulse response become slower as temperature increases because the ON resistance of MOS transistors and the diffusion resistance inside the scanning circuit increase, and the maximum operating frequency decreases but the minimum operating clock voltage increases.

Figures 4-23 and 4-24 show minimum operating clock pulse voltage vs. readout frequency at different temperatures from -40 °C to +50 °C while the duty ratio of two-phase clock pulses is set to 1:1. When the readout frequency is low, the threshold voltage Vth is predominant in determining the minimum operating clock pulse voltage, and the lower the temperature, the higher the minimum operating clock pulse voltage becomes. On the other hand, in high-speed operation the pulse response is the dominant factor, and the higher the temperature, the higher the minimum operating clock pulse voltage becomes.

Figure 4-23 Minimum operating clock pulse voltage vs. readout frequency (S3901-512Q)

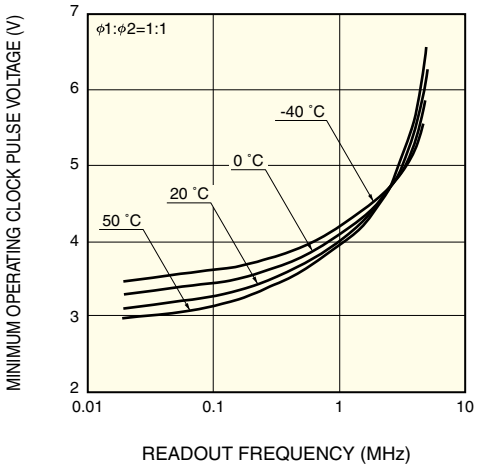
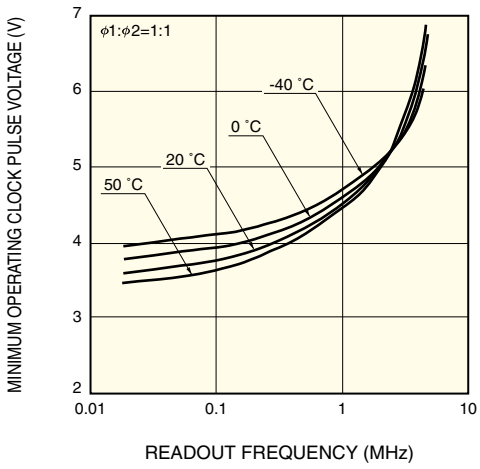


Figure 4-24 Minimum operating clock pulse voltage vs. readout frequency (S3904-1024Q)



4-10. Characteristic change by UV exposure

Silicon photodiodes characteristics tend to deteriorate after continuous exposure to UV (ultraviolet) radiation, for example dark current may increase or sensitivity may drop. This deterioration is attributed to an increase in the interface state, which occurs when binding of Si and H, O or OH at the Si-SiO_2 interface is broken by input of high-energy UV radiation. This then causes the surface leakage current to rise, leading to an increased dark current. At the same time, the photon-generated charge is trapped by this state, so the photon-generated current reduces, resulting in lowered sensitivity. This is particularly noticeable for light at shorter wavelengths because it is absorbed near the surface of the substrate.

Figures 4-25 and 4-26 respectively show spectral response and dark current characteristics of S3901-512Q, measured after exposure to UV radiation from a mercury lamp (1100 Joules/cm^2 at 254 nm).

Spectral response measured before UV exposure is also plotted in Figure 4-25 indicating there is no sensitivity drop even after UV exposure. Figure 4-26 shows dark current variations in percentage, with 100 % being equal to the initial value measured before UV exposure. It is clear that the dark current increase is suppressed to 2.5 times the initial value even after a UV exposure of 1100 Joules/cm^2.

Hamamatsu NMOS linear image sensors are designed to provide stable characteristics even after a long-term UV exposure making them ideally suited for use in spectrophotometry where sensors are likely to be used for the detection of UV radiation.

Figure 4-25 UV sensitivity after UV exposure (S3901-512Q)

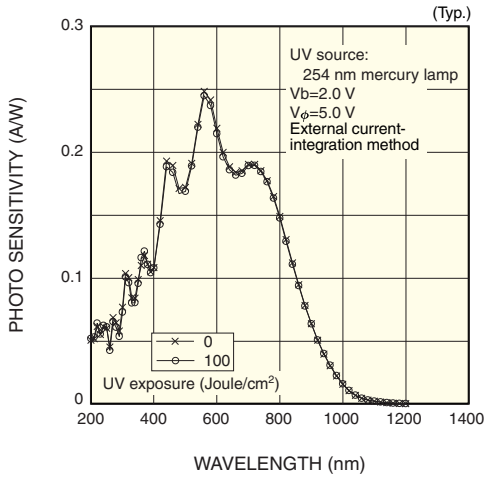


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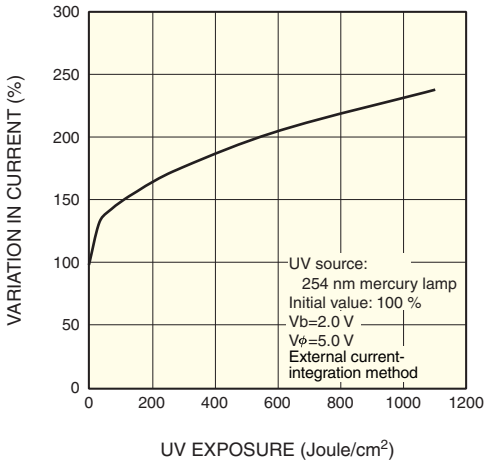
Figure 4-26 Dark current change under UV exposure (S3901-512Q)



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5. Precautions

5-1. Integration time setting

The integration time corresponds to the time interval between start pulses ϕst. This means that the integration time does not vary even if the operating frequency of the shift register is changed. The integration time can only be changed by varying the interval between the input of one start pulse and the input of the next start pulse.

When setting the integration time, its maximum and minimum times are limited by incident light intensity, dark current level, and readout time. Therefore, an optimum integration time must be selected by taking these factors into account.

(1) Incident light intensity

The output of an NMOS linear image sensor is proportional to the quantity of incident light, in other words, the product of the light intensity and the integration time. Since the maximum charge that can be stored in each photodiode is finite, it is not possible to read out a signal change exceeding the saturation output charge. In addition, such an over-saturation charge may cause blooming phenomenon, resulting in adverse effects on image sensor characteristics.

For the above reasons, the maximum integration time must be set in consideration of the incident light intensity, so that no saturation occurs in the signal output.

(2) Dark current level

The dark output is proportional to the product of the dark current and the integration time. Since the saturation output charge is constant, an increase in dark output narrows the range of light detection. The dark output also exhibits non-uniformity, so the dark output component of each pixel must be subtracted, otherwise light detection accuracy degrades with increasing dark output.

The allowable level of the dark output depends on the characteristics to be required. The allowable level of the dark output should first be determined and then the integration time set so that dark output does not exceed the required value. Because the dark output is also temperature-dependent, the integration time should be adjusted according to changes in the ambient temperature.

For example, let us consider the integration time settings needed to make measurements using S3904 series NMOS linear image sensor under conditions where the allowable dark output is 1 % of the saturation charge. Since the dark current at a saturation charge of 20 pC and operating temperature of 25 °C is typically 0.1 pA, the maximum integration time T becomes 2 seconds as calculated from the equation below. If the sensor element temperature rises to 35 °C, the dark current increases to 0.4 pA. The maximum integration time for the same allowable dark output (1 % of the saturation charge) will be 500 ms.

$$T = (Qsat \times \text{allowable value}) / I_D$$
$$= (20 \times 0.01) / 0.1 = 2\ (s)$$

(3) Readout time

When a start pulse is input, the shift register starts operation. The next start pulse cannot be input until the last pixel is scanned for output (readout time). If a start pulse is input during the readout time again, the output signals from the first scan and the second scan are mixed. In view of the these facts, it is obvious that integration time cannot be set shorter than the readout time required to scan all pixels, so the minimum integration time is limited by the readout time. Therefore, the minimum integration time is determined by the readout frequency and number of pixels.

For example, when an NMOS linear image sensor with 1024 pixels is operated at a readout frequency of 50 kHz, the readout time required for all pixels is

$$20\ \mu s \times 1024 = 20.48\ ms$$

The integration time cannot be set shorter than this value.

The readout frequency for Hamamatsu NMOS linear image sensors is matched with the clock pulse frequency. The maximum readout frequency is determined by the maximum operating frequency of the shift register. But it should be noted that image sensor characteristics such as the amount of lag may vary depending the reset time for each pixel as explained previously, even when the image sensor is operated at a frequency lower than the maximum readout frequency. Accordingly, readout time must be selected by taking into account operating and readout conditions as well as the characteristics necessary for the device application.

5-2. Output estimation

If the illuminance of light falling on the photosensitive surface is known, the output charge can be estimated from the spectral response characteristics.

Taking as an example a situation in which S3904 series (pixel pitch 25 µm, pixel height 2.5 mm) is illuminated with light at a wavelength of 500 nm and a faceplate illuminance of 1 µW/cm^2. If the integration time is set, for example, to 100 ms, then the incident exposure is given by

$$\text{Input light exposure} = \text{illuminance [W/cm}^2\text{]} \times \text{integration time [s]}$$
$$= 1 \times 10^{-6} \times 0.1\ [\text{W} \cdot \text{s/cm}^2]$$
$$= 0.1\ [\mu\text{J/cm}^2]$$

Next, let us figure out the sensitivity of S3904 series in response to incident light at 500 nm. Spectral response in Figure 4-5 is represented in sensitivity per unit area, which is 0.2 A/W at 500 nm. If the entire photodiode is illuminated, the sensitivity of S3904 series is given as follows:

$$\text{Sensitivity} = 0.2\ [\text{A/W}] \times 0.25 \times 25 \times 10^{-4}\ [\text{cm}^2]$$
$$= 1.25 \times 10^{-4}\ [\text{cm}^2 \cdot \text{A/W}]$$
$$= 125\ [\text{cm}^2 \cdot \mu\text{C/J}]$$

Thus the output charge is given by the product of input light exposure and sensitivity, as follows:

$$\text{Output charge} = \text{input light exposure} \times \text{sensitivity}$$
$$= 0.1 \times 125 = 12.5\ [\text{pC}]$$

Since the saturation charge of S3904 series is 20 pC, an output charge equal to about 60 % of the saturation charge can be obtained under the above conditions. The output charge is proportional to the integration time and as described previously, the integration time is limited by the output saturation time, so that the maximum integration time in this case will be 20/12.5 × 100 = 160 ms.

The output charge can also be estimated for image sensors with different photosensitive areas or different light wavelengths, by substituting the numerical values in the above equations.

5-3. Light sources

Since NMOS linear image sensors have spectral response characteristics, their sensitivity differs depending on light wavelength of the light source to be used. This means that light intensity and integration time must be adjusted according to the light source. Input/output characteristics of Hamamatsu NMOS linear image sensors are measured using a standard "A" light source (tungsten lamp at 2856 K color temperature).

When a tungsten lamp or deuterium lamp is used as the light source, attention should be paid to the output stability after the lamp turns on and to the output variations resulting from the lamp service life. In some cases, the sensor element temperature may rise due to the lamp heating up, causing the dark output and apparent sensitivity to increase. In addition, the sensor element temperature may rise due to repeated opening and closing of the shutter located between the lamp and the sensor, thus increasing the dark output and apparent sensitivity as well. Therefore, in applications requiring high accuracy, some means to minimize temperature change in the sensor element is essential. Such means would include, for example, radiating heat from the light source, widening the distance between light source and sensor element, and temperature control of the sensor element.

In the measurement of light from an AC-operated light source such as a fluorescent lamp, if the frequency is too low, lighting fluctuation may appear in the output as flicker effects. Therefore, such a lamp must be operated at a high frequency of about 50 kHz or more, and not at the normal frequency used in commercial power lines. In high frequency lighting, the lighting duration is sufficiently short compared to the integration time, so flicker effects on the output are reduced.

In measurement of pulsed light from an LED and other light sources, if changes in light intensity occur within the integration time, the NMOS linear image sensor operating in the charge-integration mode cannot detect these changes separately. The changes within the integration time are output as one signal.

When the light source is positioned too close to the image sensor, non-uniformity in the incident light level, which results from the light source output characteristics and/or the installation method, may appear in the image sensor output. In such cases, the light source must be positioned farther away from the sensor or a diffuser plate should be interposed between them so that the incident light becomes uniform. When focusing on an image with a lens system, the quantity of light near the image sensor might sometimes be reduced. This problem (so-called shading) can be corrected by placing a slit with an aperture pattern which is inverse to the output pattern, in the optical path.

When the incident light includes long wavelength components, resolution and output uniformity may be degraded because long wavelength light is absorbed at deeper positions within the sensor substrate. To minimize these effects, Hamamatsu NMOS linear image sensor are designed to suppress sensitivity to long wavelengths. In addition, use of an infrared-cut filter further reduces these effects. On the other hand, light of short wavelengths has higher incident energy and may cause damage inside the sensor substrate, leading to an increased dark current and lowered sensitivity. Due to the improved manufacturing process, Hamamatsu NMOS linear image sensors are engineered to resist UV radiations. However, the NMOS linear image sensor should not be exposed to UV radiations unnecessarily except during measurement, because the longer the UV exposure time, the larger the deterioration of characteristics becomes.

5-4. Positional accuracy of photosensitive area

Photodiodes are arrayed in geometrical precision on the silicon chip of an NMOS linear image sensor, providing a high degree of position detection accuracy. However, due to factors such as mounting precision of the chip onto the package or dimensional precision of the ceramic package itself, the distance from the package to the photosensitive position is specified within a certain tolerance with respect to a reference position.

Figure 5-1 shows outline drawings of an NMOS linear image sensor together with the positional accuracy of the photosensitive area. Drawing (1) of Figure 5-1 shows a top view of the image sensor, and (2) is a side view in the scanning direction, while (3) is another side view along the plane perpendicular to the scanning direction. In Hamamatsu NMOS linear image sensors, the positional accuracy in the scanning direction is specified as the distance between the first pixel position and the package center, as shown in (1). The height of the photosensitive surface is specified as the distance from the surface of the quartz window to the chip surface. The package size and the position of the photosensitive area differ according to the pixel size and number of pixels.

As stated, the position of the photosensitive area is within a certain tolerance. This means that the positional accuracy may differ slightly from image sensor to image sensor. In critical applications requiring high measurement accuracy, the image sensor should be installed in equipment having an alignment mechanism for making fine-adjustments to the positions in the X, Y and Z directions and also to the chip surface angle θ with respect to the package, so that the tolerance of each image sensor can be compensated.

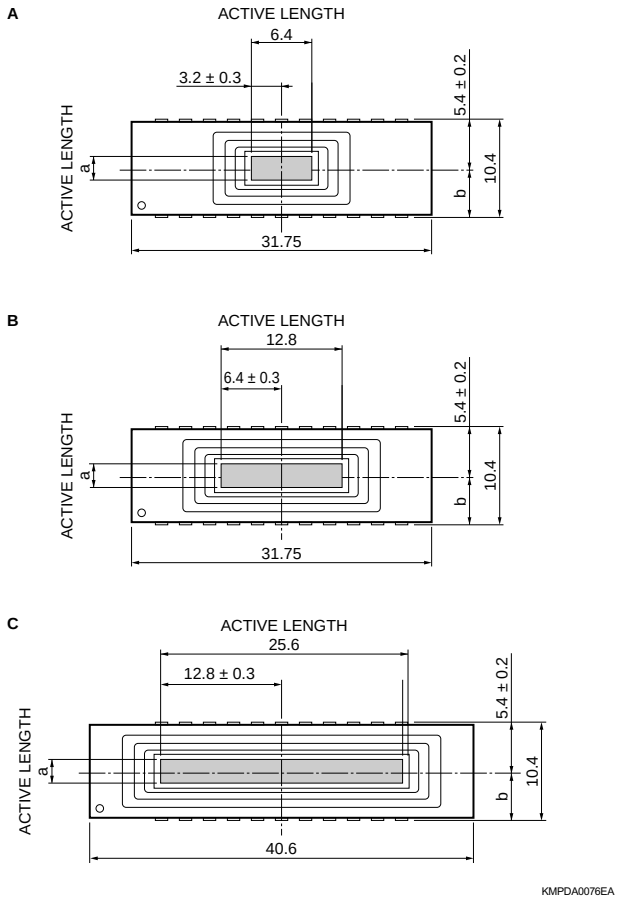
The photosensitive position tolerance with respect to the leads becomes even larger when involving package lead brazing precision which is about ±0.2 mm. Also note the direction of height, since the leads are not always brazed perfectly parallel to the package. For this reason, the photosensitive area might become tilted with respect to the board if the image sensor is installed using the leads as a reference. To avoid this, fit in

spacers between the board and package to make it level so that the package surface can be used as a reference for installing the image sensor. The table below and Figure 5-1 show the dimensional and positional tolerance of Hamamatsu NMOS linear image sensors.

Type No.	Top view	a	b	Side view
S3901/S3921-128	A	2.5	5.0 ± 0.2	D
-256	B			D
-512	C			E
S3902/S3922-128	A	0.5	5.2 ± 0.2	D
-256	B			D
-512	C			E
S3903/S3923-256	A	0.5	5.2 ± 0.2	D
-512	B			D
-1024	C			E
S3904/S3924-256	A	2.5	5.0 ± 0.2	D
-512	B			D
-1024	C			E

Figure 5-1 Dimensional outlines (Unit: mm)

(1) Package top view



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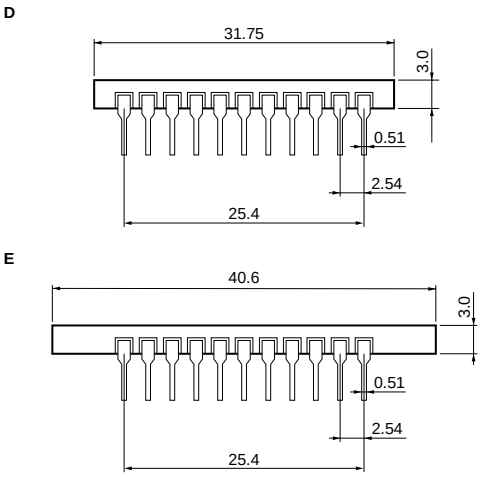
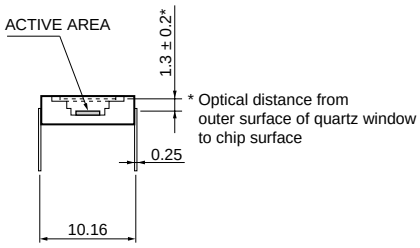
(2) Package side view



(3) Chip height (all types)



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5-5. Precautions during handling

Pay special attention to the following points to ensure correct use of NMOS linear image sensors.

(1) Absolute maximum ratings

As with other electronic devices, NMOS linear image sensors have maximum ratings specified for the supply voltage, storage temperature and operating temperature that must not be exceeded even momentarily. Always use a NMOS linear image sensor within the maximum ratings. For example, the maximum ratings for Hamamatsu NMOS linear image sensors with a quartz window are specified as 15 V for the supply voltage, -40 to +85 °C for storage temperature, and -30 to +65 °C for the operating temperature.

(2) Installation

When installing an image sensor into the socket on the circuit board, note the correct pin positions. If the image sensor is mistakenly mounted in a reversed or incorrect position, it may be damaged when power is applied. After making sure the image sensor has been installed correctly, turn on the power supply.

(3) Electrostatic countermeasures

Although NMOS linear image sensors are provided with safety measures to guard against static electricity, careful handling is required. For example, always wear cotton gloves and antistatic clothing to prevent electrostatic damage due to electrical charges from friction etc. Furthermore, electrostatic measures

should be implemented to protect the image sensor, for example, grounding of items in the work environment and tools.

(4) Faceplate (window)

Grime or scratches on the faceplate may degrade uniform sensitivity. If fingerprints or oil from hands adhere to the faceplate, the window transmittance may be lowered, causing performance deterioration. Never touch the faceplate window with bare hands. Before using the image sensor, the faceplate should be cleaned. Use a soft cloth or cotton swab moistened with ethyl alcohol to wipe off the faceplate. Do not use dry cloth or cotton swabs as these may generate static electricity. When packaging or transporting the equipment in which the image sensor is installed, take sufficient care to keep the faceplate protected from dust, grime and scratch.

5-6. Precautions when configuring driver circuit boards

The following points require particular attention when configuring driver circuit boards because the driver and readout circuits are influenced by image sensor light input section and these circuits are also characterized by a mix of digital and analog circuitry.

(1) Image sensor mounting side

The image sensor should be installed on the rear side opposite to the component-mounted side. This is to facilitate adjustment of mounted components even after the image sensor has been installed in an optical system. For example, the variable resistors can be easily accessed from the rear side during image sensor operation.

(2) Circuit board

The mounting holes of the circuit board should be slightly larger than the screw diameter to allow fine-adjustment of the sensitive area position when mounting the circuit board. The circuit board material used should be warp-resistant so that the focal point will not shift. Moreover, the board should be resistant to heat radiation from the light source.

(3) Circuit components

As stated earlier, the dark current and sensitivity of an image sensor vary greatly with sensor element temperature. To minimize the temperature rise or variations in the sensor, use circuit components which generate as little heat as possible. If components which generate heat must be used, locate these components away from the image sensor and also provide effective heat dissipation measures.

(4) Grounding

To prevent the digital circuit noise from intruding into the analog circuit via ground, isolate the digital circuit from the analog circuit, and use a thick ground line having lower resistance. The NC (no connection) terminals should all be grounded.

(5) Digital signal

An NMOS linear image sensor can be operated with a CMOS level input clock pulses. The input clock pulse line should be separated from the video signal line and power supply line as much as possible, because constant voltage variations occur within it. The input pulses should be fed to the sensor element at the specified timing. In high-speed operation, the clock voltage hold time particularly affects shift register operation. So care is required so that rise and fall times are not delayed.

(6) Analog signal

The wiring width and length from the video output terminal to the amplifier should be kept as short as possible. Further, use the same wiring width and length of signal line for the active video side and for the dummy video side, so that their capacitance matches. To avoid noise intrusion into the output signal, the video signal line should be located away from the digital signal lines subject to constant voltage variations, such as the clock line. Also, the lines should not cross each other at the front or rear of the circuit board.

(7) Supply voltage

The video bias voltage and reset voltage determine the photodiode reset potential, and the clock pulse amplitude determines the ON resistance of the address switch. Therefore, if these supply voltages for the image sensor fluctuate, the output characteristics become unstable. The power supplies used must provide good voltage regulation and also the image sensor supply voltage should be insensitive to variations in the external voltage supply. The supply voltage for the image sensor should be stable even if voltage fluctuations accompanying the operation of the circuit components occur in the power supply line. The power supply line for the sensor element should be separated as much as possible from digital signal lines such as clock line on which constant voltage variations occur.

(8) Others

Make sure circuitry is reliably shielded because noise can be generated by factors such as mechanical action in the equipment in which the image sensor and driver circuit board are installed, and this noise then mixes with the output signal.

6. Recommended driver circuits

6-1. Driver circuit for current output type

6-1-1. Current-to-voltage conversion method

(1) Recommended circuit configuration

This type of driver circuit basically consists of a control signal generator and a video signal processor. Figures 6-1 and 6-2 show the block diagram and circuit diagram of a typical driver circuit using the current-to-voltage conversion method. The control signal generator produces various control pulses required for the image sensor and external signal processor. The video signal processor performs current-to-voltage conversion, differential amplification and then outputs the processed signal. By applying external supply voltages for digital and analog circuitry, and also master clock and master start pulses, this driver circuit provides a data video output, trigger pulse and end-of-scan (EOS) pulse. Table 6-1 gives a description of the input/output terminals.

The control signal generator consists of a PLD (programmable logic device), and generates a start pulse and two-phase clock pulses to operate the shift register. The control signal generator also provides a trigger signal for external sample-and-hold and outputs it via a buffer. These signals are synchronized with an external master clock pulse, and are initialized by an external master start pulse. The master clock and master start pulses are input to the PLD via a buffer.

The video signal processor is made up of three sections. The active video output current from the image sensor is first fed to the inverting input terminal of the first-stage amplifier and converted into a voltage. The non-inverting input terminal is applied at a video bias voltage of 2 V. Similarly, another first stage amplifier performs current-to-voltage conversion of the dummy video output from the image sensor. The output of this first stage is a positive going signal with respect to the 2 V video bias voltage, with a differential waveform. The active video output includes the signal and switching noise components, while the dummy video output only consists of a switching noise component. In the differential amplifier of the next stage, the switching noise component, which is fixed pattern noise, can be eliminated by differential amplification of these two outputs. Thus a signal output without switching noise is derived from the data video terminal as the final output. This final output has a differential waveform of positive polarity with respect to ground level. The end-of-scan (EOS) terminal is pulled up at 5 V, with a resistor of 10 kΩ. The end-of-scan signal appears synchronized with the ϕ2 timing immediately after the last pixel is scanned, and is available to an external device from the EOS terminal via a buffer.

Note the following points when selecting amplifiers.

(a) Current-to-voltage conversion amplifier

As a current-to-voltage conversion amplifier, choose a high-speed dual operational amplifier (having two circuits) that exhibits low noise and less leaks.

(b) Differential amplifier

Choose an amplifier that is resistant to load capacitance.

Figure 6-1 Block diagram of recommended current-to-voltage conversion circuit

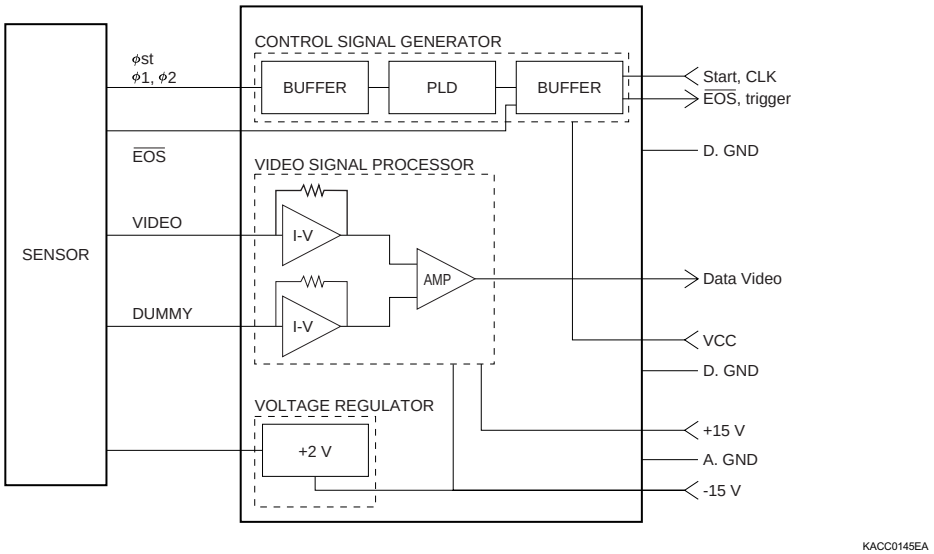


Figure 6-2 Recommended current-to-voltage conversion circuit

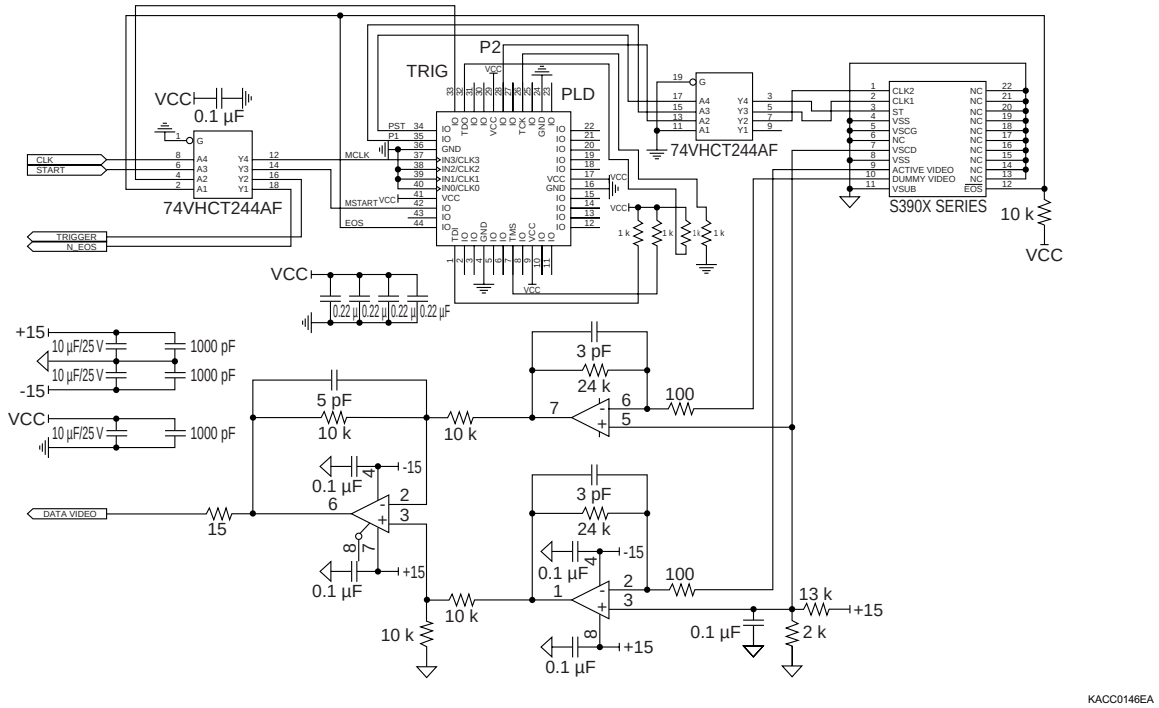


Table 6-1 Input/output terminal description of recommended current-to-voltage conversion circuit

Terminal name		Symbol on board	Polarity	Function
Input	Supply voltage Vd (for digital circuitry)	+5	-	+5 V, 70 mA
	Supply voltage Va (for analog circuitry)	+15	-	+15 V, 30 mA
		-15	-	-15 V, 30 mA
	Master start pulse ϕms	START	Positive	Initializes internally generated pulse; C-MOS logic compatible.
	Master clock pulse ϕmc	CLK	Positive	Synchronizes internally generated pulse; CMOS logic compatible.
	Ground	G	-	Ground.
Output	Video	Video	Positive	Video output.
	Trigger pulse	Trig.	Positive	A/D conversion timing signal; CMOS logic compatible.
	End-of-scan pulse	EOS	Negative	End-of-scan signal for shift register; CMOS logic compatible.

(2) Supply voltage

Table 6-2 shows typical input supply voltage, input pulse amplitude voltage, output voltage and output pulse amplitude voltage for this recommended driver circuit.

The input supply voltage Vcc for digital circuitry is +5 V, and Vs for analog circuitry is ±15 V. The input pulses consist of a master clock pulse ϕmc and a master start pulse ϕms. These are positive going pulses and their amplitude voltages Vmc and Vms are both 5 V. The trigger pulse for external output is a positive going output, while the end-of-scan pulse is a negative going output. Their amplitude voltages Vtrig and Veos are also 5 V. The final data video output obtained has positive polarity with respect to the ground.

Voltages actually applied to the image sensor are as follows: The amplitude of the clock pulses Vϕ1 and Vϕ2, and start pulse Vϕst are 5 V; the video bias voltage Vb that determines the photodiode reset voltage is 2 V; the saturation control gate voltage Vscg is 0 V; the saturation control drain voltage Vscd is 2 V which is equal to the video line bias voltage Vb. The Vss, Vsub and NC terminals are all grounded.

Table 6-2 Typical input/outupt voltages for recommended current-to-voltage conversion circuit

Input or output voltage		Symbol	Min.	Typ.	Max.	Unit
Input	Supply voltage for digital circuitry	Vd	4.85	5	5.5	V
	Supply voltage for analog circuitry	Va	±14.5	±15	±15.5	
	Mater start pulse ϕms	Vms (H)	2	5	5.4	
		Vms (L)	0	-	0.8	
	Master clock pulse ϕmc	Vmc (H)	2	5	5.4	
		Vmc (L)	0	-	0.8	
Output	Trigger pulse	Vtrig (H)	4.75	5	5.4	
		Vtrig (L)	-	-	0.4	
	End-of-scan pulse	Veos (H)	4.75	5	5.4	
		Veos (L)	-	-	0.4	
Output for image sensor	Start pulse ϕst	Vs (H)	4.75	5	5.4	
		Vs (L)	-	-	0.4	
	Clock pulse ϕ1, ϕ2	Vϕ1, Vϕ2 (H)	4.75	5	5.4	
		Vϕ1, Vϕ2 (L)	-	-	0.4	
	Video bias voltage	Vb	-	2	-	
	Saturation control drain voltage	Vscd	-	2	-	
	Saturation control gate voltage	Vscg	-	0	-	

(3) Pulse timing

The input pulse timing diagram for a recommended current-to-voltage conversion circuit is shown in Figure 6-3, along with output pulse timing for the image sensor. The input/output pulse timing conditions are also shown in Table 6-3.

Figure 6-3 Timing diagram for recommended current-to-voltage conversion circuit

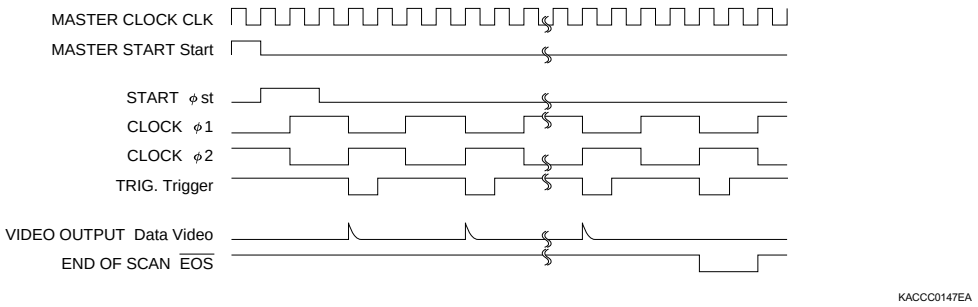


Table 6-3 Pulse timing conditions for recommended current-to-voltage conversion circuit

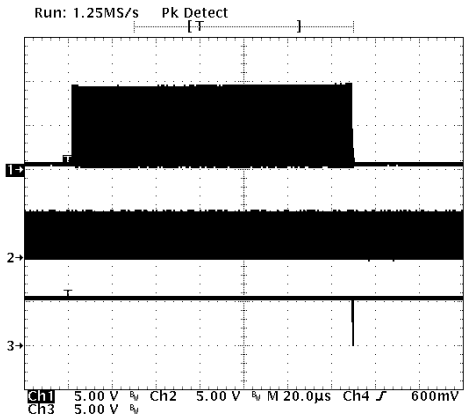
Parameter		Symbol	Min.	Typ.	Max.	Unit
Input	Mater start pulse ϕms width	tpwϕms	1/fϕmc	-	-	s
	Mater start pulse ϕms rise time / fall time	tfϕms, tfϕms	-	-	500	ns
	Master clock pulse ϕmc width	tpwϕmc	30	-	-	
	Master clock pulse ϕmc rise time / fall time	tfϕmc, tfϕmc	-	-	500	
	Master clock frequency	fϕmc	-	-	8	MHz
Output	End of scan pulse width	tpweos	-	2/fϕmc	-	s
	End of scan pulse rise time / fall time	treos, tfeos	-	-	100	ns
	Trigger pulse width	tpwtrig	-	3/fϕmc	-	s
	Trigger pulse rise time / fall time	trtrig, tftrig	-	-	100	ns
Output for image sensor	Start pulse ϕst width	tpwϕs	-	2/fϕmc	-	s
	Start pulse ϕst rise time / fall time	trϕs, tfϕs	-	-	100	ns
	Clock pulse ϕ1, ϕ2 width	tpwϕ1, tpwϕ2	-	2/fϕmc	-	s
	Clock pulse ϕ1, ϕ2 rise time / fall time	trϕ1, tfϕ1, trϕ2, tfϕ2	-	-	100	ns

The input pulses to the image sensor are supplied from the PLD at regular cycles, in minimum units of one cycle of the master clock pulse ϕmc.
The start pulse ϕst for the image sensor is produced in synchronization with the fall of the master start pulse ϕms, with a duration equal to two cycles of the master clock pulse ϕmc. Thus the master start pulse interval corresponds to the signal integration time, which is the reciprocal of the master start pulse frequency fϕms, that is, 1/fϕms (s). To ensure stable start operation, the master start pulse width tpwϕms should be longer than the master clock pulse width tpwϕmc of one cycle, and also they should be synchronized.
This driver circuit reads out one pixel in a duration equal to 4 cycles of the master clock pulse ϕmc. (One pixel may also be read out in a duration equal to one cycle or two cycles if the duty ratio of the clock pulses ϕ1 and ϕ2 is 50 %.) Therefore, all pulses other than the start pulse are generated at this cycle to produce the time-series output signal of each pixel. This means that the output signal readout frequency is 1/4th of the master clock pulse frequency fϕmc.

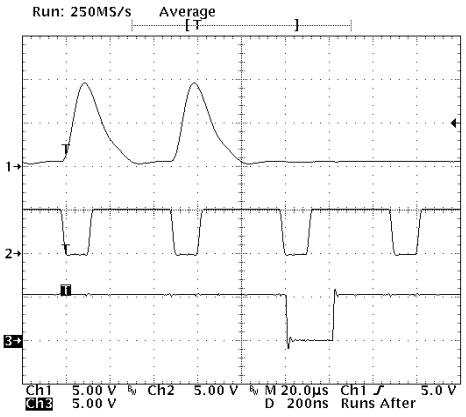
The clock pulses ϕ1 and ϕ2 for the sensor have a duty ratio of 50 %, so are complementary to each other. Both pulses are set to high level with a pulse width equal to two cycles of the master clock pulse. The 1:1 pulse ratio is most suitable when operating an image sensor at the maximum operating frequency because the upper limit of shift register operation is determined by the clock pulse width.
The signal output is obtained in synchronization with the ϕ2 timing. The timings of the start pulse ϕst and clock pulses ϕ1 and ϕ2 are also shown in Figure 6-3.
The data acquisition timing for A/D conversion in this driver circuit is set at a point one master clock pulse cycle after the signal output, and is also used for peak-hold processing of the differential waveform by using an external circuit. This timing diagram is also shown in Figure 6-3.
The end-of-scan signal is output in synchronization with the ϕ2 timing immediately after the last pixel is read out.
A saturated output is shown in Figure 6-4.

Figure 6-4 Output of recommended current-to-voltage conversion circuit (saturated output)

(a) Saturated output



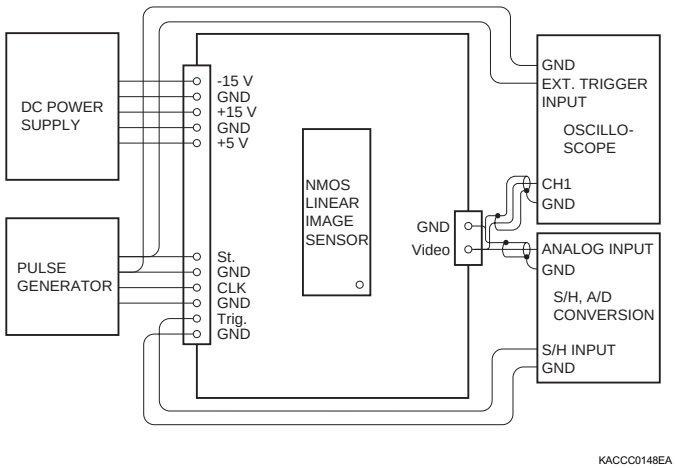
(b) Enlarged view near EOS pulse



(4) Connection

Figure 6-5 shows a wiring example for this driver circuit and peripheral devices. The power supplies (+5 V, ±15 V) should be connected to their respective power input terminals of the circuit, and the master start and master clock pulses from the pulse generator should be input to the St and CLK input terminals. The St terminal is also connected to the external trigger input terminal of the oscilloscope and the data video output (Video) is input to the oscilloscope. The trigger output terminal (Trig) and data video output terminal (Video) of this circuit should be connected respectively to the timing input terminal and analog input terminal of the S/H and A/D conversion circuit.

Figure 6-5 Wiring example (recommended current-to-voltage conversion circuit)



(5) Caution points

If operation is abnormal, check the following points.

(a) Are correct voltages (+5 V, ±15 V) being supplied to the circuit board?
(b) Are the specified master clock and master start pulses input to the circuit board?
(c) Are the clock pulses ϕ1, ϕ2 and start pulse ϕst being supplied to the image sensor socket pins?
(d) Is the end-of-scan (EOS) signal being output?

6-1-2. External current-integration method

(1) Recommended circuit configuration

This circuit basically consists of a control signal generator and a video signal processor. Figures 6-6 and 6-7 show the block diagram and circuit diagram of a recommended circuit. The control signal generator produces control pulses needed for the image sensor and signal processor. The video signal processor performs current integration, amplification and DC restoration, then outputs the processed signal. By applying external supply voltages for digital and analog circuitry, and also master clock and master start pulses, this driver circuit provides a data video output, monitor video output, trigger pulse and end-of-scan (EOS) pulse. Table 6-4 gives a description of the input/output terminals.

The control signal generator consists of a PLD (programmable logic device), and generates a start pulse and two-phase clock pulses to operate the shift register as well as signals to reset the current-integration circuit for output signal processing, clamp signals for DC restoration, and switching noise cancellation signals. The control signal generator also provides a trigger signal for external sample-and-hold and outputs it via a buffer. These signals are synchronized with an external master clock pulse, and are initialized by an external master start pulse. The master clock and master start pulses are input to the PLD via a buffer. The video signal processor can be divided into four sections. The first stage integrates the video output signal from the image sensor. The non-inverting input terminal of this first stage is applied at a video bias voltage of 2 V. A reset switch is added in

Figure 6-6 Block diagram of recommended external current-integration circuit

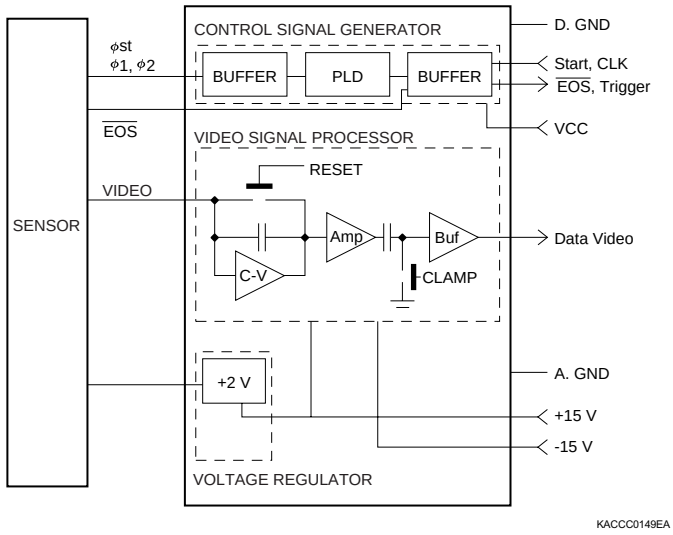


Figure 6-7 Recommended external current-integration circuit

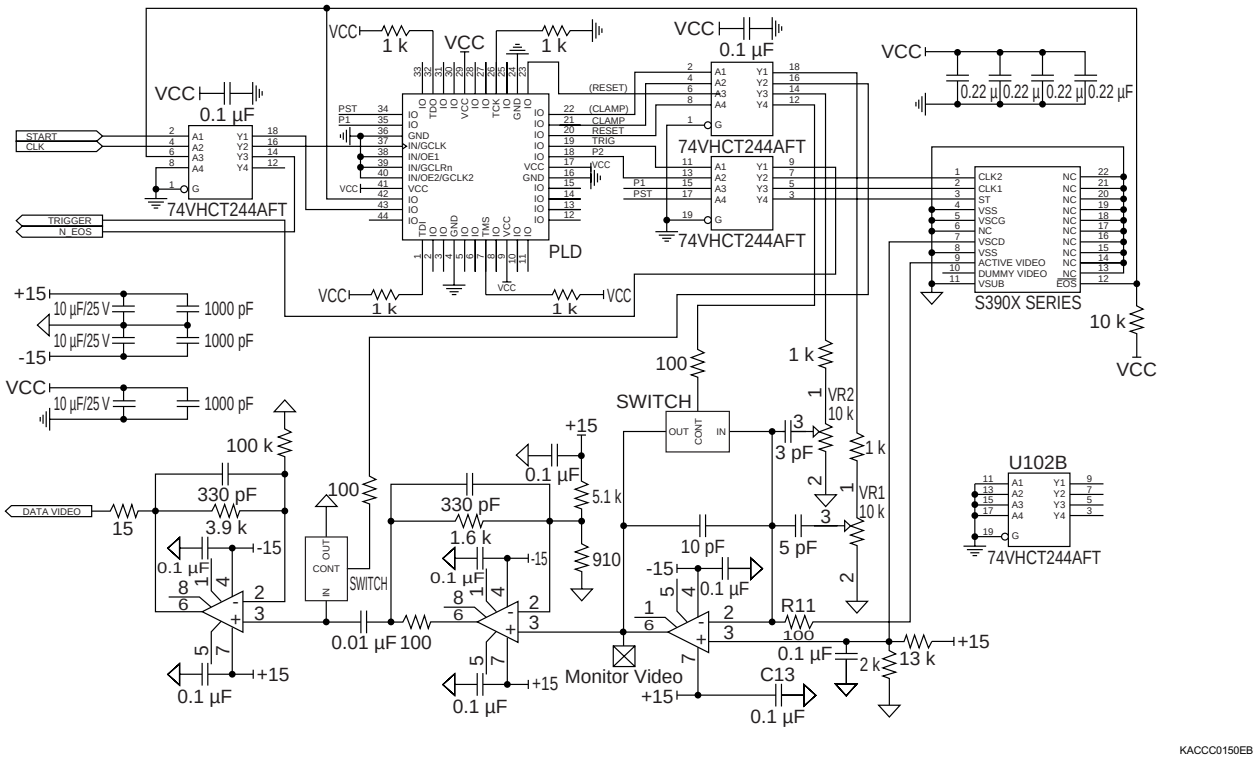


Table 6-4 Input/output terminal description of recommended external current-integration circuit

Terminal name		Symbol on board	Polarity	Function
Input	Supply voltage Vd (for digital circuitry)	+5	-	+5 V, 70 mA
	Supply voltage Va (for analog circuitry)	+15	-	+15 V, 30 mA
		-15	-	-15 V, 30 mA
	Master start pulse ϕms	START	Positive	Initializes internally generated pulse; C-MOS logic compatible.
	Master clock pulse ϕmc	CLK	Positive	Synchronizes internally generated pulse; CMOS logic compatible.
	Ground	G	-	Ground
Output	Monitor video	M.V	Positive	Output for noise cancel and adjustment
	Data video	D.V	Positive	Low noise, final video output
	Trigger pulse	Trig.	Positive	A/D conversion timing signal; CMOS logic compatible.
	End-of-scan pulse	EOS	Negative	End-of-scan signal for shirt register; CMOS logic compatible.

parallel to the integration capacitor of 10 pF, so that the capacitance is reset by a signal input to the reset switch each time a pixel is read out. The first stage also cancels the switching noise generating in synchronization with the clock pulses. The first stage output V, which is a positive going, boxcar waveform output with respect to the 2 volt video bias, is given by

$$V\ [V] = Q\ [pC] / 10\ [pF]$$

where Q is the output charge from the image sensor.
The second stage is a non-inverting amplifier with a gain of 3, which also serves as a low-pass filter to eliminate high frequency noise. This output is a positive going signal with respect to approximately 1 V, and is used as the monitor video output when adjusting the switching noise cancellation. Next is a clamping circuit consisting of a capacitor and a switching element for DC restoration of video signals. The clamping circuit holds the output potential at ground level by turning on the clamp switch for a certain period of time (clamp period) immediately after the integration capacitance is reset, so that the integration capacitance reset noise is eliminated. The clamping circuit eliminates random reset noise, while the first stage removes only fixed pattern switching noise. The output signal from this stage then changes from the ground level to positive polarity and enters the last stage. The last stage is a non-inverting amplifier with a gain of 1, also serving as a low-pass filter. The output signal is then finally derived from the data video terminal. If the output charge is Q (pC), then the output voltage Vout (V) is given by

$$Vout\ [V] = 3 \times Q\ [pC] / 10\ [pF]$$

The end-of-scan (EOS) terminal is pulled up at 5 V, with a resistor of 10 kΩ. The end-of-scan signal appears synchronized with the ϕ2 timing immediately after the last pixel is scanned, and is available to an external device from the EOS terminal via a buffer.

Note the following points when selecting circuit components.

(a) First-stage amplifier
As a first-stage amplifier, choose an amplifier having low noise and less leaks while taking the switching speed into account.

(b) Second-stage, third-stage amplifiers
Choose an amplifier that is resistant to load capacitance.

(c) Reset switch and clamp switch
Use an FET or analog switch with low ON resistance and reset noise. Also take the signal voltage range into consideration.

(2) Supply voltage

Table 6-5 gives the recommended values for input supply voltage, input pulse amplitude voltage, output voltage and output pulse amplitude voltage.
The input supply voltage Vcc for digital circuitry is +5 V, and ±Vs for analog circuitry is ±15 V. The input pulses consist of a master clock pulse ϕmc and a master start pulse ϕms. These are positive going pulses and their amplitude voltages Vmc and Vms are both 5 V. The trigger pulse for external output is also a positive going output while the end-of-scan pulse is a negative going output. Their amplitude voltages Vtrig and Veos are also 5 V. The data video output from the last stage is obtained with positive polarity with respect to ground, while the monitor video output used for adjustment of switching noise cancellation is available as a positive going signal with respect to approximately 2 V.
Voltages actually applied to the image sensor are as follows: The amplitude of the clock pulses Vϕ1 and Vϕ2, and start pulse Vϕst are 5 V; the video bias voltage Vb that determines the photodiode reset voltage is 2 V; the saturation control gate voltage Vscg is 0 V; the saturation control drain voltage Vscd is 2 V which is equal to the video line bias voltage Vb. The Vss, Vsub and NC terminals are all grounded. The dummy video output is not used with this circuit, so the dummy video output terminal is left open.

Table 6-5 Input/outupt voltages for recommended current-to-voltage conversion circuit

Input or output voltage		Symbol	Min.	Typ.	Max.	Unit
Input	Supply voltage for digital circuitry	Vd	4.85	5	5.5	V
	Supply voltage for analog circuitry	Va	±14.5	±15	±15.5	
	Mater start pulse ϕms	Vms (H)	2	5	5.4	
		Vms (L)	0	-	0.8	
	Master clock pulse ϕmc	Vmc (H)	2	5	5.4	
		Vmc (L)	0	-	0.8	
Output	Trigger pulse	Vtrig (H)	4.75	5	5.4	
		Vtrig (L)	-	-	0.4	
	End-of-scan pulse	Veos (H)	4.75	5	5.4	
		Veos (L)	-	-	0.4	
Output for image sensor	Start pulse ϕst	Vϕs (H)	4.75	5	5.4	
		Vϕs (L)	-	-	0.4	
	Clock pulse ϕ1, ϕ2	Vϕ1, Vϕ2 (H)	4.75	5	5.4	
		Vϕ1, Vϕ2 (L)	-	-	0.4	
	Video bias voltage	Vb	-	2	-	
	Saturation control drain voltage	Vscd	-	2	-	
	Saturation control gate voltage	Vscg	-	0	-	

(3) Pulse timing

The input/output pulse timing diagram for a recommended circuit is shown in Figure 6-8, along with output pulse timing for the image sensor. Pulse timing conditions are also shown in Table 6-6.

The input pulses to the image sensor are supplied from the PLD at regular cycles, with minimum units of one cycle of the master clock pulse ϕmc.

The start pulse ϕst for the image sensor is produced in synchronization with the rise of the master start pulse ϕms, with a duration equal to two cycles of the master clock pulse ϕmc. Thus the master start pulse interval corresponds to the signal integration time, which is the reciprocal of the master start pulse frequency fϕms, that is, 1/fϕms (s). To ensure stable start operation, the master start pulse width tpwϕms should be longer than the master clock pulse width tpwϕmc of one cycle, and they also should be synchronized.

This driver circuit is designed to read out one pixel in a duration equal to 4 cycles of the master clock pulse ϕmc. Within this duration, the output signal readout, integration capacitance reset and output potential clamping are performed. Therefore, all pulses other than the start pulse are generated at this cycle to produce the time-series output signal from each pixel. This means that the output signal readout frequency is 1/4th of the master clock pulse frequency fϕmc. Taking account of the relation between the integration reset time, clamp period and other characteristics, the maximum readout frequency for this driver circuit is specified as 62.5 kHz.

The clock pulses ϕ1 and ϕ2 for the sensor are set to a high level with pulse widths equal to two cycles of the master clock pulse. The signal output is obtained in synchronization with the ϕ2 timing. The timings of the start pulse ϕst and clock pulses ϕ1 and ϕ2 are shown in Figure 6-8.

Accompanying the on/off operations of address switches or integration capacitance reset switches, switching noise appears in the output signal synchronized with the reset pulse ϕreset and clock pulse ϕ2. Since this noise is fixed pattern noise, it can be canceled out by injecting a charge equal to this noise component but in opposite phase, into the output signal component. More specifically, the inverted pulses of the reset pulse ϕreset and clock pulse ϕ2 are fed to the inverting input terminal of the integration amplifier via a CR coupled circuit. The amount of charge injection is adjusted with a variable resistor.

The clamping circuit eliminates noise generated by the reset switch in the integration amplifier as well as performing DC restoration of the output signal. This random reset noise is eliminated during the period between the end of reset operation for the integration capacitance and the signal output, in other words, while ϕreset is low but ϕ2 is high. If this period is too short, noise reduction may be insufficient. In this driver circuit, this period corresponds to one cycle of the master clock pulse.

Data acquisition timing for A/D conversion is set at a point one master clock pulse cycle after signal output. As Figure 6-6 shows, the trigger pulse for external output is set at this point, in other words, set to rise at a point 1/2 of the ϕ2 high level. Therefore, the data is acquired in synchronization with the rise of the trigger pulse.

The end-of-scan signal is output in synchronization with the ϕ2 timing immediately after the last pixel is read out.

(4) Connection

Figure 6-9 shows a wiring example of this driver circuit and peripheral devices. The power supplies (+5 V, ±15 V) should be connected to the respective power input terminals of the circuit, and the master start and master clock pulses from the pulse generator should be input to the St and CLK input terminals. The St terminal should also be connected to the external trigger input terminal of the oscilloscope. The data video output terminal (D.V.) and monitor video output terminal (M.V.) of this circuit should be connected to the input terminals (CH1, CH2)

Figure 6-8 Timing diagram for recommended external current-integration conversion circuit

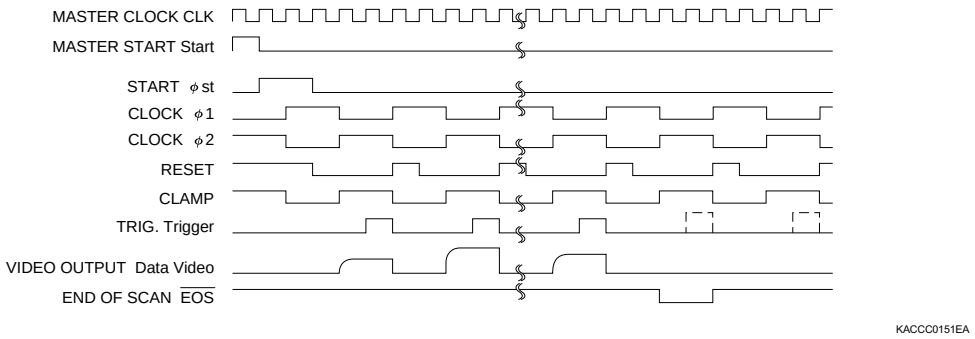


Table 6-6 Pulse timing conditions for recommended external-current integration circuit

Parameter		Symbol	Min.	Typ.	Max.	Unit
Input	Mater start pulse φms width	tpwφms	1/fφmc	-	-	s
	Mater start pulse φms rise time / fall time	trφms, tfφms	-	-	500	ns
	Master clock pulse φmc width	tpwφmc	30	-	-	
	Master clock pulse φmc rise time / fall time	trφmc, tfφmc	-	-	500	
	Master clock frequency	fφmc	-	-	375	kHz
Output	End of scan pulse width	tpweos	-	2/fφmc	-	s
	End of scan pulse rise time / fall time	treos, tfeos	-	-	100	ns
	Trigger pulse width	tpwtrig	-	1/fφmc	-	s
	Trigger pulse rise time / fall time	trtrig, tftrig	-	-	100	ns
Output for image sensor	Start pulse φst width	tpwφs	-	2/fφmc	-	s
	Start pulse φst rise time / fall time	trφs, tfφs	-	-	100	ns
	Clock pulse φ1 width	tpwφ1	-	2/fφmc	-	s
	Clock pulse φ2 width	tpwφ2	-	2/fφmc	-	
	Clock pulse φ1, φ2 rise time / fall time	trφ1, tfφ1, trφ2, tfφ2	-	-	100	ns

of the oscilloscope. The trigger output terminal (Trig) and data video output terminal (D.V.) of this circuit should be connected to the timing input terminal and analog input terminal of the S/H and A/D conversion circuit, respectively.
After all connections are complete, turn on the power to each device.

(5) Adjusting switching noise cancellation

As explained in the previous section “(3) Pulse timing” the switching noise appearing in the output can be canceled out by introducing φreset and φ2 at the inverting input terminal of the integration amplifier via a CR coupled circuit.
To make adjustment, first operate the image sensor under dark conditions and then observe the monitor video output on the oscilloscope. The monitor video output is a positive going signal with respect to 2 V, so switch the oscilloscope input selector to AC. In this state, adjust the variable resistors VR1 and VR2 shown in the circuit diagram of Figure 6-7 until switching noise synchronized with φreset and φ2 is minimized. The photographs in Figure 6-10 show the switching noise adjustment and saturated output state as displayed on the oscilloscope.

Figure 6-9 Wiring example (recommended external current integration circuit)

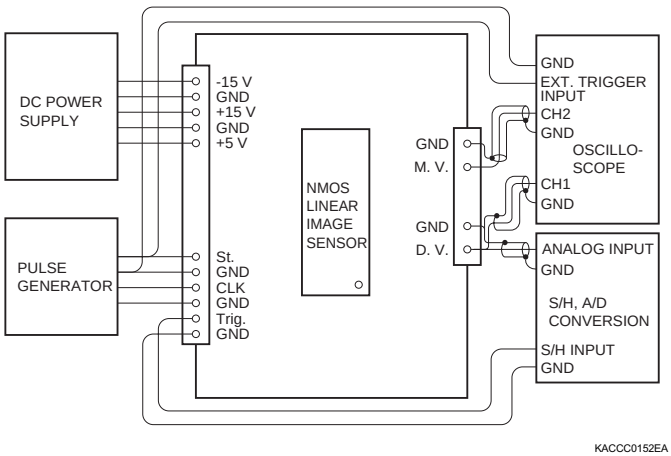
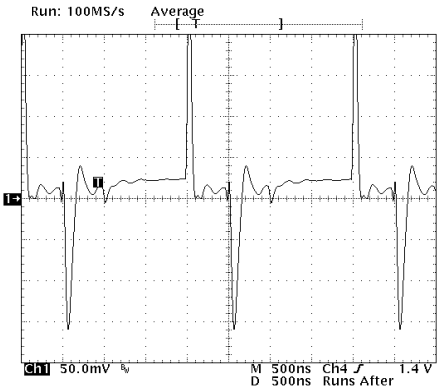
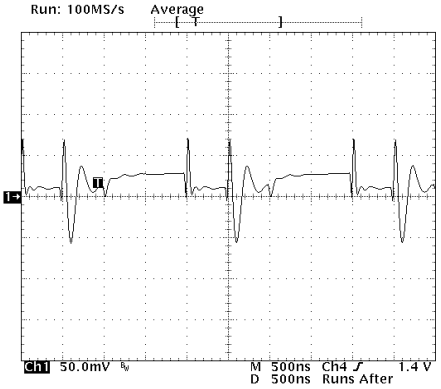


Figure 6-10 Adjustment and saturated output of external current-integration circuit

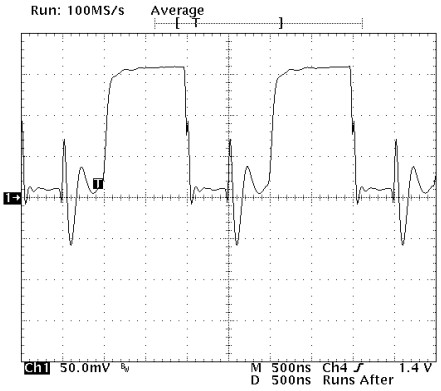
(a) Before VR1 adjustment



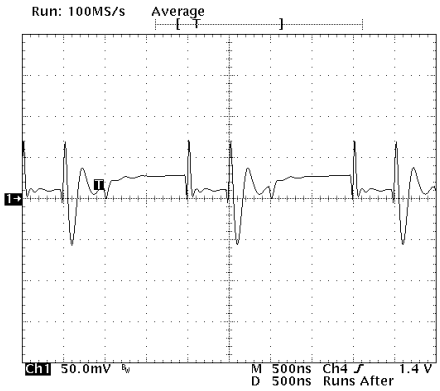
(b) After VR1 adjustment



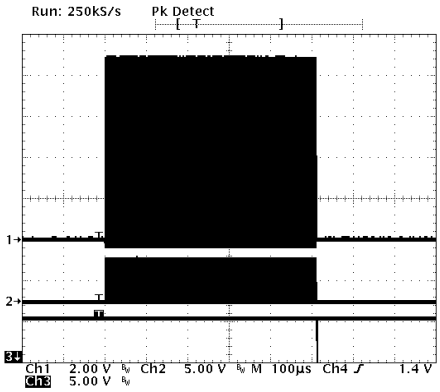
(c) Before VR2 adjustment



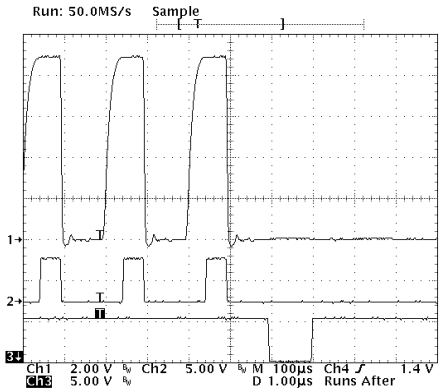
(d) After VR2 adjustment



(e) Saturated output



(f) Enlarged view near EOS pulse



(6) Caution items

If operation is abnormal, check the following points.

(a) Are correct voltages (+5 V, ±15 V) supplied to the circuit board?
(b) Are the specified master clock and master start pulses input to the circuit board?
(c) Are the clock pulses ϕ1, ϕ2 and start pulse ϕst being supplied to the image sensor socket pins?
(d) Is the end-of-scan (EOS) signal being output?

6-2. Driver circuit for voltage output type image sensor

(1) Circuit configuration

This type of driver circuit basically consists of a control signal generator and a video signal processor. Figures 6-11 and 6-12 show the block diagram and circuit diagram of a recommended driver circuit. The control signal generator produces various control pulses required for the image sensor and external signal processor. The video signal processor performs inverting amplification and DC restoration of the image sensor video signal and then outputs the processed signal. By applying external supply voltages for digital and analog circuitry, and also master clock and master start pulses, this driver circuit provides a data video output, trigger pulse and end-of-scan (EOS) pulse. Table 6-7 gives a description of the input/output terminals.

The control signal generator consists of a PLD (programmable logic device), and generates a start pulse and two-phase clock pulses to operate the shift register and also a reset signal for internal signal processing. The control signal generator also provides a trigger signal for external sample-and-hold and outputs it via a buffer. These signals are synchronized with an external master clock pulse, and are initialized by an external master start pulse. The master clock and master start pulses are input to the PLD via a buffer.

The video signal processor consists of a non-inverting amplifier and an inverting amplifier. Image sensors to be used with this driver circuit incorporate a signal processing circuit comprised of a current integration circuit utilizing video line capacitance and an impedance conversion circuit. If a load (resistance or capacitance) is added to the sensor video line, stable sensor operation cannot be maintained, so this signal should be input to the non-inverting terminal of the first-stage amplifier. However, the image sensor provides a negative going, boxcar waveform output with respect to a certain positive potential. The output signal must therefore be transformed into a signal with positive polarity with respect to ground, in order to make signal processing easy by an external circuit. In this driver circuit, the video signal is next fed to the inverting input terminal of the second-stage amplifier while the non-inverting input terminal is biased at a positive potential. The offset can be compensated by adjusting this bias voltage, and the output will be a positive

Figure 6-11 Block diagram of driver circuit for voltage output type image sensor

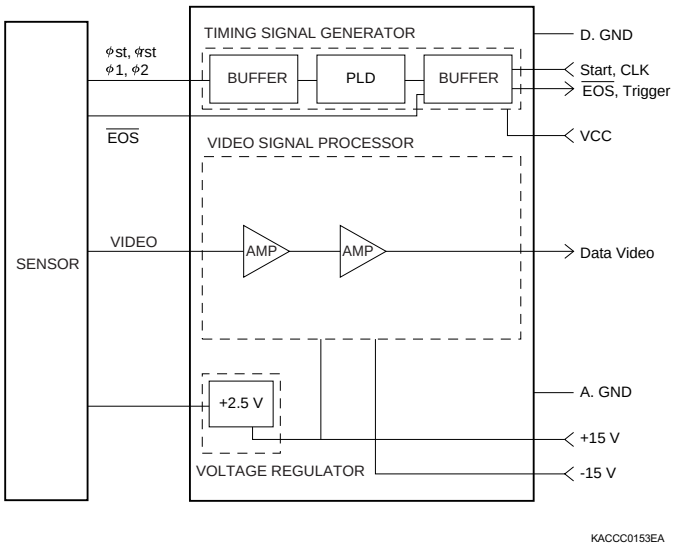


Figure 6-12 Recommended driver circuit for voltage output type image sensor

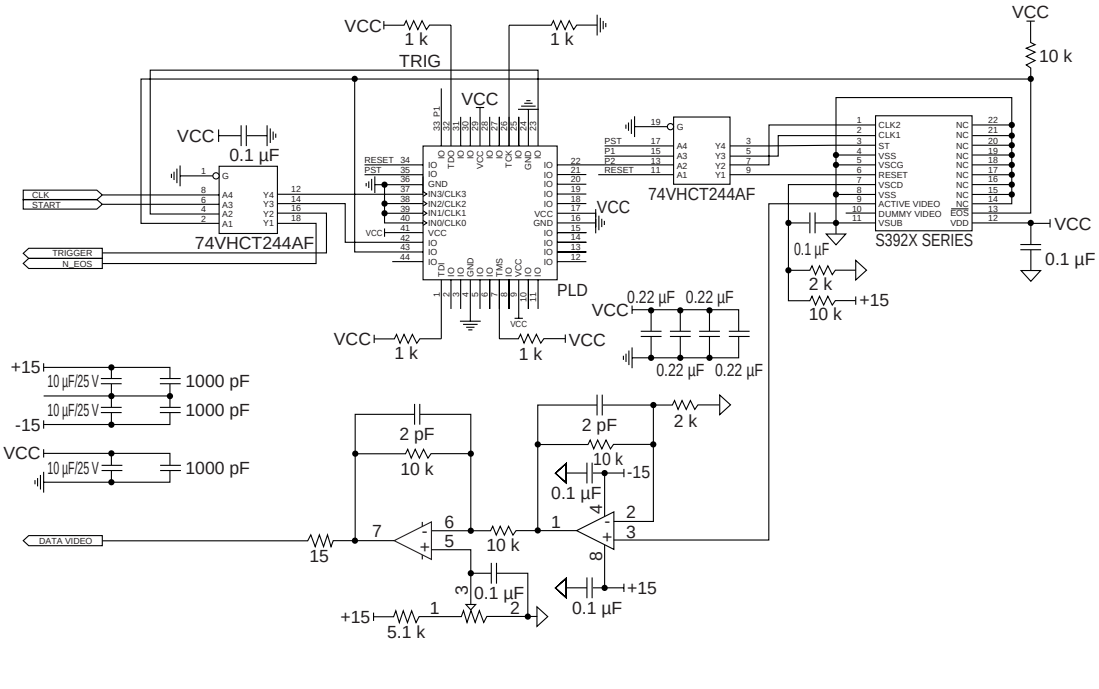


Table 6-7 Input/output terminal description of driver circuit for voltage output type image sensors

Terminal name		Symbol on board	Polarity	Function
Input	Supply voltage Vd (for digital circuitry)	+5	-	+5 V, 70 mA
	Supply voltage Va (for analog circuitry)	+15	-	+15 V, 30 mA
		-15	-	-15 V, 30 mA
	Master start pulse ϕms	START	Positive	Initializes internally generated pulse; C-MOS logic compatible.
	Master clock pulse ϕmc	CLK	Positive	Synchronies internally generated pulse; CMOS logic compatible.
	Ground	G	-	Ground.
Output	Video	Video	Positive	Video output.
	Trigger pulse	Trig.	Positive	A/D conversion timing signal; CMOS logic compatible.
	End-of-scan pulse	EOS	Negative	End-of-scan signal for shirt register; CMOS logic compatible.

signal with respect to ground. The output signal is amplified 6 times by these two amplifiers and derived from the video output terminal.

The end-of-scan (EOS) terminal is pulled up at 5 V, with a resistor of 10 kΩ. The end-of-scan signal appears synchronized with the ϕ2 timing immediately after the last pixel is scanned, and is available for an external device from the EOS terminal via the buffer.

Note the following points when selecting amplifiers.

(a) Non-inverting amplifier

Choose a high-speed operational amplifier with low noise.

(b) Inverting amplifier

Choose a high-speed operational amplifier that is resistant to load capacitance.

(2) Supply voltage

Table 6-8 shows the recommended values of input supply voltage, input pulse amplitude voltage, output voltage and output pulse amplitude voltage.

The input supply voltage Vd for digital circuitry is +5 V, and Va for analog circuitry is ±15 V. The input pulses consist of a master clock pulse ϕmc and a master start pulse ϕms. These are positive going outputs and their amplitude voltages Vmc and Vms are both 5 V. The trigger pulse for external output is a positive going output while the end-of-scan pulse is a negative going output. Their amplitude voltages Vtrig and Veos are also 5 V. The final data video output obtained has a positive polarity with respect to the ground.

Table 6-8 Input/output voltages for recommended driver circuit designed for voltage output type image sensors

Input or output voltage		Symbol	Min.	Typ.	Max.	Unit
Input	Supply voltage for digital circuitry	Vd	4.85	5	5.5	V
	Supply voltage for analog circuitry	Va	±14.5	±15	±15.5	
	Mater start pulse ϕms	Vms (H)	2	5	5.4	
		Vms (L)	0	-	0.8	
	Master clock pulse ϕmc	Vmc (H)	2	5	5.4	
		Vmc (L)	0	-	0.8	
Output	Trigger pulse	Vtrig (H)	4.75	5	5.4	
		Vtrig (L)	-	-	0.4	
	End-of-scan pulse	Veos (H)	4.75	5	5.4	
		Veos (L)	-	-	0.4	
Output for image sensor	Start pulse ϕst	Vs (H)	4.75	5	5.4	
		Vs (L)	-	-	0.4	
	Clock pulse ϕ1, ϕ2	Vϕ1, Vϕ2 (H)	4.75	5	5.4	
		Vϕ1, Vϕ2 (L)	-	-	0.4	
	Reset pulse ϕr	Vr (H)	4.75	5	5.4	
		Vr (L)	-	-	0.4	
	Reset voltage	Vr	-	2.5	-	
	Saturation control drain voltage	Vscd	-	2.5	-	
	Saturation control gate voltage	Vscg	-	0	-	
	Internal output processing circuit drain voltage	Vdd	-	5	-	

Voltages actually applied to the image sensor are as follows: The amplitude of the clock pulses Vϕ1 and Vϕ2, start pulse Vϕst, and reset pulse Vϕr are 5 V; the reset voltage Vr that determines the photodiode reset potential is 2.5 V; the saturation control gate voltage Vscg is 0 V; the saturation control drain voltage Vscd is 2.5 V which is equal to the reset voltage Vr; the supply voltage Vdd for the drain of the internal signal processor is 5 V. The Vss, Vsub and NC terminals are all grounded. The dummy video output is not used with this circuit, so the dummy video output terminal is left open.

(3) Pulse timing

The input/output pulse timing diagram for this driver circuit is shown in Figure 6-13, along with its output pulse timing for the image sensor. The pulse timing conditions are listed in Table 6-9.

The input pulses to the image sensor are supplied from the PLD at regular cycles, with minimum units of one cycle of the master clock pulse ϕmc. The start pulse ϕst for the image sensor is produced in synchronization with the fall of the master start pulse ϕms, with a duration equal to two cycles of the master clock pulse ϕmc. Thus the master start pulse interval corresponds to the signal integration time, which is the reciprocal of the master start pulse frequency fϕms, that is 1/fϕms (s). To ensure stable start operation, the master start pulse width tpwϕms should be longer than the master clock pulse width tpwϕmc of one cycle.

This driver circuit is designed to read out one pixel in a period equal to 6 cycles of the master clock pulse ϕmc. Both the readout for one pixel and the reset for the photodiode and video line are performed in this period. For this reason, all pulses other

Figure 6-13 Timing diagram of recommended driver circuit for voltage output type image sensor

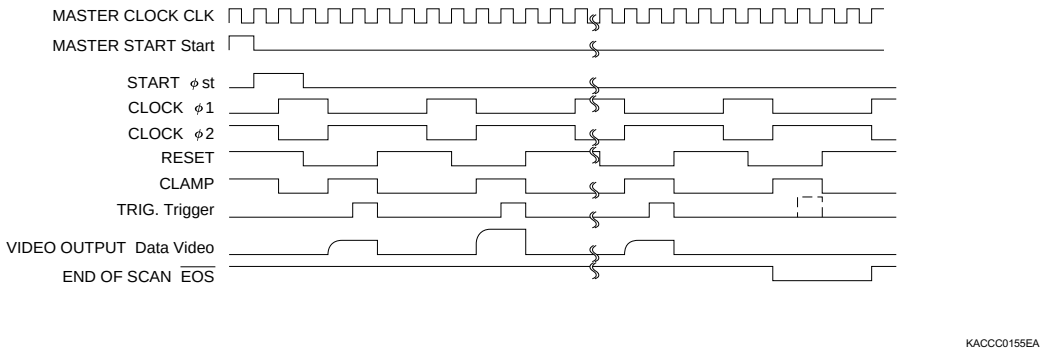


Table 6-9 Pulse timing conditions for recommended driver circuit for voltage output type image sensor

Parameter		Symbol	Min.	Typ.	Max.	Unit
Input	Mater start pulse ϕms width	tpwϕms	1/fϕmc	-	-	s
	Mater start pulse ϕms rise time / fall time	trϕms, tfϕms	-	-	500	ns
	Master clock pulse ϕmc width	tpwϕmc	30	-	-	
	Master clock pulse ϕmc rise time / fall time	trϕmc, tfϕmc	-	-	500	
	Master clock frequency	fϕmc	-	-	3	MHz
Output	End of scan pulse width	tpweos	-	4/fϕmc	-	s
	End of scan pulse rise time / fall time	treos, tfeos	-	-	100	ns
	Trigger pulse width	tpwtrig	-	3/fϕmc	-	s
	Trigger pulse rise time / fall time	trtrig, tftrig	-	-	100	ns
Output for image sensor	Start pulse ϕst width	tpwϕs	-	2/fϕmc	-	s
	Start pulse ϕst rise time / fall time	trϕs, tfϕs	-	-	100	ns
	Clock pulse ϕ1 width	tpwϕ1	-	2/fϕmc	-	s
	Clock pulse ϕ2 width	tpwϕ2	-	4/fϕmc	-	
	Clock pulse ϕ1, ϕ2 rise time / fall time	trϕ1, tfϕ1, trϕ2, tfϕ2	-	-	100	ns
	Reset pulse ϕr width	tpwϕr	-	3/fϕmc	-	s
	Reset pulse ϕr rise time / fall time	trϕr, tfϕr	-	-	100	ns
	Reset pulse ϕ2 overlap times	tϕovr	-	2/fϕmc	-	
	Reset pulse rise time to ϕ2 fall time difference	tdϕ-2	-	1/fϕmc	-	

than the start pulse are generated at this cycle to produce the time-series output signal of each pixel. This means that the output signal readout frequency is 1/6th of the master clock pulse frequency fϕmc. Taking account of the relation between the photodiode reset time and other characteristics, the maximum readout frequency for this driver circuit is specified as 500 kHz.

The clock pulses ϕ1 and ϕ2 are in a complementary relation. Both pulses are set to a high level with a pulse width respectively equal to two and four cycles of the master clock pulse. The signal output is obtained in synchronization with the ϕ2 timing. The timing of the start pulse ϕst and clock pulses ϕ1 and ϕ2 are also shown in Figure 6-13.

The photodiode potential is reset by simultaneously turning on the address switch and the reset switch for internal signal processing circuit so that the photodiode potential is set equal to the reset voltage Vr. Since the address switch operates synchronized with the clock pulse ϕ2, the reset pulse ϕr must overlap with ϕ2. In this driver circuit operation, the reset pulse ϕr sets to high level for a period equal to three cycles of the master clock pulse and the two cycles of them are overlapped with ϕ2. To maintain the photodiode reset potential at a constant value, the reset pulse ϕr falls one master clock cycle earlier than the rise of ϕ2. The timing diagram of reset pulse ϕr is also shown in Figure 6-13. The video output signal is obtained between the rise of ϕ2 and the rise of ϕr.

Data acquisition timing for A/D conversion in this driver circuit is set at a point one master clock pulse cycle after the signal output. As shown in Figure 6-13, the trigger pulse for external output is set to rise at a point 1/4th of the ϕ2 high level. Data is therefore acquired in synchronization with the rise of the trigger pulse.

The end-of-scan signal is output in synchronization with the ϕ2 timing immediately after the last pixel is read out.

(4) Connections

Figure 6-14 shows a wiring example for this driver circuit and peripheral devices. The power supplies (+5 V, ±15 V) should be connected to their respective power input terminals of the circuit, and the master start and master clock pulses from the pulse generator should be input to the St and CLK input terminals. The St terminal is also connected to the external trigger input terminal of the oscilloscope and the data video output (Video) is input to the oscilloscope. The trigger output terminal (Trig) and data video output terminal (Video) of this circuit should be connected respectively to the timing input terminal and analog input terminal of the S/H and A/D conversion circuit.

(5) Adjusting the output offset level

As explained in the previous section “(1) Circuit configuration”, the video output offset level can be adjusted by varying the voltage applied to the non-inverting input terminal of the inverting amplifier. This adjustment is made by using a variable resistor shown in the recommended driver circuit diagram.

To make this adjustment, first operate the image sensor under dark conditions and then observe the video output on the oscilloscope. Adjust the variable resistor so that the output level during the ϕ2 high and ϕr low levels are set to ground level as shown in oscilloscope photographs of Figure 6-15.

Figure 6-14 Wiring example (recommended driver circuit for voltage output type)

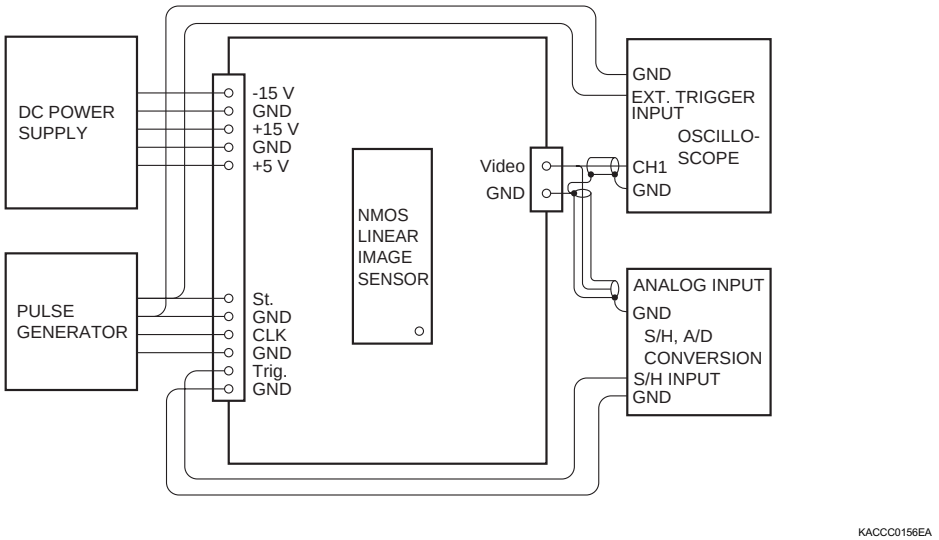
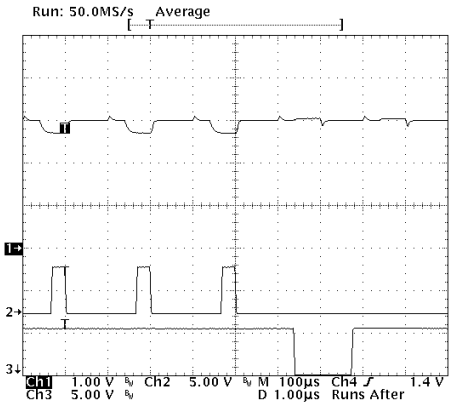
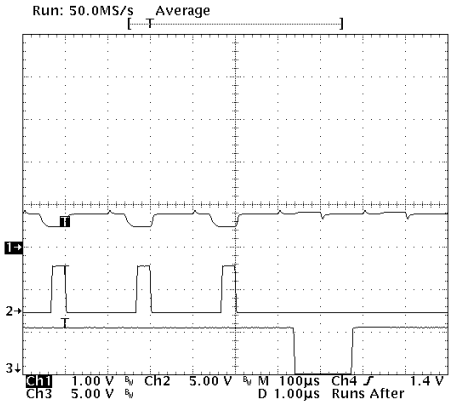


Figure 6-15 Offset adjustment and saturated output of driver circuit for voltage output type sensor

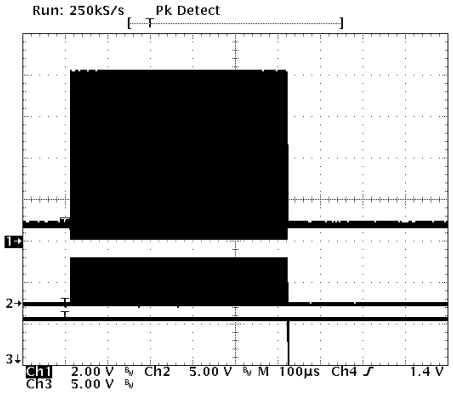
(a) Before offset adjustment



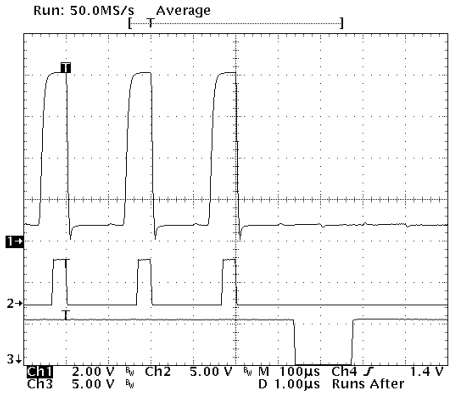
(b) After offset adjustment



(c) Saturated output



(d) Enlarged view near EOS pulse



(6) Caution points

If operation is abnormal, check the following points.

(1) Are correct voltages (+5 V, ±15 V) being supplied to the circuit board?
(2) Are the specified master clock and master start pulses input to the circuit board?
(3) Are the clock pulses ϕ1, ϕ2 and start pulse ϕst being supplied to the image sensor socket pins?
(4) Is the end-of-scan (EOS) signal being output?

6-3. Pulse generator

(1) Circuit configuration

Figure 6-16 shows the circuit diagram of a recommended pulse generator. By applying an external supply voltage of 5 V (30 mA), this pulse generator provides a master clock pulse and master start pulse outputs. Since a crystal oscillator is used as master clock, highly accurate pulse signals can be obtained. The master start pulse initializes the driver circuit and determines the integration time of the image sensor. The master clock pulse becomes a minimum pulse unit originated in the PLD and also determines the image sensor operating time (data rate).

Figure 6-17 shows timing diagrams for the master clock and master start pulses. The master start pulse width is set twice as long as the master clock pulse width.

(2) Master clock pulse setting

To set the master clock pulse, use the rotary switch SW-CLK. The original clock frequency is divided by the PLD.

(3) Master start pulse interval setting

To set the master clock pulse interval, use the rotary switch SW-START and slide switch SW-125.

This master start pulse interval corresponds to the integration time. Since integration time = X ×10^{Y} (s), the PLD should be programmed so that X can be set with SW-125 and Y with SW-START.

Figure 6-16 Recommended pulse generator circuit

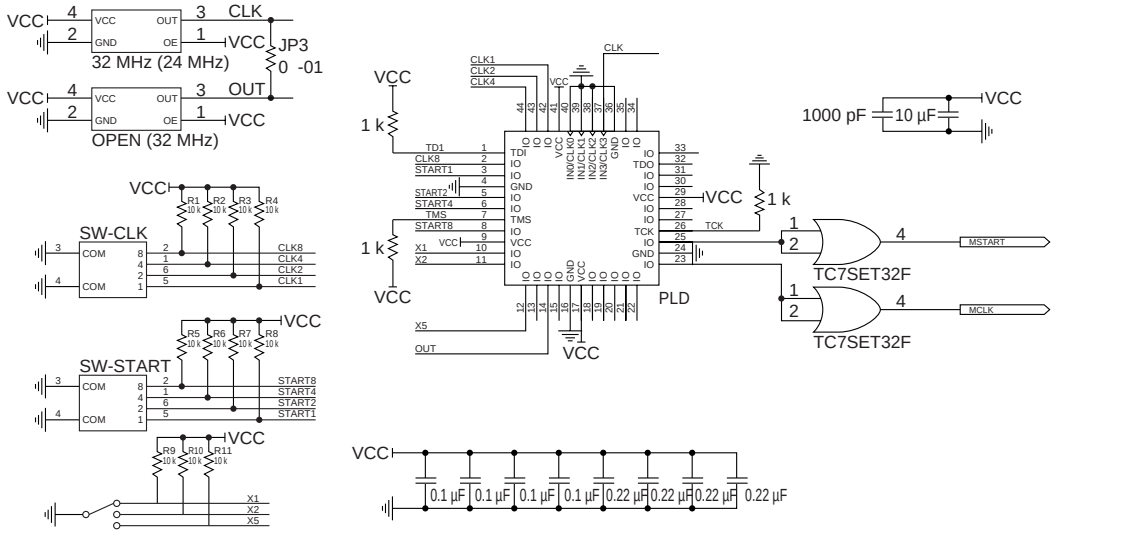
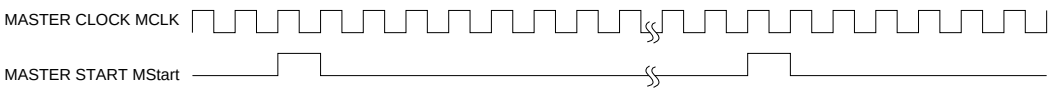


Figure 6-17 Timing diagram for recommended pulse generator circuit



7. Reliability

Hamamatsu NMOS linear image sensors are subjected to reliability testing based on Japanese Industrial Standard (JIS), with EIAJ (Japan Electronic Machinery Association) and MIL (U.S. military) standards also being taken into account as well. Reliability testing of items listed in Table 7-1 is periodically performed.

Table 7-1 Reliability testing for NMOS linear image sensors

Tested item	Conditions
High temperature storage	85 °C (Tstg Max.) for 1000 hours
High temperature operation	65 °C (Topr Max.) at Vϕ = 10 V for 1000 hours
High temperature and High humidity operation	60 °C, 90 %, Vϕ = 10 V (Clock voltage Max.) 1000 hours
Temperature Cycling (storage)	-40 °C for 30 minutes to 85 °C for 30 minutes, 100 cycles (Tstg Min. to Tstg Max.)
Shock	100 G for 6 ms, XYZ directions, 3 times each
Vibration	100 to 2000 Hz, 20 G, XYZ directions, 48 minutes
Terminal strength	Puling 0.5 kg for 30 seconds, bending 90 ° two times
Static electricity damage	C = 200 pF, R = 0 Ω, ±200 V, between all adjacent terminals

NOTE: Criteria for reliability testing are based on the maximum or minimum performance values listed in our catalog.

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