Anritsu Advancing beyond

Signal Quality Analyzer-R

PCIe/USB/Thunderbolt Test Solutions*

MP1900A

SQA-R

*: Refer to the 32G/64G NRZ/PAM4 Signal Integrity Test Solution Catalog (MP1900A_64G-E-A-1) for the information on MP1900A PAM4 test solution.

Excellent Eco Product

Support 400 GbE/800 GbE and PCIe Gen5/6

Due to the explosive growth of data traffic resulting from the popularity of smartphones and mobile terminals, network interfaces are transitioning to faster 200 GbE/400 GbE standards, and PCI bus interface speeds now exceed 10G. In addition, the equipment and chipsets using these interfaces support multi-channels and multi-protocols.
The MP1900A is a high-performance BERT with excellent expandability for supporting Physical layer evaluations of these high-speed interfaces. The all-in-one design is ideal for early stage R&D evaluations of all interfaces covering next-generation Ethernet networks to bus interconnects.

MP1900A
Signal Quality Analyzer-R

SQA-R

- Certified for PCIe Gen 3/4/5 USB3.2 Thunderbolt3
- PCIe Gen6 Base Test Ready
- PCIe/USB3.2 Sequence Editor for Troubleshooting
- USB4 USB3.2 ×2 Compliance Test Ready

Excellent Expandability

All-in-one support for both high-speed Ethernet and PCI Express interface tests

Supports transmissions up to 512 Gbit/s
• 32G bandwidth : 16ch NRZ, 8ch PAM4
• 64G bandwidth : 4ch NRZ, 4ch PAM4

8 slots for adding extra modules

Backwards compatibility with MP1800A series modules

Signal Integrity Evaluation

10Tap Emphasis built-in
Variable ISI Function
Multi-band CTLE
CDR Function (supports SSC)
Jitter Addition (SJ/RJ/BUJ/SSC) function
User-defined SSC profile function
Voltage Noise Addition (CM/DM/Gaussian) function

Link Training

Receiver tests are supported by the built-in Protocol Awareness PCIe Link Training, USB Link Training and LTSSM analysis functions.

Supports PCI Express Gen 1/2/3/4/5
Supports both USB 3.2 Gen1/2 ×1 and ×2

Supports Link Training troubleshooting using Sequence Editor

High Waveform Quality and High Sensitivity

Low Intrinsic (Residual) Jitter output (115 fs rms)
High-sensitivity Data input (15 mV)
Operation bit rates from 2.4 Gbit/s to 32.1 Gbit/s

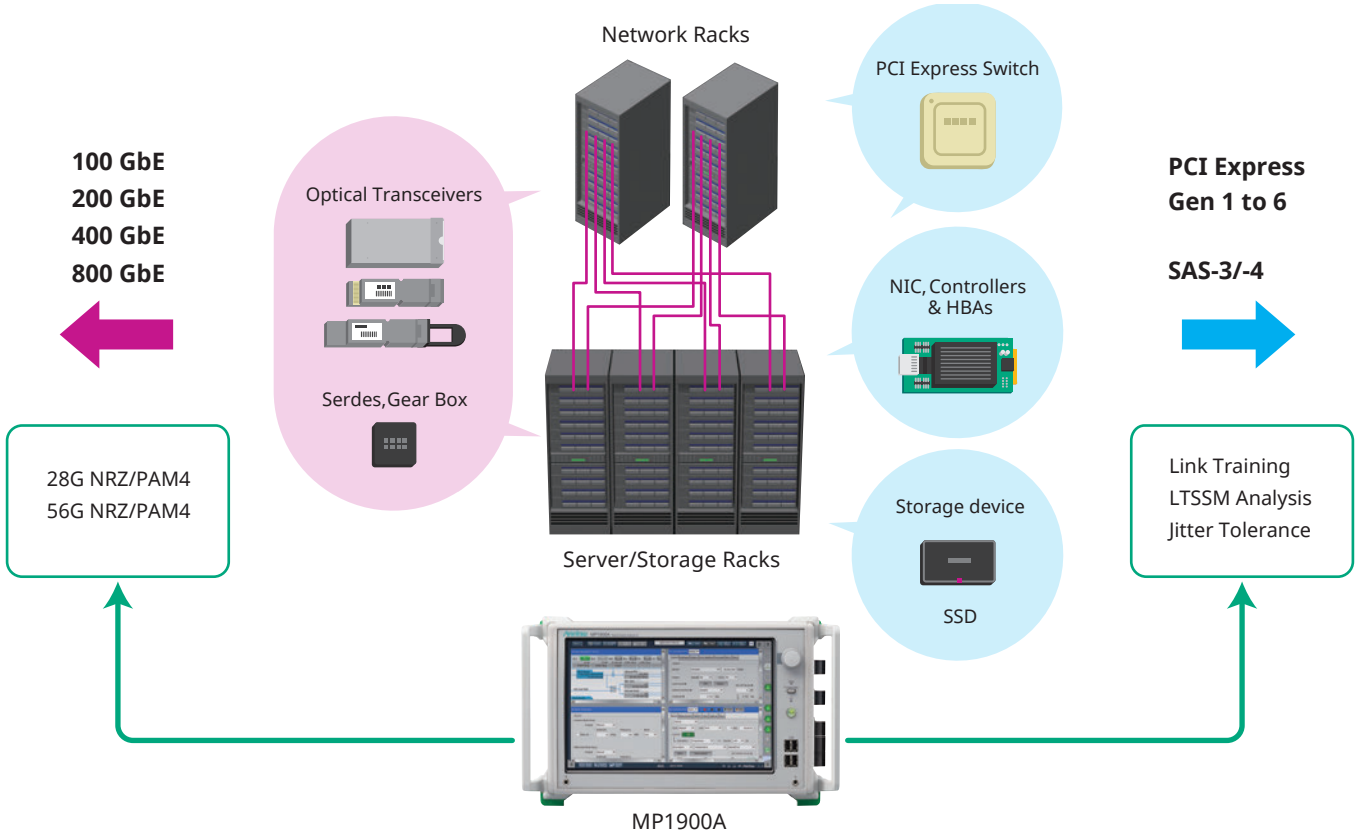
Wide Application Support

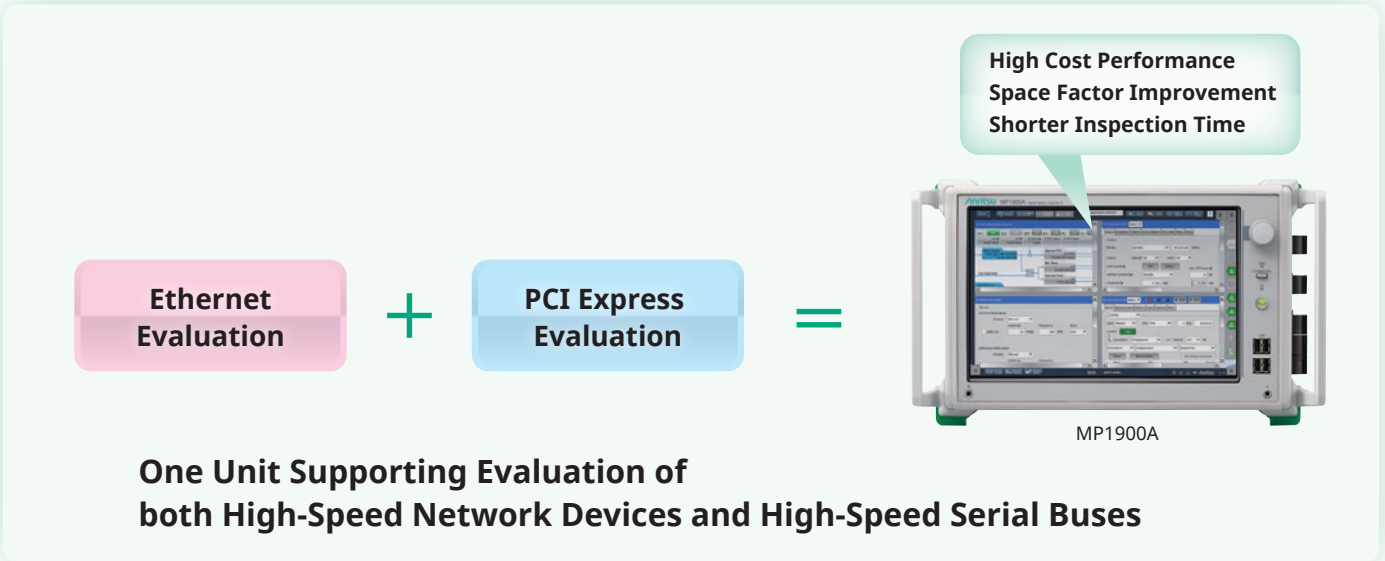
100 GbE/200 GbE/400 GbE/800 GbE, CEI-25G/28G/56G/112G, InfiniBand EDR/HDR, Fibre Channel
PCI Express Gen 1/2/3/4/5/6, Thunderbolt 1/2/3, USB3.2/4 Type C, SAS-3/-4, DP1.4
Optical module, SERDES, AOC, High-speed Interconnect

Excellent Expandability

All-in-One Support for Evaluating Next-Generation NRZ/PAM4 Network Interfaces and High-Speed Serial Buses

The Signal Quality Analyzer–R MP1900A is a modular Bit Error Rate Tester (BERT) supporting equipment external interfaces, such as next-generation Ethernet, by installing a pulse pattern generator (PPG) for outputting high-quality multi-channel NRZ/PAM4 signals over a wide bandwidth, a high-sensitivity input error detector (ED), Jitter modulation sources for Jitter Tolerance tests, etc.
Additionally, optional noise generation and 10Tap Emphasis functions can be installed for Voltage Noise Tolerance tests, etc., and installing the High-Speed Serial Data Test Software software enables efficient design evaluation for increasingly faster PCIe, USB, Thunderbolt, SAS and DP receivers.





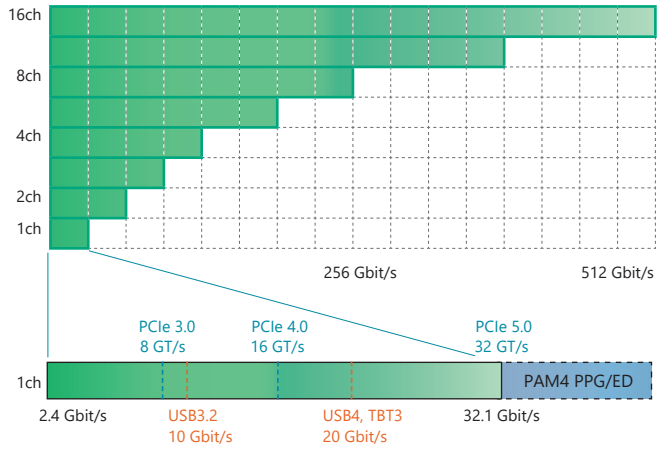
Excellent Expandability

Easy Flexibility for Multi-Channel Measurements at Various Transmission Rates and Formats

400 GbE is the standard for the next generation of large-capacity transmissions but it is still unknown how much further data traffic will grow. To cope with this data traffic growth, in addition to speeding-up NRZ signals and introducing multi-channel signalling, introduction of PAM4-format signals is also progressing. To facilitate this change to multi-channels and the new PAM4 signals, the MP1900A series is an 8-slot modular instrument that can be easily customized by selecting and adding required function modules. This flexible expandability supporting the latest communications methods ensures both efficient R&D investment and the fastest time to market.

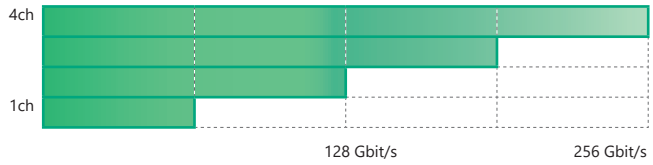
SI PPG/ED Module Expandability

• NRZ (Max. 32 Gbit/s at 1ch)

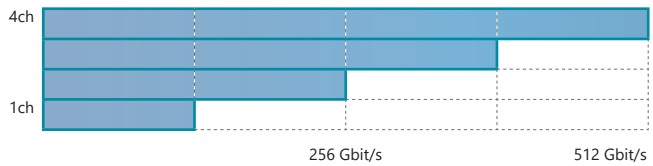


PAM4 PPG/ED Expandability*

• NRZ (Max. 64 Gbit/s at 1ch)



• PAM4 (Max. 64 Gbaud at 1ch)



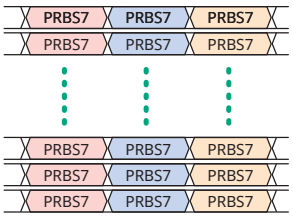
*: Refer to the 32G/64G NRZ/PAM4 Signal Integrity Test Solution Catalog (MP1900A_64G-E-A-1) for details of PAM4 PPG/ED.

In addition to installing PPG, ED, and noise-generation modules in the 8-slot main unit, existing modules for the previous MP1800A series can also be installed. The 21G/32G bit/s SI PPG/ED modules support selection of both one and two channels, enabling up to 16-channel measurement for both the PPG and ED. The PAM4 PPG and ED modules can be installed simultaneously to support up to a 4ch PPG and 4ch ED in a one channel per module configuration. Moreover, the pattern for each channel can be synchronized, providing an ideal solution for evaluating DAC, MUX and DEMUX devices as well as for crosstalk and skew tolerance tests.

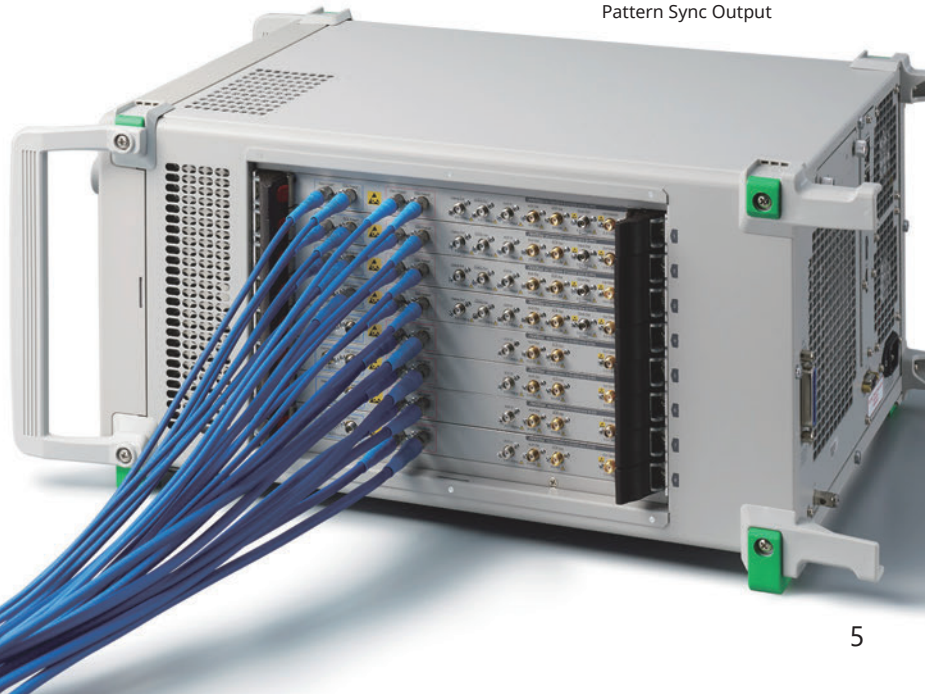
*: Refer to the MP1900A Selection Guide (MP1900A-E-Z-1) for details of the supported multi-channel configurations and module combinations. Consult our business sales representative for use of other module configurations not described in the MP1900A Selection Guide.

MP1900A

Differential
16ch



Pattern Sync Output



Multi Interface

Next-Generation High-Speed Digital Interface Receiver Test

The growth of IoT and Cloud computing applications is driving the need for digital equipment with high-speed serial interfaces handling large data volumes. To meet this need, the PCI Express (PCIe) and USB interfaces used by this digital equipment are transitioning to both next-generation PCIe Gen5 supporting speeds up to 32 GT/s as well as to Type-C USB3.2 Gen2 supporting 10 Gbit/s and USB4 supporting 20 Gbit/s, which is also compatible with Thunderbolt.

The MP1900A is a wideband BERT with a built-in Gbit/s-class PPG, ED, and Jitter/Noise addition functions as well as application software supporting measurement of next-generation, high-speed digital-interface standards (CEI-28G/56G/112G, InfiniBand, 100G/400G/800G Ethernet, Fibre Channel, Thunderbolt 3, PCIe, USB, SAS, DP) from development through to manufacturing.

All-in-One Test Support

MP1900A

PCIe Gen3/4/5 Receiver Test
Base Specification
- Stressed Eye Test

CEM Specification
- Transmitter initial Tx Equalization
- Transmitter Link Equalization response
- Receiver Link Equalization
- PLL Bandwidth

USB Type-C Receiver Test (USB4, Thunderbolt3, DP1.4)
Receiver Test
SJ Margin Test
Amplitude Margin Test

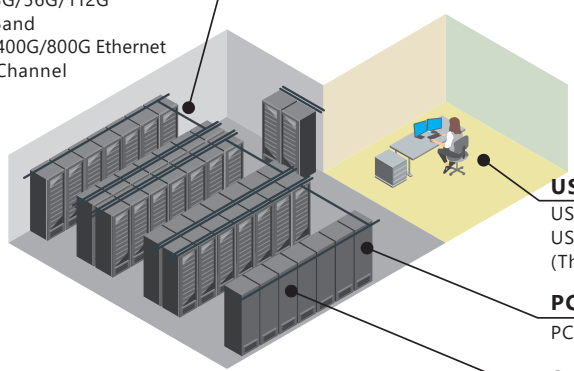
USB 3.2 Gen1/2 Receiver Test
Transmitter Eye Test
Receiver Jitter Tolerance Test

Storage Receiver Test (SAS-3/-4)
Receiver Jitter Tolerance Test

Jitter Tolerance Test
SJ/RJ/BUJ Injection
Low-rate estimated BER measurement

Target Applications

General Interfaces
CEI-28G/56G/112G
InfiniBand
100G/400G/800G Ethernet
Fibre Channel



USB
USB3.2、4
USB Type-C
(Thunderbolt3 DP1.4)

PCI Express
PCIe-Gen1, 2, 3, 4, 5, 6

Storage Device
SAS-3/-4

Various Applications

Internal and external interfaces, such as Ethernet, PCIe, and SAS, are supported along with USB3.2, 3.4, and Thunderbolt via USB Type-C connectors and cables, and Display Port.

MP1900A supports PCIe 3.0, 4.0 and 5.0 as well as SAS using the same configuration.

Full Automation

Full Automation Software

Automation software for automating receiver tests of high-speed serial bus interfaces controls the MP1900A (PPG/ED, noise signal source, variable ISI channel) and real-time oscilloscope to automate calibration of signals required for complex operations, Jitter Tolerance tests, and creation of reports. The high-reproducibility, easy measurements greatly reduce the work load of test engineers.

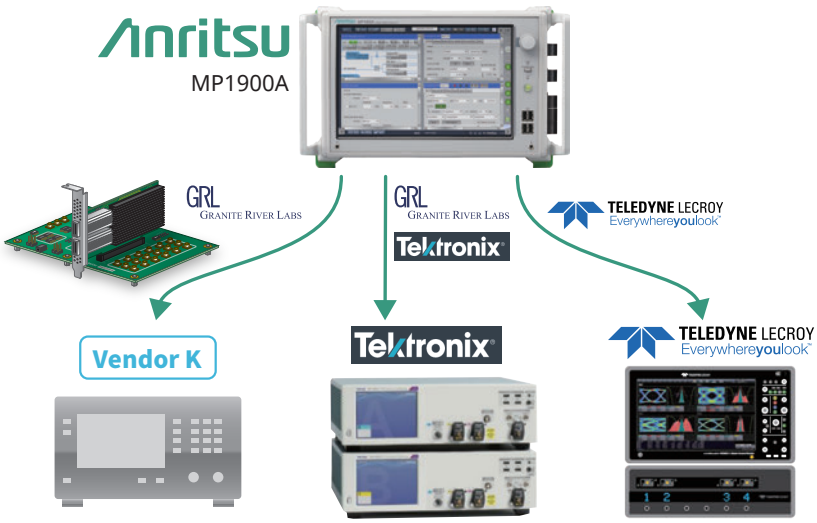
Features

- Controls each measuring instrument to simplify calibration, measurement conditions settings, and test execution
- Calibrates test signal and executes receiver test with high reproducibility
- Automates standards-compliant Jitter and amplitude Pass/Fail evaluations
- Selectable Various Oscilloscope

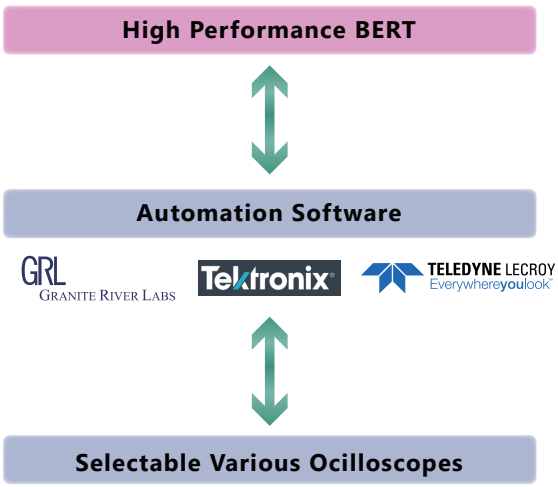
Selectable Various Oscilloscope

Real-time oscilloscopes from the main makers can be used in combination with the MP1900A to calibrate test signals, helping cut capital investment costs by making efficient use of owned assets.

Refer to the Selection Guide (MP1900A-E-Z-1) for the combination of supported real-time oscilloscopes and automation software.



Customers' Real-Time Oscilloscope

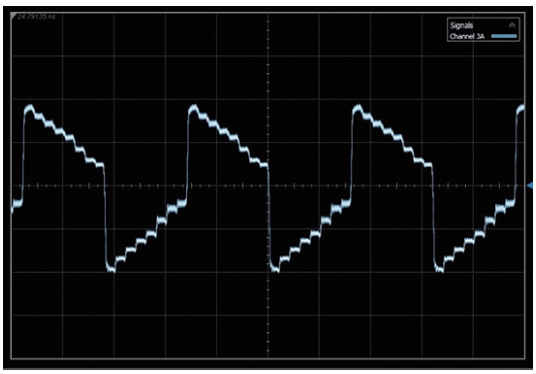


Strengthened Signal Integrity Evaluations in Addition to New SI PPG, SI ED and Noise Generator Modules

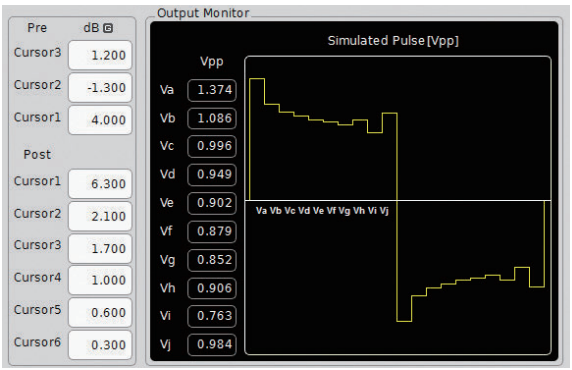
Emphasis and equalizer functions are built-in to correct transmission path losses and assure signal integrity as signals become faster and as high-speed devices use lower signal levels to help reduce power consumption.

10Tap Emphasis

The 10Tap Emphasis option installed in the transmission-side21G/32 Gbit/s SI PPG MU195020A can accurately replay simulated waveforms for various devices and channels (corrected for loss after passage through channel) to help improve design efficiency.



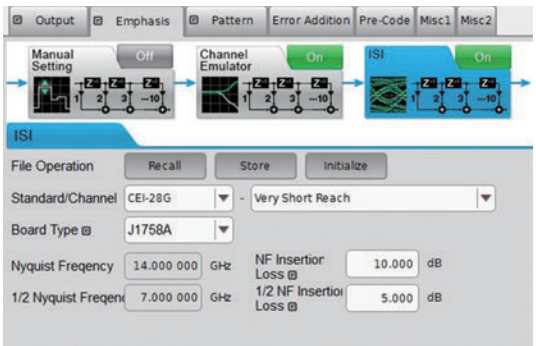
Waveform adjustment using 10Tap Emphasis Function



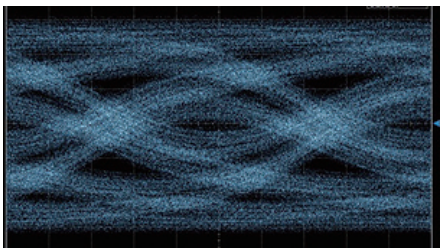
Emphasis Setting Screen Example

Additionally, the Variable ISI (option) can generate a signal with simulated Loss between the Tx and Rx channels of high-speed devices by setting the channel Loss for the frequencies defined in CEI-28 G/25G and the S-parameter information, and can also easily output a Loss-corrected waveforms. As a result, channel-Loss dependent high-speed device performance tests can be run easily with good reproducibility without needing to prototype multiple channel boards, helping cut development time.

* For Variable ISI (option), use either in combination with ISI Board J1758A (select J1758A) or in combination with external channel board (select Not Specified).



ISI Setting Screen Example

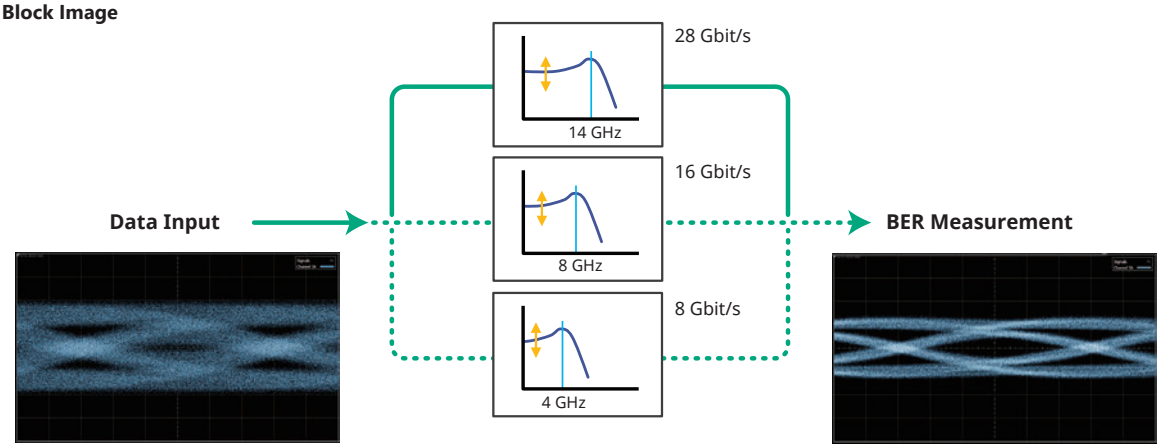


ISI, CEI-28G, 14 dB Loss waveform (typical)

Multi-band CTLE

Installing the CTLE option supporting multi-band input signals of 28, 16, and 8 Gbit/s at the receive-side of the 21G/32G bit/s SI ED MU195040A permits BER measurements even when the Eye is closed by transmission path losses. Since this CTLE function is a hardware equalizer rather than the software emulator, it supports evaluation of TRx BER performance under near-to-live conditions, such as BER evaluation of test signals, and comparison of DUT BER measurement results.

3-band CTLE Block Image



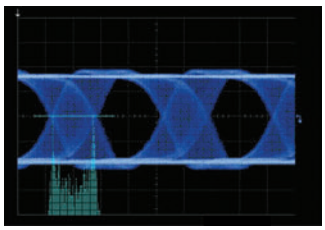
Waveform after passage through 28 Gbit/s, –10 dB @ 14 GHz channel

28 Gbit/s open Eye waveform using CTLE

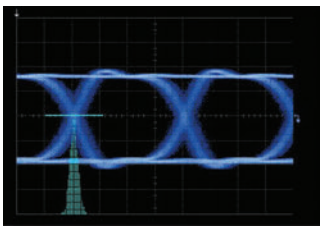
SI PPG/ED Signal Integrity Evaluation

Jitter/Noise Addition

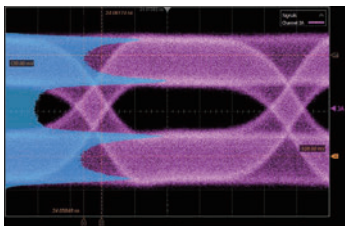
To perform DUT receiver stressed input tolerance tests, the BER is measured under the worst conditions using a stressed signal with added jitter and voltage noise. Using the MP1900A series with the Jitter Modulation Source MU181500B, Jitter Tolerance Test MX183000A-PL001 software, and Noise Generator MU195050A for adding CM/DM/White Noise supports receiver tolerance tests in conformance with the various interface standards. The MP1900A series offers strong support for receiver stressed input tolerance tests by generating high-quality signals before jitter and noise addition as well as for adding high-linearity jitter and noise.



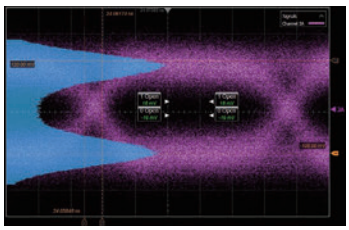
Sinusoidal Jitter (SJ)



Random Jitter (RJ)



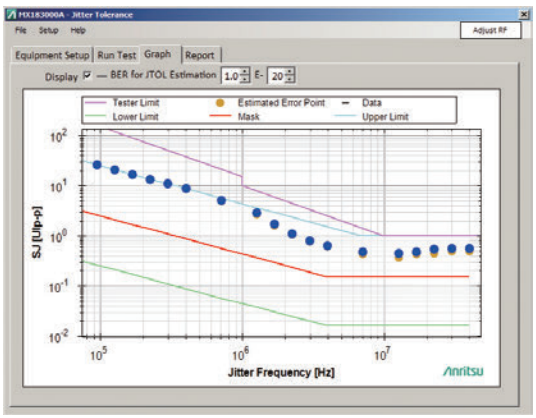
CM/DM Noise



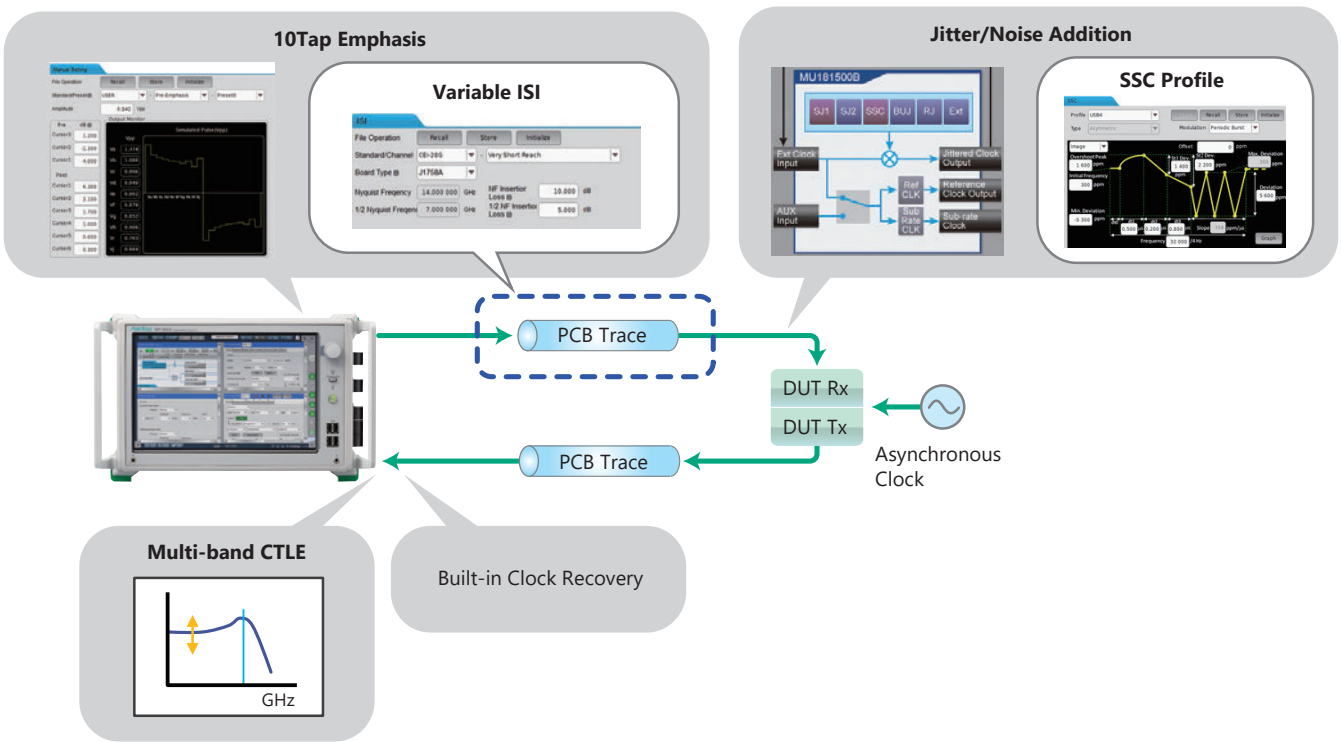
White Noise

Jitter Tolerance Test Function (MX183000A-PL001)

- High-versatility Jitter Tolerance measurements
- PHY Device Jitter Tolerance tests by impressing SJ/RJ/BUJ
- Standards-compliant Mask measurements
- Fast measurement times using low error rate estimation function, such as 1E–12 and 1E–15
- Tolerance measurements versus device characteristics using four Binary, Upward, Downward, Binary + Linear methods



Low Error Rate Estimation BER Measurements



SI PPG/ED Link Training

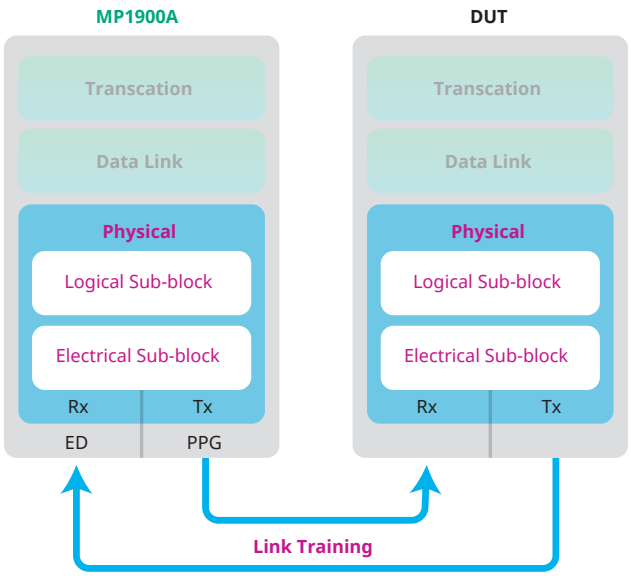
The PCI Express and 10 Gbit/s USB3.2 standards require PHY layer tests such as Jitter Tolerance tests on an established Link to assure interconnectivity between the host and device. Additionally, it is necessary to determine whether the cause is a physical or logical fault at a Link fault.

The MP1900A PCI Express/USB functions have Protocol Awareness with a Link Training function required for evaluating the PHY layer as well as an analysis function for detecting each LTSSM state transition to help troubleshoot faults. When more detailed debugging is required, the training sequence generation timing can be adjusted using the Sequence Editor function (MU195020A-050).

These all-in-one functions facilitate efficient PHY layer evaluation of PCIe Gen1 to Gen5 and USB3.2 receivers through inspection and fault troubleshooting.

Moreover, combination with the Jitter Tolerance Measurement function (MX183000 A-PL001) supports consistent receiver tests of high-speed serial interfaces.

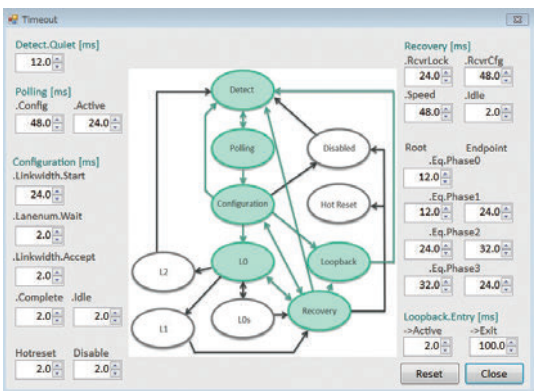
LTSSM: Link Training Status State Machine



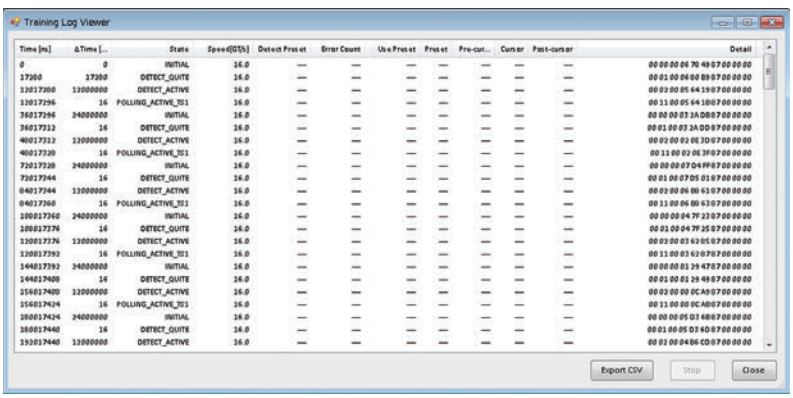
Supports physical layer measurements of add-in cards and system boards

- Tx LEQ: Transmitter Link Equalization response Test
- Rx LEQ: Receiver Link Equalization Test
- Receiver Jitter Tolerance Test

PCI Express Link Training (MX183000A-PL021/PL025)

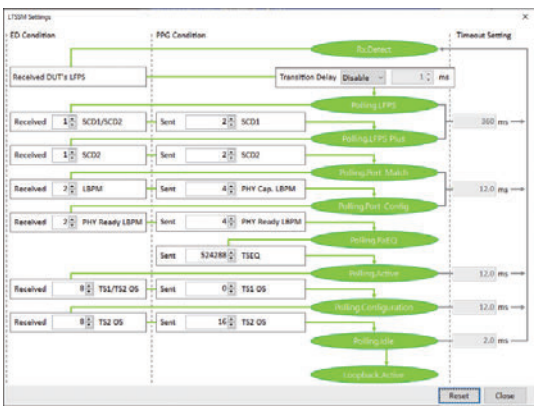


PCIe Link Training State Transition

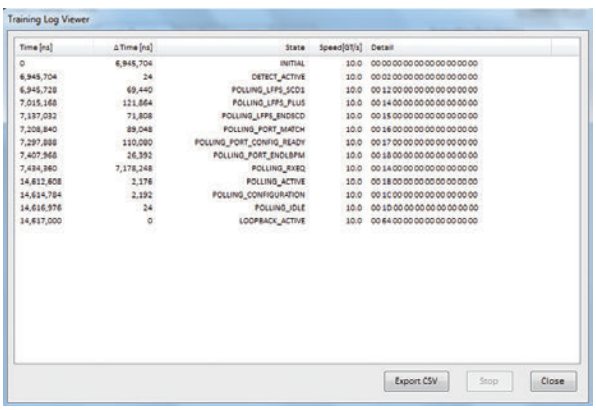


LTSSM Log of each LTSSM State Transition

USB Link Training (MX183000A-PL022/PL023)



USB Link Training State Transition



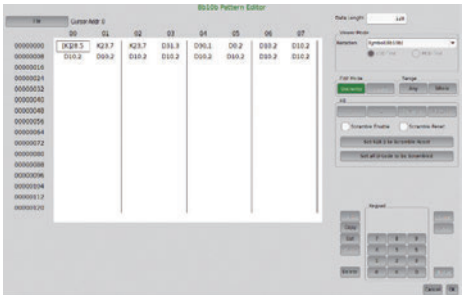
LTSSM Log of each LTSSM State Transition

SI PPG/ED Sequence Editor

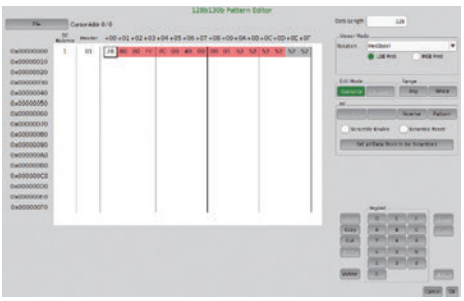
The PCI Express and USB 3.2 tests require state control using Link Training. However, sometimes at device testing, Link Training does not operate normally at test execution.
The MP1900A Sequence Editor can make the DUT loopback state by outputting the ordered set used in the PCIe Gen1/2/3/4/5, USB3.1 Gen1/2 PHY layer protocol from PPG. It is possible to arbitrarily set the information of the ordered set to be used, the number to be transmitted, and the order of transmission, and analyze the cause of not being able to link up by changing the transition conditions.

Sequence Editor Function (MU195020A-050), Sequence Editor Function PCIe 5 Extension (MU195020A-051)

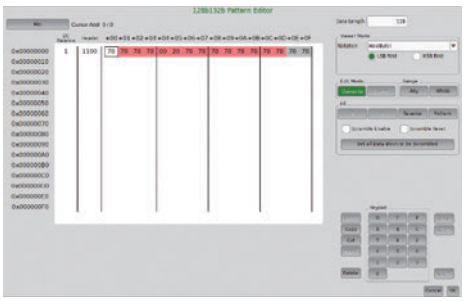
Sequence Editor Settings



PCIe/USB 8B/10B Editing



PCIe 128B/130B Editing



USB 128B/132B Editing

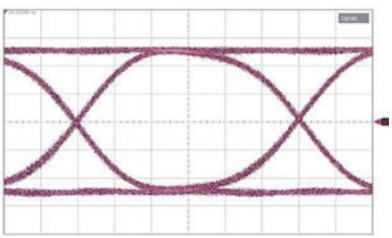
SI PPG/ED High Waveform Quality and High Sensitivity

Low-Noise, High-Quality BERT with Low Intrinsic Jitter Output, High Sensitivity and Wideband Input

Assuring DUT design margins has become an important issue as transmission rates have become faster and PAM4 Signal formats have been introduced. Designers require more accurate evaluations to confirm that adequate margins are maintained. As a result, the impact of uncertainty elements, such as noise and Intrinsic Jitter characteristics of measuring instruments, on results can no longer being ignored. These newly developed best-of-class PPG with lowest-level Intrinsic Jitter and high-sensitivity ED can measure DUT guaranteed margins more accurately to help improve R&D efficiency.

Low Intrinsic Jitter Data Output PPG

The MU195020A PPG has an Intrinsic Jitter of just 115 fs rms.



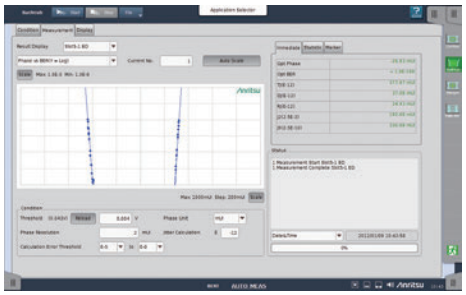
28.1 Gbit/s PRBS $2^{31} - 1$
Typical Output Waveform

Low intrinsic RJ 115 fs rms

High-Sensitivity, Wideband Input ED

The assured ED input analog bandwidth is 40 GHz. This bandwidth supports evaluation of Eye margin characteristics with high reproducibility even at input of small signals.

Example of Eye Contour Measurement at Input of Small 50 mVp-p Signal

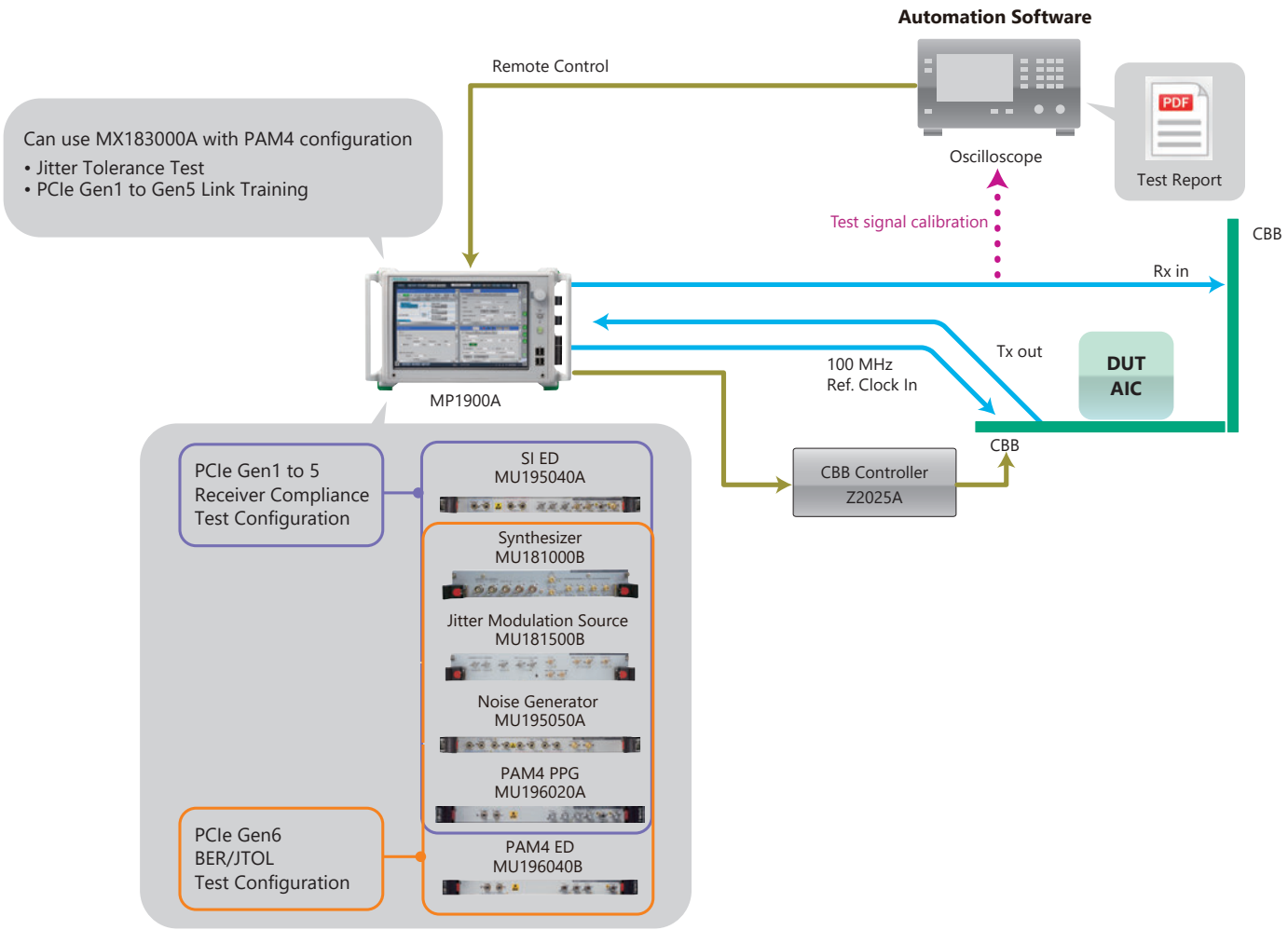


Bathtub Measurement Example

Future Expandability

PAM4 signaling has been adopted for the next-generation PCIe Gen6 interface.
The MP1900A with installed PAM4 PPG module supports PCIe Gen1 to Gen5 measurements, such as Link Negotiation.
As a result, the transition to PCIe Gen Gen6 is easy*.

*: Contact our business section about support for PCIe Gen6 compliance test.

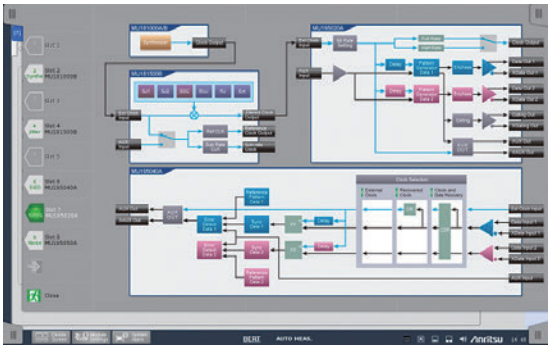


Easy to Use Operability

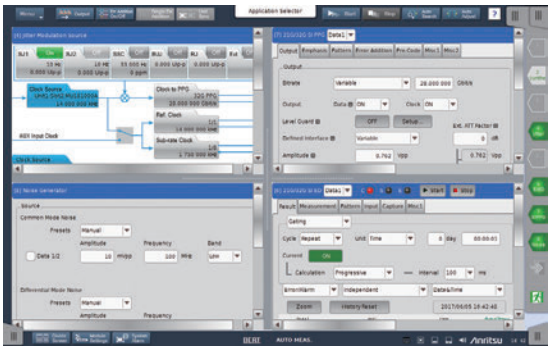
Improved Operability with New System View, User Interface, and Multi-windows

The MP1900A features easy intuitive operability based on a redesigned GUI and large 12.1-inch touch-panel LCD. Fast mistake-free settings help shorten measurement times.

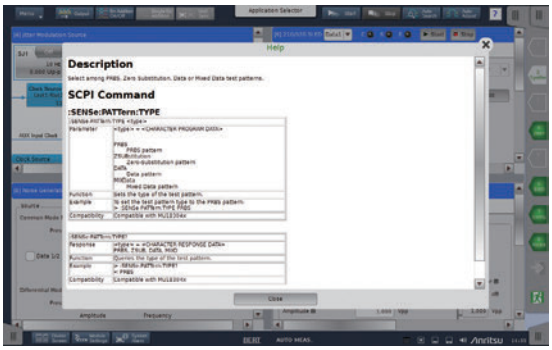
The newly developed system view displays system functions as easy-to-understand blocks, supporting smooth settings and easy operation of each module.



Four split screens help improve the efficiency of multi-channel measurements.

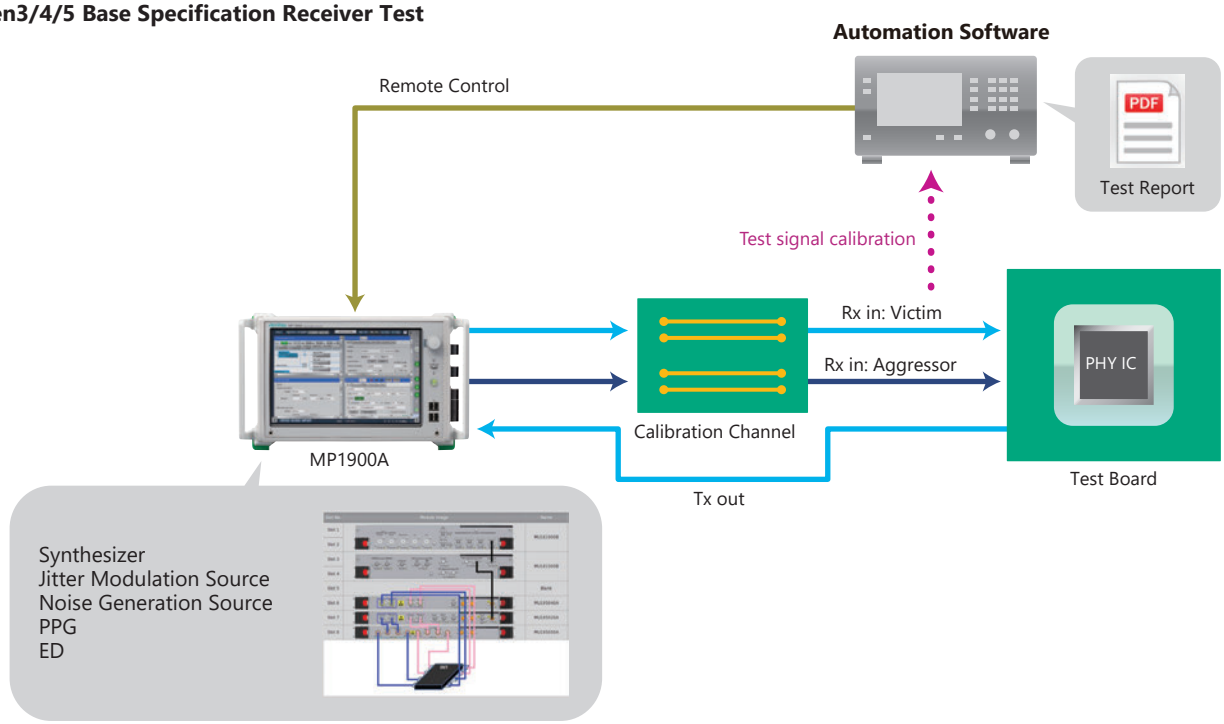


The Help function displays the remote commands corresponding to GUI operations, which simplifies automated system configurations.



Application Examples

PCIe Gen3/4/5 Base Specification Receiver Test



Required Items

- Cross Talk Test
- Jitter Tolerance Test
- Emphasis Effect Validation
- Supports Common/Separate Clock Architecture

PCI Express Gen5 Base Solution Features

- All-in-One Crosstalk Test using 2ch PPG
- Automatic Calibration using Variable ISI Option Without Changing Calibrated Channel Connection
- True BER Measurement using SKP OS Filtering Function
- Support for All SRIS, SRNS, and Common Clock Architectures

Crosstalk Test

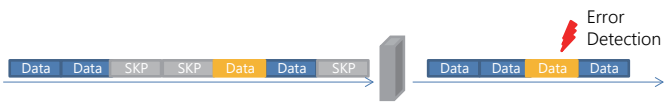
Crosstalk has a large impact on the integrity of 32 GT/s Gen5 signals.

Crosstalk can be evaluated easily with good reproducibility using the 2ch PPG with a high differential amplitude of up to 2.6 Vpp.

SKP OS Filtering

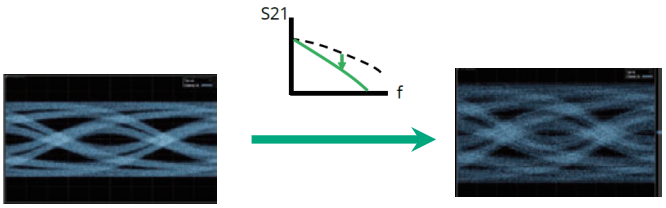
The SKIP Symbol used to absorb frequency deviation must be excluded from the target BER measurement. The Error Detector automatically discriminates between Data and SKIP symbols to measure the true BER.

This function supports PCIe Gen1 to Gen5.



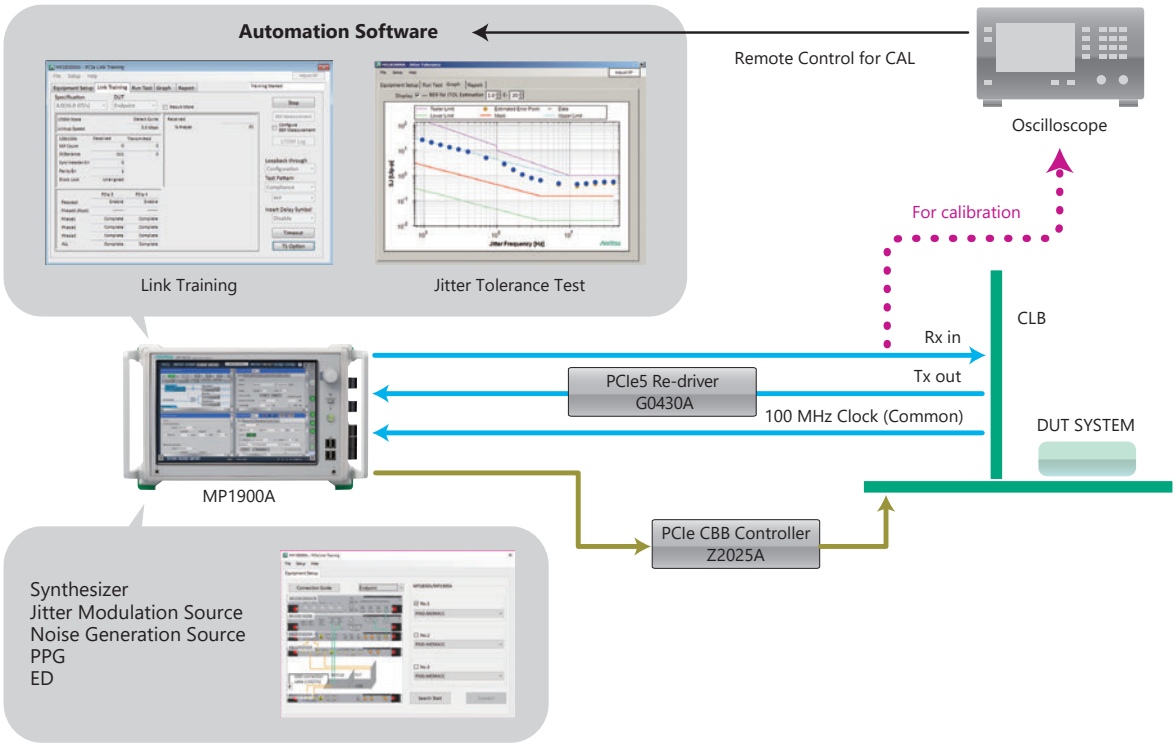
Variable ISI Function

Calibration can be performed without changing the trace connection by generating a signal simulating channel loss using the Emphasis function supporting up to 10Taps (MU195020A-011, 021 options).



Application Examples

PCIe Gen3/4/5 CEM Specification Receiver Test



Required Items

- Link Training function
- Jitter Tolerance Test
- Emphasis Effect Validation
- Supports Common/Separate Clock Architecture

PCI Express CEM Solution Features

- All-in-one support for Protocol Awareness PCIe Gen1 to Gen5 receiver tests
- Event Trigger Function for Tx/Rx Link Equalization Test
- 2.4 Gbit/s to 32.1 Gbit/s high-speed BERT
- Low-intrinsic-jitter and high-quality output waveform, high-sensitivity ED
- Link Training, Link Equalization and LTSSM analysis functions
- 10Tap Emphasis function
- 12 dB CTLE and Clock Recovery functions
- CMI and DMI Noise addition, and SJ, RJ, BUJ, and SSC Jitter Addition functions
- Thunderbolt 3, USB3.2/4, PCI Express Gen5 support
- Full automation including CBB control

PCIe CBB Controller Z2025A

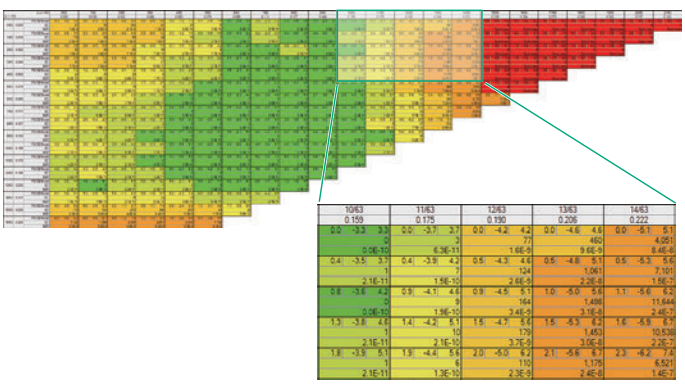
The DUT must be reset and transitioned to the Initial state before starting Link Training.
The PCIe CBB Controller Z2025A fully automates control of Rx LEQ and Tx LEQ using the Power Reset and Power Cycle control pins implemented by PCIe CBB 4.0 (Compliance Base Board 4.0).

PCIe Re-Driver G0430A

The Rx test requires establishment of a DUT return path. If the return-path physical loss is greater than about 18 dB, connection of an external equalizer is recommended since there is a risk of detecting errors in the return path. The return path can be established by using PCIe5 Re-Driver Set G0430A.

Matrix Scan Function

To secure high-quality communications with the Link partner, the best combination of the Tx-side EQ and Rx-side EQ must be selected.
The Matrix scan function scans for the best Tx EQ setting at the receiver to find the best setting automatically at the receiver.

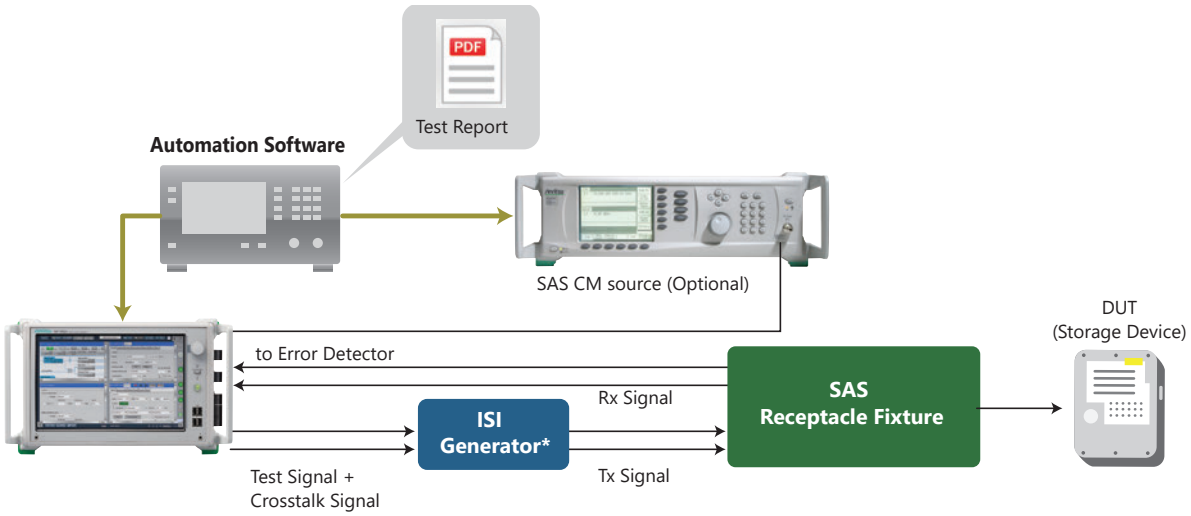


Link Training Function (MX183000A-PL021/PL025)

The PCI Express receiver test requires establishment of the Link status using LTSSM before performing the DUT BER test.
Installing the PCIe Link Training option in the MP1900A supports verification of the Link status required for measurement. This option has an LTSSM Analysis function for troubleshooting problems the Link status cannot be configured.

Application Examples

SAS-3/-4 Receiver Test



*: Should use specified ISI generator by PCIe or SAS

Required Functions

- 12 Gbit/s to 22.5 Gbit/s BERTS
- Stressed Signal Calibration and Test
- Jitter Margin Test

Wideband BERTS

The same configuration covers SAS-3 (12 Gbit/s), SAS-4 (22.5 Gbit/s) and PCI Gen1 to Gen5 measurements.

Receiver Test

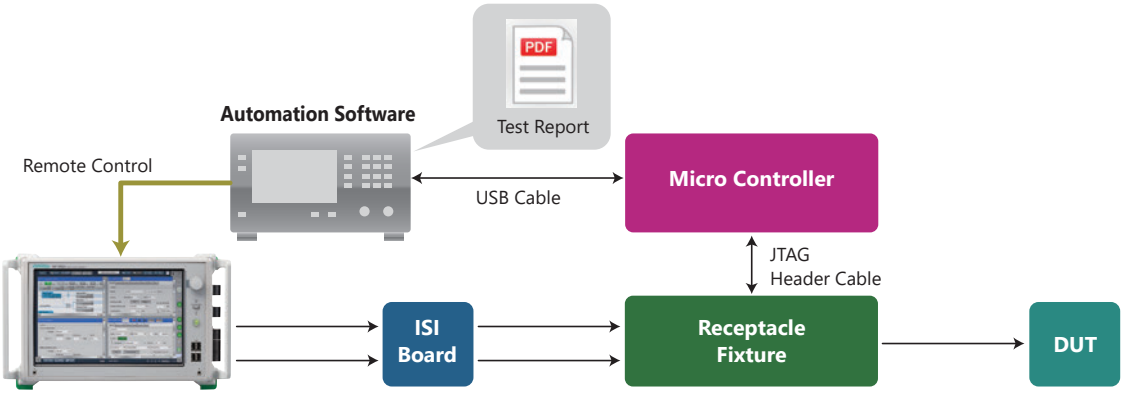
Stressed signal calibration and measurements can be automated using the automation software to shorten the design stage by cutting Compliance test times and improving measurement reproducibility.

Jitter Margin Test

The automation software supporting jitter tolerance tests helps simplify receiver performance evaluations required by storage, HBAs, and ICs.

Application Examples

USB Type-C Receiver Test (USB4, Thunderbolt3)



Required Functions

- 20 Gbit/s PPG
- Stressed Signal Calibration Function
- Jitter Tolerance Function

Supports USB Type-C

Supports specified bit rates (USB4 20G, Thunderbolt3 20.625G)

Stressed Signal Calibration

Automation Software supports automatic stressed signal calibration as specified by USB Type-C.

Stressed Signal Input Test

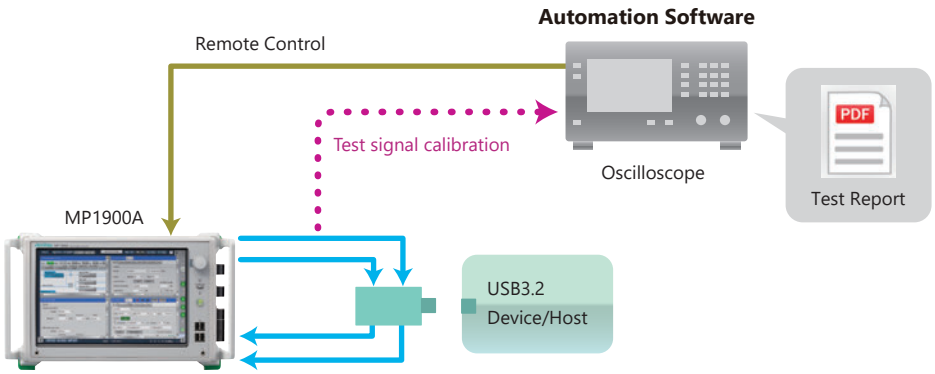
- Supports Rx BER measurements required by Host/Device compliance test
- Supports automatic Rx test using Tenlira scripts
- Supports automatic Pass/Fail measurement for Rx stressed signal tests

Receiver Test

Calibration and the Jitter Tolerance test can both be automated using the automation software. Automation helps cut design verification times.

Application Examples

USB 3.2 Gen1/2 Receiver Test



Required Functions

- Loopback State Setting Function
- Jitter Tolerance Function
- Automatic Receiver Test Function
- Link Training Function

Link Training Function

Automated evaluation of BER required by the Compliance Test can be configured using the MX183000A and MX183000A-PL022/023 option.

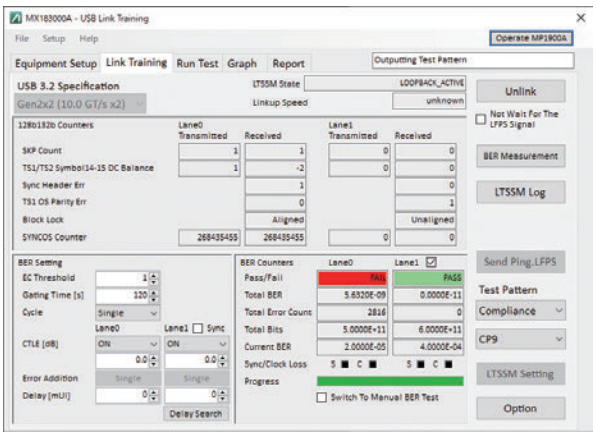
- Supports transition to Loopback mode used for USB 3.2 Gen1/2 ×1 and ×2 device evaluation
- Supports troubleshooting using LTSSM analysis function when unable to transition to Loopback mode
- Detailed troubleshooting analysis is supported by changing the timeout for each state
- Supports easy troubleshooting when problems occur when changing timeout at each state by using LTSSM trigger to capture transient signals using oscilloscope when state does not transition normally

Receiver Jitter Tolerance Test

Jitter Tolerance tests can be automated using the MX183000A-PL001 software to help shorten the design validation time.

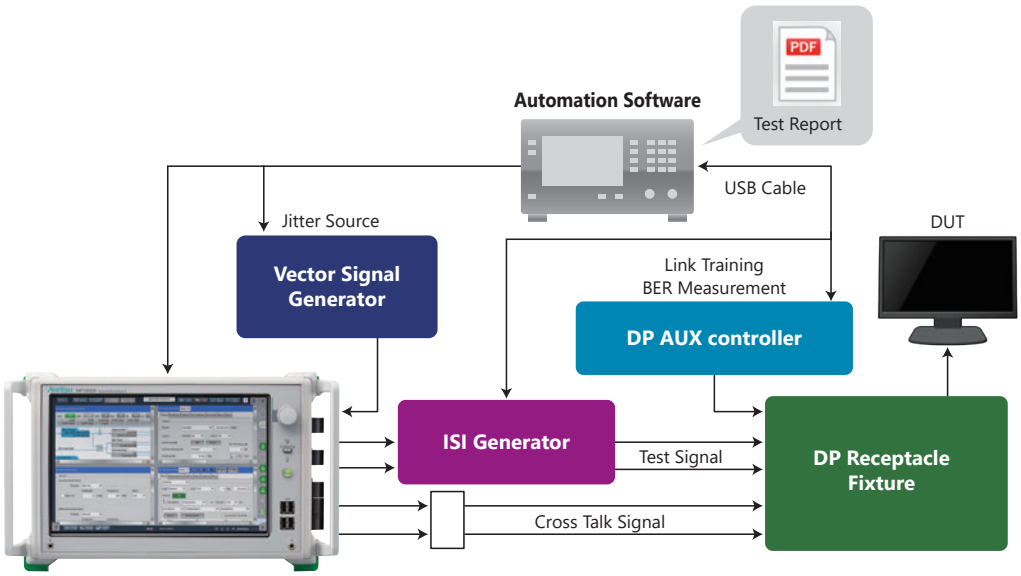
x2 Device Evaluation

Lane 0 and Lane 1×2 devices can be evaluated simultaneously using the MX183000A-PL023.
Crosstalk effects can also be analyzed by impressing skew between lanes.



Application Examples

DisplayPort1.4 Sink Test



Required Functions

- 2.7 Gbit/s to 8.1 Gbit/s PPG
- Stressed Signal Calibration and Test
- USB Type-C Alternative Mode Operation

Wideband PPG

One module covers RBR (1.62 Gbit/s)*, HBR (2.7 Gbit/s), HBR2 (5.4 Gbit/s), and HBR3 (8.1 Gbit/s).
Expandible up to 32 Gbit/s without hardware upgrade.
Supports DisplayPort 2.0 (20 Gbit/s) and future faster standards

*: Can generate special RBR (1.62 Gbit/s) pattern

Sync Sensitivity Test

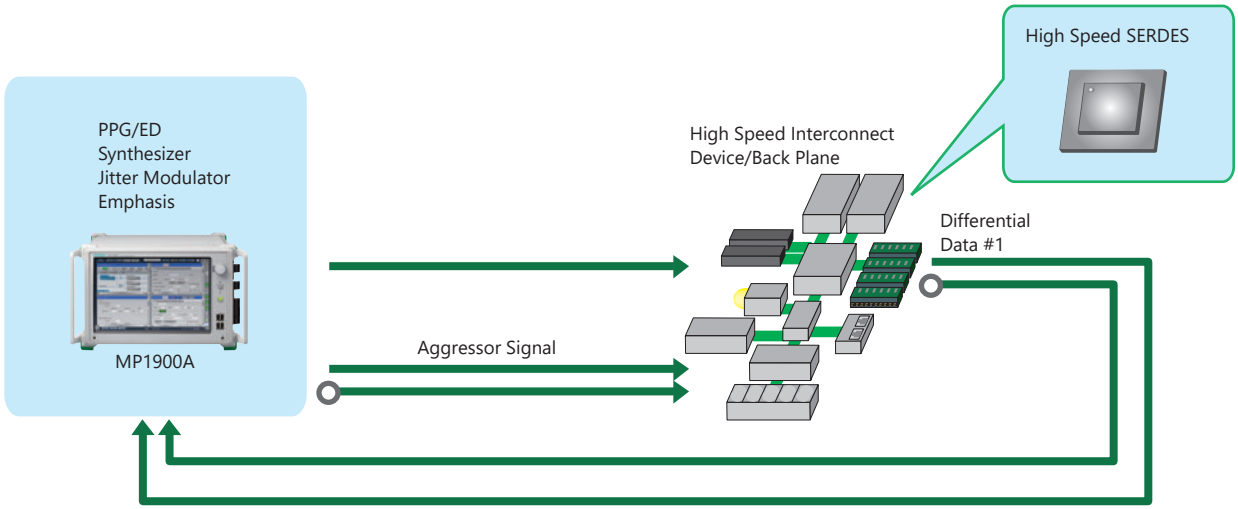
Stressed signal calibration and measurements can be automated using the automation software to shorten the design stage by cutting Compliance and Jitter Tolerance Margin test times and improving measurement reproducibility.

USB Type-C Alternative Mode

Measurement of the Alternative Mode transmitting Display Port signals using the Auto USB Type-C connector is supported.

Application Examples

High-speed Interconnect Evaluation



Required Test Items

- 32.1 Gbit/s Multi-channel signal generation
- Jitter Tolerance test
- Emphasis efficiency check
- Crosstalk test

Multi-channel

Along with support for multi-channels, the bit rate of devices such as back planes of high-performance servers is becoming increasingly faster. The MP1900A supports generating both the Victim signal with controlling Emphasis and the Aggressor signal for crosstalk testing simultaneously. The MP1900A offers multi-channel measurements for TRx devices such as Transceiver, SERDES and Clock Data Recovery (CDR).

Skew and Crosstalk Effect Check

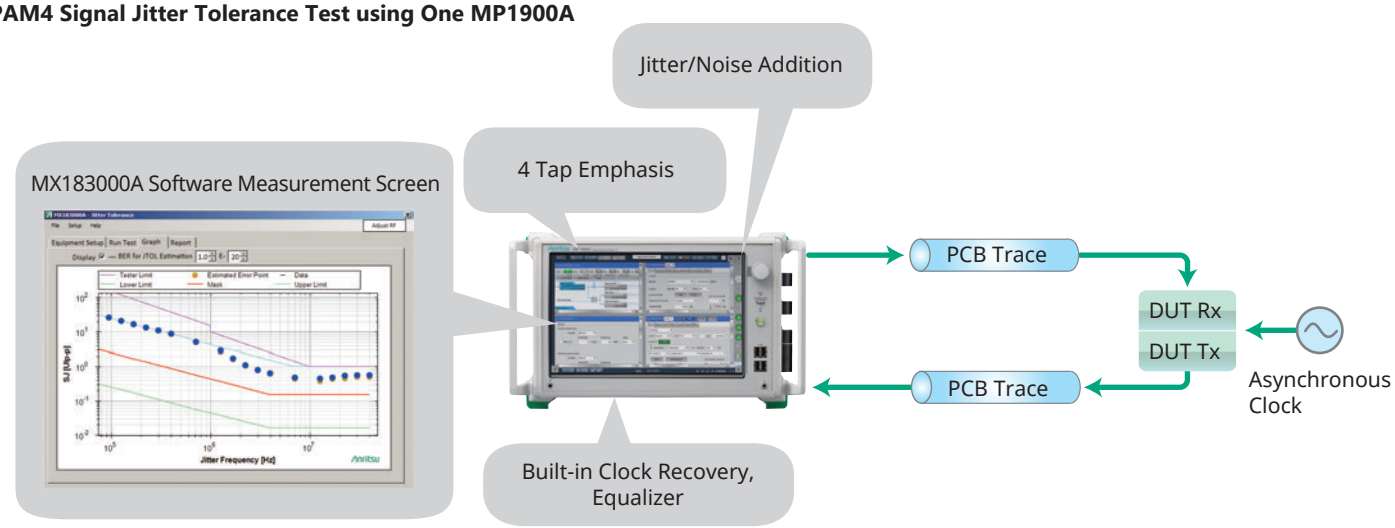
Processing high speed digital signals requires both logic tests and actual equipment tests. The MP1900A supports both pattern synchronization and phase adjustment functions, permitting easy tests of Rx device skew tolerance and crosstalk effects.

Jitter Tolerance Test

Jitter Tolerance tests supporting various standards can be run by simultaneously impressing SJ (2 tone), RJ, BUJ, and SSC up to 32.1 Gbit/s using the MX183000A-PL001 and MU185000B Jitter modulation sources.
The Eye opening of signals passing through the back-plane is degraded by loss in the board traces.

Application Examples

PAM4 Signal Jitter Tolerance Test using One MP1900A



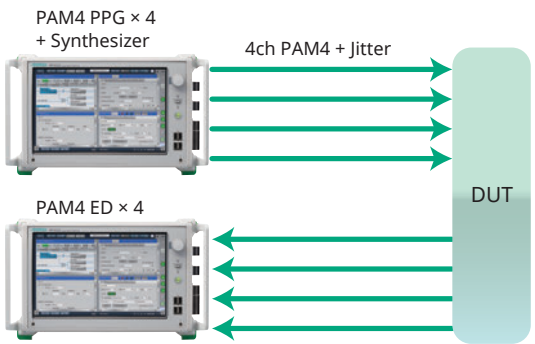
Required Items

- PAM4 BER measurement
- Jitter Tolerance Test

BER Measurements of 64-Gbaud PAM4 Signals

BER measurements can be performed in real-time using the PAM4 PPG and ED modules with no need for other external equipment*.

- World-first, all-in-one solution requiring no other external equipment
- Module with built-in clock recovery, equalizer
- Wide-range Emphasis function
- High-sensitivity data input
- Symbol BER evaluation



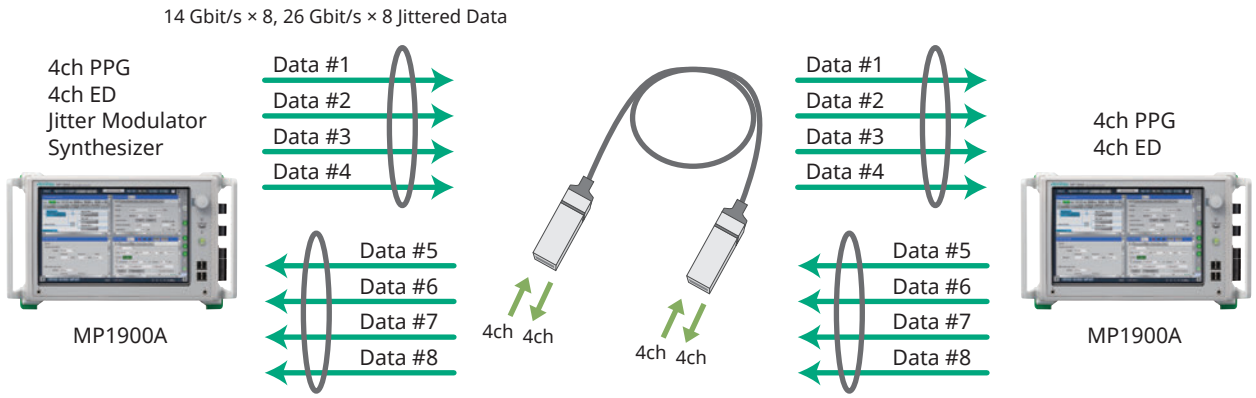
*: Refer to the 32G/64G NRZ/PAM4 Signal Integrity Test Solution Catalog (MP1900A_64G-E-A-1) for details of PAM4 PPG/ED.

Jitter Tolerance Test

Testing the DUT receiver input stress tolerance requires BER measurements under severe conditions using a stressed signal with added jitter and noise. The all-in-one MP1900A series supports receiver stress tests for various interface specifications using the Jitter Modulation Source MU181500B for adding SJ, RJ, BUJ, and SSC simultaneously, the Jitter Tolerance Test MX183000A-PL001 software, and the Noise Generator MU195050A for adding CM/DM/White voltage noise. The MP1900A series provides strong support for high-quality signals prior to jitter and noise addition, as well as receiver stressed-signal tolerance tests using high-linearity jitter and noise addition functions.

Application Examples

InfiniBand EDR (25.78G) AOC Evaluation



Required Test Items

- 8ch (4ch two ways) simultaneous BER measurement
- Crosstalk Test
- Jitter Tolerance Test
- Bathtub Jitter and Eye Diagram Analysis

8ch (4ch two ways) Simultaneous BER Measurement

QSFP Active Optical Cables (AOC) used by InfiniBand, etc., perform simultaneous transmission over a total of 8 channels using two-way transmissions over 4 channels. The MP1900A incorporates 8 channels (8ch PPG + 8ch ED) simultaneously in one main unit and can measure all channels at one time, offering excellent performance and shorter measurement times. Moreover, InfiniBand HDR measurement is also supported using PAM signals.

Jitter Tolerance Test

AOCs in data centers are using low input and output amplitude levels to cut power consumption costs, making it important to assure interconnectivity. With its high sensitivity data input and CTLE, the MU195040A supports reception of low-amplitude, low-Eye-opening Data signals and perform high-reproducibility DUT Jitter Tolerance tests.

Crosstalk Effect Confirmation

Implementing 20 Gbit/s class transmissions not only requires logic tests but also requires actual equipment verification tests. Since the MP1900A has both pattern synchronization and independent phase tuning for each channel, tests on items such as the effect of AOC crosstalk are implemented easily.

Bathtub Jitter and Eye Diagram Analysis

Bathtub Jitter Analysis (separate TJ, RJ, DJ) is supported by the built-in as standard Clock Delay function. Low bit error rates, such as 1E-12 and 1E-15, can also be estimated quickly from the change in bit error rate versus phase.

Automation Software Selection Guide

The MP1900A can execute the following receiver tests using automation software in combination with a real-time oscilloscope. Refer to the next page for option configurations required by the MP1900A. Refer to the Selection Guide (MP1900A-E-Z-1) for the supported combination of real-time oscilloscopes and automation software.

Interface Type	Compliance Test Item	
PCIe Gen 3/4/5	Base Spec	Stressed Eye Test
	CEM Spec	Transmitter initial Tx Equalization Transmitter Link Equalization response (Tx LEQ) Receiver Link Equalization (Rx LEQ) PLL Bandwidth
USB3.2 Gen1/2	Transmitted Eye Test Receiver Jitter Tolerance Test	
USB Type-C (USB4, Thunderbolt3)	Receiver Test SJ Margin Test Amplitude Margin Test	
SAS-3/-4	Receiver Jitter Tolerance Test	
DP1.4	Sink Jitter Tolerance Test	

Module Selection Guide

Refer to the Selection Guide (MP1900A-E-Z-1) for details on the module and option combinations.

Category	Module/Option	Name	PCIe Gen1 to 5 Receiver Compliance Test*1	PCIe Gen1 to 5 Receiver Compliance Test + Gen6 BER/JTOL Tests*1	PCIe Gen1 to 5 Receiver Base Spec Crosstalk Test
Main Frame	MP1900A	Signal Quality Analyzer-R	1	1	1
Synthesizer	MU181000B	12.5 GHz 4 Port Synthesizer	1	1	1
	MU181000B-001	Jitter Modulation Source			
	MU181000B-002	SSC Extension	1	1	1
Jitter Modulation	MU181500B	Jitter Modulation Source	1	1	1
21G/32G PPG	MU195020A	21G/32G bit/s SI PPG	1		1
	MU195020A-001	32G bit/s Extension	1*2		1*2
	MU195020A-010	1ch Data Output	1		
	MU195020A-020	2ch Data Output			1
	MU195020A-011	1ch 10Tap Emphasis	1		
	MU195020A-021	2ch 10Tap Emphasis			1
	MU195020A-030	1ch Data Delay			
	MU195020A-031	2ch Data Delay			1
	MU195020A-040	1ch Variable ISI			
	MU195020A-041	2ch Variable ISI			1*3
	MU195020A-050	Sequence Editor Function	1*4		1*4
	MU195020A-051	Sequence Editor Function PCIe 5 Extension	1*4		1*4
PAM4 PPG	MU196020A	PAM4 PPG		1	
	MU196020A-001	32G baud		1	
	MU196020A-002	58G baud			
	MU196020A-003	64G baud			
	MU196020A-011	4Tap Emphasis		1	
	MU196020A-030	Data Delay			
	MU196020A-040	Adjustable ISI			
	MU196020A-042	FEC Pattern Generation		1	
	MU196020A-050	Inter-Module Synchronization			
21G/32G ED	MU195040A	21G/32G bit/s SI ED	1	1	1
	MU195040A-001	32G bit/s Extension	1*2	1*2	1*2
	MU195040A-010	1ch ED	1	1	
	MU195040A-020	2ch ED			1
	MU195040A-011	1ch CTLE	1	1	
	MU195040A-021	2ch CTLE			1
	MU195040A-022	Clock Recovery	1	1	1
PAM4 ED	MU196040B	PAM4 ED		1*5	
	MU196040B-001	32G baud (2.4G to 32.1G)		1*5	
	MU196040B-002	58G baud (NRZ: 2.4G to 64.2G, PAM4: 2.4G to 58.2G)			
	MU196040B-011	Equalizer		1*5	
	MU196040B-021	29G baud Clock Recovery (2.4G to 29G)			
	MU196040B-022	32G baud Clock Recovery (2.4G to 32.1G)		1*5	
	MU196040B-023	58G baud Clock Recovery Extension (51G to 58.2G)			
	MU196040B-041	SER Measurement		1	
	MU196040B-042	FEC Analysis		1	
Voltage Noise	MU195050A	Noise Generator	1	1	1
	MU195050A-001	White Noise			
Software	MX183000A-PL001	Jitter Tolerance Test	1	1	1
	MX183000A-PL021	PCIe Link Training	1*6	1*6	1*6
	MX183000A-PL025	PCIe 5 Link Training	1*6	1*6	1*6

*1: Anritsu contributes as a PCI-SIG member to PCI Express standards.
*2: Required for PCIe Gen5 support
*3: Supports Gen5 Base Spec receive test
*4: Used for debugging PCIe Link training. PCIe Gen1-4 requires MU195020A-050 while PCIe Gen5 requires both MU195020A-050 and -051.
*5: PAM4 ED supports future Gen6 BER and JTOL measurements; enquire about support for Gen6 receiver tests.
*6: PCIe Gen1-4 requires MX183000A-PL021 while PCIe Gen5 requires both MX183000A-PL021 and -PL025.

Module Selection Guide

Category	Module/Option	Name	USB3.2 ×1 Receiver Test	USB3.2 ×2 Receiver Test	USB Type-C, DP Receiver Test
Main Frame	MP1900A	Signal Quality Analyzer-R	1	1	1
Synthesizer	MU181000B	12.5 GHz 4 Port Synthesizer	1	1	1
	MU181000B-001	Jitter Modulation Source			
	MU181000B-002	SSC Extension			
Jitter Modulation	MU181500B	Jitter Modulation Source	1	1	1
21G/32G PPG	MU195020A	21G/32G bit/s SI PPG	1	1	1
	MU195020A-001	32G bit/s Extension			
	MU195020A-010	1ch Data Output	1		1*7
	MU195020A-020	2ch Data Output		1	1*7
	MU195020A-011	1ch 10Tap Emphasis	1		1*7
	MU195020A-021	2ch 10Tap Emphasis		1	1*7
	MU195020A-030	1ch Data Delay			
	MU195020A-031	2ch Data Delay		1	
	MU195020A-040	1ch Variable ISI			
	MU195020A-041	2ch Variable ISI			
	MU195020A-050	Sequence Editor Function	1*8	1*8	
	MU195020A-051	Sequence Editor Function PCIe 5 Extension			
21G/32G ED	MU195040A	21G/32G bit/s SI ED	1	1	
	MU195040A-001	32G bit/s Extension			
	MU195040A-010	1ch ED	1		
	MU195040A-020	2ch ED		1	
	MU195040A-011	1ch CTLE	1		
	MU195040A-021	2ch CTLE		1	
	MU195040A-022	Clock Recovery	1	1	
Voltage Noise	MU195050A	Noise Generator	1	1	1
	MU195050A-001	White Noise			
Software	MX183000A-PL001	Jitter Tolerance Test	1		
	MX183000A-PL021	PCIe Link Training			
	MX183000A-PL022	USB Link Training	1	1*9	
	MX183000A-PL023	USB 3.2 × 2 Link Training		1*9	
	MX183000A-PL025	PCIe 5 Link Training			

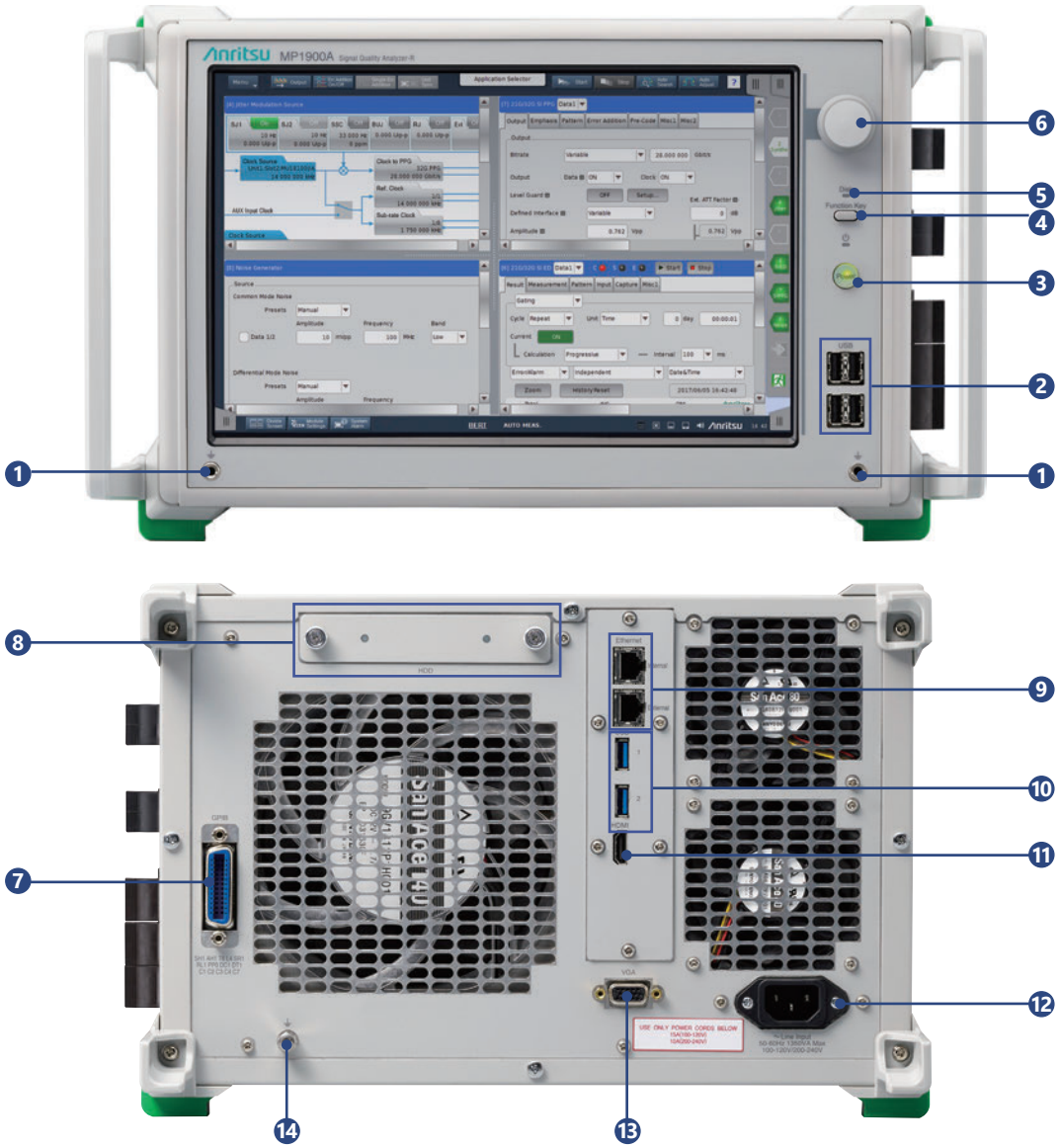
*7: Select either 1ch or 2ch. Either 1ch or 2ch can be selected for USB Type-C. DP receiver test requires 2ch.
*8: Used for debugging USB3.2 Link training.
*9: USB3.2 ×2 Link training requires both MX183000A-PL022 and -PL023.

Category	Module/Option	Name	SAS Receiver Test	Thunderbolt3/USB4 Receiver Test	DP1.4 Sink Test
Main Frame	MP1900A	Signal Quality Analyzer-R	1	1	1
Synthesizer	MU181000B	12.5 GHz 4 Port Synthesizer	1	1	1
	MU181000B-001	Jitter Modulation Source			
	MU181000B-002	SSC Extension	1		
Jitter Modulation	MU181500B	Jitter Modulation Source	1	1	1
21G/32G PPG	MU195020A	21G/32G bit/s SI PPG	1	1	1
	MU195020A-001	32G bit/s Extension	1*10		
	MU195020A-010	1ch Data Output	1	1	
	MU195020A-020	2ch Data Output			1
	MU195020A-011	1ch 10Tap Emphasis	1	1	
	MU195020A-021	2ch 10Tap Emphasis			1
	MU195020A-030	1ch Data Delay			
	MU195020A-031	2ch Data Delay			
	MU195020A-040	1ch Variable ISI	1		
	MU195020A-041	2ch Variable ISI			
	MU195020A-050	Sequence Editor Function			
	MU195020A-051	Sequence Editor Function PCIe 5 Extension			
21G/32G ED	MU195040A	21G/32G bit/s SI ED	1		
	MU195040A-001	32G bit/s Extension	1*10		
	MU195040A-010	1ch ED	1		
	MU195040A-020	2ch ED			
	MU195040A-011	1ch CTLE	1		
	MU195040A-021	2ch CTLE			
	MU195040A-022	Clock Recovery	1		
Voltage Noise	MU195050A	Noise Generator	1	1	1
	MU195050A-001	White Noise			
Software	MX183000A-PL001	Jitter Tolerance Test			
	MX183000A-PL021	PCIe Link Training			
	MX183000A-PL022	USB Link Training			
	MX183000A-PL023	USB 3.2 × 2 Link Training			
	MX183000A-PL025	PCIe 5 Link Training			

*10: Required for SAS-4 support

Signal Quality Analyzer-R MP1900A Panel Layout

Front/Rear Panel



1 Ground Jack
Wrist strap to discharge static electricity

2 USB Port
Four USB2 ports for connecting peripherals

3 Power Switch
Switches power on and off; Standby LED over power switch lights when power cord connected and Power switch set to off

4 Function Keys
Keys for defining functions using software

5 HDD Access LED
Lamp that lights during access to built-in HDD

6 Rotary Encoder
Switch to increase/decrease numeric values by turning knob

7 GPIB
GPIB Connector

8 HDD
Slot for secondary 2.5" HDD

9 Ethernet Connector
External: For Remote Control
(Internal: Reserved for future function expansion)

10 USB Port
Two USB3.0 ports for peripherals

11 HDMI
HDMI connector for displaying screens on external screen

12 Power Inlet
Socket for connecting 3-pole power cord to supply 100 V(ac) to 12 V(ac) or 200 V(ac) to 240 V(ac) power

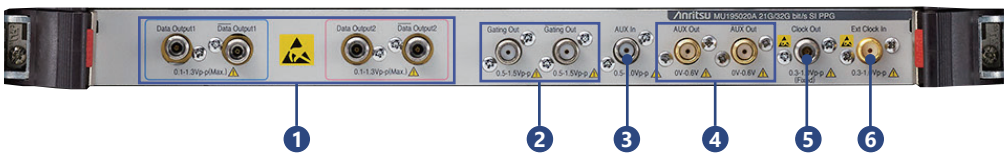
13 VGA
VGA connector for displaying screens on external screen

14 Frame Ground Terminal
Terminal for discharging electrostatic charges; connect DUT and common ground using ground strap

Signal Quality Analyzer-R MP1900A Panel Layout

Modules

21G/32G bit/s SI PPG MU195020A



1. **Data Output, $\overline{\text{Data}}$ Output**
   Connectors outputting differential Data and $\overline{\text{Data}}$ signals
2. **Gating Out, $\overline{\text{Gating}}$ Out**
   Repeat: Timing signal output
   Burst: Timing signal output used at Burst
3. **Aux In**
   Auxiliary signal input connector
   Either Error Injection or Burst can be selected.
4. **Aux Out, $\overline{\text{Aux}}$ Out**
   Auxiliary signal output connectors
   Output of any of 1/N Clock, Pattern Sync, and Burst2 can be selected.
5. **Clock Out**
   Clock signal output connector
6. **Ext Clock In**
   Clock signal input connector

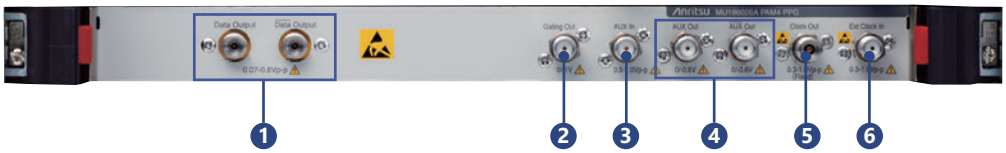
21G/32G bit/s SI ED MU195040A

1. **Data Input, $\overline{\text{Data}}$ Input**
   Input connectors for Data and $\overline{\text{Data}}$ signals
   Supports both differential and single inputs
   When the Clock Recovery MU195040A-x22 is installed, the clock is recovered from the signal input to Data Input1.
2. **Aux In**
   Auxiliary signal input connector
   Any of External Mask, Burst, and Capture External Trigger can be selected.
3. **Aux Out, $\overline{\text{Aux}}$ Out**
   Auxiliary signal output connectors
   Any of 1/N Clock, Pattern Sync, Error, Sync Gain can be output.
4. **Ext Clock In**
   Clock signal input connector

Signal Quality Analyzer-R MP1900A Panel Layout

Modules

PAM4 PPG MU196020A

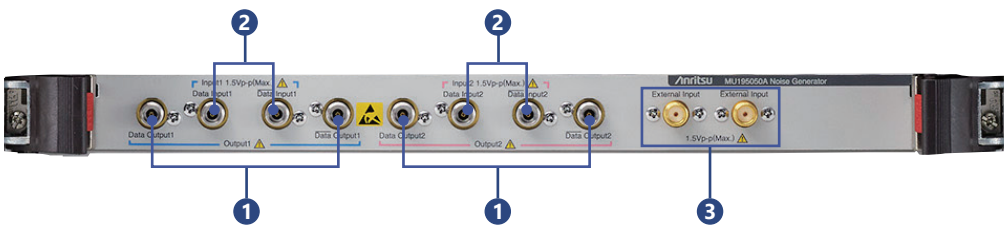


1. **Data Output, $\overline{\text{Data}}$ Output**
   Connectors outputting differential Data and $\overline{\text{Data}}$ signals
2. **Gating Out**
   Repeat: Timing signal output
   Burst: Timing signal output used at Burst
3. **Aux In**
   Auxiliary signal input connector
   Either Error Injection or Burst can be selected.
4. **Aux Out, $\overline{\text{Aux}}$ Out**
   Auxiliary signal output connectors
   Output of any of 1/N Clock, Pattern Sync, and Burst2 can be selected.
5. **Clock Out**
   Clock signal output connector
6. **Ext Clock In**
   Clock signal input connector

PAM4 ED MU196040B

1. **Data Input, $\overline{\text{Data}}$ Input**
   Input connectors for Data and $\overline{\text{Data}}$ signals
   Supports both differential and single inputs
2. **Aux In**
   Auxiliary signal input connector
   Any of External Mask, Burst, and Capture External Trigger can be selected.
3. **Aux Out, $\overline{\text{Aux}}$ Out**
   Auxiliary signal output connectors
   Any of 1/N Clock, Pattern Sync, Error, Sync Gain can be output.
4. **Ext Clock In**
   Clock signal input connector

Noise Generator MU195050A



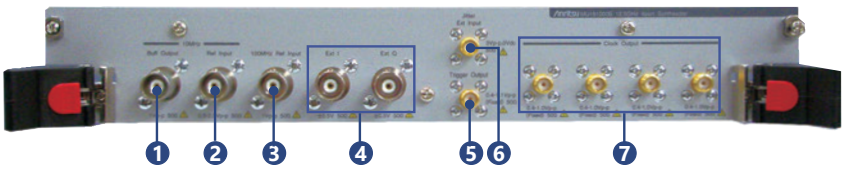
1. **Data Output, $\overline{\text{Data}}$ Output**
   Connector for outputting differential Data and $\overline{\text{Data}}$ Signal with added noise
2. **Data Input, $\overline{\text{Data}}$ Input**
   Connector for inputting Data and Data signal with added noise
3. **External Input, $\overline{\text{External}}$ Input**
   External noise input connectors

* Input2 and Output2 are not used by the MU196020A

Signal Quality Analyzer-R MP1900A Panel Layout

Modules

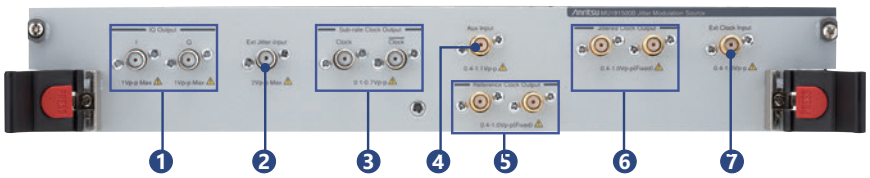
12.5 GHz 4port Synthesizer MU181000B



1. **10 MHz Buff Output**
   Output 10 MHz clock for reference
2. **10 MHz Ref Input**
   Inputs 10 MHz clock for reference
3. **100 MHz Ref Input***1
   Inputs 100 MHz clock for reference
4. **Ext I, Q***2
   Inputs I, Q signals
5. **Trigger Output***2
   Outputs 1/1 or 1/64 clock frequency
6. **Jitter Ext Input***2
   Inputs modulation signal source
7. **Clock Output 1 to 4**
   Outputs clocks

*1: Only when Jitter Modulation Option (MU181000B-001) or SSC Extension (MU181000B-002) installed
*2: Only when Jitter Modulation Option installed (MU181000B-001)

Jitter Modulation Source MU181500B



1. **IQ Output**
   Outputs IQ signal
2. **Ext Jitter Input**
   Inputs Jitter Modulation Source
3. **Sub-rate Clock Output**
   Differential Clock Output signal generated from 1/8 to 1/256-divided Clock Output based on any of following Clock inputs
   • Ext Clock Input • Aux Input
4. **Aux Input**
   Inputs clock signal
5. **Reference Clock Output**
   Dual-system Clock Output signal generated from either 1/1, 1/2, or 1/4-divided Jitter Clock Output based on any of following Clock inputs
   • Ext Clock Input • Aux Input
6. **Jittered Clock Output**
   Two outputs jitter modulated clock signal
7. **Ext Clock Input**
   Inputs external clock

28G/32G bit/s PPG (1ch or 2ch) MU183020A

1. **Data1/$\overline{\text{Data1}}$ Output***3
   Output for 1ch differential data signal
2. **Data2/$\overline{\text{Data2}}$ Output***4
   Output for 2ch differential data signal
3. **Gating Output**
   Output for burst timing signal
4. **Aux Input**
   Input for auxiliary signal
5. **Aux/$\overline{\text{Aux}}$ Output**
   Output for differential auxiliary signal
6. **Clock Output**
   Output for clock signal
7. **Ext Clock Input**
   Input for external clock signal

*3: Data/$\overline{\text{Data}}$ when 1ch option was selected.
*4: Not implemented when 1ch option was selected.

28G/32G bit/s High Sensitivity ED (1ch or 2ch) MU183040B

1. **Data1/$\overline{\text{Data1}}$ Input***5
   Input for 1ch differential data signal
2. **Data2/$\overline{\text{Data2}}$ Input***6
   Input for 2ch differential data signal
3. **Aux Input**
   Input for auxiliary signal
4. **Aux/$\overline{\text{Aux}}$ Output**
   Output for differential auxiliary signal
5. **Ext Clock Input**
   Input for external clock signal

*5: Data/$\overline{\text{Data}}$ when 1ch option was selected.
*6: Not implemented when 1ch option was selected.

Signal Quality Analyzer-R MP1900A Specifications

Refer to the MP1900A Data Sheet (MP1900A_Datasheet-E-A-1) for detailed specifications.

Signal Quality Analyzer-R MP1900A

LCD		12.1" WXGA 1280 × 800
Remote Interface		GPIB, LAN
Module Slots		8
External Equipment Interface		USB × 6, VGA × 1, HDMI × 1
OS		Window Embedded Standard 7
Power Supply		100 V(ac) to 120 V(ac), 200 V(ac) to 240 V(ac), 50 Hz to 60 Hz Power consumption: 1350 VA max.
Dimensions and Mass		340 (W) × 222.5 (H) × 451 (D) mm, 20 kg (excluding modules)
CE	EMC	2014/30/EU, EN61326-1, EN61000-3-2
	LVD	2014/35/EU, EN61010-1
	RoHS	2011/65/EU, (EU) 2015/863, EN IEC 63000: 2018
UKCA	EMC	S.I. 2016 No.1091, EN 61326-1, EN61000-3-2
	LVD	S.I. 2016 No.1101, EN 61010-1
	RoHS	S.I. 2012 No.3032, EN IEC 63000:2018

12.5 GHz 4 Port Synthesizer MU181000B

Clock Output	Number of Output: 4 Frequency Range: 0.1 GHz to 12.5 GHz, Steps: 1 kHz/1 MHz Level: 0.4 Vp-p to 1 Vp-p (AC) Connector: SMA (f), Termination: 50Ω/GND
10 MHz Input	Frequency: 10 MHz ±10 ppm Level: 0.5 Vp-p to 2.0 Vp-p Connector: BNC, Termination: 50Ω/GND
10 MHz Output	Level: 1.0 Vp-p ±30% (AC) Connector: BNC, Termination: 50Ω/GND
100 MHz Reference Signal Input (SSC Extension MU181000B-002)	Outputs either 100 MHz with phase deviation x25, x50, or x80 frequency-multiplied clock from Clock Output connector Supports PCI Express Host Reflclk input Modulation Frequency: 30 kHz to 33 kHz Level: 0.15 Vp-p to 1.3 Vp-p (AC) Connector: BNC

Jitter Modulation Source MU181500B

External Clock Input	Frequency Range: 0.800 000 GHz to 15.000 000 GHz Amplitude: 0.4 Vp-p to 1.0 Vp-p Connector: SMA (f), Termination: 50Ω/AC Coupling
Jittered Clock Output	Number of Output: 2 Amplitude: 0.4 Vp-p to 1.0 Vp-p Connector: SMA (f), Termination: 50Ω/AC Coupling
SJ1	Modulation Frequency: 10 Hz to 250 MHz Amplitude: 0 to 2000 UI @Modulation Frequency 10 kHz to 100 kHz 0 to 1 UI @Modulation Frequency 10 MHz to 250 MHz (Different depending on the operating bit rate)
Built-in SJ2	Modulation Frequency: 33 kHz, 87 MHz, 100 MHz, 210 MHz
Spread Spectrum Clocking (SSC)	Modulation Frequency: 28 kHz to 37 kHz Deviation: 0 to 7000 ppm
Random Jitter (RJ)	Bandwidth: 10 kHz to 1 GHz Amplitude: 0 to 0.5 UI (Different depending on the operating frequency)
Bounded Uncorrelated Jitter (BUJ)	PRBS Pattern Length: $2^n - 1$ (n = 7, 9, 11, 15, 23, or 31) BUJ Rate: 0.1 Gbit/s to 3.2 Gbit/s, 4.9 Gbit/s to 6.25 Gbit/s, 9.8 Gbit/s to 12.5 Gbit/s Filter Type (LPF 3 dB Bandwidth): 50, 100, 200, 300, 500 MHz, Through Amplitude: 0 to 0.5 UI (Different depending on the operating frequency)
External Jitter	Bandwidth: 10 kHz to 1 GHz

Noise Generator MU195050A

Number of Channels	2
Insertion Loss	–3 dB
CMI: Common Mode Noise	0.1 GHz to 6 GHz: Sinusoidal wave
DMI: Differential Mode Noise	2 GHz to 10 GHz: Sinusoidal wave
White Noise	10 MHz to 10 GHz
Crest Factor	>5

Signal Quality Analyzer-R MP1900A Specifications

Refer to the MP1900A Data Sheet (MP1900A_Datasheet-E-A-1) for detailed specifications.

21G/32G bit/s SI PPG MU195020A

Operation Rate (NRZ)	2.4 Gbit/s to 21 Gbit/s or 32.1 Gbit/s
Number of Channels	1 or 2
Output Amplitude	0.1 Vp-p to 1.3 Vp-p (Single-end) 0.2 Vp-p to 2.6 Vp-p (Differential)
Emphasis	10Tap
Channel Emulator	Normal: Emulates Insertion Loss using S-parameter data Inverse: Performs De-Emphasis compensation for S-parameter Insertion Loss S-Parameter file: S2P,S4P
ISI	Emulates ISI output using CEI-28G/25G Nyquist frequency loss setting Supports loss control in combination with ISI Board J1758A accessory Insertion Loss setting: 1.5 to 25 dB, 0.01 dB step, Nyquist frequency 0 to 25 dB, 0.01 dB step, 1/2 Nyquist frequency
Tr/Tf (20 to 80%)	12 ps (typ.)
Random Jitter	115 fs rms (typ.)
PCIe, USB Link Training	Supported (MX183000A-PL021/PL022/PL025)
Output Connector	K (f)

21G/32G bit/s SI ED MU195040A

Operation Rate (NRZ)	2.4 Gbit/s to 21 Gbit/s or 32.1 Gbit/s
Number of Channels	1 or 2
Input Attitude	0.05 Vp-p to 1.0 Vp-p (Single-End) 0.1 Vp-p to 2.0 Vp-p (Differential)
Input Sensitivity (Eye Height)	15 mV (28.1 Gbit/s, NRZ) 30 mV/Eye (28.1 Gbaud, PRBS15, PAM4)
CTLE	Peak Frequency: 14, 8, 4 GHz Gain: 0 to –12 dB
Clock Recovery	Yes, supports SSC
PCIe, USB Link Training	Supported (MX183000A-PL021/PL022/PL025)
Input Connector	K (f)

PAM4 PPG MU196020A

Operation Rate (PAM4/NRZ)	2.4 Gbaud to 32.1/58.2/64.2 Gbaud (option selection)
No. of Channels	1
Output Amplitude	70 mVp-p to 800 mVp-p (Single-end) 140 mVp-p to 1600 mVp-p (Differential)
Offset	–2 V to +3.3 V
Emphasis	4 Tap, –20 to +20 dB
Channel Emulator	Generates waveform with insertion loss and simulates waveform with corrected insertion loss Set by loading S-Parameter file (S2 P, S4 P)
ISI	Simulates ISI generation waveform Set using loss (–8.00 to 8.00 dB) at CEI-specified Nyquist frequency Used in combination with channel board, such as J1800A/J1758A (optional accessories parts), or Noise Module MU195050A
Independently Variable PAM4 3 Eye	20 to 50% (PAM4 Amplitude 0/3 level = 100%)
PAM4 Pattern	SSPRQ, PRBS13Q, PRBS31Q, RS-FEC, etc.
PAM4 Pattern Error Addition	MSB Error, LSB Error, LSB&MSB Error, RS-FEC Symbol Error
Tr/Tf (20 to 80%)	8.5 ps (typ., NRZ)
Random Jitter	170 fs rms (typ., NRZ)
Output Connector	V (f)

PAM4 ED MU196040B

Operation Rates (PAM4/NRZ)	2.4 Gbaud to either 32.1 Gbaud, or 58.2 Gbaud (PAM4)/64.2 Gbaud (NRZ) (option selection)
No. of Channels	1
Input Amplitude	NRZ: ≤32.1G: 0.05 Vp-p to 1.0 Vp-p, >32.1G: 0.1 Vp-p to 1.0 Vp-p PAM4: ≤32.1G: 0.3 Vp-p to 1.0 Vp-p, >32.1G: 0.4 Vp-p to 1.0 Vp-p
Input Sensitivity (Eye Height)	NRZ: 19 mV @ 26.5625 Gbaud, 21 mV @ 53.125 Gbaud PAM4: 23 mV @ 26.5625 Gbaud, 36 mV @ 53.125 Gbaud
Clock Recovery (Option)	2.4 Gbaud to 32.1 Gbaud, 51 Gbaud to 58.2 Gbaud
Equalizer (Option)	Low-frequency Equalizer (≤1 GHz, 2 dB typ.) + DFE (1.4 dB typ.)
PAM4 Patterns	SSPRQ, PRBS13Q, PRBS31Q, etc.
PAM4 Counter	MSB, LSB, Symbol 0 to 3 (Option)
Input Connector	V (f)

Signal Quality Analyzer-R MP1900A Ordering Information

When ordering, determine the configuration by referencing the selection guide (MP1900A-E-Z-1) and specify the type, model, name, and quantity.
The names listed in the chart below are Order Names. The actual name of the item may differ from the Order Name.

MP1900A

Model/Order No.	Name	
	Main Frame*1	
MP1900A	Signal Quality Analyzer-R	
	Standard Accessories	
G0342A	ESD DISCHARGER:	1
J1211	POWER CORD. 3M:	1
J1627A	GND connection cable:	1
P0031A	USB Memory:	1
Z0306A	Wrist Strap:	1
MX190000A	Signal Quality Analyzer-R Control Software*2	
MX183000A	High-Speed Serial Data Test Software*3, *4	
	Retrofit Option	
MP1900A-110	Windows10 Upgrade Retrofit*5	
	Maintenance Service	
MP1900A-ES310	Three Years Extended Warranty Service	
MP1900A-ES510	Five Years Extended Warranty Service	

*1: The Windows 10 OS will be installed in all orders from July 1, 2020.
*2: Standard software pre-installed in Signal Quality Analyzer-R MP1900A
*3: Trial software pre-installed in Signal Quality Analyzer-R MP1900A for extending functions with 30-day free trial period following first launch. When requiring the official version after the 30-day trial period, obtain the official license by purchasing the separate MX183000A-PLxx software license. Refer to the software license.
*4: The PAM4 Control function is bundled with the MX183000A as a standard function and can be used without a license.
*5: MP1900A main units running Windows Embedded Standard 7 are retrofitted to Windows 10 using a hardware upgrade. Anritsu destroys the unnecessary, post-upgrade Windows Embedded Standard 7 parts. For details, contact our sales representative.

MU181000B

Model/Order No.	Name	
	Module	
MU181000B	12.5 GHz 4port Synthesizer	
	Standard Accessories	
J1624A	Coaxial Cable 0.3 m (SMA, DC to 18 GHz):	4 pcs
	Option	
MU181000B-001	Jitter Modulation	
MU181000B-002	SSC Extension	
	Retrofit Option	
MU181000B-101	Jitter Modulation Retrofit	
MU181000B-102	SSC Extension Retrofit	
	Maintenance Service	
MU181000B-ES310	Three Years Extended Warranty Service	
MU181000B-ES510	Five Years Extended Warranty Service	

MU181500B

Model/Order No.	Name	
	Module	
MU181500B	Jitter Modulation Source	
	Standard Accessories	
J1624A	Coaxial Cable 0.3 m (SMA, DC to 18 GHz):	1 pc
J1508A	BNC-SMA Connector Cable (30 cm):	2 pcs
J1137	Terminator:	6 pcs
J1341A	Open:	2 pcs
Z0897A	MP1800A Manual CD:	1 pc
Z0918A	MX180000A Software CD:	1 pc
	Maintenance Service	
MU181500B-ES310	Three Years Extended Warranty Service	
MU181500B-ES510	Five Years Extended Warranty Service	

MU195050A

Model/Order No.	Name	
	Module	
MU195050A	Noise Generator	
	Standard Accessories	
J1632A	Terminator:	4
J1359A	Coaxial Adapter (K-P, K-J, SMA):	4
J1717A	COAXIAL ADAPTOR (SMA-P, SMA-J):	2
J1341A	Open:	6
J1746A	Skew Match Pair Semrigid Cable (K connector, Data Input1):	1 set
J1747A	Skew Match Pair Semrigid Cable (K connector, Data Input2):	1 set
J1792A	Skew Match Pair Semrigid Cable (V-K connector, MU196020A PPG Output to MU195050A Noise Data Input1):	1 set
	Option	
MU195050A-001	White Noise	
	Retrofit Option	
MU195050A-101	White Noise Retrofit	
	Maintenance Service	
MU195050A-ES310	Three Years Extended Warranty Service	
MU195050A-ES510	Five Years Extended Warranty Service	

Signal Quality Analyzer-R MP1900A Ordering Information

When ordering, determine the configuration by referencing the selection guide (MP1900A-E-Z-1) and specify the type, model, name, and quantity.

MU195020A

Model/Order No.	Name	
	Module	
MU195020A	21G/32G bit/s SI PPG	
	Standard Accessories	
J1632A	Terminator:	5
J1341A	Open:	2
J1359A	Coaxial Adapter (K-P, K-J, SMA):	1
J1717A	COAXIAL ADAPTOR (SMA-P, SMA-J):	6
	Option	
MU195020A-001	32G bit/s Extension	
MU195020A-010	1ch Data Output	
MU195020A-020	2ch Data Output	
MU195020A-011	1ch 10Tap Emphasis	
MU195020A-021	2ch 10Tap Emphasis	
MU195020A-030	1ch Data Delay	
MU195020A-031	2ch Data Delay	
MU195020A-040	1ch Variable ISI	
MU195020A-041	2ch Variable ISI	
MU195020A-050	Sequence Editor Function*6	
MU195020A-051	Sequence Editor Function PCIe 5 Extension*6	
	Retrofit Options	
MU195020A-101	32G bit/s Extension Retrofit	
MU195020A-120	2ch Data Output Retrofit	
MU195020A-111	1ch 10Tap Emphasis Retrofit	
MU195020A-121	2ch 10Tap Emphasis Retrofit	
MU195020A-130	1ch Data Delay Retrofit	
MU195020A-131	2ch Data Delay Retrofit	
MU195020A-140	1ch Variable ISI Retrofit	
MU195020A-141	2ch Variable ISI Retrofit	
MU195020A-350	Sequence Editor Function Retrofit	
	When Option 010/110 Installed	
J1632A	Terminator:	2
J1359A	Coaxial Adapter (K-P, K-J, SMA):	2
	When Option 020/120 Installed	
J1632A	Terminator:	4
J1359A	Coaxial Adapter (K-P, K-J, SMA):	4
	Maintenance Service	
MU195020A-ES310	Three Years Extended Warranty Service	
MU195020A-ES510	Five Years Extended Warranty Service	

*6: Option 050 supports PCIe Gen 1 to Gen 4, and USB 3.2 ×1. Option 051 supports PCIe Gen5. Option 050 is required when adding Option 051.

MU196020A*11

Model/Order No.	Name	
	Module	
MU196020A	PAM4 PPG	
	Standard Accessories	
J1632A	TERMINATOR:	4
V210	TERMINATOR (V):	2
J1341A	OPEN:	2
J1359A	COAXIAL ADAPTOR (K-P.K-J,SMA):	1
J1717A	COAXIAL ADAPTOR(SMA-P.SMA-J):	5
	Option	
MU196020A-001	32G baud*	
MU196020A-002	58G baud*	
MU196020A-003	64G baud*	
MU196020A-011	4Tap Emphasis	
MU196020A-030	Data Delay	
MU196020A-040	Adjustable ISI	
MU196020A-042	FEC Pattern Generation	
MU196020A-050	Inter-Module Synchronization	
	Retrofit Options	
MU196020A-112	32G to 58G baud Extension Retrofit	
MU196020A-113	32G to 64G baud Retrofit	
MU196020A-123	58G to 64G baud Retrofit	
MU196020A-111	4Tap Emphasis Retrofit	
MU196020A-130	Data Delay Retrofit	
MU196020A-140	Adjustable ISI Retrofit	
MU196020A-142	FEC Pattern Generation Retrofit	
MU196020A-150	Inter-Module Synchronization Retrofit	
	Maintenance Service	
MU196020A-ES310	Three Years Extended Warranty Service	
MU196020A-ES510	Five Years Extended Warranty Service	

*: Select any one

MU195040A

Model/Order No.	Name	
	Module	
MU195040A	21G/32G bit/s SI ED	
	Standard Accessories	
J1632A	Terminator:	2
J1341A	Open:	1
J1717A	COAXIAL ADAPTOR (SMA-P, SMA-J):	4
	Option	
MU195040A-001	32G bit/s Extension	
MU195040A-010	1ch ED	
MU195040A-020	2ch ED	
MU195040A-011	1ch CTLE	
MU195040A-021	2ch CTLE	
MU195040A-022	Clock Recovery	
	Retrofit Options	
MU195040A-101	32G bit/s Extension Retrofit	
MU195040A-120	2ch ED Retrofit	
MU195040A-111	1ch CTLE Retrofit	
MU195040A-121	2ch CTLE Retrofit	
MU195040A-122	Clock Recovery Retrofit	
	When Option 010/110 Installed	
J1341A	Open:	3
J1359A	Coaxial Adapter (K-P, K-J, SMA):	2
J1887A	Fixed Attenuator (6 dB, K Connector):	2
	When Option 020/120 Installed	
J1341A	Open:	5
J1359A	Coaxial Adapter (K-P, K-J, SMA):	4
J1887A	Fixed Attenuator (6 dB, K Connector):	4
	Maintenance Service	
MU195040A-ES310	Three Years Extended Warranty Service	
MU195040A-ES510	Five Years Extended Warranty Service	

MU196040B*11

Model/Order No.	Name	
	Module	
MU196040B	PAM4 ED	
	Standard Accessories	
J1632A	TERMINATOR:	2
V210	TERMINATOR (V):	2
J1341A	OPEN:	2
J1359A	COAXIAL ADAPTOR (K-P.K-J,SMA):	1
J1717A	COAXIAL ADAPTOR (SMA-P.SMA-J):	3
41V-6	Fixed Attenuator 6 dB:	2
	Option	
MU196040B-001	32G baud (2.4G to 32.1G)	
MU196040B-002	58G baud (NRZ: 2.4G to 64.2G, PAM4: 2.4G to 58.2G)	
MU196040B-011	Equalizer	
MU196040B-021	29G baud Clock Recovery (2.4G to 29G)	
MU196040B-022	32G baud Clock Recovery (2.4G to 32.1G)	
MU196040B-023	58G baud Clock Recovery Extension (51G to 58.2G)	
MU196040B-041	SER Measurement	
	Retrofit Options	
MU196040B-111	Equalizer Retrofit	
MU196040B-112	32G to 58G baud Extension Retrofit	
MU196040B-121	29G baud Clock Recovery Retrofit	
MU196040B-122	32G baud Clock Recovery Retrofit	
MU196040B-123	58G baud Clock Recovery Extension Retrofit	
MU196040B-124	32G baud Clock Recovery Extension Retrofit	
MU196040B-141	SER Measurement Retrofit	
	Maintenance Service	
MU196040B-ES310	Three Years Extended Warranty Service	
MU196040B-ES510	Five Years Extended Warranty Service	

Signal Quality Analyzer-R MP1900A Ordering Information

When ordering, determine the configuration by referencing the selection guide (MP1900A-E-Z-1) and specify the type, model, name, and quantity.

MU183020A

Model/Order No.	Name	
	Module	
MU183020A	28G/32G bit/s PPG	
	Standard Accessories	
J1137	Terminator:	3 pcs
J1359A	Coaxial Adaptor (K-P, K-J, SMA):	1 pc
J1341A	Open:	1 pc
J0541E	6 dB Fixed Attenuator:	1 pc
Z0897A	MP1800A Manual CD:	1 pc
Z0918A	MX180000A Software CD:	1 pc
	Options	
MU183020A-001	32G bit/s Extension	
MU183020A-012	1ch 2 V Data Output	
MU183020A-013	1ch 3.5 V Data Output	
MU183020A-022	2ch 2 V Data Output	
MU183020A-023	2ch 3.5 V Data Output	
MU183020A-030	1ch Data Delay	
MU183020A-031	2ch Data Delay	
	Retrofit Options	
MU183020A-101	32G bit/s Extension Retrofit	
MU183020A-112	1ch 2 V Data Output Retrofit	
MU183020A-113	1ch 3.5 V Data Output Retrofit	
MU183020A-122	2ch 2 V Data Output Retrofit	
MU183020A-123	2ch 3.5 V Data Output Retrofit	
MU183020A-130	1ch Data Delay Retrofit	
MU183020A-131	2ch Data Delay Retrofit	
	Standard Accessories for MU183020A-x12, x13	
J1137	Terminator:	2 pcs
J1359A	Coaxial Adaptor (K-P, K-J, SMA):	2 pcs
	Standard Accessories for MU183020A-x22, x23	
J1137	Terminator:	4 pcs
J1359A	Coaxial Adaptor (K-P, K-J, SMA):	4 pcs
	Maintenance Service	
MU183020A-ES310	Three Years Extended Warranty Service	
MU183020A-ES510	Five Years Extended Warranty Service	

MU183040B

Model/Order No.	Name	
	Module	
MU183040B	28G/32G bit/s High Sensitivity ED	
	Standard Accessories	
J1137	Terminator:	2 pcs
J1341A	Open:	1 pc
Z0897A	MP1800A Manual CD:	1 pc
Z0918A	MX180000A Software CD:	1 pc
	Options	
MU183040B-001	32 Gbit/s Extension	
MU183040B-010	1ch ED	
MU183040B-020	2ch ED	
MU183040B-022	2.4G to 28.1G bit/s Clock Recovery	
MU183040B-023	25.5G to 32.1G bit/s Clock Recovery	
	Retrofit Options	
MU183040B-101	32 Gbit/s Extension Retrofit	
MU183040B-110	1ch ED Retrofit	
MU183040B-120	2ch ED Retrofit	
MU183040B-122	2.4G to 28.1G bit/s Clock Recover Retrofit	
MU183040B-123	25.5G to 32.1G bit/s Clock Recovery Retrofit	
	Standard Accessories for MU183040B-x10	
J1341A	Open:	2 pcs
J1359A	Coaxial Adaptor (K-P, K-J, SMA):	2 pcs
41KC-6	Precision Fixed Attenuator 6 dB:	2 pcs
	Standard Accessories for MU183040B-x20	
J1341A	Open:	4 pcs
J1359A	Coaxial Adaptor (K-P, K-J, SMA):	4 pcs
41KC-6	Precision Fixed Attenuator 6 dB:	4 pcs
	Maintenance Service	
MU183040B-ES310	Three Years Extended Warranty Service	
MU183040B-ES510	Five Years Extended Warranty Service	

Software License

Model/Order No.	Name
MX183000A	High-Speed Serial Data Test Software
MX183000A-PL001	Jitter Tolerance Test
MX183000A-PL011	PCIe Link Sequence
MX183000A-PL021	PCIe Link Training*7
MX183000A-PL022	USB Link Training*8
MX183000A-PL023	USB 3.2 × 2 Link Training*8
MX183000A-PL025	PCIe 5 Link Training*7
MX183000A-PL031	DUT Error Counts Import

*7: The PL021 option supports PCIe Gen1 to Gen4.
The PL025 option supports PCIe Gen5. PL021 is required to add PL025.
*8: PL022 supports USB 3.2 ×1. PL023 supports USB 3.2 ×2. PL022 is required to add PL023.

On Using VISA*9

The National Instruments™ (NI hereafter) NI-VISA*10 software must be installed to use the MX183000A (this product hereafter). We recommend using NI-VISA saved on the product USB memory stick.
Customers may only use NI-VISA saved on the product memory stick. NI-VISA on the memory stick may not be used for other applications with other products.
When uninstalling this product from the controller PC, etc., also uninstall NI-VISA from the USB memory.

*9: Abbreviation for Virtual Instrument Software Architecture. This is I/O software for remote control of measuring instruments via GPIB, Ethernet and USB interfaces.
*10: NI-VISA was developed by National Instruments for VXI Plug&Play Alliance standards compliant I/O interfaces.
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Optional Accessories

Model/Order No.	Name
J1632A	Terminator
V210	TERMINATOR (V)
J1678A	ESD Protection Adapter-K
J1679A	ESD Protection Adapter-V
J1359A	Coaxial Adapter (K-P, K-J, SMA)
34VFK50A	Fixed Adapter (V-F, K-M)*11
34VKF50A	Fixed Adapter (V-M. K-F)
41KC-3	Fixed Attenuator 3 dB
41KC-6	Fixed Attenuator 6 dB
41KC-10	Fixed Attenuator 10 dB
41KC-20	Fixed Attenuator 20 dB
41VA-3	Fixed Attenuator 3 dB
41VA-6	Fixed Attenuator 6 dB
41VA-10	Fixed Attenuator 10 dB
41VA-20	Fixed Attenuator 20 dB
J1887A	Fixed Attenuator (6 dB, K Connector)
J1758A	ISI Board
J1800A	ISI Board V
K261	DC Block
K240C	Precision Power Divider
V240C	Fixed Power divider
J1510A	Pick OFF Tee (K)
J1793A	Pick OFF Tee (V)
K241C	Power Splitter
J1748A	Power Splitter (1.5 GHz to 18 GHz, SMA, using MU195020A × 4 to MU181500B connection)
J1624A	COAXIAL CABLE 0.3 m (18 GHz and SMA)
J1342A	COAXIAL CABLE 0.8 m (APC3.5 connector)
J1439A	Coaxial cable (0.8 m, K connector)
J1625A	Coaxial Cable 1 m (18 GHz, SMA)
J1449A	Measurement kit (J1324A × 2, J1439A × 2, J1625A × 1)

Model/Order No.	Name
J1550A	Coaxial skew match cable (0.8 m, APC3.5 connector)
J1551A	Coaxial skew match cable (0.8 m, K connector)
J1728A	Electrical Length Specified Coaxial Cable (0.4 m, K connector)
J1741A	Electrical Length Specified Coaxial Cable (0.8 m, K Connector)
J1789A	Electrical Length Specified Coaxial Cable*11 (0.4 m, V connector)
J1790A	Electrical Length Specified Coaxial Cable*11 (0.8 m, V connector)
J1792A	Skew match pair semirigid cable (V-K connector, MU196020A PPG Output to MU195050A Noise Data Input1)
J1761A	PCIe Reference Clock Cable Kit
Z2025A	PCIe CBB Controller
Z2029A	PCIe Reference Clock Buffer
J1890A	PCIe5 Re-Driver Set
G0430A	PCIe5 Re-Driver Set
AH54192A	56Gbaud Differential Linear Amplifier
W3911AE	MP1900A Operation Manual
W3913AE	MX190000A Operation Manual
W3813AE	MX183000A Operation Manual
W3915AE	MU195020/40/50A Operation Manual
W3976AE	MU196020/40A OPERATION MANUAL
B0576A	Blank Panel
B0736A	Front Cover (For MP1900A)
B0737A	Carrying Case (For MP1900A, with B0736A)
B0738A	Rack Mount Kit (For MP1900A)
Z1746A	Stylus
Z0541A	USB Mouse
J0008	GPIB CABLE, 2.0 m
Z0917A	Shielded LAN Cable, 5 m
Z1953A	Gigabit Ethernet Switch (5 Port)
Z0306A	Wrist Strap
Z1964A	Torque Wrench (Right Angle)

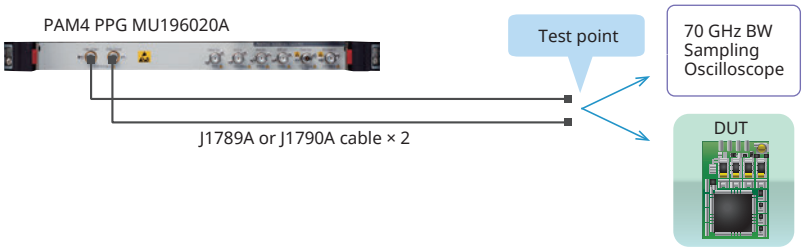
J1815A MP1900A PCIe Measurement Component Set

The following table lists the component set required by the PCIe Gen3/4/5 Tx/Rx LEQ test.

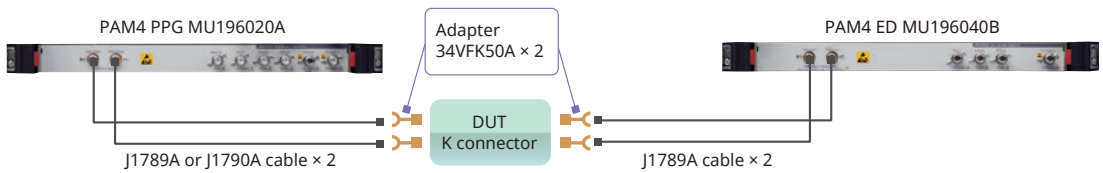
Item	Description	Qty.	Remarks
Optional Accessories	MP1900A PCIe Measurement Component Set	1	J1815A

Accessories	Qty.	Comment
Coax skew match cable, 0.8 m K connector	4	Junflon J12J103220-00-1
AE-TMC-10205	2	Coax cable, 1 m, SMA connector
PICK OFF TEE	2	Anritsu 3-68231
SMPF-SMAJ-TFLEX-10CM-5PS	2	SMP to SMA adapter cable
BNC-SMA cable	2	
K261	2	DC Block
K241C	2	Power Splitter

*11: We recommend using either the J1789A or J1790A as the coaxial cable for the MU196020A data output. Recommend using coaxial cable J1789A for MU196040B Data IN. The MU196020A data output specifications are defined based on the performance observed using a 70-GHz bandwidth oscilloscope connected as shown below.



The MU196020A Data OUT and MU196040B Data IN connectors, and the J1789A/J1790A cables all use V-connectors. Consequently, for K-connectors, use 34VFK50 adapters as shown in the following figure.



DUT Connection Setup for K-connectors

Anritsu Advancing beyond

Specifications are subject to change without notice.

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