Application Note

Anritsu envision : ensure

USB Type-C based Thunderbolt Generation 3 and USB 3.1 RX test solution

Signal Quality Analyzer MP1800A Series

Table of Contents

1 Outline

This article outlines Anritsu's Thunderbolt 3 (TBT 3 below) and USB 3.1 Rx Test Solution, test procedures, and precautions.

More PCs and peripheral equipment using USB Type-C connectors are being released commercially recently. USB Type-C uses the latest USB 3.1 standard and an industry group called USB-IF (USB Implementers Forum, Inc. http://www.usb.org/home) creating standards for the latest USB connectors has been established as a not-for-profit organization. The USB Type-C connector is already used on Apple MacBook laptops and PCs by Dell and other makers.

This connector has a flippable feature and it can supply up to 100 W of power if the Power Delivery standard is supported.

Although USB 3.1 generation 1 (Gen 1 below) supports transmission speeds of 5 Gbps, and USB 3.1 Generation 2 (Gen 2 below) supports transmission speeds of 10 Gbps, when operating in USB Type-C Alternative Mode, TBT 3 is supported with transmission speeds of 40 Gbps (20 Gbps x 2 lanes), which is four times faster than USB 3.1 Gen 2.

To display compliance with the standards, equipment using USB 3.1 and TBT requires verification testing at quarterly events such as USB Workshop, TBT PlugFest, etc. Anritsu participates as a USB and TBT vendor at both these events to promote equipment certification.

In addition, Anritsu's MP1800A has received world-first approval from Intel Corporation as an official measuring instrument for TBT 3 certification. Moreover, official approval for USB 3.1 testing is expected to be received from USB-IF at WS-103 to be held in 2017.

2 Test Preparation

To obtain certification as a test instrument for USB 3.1 and TBT 3, it is necessary to gain approval at events held each quarter. USB test events are sponsored by USB-IF, and TBT are sponsored by Intel Corporation (http://www.intel.com/content/www/us/en/io/thunderbolt/thunderbolt-technology-developer.html). Additionally, development of equipment conforming to the Thunderbolt standards requires a Technical License Agreement (TLA hereafter) with Intel Corporation.

Anritsu offers Rx tolerance test solutions for both USB and TBT devices installed in USB Type-C connectors. Additionally, Anritsu also offers automatic calibration software developed in cooperation with GRL Corporation (http://graniteriverlabs.com/anritsu-mp1800a/) for test signals required by Rx tolerance tests.

Anritsu's USB 3.1 and TBT 3 Solution features software switching of the test target signals without changing the physical connection. In many cases, USB 3.1 and TBT 3 are installed in the same chip package and reconnection can be omitted because both high-speed interfaces can be tested by one connection.

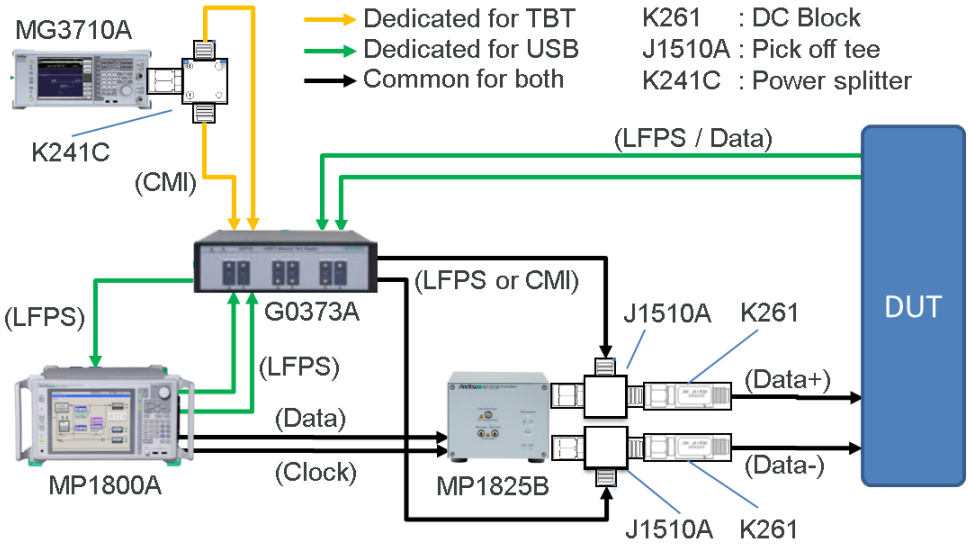


Fig. 2 USB 3.1/TBT 3 Test System

3 Thunderbolt Test

The TBT host receiver test specifies near end (TP2) and far end (TP3EQ) test points.

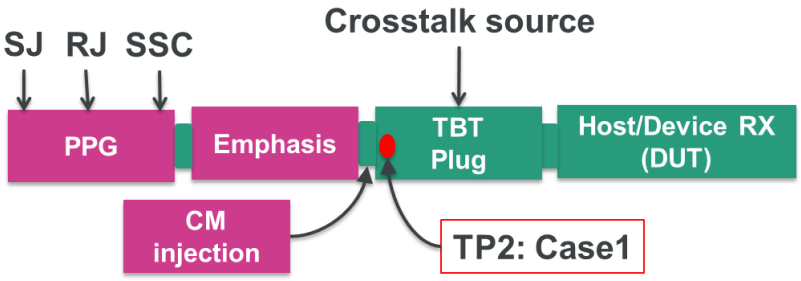


Fig. 3.1 TBT Near End Test Point (TP2)

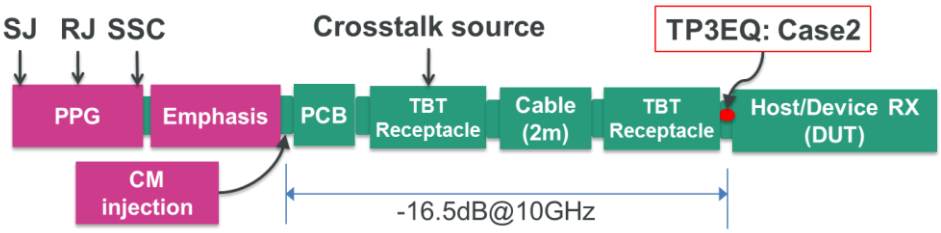


Fig. 3.2 TBT Far End Test Point (TP3EQ)

The test specifies applying sinusoidal Jitter, random Jitter, Spread Spectrum Clocking, and Common Mode noise from the measurement equipment side at both the TP2 and TP3EQ test points. Moreover, at BER measurement, an 800 mV differential divided clock signal is input as the Crosstalk Aggressor to the side that is not the measurement target of bidirectional TBT lanes.

3.1 Equipment Setup

The TBT 3 test equipment setup is shown below.

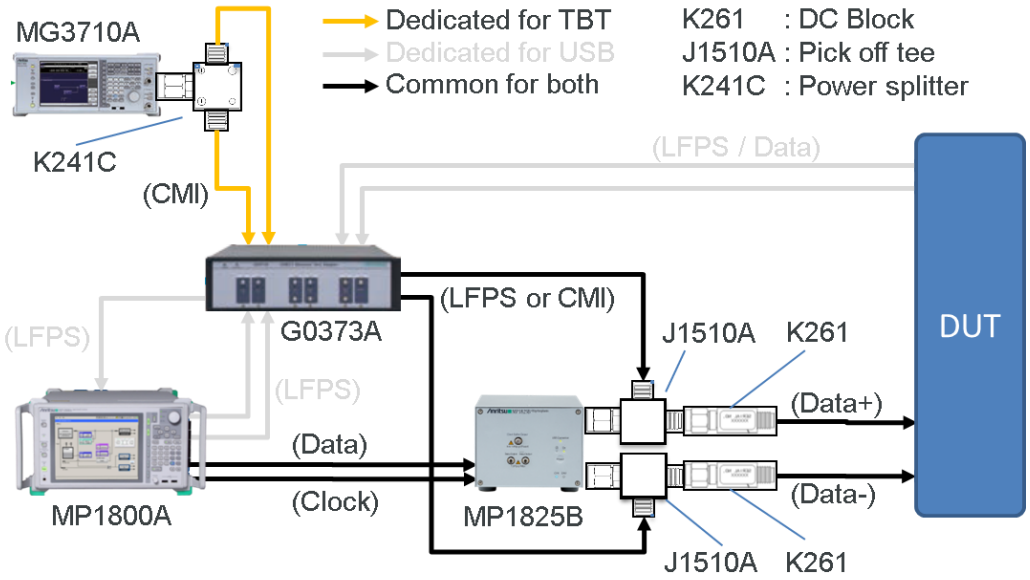


Fig. 3.3 TBT Test Setup

The gray lines with arrows in the above figure are only for the USB test setup and are not required for the TBT test.

Moreover, the G0373A is not required if only performing TBT tests. In this case, connect directly to the J1510A from the MG3710A K241C power splitter.

Table 3.1 TBT Test Configuration

Model Number	Model Name	Options	Qty	Note
MP1800A	Signal Quality Analyzer	002, 007, 015, 032	1	Main frame
MU181000B	4 Port Synthesizer	-	1	Synthesizer
MU181500B	Jitter Generation Module	-	1	Jitter source
MU183020A	28G/32G bit/s PPG	012, 030	1	PPG
MP1825B	4Tap Emphasis	002	1	Emphasis
MG3710A	Vector Signal Generator	002, 029, 032, 041	1	
G0373A	USB3.1 USB Test Receiver Adapter		1	Required for USB test
GRL-TBT3-RXA	GRL Thunderbolt3 Receiver Calibration and Test Software		1	
J1510A	Pick Off Tee	-	2	
K261	DC Block	-	2	
K241C	Power Splitter	-	1	
J1551A	Skew Matched 0.8 m K	-	1	Emphasis to DUT for Data
J1550A	Skew Matched 0.8 m APC3.5	-	1	MG3710A to G0373A
J1624A	0.3 m SMA	-	2	G0373A to J1510A
J1611A	1.3 m K	-	1	PPG–Emphasis for Clock
J1439A	0.8 m K	-	1	PPG–Emphasis for Data

3.2 Waveform Calibration and BER Measurement

Calibrate the waveform before starting the test. Since this is described in the MOI included in the GRL-TBT3-RXA packaging, this section only summarizes the waveform calibration. Perform calibration at each of the TP2 and TP3EQ test points described previously.
First, with Emphasis disabled, set the Eye inner amplitude to a differential of 700 mVp-p.

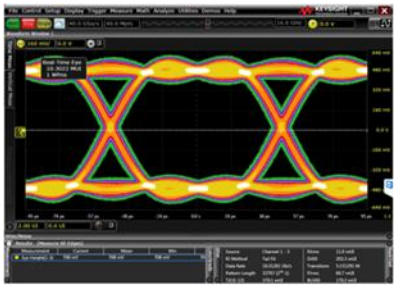


Fig3.4 Inner Eye Amplitude Setting

Then, perform the 16 different Emphasis settings specified in the TBT standards and choose the Emphasis setting where the DDJ is smallest.

Fig. 3.5 Selecting Minimum DDJ Setting from 16 Emphasis Settings

After choosing the Emphasis setting, set the Common Mode Interference (CMI hereafter) amplitude and frequency. After setting the optimum value. Set the CMI output to Off to perform subsequent calibration.
Additionally, perform calibration for random Jitter, sinusoidal Jitter and total Jitter. At calibration for each of the first two Jitter types, apply either random Jitter or sinusoidal Jitter only and set the other Jitter to off.

Fig. 3.6 RJ/SJ/TJ Adjustment

On completing both the sinusoidal Jitter and random Jitter calibrations, set both Jitters and CMI to On and measure the total Jitter. Basically, total Jitter should be the required value at this stage but if it does not match the required value, when the sinusoidal Jitter is 100 MHz, change the sinusoidal Jitter value and if the sinusoidal Jitter value is not 100 MHz, change the random Jitter value to match the final target value.
After completing Jitter calibration, adjust the Eye inner height to complete the waveform calibration.
Next, connect the DUT as shown below, and perform the final Good/No Good test evaluation.
Connect the output of the measuring instrument passing via the Intel Plug/Receptacle Fixture to the DUT and

measure the BER at the above-described calibrated stress signal with sinusoidal Jitter applied at the points specified in the TBT Compliance Test Specification. At the TBT Jitter tolerance test, it is not necessary to transition the DUT to the Loopback mode; BER measurement uses the DUT built-in BER counter and Good/No Good evaluation of this result is handled either by the PC with installed TBT 3 chip or TBT micro controller.
The BER measurement result is passed if it is E-12 or better.

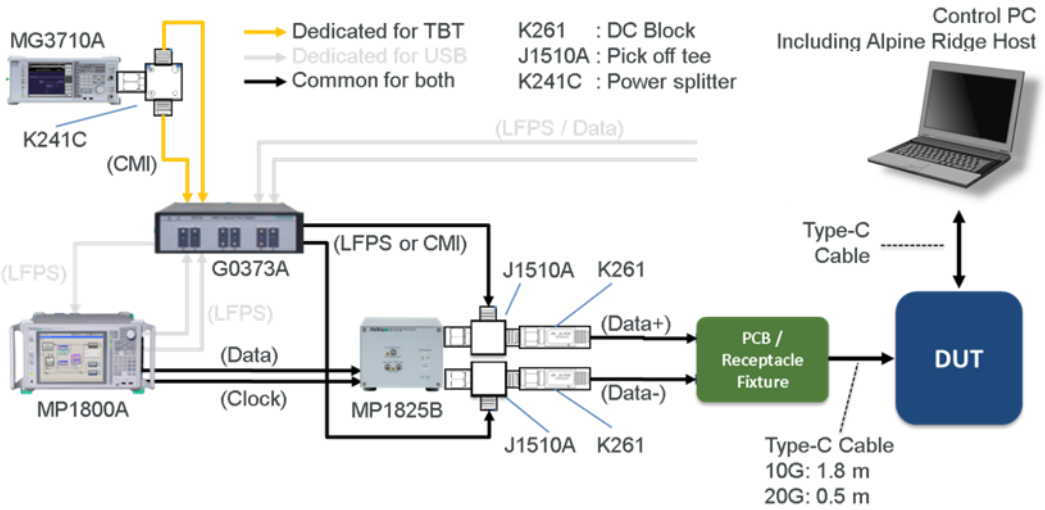


Fig. 3.7 TBT Test Setup (TP3EQ)

4 USB Test

USB 3.1 has two operating statuses: Gen 1 operating at 5 Gbps, and Gen 2 operating at 10 Gbps. At the Rx stress test, since test target generation is specified and BER is measured with the stressed waveform applied, it is necessary to transition to the Loopback mode. Setting this operation state is performed by using communications using a low-speed signal called the Low Frequency Pulse Sequence (LFPS) between the DUT and measuring instrument at connector connection.
There are two test targets: the device and host, and a different fixture is used for each. The fixture can be obtained from the USB-IF website.

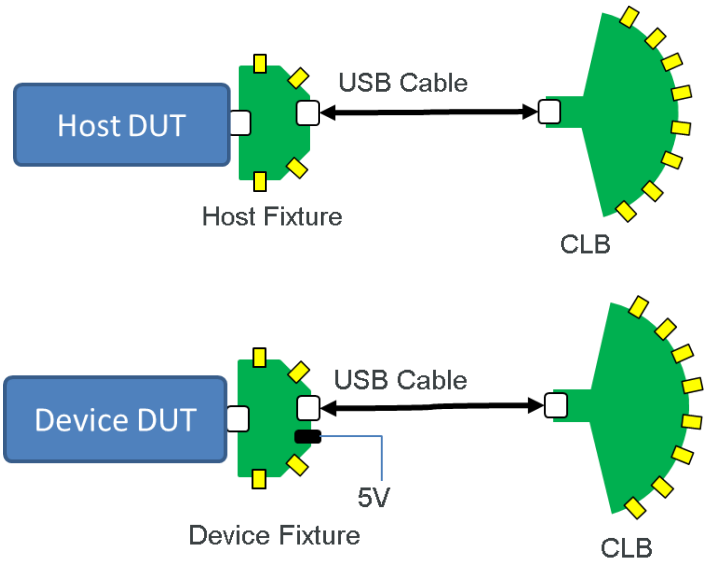


Fig. 4.1 USB Test Fixtures

4.1 Equipment Setup

The following figure shows the USB 3.1 test setup.

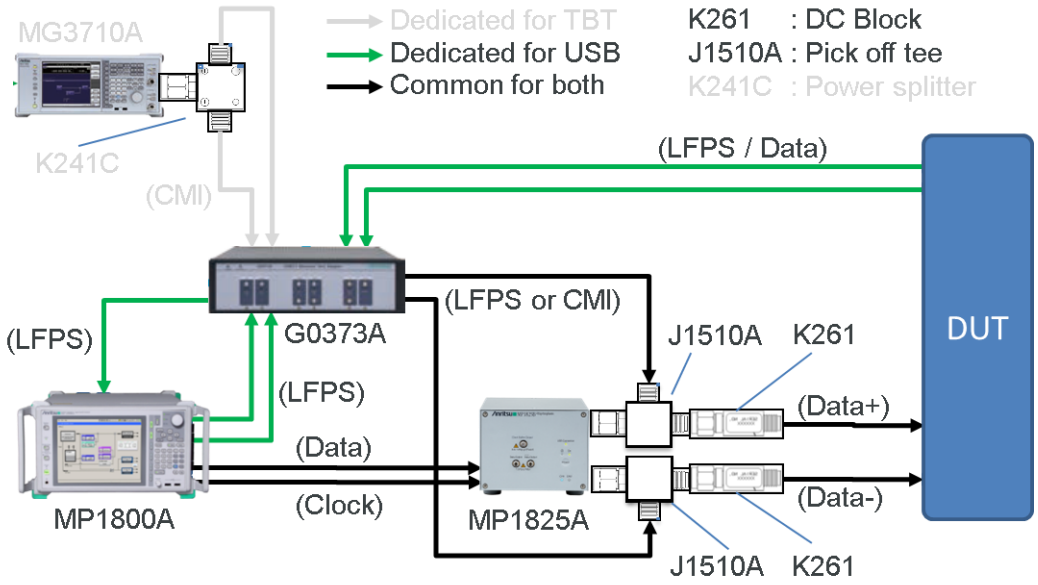


Fig. 4.2 USB Test Setup

The gray lines with arrows in the above figure are required only for TBT tests and are unnecessary for USB tests. Similarly, the MG3710A and K241C are also unnecessary when using for USB tests. Additionally, the DC Block K261 between the DUT and MP1825B is also not required for USB tests. These parts will not cause problems if they remain in the test setup when using for combined TBT testing.

Table 4.1 USB Test Configuration

Model Number	Model Name	Options	Qty	Note
MP1800A	Signal Quality Analyzer	002, 007, 015, 032	1	Main Frame
MU181000B	4 Port Synthesizer	-	1	Synthesizer
MU181500B	Jitter Generation module	-	1	Jitter source
MU183020A	28G/32G bit/s PPG	012, 030	1	PPG
MP1825B	4Tap Emphasis	002	1	Emphasis
G0373A	USB3.1 USB Test Receiver Adapter		1	
GRL-USB31-RXA	GRL USB3.1 Receiver Calibration and Test Software		1	
USB SigTest	Version 4.0.19 or above			USB-IF www.usb.org
J1510A	Pick Off Tee	-	2	
K261	DC Block	-	2	Not required for USB
J1551A	Skew matched 0.8 m K	-	2	Emphasis to DUT for Data
J1625A	1.0 m SMA	-	3	G0373A to MP1800A
J1624A	0.3 m SMA	-	2	G0373A to J1510A
J1611A	1.3 m K	-	1	PPG–Emphasis for Clock
J1439A	0.8 m K	-	1	PPG–Emphasis for Data

4.2 Waveform Calibration and BER Measurement

Calibration must be performed also before starting USB 3.1 tests. Since this is described in the MOI included in the GRL-TBT3-RXA packaging, this section only summarizes the waveform calibration.
The USB 3.1 specifications issued by USB-IF specify Rx stress tests using the following target values. In other words, generate the following signals from the measuring instruments and perform Good/No Good evaluation.

Table 4.2 Input Jitter Requirements for Rx Tolerance Testing

Symbol	Parameter	Gen 1 (5GT/s)	Gen 2 (10GT/s)	Units	Notes
f1	Tolerance corner	4.9	7.5	MHz	
J_{RJ}	Random Jitter	0.0121	0.01308	UI rms	1
$J_{RJ\_P\text{-}P}$	Random Jitter peak- peak at 10^{-12}	0.17	0.184	UI p-p	1,4
J_{PJ_500kHz}	Sinusoidal Jitter	2	4.76	UI p-p	1,2,3
J_{PJ_1Mhz}	Sinusoidal Jitter	1	2.03	UI p-p	1,2,3
J_{PJ_2MHz}	Sinusoidal Jitter	0.5	0.87	UI p-p	1,2,3
J_{PJ_4MHz}	Sinusoidal Jitter	N/A	0.37	UI p-p	1,2,3
J_{PJ_f1}	Sinusoidal Jitter	0.2	0.17	UI p-p	1,2,3
J_{PJ_50MHz}	Sinusoidal Jitter	0.2	0.17	UI p-p	1,2,3
J_{PJ_100MHz}	Sinusoidal Jitter	N/A	0.17	UI p-p	1,2,3
V_full_swing	Transition bit differential voltage swing	0.75	0.8	V p-p	1
V_EQ_level	Non transition bit voltage (equalization)	-3	Preshoot=2.7 De-emphasis= -3.3	dB	1

Notes:

1. All parameters measured at TP1. The test point is shown in Figure 6-19.
2. Due to time limitations at compliance testing, only a subset of frequencies can be tested. However, the Rx is required to tolerate Pj at all frequencies between the compliance test points.
3. During the Rx tolerance test, SSC is generated by test equipment and present at all times. Each J_{Pj} source is then added and tested to the specification limit one at a time.
4. Random jitter is also present during the Rx tolerance test, though it is not shown in Figure 6-20.
5. The JTOL specs for Gen 2 comprehend jitter peaking with re-timers in the system and has a 25dB/decade slope.

TP1 in the above table is the output connector of the measuring instrument.

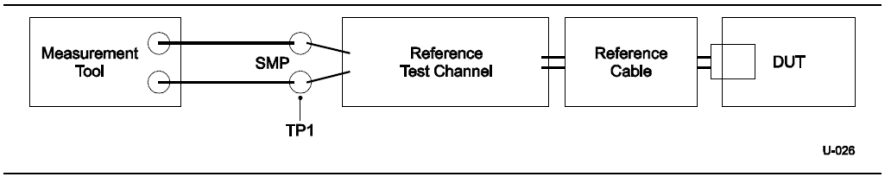
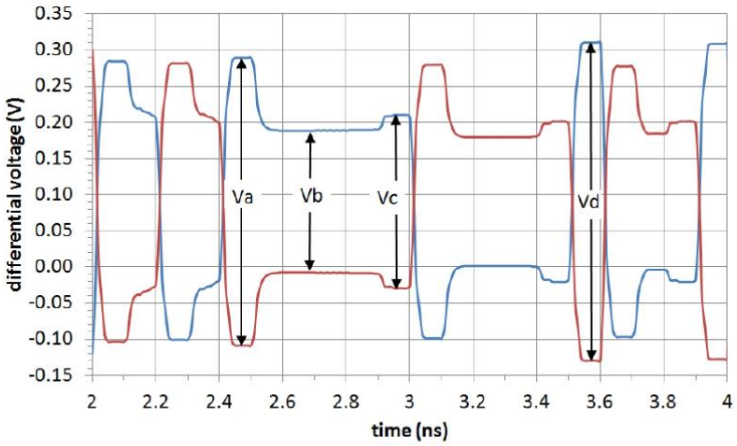


Fig 4.3 Tx Normative Setup with Reference Channel

In addition, V_EQ_Level in Table 4.2 is calculated from Preshoot and De-emphasis using the following equation.



Preshoot = 20log(Vc/Vb)
De-emphasis = 20log(Vb/Va)

Fig 4.4 Example Output Waveform for 3-tap Transmit Equalizer

After calibrating the waveform, connect as shown in Fig. 4.5 and perform Good/No Good evaluation. For USB 3.1 Gen 2 , the result is passed if there is 1 or less errors in a period of 120 seconds while the stressed signal is applied.

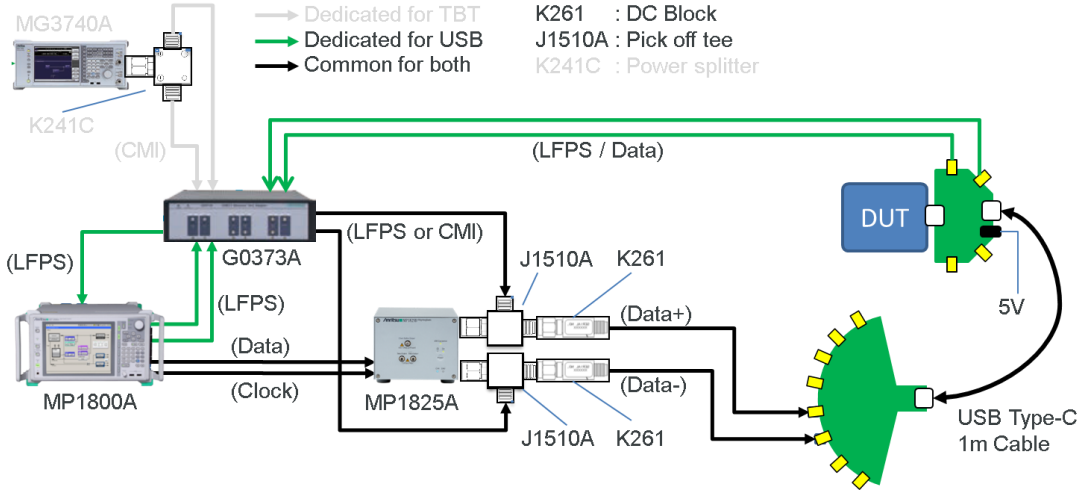


Fig 4.5 USB Test Setup

4.3 Precautions

The following describes precautions when performing USB 3.1 tests.

First, the USB Type-C cable itself is flippable and can be used in both front and back orientations but at the Compliance test, note that the cable is not flippable because the measuring instrument itself is not connected to all routes. Although the CLB, Host Fixture, and Device Fixture are used when connecting the DUT and measuring instrument, the signal passage route is fixed. Perform testing after having confirmed the CLB and Fixture connection locations and the USB back and front.

Next, when performing the test, the LFPS signal is determined by the Gen 1/Gen 2 usage but communications are established immediately after connecting the device. If communications using the LFPS fail for some reason, such as a loose connector connection, etc., the transition to the Loopback mode may not occur. Since communications using LFPS are not re-stablished automatically, note that it is necessary to disconnect the fixture from the DUT and reconnect.

Furthermore, at connection of a USB device such as memory storage, the Device Test Fixture requires a +5 V power supply unlike the Host Test Fixture for connecting a USB host such as a PC.

Moreover, as shown in Fig 4.6, there are two pairs of jumper short pins (CC1 and CC2) on the Test Fixture. When the CC1 pair is shorted, Rx1 can be used, and when the CC2 pair is shorted, Rx2 can be used. Either the CC1 or the CC2 pair must be shorted, Neither Rx1 nor Rx2 can be used if both pairs are shorted or open at the same time.

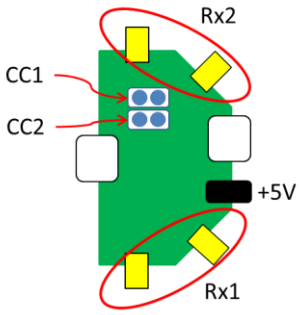


Fig. 4.6 Device Test Fixture

As another precaution, if Emphasis applied to the signal from the DUT side is either too strong or too weak, the transition to the Loopback mode may not performed correctly so the test may not be performed correctly.
Take care to note the above points at USB testing.

5 Anritsu Solution

Anritsu offers a solution in partnership with GRL Corporation for testing Thunderbolt 3 and USB 3.1 Gen 1/2 using USB Type-C. The Anritsu BERT MP1800A Signal Quality Analyzer has a synchronous multi-channel high-quality waveform PPG as well as the world's best-of-class high-sensitivity ED with precision Jitter generation function, supporting accurate measurement results with extremely high reproducibility.

Combining the MP1800A with GRL's automatic waveform calibration software simplifies the complex waveform calibration procedure as well as supports repeated testing under the same measurement conditions.

6 Remarks

Universal Serial Bus 3.1 Specification Revision.1.0

USB Type-C Thunderbolt Alternate Mode Electrical Host/Device Compliance Test Specification Rev. 1.5 Version 0.81

GRL Thunderbolt 3 Receiver MOI

GRL USB 3.1 Receiver MOI

Anritsu envision : ensure

Specifications are subject to change without notice.

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