ORTEC®

DSPEC 50 and DSPEC 502

Advanced, Fourth-Generation ORTEC DSP-Based Gamma-Ray Spectrometers for Germanium Detectors

• Hardware Features

- Single MCA (DSPEC 50) and dual MCA (DSPEC 502) versions.
- Highly stable against variations in count rate and temperature.
- PHA and List Mode acquisitions.
- Automated set-up: Automatic Pole Zero Adjust, Baseline Restorer, and Optimize.[1]
- High throughput capabilities for high count rate applications.
- Digital spectrum stabilizer.
- USB 2.0 and Ethernet capability (TCP/IP protocol).
- Large front panel display for at-a-glance system status information.
- Support for all HPGe detector types, old and new.

• Advanced DSP Algorithms Ensure Enhanced Spectroscopic Performance

- Correct treatment of highly variable count rates and short half lives: ZDT “loss free” dead-time correction with uncertainty calculation.[2]
- Low Frequency Rejection (LFR) mode improves resolution by rejection of low frequency noise, e.g., electrical line noise or vibration-induced microphonics.
- Resolution Enhancer improves FWHM of HPGe detectors with degradation due to charge trapping, e.g., from radiation damage.
- Enhanced Throughput Mode for the ultimate in high throughput counting, up to 30% boost in system throughput.

[1]Patent No. 5,872,363
[2]Patent No. 6,327,549

Experience-Based Performance

DSPEC 50 and DSPEC 502 salute the 50th year in which ORTEC has delivered innovative and quality nuclear instrumentation to scientists in a broad range of applications world wide. Fifteen years after the first ORTEC DSPEC® digital spectrometer received acclaim among spectroscopists for its performance and stability, the new DSPEC 50 and DSPEC 502 are landmark products which bring together our long design experience in digital spectrometers and the ongoing innovation skills of our developers.[3]

The “retro” look front panel, which incorporates a built-in display, a reminder of earlier times in the evolution of multichannel analyzers, but inside, the DSPEC 50 is packed full of the latest digital signal processing technology and quality design.

Digital spectrometers are inherently more stable than the analog variety common in the past. In introducing the DSPEC 50, ORTEC has launched an all-new digital instrument platform, enhanced with a number of unique features and modes of operation which have distinct benefit in real-world applications.

DSPEC 50 Features at a Glance

For High-Rate Spectroscopy Applications

“Loss Free” or “Zero Dead Time” (ZDT)
The usual way to account for counting losses at high rates is by extending the acquisition time. The underlying assumption is that the sample count rate does not change during the total counting period. This is far from true when short half lives are encountered or the sample is in motion (e.g., flowing through a pipe). ORTEC has refined the loss-free counting technique in the digital domain. In this method, the spectrum itself is corrected pulse by pulse, and the ZDT method provides both an accurately corrected spectrum and correctly calculated statistical uncertainty.

“Enhanced Throughput” Mode
Accuracy at high input count-rates can be limited by the speed at which the spectrometer stores data to memory. It is said to be “throughput-limited.” Pulse pileup means that beyond a certain point, as input count-rate increases still further, the rate of data stored to memory DECREASES, reducing result quality. By developing a new kind of digital peak detection algorithm, ORTEC has increased the maximum throughput by up to 30% by removing some of the dead time associated with the process of pulse peak amplitude determination.

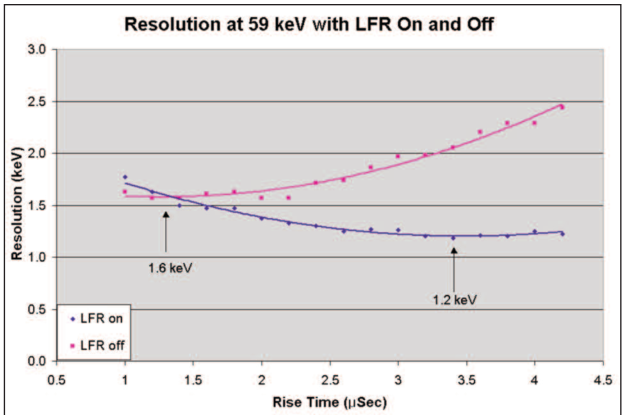
For Samples in Motion

List Mode
For situations in which the sample is moving relative to the detector, it is often vitally important to be able to measure an activity profile as a function of time. Examples of such applications include aerial and land-based surveying and portal monitoring. It is usually a requirement that no “dead periods” occur, associated with the acquire-store-clear-restart cycle. In the list mode of operation, data are streamed directly to the computer, event by event. There is no associated “dead period.” In the DSPEC 50 implementation, each event is timestamped to an accuracy of 200 nanoseconds. Via the use of the A11-B32 Programmer’s Toolkit, the data may be made into a spectrum for off-line analysis by one of ORTEC’s wide range of analysis software products or user-developed codes.

[3]In the remainder of this document the statement DSPEC 50 refers to both models unless otherwise stated.

For Hostile Environments and Mechanical Coolers

Low-Frequency Rejector (LFR)
HPGe detectors do not always perform well in environments where there is mechanical vibration. Microphonic noise degrades energy resolution by adding low frequency periodic electrical noise to the primary signal. Electrical ground loops are also a source of low frequency electrical noise. The increasing use of mechanical coolers for HPGe detectors to eliminate the need for LN_2 and increasing need to take HPGe detectors out of the laboratory environment mean an increase in mechanical vibration. DSPEC 50 incorporates a Low-Frequency Rejecter (LFR) Filter feature, which reduces the effects of such noise sources.

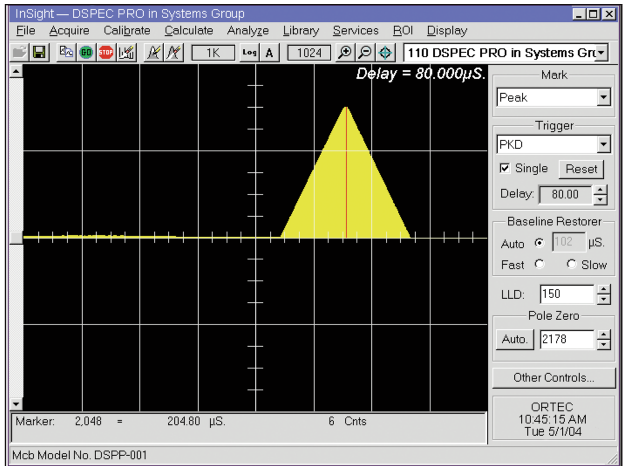


The effect of the LFR filter on a mechanically cooled HPGe detector.

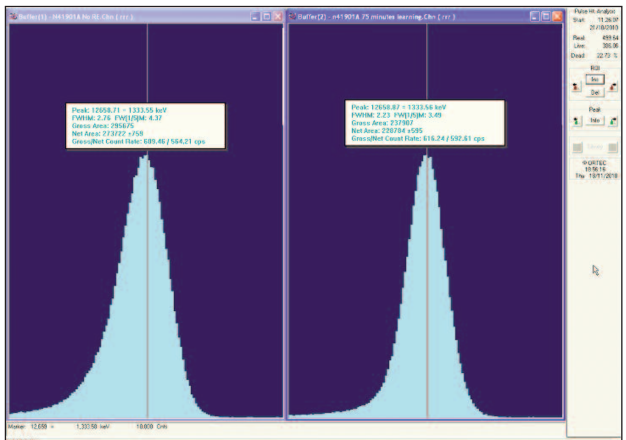
For Enhancement of Resolution in Large or Neutron Damaged Detectors

Ballistic Deficit and Charge Trapping Correction
The trapezoidal digital filter in the DSPEC 50 is the same as all other ORTEC DSPEC family members. It allows adjustment of the filter to optimize the resolution performance of large HPGe detectors which often have low-side peak tailing when ballistic deficit is present. These large detectors are increasing in use in low level counting applications. The adjustment is largely automated by the use of the "OPTIMIZE" feature and may be monitored by the InSight™ Virtual Oscilloscope mode.

The DSPEC 50 offers even further capability in the form of the Resolution Enhancer, a charge trapping corrector which can be used to reduce the peak degradation for neutron damaged detectors. The neutron damage to the crystal lattice causes "trapping" centers which hold some of the charge created by the gamma-ray interaction. This results in low-side tailing similar to ballistic deficit although the cause is different. The charge trapping corrector is calibrated or "trained" for the individual detector such that it adds back the pulse height deficit, event by event.



InSight Virtual Oscilloscope Mode.



The charge trapping corrector improves FWHM resolution by 20% on an N-type detector.

DSPEC 50 Display Modes

The large color display of the DSPEC 50 is used in the initial set-up of the Ethernet communications. The status displays can be used to provide several standard views:

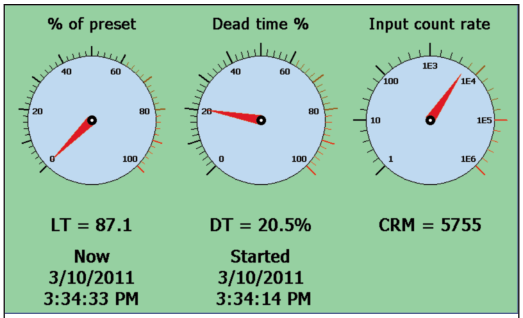
The "Gauges Display"
The gauges display provides a simple-to-read analog representation of the system acquisition status, the green background indicates "count in progress".

The "Big Numbers" Display
The big numbers display provides status information clearly visible from a distance.

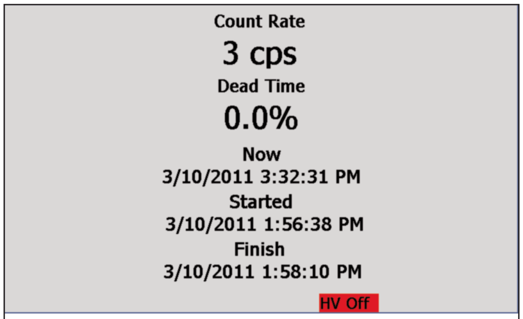
The "Chart" Display
The chart display monitors count-rate, dead time, and gain stabilizer activity during acquisition, thereby providing reassurance that all is well. The gain stabilizer display is only shown when the gain stabilizer is enabled.

Spectrum Display
The spectrum display provides a live spectral display which will show all ROIs set in the unit. In addition, ROIs may be set for the net area which can be used to perform a simple activity estimate based on the net area, the live time, and a user supplied factor (yellow). This permits the display of on-screen activity estimates for acquiring peaks.

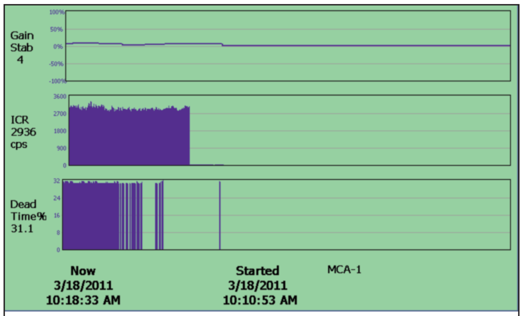
Displays Set-Up Screen
A simple to use displays set-up screen allows a user to choose what is displayed and the duration of the display type if more than one is chosen. User supplied JPGs may also be displayed.



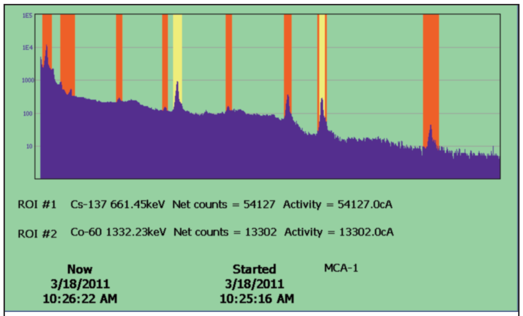
The "Gauges" Display.



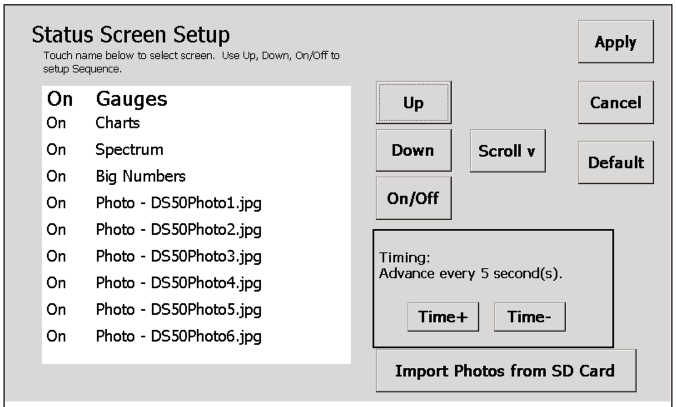
The "Big Numbers" Display.



The "Chart" Display.



The "Spectrum" Display.



Display Set-Up Screen.

DSPEC 50 Specifications

Display: 7” backlit color LCD provides status information. Displayed information is selectable by the user.

USB 2.0 Connection: For use when connecting one or more DSPEC 50 or 502 instruments to a single computer. ORTEC CONNECTIONS software supports up to 255 USB-connected devices per computer.

Ethernet Connection: Allows control of a DSPEC 50 from one or more PCs across a network. Standard 10/100M Ethernet connection. TCP/IP Protocol. Link and Activity LEDs are integrated into the RJ-45 connector.

System Gain Settings:

Coarse Gain: 1, 2, 4, 8,16 ,32, 64, and 128.

Fine Gain: 0.5 to 1.1.

The available range of gain settings supports all types of HPGe detectors. Specifically, the following maximum energy values are achievable using the standard ORTEC preamplifier (maximum gain to minimum gain):

COAX	187 keV to 24 MeV
LO-AX	94 keV to 12 MeV
GLP/SLP	16.5 keV to 2 MeV
IGLET-X	8 keV to 1 MeV

Preamplifiers: Computer selectable as either resistive or TRP preamplifier.

System Conversion Gain: The system conversion gain is software controlled from 512 to 16k channels.

Digital Filter Shaping-Time Constants:

Rise Times: 0.8 μs to 23 μs in steps of 0.2 μs.

Flat Tops: 0.3 to 2.4 in steps of 0.1 μs.

Digital Spectrum Stabilizer: Controlled via computer, stabilizes gain and zero errors.

System Temperature Coefficient

Gain: <50 ppm/°C. [Typically <30 ppm/°C.]

Offset: <5 ppm/°C of full scale, with Rise and Fall times of 12 μs, and Flat Top of 0.8 μs. (Similar to analog 6 μs shaping.)

Maximum System Throughput: >100,000 cps with LFR off. >34,000 cps with LFR on. Depends on shaping parameters.

Pulse Pile-Up Rejecter: Automatically set threshold. Pulse-Pair Resolution: Typically <500 ns.

Automatic Digital Pole-Zero Adjustment: Computer controlled. Can be set automatically or manually. Remote diagnostics via InSight Oscilloscope mode. (Patented.)

Digital Gated Baseline Restorer: Computer controlled adjustment of the restorer rate (High, Low, and Auto). (Patented.)

LLD: Digital lower level discriminator set in channels. Hard cutoff of data in channels below the LLD setting.

ULD: Digital upper level discriminator set in channels. Hard cutoff of data in channels above the ULD setting.

Ratemeter: Count-rate display on MCA and/or PC screen.

Battery: Internal battery-backed up memory to maintain settings in the event of a power interruption.

Inputs and Outputs

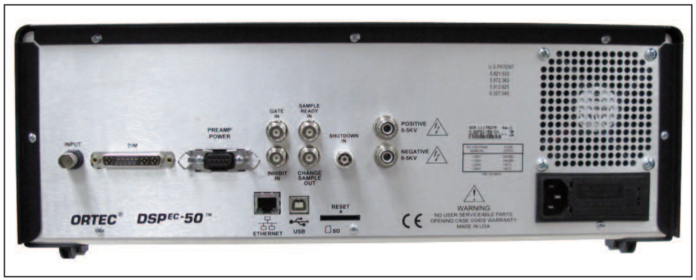
If both MCAs are installed (502 model), each MCA has each of the following connectors:

Detector: Multipin connector (13W3) with the following:

Preamp Power: 1 W maximum (+12 V, –12 V, +24 V, –24 V, 2 GND).
Analog In: Normal amplifier input.
TRP Inhibit.
Power for SMART-1 or DIM.
Control of HV and SMART-1 Detector (2 wires).

Analog In: Rear-panel BNC accepts preamplifier signals of either polarity, with rise times less than the selected Flat Top Time setting and exponential decay time constant in the range of 40 µs to infinity (including transistor-reset and pulsed-optical reset preamplifiers). Input impedance >500 Ω, input is dc-coupled and protected to ±12 V.

ADC Gate In: Rear-panel BNC accepts slow positive NIM input; computer selectable as off, coincidence, or anticoincidence. ADC GATE must overlap and precede



the Flat Top region by 0.5 µs, and extend beyond the Flat Top region by 0.5 µs. InSight Oscilloscope allows easy alignment of the ADC GATE signal with the digital output pulse.

Inhibit In: Rear-panel BNC connector accepts reset signals from transistor-reset (TRP) or pulsed-optical (POF) preamplifiers. Positive NIM logic or TTL level can be used. Inhibit input initiates the protection against distortions caused by preamplifier reset. This includes turning off the baseline restorer, monitoring the overload recovery, and generating the pile-up reject and busy signals for the duration of the overload. These last two signals are used internally to provide information to the dead-time correction circuitry.

USB 2.0: Universal serial bus for PC communications.

Ethernet Connection: Standard 10/100M Ethernet connection. Link and Activity LEDs are integrated into the connector.

Electrical and Mechanical

Change Sample Out: Rear panel BNC connector, TTL compatible.

Sample Ready In: Rear-panel BNC connector, accepts TTL level signal from Sample Changer. Software selectable polarity.

Preamp Power Out: Rear-panel, 9-pin D connector; provides ±24 V and ±12 V for preamplifier power.

Dimensions: 42.55 cm W x 35.56 cm D x 15.24 cm H (16.75 in. W x 14 in. D x 6 in. H).

Weight
DSPEC 50: 11 kg (24.25 lbs).
DSPEC 502: 11.7 kg (25.8 lbs).

Power
Input Voltage: 100–220 V AC.
Input Frequency: 47–63 Hz.
110 watts.

Operating Environment: 0° to 50°C.

Operating Systems: Windows® 2000/XP/7.

HPGe Detector High Voltage Supplies

DSPEC 50 offers high voltage supply flexibility having both internal HV supplies and support for ORTEC DIM and SMART-1 detector HV systems.

Internal HV Supplies

Positive Output: Rear-panel SHV connector, +500 to +5 kV. Computer controlled. Only active when the unit is set for positive bias.

Negative Output: Rear-panel SHV connector, –500 to –5 kV. Computer controlled. Only active when the unit is set for negative bias.

Shutdown In: Rear-panel BNC is used to turn off the bias supply voltage in the event that the detector warms up. The SHUTDOWN must be connected to the Bias Shutdown of the detector, or the high voltage will not turn on. The remote shutdown may be set to ORTEC or TTL mode via computer control.

In ORTEC mode, the Remote Shutdown has the following properties:

- An open circuit applied to the SHUTDOWN input indicates a warm detector; therefore, the high voltage is turned off.
- Drawing a current of 0.33 mA from the SHUTDOWN input indicates a cool detector; therefore, the high voltage can be turned on.

In TTL Mode, the Remote Shutdown has the following properties:

- An open circuit or a >2.4 V signal on the input indicates that the detector is cool.
- A <0.8 V signal on the input indicates that the detector is warm and the supply should be off.

The SHUTDOWN input is clamped at –700 mV by an internal clamp. For use with a detector without a shutdown circuit, this feature can be defeated by being left open in TTL mode.

DIM and SMART-1 Detector Types

On a SMART-1 HPGe detector, the HV module is integral with the detector itself. For “legacy” or “non-SMART-1” detectors, the HV supply is in the form of a Detector Interface Module or “DIM” with 2 m cables. The DIM has a mating connector for the traditional detector cable set: 9-pin D preamp power cable, Analog In, Shutdown In, Bias Out, and Inhibit In.

DIMS for non-SMART-1 detectors are available with the following high voltage options:

DIM-POSGE: Detector Interface Module for ANY Non-SMART-1 positive bias HPGe detector.

DIM-NEGGE: Detector Interface Module for ANY Non-SMART-1 negative bias HPGe detector.

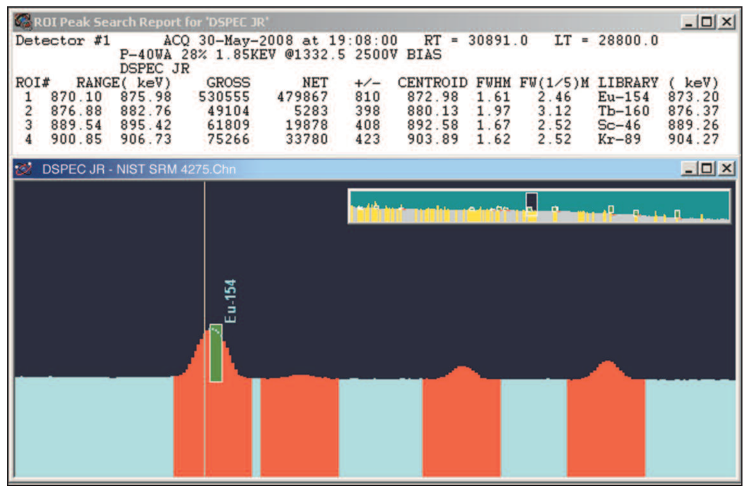
DIM-POSNAI: Detector Interface Module for ANY positive bias NaI detector.

DIM-296: Detector Interface Module with Model 296 ScintiPack tube base/preamplifier/bias supply for NaI detectors with 14-pin, 10 stage photomultiplier tubes.

Front Panel Display: In all cases, Bias Voltage Setting and Shutdown polarity are set from the computer. The DSPEC 50 can monitor the output voltage and shutdown state; Detector high voltage value (read only); and Detector high voltage state (on/off) are displayed on the front panel LCD. The SMART-1 detector provides additional state-of-health information by monitoring the following functions: Detector element temperature (read only); Detector overload state; and Detector serial number (read only).

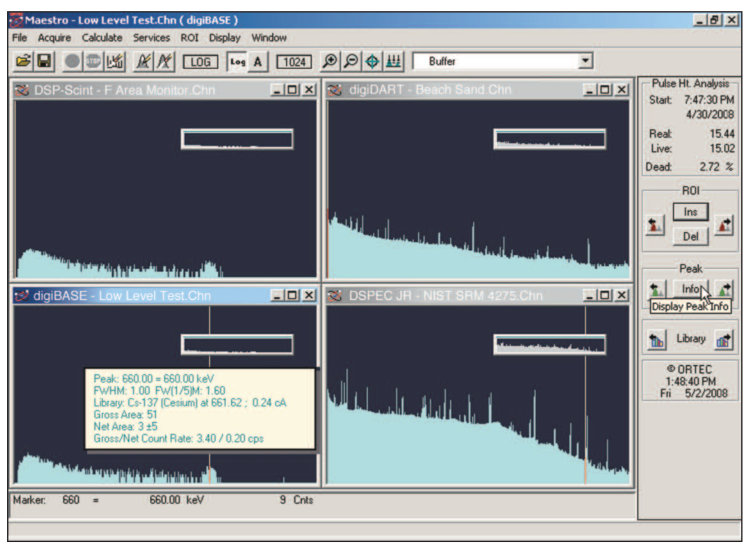
MAESTRO MCA Software

The DSPEC 50 includes the benchmark MCA software MAESTRO. MAESTRO gives full control of the data to the user with the latest features. The Multiple Detector Interface allows viewing up to 8 live, acquiring detectors and 8 static buffer windows simultaneously for a total of 16 interactive windows.



Features Include:

- Microsoft Windows user interface for control and spectrum manipulation using the mouse or keyboard.
- Multi-Detector Interface (MDI).
- Single key or mouse button for:
  - Setting/deleting ROIs
  - Indexing to next ROI
  - Indexing to next peak
  - Indexing to next library energy
  - Logarithmic and auto-scaling-linear vertical display
  - Real-time display on any mix of MCBs
  - Identical operation for local MCBs and network MCBs



Advanced Features of MAESTRO

- Mariscotti fast peak search, with nuclide identification by library lookup.
- Activity, net and gross areas (with uncertainty), centroid and shape for peaks.
- Data protection with "detector locking" by name, not by workstation.
- Comprehensive JOB STREAMING.
- Integrated Local Area Network (LAN) support.

For further details of MAESTRO and of the other optional software packages, visit: http://www.ortec-online.com/Solutions/applications-software.aspx.

Ordering Information

• Detector connection cable not included.

Model	Description
DSPEC-50	DSPEC 50 with MAESTRO Software, single MCA, and single internal High Voltage Power Supply.
DSPEC-502	DSPEC 502 with MAESTRO Software, two MCAs, and two internal High Voltage Power Supplies.
Detector Connection Cable	
931431	Detector Interface Module (DIM) cable, 4-ft length.
683410	Detector Interface Module (DIM) cable, 10-ft length.

Optional Equipment

The ASC2 Automatic Sample Changer is ideal for labs processing a large number of samples with minimal operator interaction allowing for routine counting outside of normal working hours – without the extra labor costs.

ASC2 Sample Changer.

Specifications subject to change
101512

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