S32K144 PMSM SINGLE-SHUNT SOLUTION

JASON YANG

NOV 2019

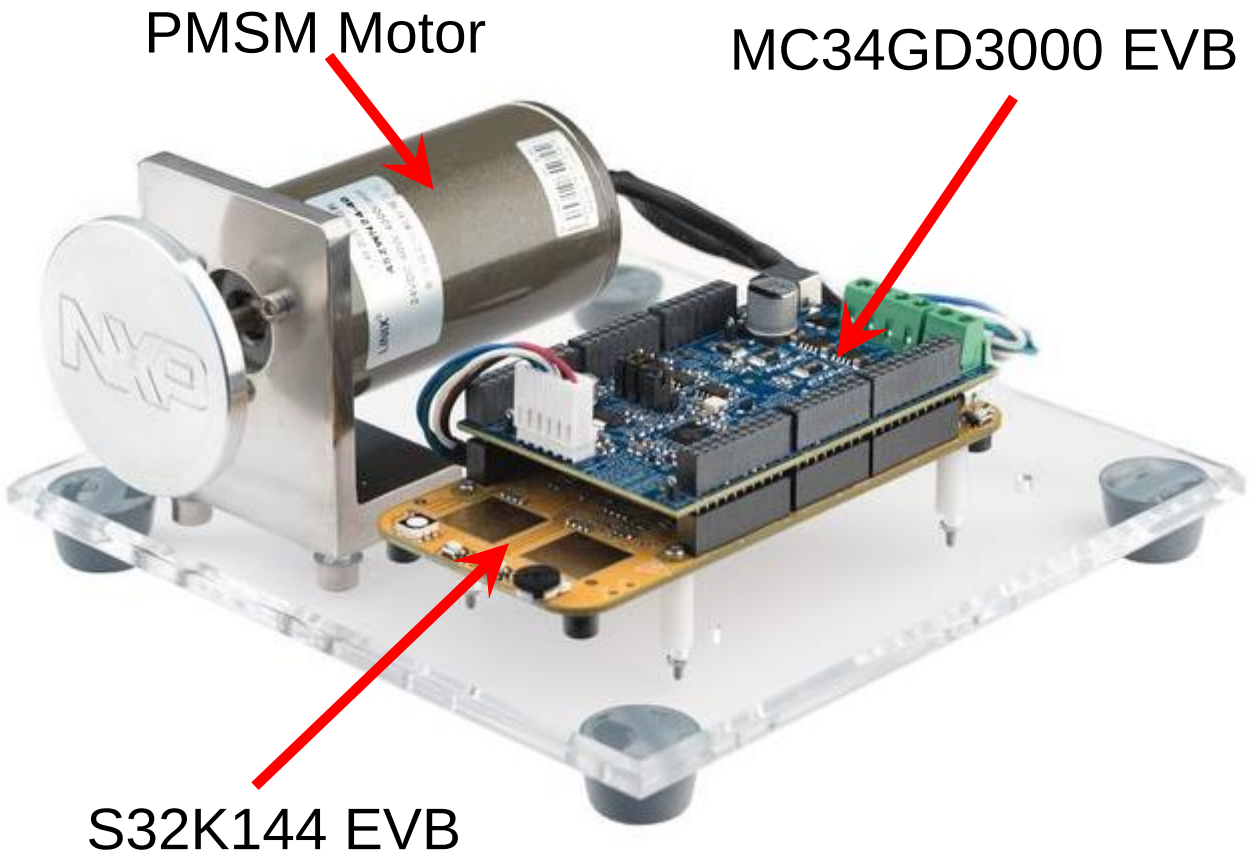
Agenda

- Hardware Overview
- S32K144 Motor Control Peripherals
  - TRGMUX, FTM, PDB, ADC
- Dual-Shunt Solution
- Single-Shunt Solution
  - Basic mechanism
  - Double-switch PWM generation
  - Timing and synchronization
  - Software execution time
  - Issues and solution

HARDWARE OVERVIEW

MTRDEVKSPNK144: 3-phase PMSM Development Kit

- 32-bit NXP S32K144 controller board
- 3-phase low-voltage power stage DEVKIT-MOTORGD based on SMARTMOS® MC34GD3000 pre-driver
- Supports low-voltage PMSM motors
- DC-bus overvoltage, overcurrent and under-voltage fault detection
- **Demo software** (Rev1.3) created in S32 Design Studio for Arm®
- FreeMASTER visualization/configuration support
- **Quick Start Guide and Schematic** available
- **Application note** coming soon



Connections

FTM3 – PWM output to GD3000

ADC0_CH4 – Phase A current sampling

ADC1_CH15 – Phase B current sampling

ADC1_CH6 – DC bus current sampling

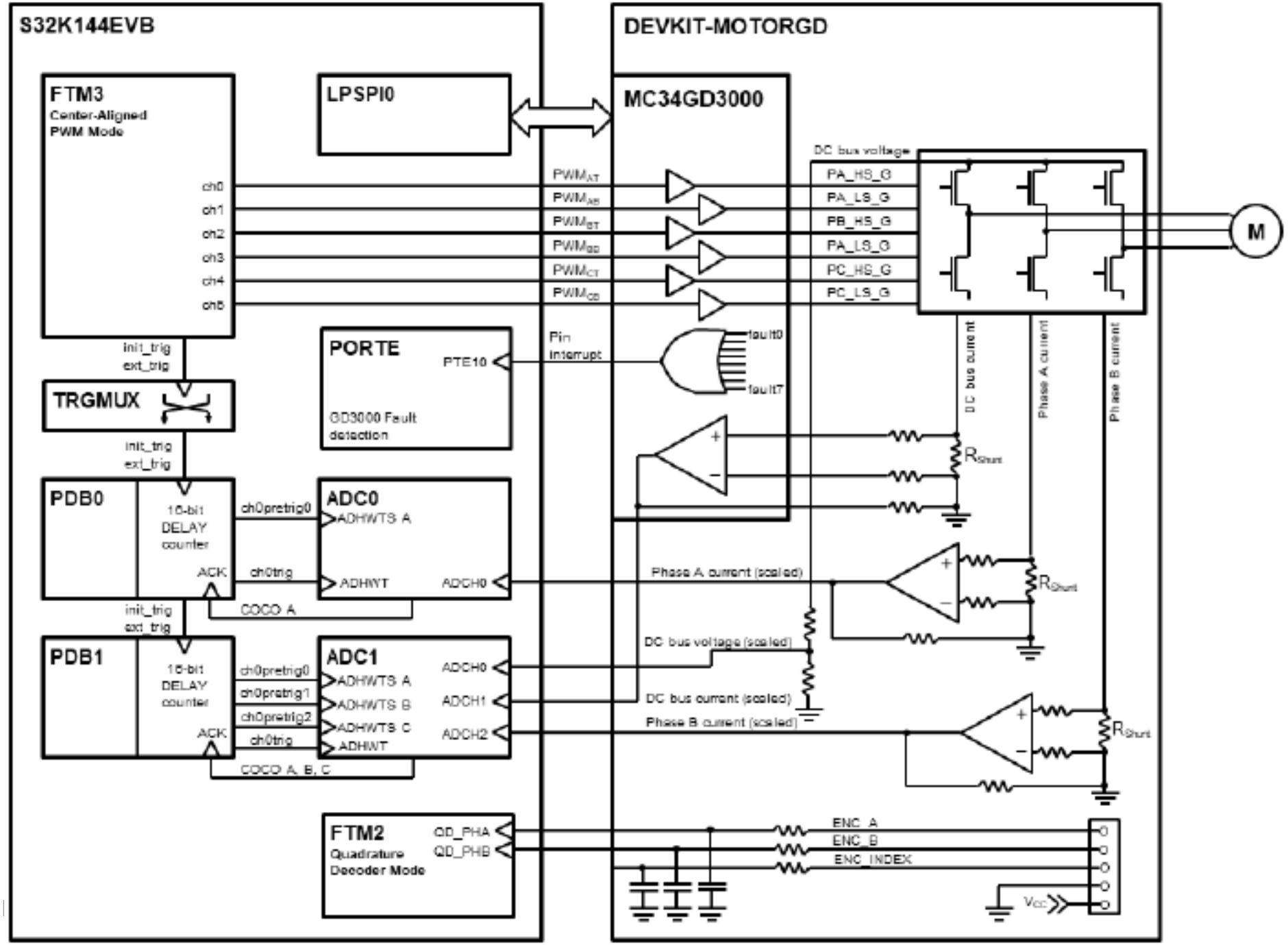
ADC1_CH7 – DC bus voltage sampling

LPSPI0 – Interface with GD3000

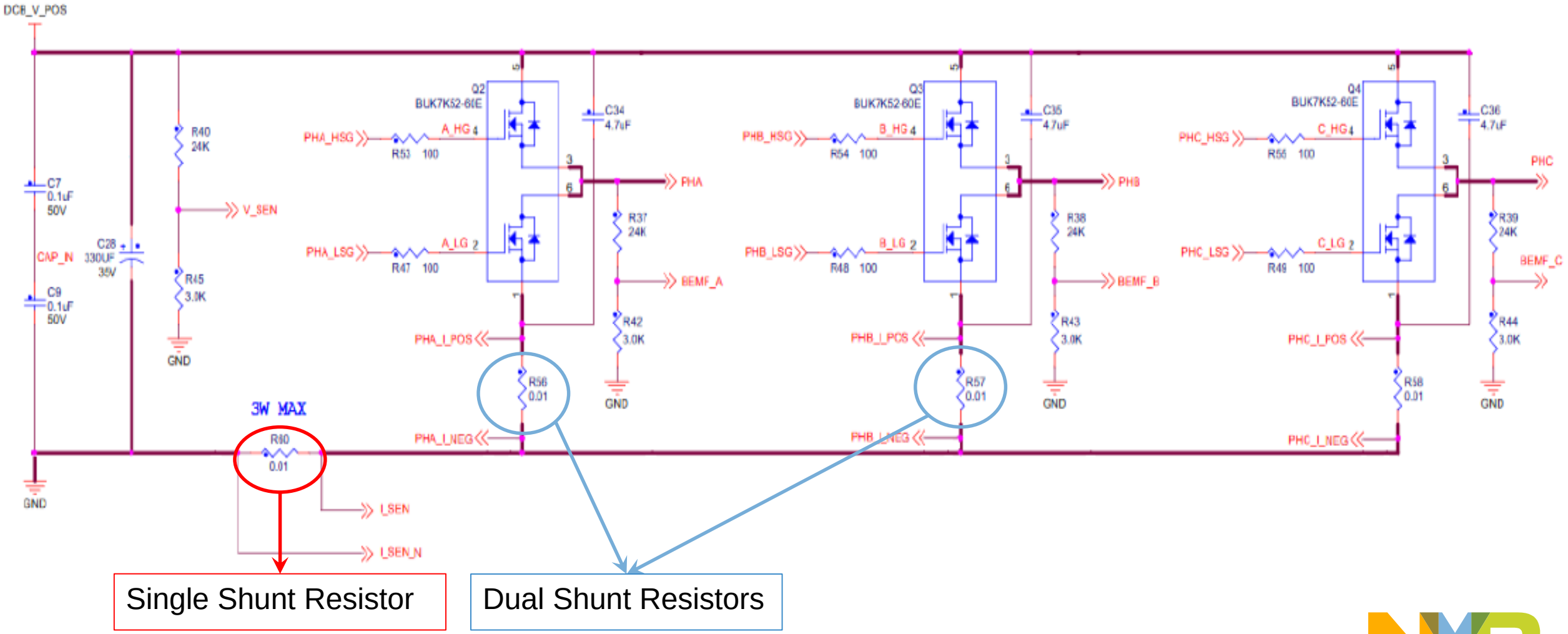
LPUART1 – Interface with PC FreeMaster

PTE10 – INT input from GD3000

GPIO for Buttons;
GPIO for enable/reset GD3000
GPIO for TRGMUX output
GPIO for RGB LED
GPIO for software debug



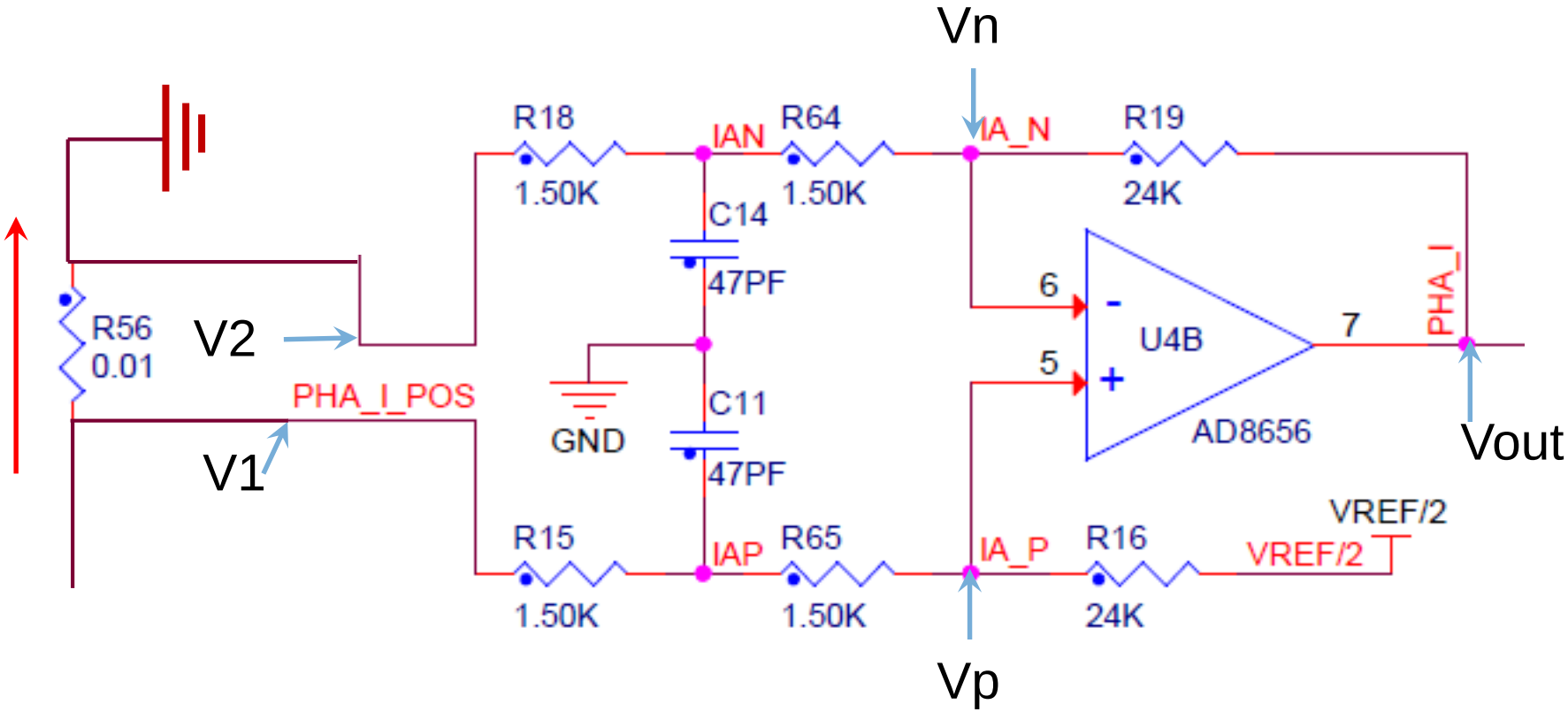
3-Phase Inverter Circuit



Single Shunt Resistor

Dual Shunt Resistors

Current Sampling Circuit (Dual Shunt)



$$\frac{Vout - Vn}{24Kohm} = \frac{Vn - V2}{3Kohm} \quad (1)$$

$$\frac{Vref/2 - Vp}{24Kohm} = \frac{Vp - V1}{3Kohm} \quad (2)$$

(1) – (2):
(and we know Vn == Vp, Vref/2 = 2.5V)

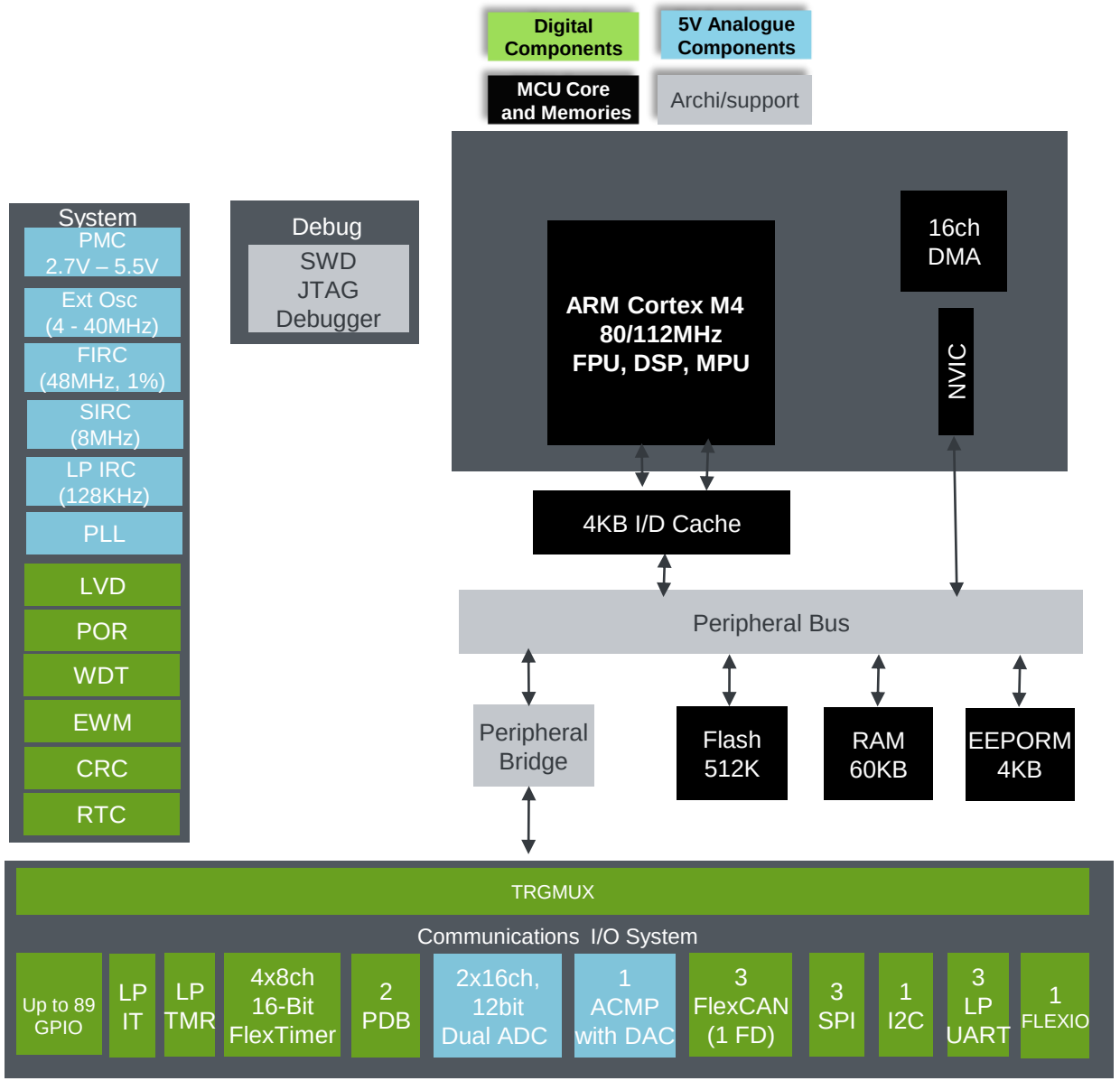
$$(V1 - V2) * 8 = (Vout - 2.5V)$$

$$(V1 - V2) * 10 = (Vout - 2.5V) \text{ (for Single Shunt)}$$

S32K144 MOTOR CONTROL PERIPHERALS

S32K144

- **ARM Cortex M4 Core**, 80MHz with **FPU**
- 4K I/D **Cache**
- **FTM** generates 3 pairs of complementary PWMs with flexible synchronization mechanism
- **TRGMUX**: FTM can trigger PDB timer start
- **ADC** sampling can be triggered by **PDB** with multiple delays;
- **LPSPI** is used to control GD3000
- **LPUART** is used for FreeMaster communication



Clock Settings Summary

SOSC		
SOSC Clock [Hz]	8000000	8 MHz
SOSC Clock Div1 [Hz]	8000000	8 MHz
SOSC Clock Div2 [Hz]	8000000	8 MHz

SPLL		
SPLL Clock [Hz]	160000000	160 MHz
SPLL Clock Div1 [Hz]	80000000	80 MHz
SPLL Clock Div2 [Hz]	40000000	40 MHz

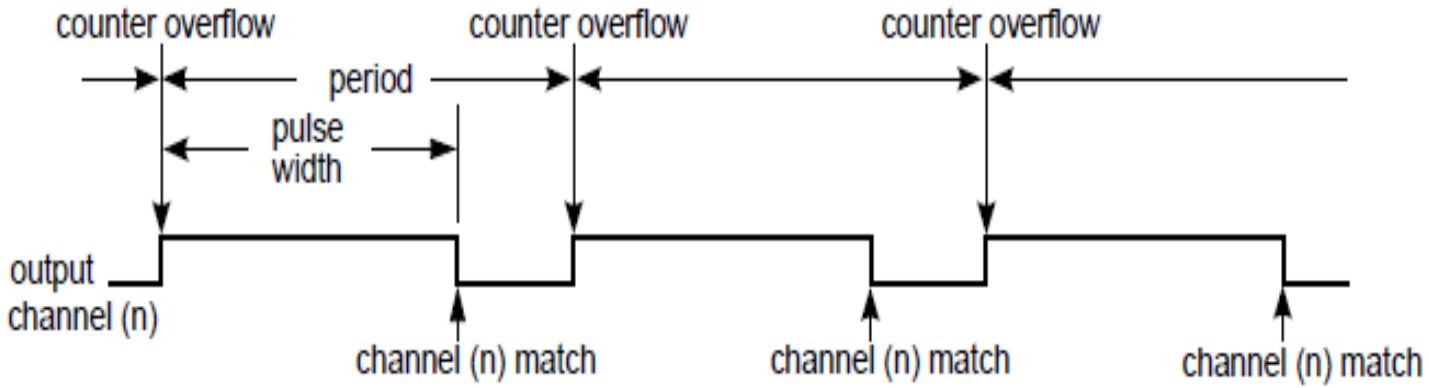
RUN Mode		
Core Clock [Hz]	80000000	80 MHz
Bus Clock [Hz]	40000000	40 MHz
Slow Clock [Hz]	26666666.666666668	26.667 MHz

Peripheral functional clocks		
ADC_0 clock [Hz]	40000000	40 MHz
ADC_1 clock [Hz]	40000000	40 MHz
FLEXIO_0 clock [Hz]	0	0 Hz
FTM_0 clock [Hz]	0	0 Hz
FTM_1 clock [Hz]	8000000	8 MHz
FTM_2 clock [Hz]	8000000	8 MHz
FTM_3 clock [Hz]	80000000	80 MHz
LPI2C_0 clock [Hz]	0	0 Hz
LPIT_0 clock [Hz]	40000000	40 MHz
LPSPI_0 clock [Hz]	40000000	40 MHz
LPSPI_1 clock [Hz]	0	0 Hz
LPSPI_2 clock [Hz]	0	0 Hz
LPTMR_0 clock [Hz]	0	0 Hz
LPUART_0 clock [Hz]	40000000	40 MHz
LPUART_1 clock [Hz]	40000000	40 MHz
LPUART_2 clock [Hz]	0	0 Hz

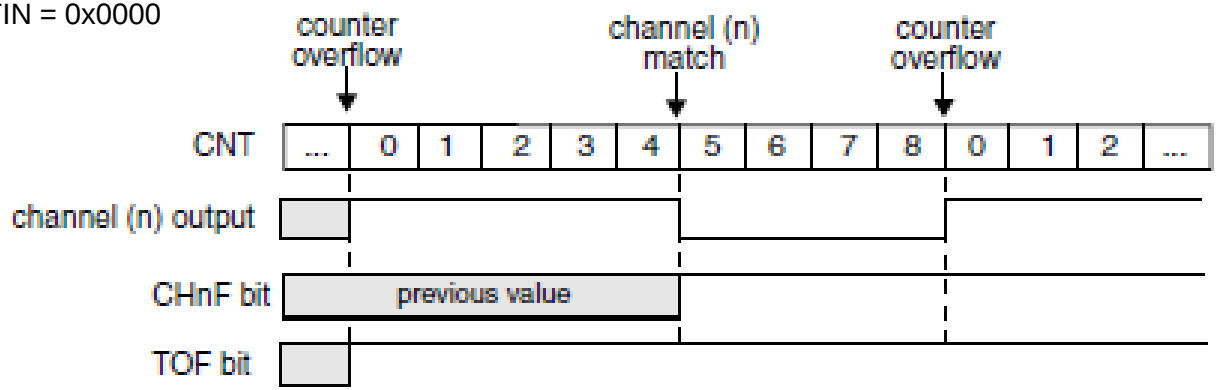
FTM: Edge Aligned PWM

ELSnB:ELSnA selects the polarity

- QUADEN = 0
- DECAPEN = 0
- COMBINE = 0
- CPWMS = 0, and
- MSnB = 1



MOD = 0x0008
CnV = 0x0005
CNTIN = 0x0000

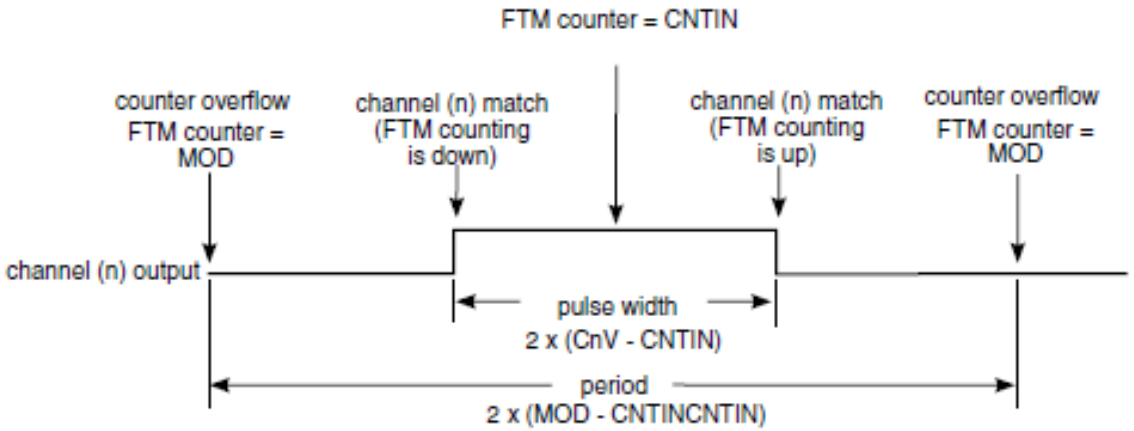


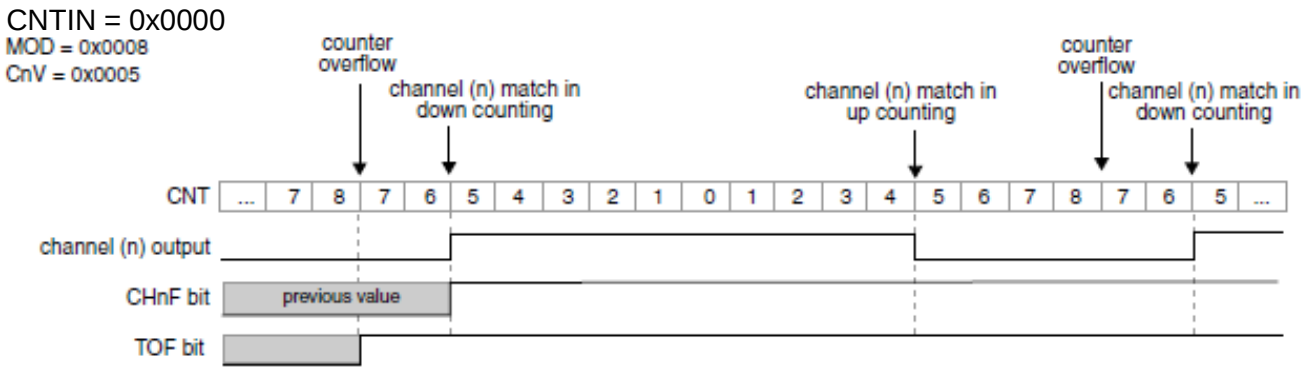
FTM: Center aligned PWM

ELSnB:ELSnA selects the polarity

- QUADEN = 0
- DECAPEN = 0
- COMBINE = 0, and
- CPWMS = 1

MSnB: MSnA are meaningless





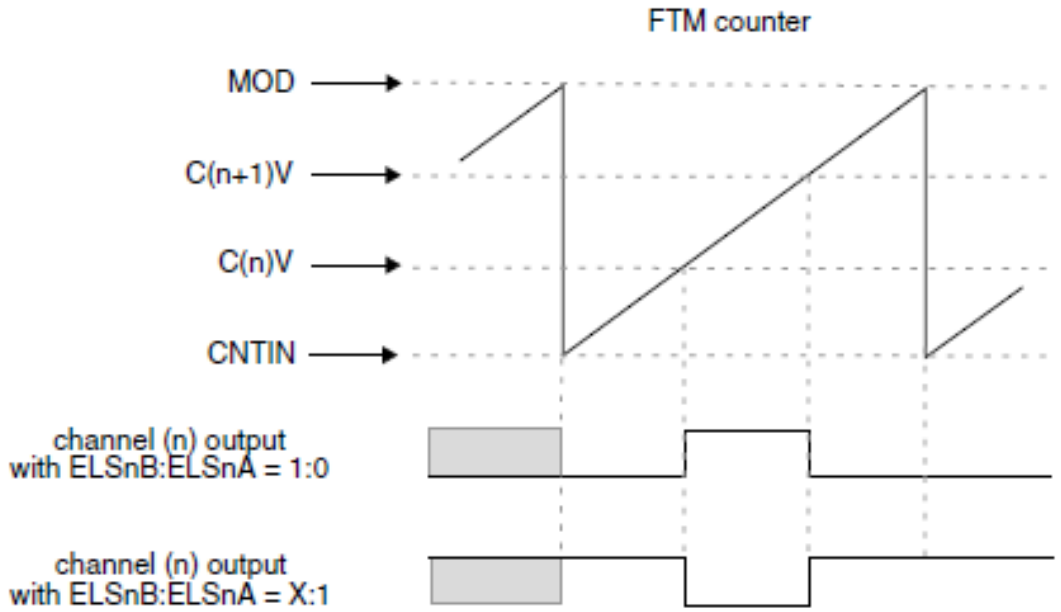
When the counter works in down-up mode, only center-edge PWM function is available for all the channels

FTM: Combine PWM

== Asymmetrical PWM generation

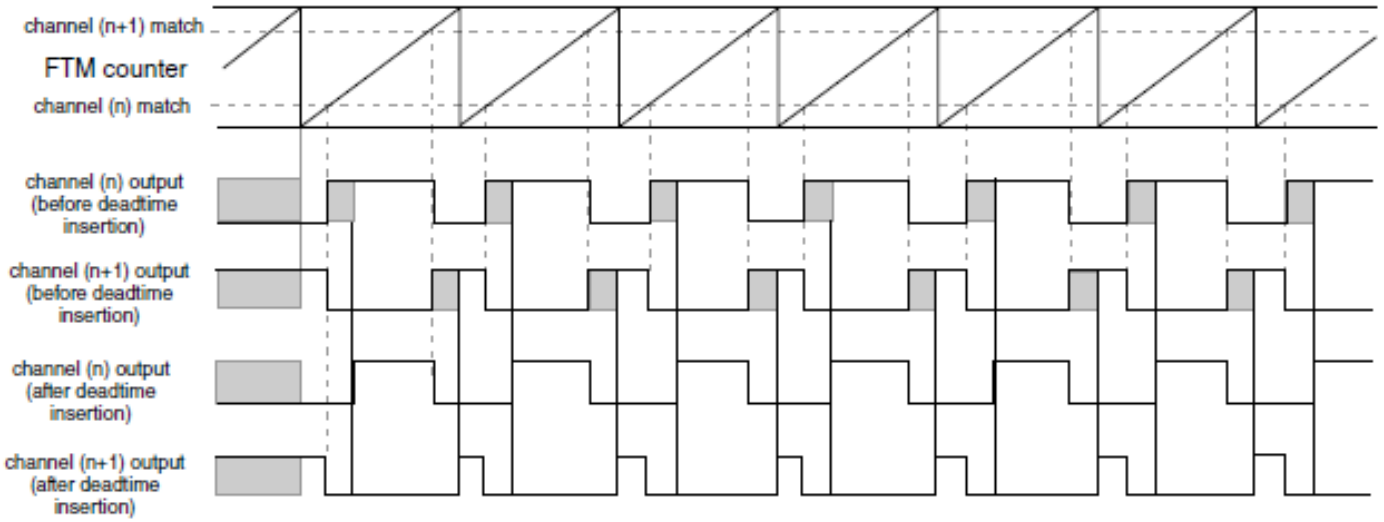
- QUADEN = 0
- DECAPEN = 0
- COMBINE = 1, and
- CPWMS = 0

MSnB: MSnA are meaningless (same for n+1)



ELSnB: ELSnA controls the polarity of the channel outputs. By defaut outputs on channel n and n+1 are complemented, without dead time. If ELSnB:ELSnA = 00, then the channel n output is not controlled by the FTM (dito n+1).

FTM: Complementary PWM with deadtime

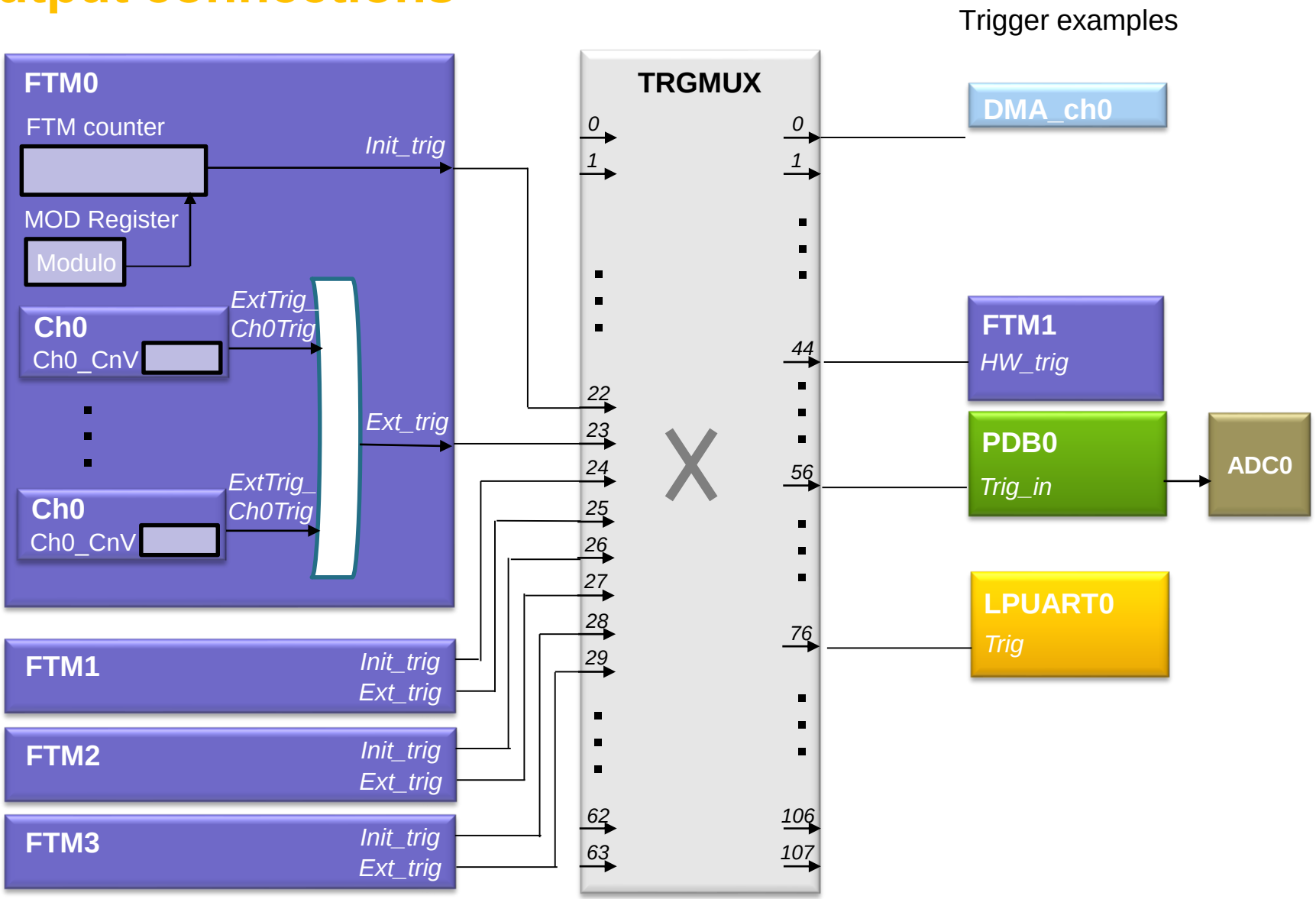


Deadtime insertion is enabled for channel n and (n+1) when DTENx=1 and DTVAL[5:0] is not zero in the register COMBINE.

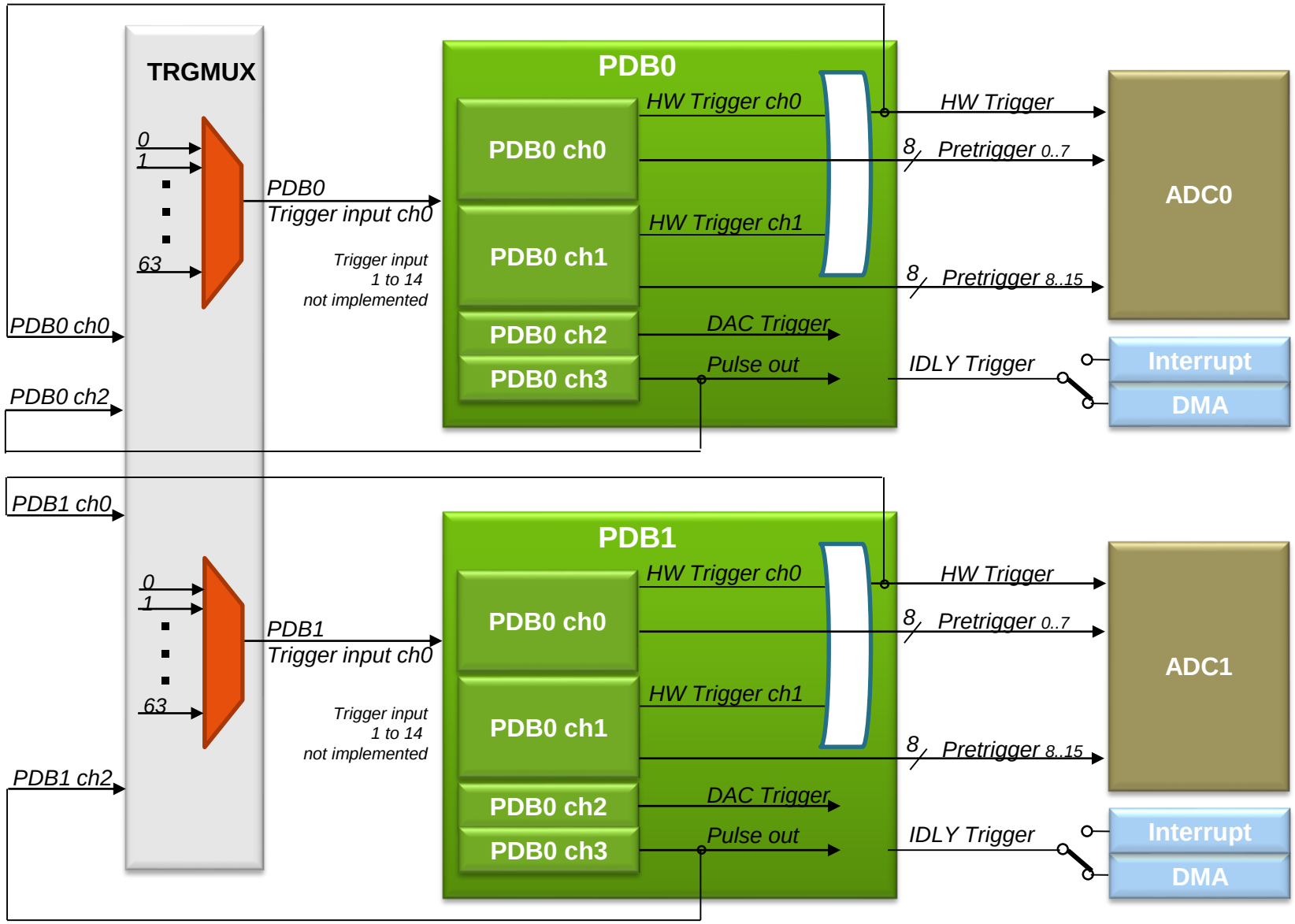
Deadtimes are a 5bit multiple of the system clock with a configurable prescaler (1, 4, 16). (12.5ns to 6,4µs)

Deadtimes apply to the rising edge

Trigger output connections



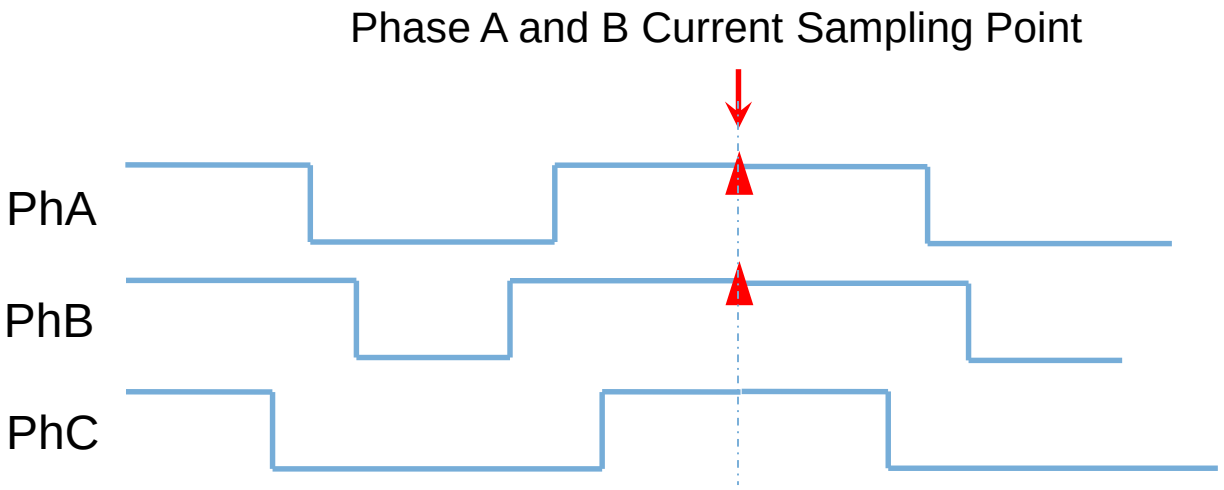
PDB connections

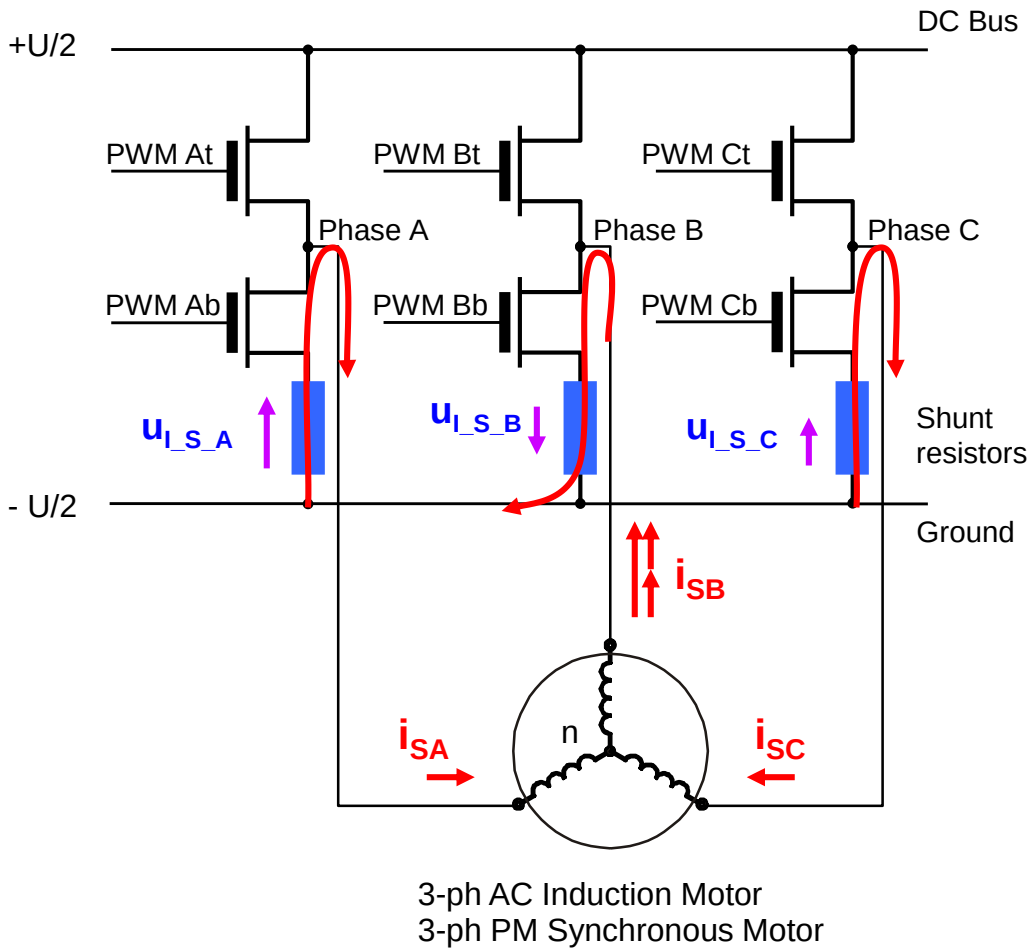


DUAL-SHUNT SOLUTION

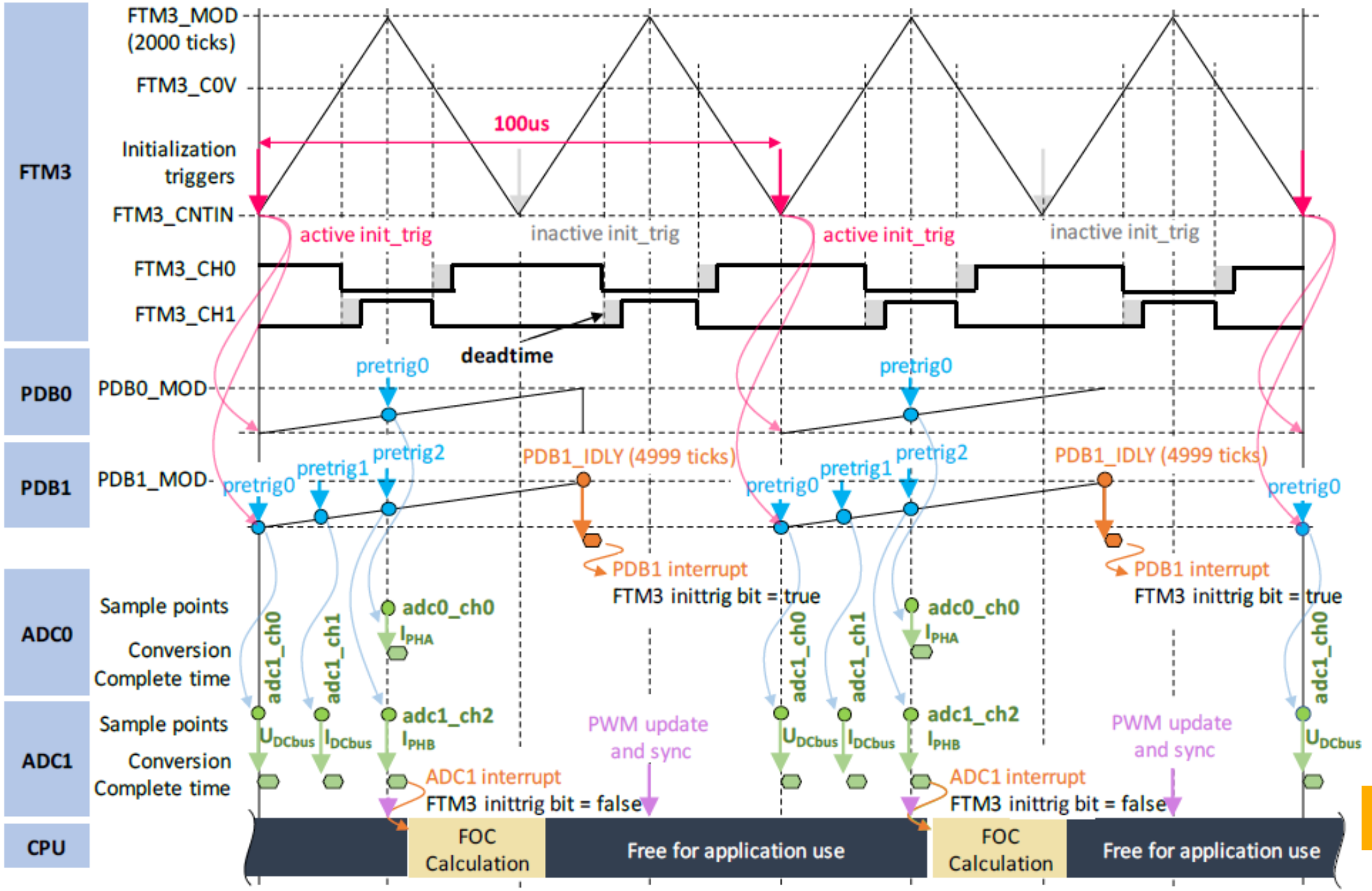
Current Sensing with Shunt Resistors

- Shunt resistors voltage drop measured
- SW calculation of all 3 phase currents needed
  - Phase (e.g. Phase A) current sensing possible only when bottom switch (transistor + diode) is conducting
- Dual-sampling required



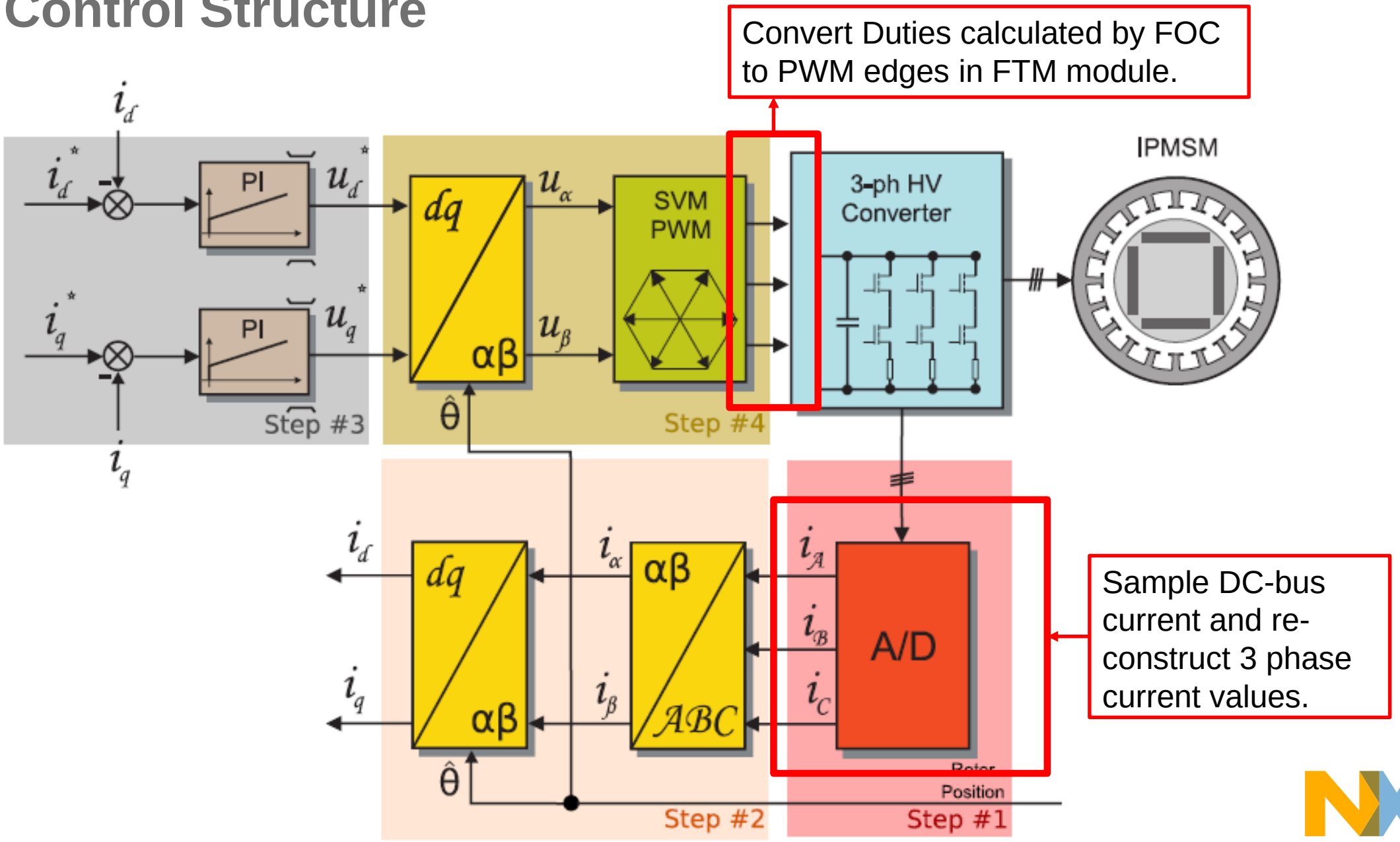


3-ph AC Induction Motor
3-ph PM Synchronous Motor


FTM3
PDB0
PDB1
ADC0
ADC1
CPU
FTM3_MOD
(2000 ticks)
FTM3_C0V
100us
Initialization
triggers
FTM3_CNTIN
active init_trig
inactive init_trig
active init_trig
inactive init_trig
FTM3_CH0
FTM3_CH1
deadtime
pretrig0
PDB0_MOD
pretrig0
pretrig1
pretrig2
PDB1_IDLY (4999 ticks)
PDB1_MOD
pretrig0
pretrig1
pretrig2
PDB1_IDLY (4999 ticks)
pretrig0
PDB1 interrupt
FTM3 inittrig bit = true
PDB1 interrupt
FTM3 inittrig bit = true
Sample points
Conversion
Complete time
adc1_ch0
adc1_ch1
adc0_ch0
IPHA
adc1_ch0
adc1_ch1
adc0_ch0
IPHA
adc1_ch0
Sample points
Conversion
Complete time
UDCbus
IDCbus
adc1_ch2
IPHB
PWM update
and sync
UDCbus
IDCbus
adc1_ch2
IPHB
PWM update
and sync
UDCbus
ADC1 interrupt
FTM3 inittrig bit = false
ADC1 interrupt
FTM3 inittrig bit = false
FOC
Calculation
Free for application use
FOC
Calculation
Free for application use

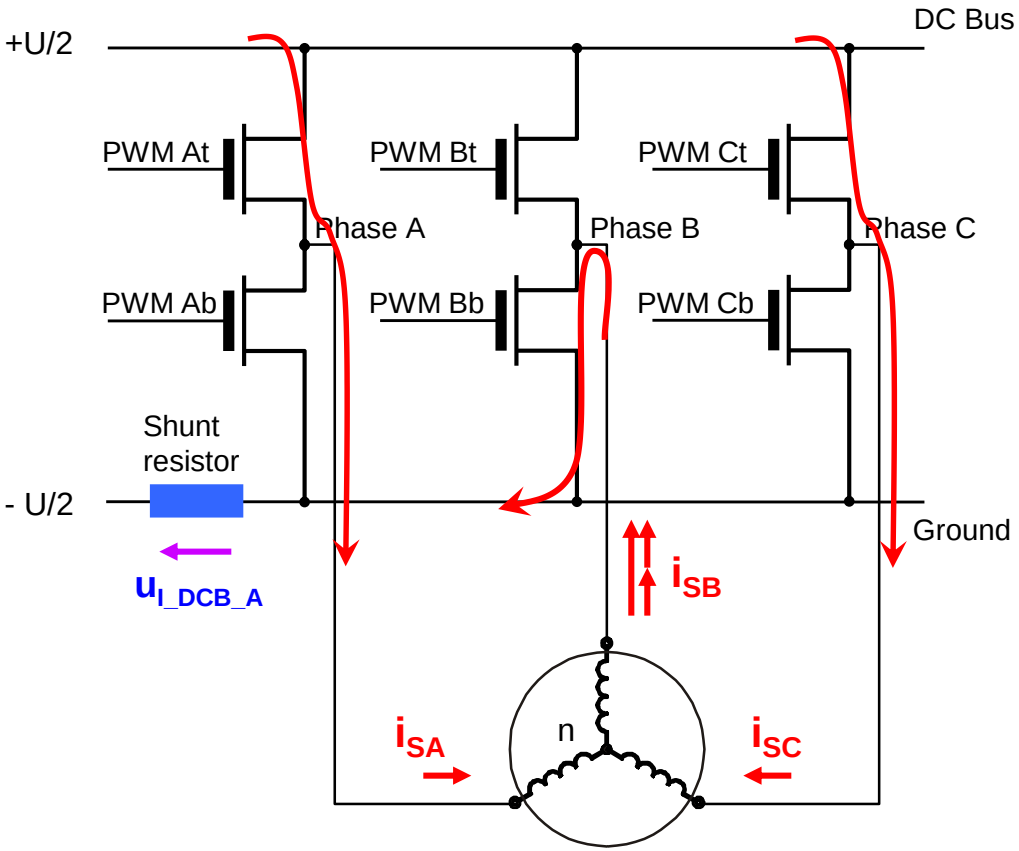
SINGLE-SHUNT SOLUTION

FOC Control Structure

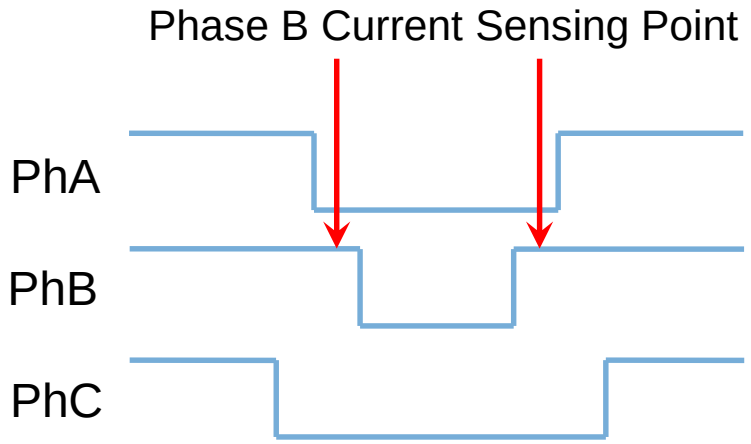


BASIC MECHANISM

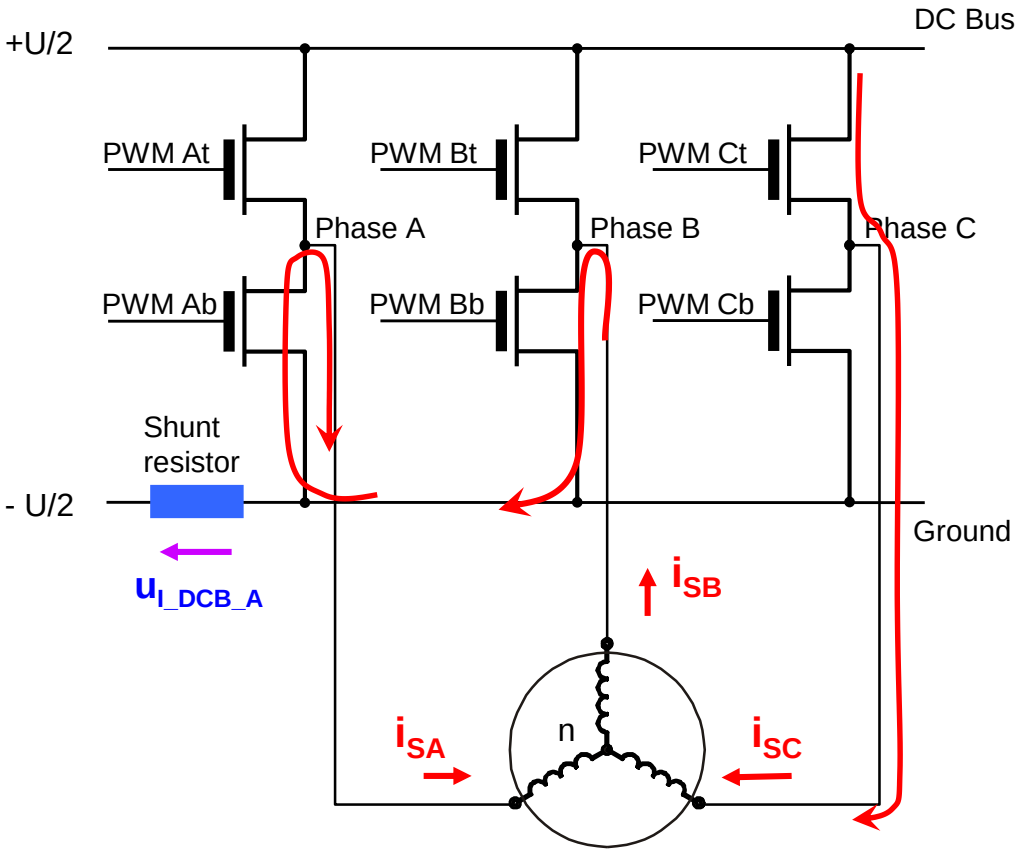
Current Sensing for Single Shunt – Phase B current



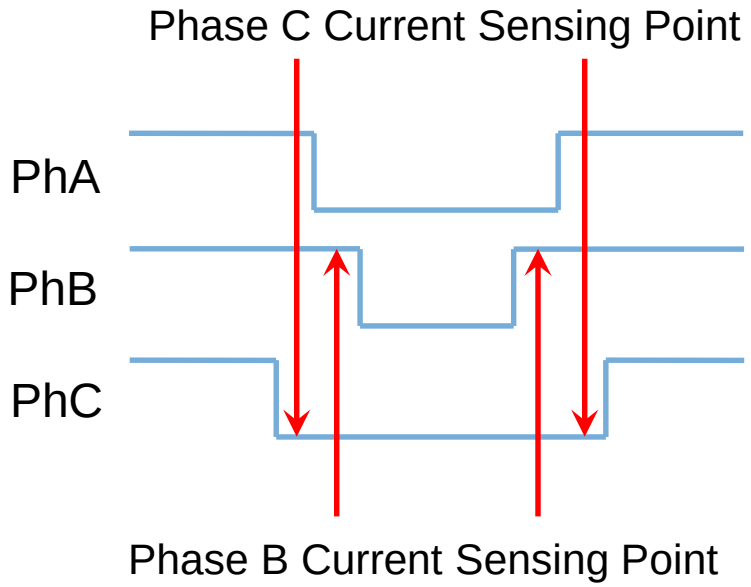
3-ph AC Induction Motor
3-ph PM Synchronous Motor



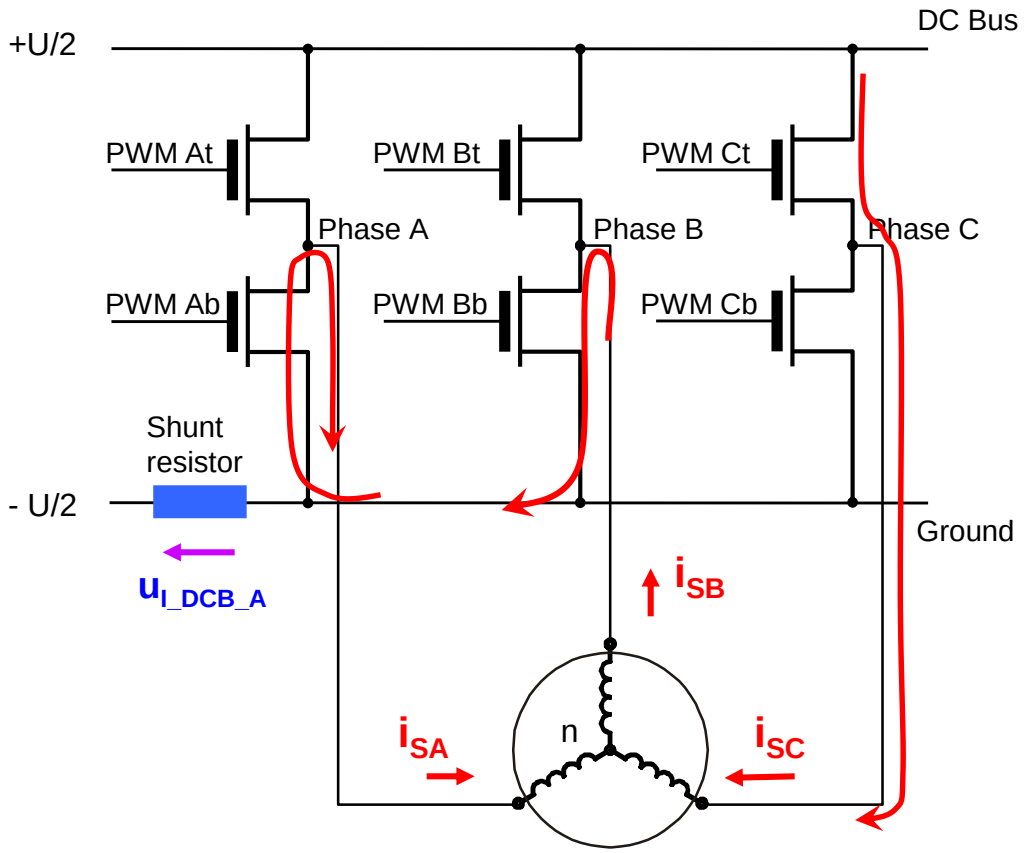
Current Sensing for Single Shunt – Phase C current



3-ph AC Induction Motor
3-ph PM Synchronous Motor

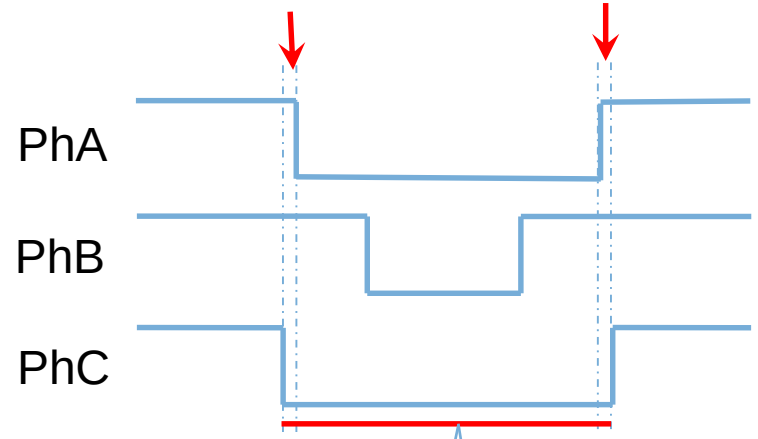


Current Sensing for Single Shunt – Double Switch PWM

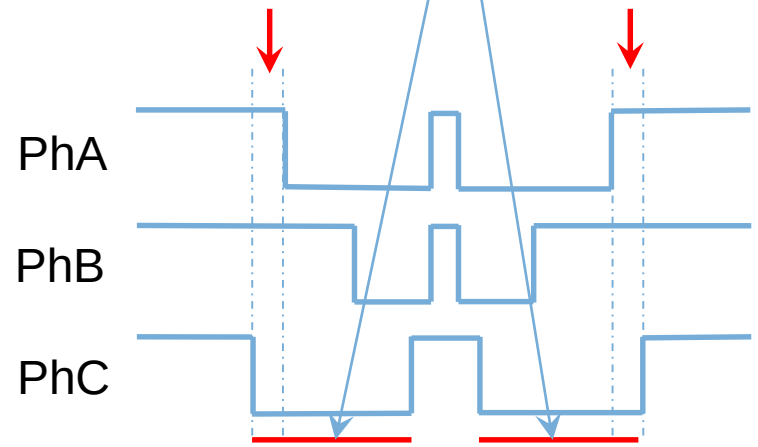


3-ph AC Induction Motor
3-ph PM Synchronous Motor

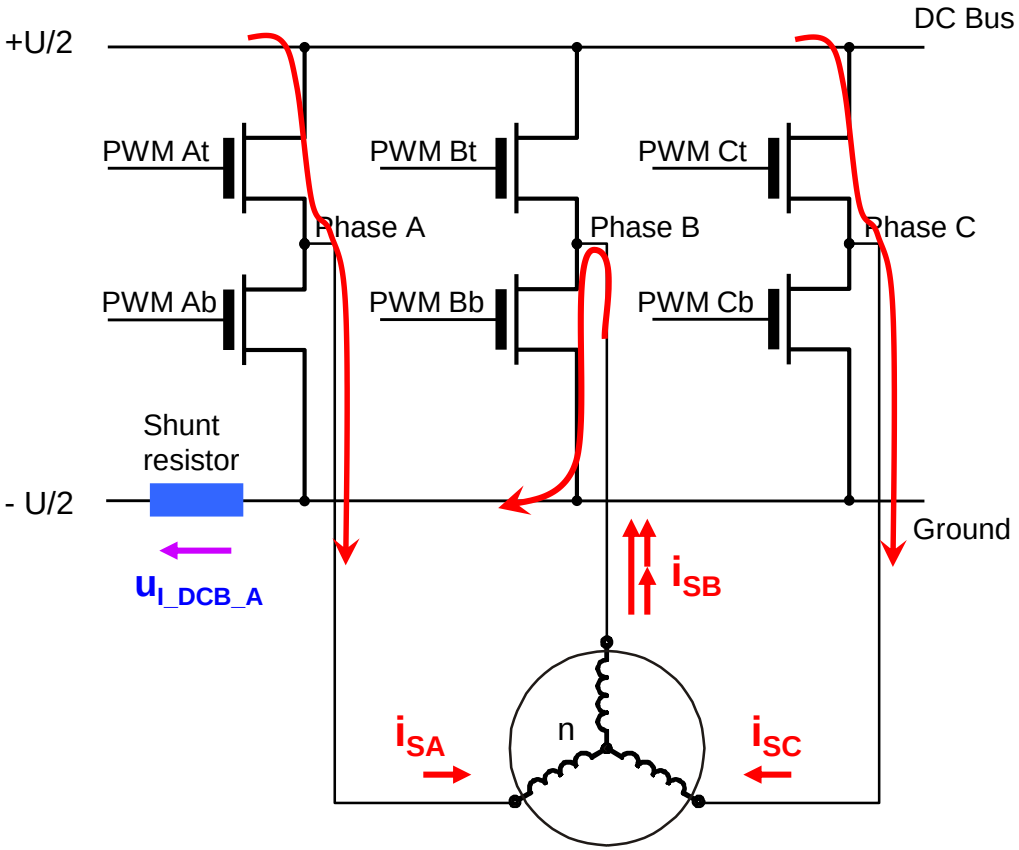
Too narrow for ADC sampling.
Need Adjust PWM Waveform.



Adjust PhC Center Pulse Width to create enough delta time between PhA and PhC PWM edges.

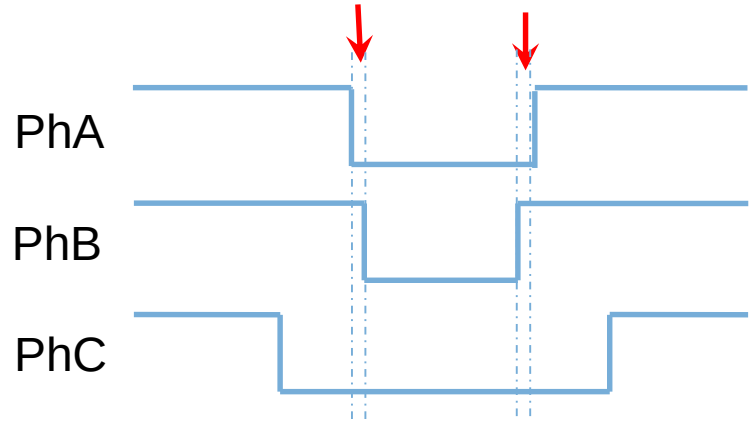


Current Sensing for Single Shunt – Double Switch

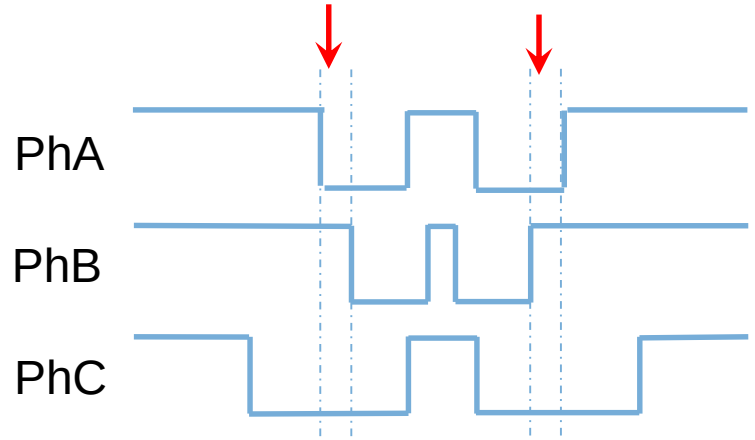


3-ph AC Induction Motor
3-ph PM Synchronous Motor

Too narrow for ADC sampling.
Need Adjust PWM Waveform.

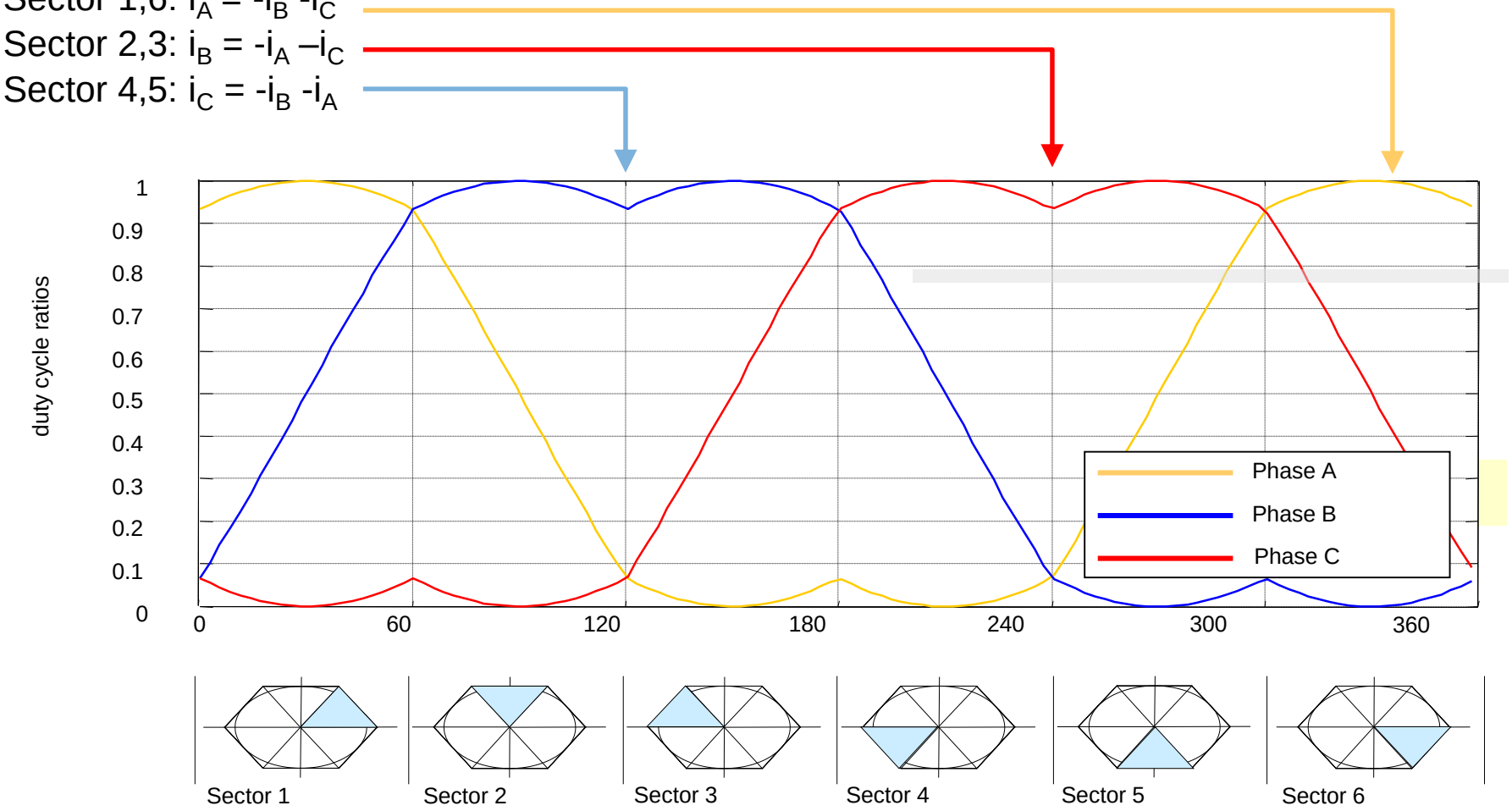


Adjust PhA and PhC Center Pulse Width to create enough delta time between PhA and PhB PWM edges.



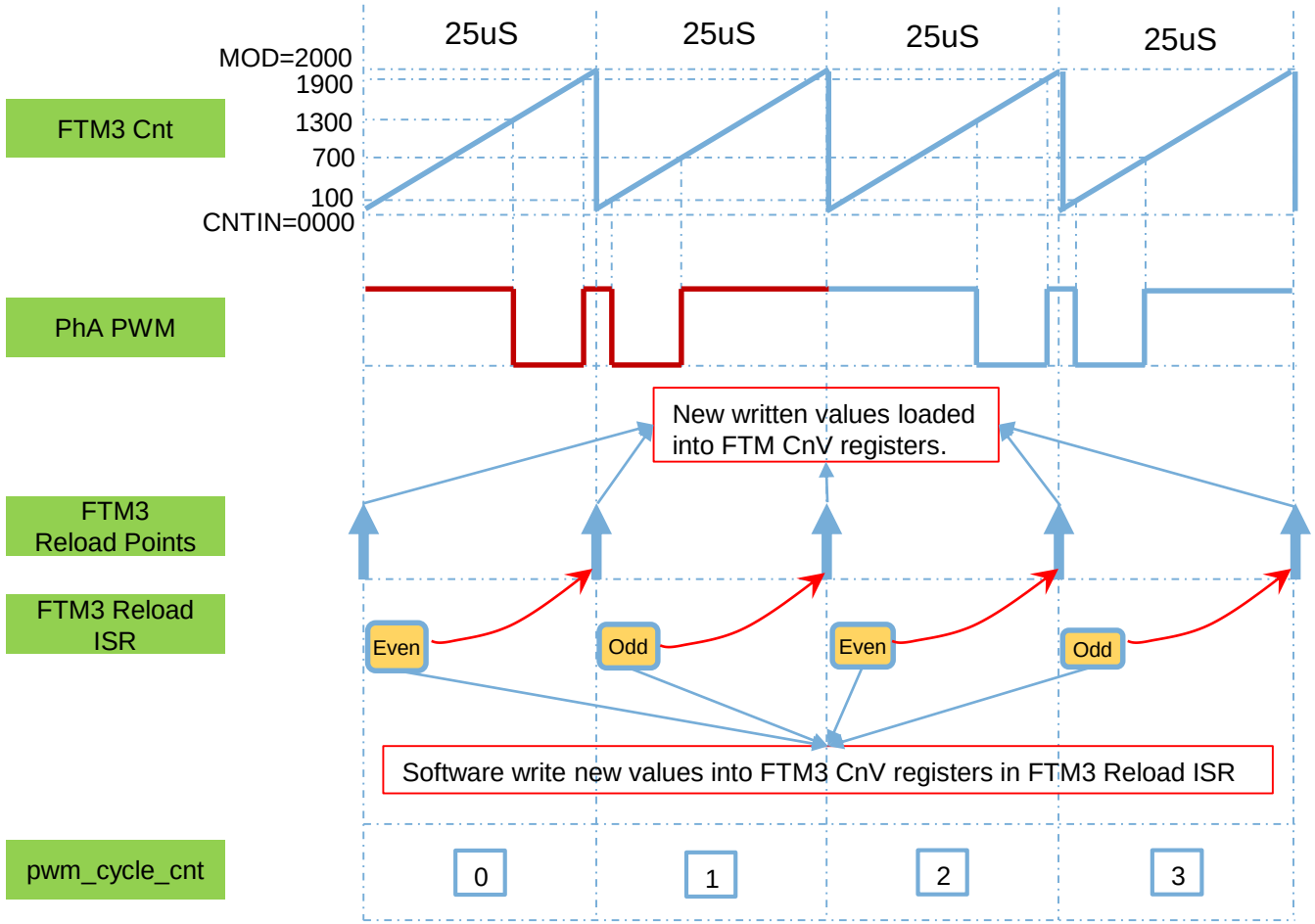
Current Sensing - Calculation

- Phase currents reconstruction according to Phase PWM signals (sectors 1..6)
- 3rd phase current calculated from 2 measured phases:
  - Sector 1,6: $i_A = -i_B - i_C$
  - Sector 2,3: $i_B = -i_A - i_C$
  - Sector 4,5: $i_C = -i_B - i_A$



DOUBLE-SWITCH PWM GENERATION

Double Switch PWM Generation



1)Use two 25uS simple PWM to create one 50uS double-switch PWM;

2) Enable FTM3 reload interrupt in MCU initialization;

3) Update CnV registers with two sets of values in FTM3 reload ISR. One set of CnV values for even cycle ISR and the other for odd cycle ISR. For example, to generate 30% duty PWM:

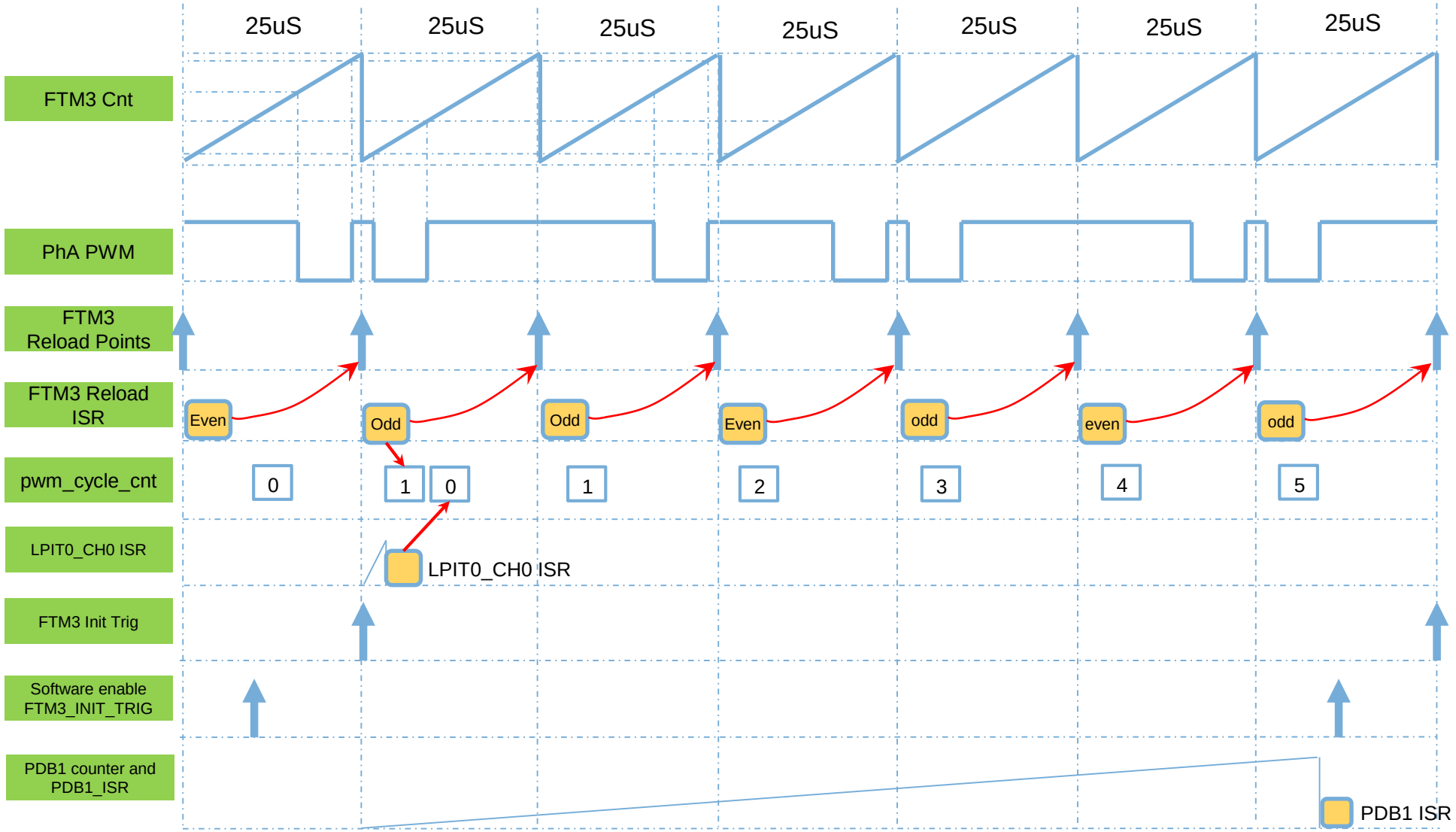
Even cycle: pwm_cycle_cnt==0 means it's an even cycle
increment pwm_cycle_cnt++;
write **100** to C0V and write **700** to C1V;
FTM_PWMLOAD_LDOK=1;

Odd cycle: pwm_cycle_cnt==1 means it's an odd cycle
increment pwm_cycle_cnt++;
write **1300** to C0V and write **1900** to C1V;
FTM_PWMLOAD_LDOK=1;

4) The CnV registers update occurred at the next reload point

5) Combine even cycle and odd cycle together to create a 50uS period double-switch PWM.

Double Switch PWM Synchronization with FTM_INIT_TRIG



1) Software enabling FTM3_INIT_TRIG may occur in even PWM cycle or odd PWM cycle. (FTM3_EXTTRIG_INITTRIGEN = 1).

2) If FTM3_INIT_TRIG enabling occurred in even PWM cycle, the PWM is not correctly synchronized with the FTM init trigger.

3) FTM3_Init_Trig will let LPIT0_CH0 to run. And LPIT ISR occurred.

4) In LPIT0_CH0 ISR, software changes the pwm_cycle_cnt to 0. So PWM is correctly synchronized to FMT init trigger.

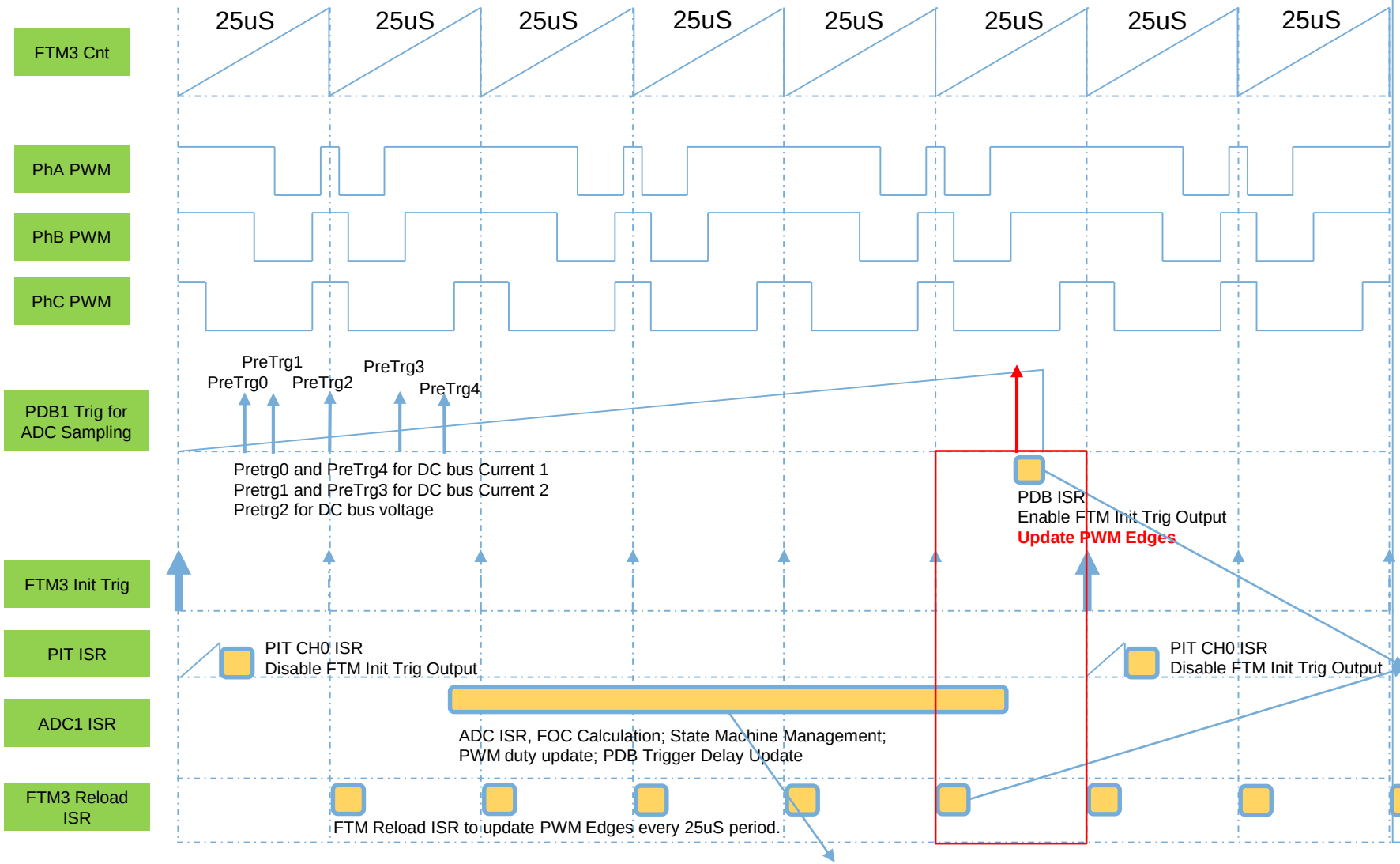
5) And in LPIT0_CH0_ISR, software disable FTM3_INIT_TRIG;

6) FTM3_INIT_TRIG start the PDB1 counter. In PDB1 ISR, software will re-enable FTM3_INIT_TRIG;

7) One control loop takes 150uS. It means the FTM3_INIT_TRIG occurred every 6 PWM cycles.

TIMING AND SYNCHRONIZATION

Single-Shunt Timing Chart



1. FTM3 configured in edge mode, combine mode, 25uS period; After writing LDOK bit, the new values will be effective at next reload point (FTM counter wrap from MOD to CNTIN).

2. FTM3 Reload interrupt enabled; and in its ISR, PWM registers CnV are updated for next period;

3. Software will enable FTM3 Init Trigger at certain point;

4. FTM3 Init Trig start LPIT0_CH0 and PDB1 through TRGMUX settings;

5. Use LPIT0_CH0 ISR to disable FTM3 Init Trig

6. PDB1 timer start and trigger ADC1 sampling: sample ADC1_Ch6 4 times for DC bus current; sample ADC1_Ch7 1 time for DC bus voltage;

7. When all ADC results ready, ADC1 ISR occurred, calculate phase A/B/C currents, run FOC, calculate PWM edges, and PDB1 pre-trigger delays; Update PDB1 registers;

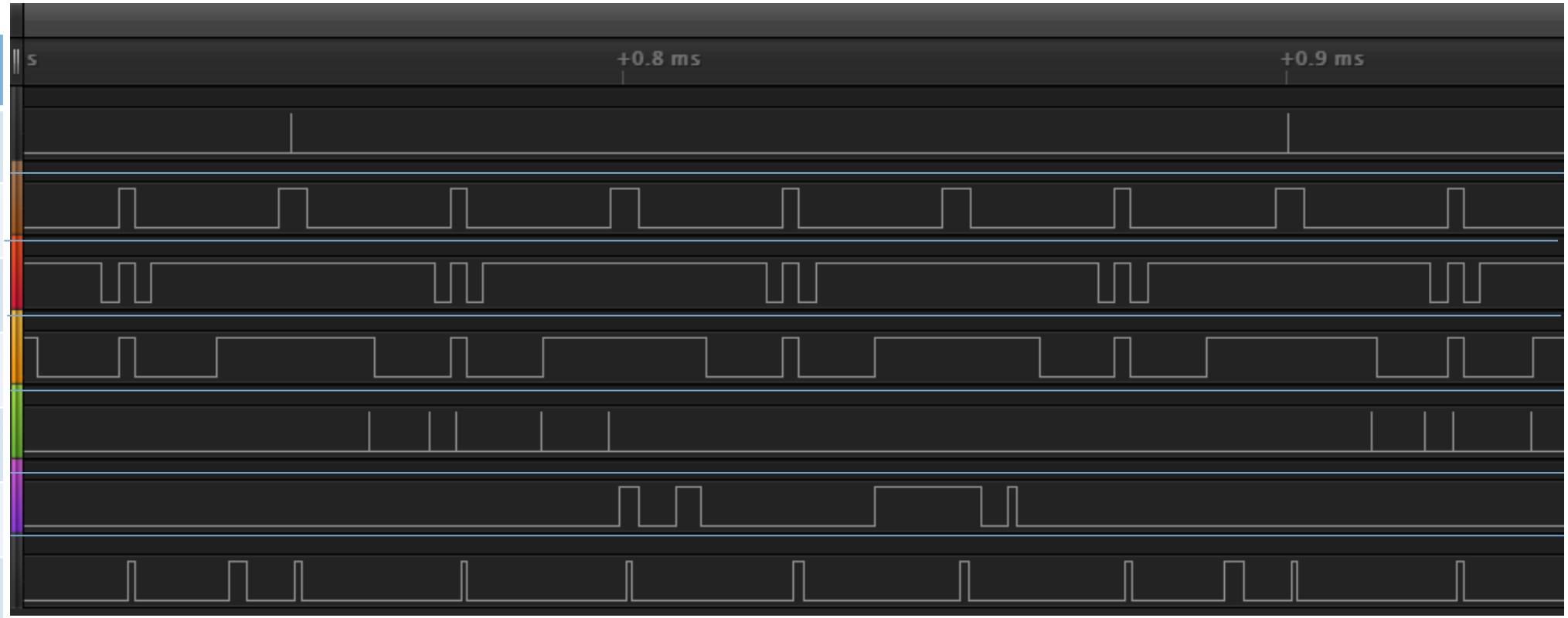
8. PDB1 ISR occurred in the last 25uS window. Re-enable FTM3 Init Trig, update PWM edges with new values;

9. Within the 25uS window, FTM3 CnV registers are updated twice, 1st is at the beginning in FTM3 Reload ISR, 2nd is in PDB1 ISR; 2nd time will take effect even though the LDOK is already written in the Reload ISR.

FOC execution time is 72uS without optimization;
FOC execution time is 43.5uS with highest level compiler optimization;

Oscilloscope Captured Signals

Channel Labels
FTM3_INIT_TRIG
PhA_PWM
PhB_PWM
PhC_PWM
PDB_PreTrig
Software Exe Time
FTM3 Reload ISR Or PDB ISR

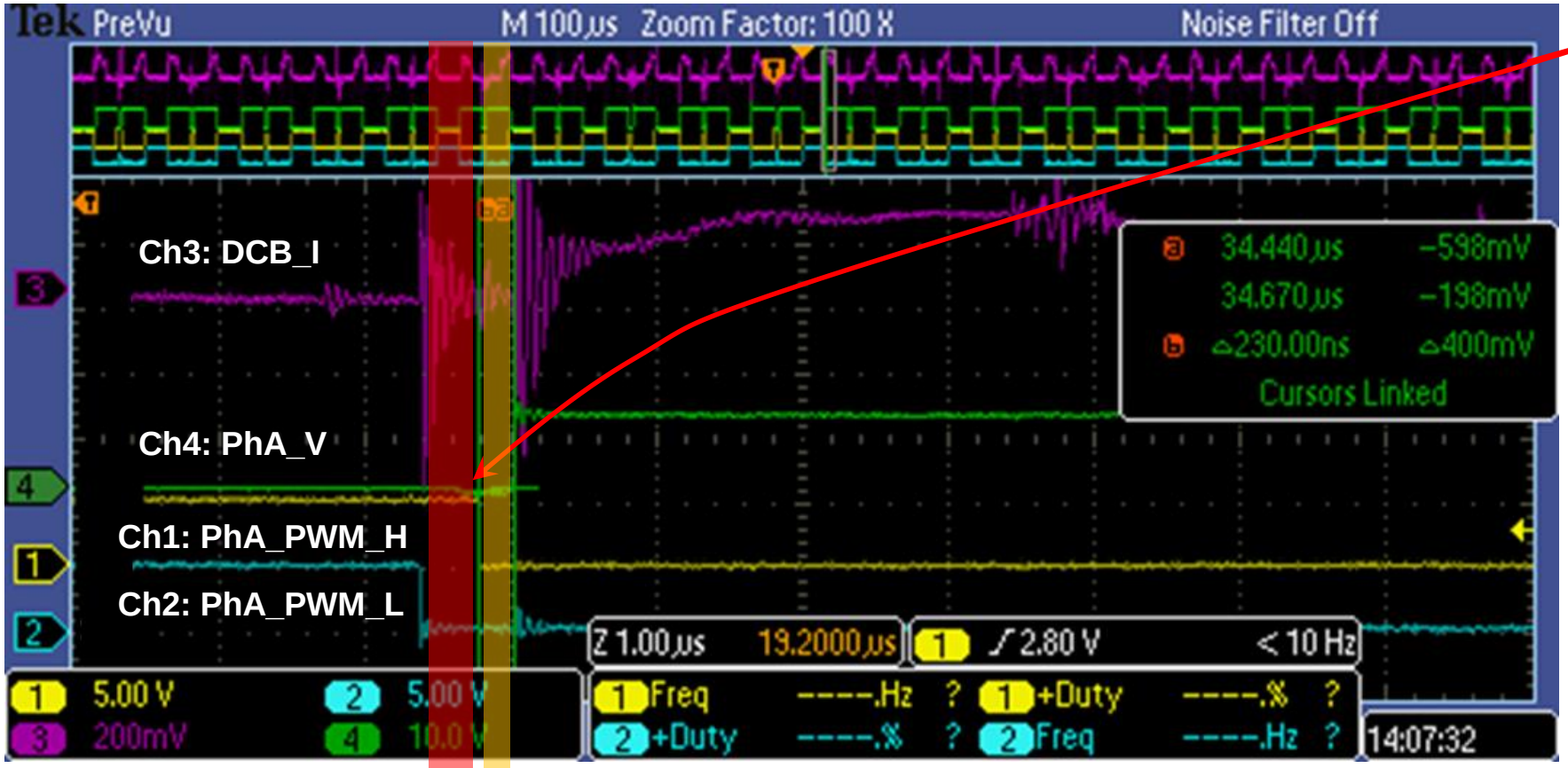


SOFTWARE EXECUTION TIME

Software Execution Time

	S32K144 Single Shunt	S32K144 Dual Shunt
Board Buttons	2.6uS	1.3uS
MEAS_Get3PhCurrent	5.3uS	5.1uS
FaultDetection	4.7uS	4.3uS
CalcOpenLoop() AMCLIB_BemfObsrvDQ() AMCLIB_TrackObsrv() Mode Identification	17.7uS	15.4uS
FocSlowLoop()	8.8uS	7.2uS
FocFastLoop()	13.3uS	11.9uS
ACTUATE_SetDutycycle()	3.9uS	2.9uS
LED and FMSTR_Recorder	1.3uS	1.3uS
Total (with FocSlowLoop)	57.6	49.4
Total (without FocSlowLoop)	48.8	42.2

PDB TRIGGER TIMING OFFSET



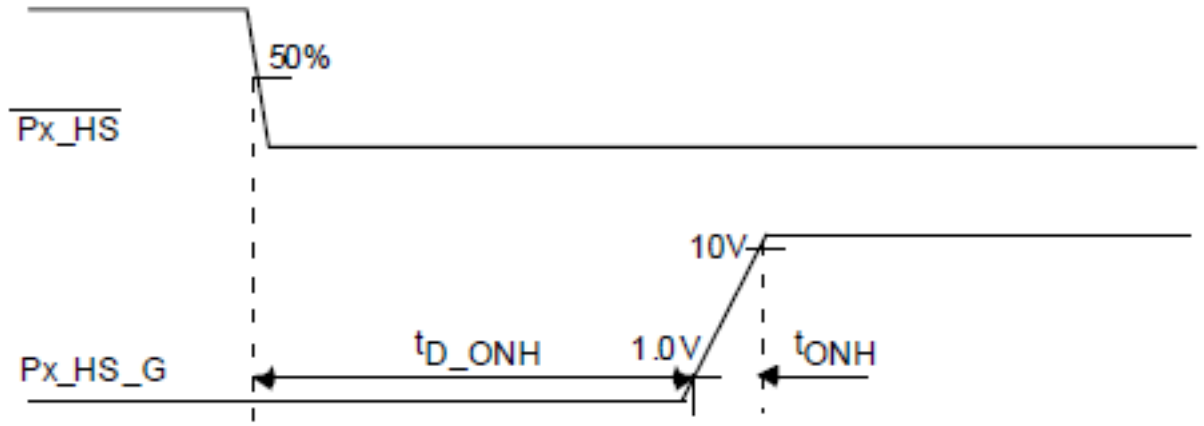
MCU PWM_H output to PhA MOSFET output delay: 0.23uS;
Dead time 0.39uS;

Software set PDB1 pretrigger **0.5uS** before MCU PWM_H transition edge.

Minimum ADC sample width: 1.5uS;

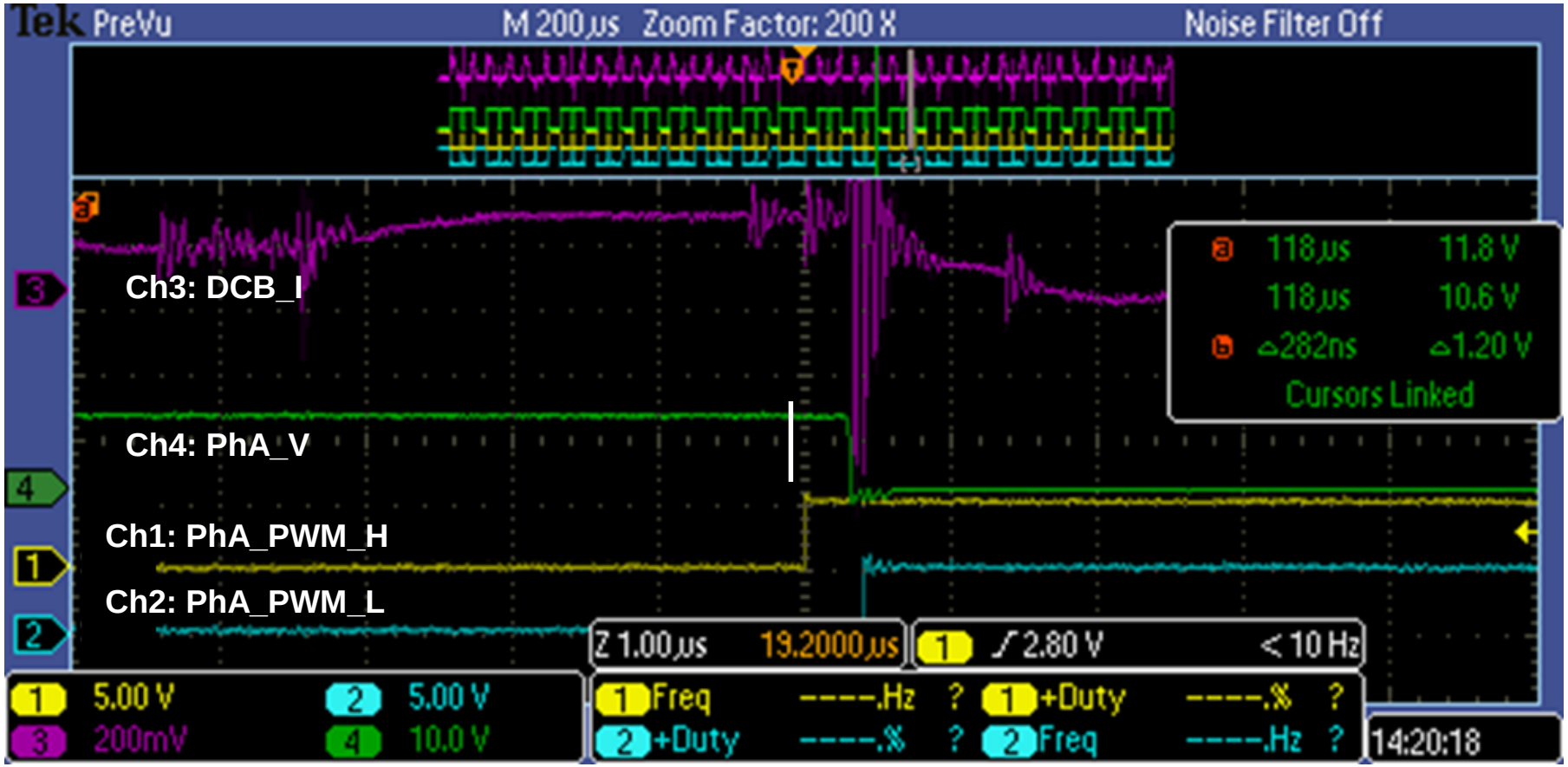
GD3000 Turn On Delay = 0.26uS

Deadtime = 0.4uS



GATE DRIVE

t_{ONH}	High-side turn on time • Transition time from 1.0 V to 10 V, Load: C = 500 pF, Rg = 0, (Figure 7)	–	20	35	ns	(42)
t_{D_ONH}	High-side turn on delay • Delay from command to 1.0 V, (Figure 7)	130	265	386	ns	(43)
t_{OFFH}	High-side turn off time • Transition time from 10 V to 1.0 V, Load: C = 500 pF, Rg = 0, (Figure 8)	–	20	35	ns	(42)
t_{D_OFFH}	High-side turn off delay • Delay from command to 10 V, (Figure 8)	130	265	386	ns	(43)

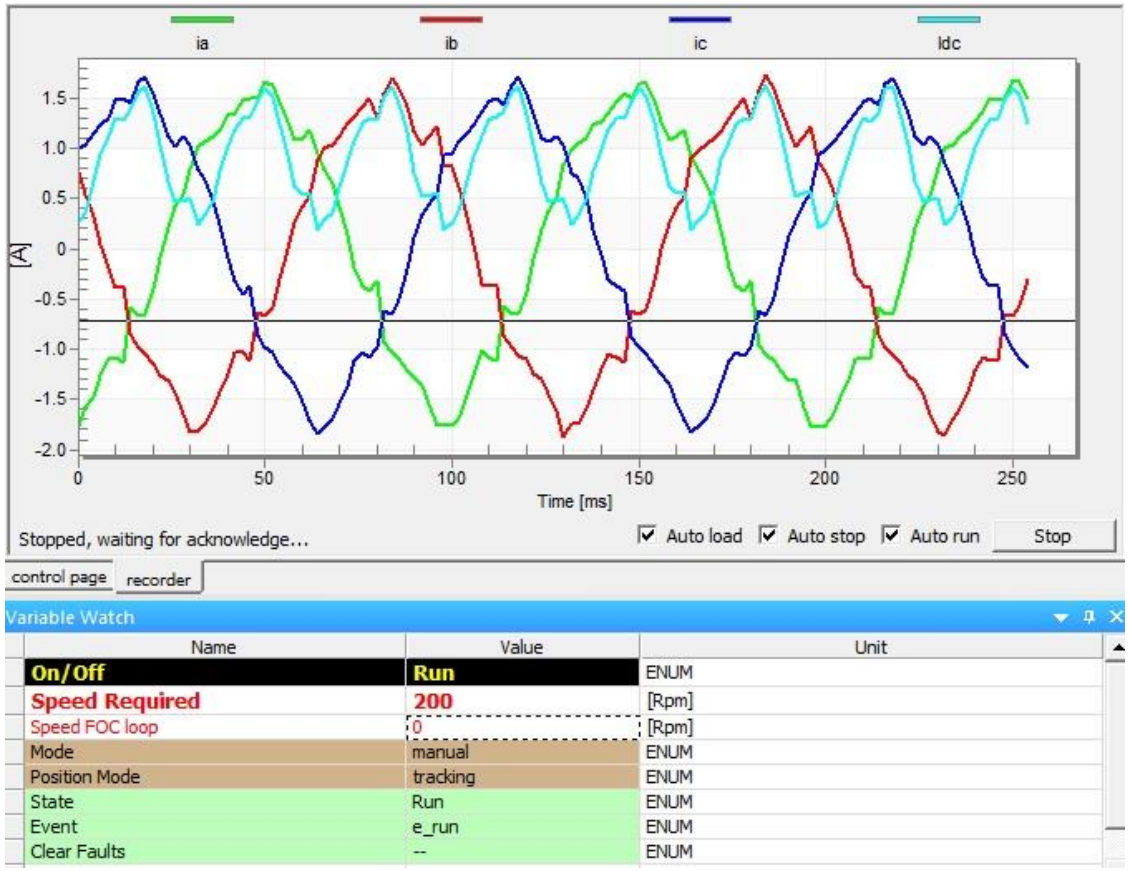

Tek PreVu
M 200µs Zoom Factor: 200 X
Noise Filter Off
Ch3: DCB_I
Ch4: PhA_V
Ch1: PhA_PWM_H
Ch2: PhA_PWM_L
118µs 11.8 V
118µs 10.6 V
Δ282ns Δ1.20 V
Cursors Linked
Z 1.00µs 19.2000µs
2.80 V
< 10 Hz
5.00 V
5.00 V
200mV
10.0 V
Freq ----.Hz
+Duty ----.%
+Duty ----.%
Freq ----.Hz
14:20:18

ISSUES AND SOLUTION

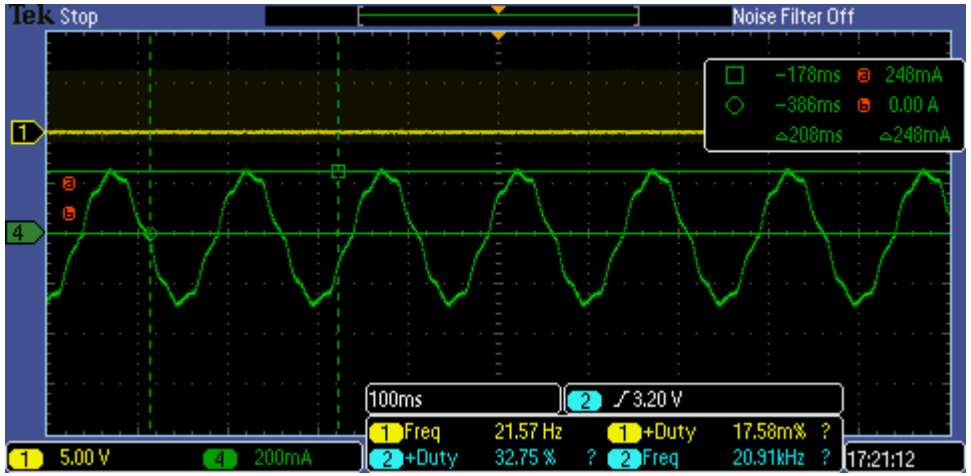
Issue – Current Measurement And Calculation

- Current sampling values (1.6A) don't match the results by current probe (2.5A);
- This issue was resolved by removing the C16 capacitor on GD3000 EVB.
- This capacitor create a low pass filter causing ADC not able to sample the accurate DC bus current value.

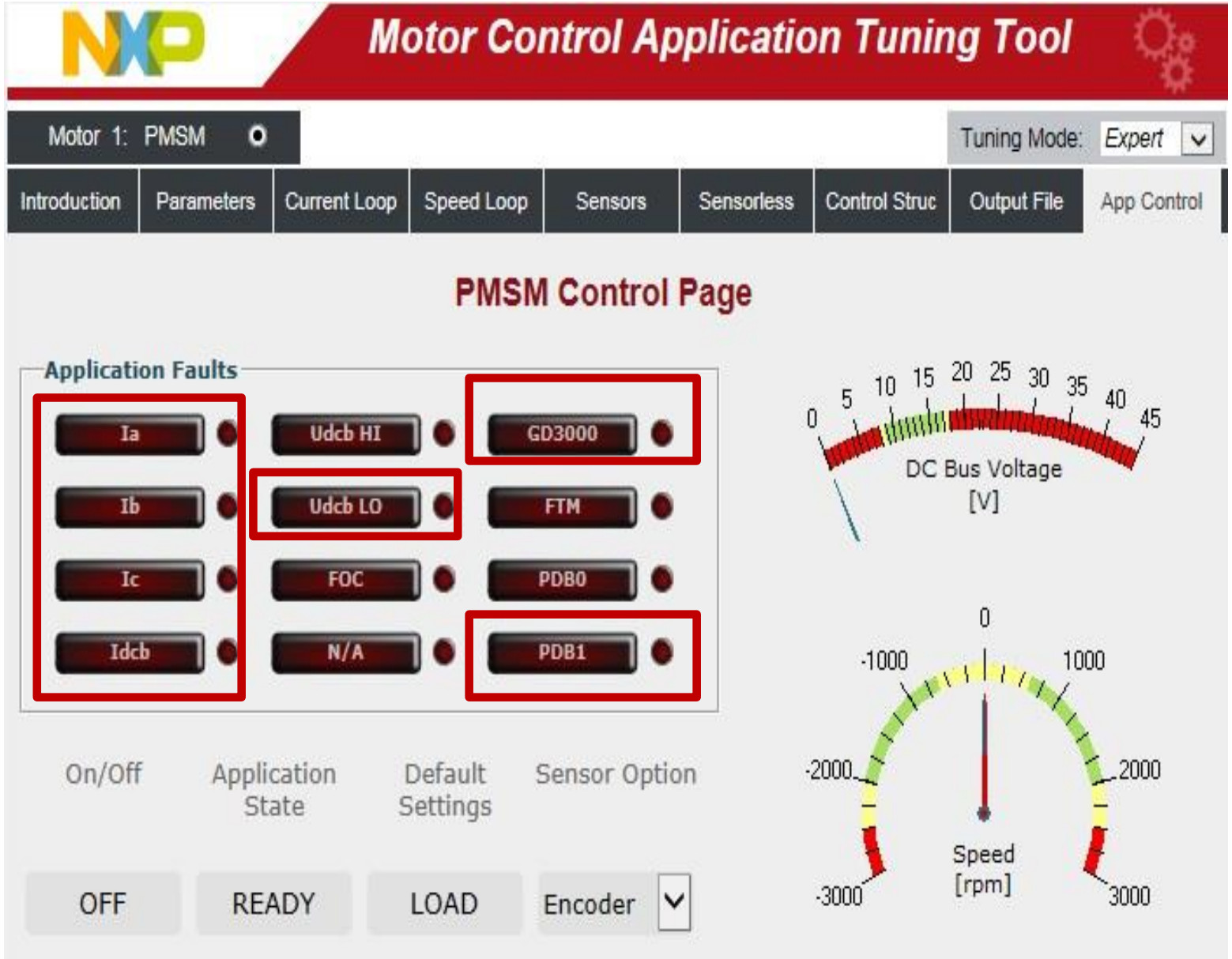
ADC Measurement: +/-1.6A



Current Probe: +/-2.5A



Faults Handling



Encountered following faults during debug:

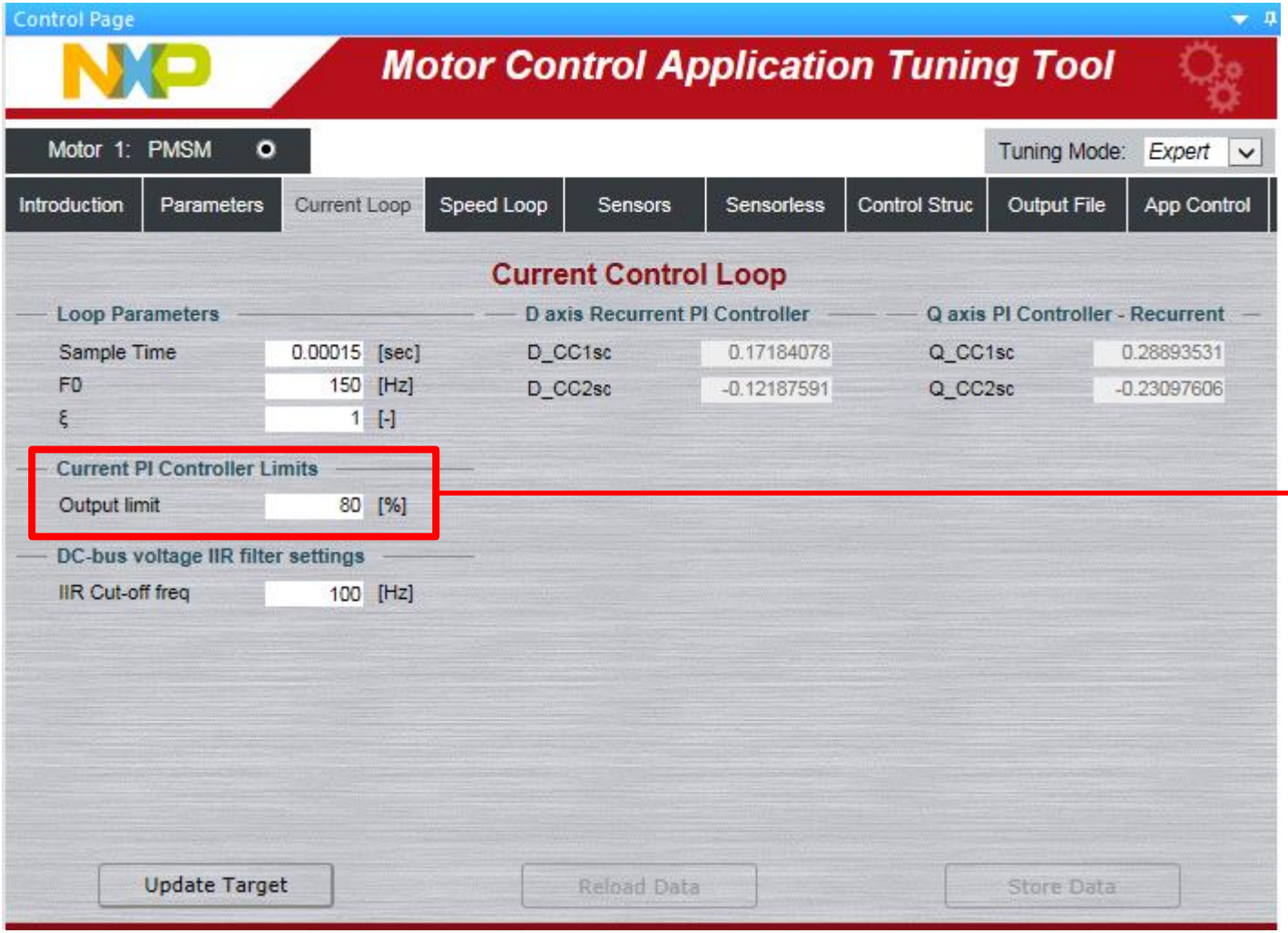
Ia/Ib/Ic/Idcb over-current:
Change the current limits values set in configuration header file.

Udcb Lo:
Maybe the power supply voltage is pulled low by transient big current.
Properly increase the power supply current limit.

GD3000:
Adjust the resistor on PCB to change the over-current limit value

PDB1:
PDB1 sequence error, maybe ADC conversion is not completed while a new PDB pre-trigger occurred.

Current Loop Parameters



This is the max allowed PWM duty 80%.

SECURE CONNECTIONS
FOR A SMARTER WORLD