MAGNIV DEEP DIVE TRAINING

RAYMOND TANG

2019.12

SECURE CONNECTIONS
FOR A SMARTER WORLD

CONFIDENTIAL AND PROPRIETARY

Agenda

- MagniV Family Overview
- S12Z Core Introduction
- Peripheral Introduction (Selected)
  - CPMU
  - Power Domain
  - PMF, PTU and ADC
  - GDU
- Case Sharing
- QA

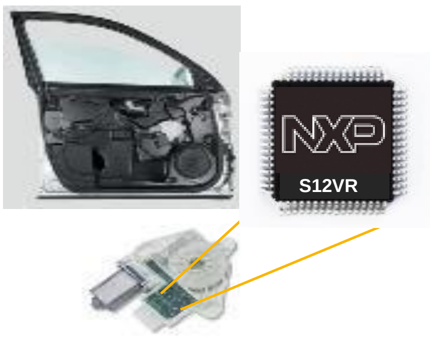
MAGNIV FAMILY OVERVIEW

MagniV Family Overview

S12 MagniV simplifies system design by integrating High-Voltage (HV) analog features onto MCUs for automotive applications

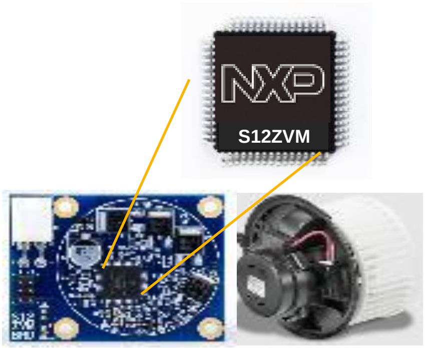
Motor Control focus

S12VR
Relay driven motors



- Window lift
- Sunroof
- Power doors

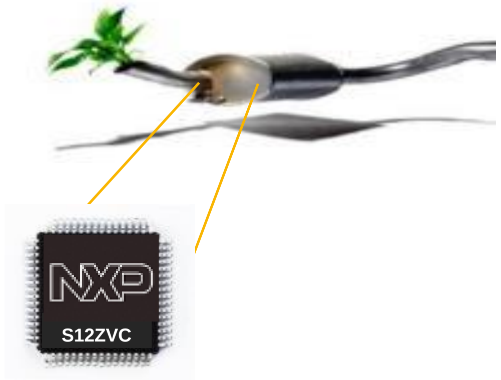
S12ZVM
BLDC/DC motors



- Fuel pump
- Oil pump
- Fans
- Wipers

Sensor Interface focus

S12ZVC
CAN nodes



- Safety sensors
- Emission sensors
- Gear shift

S12ZVL
LIN Nodes

- Steering wheel switches
- Door modules
- Sensors

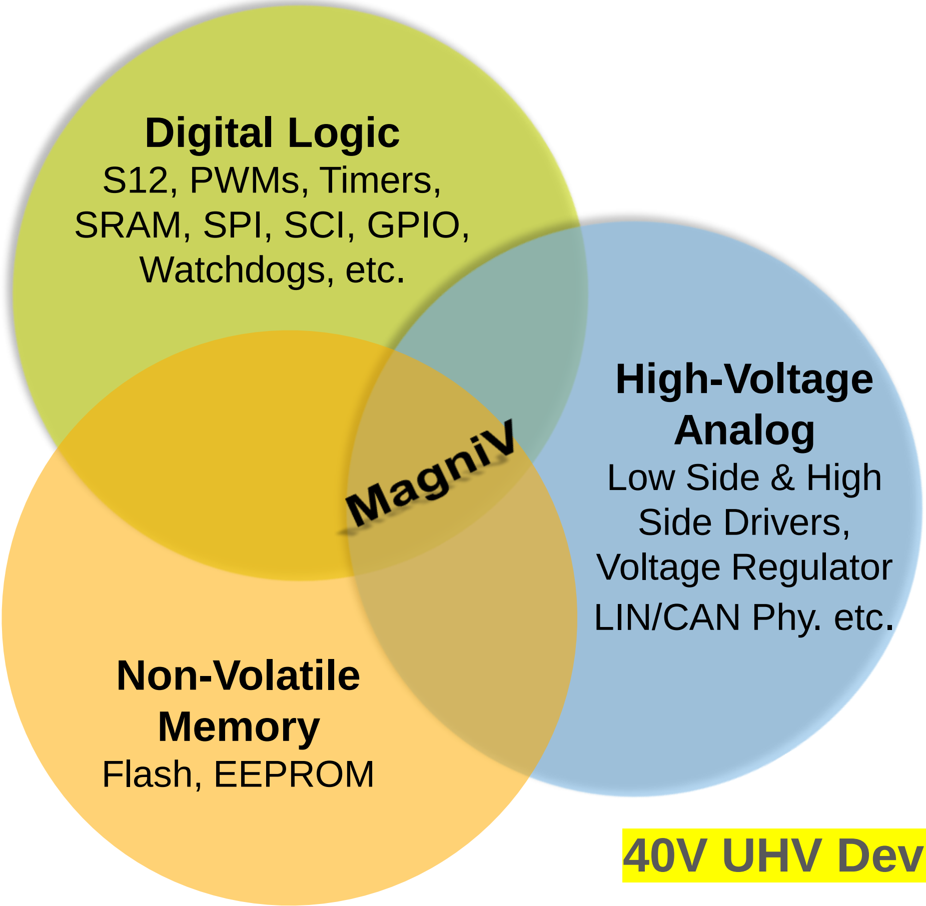
✓ **Reduced PCB Space**

✓ **Reduced Bill of Material**

✓ **Improved manufacturing efficiency and quality**

✓ **Simplified development**

MagniV Family Overview - Technology



Digital Logic
S12, PWMs, Timers, SRAM, SPI, SCI, GPIO, Watchdogs, etc.

High-Voltage Analog
Low Side & High Side Drivers, Voltage Regulator
LIN/CAN Phy. etc.

Non-Volatile Memory
Flash, EEPROM

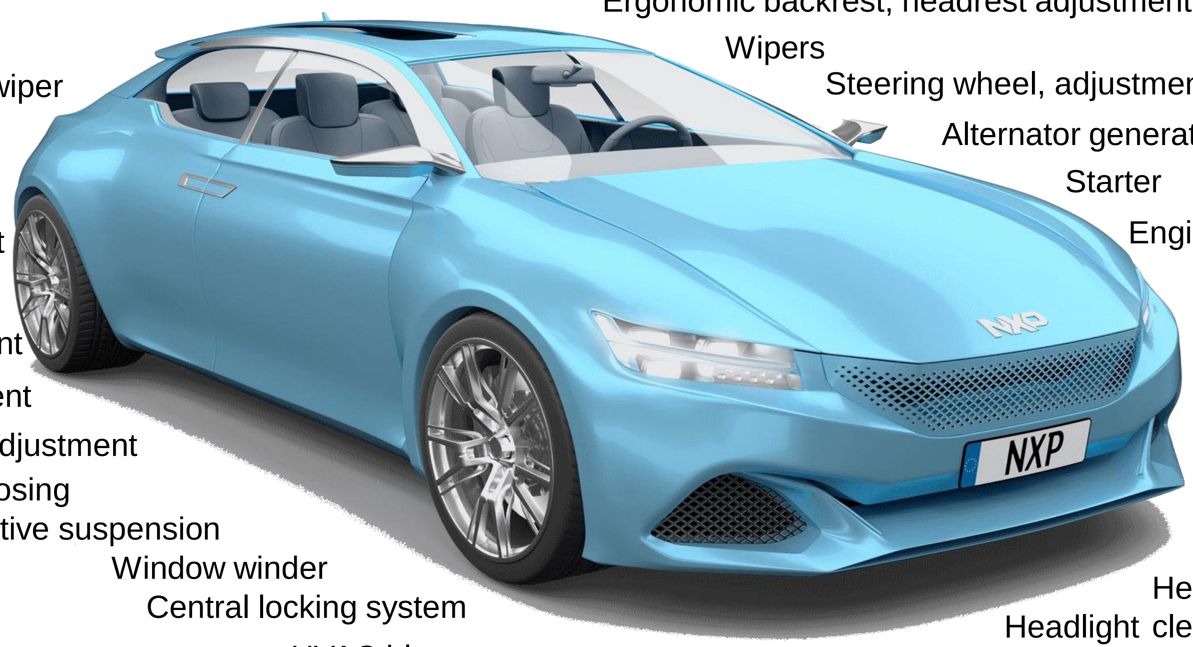
40V UHV Devices

Existing
Low Leakage 180nm CMOS+NVM

MagniV Family Overview - Motor Control

Electric Motors

Electric motors shipped into automotive applications increasing from 2.5 billion ('13) to 3 billion ('15)*



Sliding roof

Convertible roof

Circular pump for stationary heating system

Heating and air conditioning system

Idle position adjustment system

Ergonomic backrest, headrest adjustment

Tailgate closing

Wipers

Rear windscreen wiper

Steering wheel, adjustment

Belt system

Alternator generator

Starter

Fuel pump

Engine cooling fan

Headrest adjustment

Headlight range adjustment unit

Seat control

Backrest adjustment

Circular pump for heating and cooling water circuit

Mirror adjustment

Rear seat adjustment

Door closing

Scavenging pump, high-pressure pump

Active suspension

Window winder

Headlight cleaning

Central locking system

Headlight tilting

HVAC blower

Arial drive

ABS pump

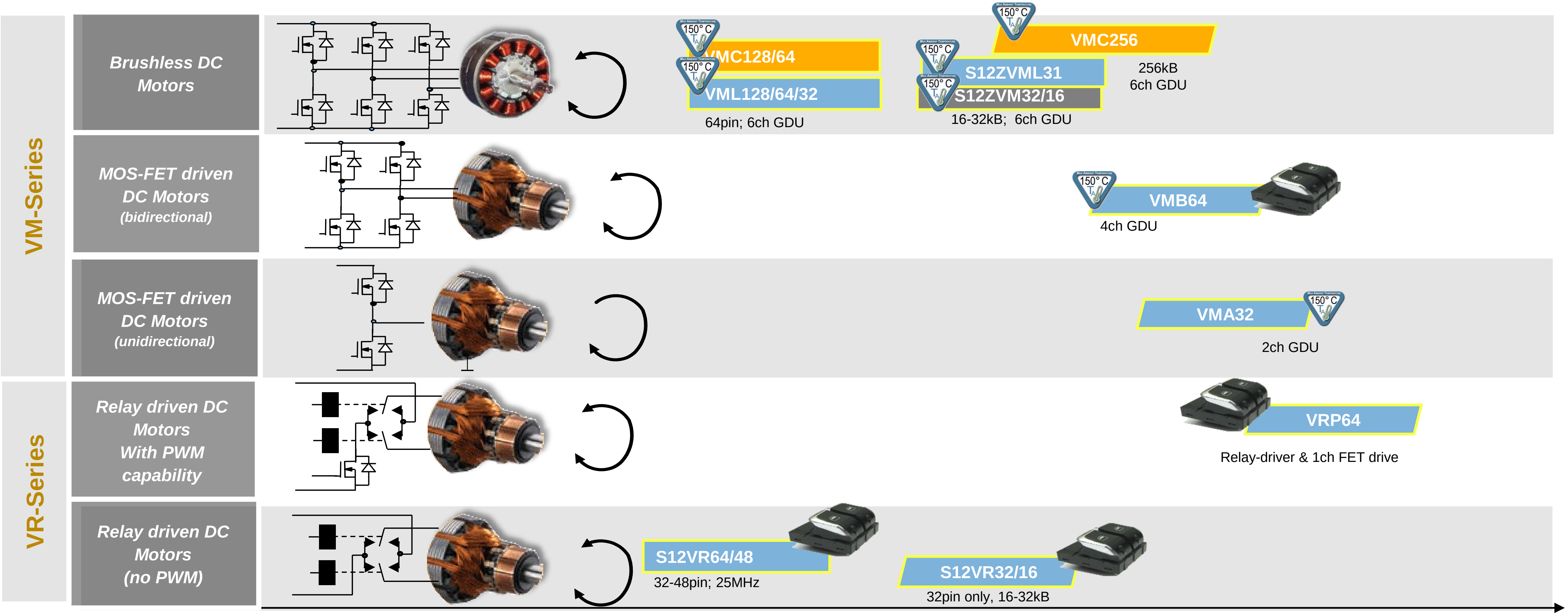
EPS drive

~30 electric motors per vehicle

S12 MagniV covering most common motors:
BL motors continuously/often in operation
DC motors rarely in operation

* according report from IHS Inc

MagniV Family Overview - Motor Control Products



VM-Series

Brushless DC Motors

VMC128/64
VML128/64/32
64pin; 6ch GDU

S12ZVML31
S12ZVM32/16
16-32kB; 6ch GDU

VMC256
256kB
6ch GDU

MOS-FET driven DC Motors (bidirectional)

VMB64
4ch GDU

MOS-FET driven DC Motors (unidirectional)

VMA32
2ch GDU

VR-Series

Relay driven DC Motors With PWM capability

VRP64
Relay-driver & 1ch FET drive

Relay driven DC Motors (no PWM)

S12VR64/48
32-48pin; 25MHz

S12VR32/16
32pin only, 16-32kB

🟦 LIN applications
🟧 CAN applications
⬛ PWM controlled apps

Switch panel interface
(HS-drivers & HVIs)
Main usecase: WL/SR

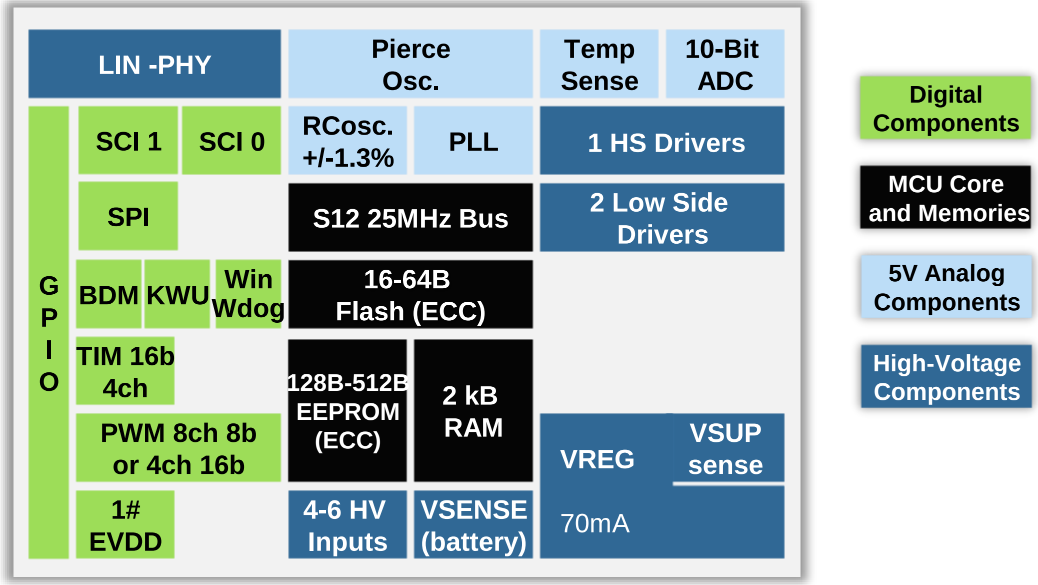
150° C High temp option (AEC Grade 0)

MagniV Family Overview - S12VR

Relay based DC Motors

Key Features:

- S12 (25 MHz max) 16-bit CPU compatible with the S12G family and MM912 solutions.
- Voltage Regulator operating directly from car battery (No ext regulator needed) capable to drive 20mA to drive offchip components (eg powering Hall sensor))
- LIN Physical Layer: LIN 2.x / J2602 compliant ; +/- 8kV ESD capability
- Up to 512B EEPROM with ECC, 4 byte erasable
- 2 Low-Side drivers with active clamps to drive relays (inductive load) for bi-directional brushed DC Motors
- Up to 2 HS drivers: For indicator LED and Switch supply
- 4 High Voltage Inputs: 12V Inputs for Switch Monitoring, ESD-protected, can be used for wake-up/interrupts or 12V analog inputs routed to ADC internally through selectable divider ratio.
- On chip RC Oscillator; trimmed to +/- 1,3% tolerance over full temperature range



LIN -PHY

Pierce Osc.

Temp Sense

10-Bit ADC

GPIO

SCI 1

SCI 0

RCosc. +/-1.3%

PLL

1 HS Drivers

SPI

S12 25MHz Bus

2 Low Side Drivers

BDM

KWU

Win Wdog

16-64B Flash (ECC)

TIM 16b 4ch

128B-512B EEPROM (ECC)

2 kB RAM

PWM 8ch 8b or 4ch 16b

VREG

VSUP sense

70mA

1# EVDD

4-6 HV Inputs

VSENSE (battery)

Digital Components

MCU Core and Memories

5V Analog Components

High-Voltage Components

Target Applications

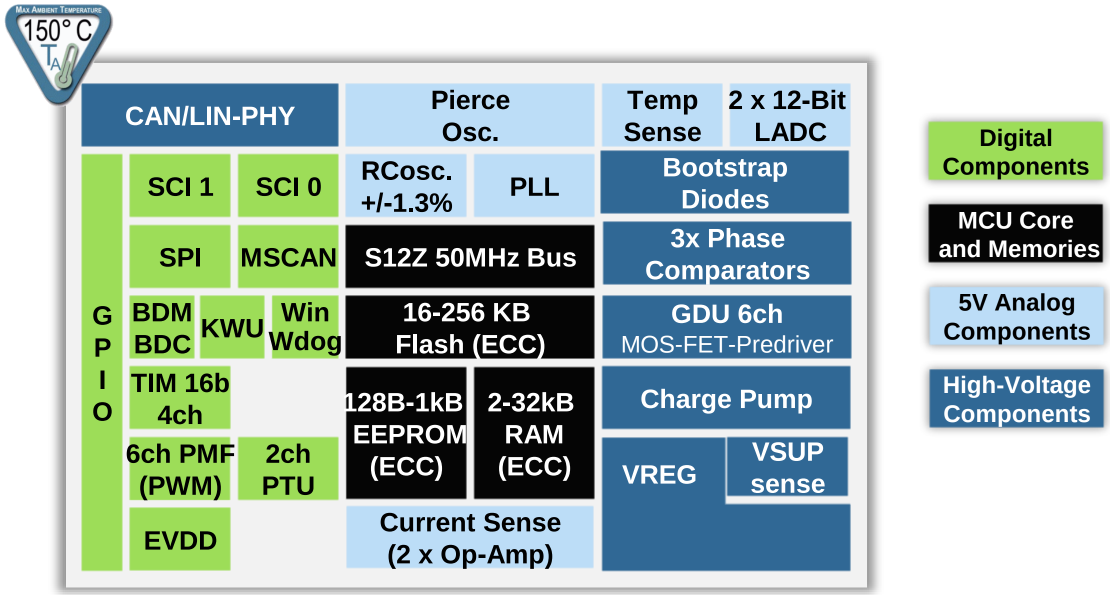
- Automotive power window lift / sunroof with antipinch
- Any relay driven DC motors
- LIN slaves with space constraints

Family options:

- Flexible Flash Options: 16kB to 64kB Flash
- Packaging: 32-LQFP or 48-LQFP
- C / V / M Temperature options (up to 125°C Ta)

MagniV Family Overview - S12ZVM *(Carcassonne/Obidos/VMC256)*

BLDC/PMSM/SR motor control

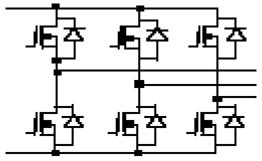


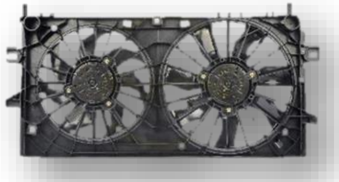
Key Features:

- S12Z CPU @ 50MHz bus speed
- 6ch Gate Drive Unit (GDU) with 50-150nC total Gate Charge drive capability, incl charge pump for High-Side, Bootstrap diodes for charging external bootstrap capacitors
- Embedded VREG with switchable 5V/20mA sensor supply
- LIN PHY, LIN2.1 / 2.2 / J2602 compliant
- CAN-PHY
- Dual 12bit list-based ADC (LADC), synch with PWM through Programmable Trigger Unit (PTU)
- 2x Op-amp for current sensing

Target applications:

- Sensorless BLDC or PMSM motor control
- Switched Reluctance Motor
- Bidirectional DC motors (H-Bridge)
- Various pumps (oil, fuel, water, vacuum)
- Cooling fan, HVAC blower, Turbocharger





Options:

- Package: 64-LQFP-EP, 48 LQFP-EP, 80-LQFP-EP
- Memory: 16kB / 32kB / 64kB / 128kB / 256kB Flash
- Spec-Options:
  - L with LIN phy
  - C with CAN-PHY (256kB only)
  - C with 2nd Vreg for external CAN phy (128/64kB)
  - “ “ with High Voltage PWM-communication interface
- Temperature: V / M / W (up to 150°C Ta per AEC-Q100 Grade 0)

MagniV Family Overview - S12ZVMB

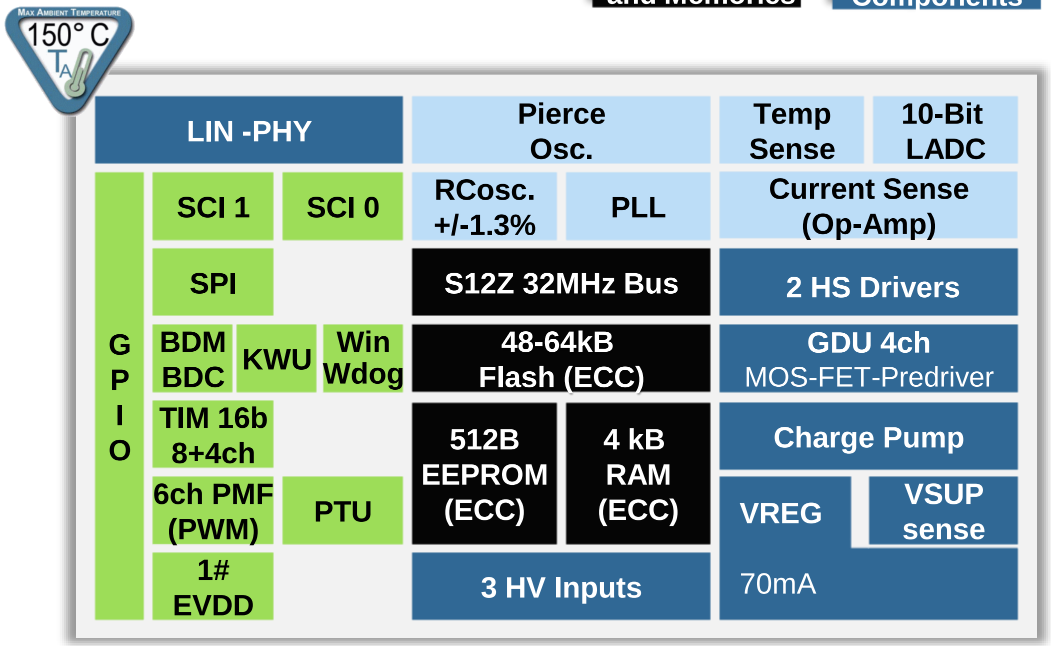
LIN based Integrated H-Bridge driver

Digital Components

5V Analogue Components

MCU Core and Memories

High-Voltage Components



Max Ambient Temperature 150° C T_A

LIN -PHY | Pierce Osc. | Temp Sense | 10-Bit LADC

GPIO

SCI 1 | SCI 0 | RCosc. +/-1.3% | PLL | Current Sense (Op-Amp)

SPI | S12Z 32MHz Bus | 2 HS Drivers

BDM BDC | KWU | Win Wdog | 48-64kB Flash (ECC) | GDU 4ch MOS-FET-Predriver

TIM 16b 8+4ch | 512B EEPROM (ECC) | 4 kB RAM (ECC) | Charge Pump

6ch PMF (PWM) | PTU | VREG | VSUP sense

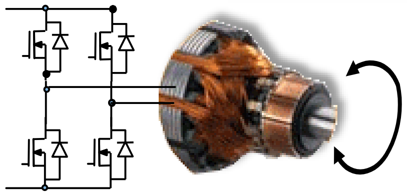
1# EVDD | 3 HV Inputs | 70mA

Key Features:

- S12Z CPU @ 32MHz bus speed
- VREG + 5V/20mA switchable sensor supply
- LIN PHY, LIN2.1 / 2.2 / J2602 compliant
- High Voltage Inputs (HVI) with internal connection to ADC for analog 12V measurements
- High-Side Drivers for switch panel and LED
- H-Bridge Gate Pre-Driver for 4-NMOS control (Gate Charge 50-80nC)

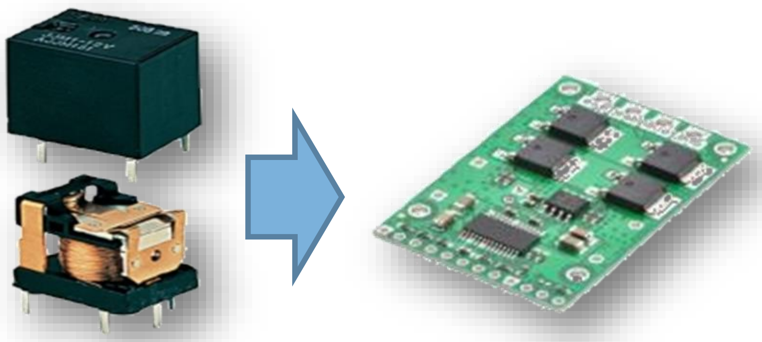
Target applications:

- Windowlift / Sunroof
- LIN-controlled Valves for gases / liquids (EGR-control)
- Seat-position, Lordosis
- Belt pretentioner, prefetcher



Options:

- Package: 48-LQFP; (64 LQFP tbd)
- Memory: 48 … 64kB Flash
- Temperature: V / M / W

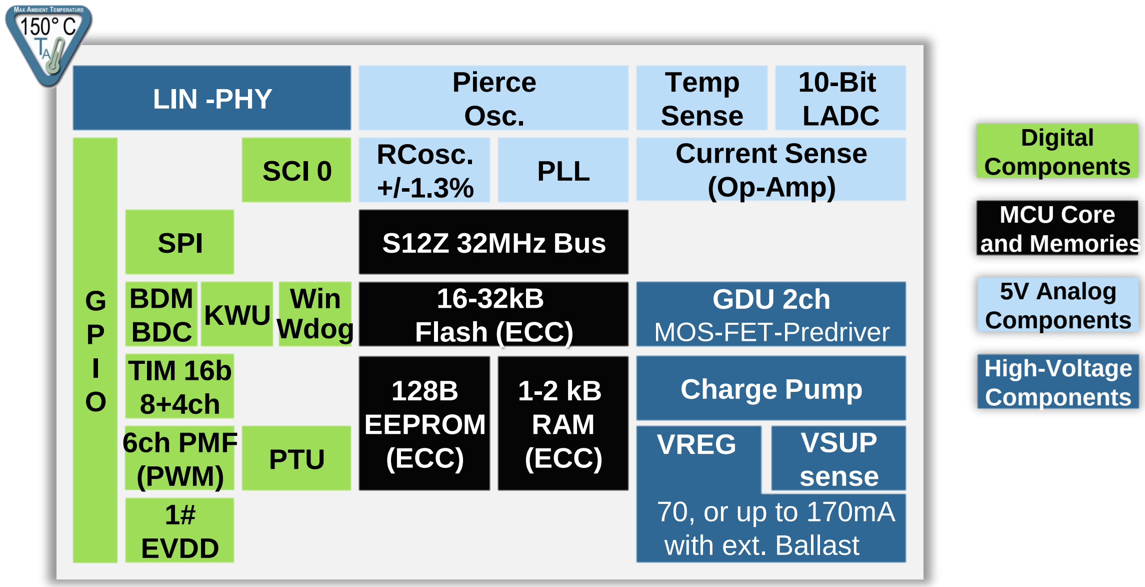


MagniV Family Overview - S12ZVMA

LIN based Integrated half-Bridge driver

Key Features:

- S12Z CPU @ 32MHz bus speed
- VREG + 5V/70mA; nominal 6-18V; extended (with degradation) down to 3.5V with boost option (fuelpump)
- HV-PHY / LIN PHY, LIN2.1 / 2.2 / J2602 compliant; HV-PHY allows control of directly through 12V PWM command (with error/tack response)
- 16/32kB Flash, 2kB RAM, 128B EEPROM
- Half-Bridge Gate Pre-Driver for 2-NMOS control (1xLS, 1xHS; Gate Charge 50-80nC)
- Integrated Bootstrap Diode (to charge the external bootstrap capacitor)



Max Ambient Temperature 150° C T_A

LIN -PHY

Pierce Osc.

Temp Sense

10-Bit LADC

GPIO

SCI 0

RCosc. +/-1.3%

PLL

Current Sense (Op-Amp)

SPI

S12Z 32MHz Bus

BDM BDC

KWU

Win Wdog

16-32kB Flash (ECC)

GDU 2ch MOS-FET-Predriver

TIM 16b 8+4ch

128B EEPROM (ECC)

1-2 kB RAM (ECC)

Charge Pump

6ch PMF (PWM)

PTU

VREG

VSUP sense

70, or up to 170mA with ext. Ballast

1# EVDD

Digital Components

MCU Core and Memories

5V Analog Components

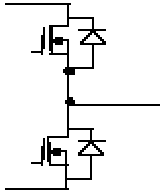
High-Voltage Components

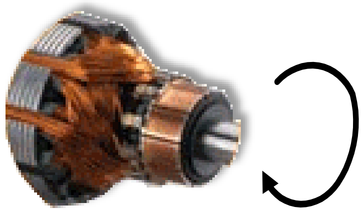
Options:

- Package: 32-LQFP; 48-LQFP
- Memory: 16 … 32kB Flash
- Temperature: V, M, W
- LIN: with LIN-PHY or with HV-PWM-interface

Applications:

- DC-motors (unidirectional) such as pumps, fans
- Electromechanic actuators (eg. Valves)
- Any kind of automotive load that remotely needs to get switched by a FET (via a LIN or PWM-signal) like horn, aux. Heating, lighting, smart junction box, ...



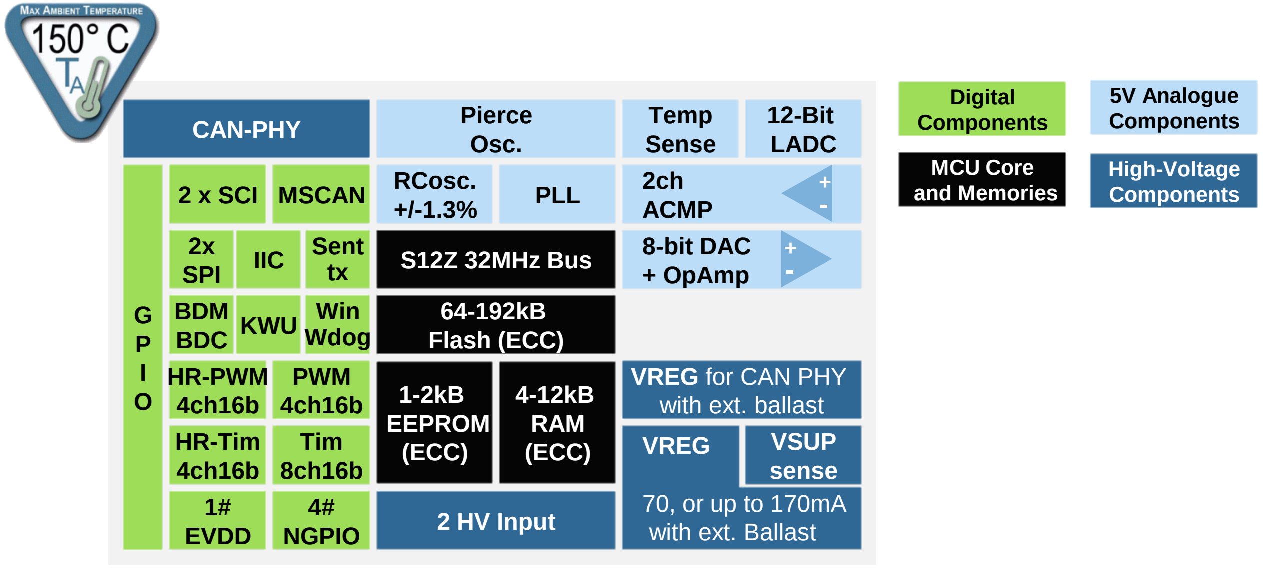


MagniV Family Overview - S12ZVC

Integrated CAN Nodes

Key Features:

- S12Z core (32 MHz)
- On chip CAN PHY:
  - CAN-supply requires ext. Ballast Transistor
  - Dominant Txd timeout
  - OEM emission limits achieved WITHOUT Choke (up to 500kbps)
- 12V VREG (device + ext comp)
  - 70mA total, 170mA with ext. Ballast
- High Voltage Input (HVI)
  - internal tied ADC for 12V analog measurements
- Specific features for sensor applications:
  - list-based 12-Bit ADC (LADC)
  - 16ns resolution Timer / PWM
  - 2x Analog Comparator with 8Bit DAC
  - SENT



Family Options:

- Flexible Memory Options: 64 kB to 128 kB Flash version
- 48-LQFP or 64-LQFP-EP Packaging
- C / V / M / W Temperature options (**up to 150°C Ta**)
- Fully featured (S12ZVCAx) or reduced featureset S12ZVCx)

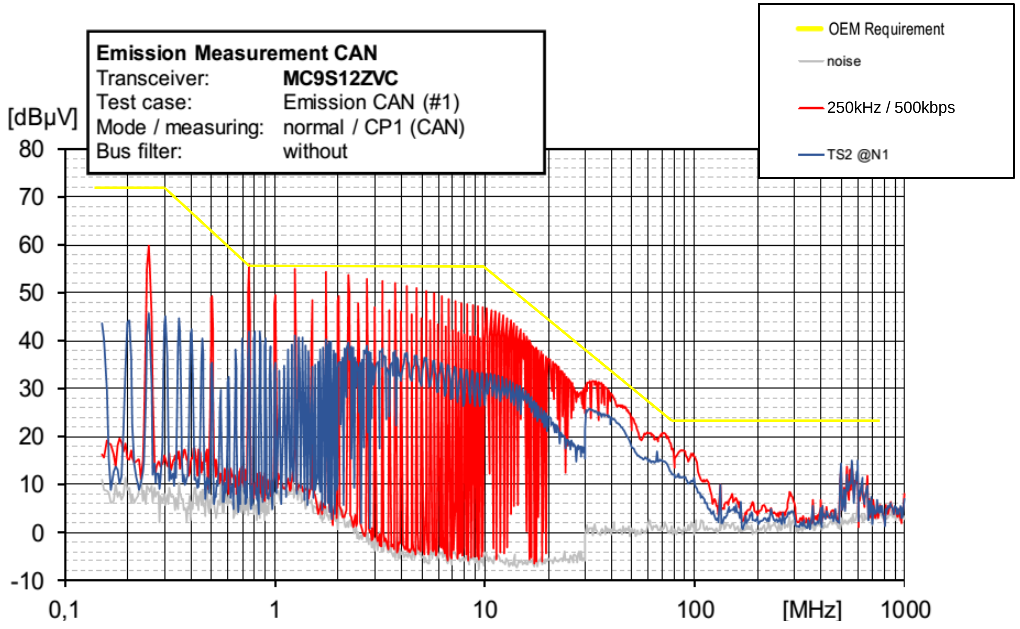
S12ZVC: OEM Emission Limits Achieved without Choke (up to 500kbps)

Operation without Common Mode Choke

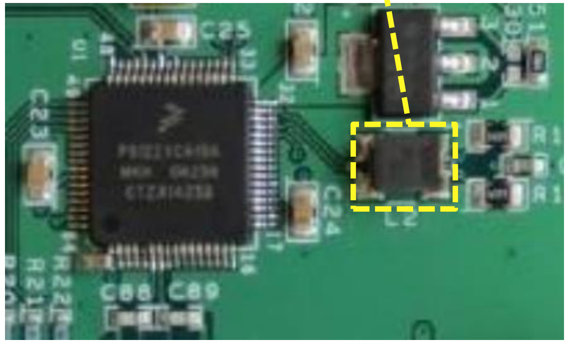
Saving:
~$0.20 BOM cost
~40mm² PCB area

Configuration without bus filter

Test case 1:
Emission CAN - normal mode

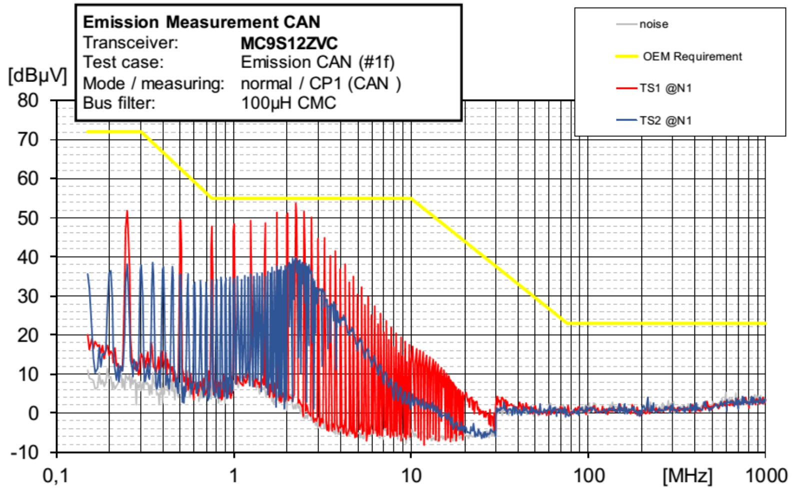


Operation With Common Mode Choke



Configuration with 100 µH CMC

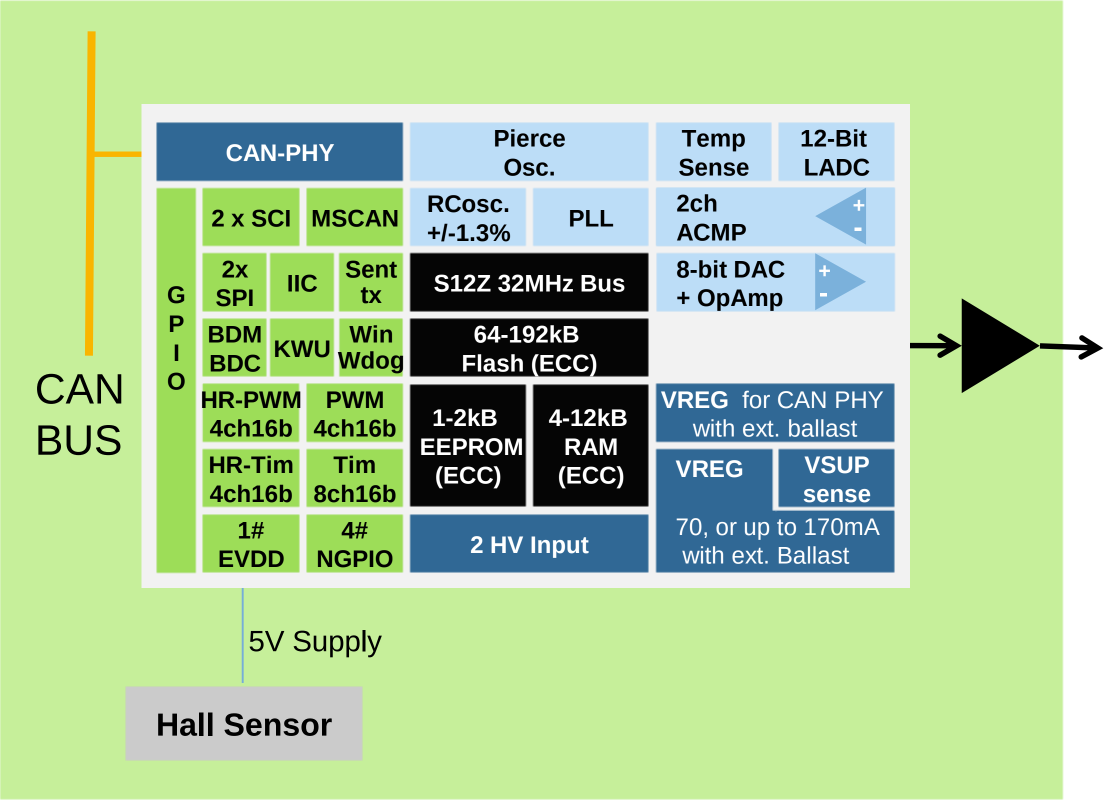
Test case 1f:
Emission CAN - normal mode



S12ZVC for Seatbelt Pretensioner

S12ZVC Benefits:

- CAN-based
- Limited PCB-space
- ASIL-requirements



CAN BUS

CAN-PHY

Pierce Osc.

Temp Sense

12-Bit LADC

GPIO

2 x SCI

MSCAN

RCosc. +/-1.3%

PLL

2ch ACMP

2x SPI

IIC

Sent tx

S12Z 32MHz Bus

8-bit DAC + OpAmp

BDM BDC

KWU

Win Wdog

64-192kB Flash (ECC)

HR-PWM 4ch16b

PWM 4ch16b

1-2kB EEPROM (ECC)

4-12kB RAM (ECC)

VREG for CAN PHY with ext. ballast

HR-Tim 4ch16b

Tim 8ch16b

VREG

VSUP sense

1# EVDD

4# NGPIO

2 HV Input

70, or up to 170mA with ext. Ballast

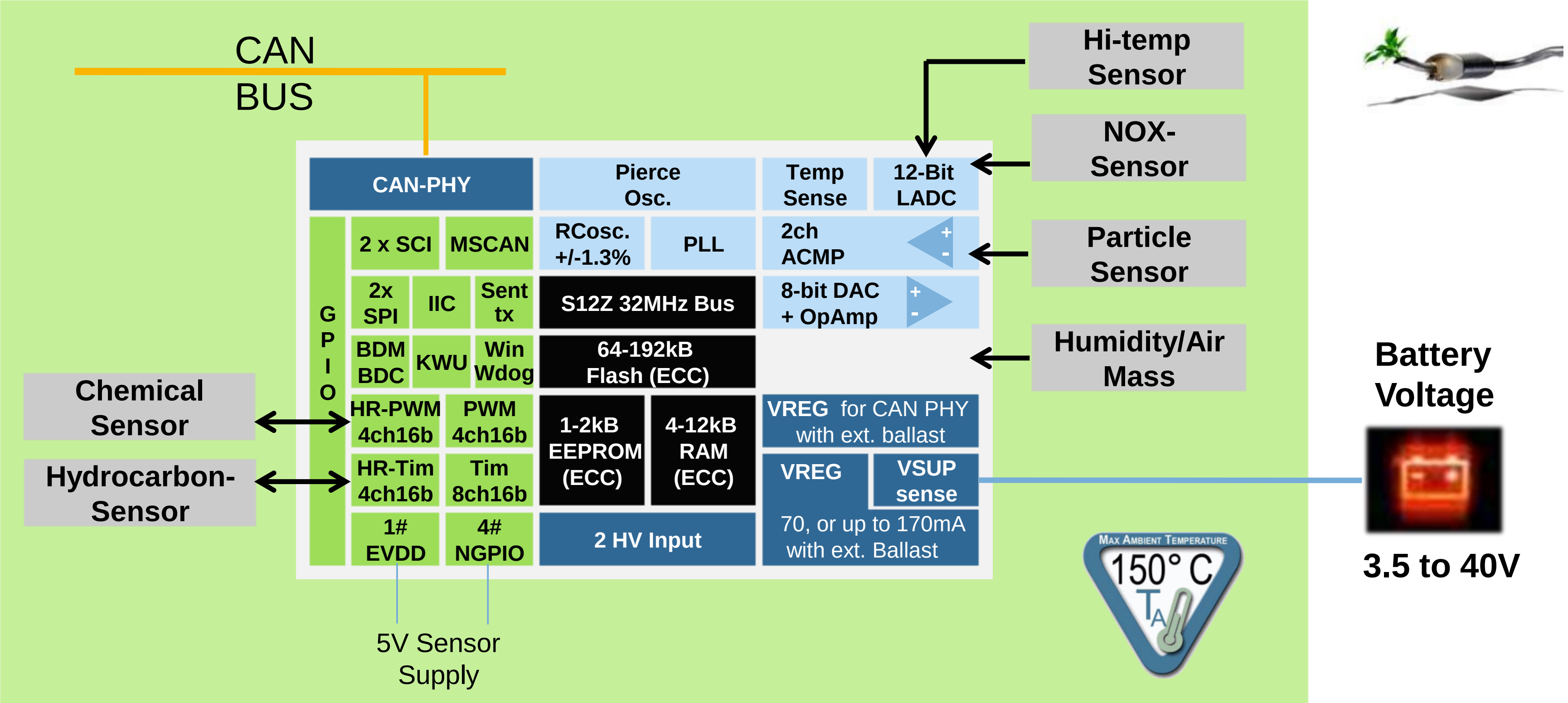
5V Supply

Hall Sensor

S12ZVC for Powertrain Sensors

S12ZVC Benefits:

- Limited PCB-space
- ASIL-requirements
- High resolution timers and DMA enabled LADC
- On-chip analog comparator and DAC
- EVDD 5 V switchable sensor supply



CAN BUS

CAN-PHY | Pierce Osc. | Temp Sense | 12-Bit LADC

GPIO

2 x SCI | MSCAN | RCosc. +/-1.3% | PLL | 2ch ACMP

2x SPI | IIC | Sent tx | S12Z 32MHz Bus | 8-bit DAC + OpAmp

BDM BDC | KWU | Win Wdog | 64-192kB Flash (ECC)

HR-PWM 4ch16b | PWM 4ch16b | 1-2kB EEPROM (ECC) | 4-12kB RAM (ECC) | VREG for CAN PHY with ext. ballast

HR-Tim 4ch16b | Tim 8ch16b | VREG | VSUP sense

1# EVDD | 4# NGPIO | 2 HV Input | 70, or up to 170mA with ext. Ballast

5V Sensor Supply

Chemical Sensor

Hydrocarbon-Sensor

Hi-temp Sensor

NOX-Sensor

Particle Sensor

Humidity/Air Mass

Max Ambient Temperature 150° C T_A

Battery Voltage

3.5 to 40V

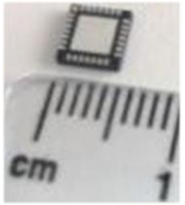
MagniV Family Overview - S12ZVL

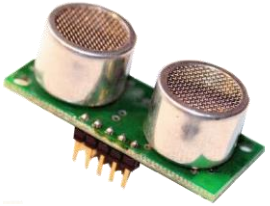
Integrated LIN Nodes

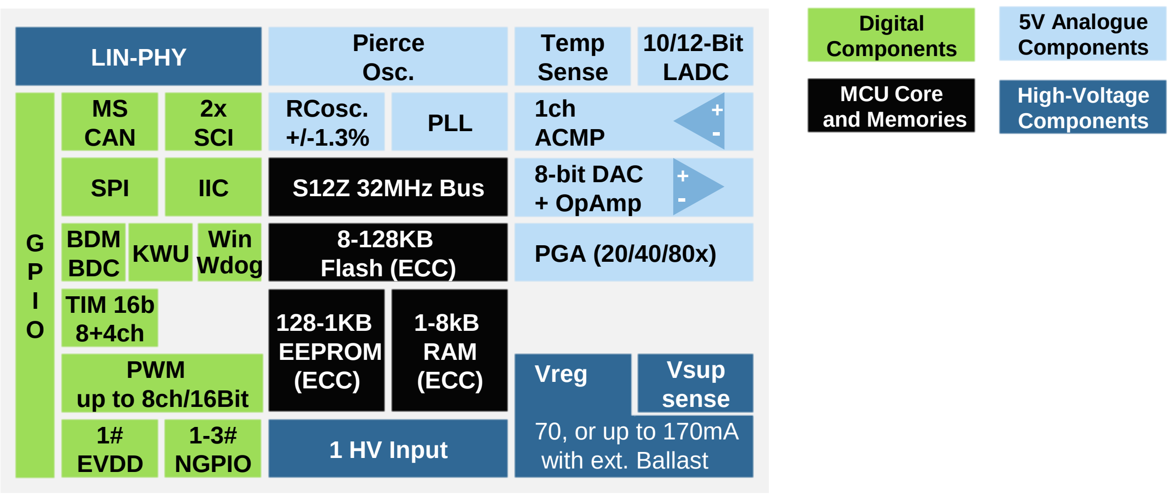
Key Features:

- S12Z core (32 MHz)
- 12V VREG (device + ext comp)
  - 70mA total (170mA with ext. Ballast)
- LIN-PHY, LIN2.x / J2602 compliant
- MS-CAN digital interface (48K+ only)
  - CAN – LIN gateway
- On chip RC Oscillator
  - +/- 1.3% over full temp range
  - No need for ext Xtal
- High Voltage Input (HVI)
  - internal tied ADC for 12V analog measurements
- Evdd 5V/20mA (switchable output overcurrent protected)
- List-based 10-Bit ADC (LADC)
- Optional S12ZVLA : enhanced analog
  - 12-Bit LADC, PGA, Analog Comparator, and DAC
- 1-3x N-GPIO (25 mA sink capability

Max Ambient Temperature 150° C TA







LIN-PHY
Pierce Osc.
Temp Sense
10/12-Bit LADC
GPIO
MS CAN
2x SCI
RCosc. +/-1.3%
PLL
1ch ACMP
SPI
IIC
S12Z 32MHz Bus
8-bit DAC + OpAmp
BDM BDC
KWU
Win Wdog
8-128KB Flash (ECC)
PGA (20/40/80x)
TIM 16b 8+4ch
128-1KB EEPROM (ECC)
1-8kB RAM (ECC)
PWM up to 8ch/16Bit
Vreg
Vsup sense
1# EVDD
1-3# NGPIO
1 HV Input
70, or up to 170mA with ext. Ballast

Digital Components
5V Analogue Components
MCU Core and Memories
High-Voltage Components

Family Options:

- Flexible Memory Options: 8 kB to 128 kB Flash version
- Optional Analog Enhancement (S12ZVLA64/96/128) with 12 Bit ADC, ACMP, DAC & PGA
- 32-LQFP , 48-LQFP or 32QFN Packaging
- C / V / M /W Temperature options (up to 150°C Ta)

S12ZVL Target Applications

LIN Sensors

Product Function

- Connect sensors to LIN-Network (with signal pre-conditioning)

Market Requirements

- LIN-PHY, 12V-Vreg, MCU
- Small form factor (QFN)
- ADC, SPI

LIN Switch Panels

Product Function

- Read multiple switch-positions and feed into LIN-network

Market Requirements

- LIN-PHY, 12V-Vreg, MCU
- Multiple GPIOs
- ADC

LIN Actuator

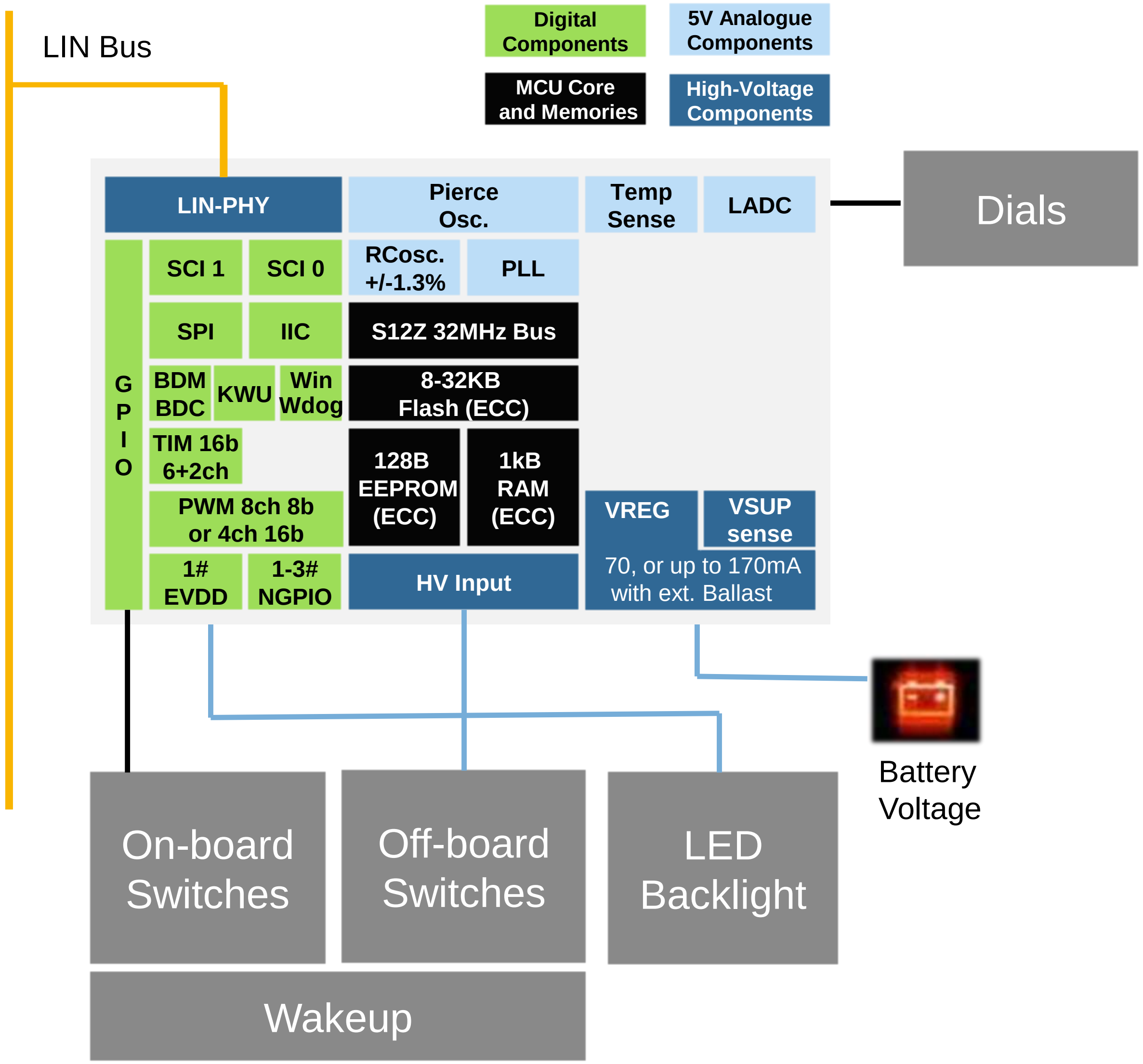
Product Function

- Convert LIN-command into an activity (eg driving LEDs)

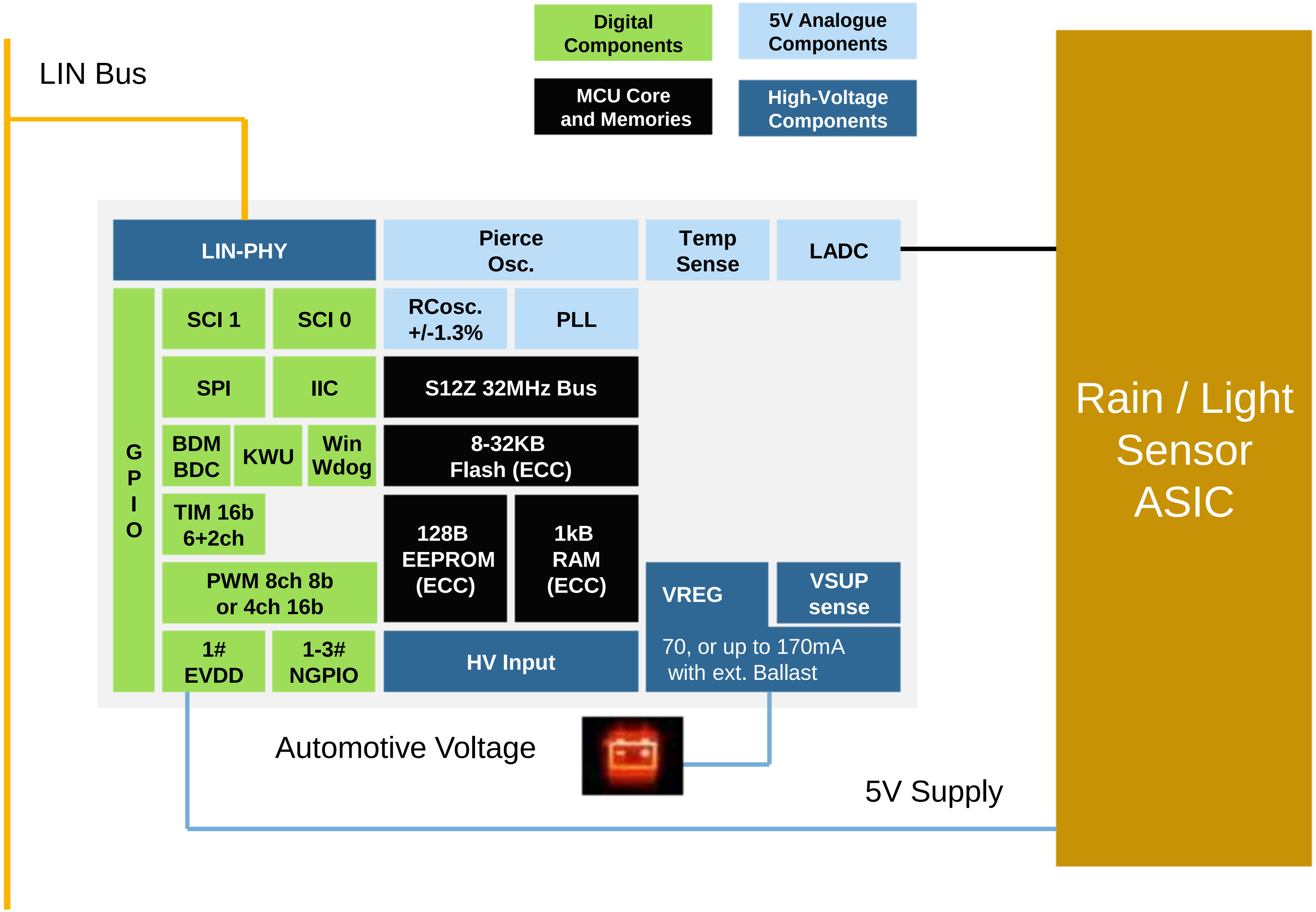
Market Requirements

- LIN-PHY, 12V-Vreg, MCU
- Drivers (3x25mA drive strength in case of RGB-LED)
- ADC

S12ZVL for Switch Panel Applications



S12ZVL for Sensor Applications



Digital Components

5V Analogue Components

MCU Core and Memories

High-Voltage Components

LIN Bus

LIN-PHY

Pierce Osc.

Temp Sense

LADC

GPIO

SCI 1

SCI 0

RCosc. +/-1.3%

PLL

SPI

IIC

S12Z 32MHz Bus

BDM BDC

KWU

Win Wdog

8-32KB Flash (ECC)

TIM 16b 6+2ch

128B EEPROM (ECC)

1kB RAM (ECC)

PWM 8ch 8b or 4ch 16b

VREG

VSUP sense

70, or up to 170mA with ext. Ballast

1# EVDD

1-3# NGPIO

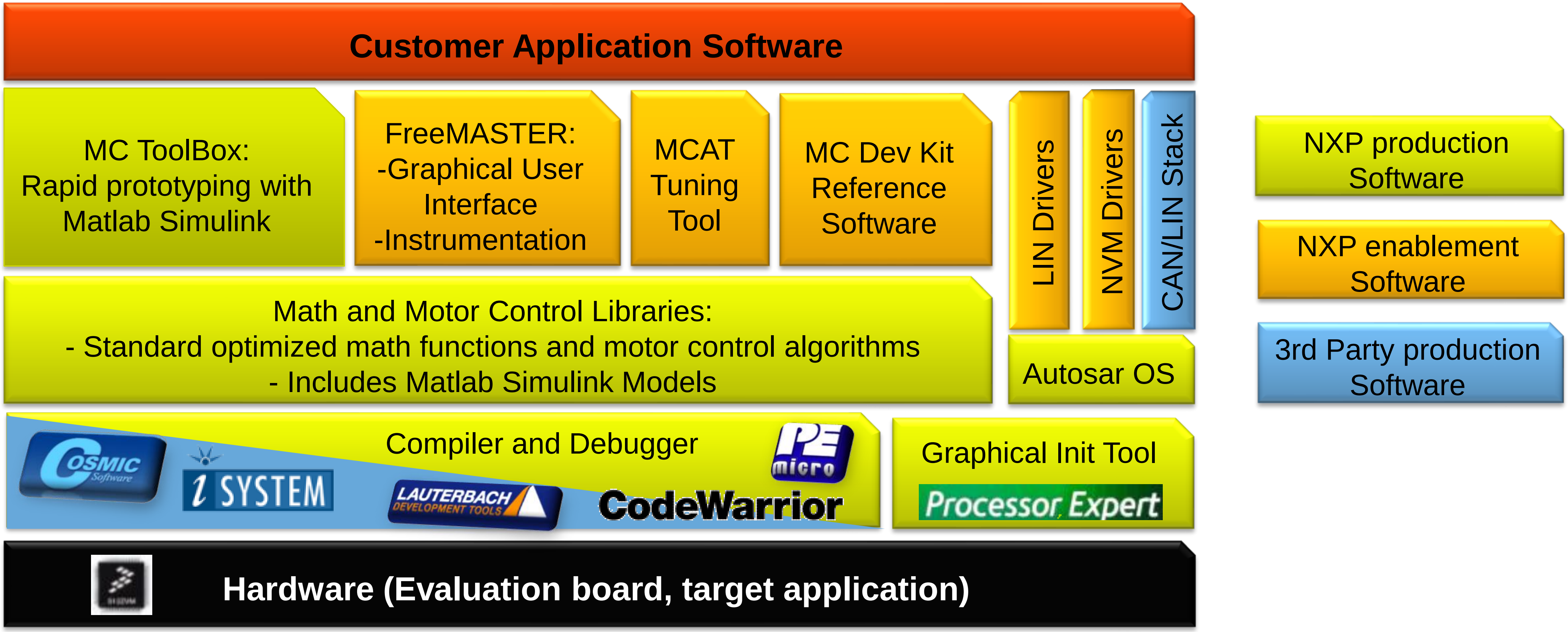
HV Input

Automotive Voltage

5V Supply

Rain / Light Sensor ASIC

MagniV Family Overview - The Complete Solution



Customer Application Software

MC ToolBox:
Rapid prototyping with
Matlab Simulink

FreeMASTER:
-Graphical User
Interface
-Instrumentation

MCAT
Tuning
Tool

MC Dev Kit
Reference
Software

LIN Drivers

NVM Drivers

CAN/LIN Stack

Math and Motor Control Libraries:
- Standard optimized math functions and motor control algorithms
- Includes Matlab Simulink Models

Autosar OS

Compiler and Debugger

Graphical Init Tool

Hardware (Evaluation board, target application)

NXP production
Software

NXP enablement
Software

3rd Party production
Software

MagniV Family Overview Summary

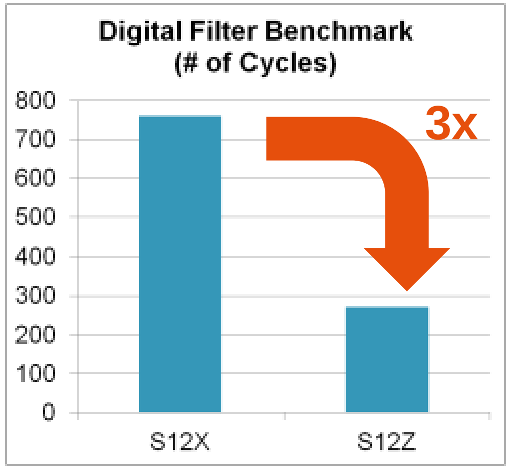
- MagniV Most Common Success Factors:
  - High analog **integration** for reduced PCB size and system cost
  - Wide **scalability** supporting platform design
  - **Ease of use** by having key active components integrated
  - **Pre-certification** for EMI/EMC for approval at major OEM’s reducing Tier1’s risk
  - **Market Leadership** in integrated solutions
  - Ahead of competition on several turnkey-solutions for **Faster Time to market**
  - **Grade0 support** not only for motor control
  - Strong **knowledge & support** on Software and Hardware enabling customers Motor Control Applications
  - Supporting **Safety & Security** Standards

S12Z CORE INTRODUCTION

S12Z Performance Benefits

Improved Performance for Motor Control

- 100 MHz CPU @ 50 MHz bus speed
- Harvard architecture accelerates data handling



- Improved standard math instructions (32bit MAC)
- Fractional math instructions added
- Advanced Register set optimized to achieve less memory access (improves current consumption)

Improved Software Friendliness

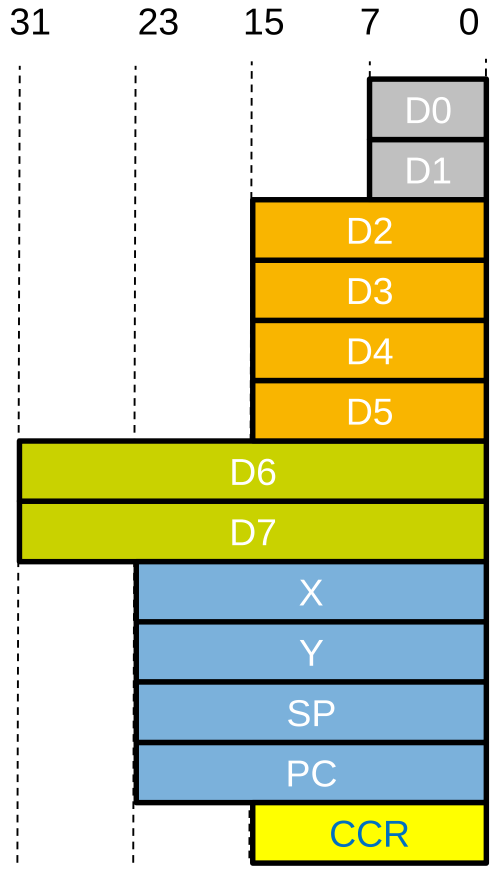
- 24-bit linear address map to ease software development and porting
- Instructions/addressing optimized for C programming
- Added 8- and 32-bit registers allow further compiler code size optimization

S12Z… really a 16-bit MCU?

24-bit address bus maps up to 16MB (no paging needed!)

- Multiple length registers / data paths:
  - 32-Bit data paths, ALU, Data registers
  - 24-bit address bus, Stack Pointer, Program Counter and X/Y Index registers
  - It has a 16-bit I/O data path
  - 16-bit is its “int” native data type
  - Handles 8-Bit data and indices better than S12X
- Benefits:
  - 24-bit address = 16MB vs. 64KB of a typical 16-bit address bus
  - Multiple length registers = less RAM load/store accesses

Expanded programmer’s model



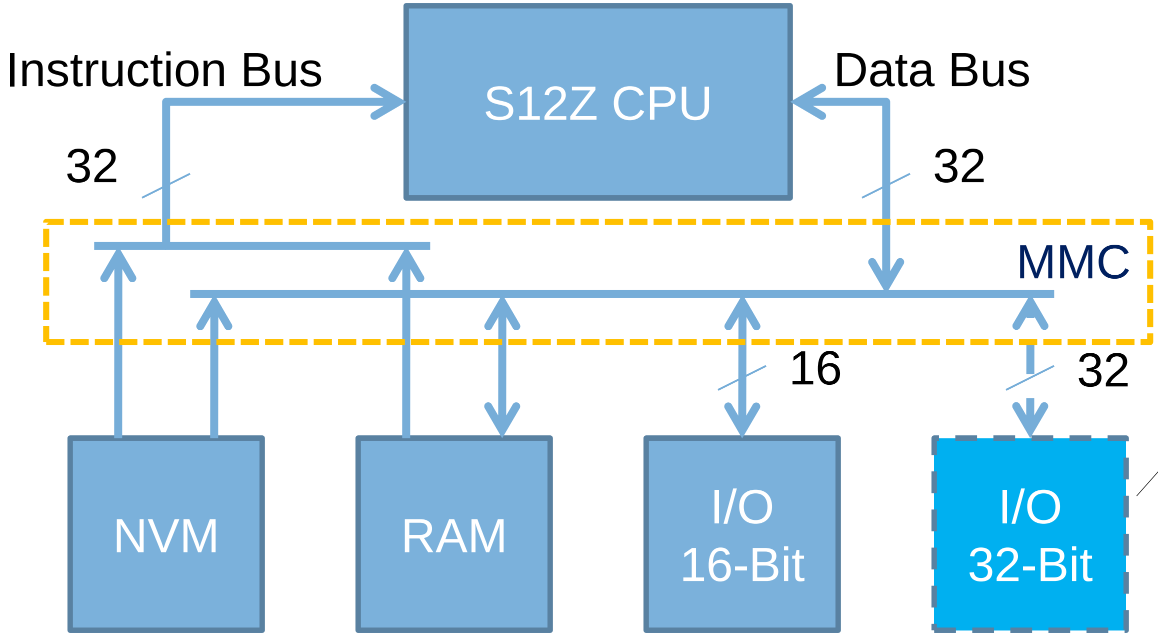
S12Z CPU Enhancements

Instructions and Addressing optimized for C-programming

- Harvard Architecture – Parallel data & code accesses
- CPU operates at 100MHz
- Fractional Math support
- Instructions/addressing optimized for C programming
- Register set optimized to reduce code size and memory access

Attribute	S12Z	S12XE
Shifter	**32**-Bit multi-bit 1 cycle	16-bit single-bit 2 cycles
Multiplier	**32*32** 2.5 cycles 16*16 1 cycle	-- 16*16 1 cycle
Divider	32 = **32/32** 18.5 cycles	32 = 32/16 11 cycles
MAC	32 += **32*32** 3.5 cycles	32 += 16*16 13 cycles
Fractional math support	**Yes**	No
Bus speed	50MHz	50MHz

S12Z core - Platform



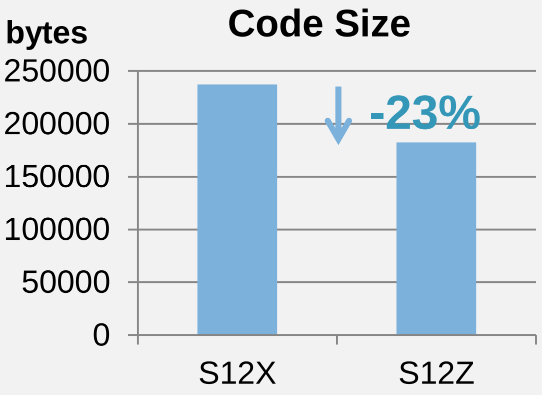
Optional! Allows addition of a 32-bit Peripherals

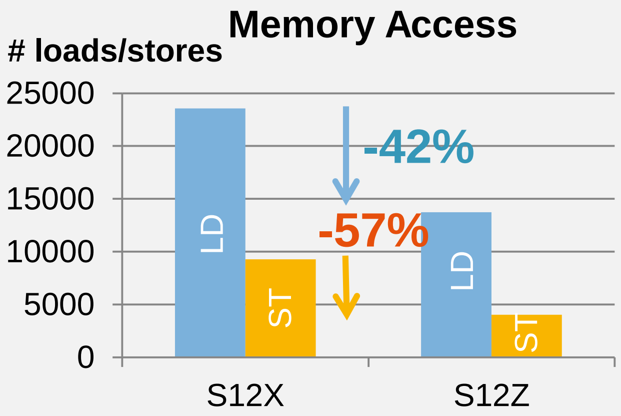
- CPU operates at 100MHz (All performance numbers for 180nm!)
- NVM works with 1 Wait-state => effective 20ns accesses
- RAM bus can load and store w/ 100MHz
- I/O busses are working w/ 50MHz to reduce power consumption and die area

S12Z Benchmarks Results

- S12Z typically saves ~20% code size versus S12X
- S12Z typically uses ~30% less memory accesses than S12X which saves power

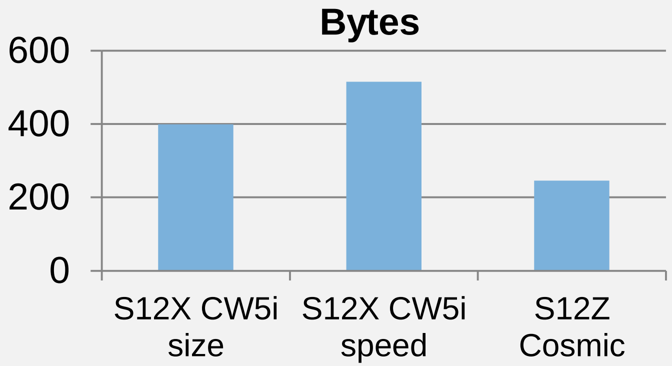
Large Application Code Example:

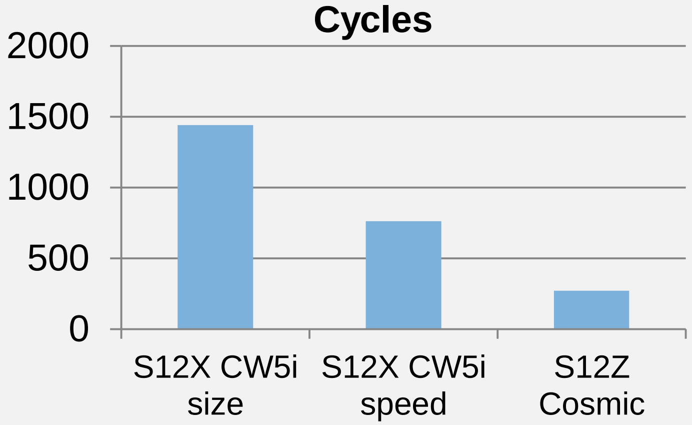




Digital Filter:

S12Z is faster and denser than any optimization option of S12X





S12Z – Cost aspects

- Code size typically 20% smaller than S12X

  ⇒ Smaller NVM size needed

  ⇒ Less NVM accesses => lower current consumption

- Register set optimized

  ⇒ Less RAM loads & Store required (ca. -30% vs. S12X)

  ⇒ lower current consumption

- Overall >2x better MIPS/mW expected

- Faster code development time due to simpler memory model and better “C-friendliness” of the instruction set

PERIPHERAL INTRODUCTION (SELECTED)

Peripheral Introduction - Overview

High-Voltage Components

VREG for tot. supply:
- 70mA w/o ext comp. or
- 170mA with ext. ballast

LIN-PHY

CAN-PHY

V-BAT SENSE

V-SUP SENSE

HVI (12V-input with ADC)

LS-drivers

HS-drivers

Charge Pump

4-6ch MOSFET Predriver (50-100nC)

Digital Components

MS-CAN

SCI

SPI

IIC

GPIO

PGPIO 20mA

NGPIO 25mA

BDM/BDC

Key Wakeups

Win Wdog

RTC

Timer
16Bit
(25-64MHz)

PWM
8/16Bit
(25-50MHz)

Motorcontrol PWM With Fault protection

Programmable Trigger Unit

Sound Generator

Segment LCD (4x40)

Stepper Motor Driver with SSD

MCU Core and Memories

S12- or S12Z-CPU
25/32/50MHz bus

Flash (ECC)
8kB – 128kB

EEPROM (ECC)
128B – 4kB

RAM (ECC)
512B - 8kB

5V Analogue Components

ADC
10-12Bit resolution
1-2 S/H-units
Up to 16ch total

Temp Sense

Current Sense
(2 x Op-Amp)

Pierce Osc.

RCosc. +/-1.3%

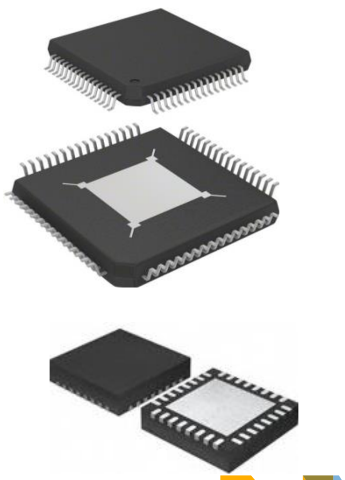
PLL

Packaging

LQFP:
32/48/64/100/144-pin

LQFP-EP:
48/64-pin

QFN:
32-pin (5x5mm)



Peripheral Introduction – CPMU

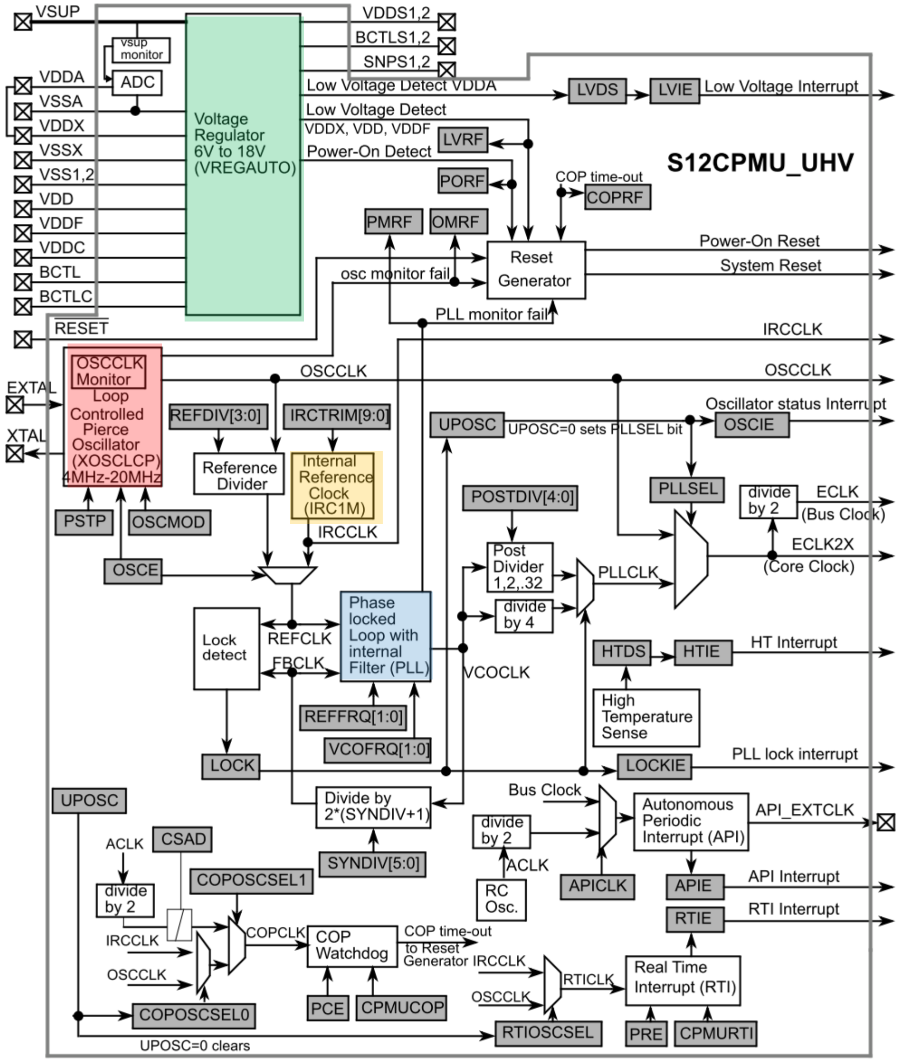


Figure 8-1. Block diagram of S12CPMU_UHV_V10_V6

🟥 XOSCLCP	🟩 VREGAUTO	🟦 PLL	🟨 IRC1M

- The Pierce oscillator (XOSCLCP) provides a robust, low-noise and low-power external clock source. It is designed for optimal start-up margin with typical crystal oscillators

- The Voltage regulator (VREGAUTO) operates from the range 6V to 18V. It provides all the required chip internal voltages and voltage monitors

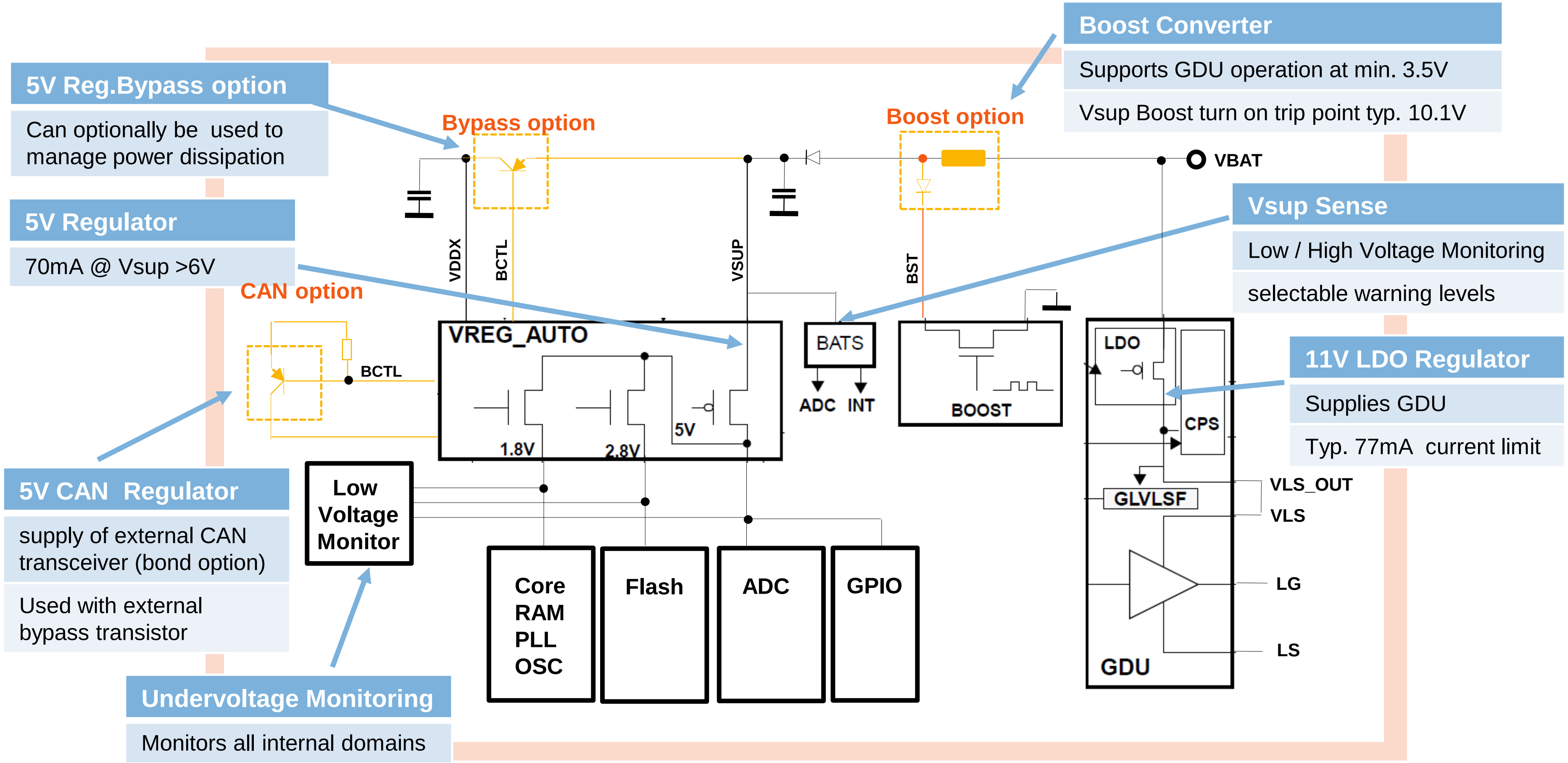
- The Phase Locked Loop (PLL) provides a highly accurate frequency multiplier with internal filter

- The Internal Reference Clock (IRC1M) provides a 1MHz internal clock.

Peripheral Introduction – Power Domain

S12ZVM for example

Flexible Boost & Bypass Option



5V Reg.Bypass option

Can optionally be used to manage power dissipation

5V Regulator

70mA @ Vsup >6V

5V CAN Regulator

supply of external CAN transceiver (bond option)

Used with external bypass transistor

Undervoltage Monitoring

Monitors all internal domains

Boost Converter

Supports GDU operation at min. 3.5V

Vsup Boost turn on trip point typ. 10.1V

Vsup Sense

Low / High Voltage Monitoring

selectable warning levels

11V LDO Regulator

Supplies GDU

Typ. 77mA current limit

Peripheral Introduction – Power Domain

S12ZVM for example

Boost Converter

Can optional ly be enabled

Vsup Boost turn on trip point typ. 10.1V

5V Regulator

70mA @ Vsup >6V

1.8V Core Regulator

Follows 5V regulator

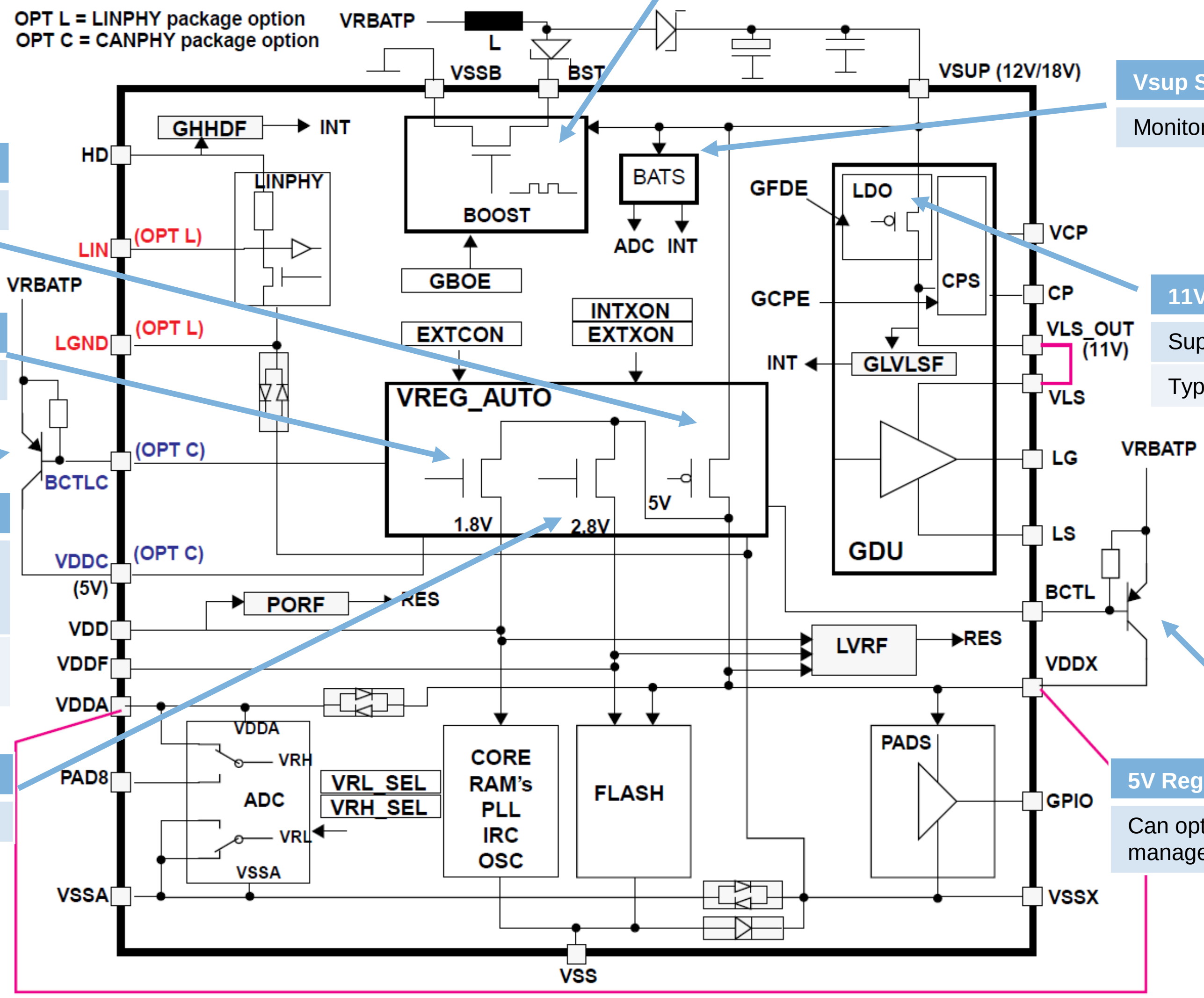
5V CAN Regulator

For supply of external CAN Transceiver (bond option with LIN/LGND pins)

Used with external bypass transistor

2.8V Flash Regulator

Follows 5V regulator



Vsup Sense

Monitors Vsup

11V LDO Regulator

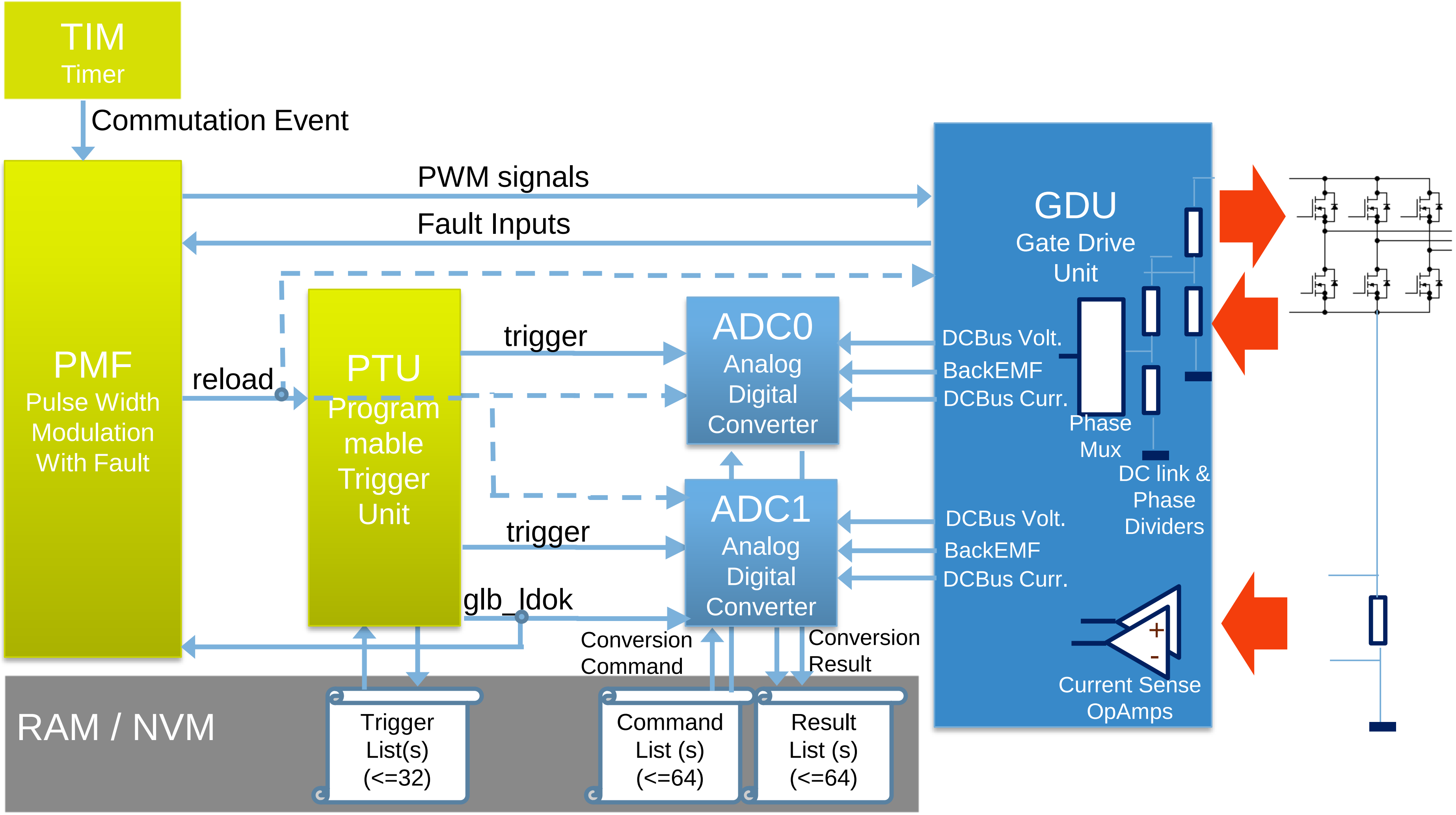
Supplies GDU

Typ. 77mA current limit

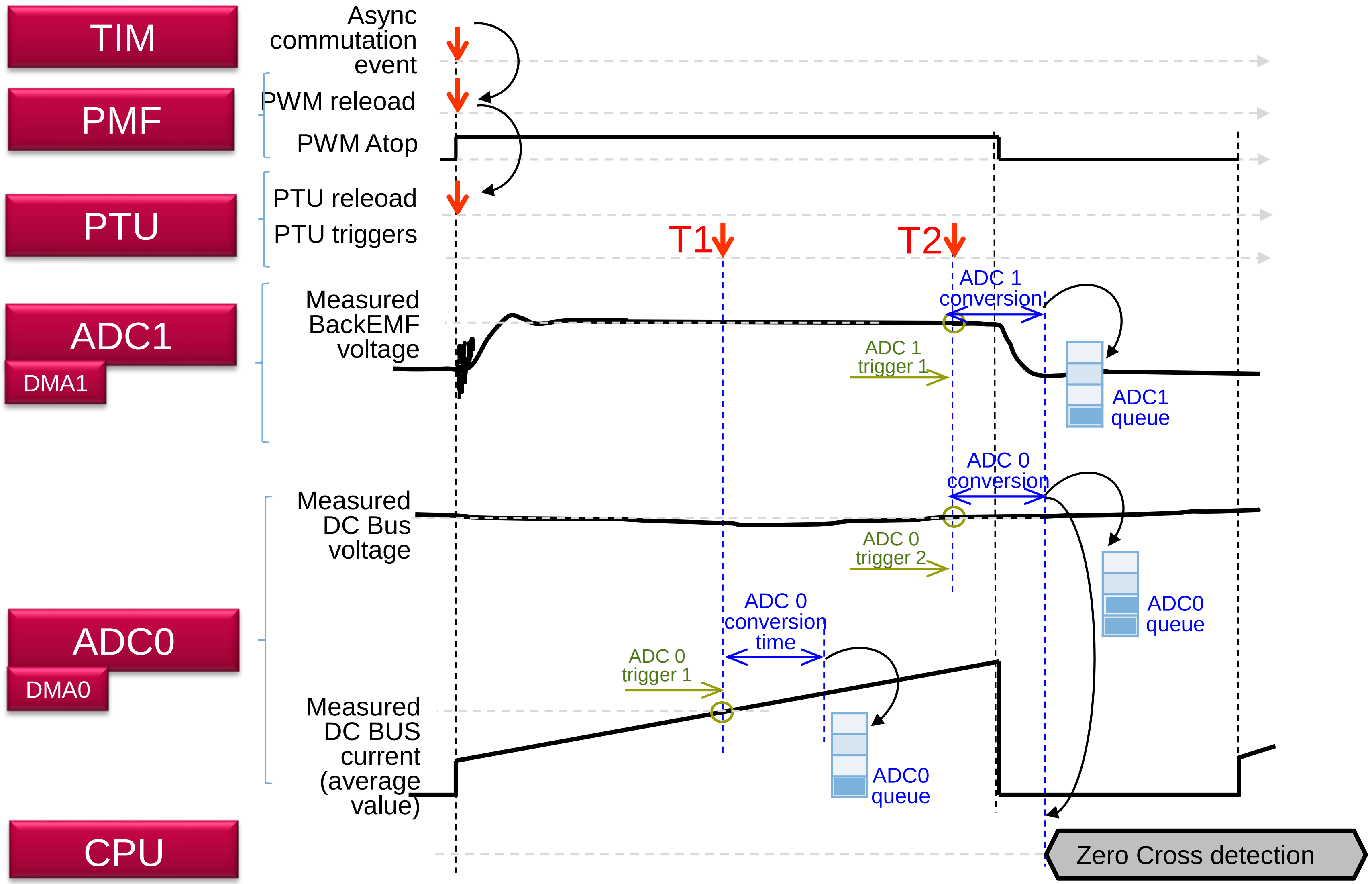
5V Reg.Bypass option

Can optional ly be used to manage power dissipation

Motor Control Loop Implementation

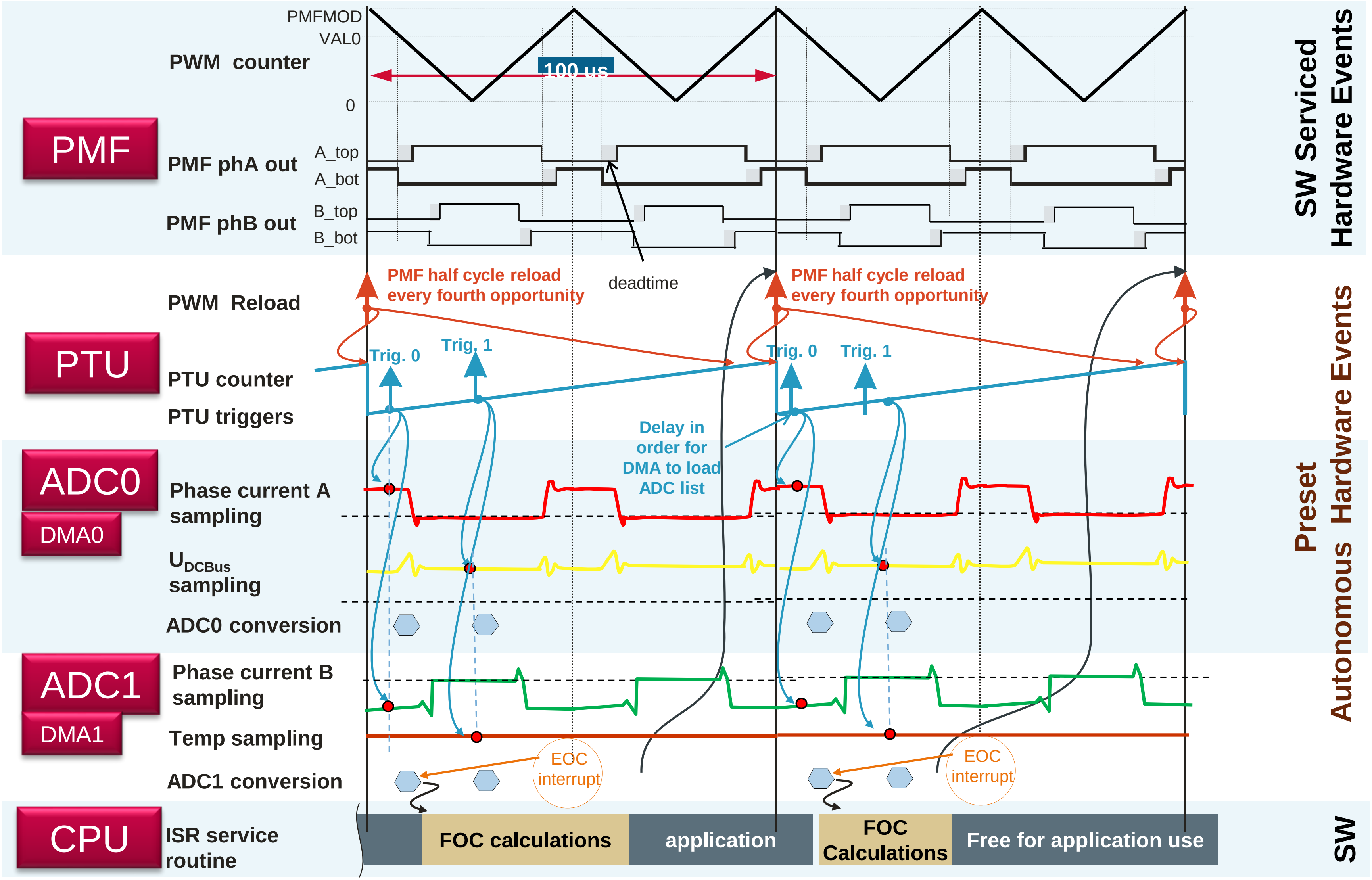


Fully automatic control loop



Autonomous PMSM Application Timing

Two shunts current sensing

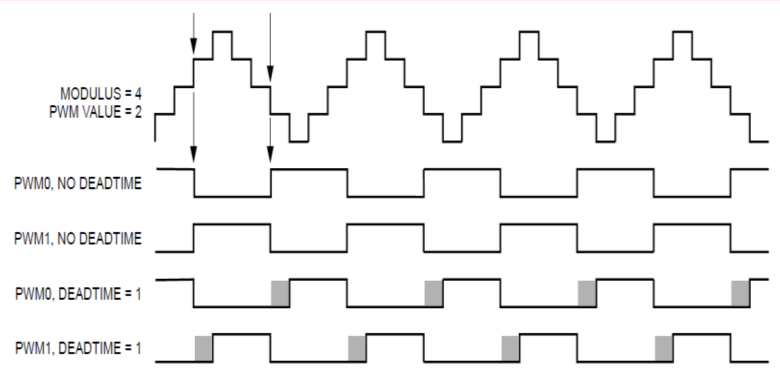


Pulse Width Modulator Module (PMF)

- **6 PWM channels, 3 independent counters**
  - Up to 6 independent channels or 3 complementary pairs
- **Based on core clock (max. 100MHz)**
- **Complementary operation:**
  - Dead time insertion
  - Top and Bottom pulse width correction
  - Double switching
  - Separate top and bottom polarity control
- **Edge- or center-aligned PWM signals**
- **Integral reload rates from 1 to 16**
- **6-step BLDC commutation support, with optional link to TIM Output Compare**
- **Individual software-controlled PWM outputs**
- **Programmable fault protection**

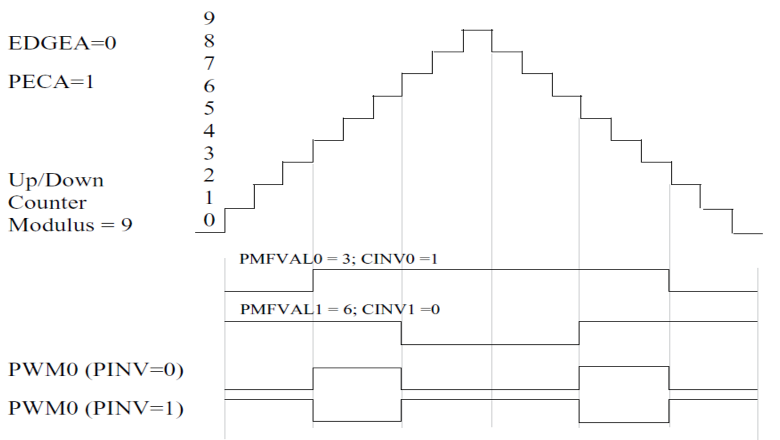
Complementary Mode

with / without dead time insertion



Double-Switching Mode

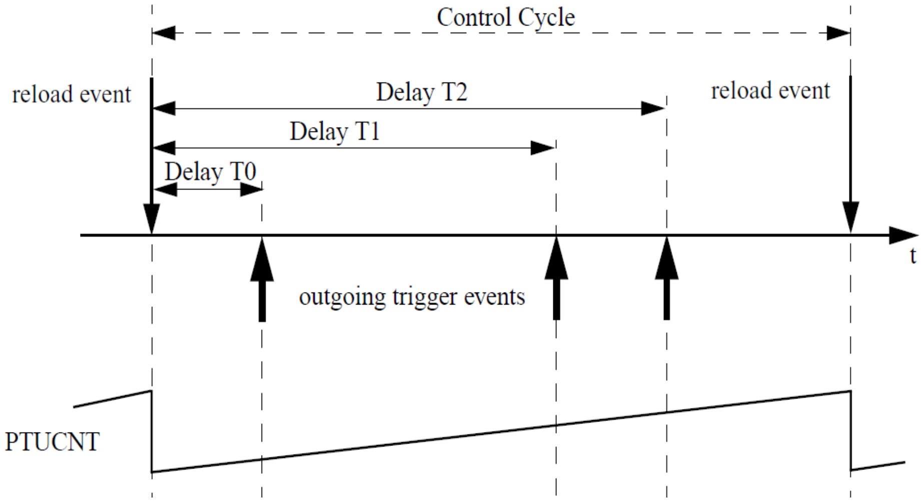
for single shunt system

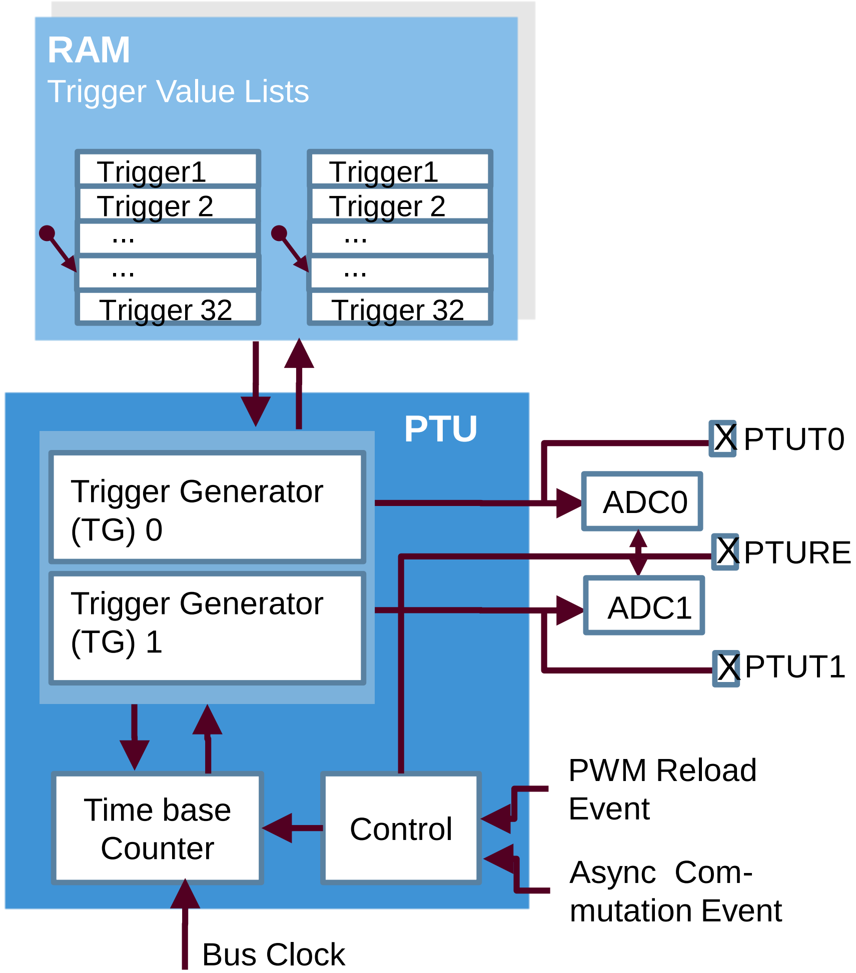


Programmable Trigger Unit (PTU)

Completely avoids CPU involvement to trigger ADC during the control cycle

- One 16-bit counter as time base
- Two independent trigger generators (TG)
- Up to 32 trigger events per trigger generator
- Trigger Value List stored in system memory
- Double buffered list, so that CPU can load new values in the background
- Software generated “Reload” & trigger event
- synchronized with PMF and ADC to guarantee coherent update of all control loop modules





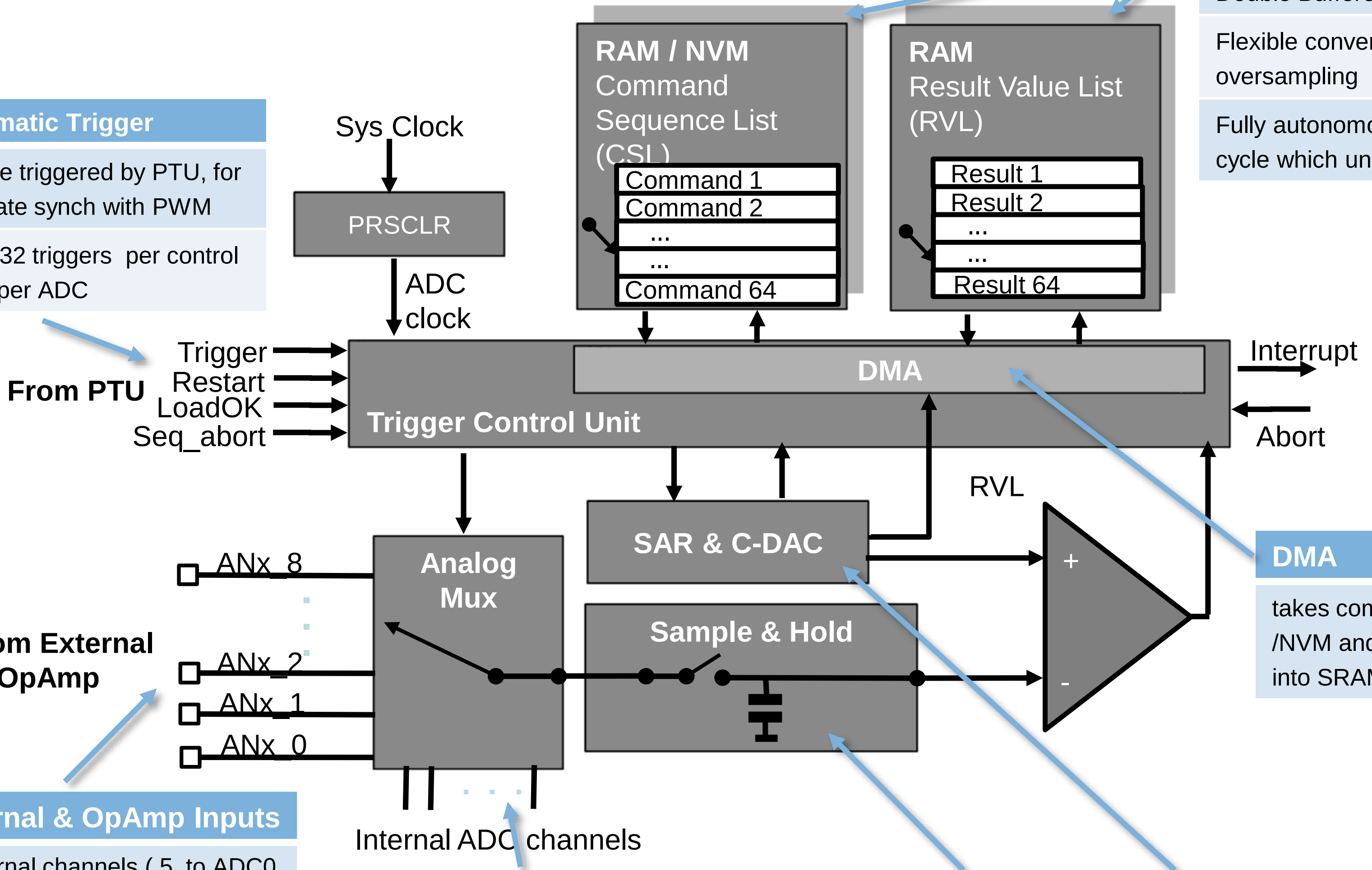
Peripheral Introduction – ADC

Automatic Trigger

- Can be triggered by PTU, for accurate synch with PWM
- Up to 32 triggers per control cycle per ADC

Command and Result List

- Double Buffered
- Flexible conversion sequence and oversampling
- Fully autonomous motor control cycle which unloads CPU



DMA

- takes commands from SRAM /NVM and stores results back into SRAM

External & OpAmp Inputs

- 9 external channels (5 to ADC0 and 4 to ADC1)
- OpAmp Output shared with ADC external channel

Monitoring Internal Signals

- DC Link, Phaase voltages, Vsup
- Vreg & ADC Temp sensors
- Bandgap voltage

Sample Time

- Selectable : 480ns to 2.88µs

Conversion Time

- 1.8µs @ max. ADC clock for 12bit

Peripheral Introduction – ADC – Internal Channels

Internal Channels give access to following internal signals

ADC0

Channel Select						ADC Channel	Signal
0	0	1	0	0	0	Internal_0	ADC0 temperature sensor
0	0	1	0	0	1	Internal_1	VREG temperature sensor or Bandgap voltage
0	0	1	0	1	0	Internal_2	GDU phase multiplexer voltage
0	0	1	0	1	1	Internal_3	GDU DC link voltage monitor
0	0	1	1	0	0	Internal_4	BATS VSUP sense voltage

ADC1

Channel Select						ADC Channel	Signal
0	0	1	0	0	0	Internal_0	ADC1 temperature sensor
0	0	1	0	0	1	Internal_1	VREG temperature sensor or Bandgap voltage
0	0	1	0	1	0	Internal_2	GDU phase multiplexer voltage
0	0	1	0	1	1	Internal_3	GDU DC link voltage monitor

Peripheral Introduction – ADC – Conversion Modes

- Single channel conversion
- Multi channel conversion
  - Sequentially convert flexible selectable order of channels
- Continuous conversion on a single channel
- Continuous conversion on multiple channels
- Oversampling of a single channel
- Oversampling of multiple channel
  - Order and channel selection flexible

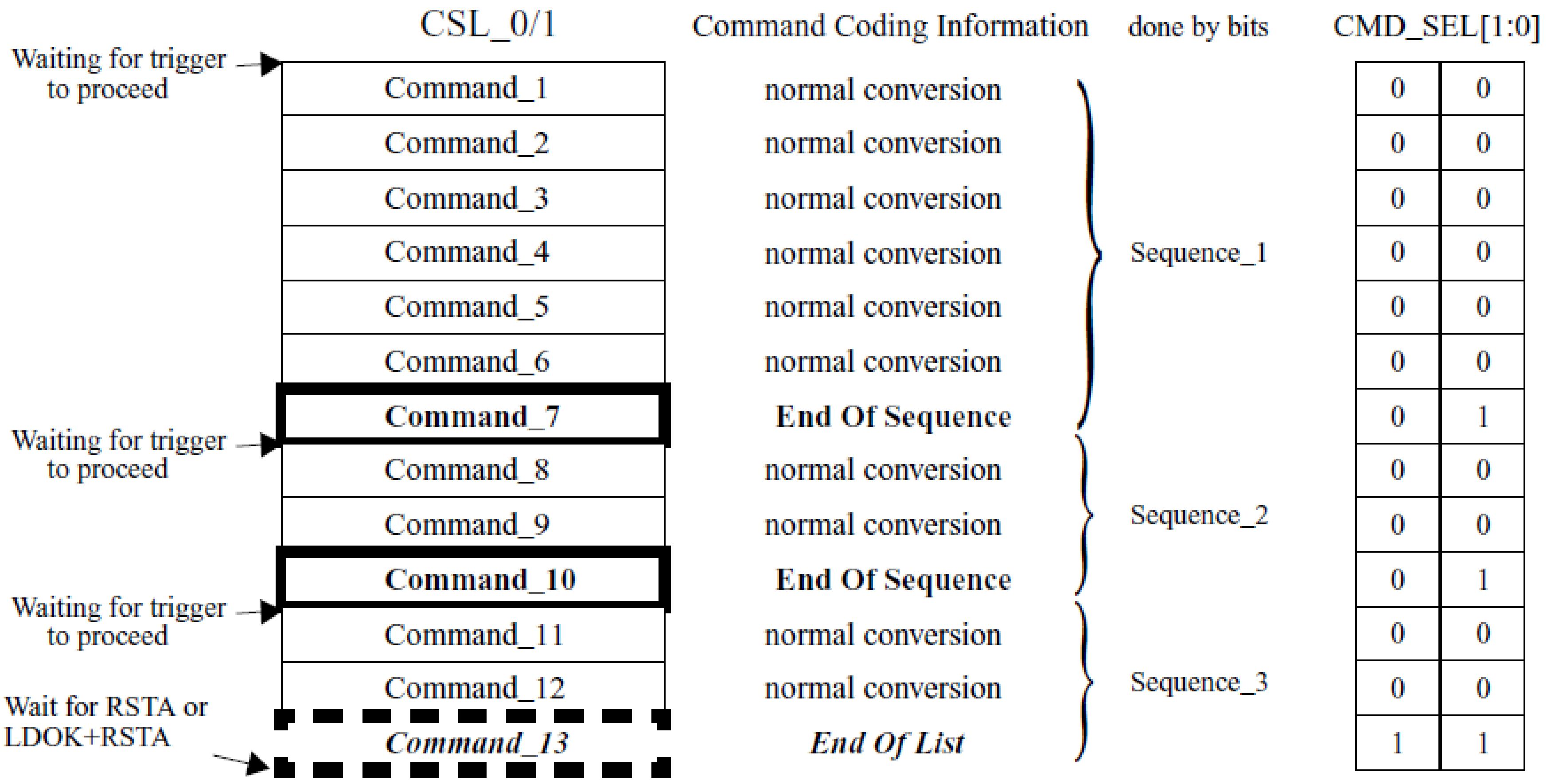
Trigger Mode

Restart event starts 1st conversion
Restart Event **IS** a trigger event

Restart Mode

Fully time controlled conversion
Restart Event **IS NOT** a trigger event

Peripheral Introduction – ADC – Command Sequence List



	CSL_0/1	Command Coding Information	done by bits	CMD_SEL[1:0]	
Waiting for trigger to proceed	Command_1	normal conversion	Sequence_1	0	0
	Command_2	normal conversion		0	0
	Command_3	normal conversion		0	0
	Command_4	normal conversion		0	0
	Command_5	normal conversion		0	0
	Command_6	normal conversion		0	0
	Command_7	**End Of Sequence**		0	1
Waiting for trigger to proceed	Command_8	normal conversion	Sequence_2	0	0
	Command_9	normal conversion		0	0
	Command_10	**End Of Sequence**		0	1
Waiting for trigger to proceed	Command_11	normal conversion	Sequence_3	0	0
	Command_12	normal conversion		0	0
Wait for RSTA or LDOK+RSTA	***Command_13***	***End Of List***		1	1

Peripheral Introduction – ADC – ADC Conversion Command

Conversion Command Type:

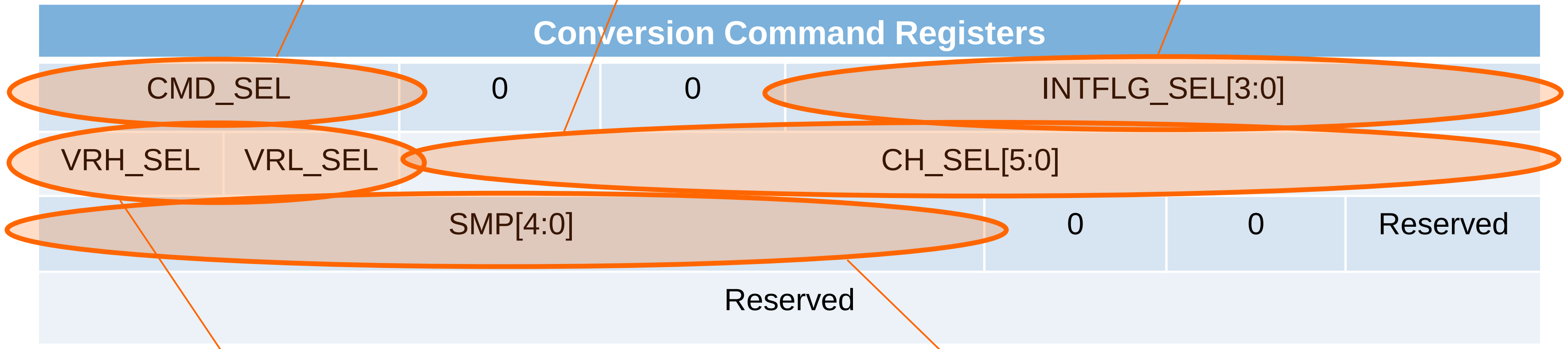
- Normal conversion
- End of sequence
- End of List

Conversion Interrupt Flag Select:

- which Int Flag gets set at end of conversion

Conversion Input Channel Select:

- Select input channel for this conversion



<table>
<tr><th colspan="8">Conversion Command Registers</th></tr>
<tr><td colspan="2">CMD_SEL</td><td>0</td><td>0</td><td colspan="4">INTFLG_SEL[3:0]</td></tr>
<tr><td>VRH_SEL</td><td>VRL_SEL</td><td colspan="6">CH_SEL[5:0]</td></tr>
<tr><td colspan="5">SMP[4:0]</td><td>0</td><td>0</td><td>Reserved</td></tr>
<tr><td colspan="8">Reserved</td></tr>
</table>

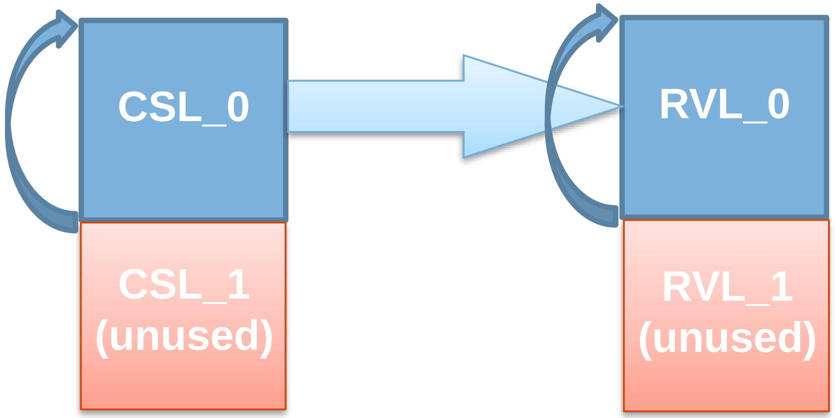
Select Reference High / Low:

- VRH_SEL = 0 = VRH_0 Selected = PAD8 (default)
  VRH_SEL = 1 = VRH_1 Selected = VDDA
- VRL_SEL = 0 = VRL_0 Selected = VSSA
  VRH_SEL = 1 = VRL_1 Selected = VSSA
  VRL_1 recommended (low noise) = non-default

Sample Time Length:

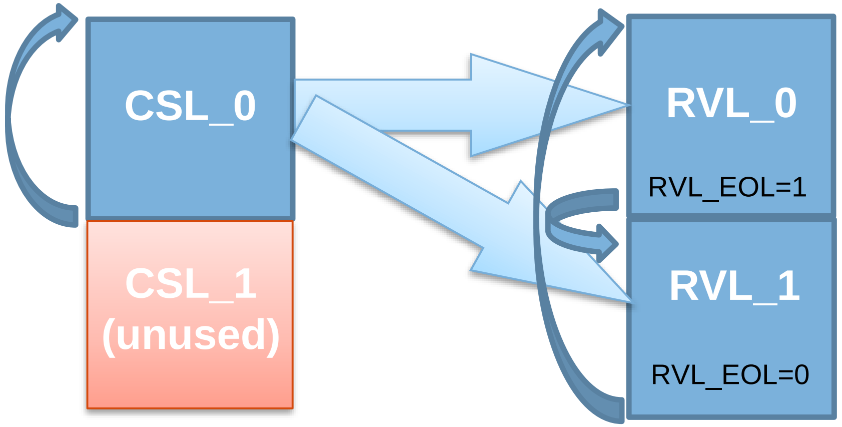
- Select Sample Time in units of ADC clock cycles
- 4 to 24 ADC clock cycles selectable
  → fastest = 480ns @ 8.33MHz (up to 150°C Tj)
  @ 50MHz bus
  → fastest = 640ns @ 6.25MHz (up to 175°C Tj)
  @ 50MHz bus

ADC – Command Sequence List & Result Value List



CSL single buffer mode - RVL single buffer mode

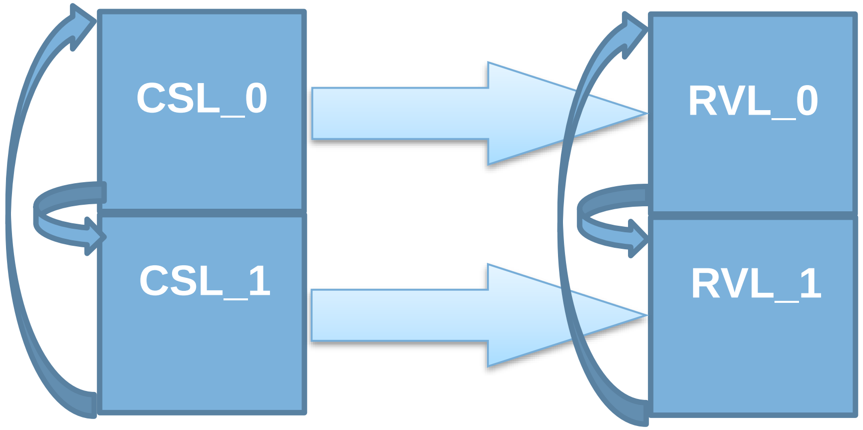
- default setting after reset
- after last command in list with type identifier End of list“ CSL and RVL index counters



CSL single buffer mode - RVL double buffer mode

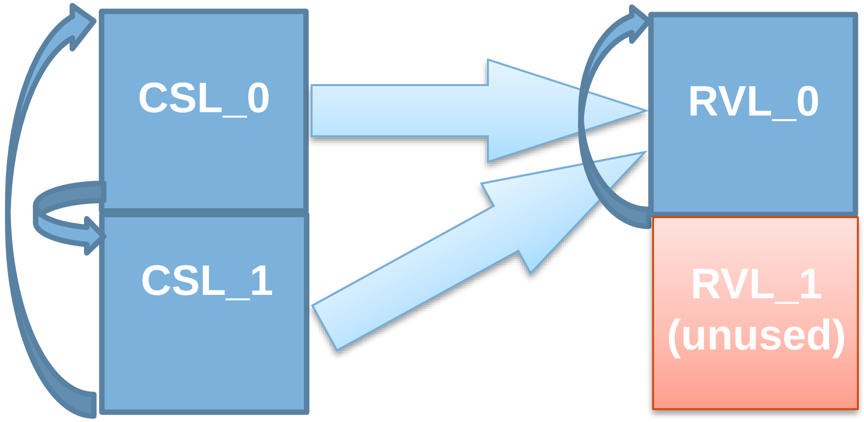
- increases latency time for CPU to read RVL buffers
- after last command in CSL or after CSL abort the RVL is switched
- first command result of new CSL cycle gets stored in new RVL
- RVL_EOL bit in ADCEOLRI register shows the last active RVL when “End Of List” command type was executed

ADC – Command Sequence List & Result Value List usage



CSL double buffer mode - RVL double buffer mode

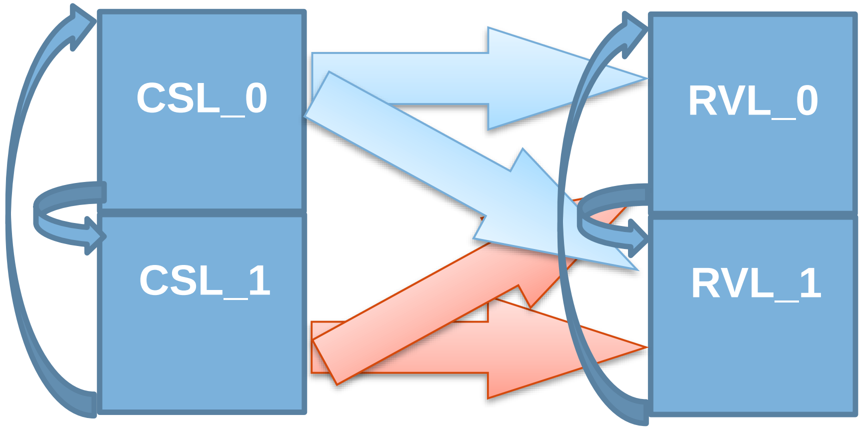
- can be used if the channel order or CSL length varies very frequently in an application.
- CSL and RVL switch after CSL end of list command reached and after assertion of LDOK+RSTA



CSL double buffer mode - RVL single buffer mode

- can be used if the channel order or CSL length varies very frequently in an application with different result SW handling
- CSL switchs after CSL end of list command reached and after assertion of LDOK+RSTA, while RVL index gets cleared

ADC – Command Sequence List & Result Value List usage



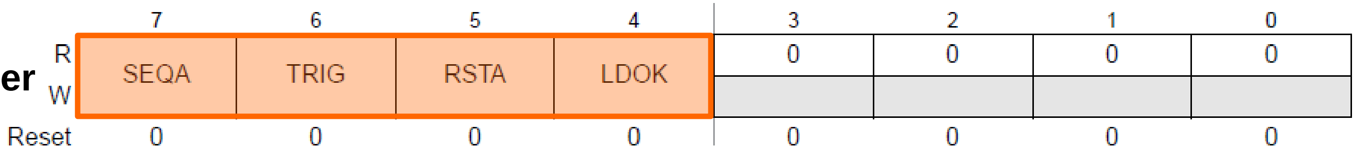
CSL double buffer mode - RVL double buffer mode

- at the end of a CSL end of list command the CSL is not always swapped (bit LDOK not always set with bit RSTA).
- The Result Value List is swapped whenever a CSL is finished or a CSL got aborted.

ADC – Conversion Flow Control

- The conversion flow is controlled by signals which are reflected in the ADC Conversion Flow Control Register ADCFLWCTL :
  - SEQA (Seq_Abort), TRIG(Trigger), RSTA(Restart), LDOK(LoadOK)

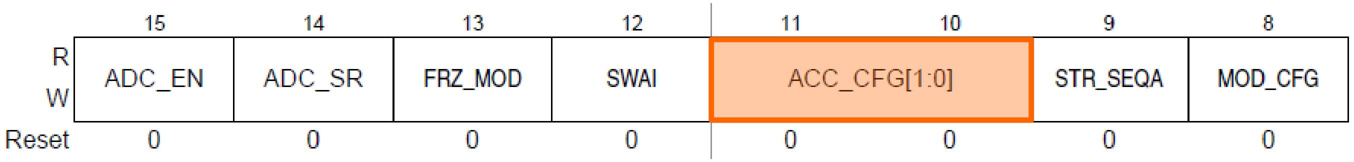
ADCFLWCTL Register



	7	6	5	4	3	2	1	0
R	SEQA	TRIG	RSTA	LDOK	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

- They can be modified in two different ways:
  - Via Data-Bus accesses
  - Via Internal Interface Signals (Trigger, Restart, LoadOK and Seq_Abort)
  - This is selected by ACC_CFG bits in ADCCTRL0 Register

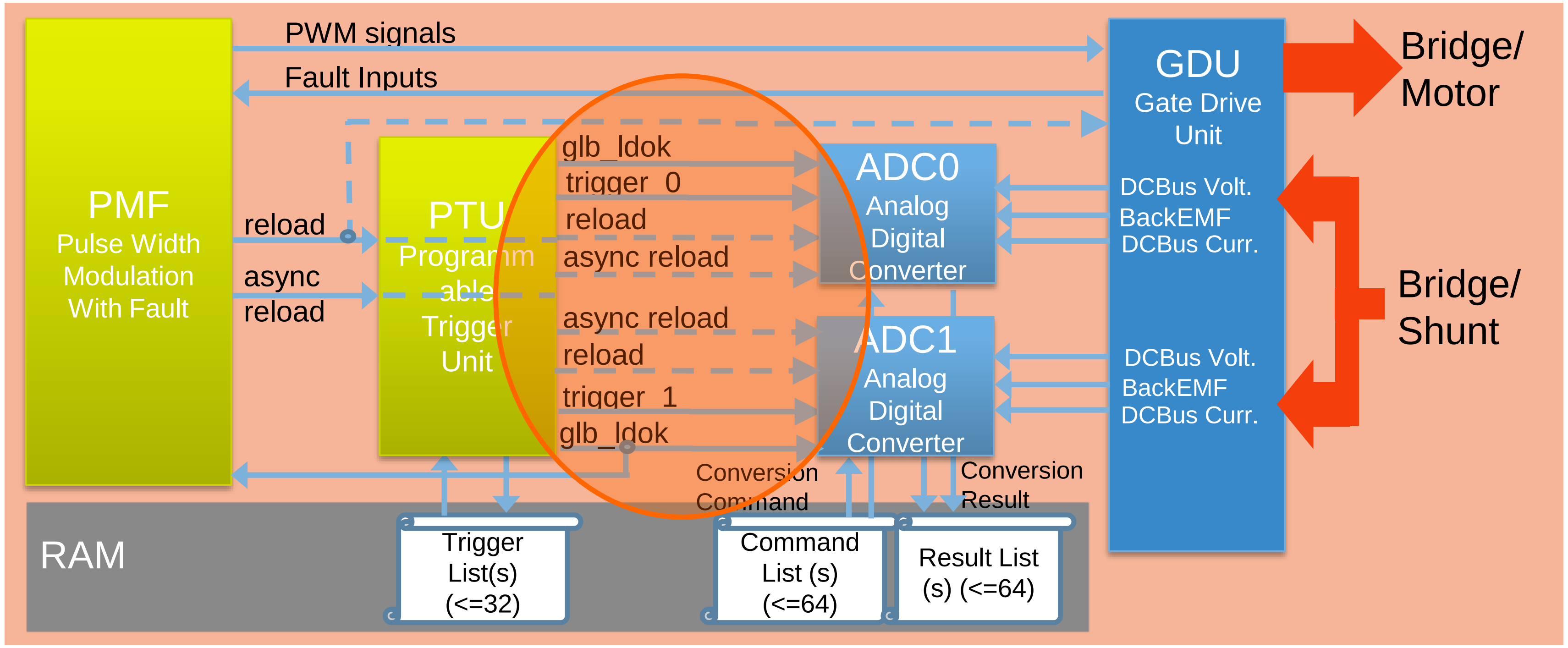
ADCCTL_0 Register

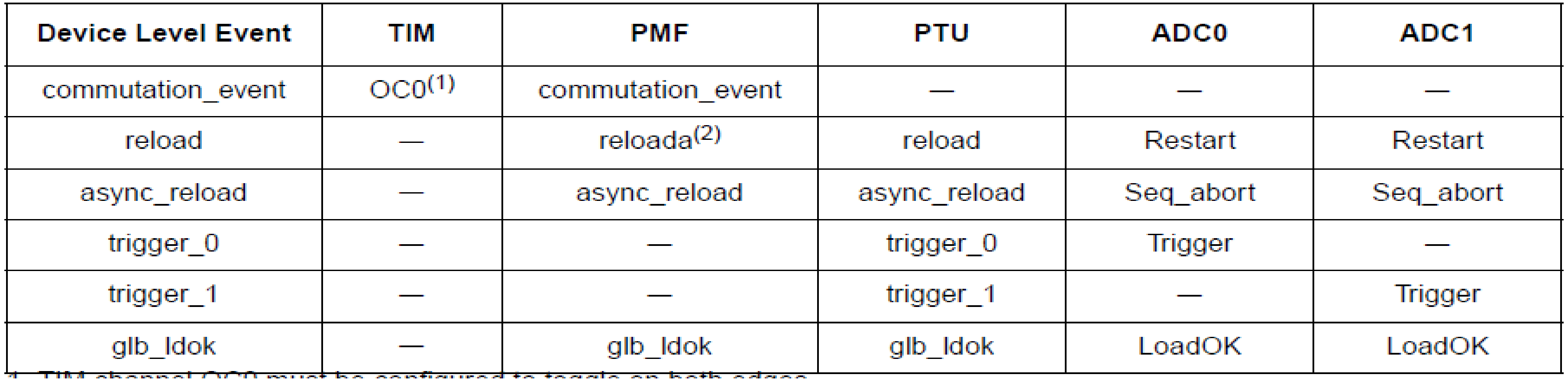


	15	14	13	12	11	10	9	8
R	ADC_EN	ADC_SR	FRZ_MOD	SWAI	ACC_CFG[1:0]		STR_SEQA	MOD_CFG
W								
Reset	0	0	0	0	0	0	0	0

ACC_CFG [1]	ACC_CFG [0]	Access Mode
0	0	No access path enabled
0	1	Single Access via Internal Interface
1	0	Single Access via Data Bus
1	1	Dual Access mode

ADC – Internal Conversion Flow Signals



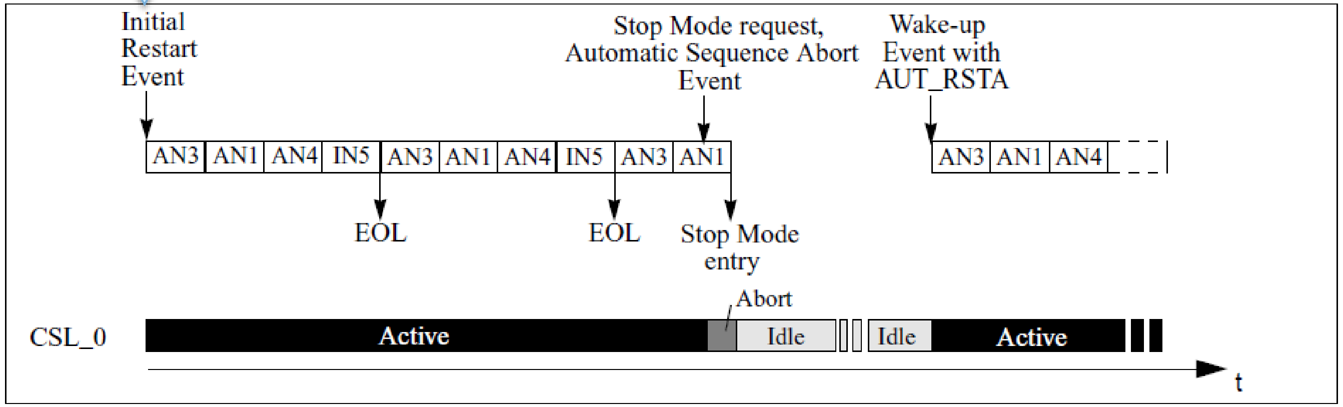


Device Level Event	TIM	PMF	PTU	ADC0	ADC1
commutation_event	OC0[1]	commutation_event	—	—	—
reload	—	reloada[2]	reload	Restart	Restart
async_reload	—	async_reload	async_reload	Seq_abort	Seq_abort
trigger_0	—	—	trigger_0	Trigger	—
trigger_1	—	—	trigger_1	—	Trigger
glb_ldok	—	glb_ldok	glb_ldok	LoadOK	LoadOK

1. TIM channel OC0 must be configured to toggle on both edges

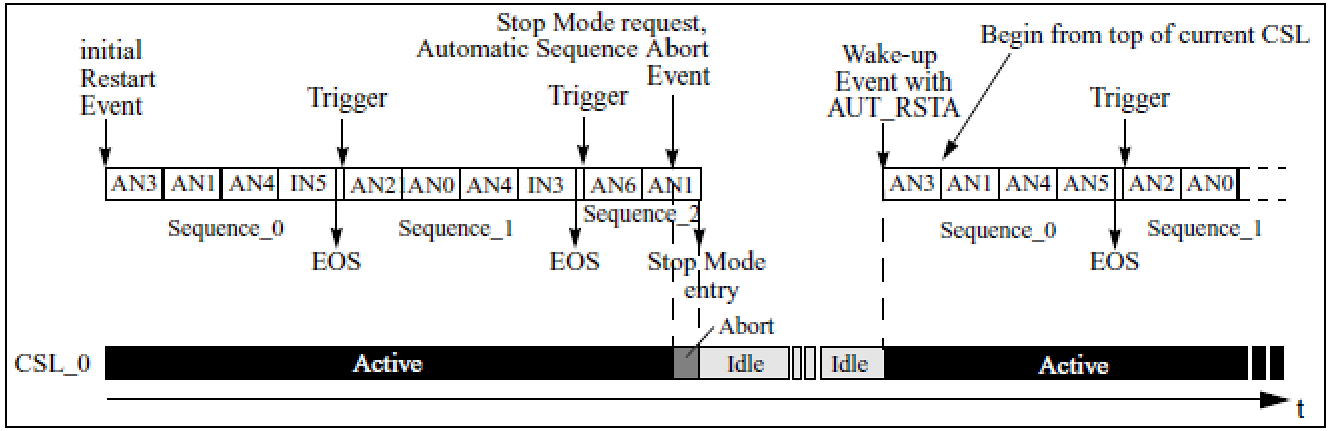
ADC – Conversion Flow Trigger Mode

Restart Event = Trigger for first coverstion sequence



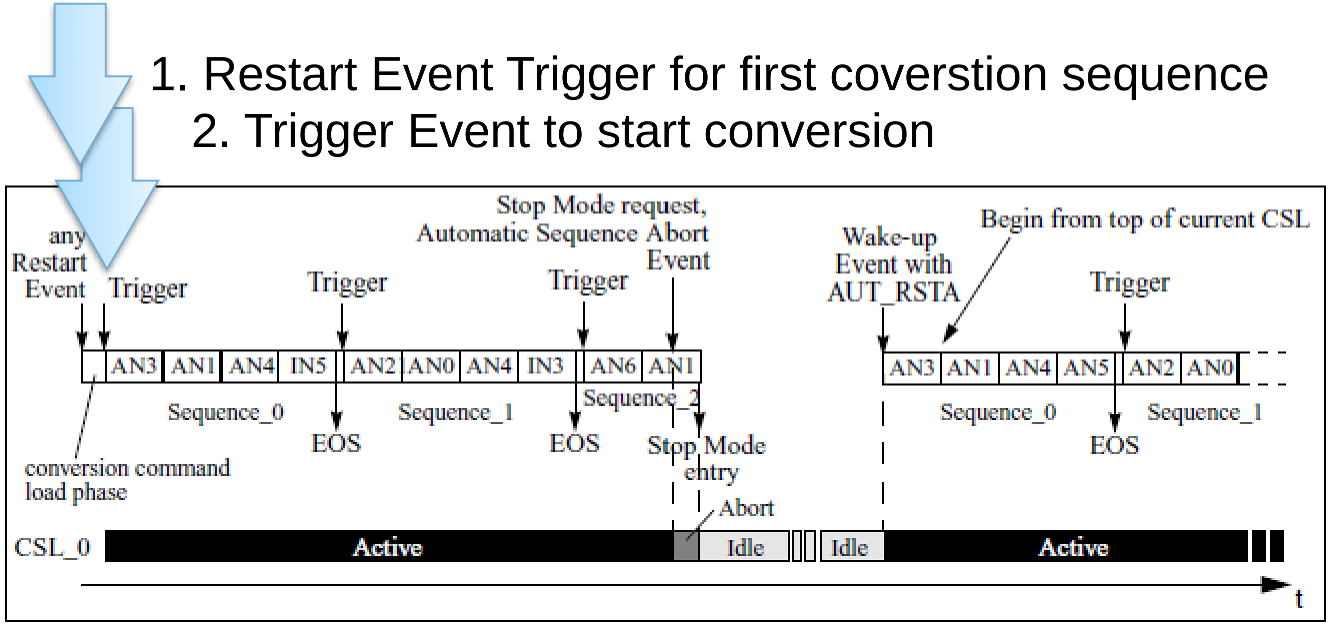
Example 1:
Trigger Mode used for simple continuous conversion in single buffer mode

Restart Event = Trigger for first coverstion sequence



Example 2:
Trigger Mode used for periodic and timed conversion of different groups of channels in single buffer mode

ADC – Conversion Flow Restart Mode



1. Restart Event Trigger for first coverstion sequence
2. Trigger Event to start conversion

Example :
Restart Mode used for periodic and fully timed conversion (incl. Start) of different groups of channels in single buffer mode

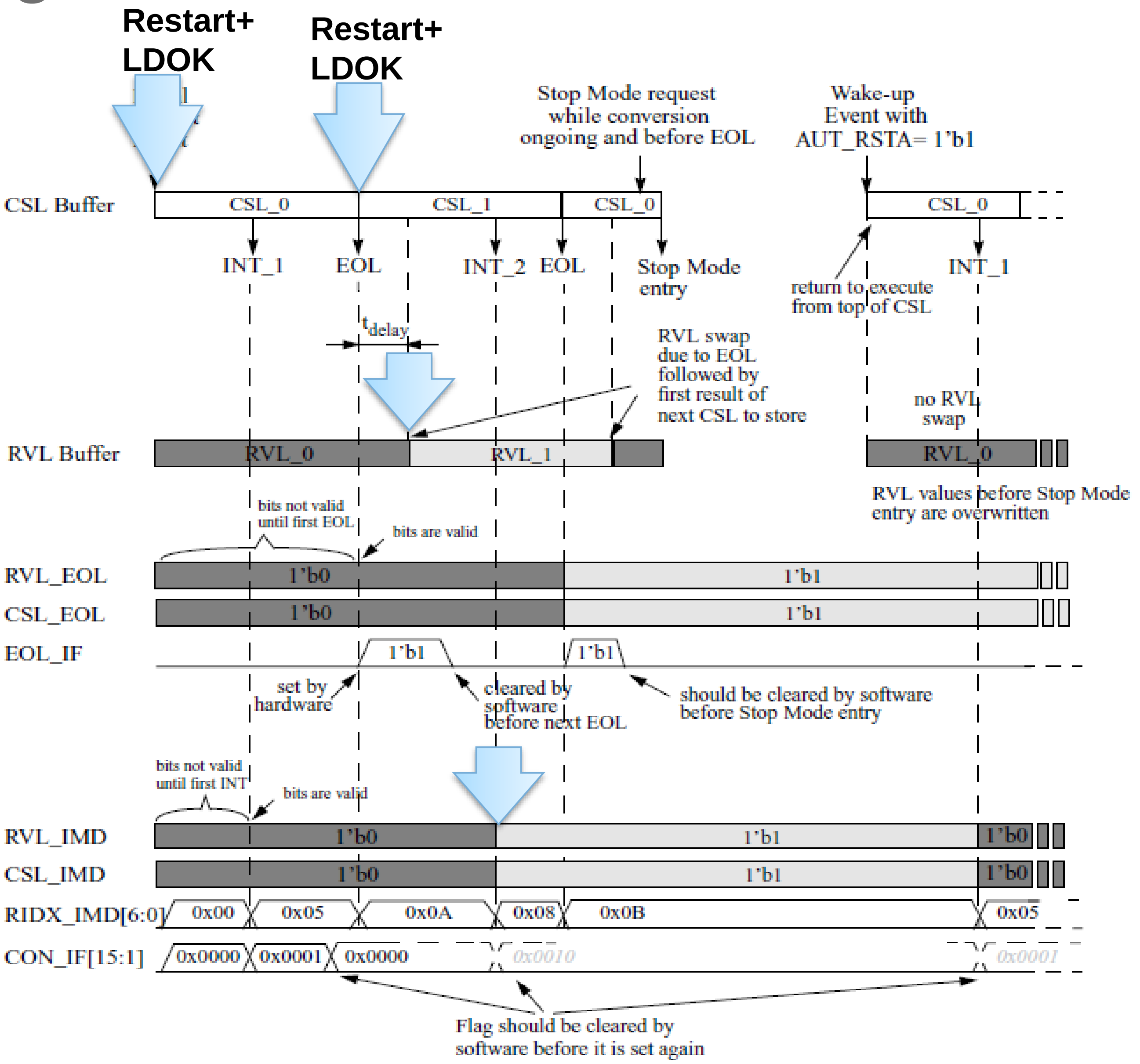
ADC – Buffer Swapping

Swap of CSL:

Requested by

- Positive edge of Internal Interface signal Restart after or simultaneously with positive edge of Internal Interface signal LoadOK

-Write Access via Data Bus to set control bit RSTA simultaneously with bit LDOK;



Restart+ LDOK
Restart+ LDOK
Stop Mode request while conversion ongoing and before EOL
Wake-up Event with AUT_RSTA= 1'b1
CSL Buffer
CSL_0
CSL_1
CSL_0
CSL_0
INT_1
EOL
INT_2
EOL
Stop Mode entry
return to execute from top of CSL
INT_1
t_delay
RVL swap due to EOL followed by first result of next CSL to store
no RVL swap
RVL Buffer
RVL_0
RVL_1
RVL_0
RVL values before Stop Mode entry are overwritten
bits not valid until first EOL
bits are valid
RVL_EOL
1'b0
1'b1
CSL_EOL
1'b0
1'b1
EOL_IF
1'b1
1'b1
set by hardware
cleared by software before next EOL
should be cleared by software before Stop Mode entry
bits not valid until first INT
bits are valid
RVL_IMD
1'b0
1'b1
1'b0
CSL_IMD
1'b0
1'b1
1'b0
RIDX_IMD[6:0]
0x00
0x05
0x0A
0x08
0x0B
0x05
CON_IF[15:1]
0x0000
0x0001
0x0000
0x0010
0x0001
Flag should be cleared by software before it is set again

Swap of RVL:

Requested by

- EOL

- certain tdelay to be considered until swapping

- indicated indirectly by RVL_IMD after first INT_x

ADC – ADC Errors

- **Double bit ECC Error (DBECC_ERR):**
  - double bit ECC error occurred during conversion command load or result storage

  → ADC stops operation, ADC soft reset needed
- **Access Error (IA_EIF):**
  - During storing result illegal access error occured

  → ADC stops operation, check address definition of result buffers
- **Command Value Error (CMD_EIF):**
  - Invalid conversion command

  → ADC stops operation, check command memory
- **'End of List' Error (EOL_EIF):**
  - Command with EOL command type missing in CSL

  → ADC stops operation, check command memory
- **Trigger Error (TRIG_EIF):**
  - no Restart before trigger or trigger occurs while trigger processed or during a conversion

  → ADC stops operation

- **Restart Error (RESTAR_EIF):**

  Restart occurs after trigger and bevore EOL or abort

  →ADC continues operation
- **LDOK Error (LDOK_EIF):**

  Restart Mode: Restart occurred without Load OK

  →ADC continues operation
- **Conversion Interrupt Flag Overrun Error (CONIF_OIF):**

  Overrun occured for one of the CON_IFs

  → ADC continues operation

ADC – Example Code: ADC List initialisation

```
#pragma DATA_SEG adcLists
  volatile char ADC0CommandList[6][4] = {
  {0x40,0xD0,0x00,0x00},    // end of sequence + no int [40] , current sense channel,
  {0xC0,0xCB,0x00,0x00},   // end of list + no int [C0], VDDA voltage + HD voltage channel [CB], 4 clock
                               cycles sample time [00], reserved [00]
  {0x00,0x00,0x00,0x00},
  {0x00,0x00,0x00,0x00},
  {0x00,0x00,0x00,0x00},
  {0x00,0x00,0x00,0x00}
  };
  volatile char ADC1CommandList[6][4] = {
  {0xC0,0xCA,0x00,0x00},   // end of list + no int.[C0], VDDA voltage + phase voltage [CA], 4 clock
                               cycles sample time [00], reserved [00]
  {0x00,0x00,0x00,0x00},
  {0x00,0x00,0x00,0x00},
  {0x00,0x00,0x00,0x00},
  {0x00,0x00,0x00,0x00},
  {0x00,0x00,0x00,0x00}
  };

  volatile unsigned short ADC0ResultList[6] = {0, 0, 0, 0, 0, 0};
  volatile unsigned short ADC1ResultList[6] = {0, 0, 0, 0, 0, 0};
#pragma DATA_SEG DEFAULT
```

ADC – ADC initialisation

```
void initADC(void){

  /************* ADC0 ***********************
  ADC0CTL_0_ACC_CFG = 3;      // Dual access mode (via data bus & internal signals)
  ADC0CTL_0_STR_SEQA = 1;     // Store result at abort/restart
  //ADC0CTL_1 = 0;

  ADC0TIM = ADC_TIM;          // clock: clk = fbus / (2x(reg.value + 1)) [0.25 - 8MHz]

  ADC0FMT_DJM = 0;            // left justified result data
  ADC0FMT_SRES = 4;           // 12-bit result

  ADC0CONIE_1_EOL_IE = 1;     // End of list interrupt enable

  // ADC0 Command Base Pointer
  ADC0CBP_0 = (uint8_t)((((long)ADC0CommandList) >> 16) & 0x0000FF);
  ADC0CBP_1 = (uint8_t)((((long)ADC0CommandList) >> 8) & 0x0000FF);
  ADC0CBP_2 = (uint8_t)((long)ADC0CommandList & 0x0000FF);

  // ADC0 Result Base Pointer
  ADC0RBP_0 = (uint8_t)((((long)ADC0ResultList) >> 16) & 0x0000FF);
  ADC0RBP_1 = (uint8_t)((((long)ADC0ResultList) >> 8) & 0x0000FF);
  ADC0RBP_2 = (uint8_t)((long)ADC0ResultList & 0x0000FF);

…
```

ADC – ADC initialisation - 2

```
// ADC0 Command/Result Offset registers
ADC0CROFF1 = 0;

ADC0CTL_0_ADC_EN = 1;          // enable ADC0
ADC0EIE = 0xEE;                // enable all errors interrupts


/************ ADC1 ***********************
ADC1CTL_0_ACC_CFG = 3;         // Dual access mode
ADC1CTL_0_STR_SEQA = 1;        // Store result at abort/restart
//ADC1CTL_1 = 0;

ADC1TIM = ADC_TIM;             // clock: clk = fbus / (2x(reg.value + 1)) [0.25 - 8MHz]

ADC1FMT_DJM = 0;               // left justified result data
ADC1FMT_SRES = 4;              // 12-bit result

//ADC1CONIE_1_EOL_IE = 1;      // End of list interrupt enable - Used only for debugging

…
```

ADC – ADC initialisation - 2

```
  // ADC1 Command Base Pointer
  ADC1CBP_0 = (uint8_t)((((long)ADC1CommandList) >> 16) & 0x0000FF);
  ADC1CBP_1 = (uint8_t)((((long)ADC1CommandList) >> 8) & 0x0000FF);
  ADC1CBP_2 = (uint8_t)((long)ADC1CommandList & 0x0000FF);

  // ADC1 Result Base Pointer
  ADC1RBP_0 = (uint8_t)((((long)ADC1ResultList) >> 16) & 0x0000FF);
  ADC1RBP_1 = (uint8_t)((((long)ADC1ResultList) >> 8) & 0x0000FF);
  ADC1RBP_2 = (uint8_t)((long)ADC1ResultList & 0x0000FF);

  // ADC1 Command/Result Offset registers
  ADC1CROFF1 = 0;

  ADC1CTL_0_ADC_EN = 1;          // enable ADC1
  ADC1EIE = 0x08;                // Enable Trigger Error ISR only

}
```

ADC – ADC Error handling

```
interrupt void ADC0error_ISR(void)
{
char tmpAdcEIF;

  tmpAdcEIF = ADC0EIF;
  if (tmpAdcEIF & 0x02) {              // Load Ok Error
      AdcErrorLDOK++;
      ADC0EIF = 0x02;
  }
  if (tmpAdcEIF & 0x04) {              // Restart Request Error
      AdcErrorRSTAR++;
      ADC0EIF = 0x04;
  }
  if (tmpAdcEIF & 0x08) {              // Trigger Error => Soft Reset
      AdcErrorTRIG++;
      ADC0CTL_0_ADC_SR = 1;
  }
  if (tmpAdcEIF & 0x20) {              // End Of List Error => Soft Reset
      AdcErrorEOL++;
      ADC0CTL_0_ADC_SR = 1;
  }
  if (tmpAdcEIF & 0x40) {              // Command Value Error => Soft Reset
      AdcErrorCMD++;
      ADC0CTL_0_ADC_SR = 1;
  }
  if (tmpAdcEIF & 0x80) {              // Illegal Access Error => Soft Reset
      AdcErrorIA++;
      ADC0CTL_0_ADC_SR = 1;
  }
}
```

Peripheral Introduction – Gate Driver Unit (GDU) Topology

11V LDO

supplies the LS drivers

charges bootstrap cap for the HS drivers

Voltage Monitoring

HD High Voltage Monitor @ typ. 21/27.3 V

VLS Low Voltage trip point: 6.2 .. 7V

Integrated Dividers

HD: divider 12 ; HS : divider 6

Phase Comparators

Compares HS against DCbus/2 in HW

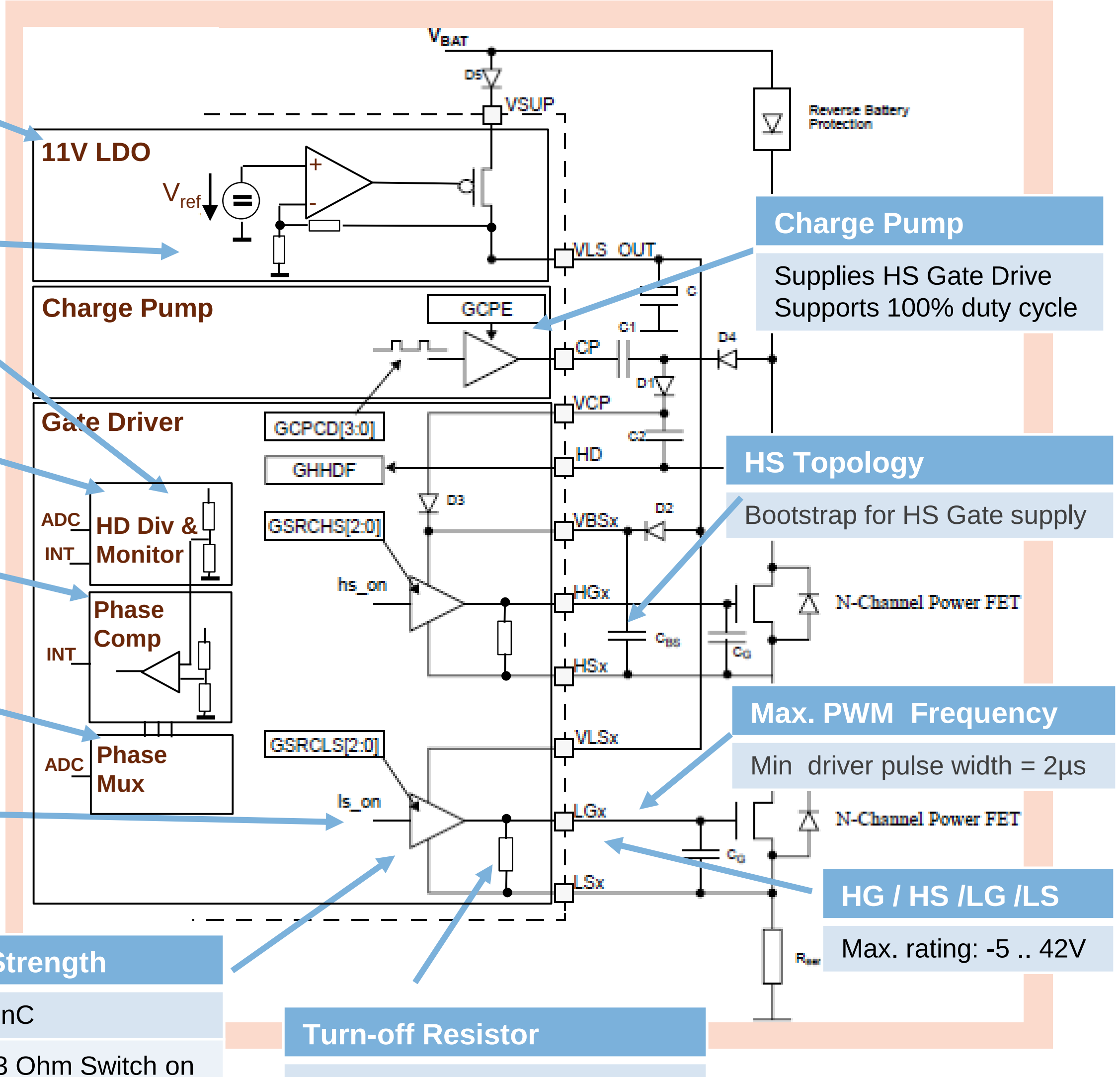
Phase Multiplexer

Switched in each sector

Slew Rate Control

Output current limitation of Iout via selectable Iref

8 selectable slew rates



Charge Pump

Supplies HS Gate Drive
Supports 100% duty cycle

HS Topology

Bootstrap for HS Gate supply

Max. PWM Frequency

Min driver pulse width = 2µs

HG / HS /LG /LS

Max. rating: -5 .. 42V

Drive Strength

Typ 100nC

Typ. 6.3 Ohm Switch on
Typ. 16 Ohm Switch off

Turn-off Resistor

80kOhm pull down integrated

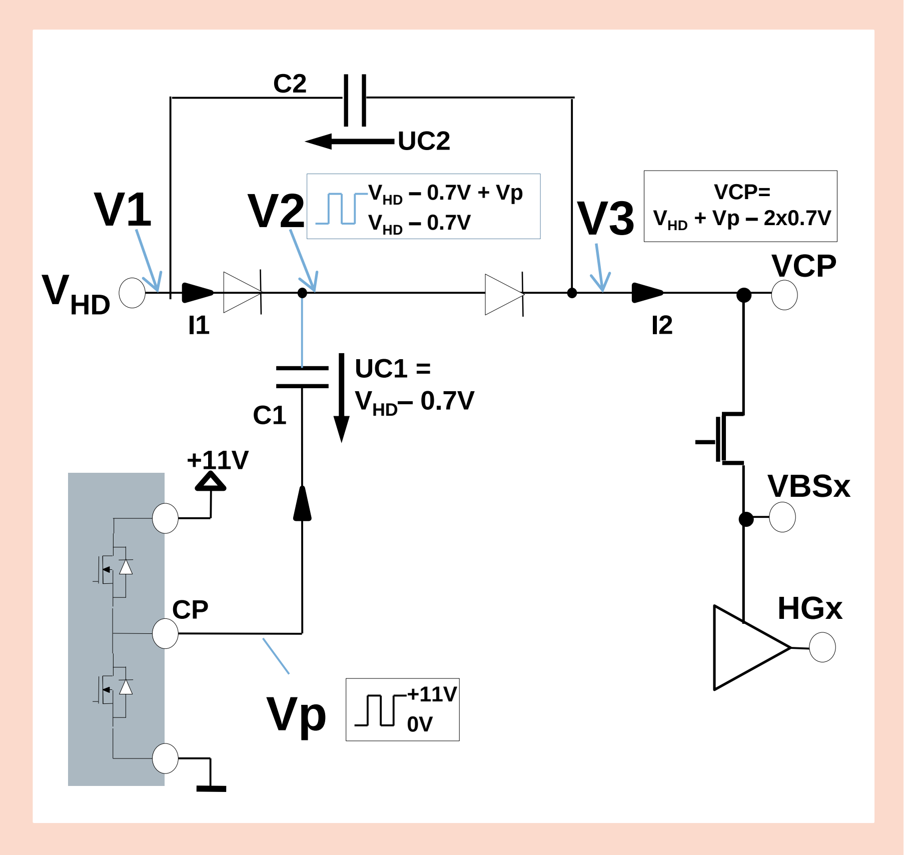
GDU – Charge pump basic characteristic

Charge pump states :

- Vp = 0
  - Load C1 to V_{HD} – 0.7V
- Vp = +11V
  - Load C2 with charge of C1
  - dUC2 = UC1 * C1/C2
  - UC2 = VHD– 2x0.7V

Characteristic Summary

- Charge pump adds fixed voltage on top of V1
  - Independent of the relation of V1 and Vp
  - If V1 = Vp it serves as a voltage doubler
- I1 = 2 x I2
- V3 ripple is minimum for C2 >> C1
  - reduces the feedthrough of V1 ripple on V3
- Lower plate of C2 should be connected to V_{HD}



V3 = V1 + Vp – 2 x 0.7V

GDU – Charge Pump Dimensioning

Component selection depends on

- selected charge pump frequency
- acceptable voltage ripple
- GDU current for the static HS Switch drive
- acceptable power dissipation (on charge pump diodes)

$$f >= \frac{I_{GDU}}{C_{pump} * V_{ripple}}$$

Example EVB board setup:

C1 = 10nF

C2 = 100nF

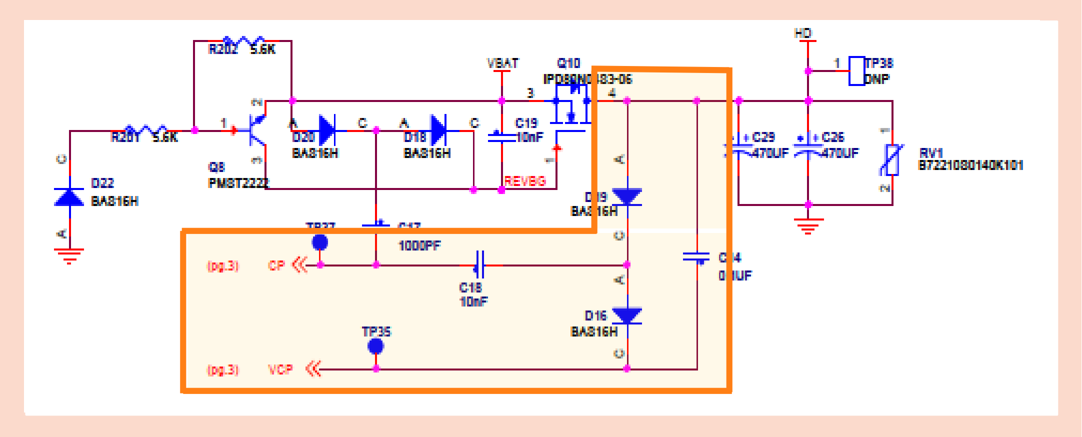
(connected to V_{HD})

f = 500kHz

I_{GDU} = 2mA

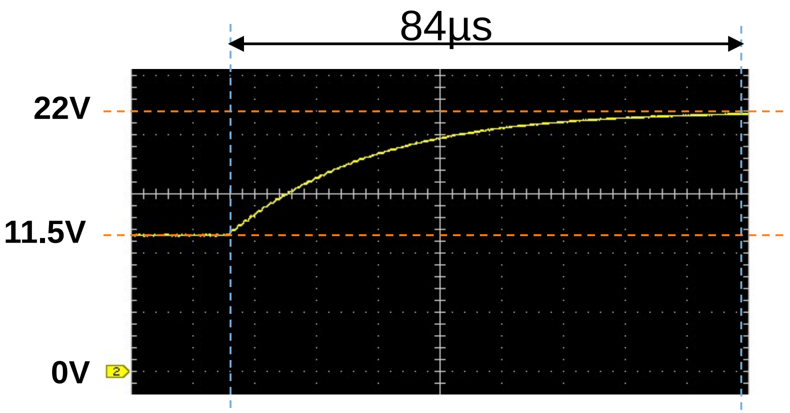
(assuming worst case of 3 HS to be switched at same time)

$$\rightarrow V_{ripple} = \frac{2mA}{10nF * 500kHz} = 40mV$$

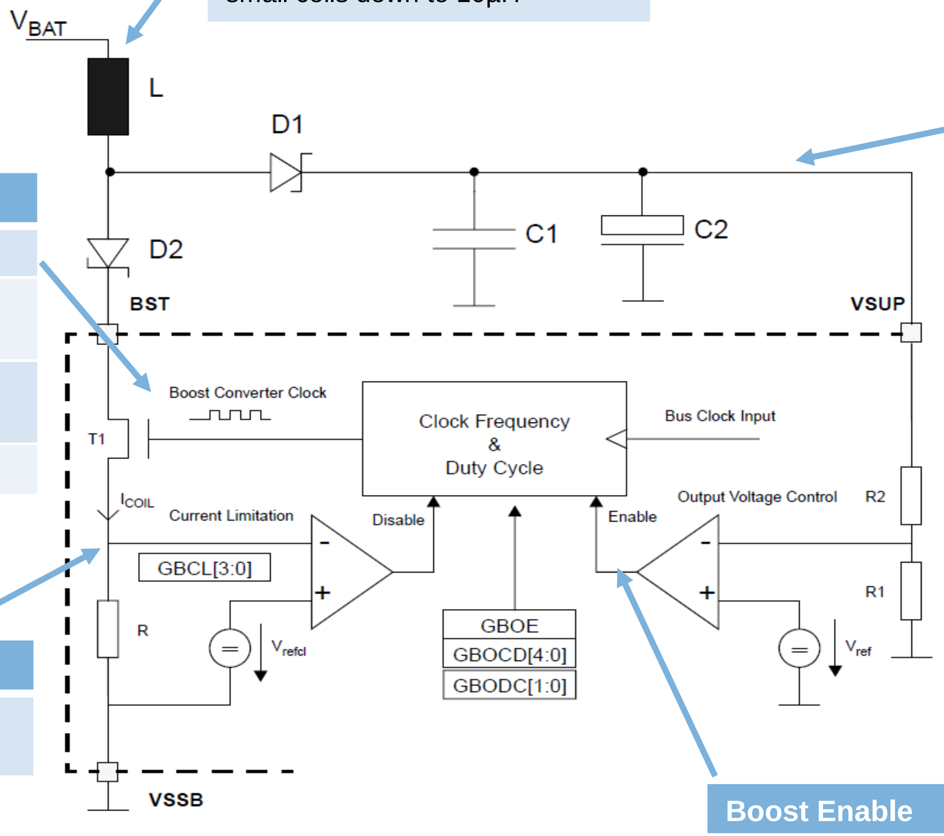


Charge Pump startup:

Measured smooth charge pump startup on VCP @ 1.56MHz



GDU – Boost Converter



Coil Size

High frequency option allows small coils down to 10µH

Step-up frequency /duty cycle

Wide range selectable

Optimizes dI/dt and power dissipation

Frequency range : 62.5kHz .. 12.5MHz @ 50MHz fbus

Duty cycle : 25%, 50% or 75%

Boost Function

Optional

guarantees a V_{GS} > 9V at low V_{BAT} conditions

Coil Current limitation

threshold selectable between typ. 190mA, 380mA and 560mA

Boost Enable

V_{BAT} <9.5V → Boost Converter enabled

GDU – Boost Converter

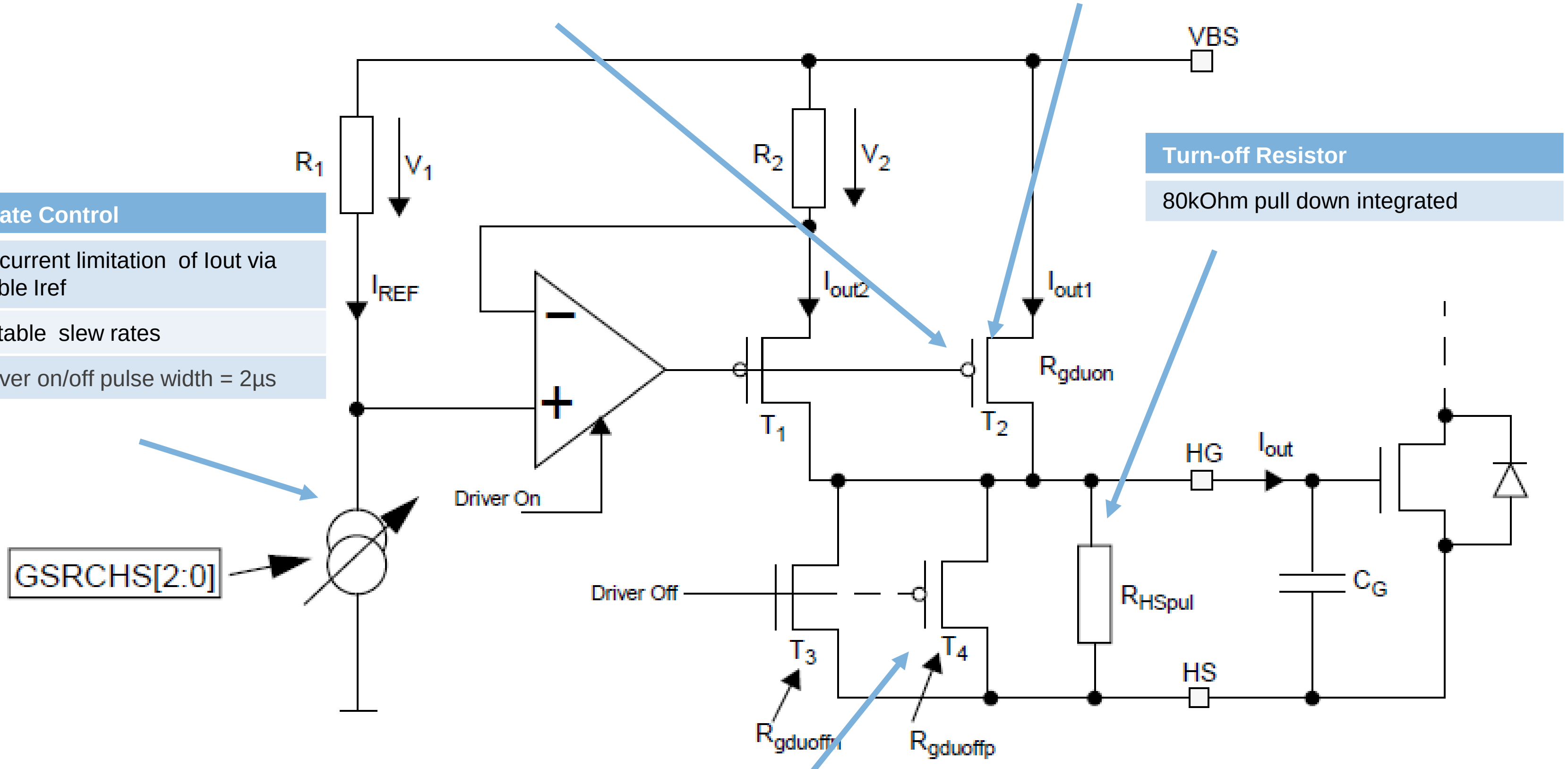
Without Boost

Vsup	MCU	GDU
20V…40V	Full	Disabled
7V…20V	Full	Enabled Vgs> Vsup – 2*Vbe (5V min)
6V .. 7V	Full	Disabled
3.5V .. 6V	Full Iddx = 25mA max if no external PNP	Disabled
<3.5V	Reset	Disabled

With Boost

Vsup	MCU	GDU
20V... 40V	Full	Disabled
9.5V...20V	Full	Boost OFF for Vsup > 11V Vgs = 9.6V
6V…9.5V	Full	Boost ON Vgs >9V
3.5V .. 6V	Full Iddx = 25mA max if no external PNP	Boost ON Vgs >9V
<3.5V	Reset	Disabled

GDU – Gate Driver Details



Driver current - Switch On

Typ. 6.3 Ohm

Max. Frequency

Min driver on/off pulse width = 2µs

Turn-off Resistor

80kOhm pull down integrated

Slew Rate Control

Output current limitation of Iout via selectable Iref

8 selectable slew rates

Min driver on/off pulse width = 2µs

Driver current - Switch Off

PMOS dominating

Typ. 16 Ohm

GDU – GDU Slew Rate Control

GDUSRC Register

Module Base + 0x0005

Access: User read/write[1]

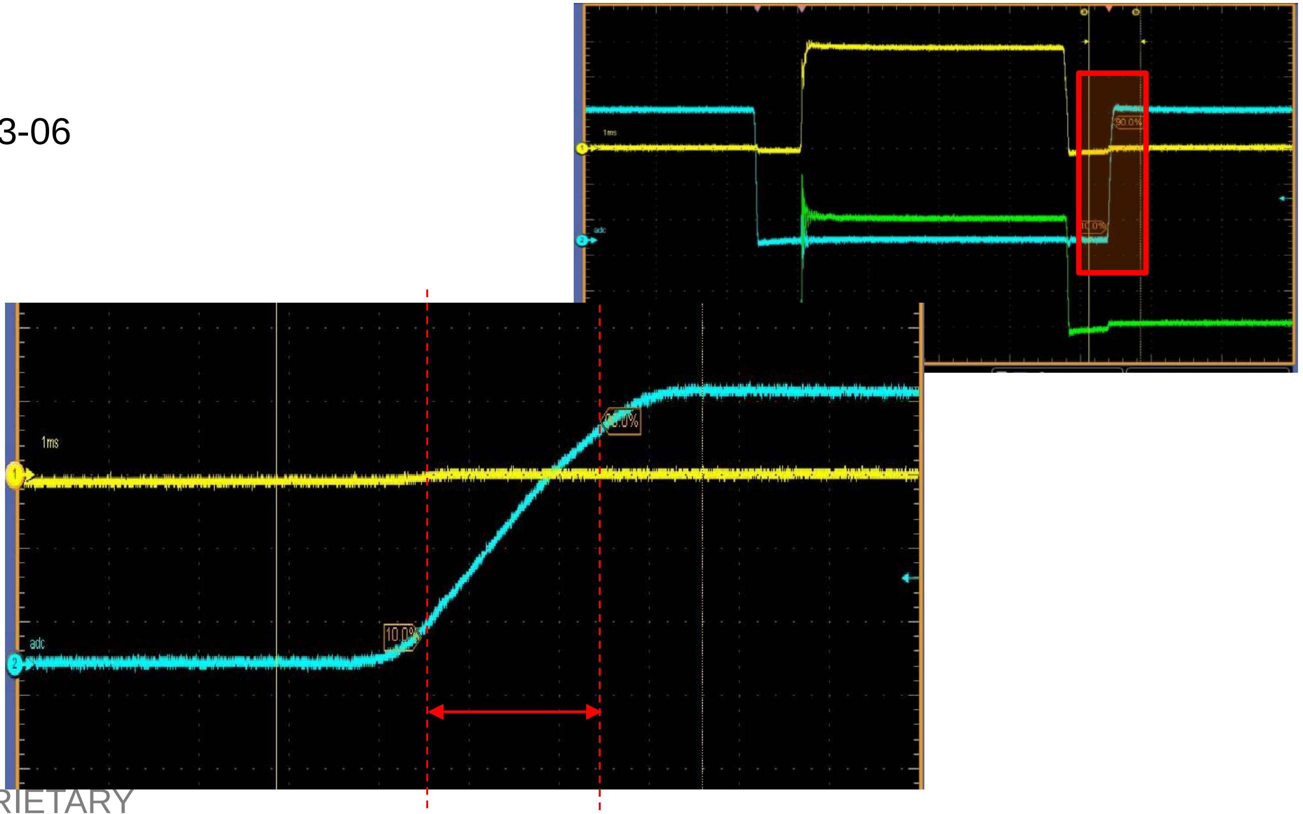
	7	6	5	4	3	2	1	0
R	0	GSRCHS[2:0]			0	GSRCLS[2:0]		
W								
Reset	0	1	0	0	0	1	0	0

Only writable if GDU Write Protection GWP disabled!

Example

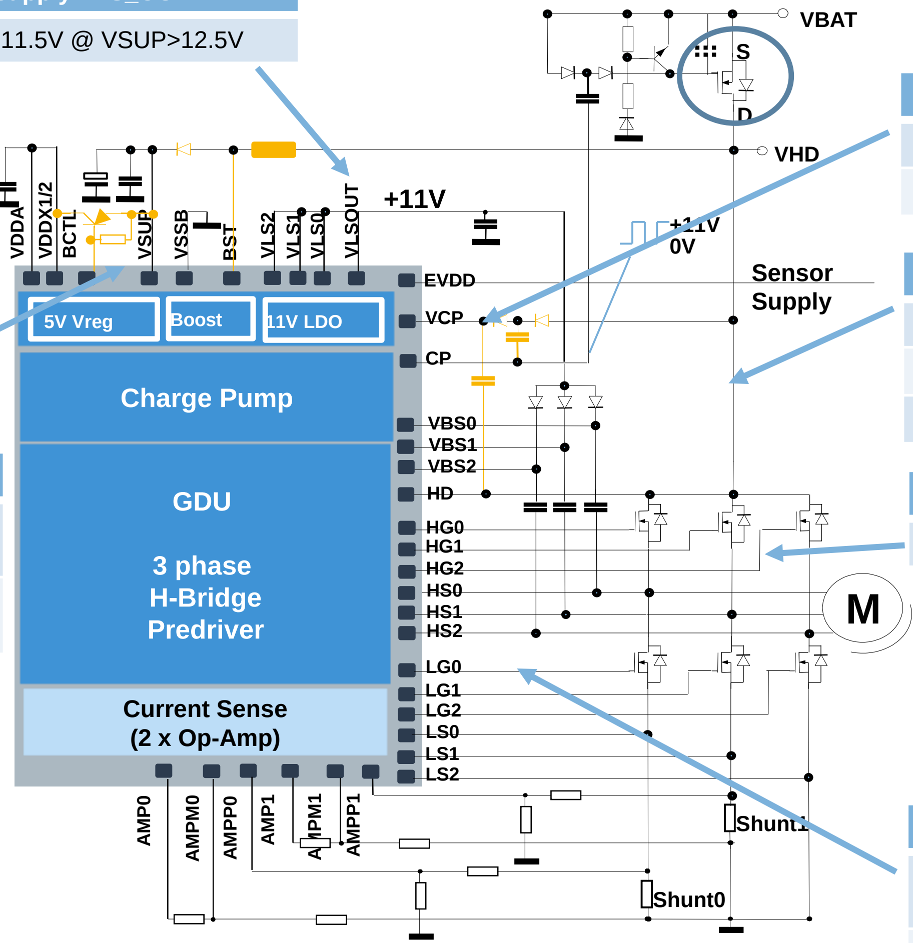
measured with IPD80N04S3-06
0Ohm gate resistance
Low Side
10% to 90%

7: 101 ns
6: 104 ns
5: 107 ns
4: 109 ns
3: 112 ns
2: 136 ns
1: 188 ns
0: 396 ns



GDU – Gate Drive Unit voltage ranges

GDU supply VLS_OUT
10.5.. 11.5V @ VSUP>12.5V



Charge Pump Output VCP
Supplies HS Gate Drive
Pin Max. rating: -0.3 .. 42V

DC Link / High Side Drain (HD)
High Voltage Monitor @ typ. 21/27.3 V
Filter for High Side Monitor of typ. 2,7µs
Pin Max. rating: -0.3 .. 42V

HG / HS /LG /LS
Max. rating: -5 .. 42V

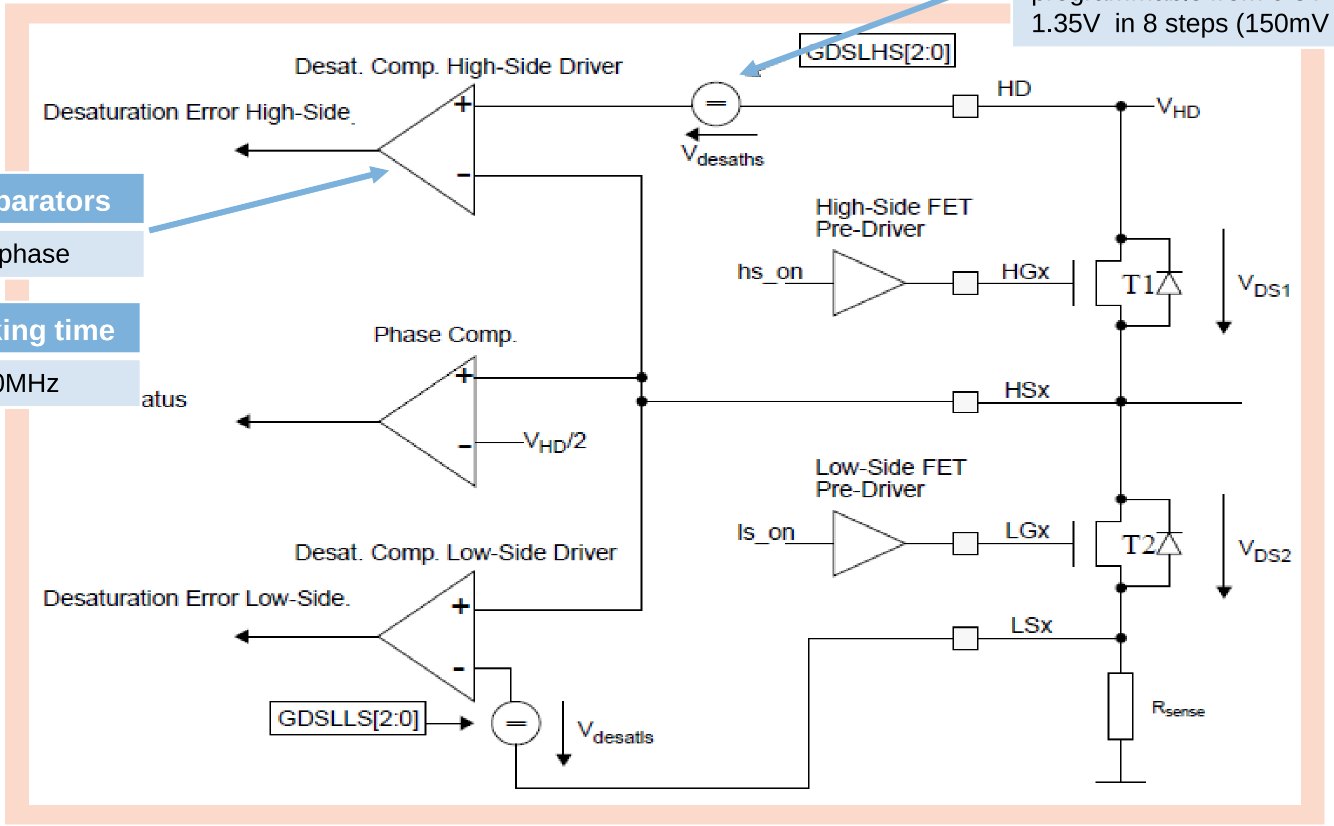
VSUP range	
Full function	Boost: 3.5..20 V Without Boost: 7..20 V
Full function/ Limited time	Boost: 3.5..26V Without Boost: 7..26 V

Vgs range
Boost: 9..12 V Without Boost: 5..12 V
Low Voltage trip point: 6.2 .. 7V

GDU – V_{DS} monitoring & Overcurrent Protection

- After turning on (any) high-side or low-side transistor, the HSx voltage is monitored

- In case of de-saturation error
  →LS/HS switched off
  → optional interrupt



Desaturation voltage

programmable from 0.3V to 1.35V in 8 steps (150mV steps)

6 Desaturation Comparators

One HS and one LS per phase

Programmable blanking time

From 80ns..4.84µs @ 50MHz

GDU – BEMF Sensing

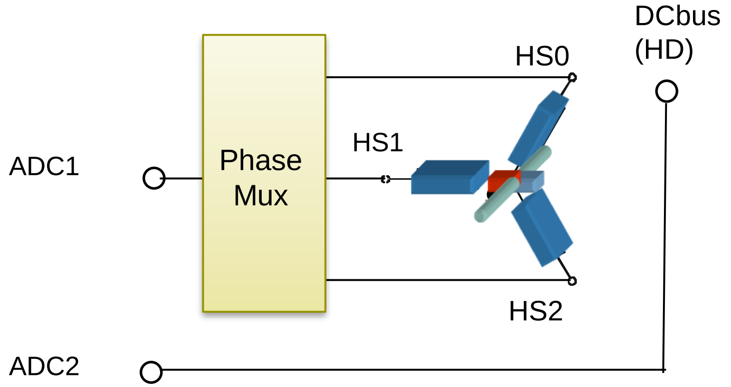
SW and HW Zero crossing topologies are both supported in S12ZVM:

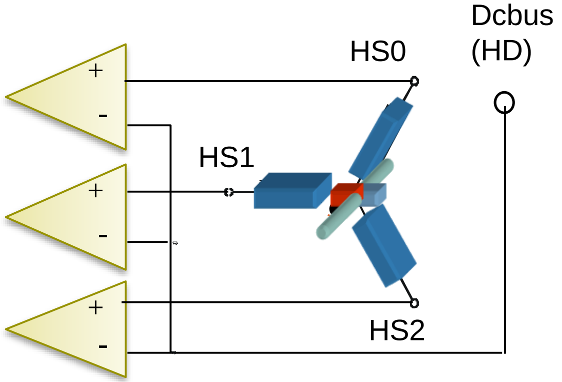
1) SW Zero crossing detection

- Integrated phase multiplexer to select the phase which is routed to the ADC internal channel
- Integrated voltage dividers for HD (DCbus) and Phase input voltages

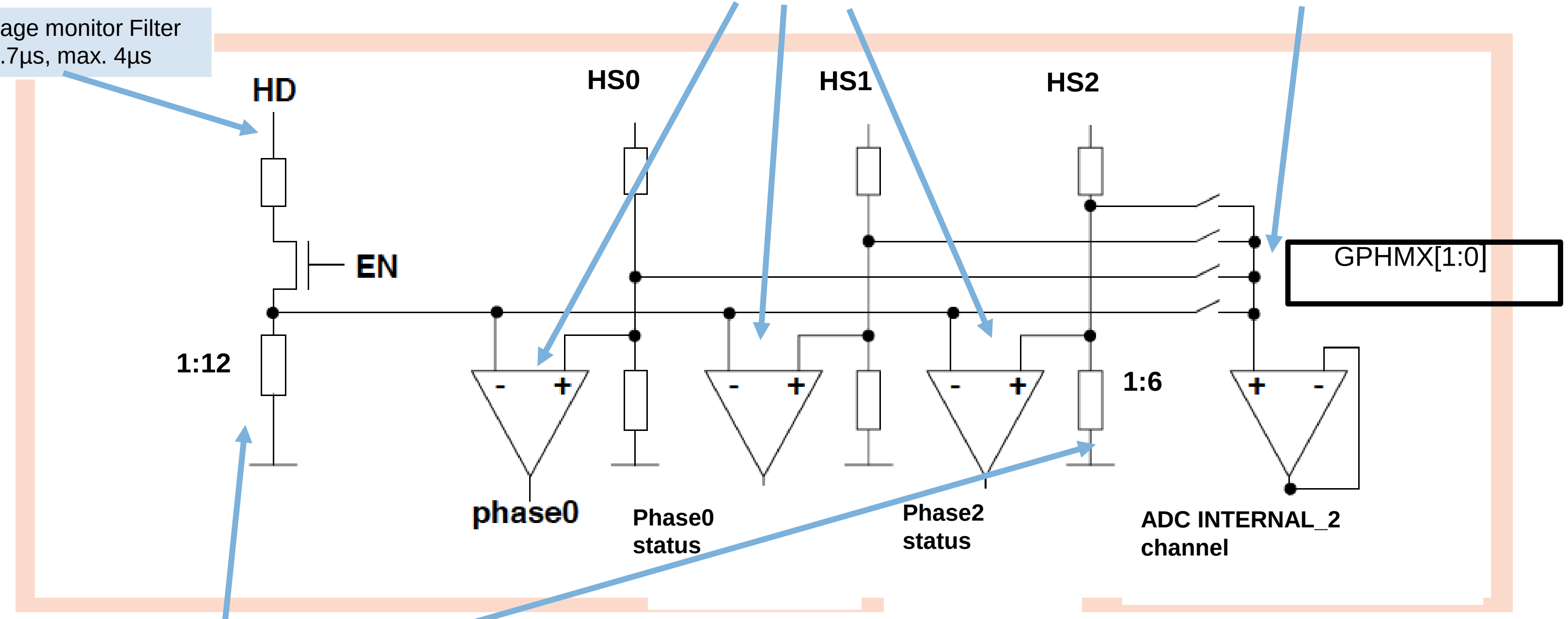
2) HW Zero crossing detection

- Integrated phase comparators to indicate if V_{HSx} is greater than $0.5*V_{HD}$
- Integrated voltage dividers





GDU – Phase Comparator



Phase Comparators

Compares against DCbus/2 in HW

Phase Multiplexer

Switched in each sector

DC Link Filter

High Voltage monitor Filter Of typ. 2.7µs, max. 4µs

Integrated Dividers

HD: divider 12 ; HS : divider 6

Secondary HD divider of 5 used for standard HD reading and for HD overvoltage detection

- The phase comparators indicate if phase voltage V_{HSx} is greater than 0.5*V_{HD}
- This can be used for BEMF detection in un-driven phases
- A multiplexer selects if the supply voltage HD or any of the phase voltages is routed to an ADC internal channel

GDU – Current measurement & Overcurrent protection

Overcurrent Comparator

Flexible programmable with 6-bit DAC

Voltage range : 3.82V .. VDDA

Current measurement

Two current sense amplifiers

Supports 2-shunt systems

Measures voltage across shunt

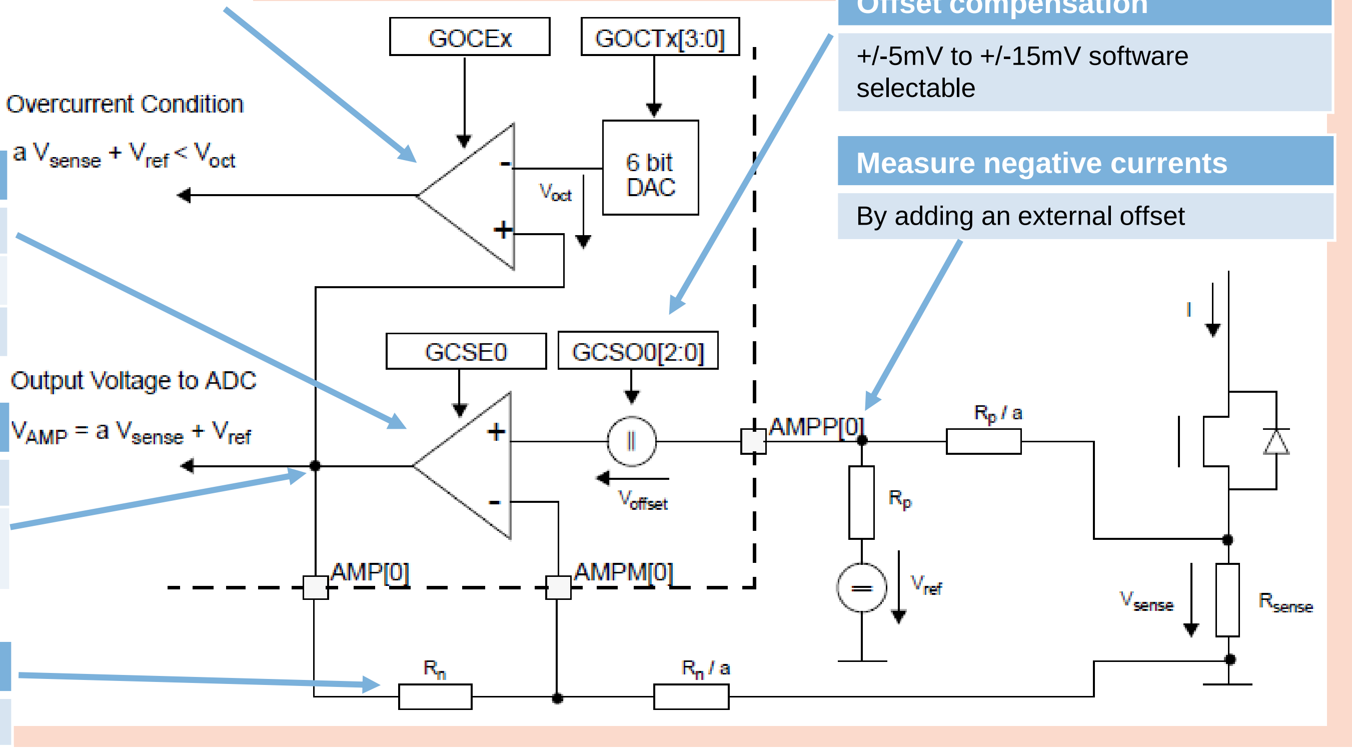
Output voltage

Range 0 V .. VDDA

measured on ADC via external channel AMP(0/1)

Gain

Selectable via external resistors



Offset compensation

+/-5mV to +/-15mV software selectable

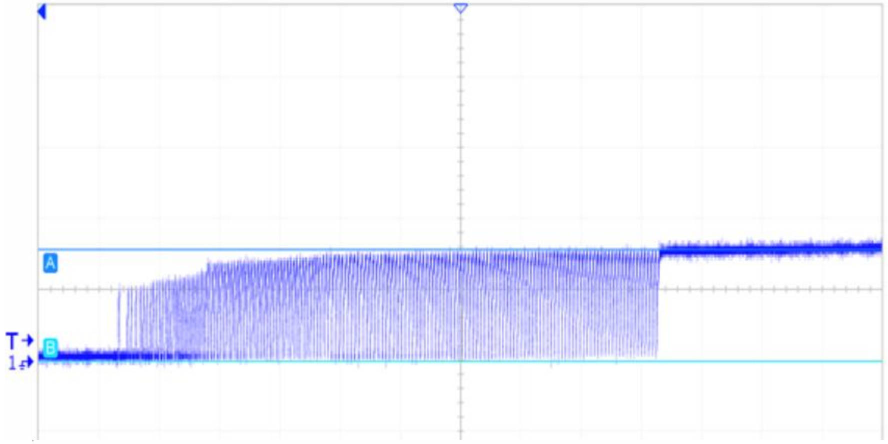
Measure negative currents

By adding an external offset

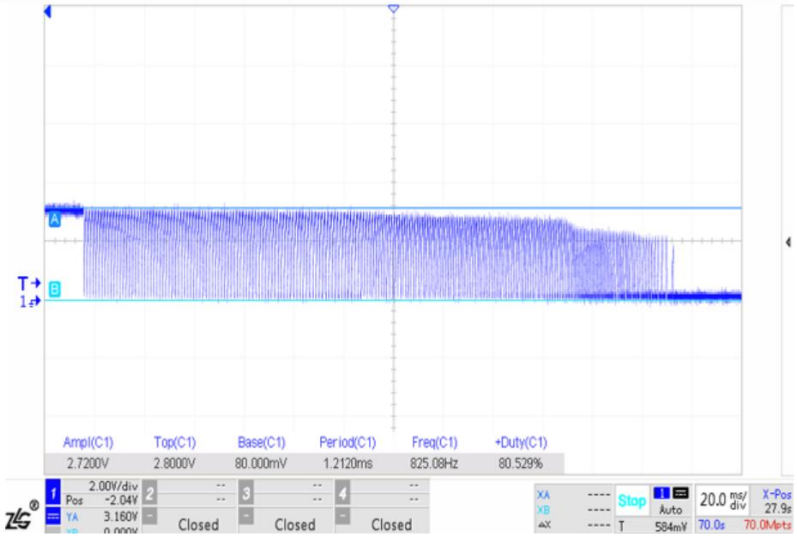
CASE SHARING

Case 1 – Some abnormal behavior @ power on or power down

- We want to know why S12ZVL reset pin will show abnormally waveform when VSUP power on or power down at 3.8v, and at this situation, GPIO will also output waveform, we capture the power on and power down waveform on GPIO and reset pin when VSUP at 3.8v point, could you help for it?

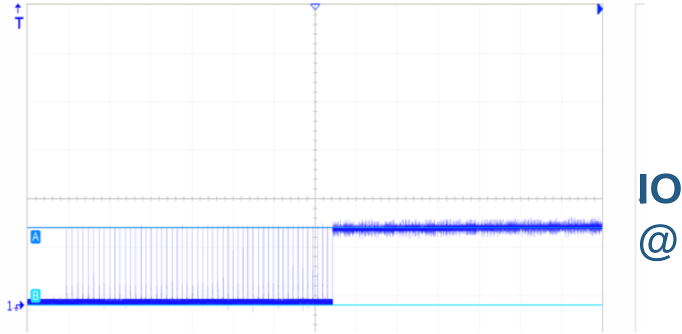


RESET PIN
@Power ON

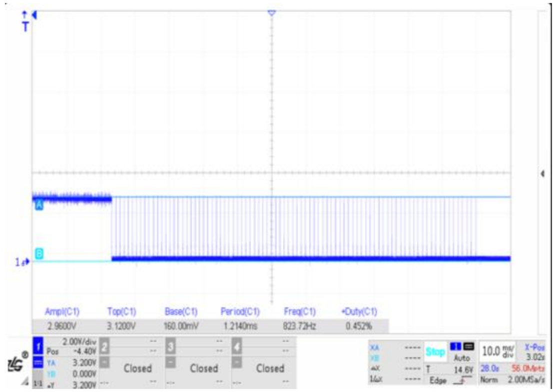


Ampl(C1)	Top(C1)	Base(C1)	Period(C1)	Freq(C1)	+Duty(C1)
2.7200V	2.8000V	80.000mV	1.2120ms	825.08Hz	80.529%

RESET PIN
@Power OFF



IO PIN
@Power ON



Ampl(C1)	Top(C1)	Base(C1)	Period(C1)	Freq(C1)	+Duty(C1)
2.9600V	3.1200V	160.00mV	1.2140ms	823.72Hz	0.452%

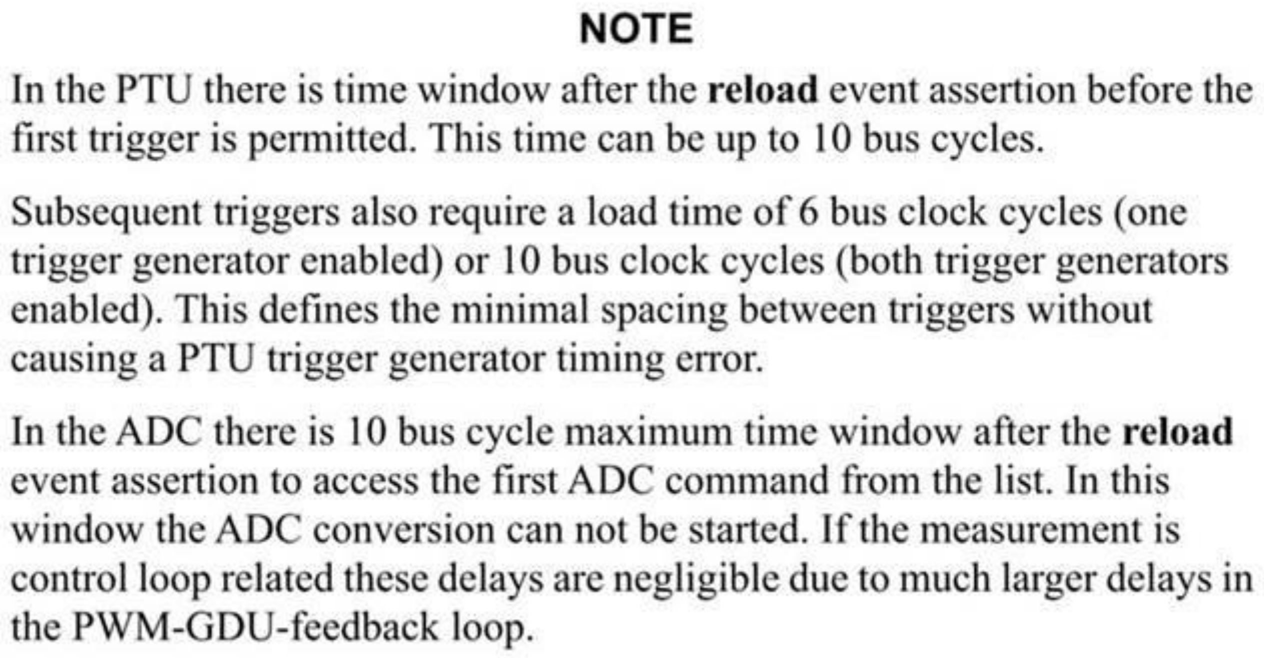
IO PIN
@Power OFF

Case 1 – Solution

- *Root cause：minimum supply voltage of S12ZVL is 3.5V. If VSUP bigger than 3.5V, the silicon will start work from RESET status. But the power on process will cause supply voltage oscillate and S12ZVL jump in and jump out RESET status.*
- *If S12ZVL jump out RESET status, the customer app may work and IO will output; but if the jump in RESET status, the IO will not output. So the IO abnormal output will show.*
- *Possible Solution: customer app should monitor supply voltage after the power on. If the supply voltage is stable and bigger than 3.5V, then the app can go other tasks, no any output before the voltage stable and bigger than 3.5V. When power down, also check the supply voltage, if supply voltage small than a certain value, for example, 4.0V, stop the output.*

Case 2 – ADC TRIG error happened if set the PTU first trigger very small

- The case happened if using PTU to trigger ADC and the first trigger point is smaller than 10.
- *The root cause is ADC need 10 bus cycle maximum time window to access the first ADC command from the list.*



NOTE

In the PTU there is time window after the **reload** event assertion before the first trigger is permitted. This time can be up to 10 bus cycles.

Subsequent triggers also require a load time of 6 bus clock cycles (one trigger generator enabled) or 10 bus clock cycles (both trigger generators enabled). This defines the minimal spacing between triggers without causing a PTU trigger generator timing error.

In the ADC there is 10 bus cycle maximum time window after the **reload** event assertion to access the first ADC command from the list. In this window the ADC conversion can not be started. If the measurement is control loop related these delays are negligible due to much larger delays in the PWM-GDU-feedback loop.

In dual shunt FOC code, the first trigger point is 0x10.

Case 3 – Any tips for tracking sampling point

- Customer met some ADC sampling issue (by using PTU and PMF method), how to position the issue and help customer to solve it.

Solution: *if can track the trigger point, the investigation become more easier.*

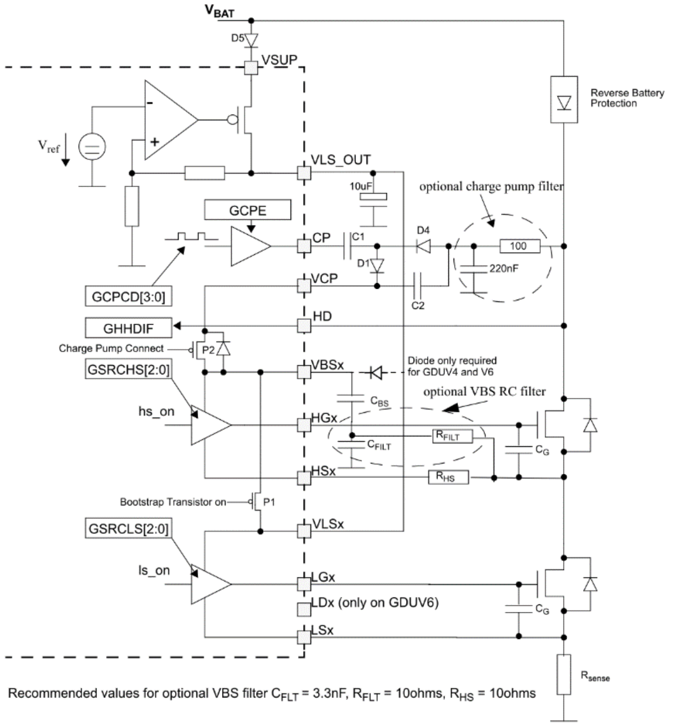
```
PTUDEBUG_PTUT0PE = 1;  // Enable Trigger Generation 0
PTUDEBUG_PTUT1PE = 1;  // Enable Trigger Generation 1
PTUDEBUG_PTUREPE = 1;  // Enable Reload generation to PIN
```

*Set the above register configuration, it can check the output of T0, T1 and reload signals in **debug mode**.*

it can’t work in normal mode.

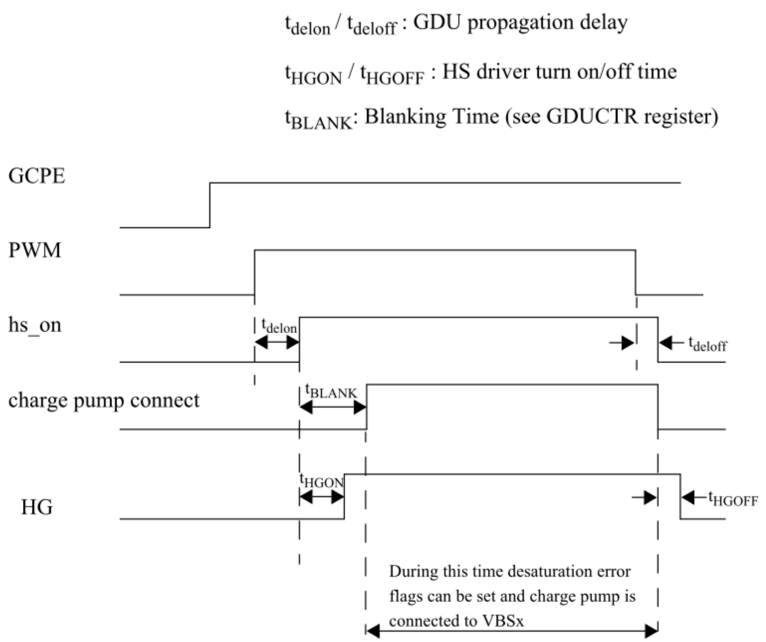
Case 4 – Bootstrap circuit can be delete?

- Charge pump are used to supply top MOSFET Vgs, the bootstrap circuit also used to turn on top MOSFET. Is it possible to simplify the circuit and delete the bootstrap circuit?
- *No, can’t only use charge pump without bootstrap circuit. But can delete charge pump circuit if not need 100% percent turn top MOSFET on. Because the charge pump circuit can’t work alone to turn on top MOSFETs.*



Recommended values for optional VBS filter C_{FLT} = 3.3nF, R_{FLT} = 10ohms, R_{HS} = 10ohms

Figure 18-21. Timing Diagram Charge Pump Connect



t_{delon} / t_{deloff} : GDU propagation delay
t_{HGON} / t_{HGOFF} : HS driver turn on/off time
t_{BLANK}: Blanking Time (see GDUCTR register)
GCPE
PWM
hs_on
t_{delon}
t_{deloff}
charge pump connect
t_{BLANK}
HG
t_{HGON}
t_{HGOFF}
During this time desaturation error flags can be set and charge pump is connected to VBSx

Charge pump circuit connect has a delay tBlank which is used in desaturation detection.

so tBlank can’t be zero.

NXP

SECURE CONNECTIONS
FOR A SMARTER WORLD