FS26

Safety system basis chip with low power for ASIL D/ASIL B

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Product data sheet
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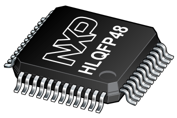

Document information

Information	Content
Keywords	Safety, SBC, automotive, low power, ASIL B, ASIL D
Abstract	Devices in the FS26 automotive safety system basis chip (SBC) family are designed to support entry and mid-range safety microcontrollers, such as those in the S32K3 series.

1 General description

Devices in the FS26 automotive safety system basis chip (SBC) family are designed to support entry and mid-range safety microcontrollers, like those in the S32K3 series. FS26 devices have multiple power supplies and the flexibility to work with other microcontrollers targeting automotive electrification. Possible FS26 applications include power train, chassis, safety, and low-end gateway technology.

This family of devices consists of several versions that are pin-to-pin and software compatible. These versions support a wide range of applications with Automotive Safety Integrity Levels (ASIL) B or D, offering choices in number of output rails, output voltage settings, operating frequencies, power-up sequencing, and integrated system-level features.

The FS26 features multiple switch mode regulators and low dropout (LDO) voltage regulators to supply the microcontroller, sensors, peripheral ICs, and communication interfaces. It offers a high-precision reference voltage supply for the system, and for two independent tracking regulators. The FS26 also offers various functionalities for system control and diagnostics, including an analog multiplexer, general-purpose input/outputs (GPIOs), and selectable wake-up events from I/O, long duration timer, or serial peripheral interface (SPI) communication.

The FS26 is developed in compliance with the ISO 26262 standard, and includes enhanced safety features with multiple fail-safe outputs. It uses the latest on demand latent fault monitoring, and can be part of a safety-oriented system partitioning scheme covering both ASIL B and ASIL D safety integrity levels.

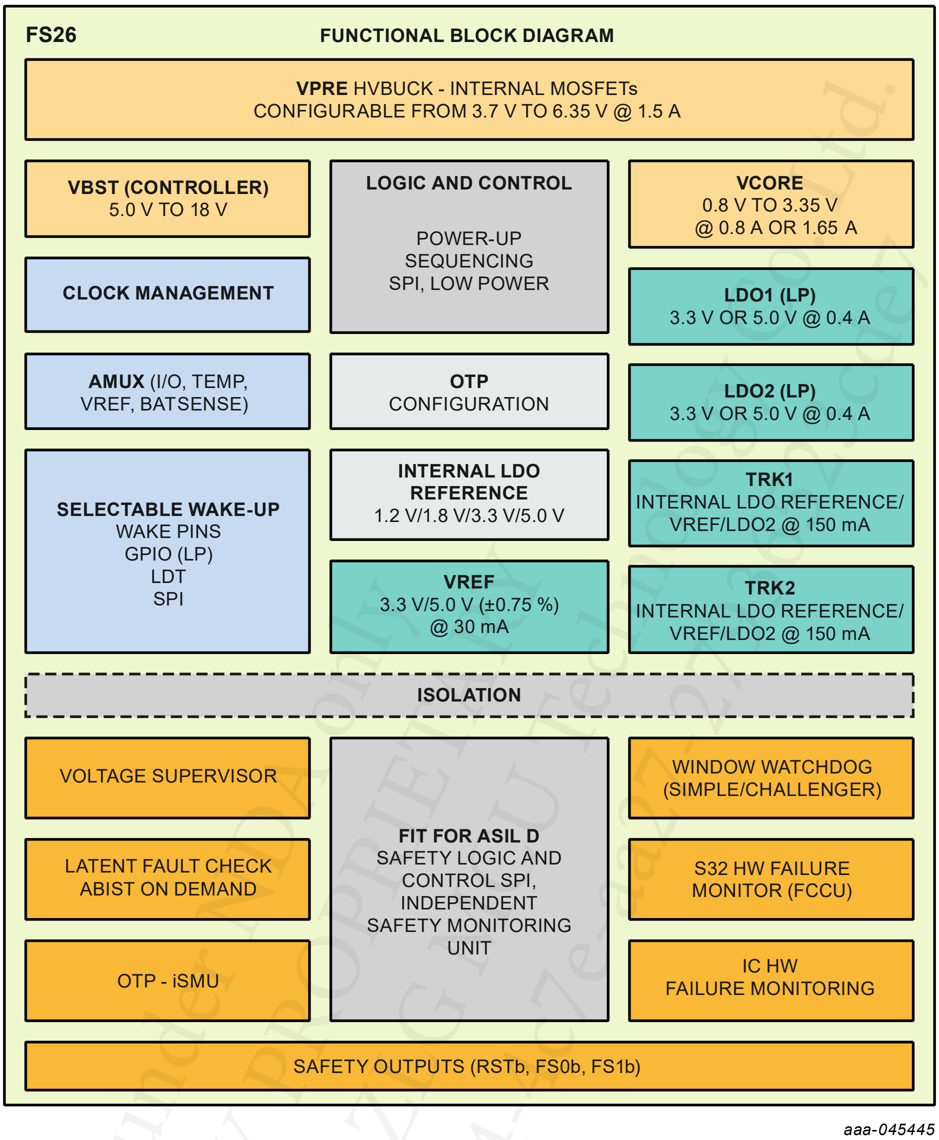

Figure 1. Functional block diagram

2 Features and benefits

Operating range

- 40 V DC maximum input voltage
- Support operating voltage range down to battery 3.2 V with VBST in front-end
- Support operating voltage range down to battery 6 V without VBST in front-end
- Low Power *LPOFF mode* with 30 µA quiescent current
- Low Power *standby mode* with 29 µA quiescent current with VPRE active. LDO1 or LDO2 activation selectable via OTP configuration. GPIO1 or GPIO2 activation selectable via SPI communication.

Power supplies

- VPRE: Synchronous buck converter with integrated FETs. Configurable output voltage and switching frequency, output DC current capability up to 1.5 A and PFM mode for Low Power *standby mode* operation.
- VCORE: Synchronous buck converter with integrated FETs. VCORE is dedicated for microcontroller core supply. Output DC current up to 0.8 A or 1.65 A (depending on part number), output voltage range setting from 0.8 V to 3.35 V.
- VBST: Asynchronous boost controller with external low-side switch, diode, and current sense resistor. VBST is configurable as front-end supply to withstand low voltage cranking profiles or in back-end supply with configurable output voltage and scalable output DC current capability.
- LDO1: LDO regulator for microcontroller I/O support with selectable output voltage between 3.3 V and 5.0 V and up to 400 mA current capability.
- LDO2: LDO regulator for system peripheral support with selectable output voltage between 3.3 V and 5.0 V and up to 400 mA current capability.
- VREF: High-precision reference voltage with 0.75 % accuracy for External ADC reference and internal tracking reference.
- TRK1 and TRK2: Voltage tracking regulators with selectable output voltage between VREF, LDO2, or Internal LDO reference. Support high-voltage protection for ECU off board operation. Each Tracker has a current capability up to 150 mA.

System support

- Two wake-up inputs with high-voltage support for system robustness
- Two programmable GPIO with wake-up capability or HS/LS driver
- Programmable long duration timer (LDT) for system shutdown and wake-up control
- Monitoring of system voltages (Including Battery voltage monitoring) through the analog multiplexer
- Selectable wake-up sources from: WAKE/GPIO pins, LDT, or SPI activity
- Device control via 32-bit SPI interface with cyclic redundancy checks (CRC)

Compliance

- Electromagnetic compatibility (EMC) optimization techniques for switching regulators, including spread spectrum, slew rate control, and manual frequency tuning.
- Electromagnetic interference (EMI) robustness supporting various automotive EMI test standards.

Functional safety

- Scalable portfolio from Automotive Safety Integrity Levels (ASIL) B to D
- Independent monitoring circuitry, dedicated interface for microcontroller monitoring, simple or challenger watchdog function
- Analog built-in self-test (ABIST1) and logical built-in self-test (LBIST) at startup
- Analog built-in self-test (ABIST2) on demand
- Safety outputs with latent fault detection mechanism (RSTB, FS0B, FS1B)

Configuration and enablement

- LQFP48 pins with exposed pad for optimized thermal management
- Permanent device customization via one time programmable (OTP) fuse memory
- OTP Emulation mode for hardware development and evaluation
- *Debug mode* for software development, MCU programming, and debugging

3 Simplified application diagram

Figure 2 shows a simplified block diagram for a typical system with an FS2630, using the boost controller to support battery cold-crank events.

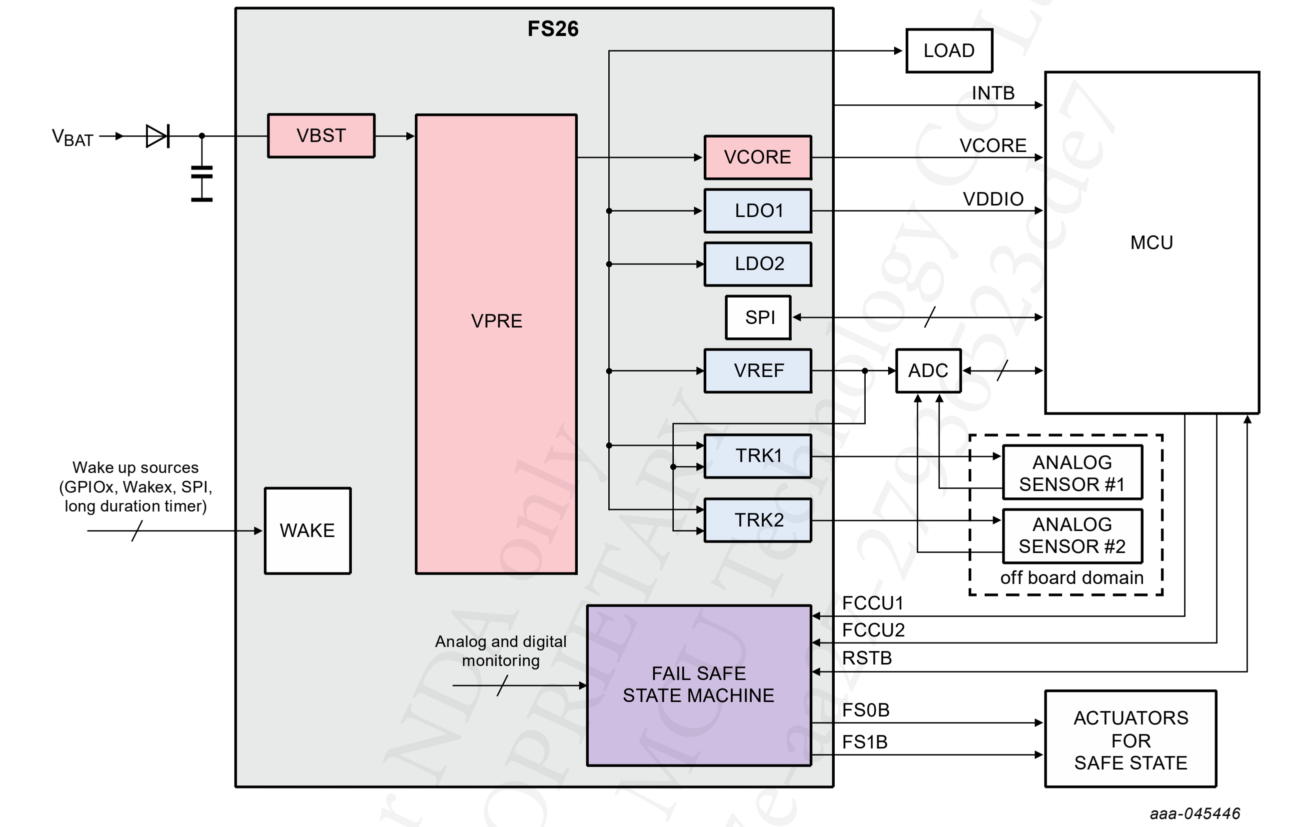

Figure 2. Example of application diagram with VBST as a front-end regulator

Figure 3 shows a simplified block diagram for a typical system with an FS2630, using the boost controller to generate a voltage above the high-voltage buck output voltage.

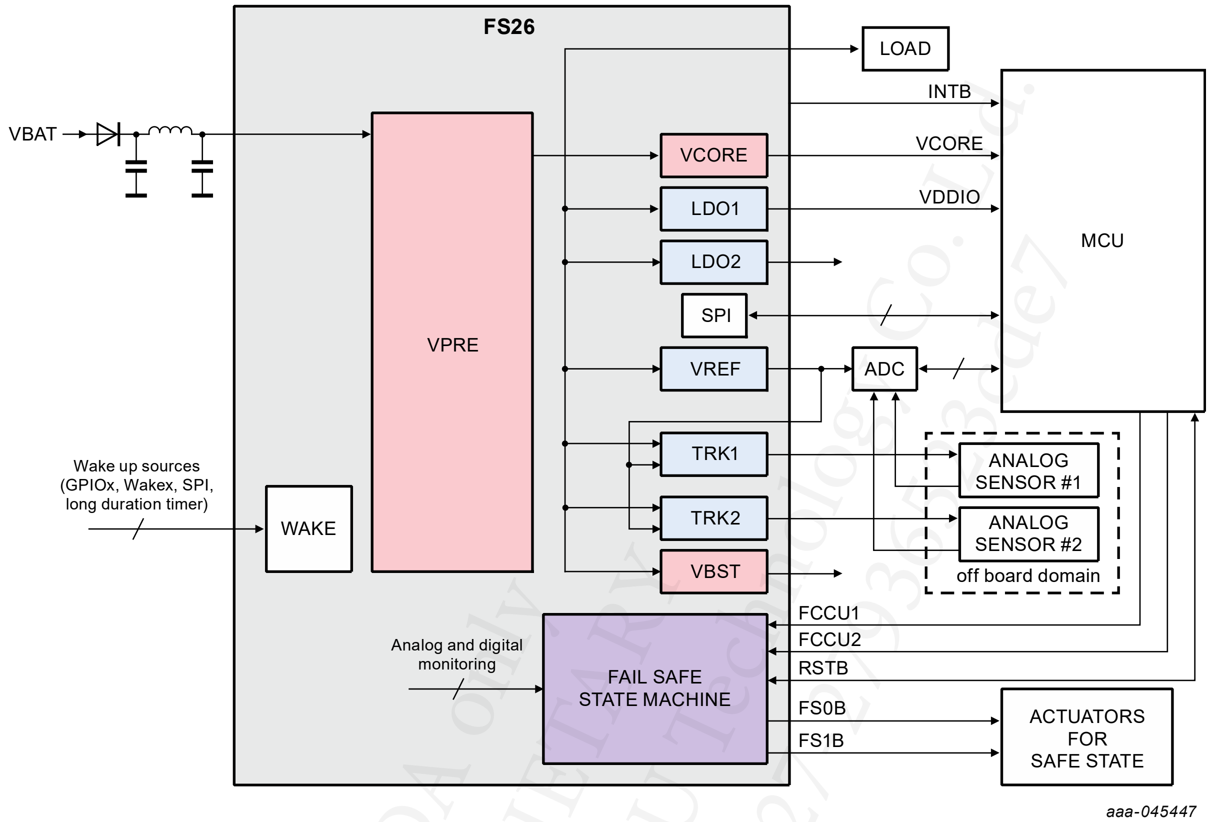

Figure 3. Example of application diagram with VBST as a back-end regulator

4 Ordering information

This section describes the part numbers available for purchase, with their main differences. It also depicts how the part number reference is built.

4.1 Part number definition

Figure 4 shows how the FS26xyz part number is used to describe the available feature set of each device.

FS26xx
Product Numbering Scheme

P		FS		26 X Y		A		M		Zzz		AD	
Release Type		Family		Product Core		Release Version		Temperature		Funct. or Param. variant		Package	
M	Production	FS	High Voltage Power Management	2600-2633	Core	A	Initial Release	M	-40 to 125 °C	A0	No OTP	AD	**LQFP48**
P	Pre-release					B-Z	as required			A1-ZZ	Unique part identification		
S	Customer special												

FS 2 6 X Y Z

Z	ASIL
B	Fit for ASIL B (Simple W/D, UV/OV, ABIST, VMON)
D	Fit for ASIL D (Challenger WD, FCCU, ABIST/LBIST, VMON)

Y	FS1b	LDT	Use case
0	no	no	Base
1	yes	no	FS1b
2	no	yes	LDT
3	yes	yes	FS1b and LDT

X	PMIC Solution
0	VCORE 0.8 A, VBST, 1 MV Buck, 2 LDOs 1 Tracker
1	VCORE 0.8 A, VBST, 1 MV Buck, 2 LDOs 2 Trackers
2	VCORE 1.65 A, VBST, 1 MV Buck, 2 LDOs 1 Tracker
3	VCORE 1.65 A, VBST, 1 MV Buck, 2 LDOs 2 Trackers

aaa-045498

Figure 4. Part number breakdown

Figure 5 maps FS26 part numbers vs. product feature sets.

Vcore	0.8 A core				1.65 A core			
EXT Supply	1 TRK		2 TRK		1 TRK		2 TRK	
ASIL Level	ASIL B	ASIL D	ASIL B	ASIL D	ASIL B	ASIL D	ASIL B	ASIL D
Base	FS2600B	FS2600D	FS2610B	FS2610D	FS2620B	FS2620D	FS2630B	FS2630D
FS1b	FS2601B	FS2601D	FS2611B	FS2611D	FS2621B	FS2621D	FS2631B	FS2631D
LDT	FS2602B	FS2602D	FS2612B	FS2612D	FS2622B	FS2622D	FS2632B	FS2632D
FS1b + LDT	FS2603B	FS2603D	FS2613B	FS2613D	FS2623B	FS2623D	FS2633B	FS2633D

aaa-045499

Figure 5. Part number mapping versus features set

4.2 Part number list

Table 1. Device segmentation

Part Number	DEV_ID[5:0]	Tracker 2 TRK2	VCORE current capability	Long Duration Timer (LDT)	Tracker 2 monitoring VMON_TRK2	FS1B	ABIST on demand ABIST2	Watchdog type	Fault recovery	FCCU monitoring	LBIST
FS2600B	01h	NO	0.8 A	NO	NO	NO	YES	Simple	NO	Optional	NO
FS2601B	02h	NO	0.8 A	NO	NO	YES	YES	Simple	NO	Optional	NO
FS2602B	03h	NO	0.8 A	YES	NO	NO	YES	Simple	NO	Optional	NO
FS2603B	04h	NO	0.8 A	YES	NO	YES	YES	Simple	NO	Optional	NO
FS2600D	05h	NO	0.8 A	NO	NO	NO	YES	Challenger	YES	YES	YES
FS2601D	06h	NO	0.8 A	NO	NO	YES	YES	Challenger	YES	YES	YES
FS2602D	07h	NO	0.8 A	YES	NO	NO	YES	Challenger	YES	YES	YES
FS2603D	08h	NO	0.8 A	YES	NO	YES	YES	Challenger	YES	YES	YES
FS2610B	09h	YES	0.8 A	NO	YES	NO	YES	Simple	NO	Optional	NO
FS2611B	0Ah	YES	0.8 A	NO	YES	YES	YES	Simple	NO	Optional	NO
FS2612B	0Bh	YES	0.8 A	YES	YES	NO	YES	Simple	NO	Optional	NO
FS2613B	0Ch	YES	0.8 A	YES	YES	YES	YES	Simple	NO	Optional	NO
FS2610D	0Dh	YES	0.8 A	NO	YES	NO	YES	Challenger	YES	YES	YES
FS2611D	0Eh	YES	0.8 A	NO	YES	YES	YES	Challenger	YES	YES	YES
FS2612D	0Fh	YES	0.8 A	YES	YES	NO	YES	Challenger	YES	YES	YES
FS2613D	10h	YES	0.8 A	YES	YES	YES	YES	Challenger	YES	YES	YES
FS2620B	11h	NO	1.65 A	NO	NO	NO	YES	Simple	NO	Optional	NO
FS2621B	12h	NO	1.65 A	NO	NO	YES	YES	Simple	NO	Optional	NO
FS2622B	13h	NO	1.65 A	YES	NO	NO	YES	Simple	NO	Optional	NO
FS2623B	14h	NO	1.65 A	YES	NO	YES	YES	Simple	NO	Optional	NO
FS2620D	15h	NO	1.65 A	NO	NO	NO	YES	Challenger	YES	YES	YES
FS2621D	16h	NO	1.65 A	NO	NO	YES	YES	Challenger	YES	YES	YES
FS2622D	17h	NO	1.65 A	YES	NO	NO	YES	Challenger	YES	YES	YES
FS2623D	18h	NO	1.65 A	YES	NO	YES	YES	Challenger	YES	YES	YES
FS2630B	19h	YES	1.65 A	NO	YES	NO	YES	Simple	NO	Optional	NO
FS2631B	1Ah	YES	1.65 A	NO	YES	YES	YES	Simple	NO	Optional	NO
FS2632B	1Bh	YES	1.65 A	YES	YES	NO	YES	Simple	NO	Optional	NO
FS2633B	1Ch	YES	1.65 A	YES	YES	YES	YES	Simple	NO	Optional	NO
FS2630D	1Dh	YES	1.65 A	NO	YES	NO	YES	Challenger	YES	YES	YES
FS2631D	1Eh	YES	1.65 A	NO	YES	YES	YES	Challenger	YES	YES	YES
FS2632D	1Fh	YES	1.65 A	YES	YES	NO	YES	Challenger	YES	YES	YES
FS2633D	20h	YES	1.65 A	YES	YES	YES	YES	Challenger	YES	YES	YES

Additional part numbers will exist with different features and parametric settings. Table 1 is an example of a part number list.

Table 2. Orderable part numbers

Part number	Description	Package
MFS2613AMDA2AD	S32K344+ FS26 EVB ASIL D S32K3X4EVB-x257	**LQFP48**
MFS2613AMDA3AD	S32K344 400 V HVBMS Reference design	
MFS2613AMDA4AD	S32K344 Body Control Module Reference design (white board)	
MFS2613AMDA6AD	S32K344 48 V MC Development platform	

Table 2. Orderable part numbers...*continued*

Part number	Description	Package
MFS2621AMDABAD	Aurix TC38, TC29	
MFS2613AMDDCAD	S32K324 5G T-BOX + Gateway	
MFS2600AMBA0AD	Superset covering FS2600B devices	
MFS2600AMDA0AD	Superset covering FS2600D devices	
MFS2601AMBA0AD	Superset covering FS2601B devices	
MFS2601AMDA0AD	Superset covering FS2601D devices	
MFS2602AMBA0AD	Superset covering FS2602B devices	
MFS2602AMDA0AD	Superset covering FS2602D devices	
MFS2603AMBA0AD	Superset covering FS2603B devices	
MFS2603AMDA0AD	Superset covering FS2603D devices	
MFS2610AMBA0AD	Superset covering FS2610B devices	
MFS2610AMDA0AD	Superset covering FS2610D devices	
MFS2611AMBA0AD	Superset covering FS2611B devices	
MFS2611AMDA0AD	Superset covering FS2611D devices	
MFS2612AMBA0AD	Superset covering FS2612B devices	
MFS2612AMDA0AD	Superset covering FS2612D devices	
MFS2613AMBA0AD	Superset covering FS2613B devices	
MFS2613AMDA0AD	Superset covering FS2613D devices	
MFS2620AMBA0AD	Superset covering FS2620B devices	
MFS2620AMDA0AD	Superset covering FS2620D devices	
MFS2621AMBA0AD	Superset covering FS2621B devices	
MFS2621AMDA0AD	Superset covering FS2621D devices	
MFS2622AMBA0AD	Superset covering FS2622B devices	
MFS2622AMDA0AD	Superset covering FS2622D devices	
MFS2623AMBA0AD	Superset covering FS2623B devices	
MFS2623AMDA0AD	Superset covering FS2623D devices	
MFS2630AMDA0AD	Superset covering FS2630D devices	
MFS2630AMBA0AD	Superset covering FS2630B devices	
MFS2631AMBA0AD	Superset covering FS2631B devices	
MFS2631AMDA0AD	Superset covering FS2631D devices	
MFS2632AMBA0AD	Superset covering FS2632B devices	
MFS2632AMDA0AD	Superset covering FS2632D devices	
MFS2633AMBA0AD	Superset covering FS2633B devices	
MFS2633AMDA0AD	Superset covering FS2633D devices	

Empty OTP samples can be ordered for engineering purposes using part numbers part numbers MFS2633AMDA0AD or MFS2633AMBA0AD. See Table 260 for the complete OTP content description.

5 Applications

xEV and powertrain market

- Inverter
- Onboard charger (OBC), DCDC
- Battery management system (BMS)
- Belt starter generator (BSG)

Body market

- Gateway
- Zonal control
- Body controller
- Smart junction box

Safety and chassis

- Suspension
- Power steering

MCU attach

- NXP S32K3 family
- Infineon Aurix family (TC2xx and TC3xx)
- Renesas RH850 family
- Cypress Traveo family

6 Block diagram

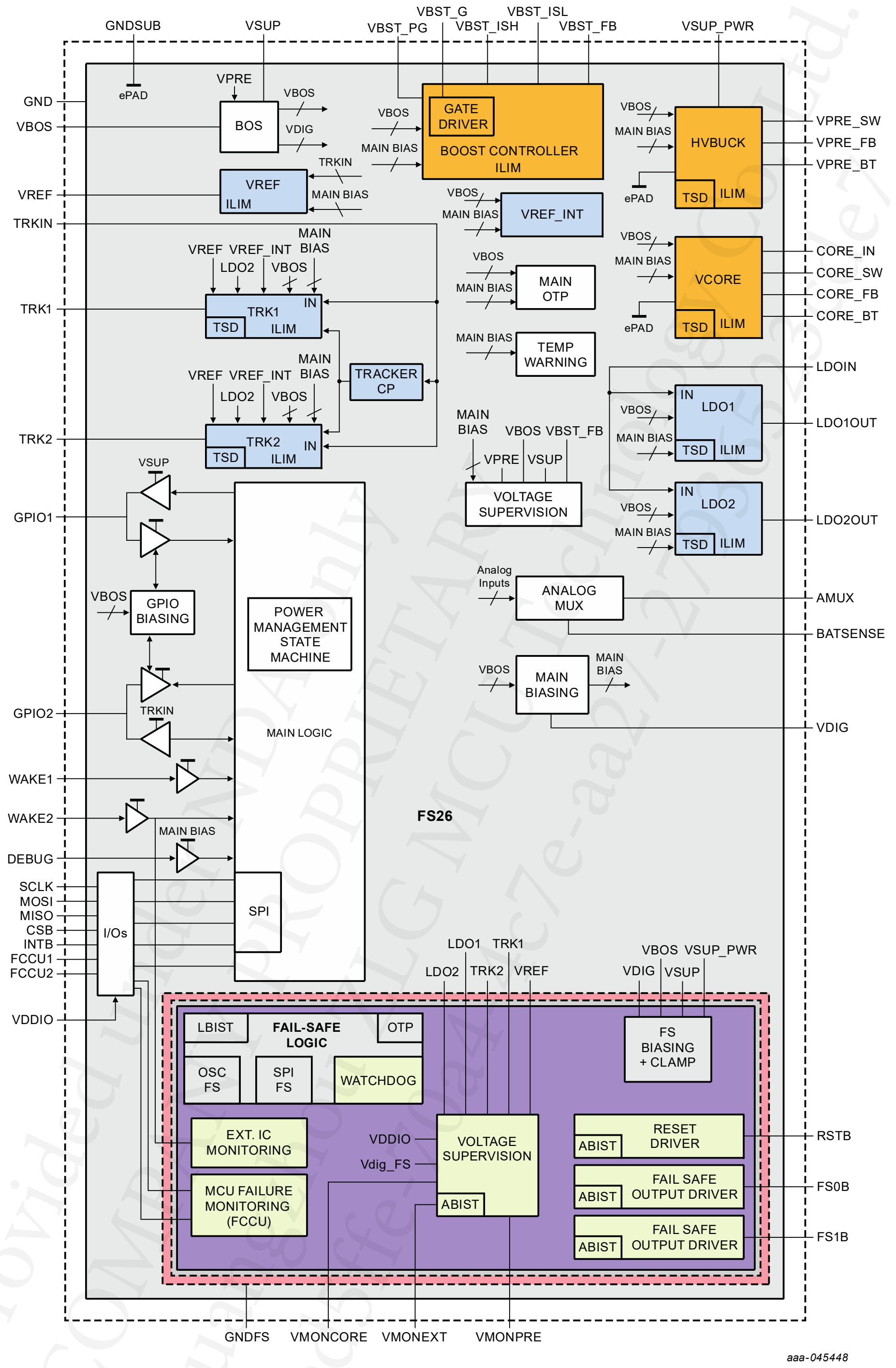

Figure 6. Block diagram of the FS26

7 Pinning information

7.1 Pinning

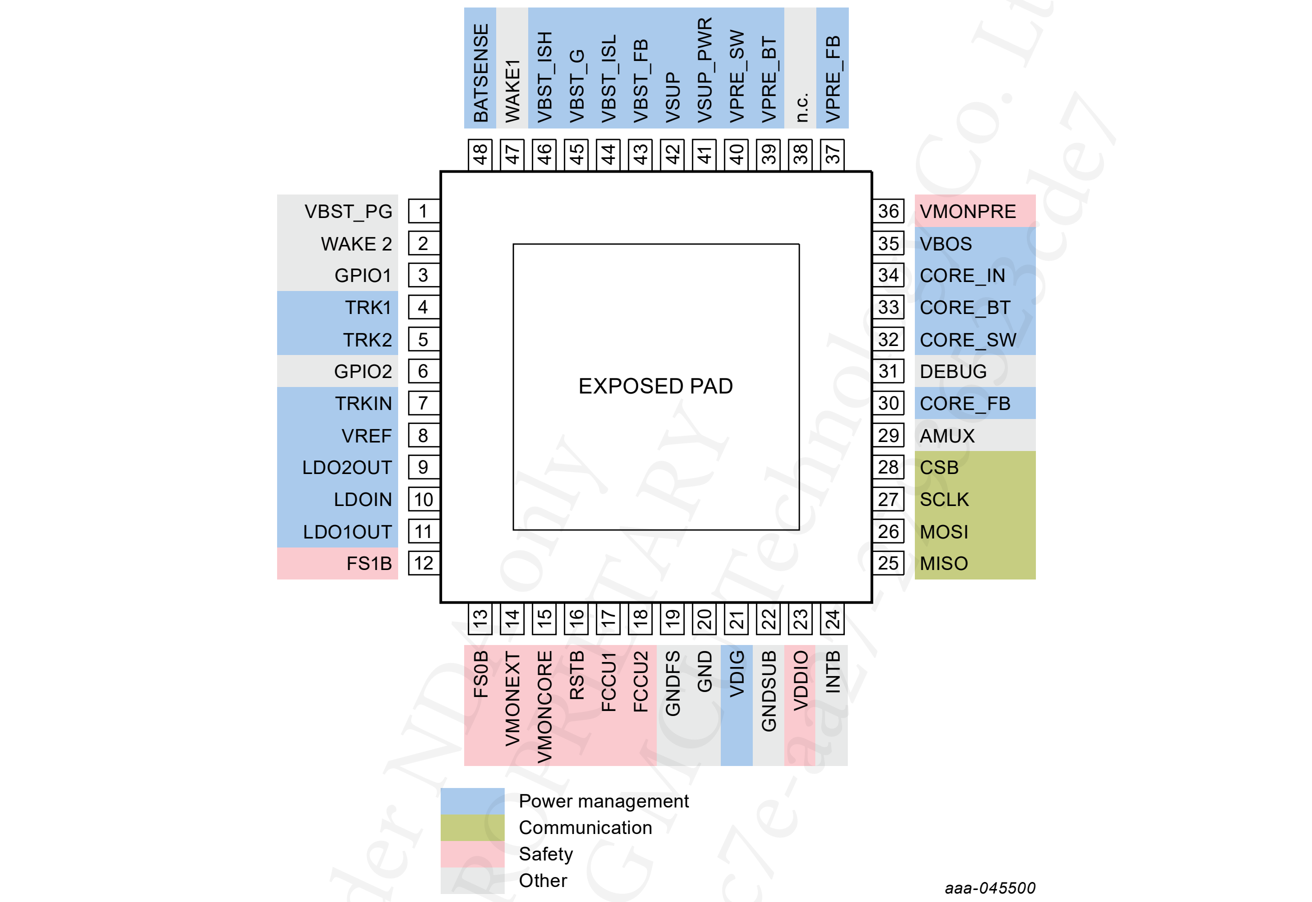

Figure 7. Pin assignment in LQFP48 package with exposed pad

7.2 Pin descriptions

Table 3. Pin descriptions

Symbol	Pin Number	Type	Description
VBST_PG	1	Digital output	Power Good signal of VBST
WAKE2	2	Analog input	WAKE2 input pin or ERRMON input
GPIO1	3	Analog output / Digital Input	General Purpose I/O 1 (GPIO1)
TRK1	4	Analog output	TRK1 regulator output
TRK2	5	Analog output	TRK2 regulator output
GPIO2	6	Analog output / Digital Input	General Purpose I/O 2 (GPIO2)
TRKIN	7	Analog input	TRK1, TRK2 and VREF regulators input
VREF	8	Analog output	Voltage reference output (VREF)
LDO2OUT	9	Analog output	LDO2 output
LDOIN	10	Analog input	LDO1 and LDO2 regulator input voltage supply
LDO1OUT	11	Analog output	LDO1 regulator output
FS1B	12	Digital output	Safety output #1 (FS01)

Table 3. Pin descriptions*...continued*

Symbol	Pin Number	Type	Description
FS0B	13	Digital output	Safety output #0 (FS02)
VMONEXT	14	Analog input	VMON_EXT voltage monitoring input
VMONCORE	15	Analog input	VMON_CORE voltage monitoring input
RSTB	16	Digital input/output	Reset input/output (RSTB)
FCCU1	17	Digital input	Fault Control Collection Unit (FCCU) pin 1
FCCU2	18	Digital input	Fault Control Collection Unit (FCCU) pin 2
GNDFS	19	Ground connection	Ground connection for fail-safe circuitry
GND	20	Ground connection	Ground connection for main circuitry
VDIG	21	Analog output	1.6 V digital supply
GNDSUB	22	Ground connection	Substrate ground
VDDIO	23	Analog input	I/O input supply
INTB	24	Digital output	Interrupt output
MISO	25	Digital output	SPI Primary In Secondary out
MOSI	26	Digital input	SPI Primary Out Secondary input
SCLK	27	Digital input	SPI clock input
CSB	28	Digital input	SPI chip select
AMUX	29	Analog output	Analog multiplexer (AMUX) output
CORE_FB	30	Analog input	VCORE feedback node
DEBUG	31	Digital input	DEBUG input pin. Used to enter OTP and *debug mode*
CORE_SW	32	Analog output	VCORE switching node
CORE_BT	33	Analog input	VCORE bootstrap supply
CORE_IN	34	Analog input	VCORE input supply
VBOS	35	Analog output	Best Of Supply (BOS) decoupling output
VMONPRE	36	Analog input	VMON_PRE voltage monitoring pin
VPRE_FB	37	Analog input	VPRE feedback node
NC	38	Not connected pin	Not connected pin
VPRE_BT	39	Analog output	VPRE boot strap capacitor
VPRE_SW	40	Analog output	VPRE switching node
VSUP_PWR	41	Analog input	VPRE converter supply pin
VSUP	42	Analog input	Supply pin for internal biasing
VBST_FB	43	Analog input	VBST feedback node
VBST_ISL	44	Analog input	VBST current sense low
VBST_G	45	Analog output	VBST low-side gate drive
VBST_ISH	46	Analog input	VBST current sense high
WAKE1	47	Analog input	WAKE1 input pin
BATSENSE	48	Analog input	Battery sense terminal
EP	49	Ground connection	Exposed pad (to be connected to ground)

8 Connection of unused pins

Table 4. Connection of unused pins

Symbol	Pin Number	Type	Connection if not used
VBST_PG	1	Digital output	Grounded
WAKE2	2	Analog input	Open - Internal pull-down can be activated by OTP (with WK2PD_OTP = 1)
GPIO1	3	Analog output / Digital Input	Open - Internal pull-down can be activated by OTP (with GPIO1PD_OTP = 1)
TRK1	4	Analog output	Open - TRK1 to be configured OFF for power-up sequence TRK1_SLOT_OTP[2:0] = 111
TRK2	5	Analog output	Open - TRK2 to be configured OFF for power-up sequence TRK2_SLOT_OTP[2:0] = 111
GPIO2	6	Analog output / Digital Input	Open - Internal pull-down can be activated by OTP (with GPIO2PD_OTP = 1)
TRKIN	7	Analog input	**Connection mandatory** when using VREF, TRK1, TRK2, or GPIO2 as high-side driver. Otherwise Open when not used.
VREF	8	Analog output	Open
LDO2OUT	9	Analog output	Open - LDO2 to be configured OFF for power-up sequence (with LDO2_SLOT_OTP[2:0] = 111)
LDOIN	10	Analog input	Open
LDO1OUT	11	Analog output	Open - LDO1 to be configured OFF for power-up sequence (with LDO1_SLOT_OTP[2:0] = 111)
FS1B	12	Digital output	Open - 2 MΩ internal pull-down
FS0B	13	Digital output	Open - 2 MΩ internal pull-down
VMONEXT	14	Analog input	Open - VMON_EXT to be disabled by OTP
VMONCORE	15	Analog input	Open
RSTB	16	Digital input/output	**Connection mandatory**
FCCU1	17	Digital input	Open - 800 kΩ internal pull-down
FCCU2	18	Digital input	Open - 200 kΩ internal pull-up to VDDIO
GNDFS	19	Ground connection	**Connection mandatory**
GND	20	Ground connection	**Connection mandatory**
VDIG	21	Analog output	**Connection mandatory with external decoupling capacitor (normalized value 1 µF)**
GNDSUB	22	Ground connection	**Connection mandatory**
VDDIO	23	Analog input	**Connection mandatory**
INTB	24	Digital output	Open - 10 kΩ internal pull-up to VDDIO
MISO	25	Digital output	Open - push-pull structure
MOSI	26	Digital input	Open - 450 kΩ internal pull-up to VDDIO
SCLK	27	Digital input	External pull-down to ground
CSB	28	Digital input	Open - 450 kΩ internal pull-up to VDDIO
AMUX	29	Analog output	Open
CORE_FB	30	Analog input	Open
DEBUG	31	Digital input	**Connection mandatory**
CORE_SW	32	Analog output	Open
CORE_BT	33	Analog input	Open
CORE_IN	34	Analog input	Open
VBOS	35	Analog output	**Connection mandatory**
VMONPRE	36	Analog input	**Connection mandatory**
VPRE_FB	37	Analog input	**Connection mandatory**
NC	38	non connected pin	Not applicable
VPRE_BT	39	Analog output	**Connection mandatory**
VPRE_SW	40	Analog output	**Connection mandatory**
VSUP_PWR	41	Analog input	**Connection mandatory**
VSUP	42	Analog input	**Connection mandatory**

Table 4. Connection of unused pins*...continued*

Symbol	Pin Number	Type	Connection if not used
VBST_FB	43	Analog input	Grounded when VBST is not used. **Otherwise, connection mandatory**
VBST_ISL	44	Analog input	Grounded when VBST is not used. **Otherwise, connection mandatory**
VBST_G	45	Analog output	Open when VBST is not used. **Otherwise, connection mandatory**
VBST_ISH	46	Analog input	Grounded when VBST is not used. **Otherwise, connection mandatory**
WAKE1	47	Analog input	Open - Internal pull-down can be activated by OTP (with WK1PD_OTP = 1)
BATSENSE	48	Analog input	**Connection mandatory**
EP	49	Ground connection	**Connection mandatory**

9 Maximum ratings

Table 5. Maximum ratings

All voltages are with respect to ground, unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Description (Rating)	Min	Max	Unit
Voltage ratings				
VPRE_BT	DC voltage at VPRE_BT pin	-0.3	45.5	V
GPIO1, GPIO2, FS1B, FS0B, VMONEXT, VMONCORE, VMONPRE, WAKE1, WAKE2, VPRE_SW, VBST_FB	DC voltage at GPIO1, GPIO2, FS1B, FS0B, VMONEXT, VMONCORE, VMONPRE, WAKE1, WAKE2, VPRE_SW, VBST_FB pins	-0.3	40	V
BATSENSE	DC voltage at BATSENSE pin with -10 mA maximum reverse current (recommended 5.1 kΩ serial resistor)	-18.0	40	V
TRK1, TRK2, VSUP, VSUP_PWR	DC voltage at TRK1, TRK2, VSUP_PWR, VSUP pins	-1.2	40	V
CORE_BT	DC voltage at CORE_BT pin	-0.3	12.5	V
DEBUG	DC voltage at DEBUG pin	-0.3	10	V
TRKIN, LDOIN, CORE_IN, VPRE_FB, CORE_SW	DC voltage at TRKIN, LDOIN, CORE_IN, VPRE_FB, CORE_SW pins	-0.3	8.5	V
VBOS	DC voltage at VBOS pin	-0.3	5.6	V
VREF, LDO2OUT, LDO1OUT, RSTB, FCCU1, FCCU2, VDDIO, INTB, MISO, MOSI, SCLK, CSB, AMUX, CORE_FB, VBST_ISH, VBST_ISL, VBST_G, VBST_PG	DC voltage at VREF, LDO2OUT, LDO1OUT, RSTB, FCCU1, FCCU2, VDDIO, INTB, MISO, MOSI, SCLK, CSB, AMUX, CORE_FB, VBST_ISH, VBST_ISL, VBST_G and VBST_PG pins	-0.3	5.5	V
VDIG	DC voltage at VDIG pin	-0.3	2	V
GNDFS, GND, GNDSUB, EP	DC voltage at GNDFS, GND, GNDSUB pins, and exposed pad (EP)	-0.3	0.3	V
WAKE1, WAKE2, GPIO1, GPIO2	DC maximum reverse current at WAKE1, WAKE2, GPIO1, GPIO2 pins	-5	—	mA

10 Electrostatic discharge

Table 6. ESD

All voltages are with respect to ground, unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Description (Rating)	Min	Max	Unit
ESD ratings				
Human body model: AEC-Q-100 Rev H.				
V_{ESD_HBM}	All pins	-2.0	2.0	kV
Charged device model: AEC-Q-100 Rev H				
V_{ESD_CDM1}	All pins	-500	500	V
V_{ESD_CDM2}	Corner pins	-750	750	V
Gun Test				
V_{ESD_CDT1}	ESD - GUN discharged contact test 330 Ω/150 pF unpowered according to IEC61000-4-2 Global pins (VSUP_PWR, VSUP, FS0B, FS1B, TRK1, TRK2, GPIO1, GPIO2, WAKE1, WAKE2)	-8	8	kV
V_{ESD_CDT2}	ESD - GUN discharged contact test 2 kΩ/150 pF unpowered according to ISO10605.2008 Global pins (VSUP_PWR, VSUP, FS0B, FS1B, TRK1, TRK2, GPIO1, GPIO2, WAKE1, WAKE2)	-8	8	kV
V_{ESD_CDT3}	ESD - GUN discharged contact test 2 kΩ/330 pF powered according to ISO10605.2008 Global pins (VSUP_PWR, VSUP, FS0B, FS1B, TRK1, TRK2, GPIO1, GPIO2, WAKE1, WAKE2)	-8	8	kV
V_{ESD_CDT4}	ESD - GUN discharged contact test 330 Ω/150 pF powered according to ISO10605.2008 Global pins (VSUP_PWR, VSUP, FS0B, FS1B, TRK1, TRK2, GPIO1, GPIO2, WAKE1, WAKE2)	-8	8	kV
V_{ESD_CDT5}	Operating ESD - GUN discharged contact test 330 Ω/150 pF powered according to ISO10605.2008 Global pins (GND, BATSENSE, FS0B, FS1B). Criteria: CLASS A	-8	8	kV

11 Thermal ratings

Table 7. Temperatures ranges

Symbol	Description	Min	Typ	Max	Unit
T_A	Ambient temperature	-40	—	125	°C
T_J	Junction temperature	-40	—	150	°C
T_{STG}	Storage temperature	-55	—	150	°C
T_{WARN}	Temperature warning threshold to set TWARN_S bit	145	155	170	°C

Table 8. Thermal resistance (per JEDEC JESD51-2)

Symbol	Description	Value	Unit
$R_{\theta JA}$	Thermal resistance Junction to Ambient[1]	25	°C/W
$R_{\theta JCBOTTOM}$	Thermal resistance Junction to Case Bottom[2][3] (with uniform power dissipation on the silicon die)	1.7	°C/W
$R_{\theta JCTOP}$	Thermal resistance Junction to Case Top[1]	13.5	°C/W
Ψ_{JT}	Thermal characterization parameter Junction to Top[4]	0.8	°C/W

[1] Determined in accordance to JEDEC JESD51-2A natural convection environment. Thermal resistance data in this report is solely for a thermal performance comparison of one package to another in a standardized specified environment. It is not meant to predict the performance of a package in an application-specific environment.
[2] Thermal resistance between the die and the printed circuit board. Board temperature is measured on the top surface of the board near the package.
[3] For exposed pad packages where the pad would be expected to be soldered, junction to case thermal resistance is a simulated value from the junction to the exposed pad without contact resistance.
[4] Thermal test board meets JEDEC specification for this package (JESD51-7).

12 EMC compliance

The FS26 EMC performance is verified against BISS generic IC EMC Test Specification version 2.0 from 07.2012 and FMC1278 Rev3 Electromagnetic Compatibility Specification for Electrical/Electronic Components and Subsystems from 2018. For performance results and specific conditions, refer to the FS26 webpage.

13 Supply voltage and operating range

13.1 Supply voltage

Depending on the chosen front-end voltage regulator (VPRE or VBST), the FS2630 can support two different supply voltage ranges.

If VBST is chosen to be the front-end DCDC converter (directly connected to the battery), the supply voltage of the FS2630 can go down to voltage levels typical of a cold-crank event. Because of this, the FS2630 can still provide all available regulated voltages, even when the battery line drops below the VPRE output voltage. In this case, the supply voltage operating range is extended to V_{BST_IN} range.

When VPRE is chosen to be the first DCDC converter connected to the battery, the FS2630 is unable to provide power rails when the supply voltage is below the V_{PRE_IN} minimum limit. This topology can be used in applications where $V_{SUP\_PWR} > V_{PRE\_PWM} + V_{PRE\_HDR}$, avoiding degraded operation (drop-out mode). Note that there is a drop between V_{BAT} and V_{SUP}. VSUP_UVTH_OTP = 1 is then mandatory.

If an application requires voltages above the VPRE output voltage, the boost controller can be used to generate these voltages. In this case, the supply voltage operating range is narrowed down to the V_{PRE_IN} voltage range.

The VSUP pin voltage V_{SUP} is monitored to avoid erratic startup and shutdown of the FS2630. Specific voltage thresholds are implemented with hysteresis. When V_{SUP} is rising, the FS2630 does not start until the V_{SUP} crosses the V_{SUP_UVH} threshold. If V_{SUP} goes below V_{SUP_UVL} before the end of the power-up sequence, the device will restart. Once the power-up sequence is finished and the device is in *normal mode*, V_{SUP_UVL} has no effect.

The VSUPUV6_I SPI bit can notify the system that the input voltage of the FS2630 is decreasing, indicating that V_{SUP} has crossed the V_{SUP_UV6} voltage threshold.

Table 9. Electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. $V_{SUP\_UVH} < V_{SUP} < 36$ V, $V_{PRE\_PWM} + V_{PRE\_HDR} < V_{SUP\_PWR} < 36$ V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
V_{SUP}	Device input supply voltage (on VSUP pin)	V_{SUP_UVL}	12	36	V
V_{SUP_PWR}	Device input supply voltage (on VSUP_PWR pin)	V_{PRE_IN}	12	36	V
V_{SUP_OV}	Threshold voltage to latch the interrupt VSUPOV_I (on VSUP pin)	19.3	20	20.7	V
V_{SUP_UV6}	Threshold voltage to latch the interrupt VSUPUV6_I (on VSUP pin)	5.8	6.0	6.2	V
V_{SUP_UVH}	V_{SUP} undervoltage threshold (rising edge on VSUP pin) VSUP_UVTH_OTP = 0 (recommended for VBST in front-end configuration) VSUP_UVTH_OTP = 1 (mandatory for VBST in back-end configuration or not used)	 4.6 5.95	 4.8 6.1	 5.0 6.25	V
V_{SUP_UVL}	V_{SUP} undervoltage threshold (falling edge on VSUP pin) VSUP_UVTH_OTP = 0 (recommended for VBST in front-end configuration) VSUP_UVTH_OTP = 1 (mandatory for VBST in back-end configuration or not used)	 4.1 5.5	 4.3 5.65	 4.5 5.8	V
V_{PRE_UVH}	V_{PRE} undervoltage threshold high (rising edge on VPRE pin)	2.9	3.0	3.1	V
V_{PRE_UVL}	V_{PRE} undervoltage threshold low (falling edge on VPRE pin)	2.5	2.6	2.7	V
V_{PRE_UVBOS}	V_{PRE} undervoltage threshold to switch VBOS from VPRE to VSUP when BOS_IN_OTP[1:0] = 0	3.4	3.55	3.7	V

13.2 Operating range

FS2630 operation range is divided in subranges with its own specificities:

- **No Operation** means the device is not providing the expected functionality or is shut down.
- **Low Voltage Extended Operation** means the device remains functional but with reduced electrical performance.
  - VPRE may be in drop out mode. VPRE output voltage may decrease below its nominal value and the transient load will be degraded.
- **Full Operation** means the device is providing the expected functionality with full electrical performance within the limits of the data sheet and within the operating mission profile of the safety manual.
- **High-voltage Extended Operation** means the device is providing the expected functionality with full electrical performance within the limits of the data sheet but for a limited period of time. This could occur during load dump or double-battery jump-start events, for example.
- **Electrical Characteristics not guaranteed** means the device remains functional, but with reduced electrical performance.
  - In Low Power mode, the quiescent current will increase.
  - In *normal mode*, the VPRE thermal limitation may trigger the thermal shutdown. VPRE transient load will be degraded.
- **Risk of damage** means the device is overstressed, with a risk of damage to the device.

The ranges are shown in Figure 8 and Figure 9.

13.2.1 Operating range in Normal mode

The FS2630 device supports two distinct topologies for boost converter configuration, giving two distinct operating ranges for the input voltage. When the boost is used as a front-end regulator, a wider input supply range is supported. When the boost is used as a back-end regulator or is not used, V_{SUP} and V_{SUP_PWR} must to be V_{PRE_HDR} higher than the VPRE output voltage V_{PRE} (V_{PRE_PWM} and / or V_{PRE_PFM}) to ensure full parametric operation.

Figure 8 describes the supply range of the FS2630 with or without the boost used as a front-end or back-end regulator. Front-end topology should be used to support cold-crank events on the battery input. In the back-end configuration, full operation is guaranteed when V_{SUP} is higher than V_{PRE_PWM} + V_{PRE_HDR}. (See Section 20.2 for V_{PRE_HDR}).

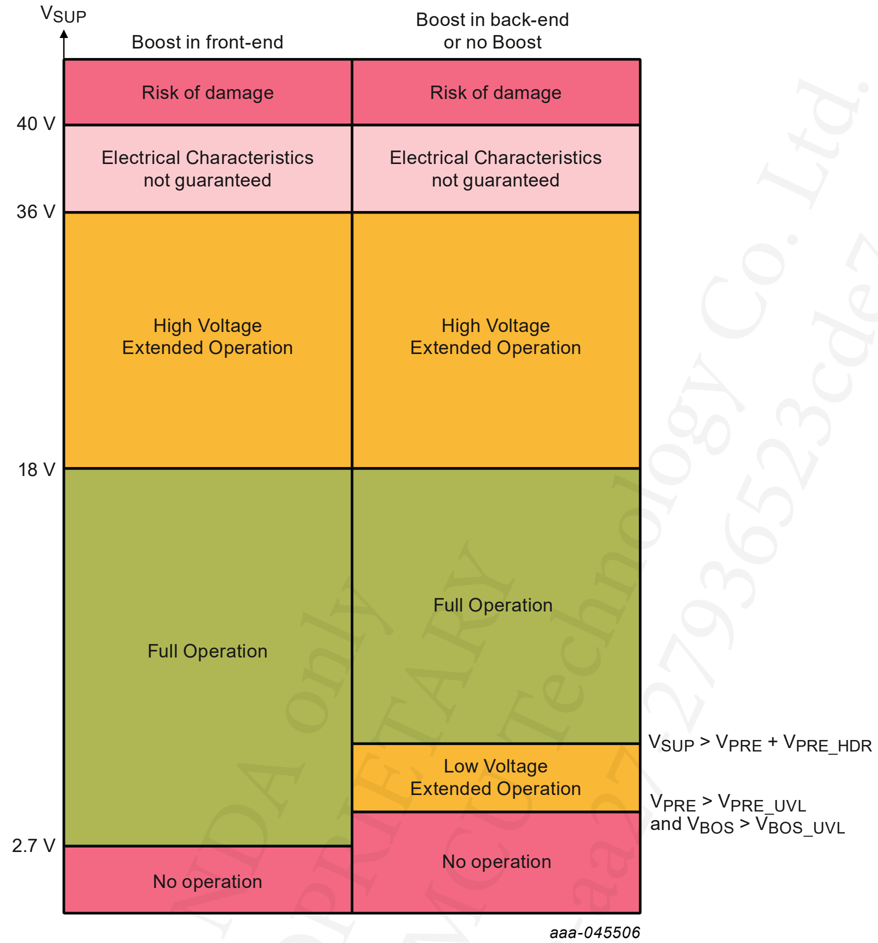

Figure 8. Input voltage range in *normal mode* (legend)

13.2.2 Operating range in Low Power modes

In *standby mode* and *LPOFF mode*, monitors are disabled to ensure lowest current consumption. The minimum operating condition is V_{BOS_POR}.

Figure 9 describes the supply range of the FS2630 in *standby mode* and *LPOFF mode*. When transitioning to *standby mode*, the boost regulator will be turned off and VPRE will switch from VPRE_OTP[5:0] to VPRE_LP_OTP[5:0].

When the device is in *LPOFF mode*, all the regulators are turned off.

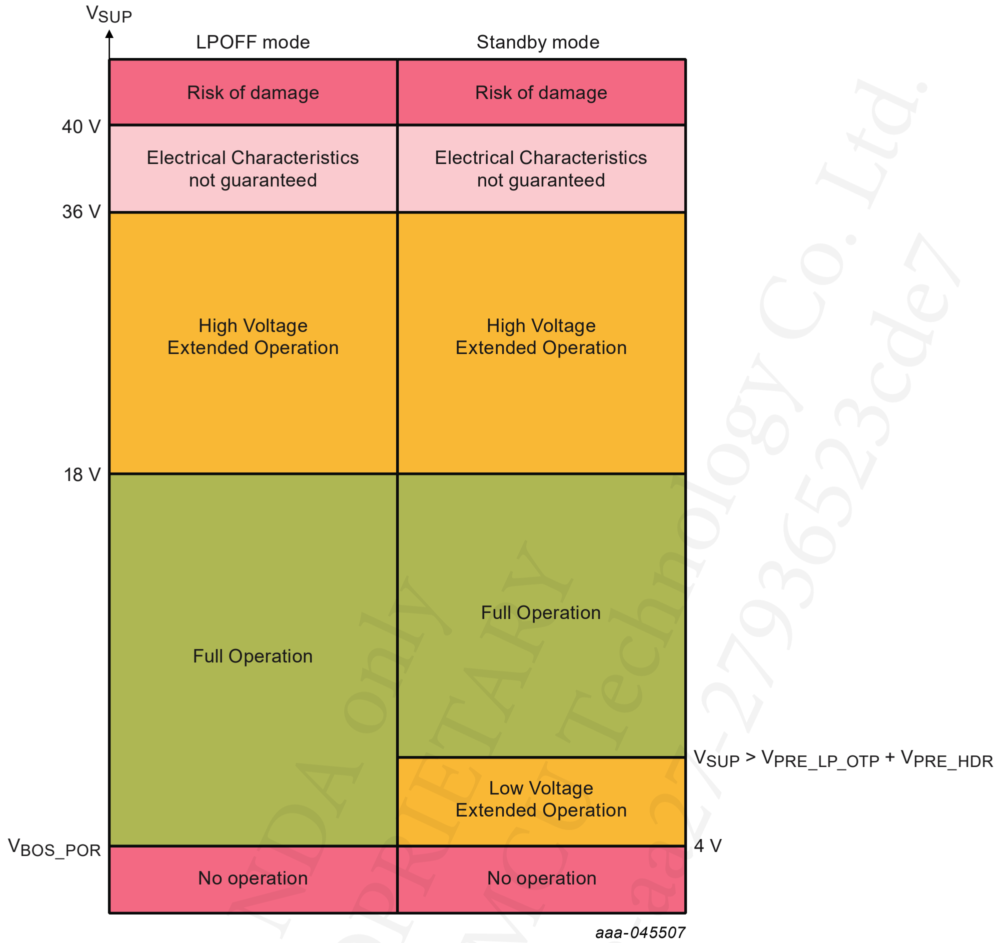

Figure 9. Input voltage range in *standby mode* and *LPOFF mode* (legend)

14 Current consumption

Table 10. Electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < V_{SUP} < 36 V, V_{PRE_PWM} + V_{PRE_HDR} < V_{SUP_PWR} < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Quiescent current					
I_{Q_NORMAL}	Current consumption in *normal mode* on the battery: • V_{SUP} = V_{SUP_PWR} = 13.5 V (including current from BATSENSE pin) • VBST enabled but not switching. • VPRE output voltage set at 5.5 V • L_{PRE} = 10 µH • VCORE enabled and output voltage set at 1.5 V • LDO1 enabled and output voltage set at 5.0 V • LDO2 enabled and output voltage set at 3.3 V • TRK1 and TRK2 enabled and output voltage set at 5 V • VREF enabled and output voltage set at 5 V • Long Duration Timer enabled • All regulators output current = 0 A		15	25	mA
I_{Q_STBY}[1]	Current consumption in *standby mode* on the battery • T_A = 25 °C • T_A = 40 °C[2] • T_A = 85 °C[2] • V_{SUP} = V_{SUP_PWR} = 12 V, 18 V (including current from BATSENSE pin) • V_{PRE_PFM} = 3.7 V (PFM mode) • L_{PRE} = 10 µH • LDO1 enabled, V_{LDO1} = 3.3 V • LDO2 disabled. Typ 3 µA additional on V_{SUP} when enabled at 3.3 V • Long Duration Timer disabled, < 1 µA when enabled. • GPIOx disabled in standby • RSTB released, pulled up to V_{PRE_PFM} • FS0B = 0 and FS1B = 0 pulled up to a disabled supply in *standby mode*.		32 36 40	— — 60	µA
I_{Q_STBY}	Current consumption in *standby mode* on the battery • T_A = 25 °C • T_A = 85 °C[2] • V_{SUP} = V_{SUP_PWR} = 5.4 V (including current from BATSENSE pin) • V_{PRE_PFM} = 3.7 V and 5.05 V (PFM mode) • L_{PRE} = 10 µH • LDO1 enabled, V_{LDO1} = 3.3 V when V_{PRE_PFM} = 3.7 V, V_{LDO1} = 5.0 V when V_{PRE_PFM} = 5.05 V. • LDO2 disabled. Typ 3 µA additional on V_{SUP} when enabled at 3.3 V • Long Duration Timer disabled. < 1 µA when enabled. • GPIOx disabled in standby • RSTB released, pulled up to V_{PRE_PFM} • FS0B = 0 and FS1B = 0 pulled up to a disabled supply in *standby mode*.		90 110	— 130	µA
I_{Q_LPOFF}, I_{Q_DFS}	Current consumption in *LPOFF mode* and *Deep Fail Safe* (DFS) state on the battery • T_A = 25 °C • T_A = 40 °C[2] • T_A = 85 °C[2] • V_{SUP} = V_{SUP_PWR} = 5.4 V, 12 V, 18 V • (Including current from BATSENSE pin) • All regulators are disabled. • Long Duration Timer disabled. < 1 µA when enabled. • GPIOx disabled in LPOFF		30 32 40	— — 60	µA

[1] VBAT current is reduced in *standby mode* due to the ratio between VBAT and VPRE voltages.
[2] Guaranteed by characterization. Tested in production at 25 °C only.

14.1 Total battery current consumption estimation in Standby mode

The *standby mode* current consumption can be estimated using Figure 10 and Figure 11 at T_A = 25 °C and T_A = 85 °C, depending on the use case. The measurements were made with the following assumptions:

- V_{SUP} = V_{SUP_PWR} = 12 V.
- L_{PRE} = 10 μH
- Long Duration Timer disabled.
- GPIOx disabled in standby.
- RSTB released and pulled up to VPRE.
- FS0B = 0 and FS1B = 0, pulled up to a disabled supply in *standby mode*.
- All regulators unloaded.

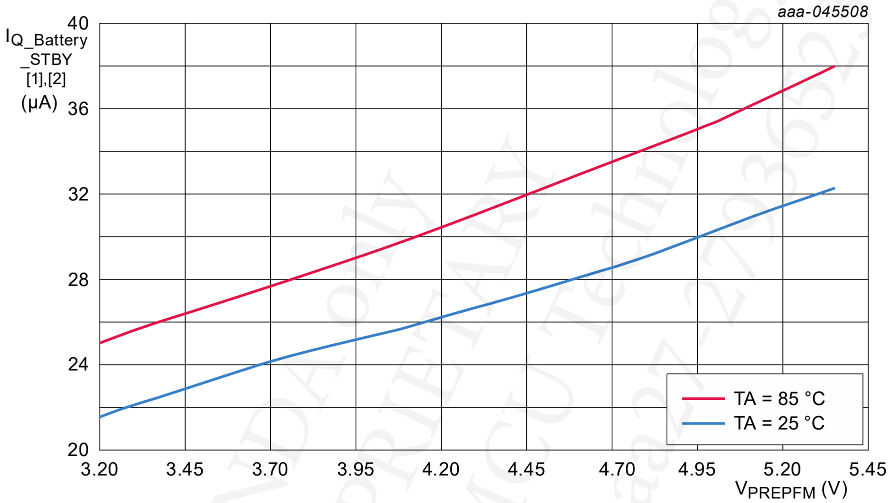

Figure 10. Battery current consumption in standby mode (LDO1 and LDO2 disabled)

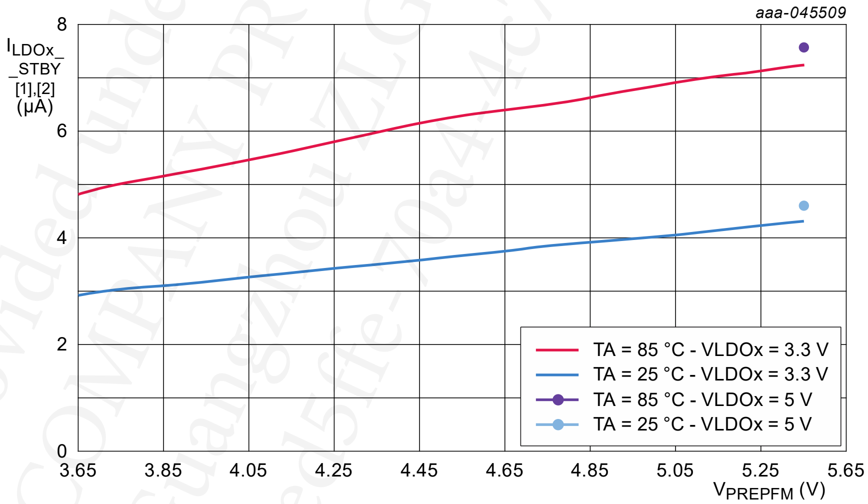

Figure 11. LDOx current consumption in standby mode

When LDOx is used at 5 V, VPRE output voltage in *standby mode* must be 5.35 V to comply with the LDOx minimum dropout voltage. [1 2]

1 In *standby mode* VBAT current is reduced, due to the ratio between VBAT and VPRE voltages.

The total *standby mode* current consumption can be estimated at either T_A = 25 °C or T_A = 85 °C using the following formula:

$$I_{Q\_Total\_Battery\_STBY} (\mu A) = I_{Q\_Battery\_STBY} + I_{LDOx\_STBY} \times N$$

where N is the number of LDOx used.

14.2 *Standby mode* current consumption

In most cases, LDO1 or LDO2 regulators are used in *standby mode* to supply light loads.

The total battery current consumption can be estimated using Figure 12 at T_A = 25 °C and T_A = 85 °C, depending on the LDO1 or LDO2 load. The measurements have been done with the following assumptions:

- V_{SUP} = V_{SUP_PWR} = 12 V.
- L_{PRE} = 10 µH
- Long Duration Timer disabled.
- GPIOx disabled in standby.
- RSTB released and pulled up to VPRE.
- FS0B = 0 and FS1B = 0, pulled up to a disabled supply in *standby mode*.
- LDO1 and LDO2 enabled.
- V_{LDO1} = 3.3 V, V_{LDO2} = 5 V and V_{PRE_PFM} = 5.35 V.
- No external load on VPRE.

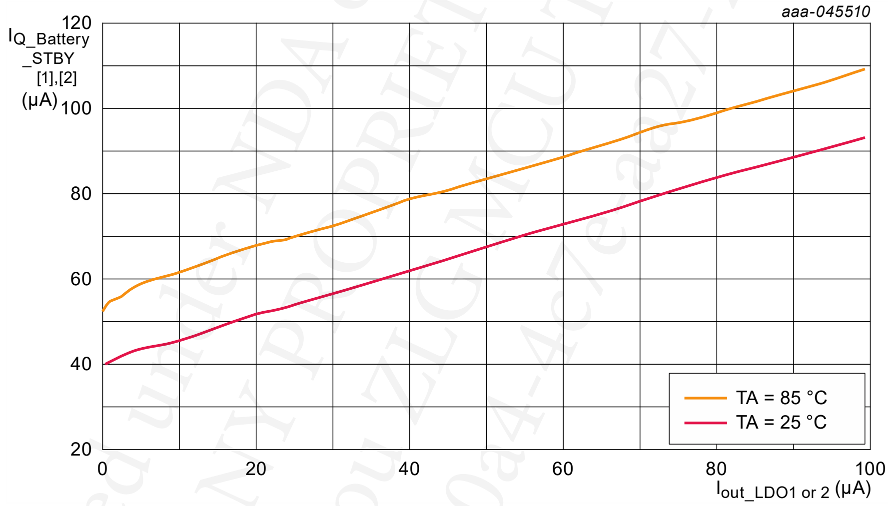

Figure 12. Total battery current consumption in *standby mode*

The total battery current consumption can also vary depending on the chosen inductor for L_{PRE}. Below additional measurements have been done with the following assumptions:

- Long Duration Timer disabled
- GPIOx disabled in standby
- RSTB released and pulled up to VPRE
- V_{SUP} = V_{SUP_PWR} = 12 V
- FS0B asserted, FS1B pulled up to a disabled supply in *standby mode*
- LDO1 and LDO2 disabled

2 Guaranteed by characterization. Tested in production at 25 °C only.

- V_{PRE_PFM} = 5.35 V or 3.7 V
- No external load on VPRE

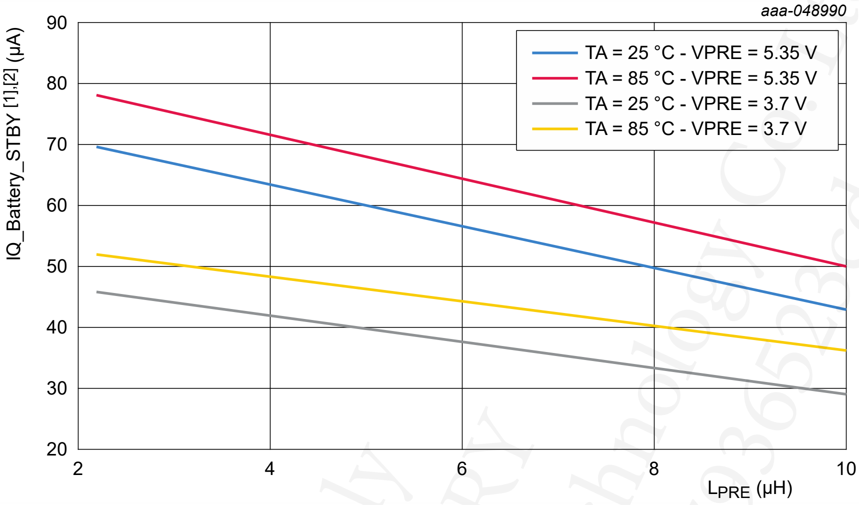

Figure 13. Battery current consumption in *standby mode* with V_{PRE_PFM} = 3.70 V or 5.35 V and LDOx disabled

15 General device operation

15.1 Simplified functional state diagram

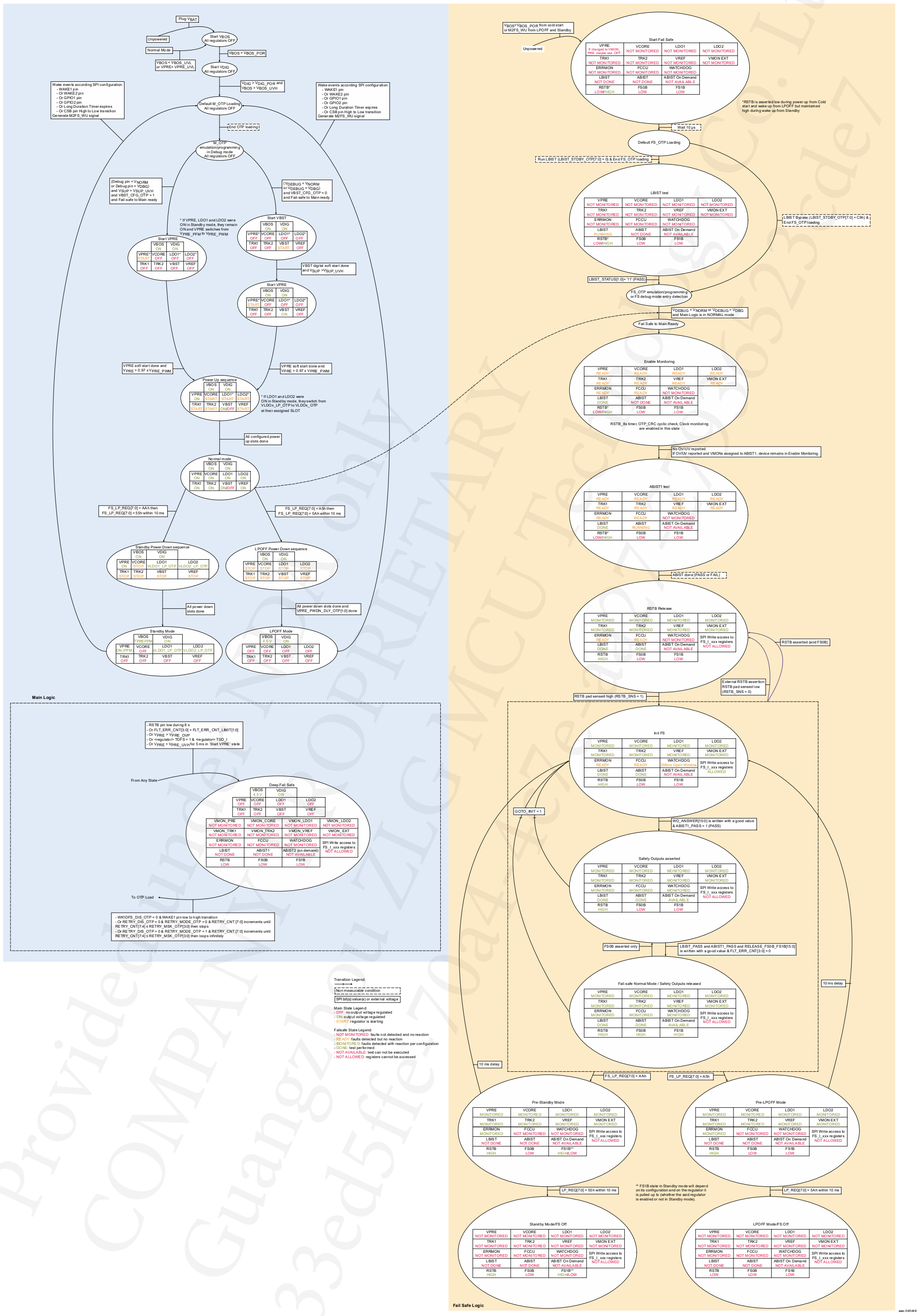

Figure 14. Simplified functional state diagram

15.2 Functional device operation and power modes

FS2630 operation is divided in two independent logic blocks to achieve best in class functional safety coverage. The main state machine manages the power management, the Low Power modes, and the wake-up sources while the fail-safe state machine manages the monitoring of the power management, the monitoring of the microcontroller and the monitoring of an external IC with ERRMON.

The FS2630 provides three main operating modes:

- ***Normal mode*** is intended to be the fully functional mode. All power supplies are enabled as required by the system, and all system functionality provided by the FS2630 is available. During *normal mode*, the fail-safe state machine is available and providing full monitoring and operation of all the safety features in the device.
- ***Standby mode*** is intended to be the Low Power ON mode, providing support to the minimum system requirements with low current consumption from the battery. During the *standby mode*, only the VPRE remains enabled to supply the microcontroller I/O rails. LDO1 and LDO2 can be enabled in this mode depending on the OTP configuration. GPIO1 and GPIO2 can remain at the same state as in *normal mode*, depending on the SPI configuration. *standby mode* is assumed to be a safe state with no critical activity, and therefore the fail-safe state machine is disabled to achieve minimum current consumption by the system.
- ***LPOFF mode*** is intended to be the Low Power OFF mode, with no active system supplies except GPIO1, which can remain enabled. Logic circuitry is internally supplied to allow proper wake up from any of the available wake-up mechanisms, with the minimum current consumption possible.

The system can wake up from any of the Low Power modes via any of the following selectable wake-up mechanisms available in the device (availability is dependent on part number):

- WAKE1 and WAKE2 pins
- GPIO1 and GPIO2 pins
- Long Duration Timer (LDT) expiration
- SPI activity via edge detection of the CSB pin

Table 11 summarizes the operating modes and available features:

Table 11. Operating modes summary

Operating mode	Power supply state			Wake-up sources and capabilities		
	VPRE	LDOx GPIOx	VBST, VCORE TRK1, TRK2, VREF	WAKEx, GPIOx	LDT	MCU
Normal mode	PWM, ON	ON (Optional)	ON (Optional)	N/A	N/A	N/A
Standby mode	PFM, ON	ON (Optional)	OFF	YES	YES (Optional)	YES
LPOFF mode	OFF	OFF (GPIO1 optional)	OFF	YES	YES (Optional)	NO

The FS2630 can also move to or through these two states:

- ***Load fuse*** state is a transitional state where the device loads its complete OTP configuration, previously programmed in its fuses. The Main and the Fail-safe state machines both have to go through this state when resuming from a power-up event.
- ***Deep Fail Safe*** (DFS) state is the device protection state. In this state, all regulators are OFF, **safety outputs are asserted**, the SPI interface is not accessible. The device waits for specific events to restart and to move to *load fuse* state to restart, and the safety outputs remain asserted until release conditions are met. DFS state entry can be disabled by setting MDFS_DIS_OTP = 1 and DFS_DIS_OTP = 1, transition request sources listed hereafter will be ignored, however the safety pins are asserted accordingly with fault sources and reactions configuration.

Below is an exhaustive list of conditions that put the FS2630 in *Deep Fail Safe* state:

- RSTB pin is sensed to low level for a time longer than 8 seconds.
- Too many faults occur: fault error counter reaches its programmed limit (FLT_ERR_CNT[3:0] = @FLT_ERR_CNT_LIMIT[1:0]).
- When FAULT_DFS_EN_OTP = 1 device enters *Deep Fail Safe* state as soon as RSTB or FS0B is asserted.
- VPRE output voltage crosses V_{PRE_OVP} threshold for a time longer than t_{PRE_OVP}.
- Each regulator is disabled when an over temperature event is detected, that is thermal shutdown (TSD). Additionally, the TSD event can be configured with M_TSD_CFG register to lead device to *Deep Fail Safe* state (for instance VPRETSD_I = 1 and VPRETDFS = 1).

Below is an exhaustive list of conditions that make the device leave the *Deep Fail Safe* state to *load fuse* state:

- WAKE1 event: resume if WK1DFS_DIS_OTP = 0 and WAKE1 pin is toggled from low to high or from high to low logic level.
- Infinite auto-retry mode: the FS2630 makes attempts to resume periodically and RETRY_CNT[7:0] increments every try. Once the RETRY_CNT[7:4] reaches the RETRY_MSK_OTP[3:0] value, the RETRY_CNT[7:0] time value is clamped and retries occur infinitely to the last clamped retry frequency (RETRY_MSK_OTP[3:0]) until a valid resume condition is detected. The OTP configuration to select this mode is RETRY_DIS_OTP = 0 and RETRY_MODE_OTP = 1.
- Limited auto-retry mode: the FS2630 makes attempts to resume while RETRY_CNT[7:4] is smaller than RETRY_MSK_OTP[3:0]. When the RETRY_CNT[7:4] reaches the RETRY_MSK_OTP[3:0] value, the FS2630 stays in the *Deep Fail Safe* state until a power-on reset event occurs (V_{BOS} < V_{BOS_POR}). The OTP configuration to select this mode is RETRY_DIS_OTP = 0 and RETRY_MODE_OTP = 0.

Example: the first time the device enters *Deep Fail Safe* state, it will try to exit this state every 100 ms, and RETRY_CNT[7:0] increments at each attempt. After 16 consecutive failed attempts, RETRY_CNT[7:4] increments and the counter uses the next value of 200 ms, and so on, until RETRY_CNT[7:4] = RETRY_MSK_OTP[3:0].

Note: the retry counter RETRY_CNT[7:0] is divided in two parts. RETRY_CNT[7:4] represents the timing the counter is currently using (100 ms, 200 ms, and so on) and RETRY_CNT[3:0] is the number of attempts performed at the current used timing. RETRY_CNT[7:0] can be read as the total number of attempts performed by the device since the first *Deep Fail Safe* entry.

15.3 Fail-safe state machine

The fail-safe state machine is designed to run independently from the main state machine. However, all necessary handshaking signals are provided to ensure seamless operation as a single device. These signals are protected up to 40 V to ensure the integrity of the fail-safe circuitry, keeping maximum isolation between both blocks.

During the power-up of the fail-safe state machine (from a cold boot or a wake-up event), the system performs logic built-in self-test (LBIST) on all the gates related to the functional safety operation, as well as analog built-in self-test (ABIST1) on all the analog blocks dedicated to safety monitoring and notification.

An ABIST on demand (ABIST2) can be requested through a SPI command, to allow the system to check the integrity of the safety mechanisms at any point during the *normal mode* and to detect potential latent faults when the application is running.

The RSTB is provided to inform the microcontroller that system power supplies are up and in regulation regardless of the results of the ABIST1. A configurable watchdog counter is included to ensure the microcontroller is able to communicate with the FS2630, which can react to any failure condition and place the system in a safe state.

Two safety outputs, FS0B and FS1B, are provided to keep the system in a safe state until the microcontroller acknowledges it is safe to start normal operation, or when a fault is present. When a fault is present, these outputs prevent the system from entering an unsafe state.

When the microcontroller is properly initialized, it can request to release FSxB through a SPI command to set the application to *normal mode*, with all the selected monitoring activated. The FS2630 will react by asserting the safety pins (RSTB and FSxB), according to its configuration, when a fault is detected.

15.4 Application flowchart

In an application, the debug pin is connected to ground and a watchdog refresh is required as soon as the *initialization phase* is closed. The system enters *normal mode* once the safety outputs are released. Figure 15 is a high-level flowchart illustrating entry into *normal mode* in the application.

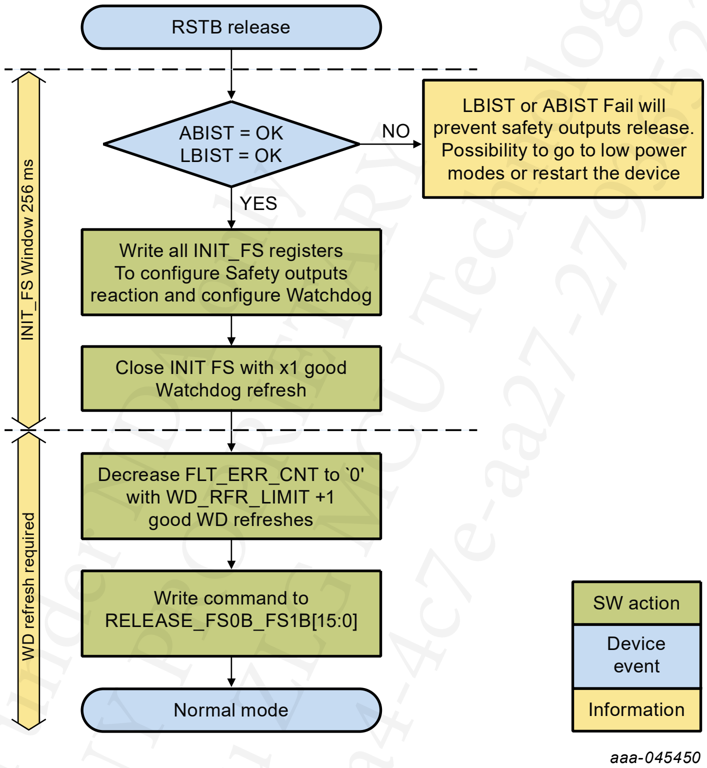

Figure 15. Application flowchart

15.5 Input power topology

The FS26 provides two input topologies to address various system needs. A reverse protection Schottky diode (D_{BAT}) between battery voltage (V_{BAT}) and the FS26 is required. Depending on the system configuration, the FS26 can obtain V_{SUP} in two main configurations:

1. The switching boost controller (VBST) can be used as the front-end supply to support system cranking events with voltage drops down to 2.7 V at the V_{BST_IN} input.
   When VBST is used as the front-end supply, the battery voltage (V_{BAT}) is applied at the input of the boost controller. During normal operation when V_{SUP} > VBST, the boost controller stops switching and operates in Pass-Through mode.

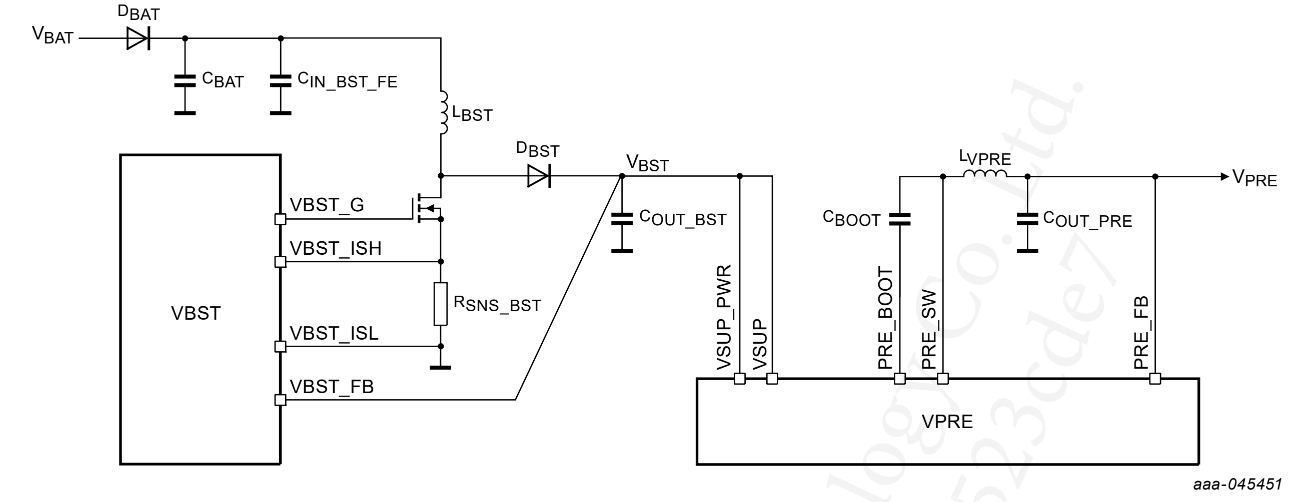

Figure 16. Input topology: front-end boost controller

When V_{SUP} < VBST, the boost controller starts switching to maintain V_{SUP} above the V_{SUP_UVH} threshold, thus ensuring system operation during crank profiles.

2. For systems with less severe or no cranking events, the input power can be applied directly to the VSUP pin. In this scenario, the FS26 can ensure functionality if $V_{SUP} > V_{PREPWM} + V_{PRE\_HDR}$ (Section 20.2 for V_{PRE_HDR}). The device will shut down if $V_{PREPWM} < V_{PRE\_UVL}$. The reverse voltage protection diode and a PI-filter are needed to guarantee optimal EMI performance.

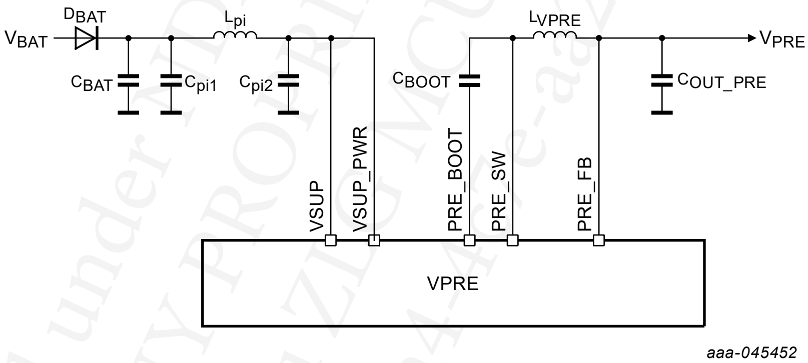

Figure 17. Input topology: direct VSUP connection

At the chip level, the power-up sequencing and operating thresholds are referenced to VSUP input. However, proper considerations should be made to ensure the system level requirements are met with respect to V_{BAT} voltage.

15.6 System power-up and power-down

When a voltage is applied to the VSUP pin, the FS26 starts its internal power-up biasing. As the internal best of supply (BOS) reaches regulation and the default OTP configuration is loaded, the system proceeds to turn on the output regulators based on the OTP configuration of the device. The regulators' power-up sequence is dependent on the input power topology used in the system:

With VBST used as the front-end supply

- VBST is enabled first and will ensure $V_{SUP} > V_{SUP\_UVH}$.

- Once V_{SUP} has crossed the V_{SUP_UVH} threshold, VPRE is enabled automatically.
- The remaining regulators will start as set in the OTP power-up sequence configuration.

Direct connection to VSUP

- Once V_{SUP} has crossed the V_{SUP_UVH} threshold, VPRE is enabled automatically.
- The remaining regulators will start in their corresponding power-up slot as set in the OTP power-up sequence configuration.

15.6.1 Regulator power-up sequence

Seven slots are available to program the startup sequence of VCORE, LDO1, LDO2, VREF, TRK1, and TRK2, as well as the GPIO1 and GPIO2 signals for external control.

The power-up sequence starts from SLOT_0 to SLOT_6, with a TSLOT_OTP[1:0] delay between each slot. RSTB is released after SLOT_6. Regulators assigned to SLOT_7 / OFF are not started during the power-up sequence and can be enabled later in *normal mode* via a SPI command. When VBST is used in back-end supply, it can only be enabled via a SPI command once the device is in *normal mode*.

Each regulator is assigned to a slot by OTP configuration using the dedicated OTP bits. Each slot is executed regardless of whether a regulator is assigned to a slot or not. Slots can be bypassed with SLOT_BYP_OTP[2:0]. A regulator assigned to a bypassed slot will not start in the power-up sequence.

When the last power-up slot is completed, monitoring of the voltages is enabled. If the soft start of a regulator is not achieved and the output voltage is still below the UV monitoring, the UV is detected and reported in the corresponding flag. Therefore, NXP recommends clearing all the UV flags at each startup during *initialization phase*.

When VCORE is enabled, the bootstrap capacitor must be charged. Therefore, the VCORE regulator output starts to ramp-up with a delay of 100 µs from the beginning of the slot.

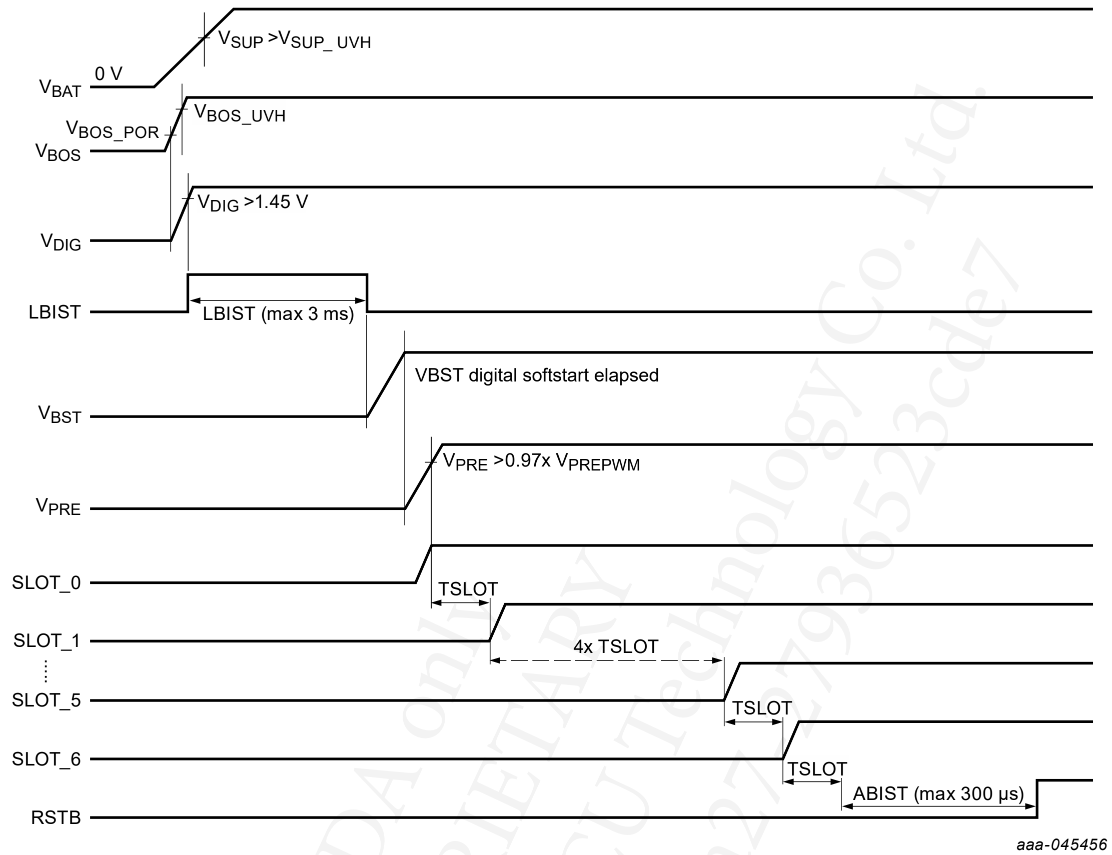

Figure 18. Power-up example with VBST as front-end supply

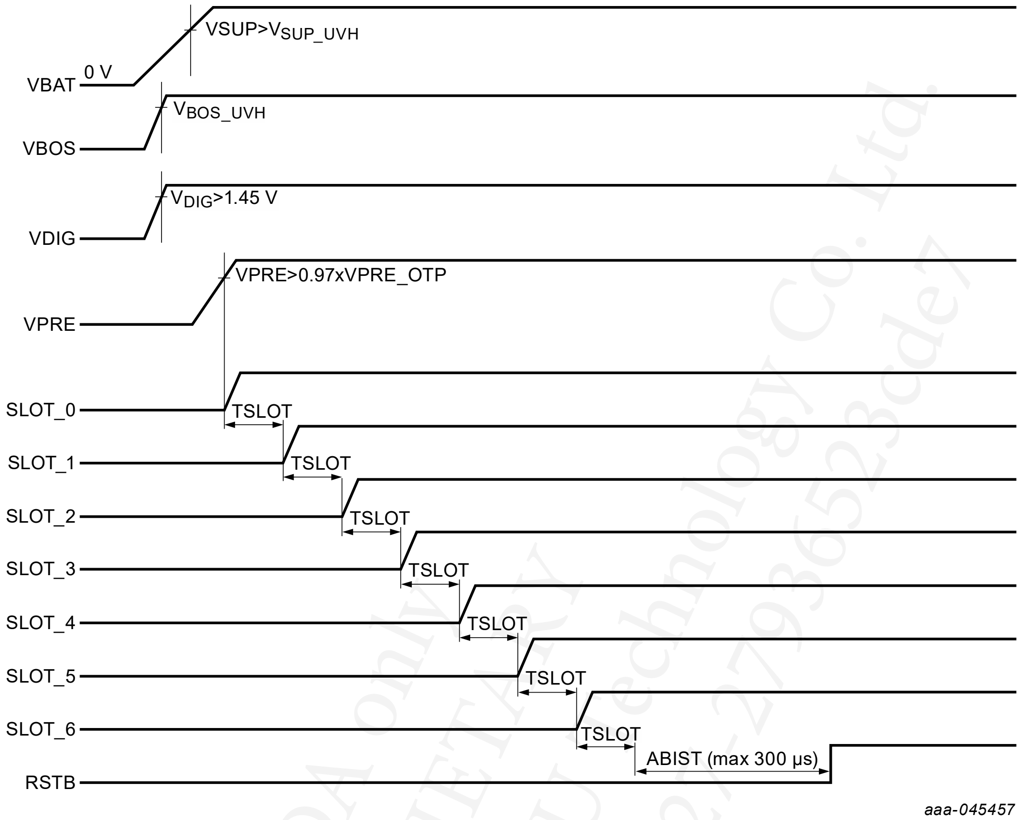

Figure 19. Power-up example with direct battery supply

To reduce the power-up timing, SLOT_BYP_OTP[2:0] setting is provided to bypass the unused slots. Devices slots jumps from the slot @SLOT_BYP_OTP[2:0] to *normal mode*, bypassing SLOT_X to SLOT_6.

Once the power-up sequence is completed, the Main state machine is in *normal mode*, which is the application running mode with all the regulators ON.

15.6.2 System power-down sequence

During a power-down event, the device uses the same slot bits to turn off the voltage regulators, in reverse order from the power-up sequence.

If a slot bypass configuration is enabled, the device will start the power-down sequence from the selected slot in the OTP configuration.

When powering down to the *standby mode*, VPRE remains enabled. LDO1 and LDO2 can be programmed to also remain enabled during the *standby mode*. GPIO1 and GPIO2 can also remain in the same state that they were in, in *normal mode*. All other regulators are disabled as defined by the slot bits.

When powering down into the *LPOFF mode*, all voltage regulators are disabled as described in the power-down sequence. Once the voltage regulators in the sequencer are disabled, the VPRE will start powering off, followed by the VBST if it is used as the front-end supply.

If VBST is used in back-end mode, the regulator will be turned off in the first power-down slot.

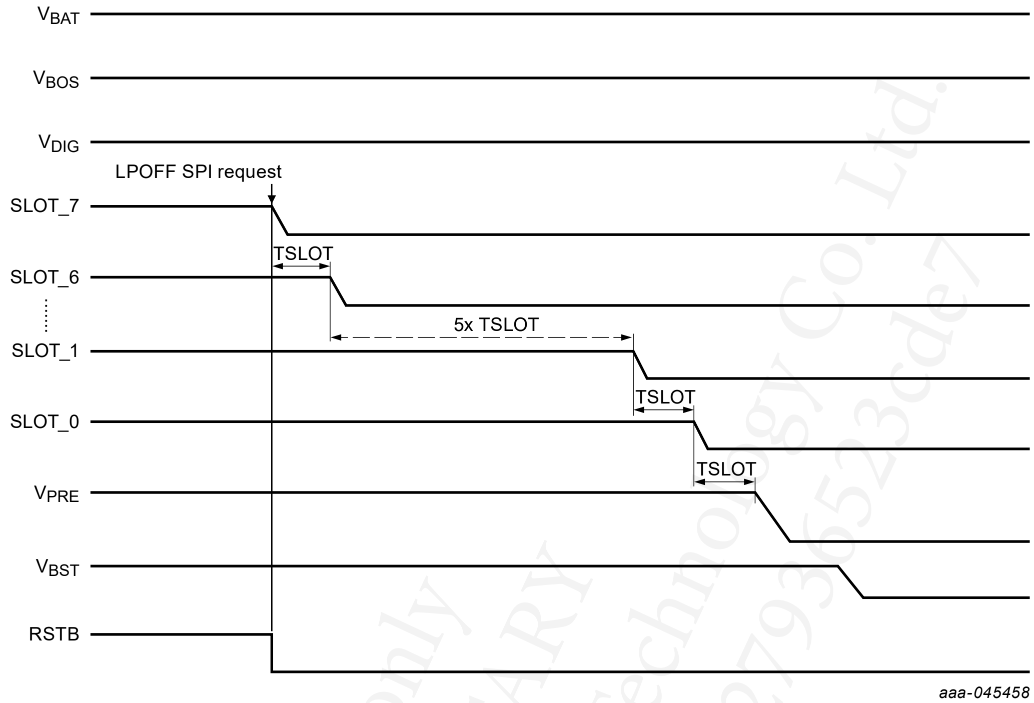

Figure 20. Power-down example with VBST as front-end supply

15.7 Wake-up sources

The FS26 has several selectable wake-up sources from the Low Power modes:

- WAKEx pin:
  - The WAKEx pins can be configured to detect wake-up events internal or external to the ECU.
  - The WAKEx pins can detect wake-up event on high level or low level.
- GPIOx pin:
  - The GPIOx pins can be configured as inputs to detect wake-up events internal to the ECU.
  - The GPIOx pins can detect wake-up event on high level or low level.
- SPI chip select wake-up (only when VDDIO is supplied):
  - When the SPI wake up is enabled, the device wakes up with any activity on the SPI bus (transition from high to low of CSB pin).
  - In case of a SPI wake up, the first SPI command is ignored, and the FS26 will be able to respond to the subsequent SPI commands after 1.5 ms.
- Long Duration Timer (LDT) expired:
  - Wake up from the LDT is available (part number dependent).
  - When the LDT is enabled, it can be configured to generate a wake-up event when the timer expires. This feature allows the system to perform cyclic system verifications while it is in the Low Power mode.

15.8 SPI communication

The FS2630 uses a 32-bit SPI, with the following arrangement:

MOSI (Main Out, Secondary In) bits:

- Bit 31: Main or fail-safe registers selection
- Bit 30 to 25: Register address

- Bit 24: Read/Write (For reading Bit 24 = 0; For writing Bit 24 = 1)
- Bit 23 to 8: Control bits
- Bit 7 to 0: Cyclic redundant check (CRC)

MISO (Main In, Secondary Out) bits:

- Bit 31-24: General device status
- Bits 23 to 8: Extended device status, or device internal control register content or device flags (see Table 13)
- Bit 7 to 0: Cyclic redundant check (CRC)

The digital SPI pins (CSB, SCLK, MOSI, MISO) are referenced to VDDIO.

The MCU is the primary driving MOSI and FS2630 is the secondary driving MISO. The MISO data is latched at the SCLK rising edge and MOSI data is latched at the SCLK falling edge, MSB first. In a write command, MISO[23:8] bits are the previous register bits and MISO[7:0] is the CRC of the message sent by the FS2630. In a read command, MOSI[23:8] bits are all 0 and MOSI[7:0] is the CRC of the message sent by the MCU. Figure 21 and Figure 22 describe the SPI communication protocol for writing data into the FS2630 or reading data from the FS2630.

The FS_EN bit is set high as soon as the fail-safe state machine enters Enable monitoring state. The bit remains enabled during the normal operation until the system has successfully moved into any of the low power states.

In all other states, FS_EN = 0.

The M_AVAL bit is set high as soon as the main state machine is in *normal mode* state. In all other states, this bit is set to 0.

	B31	B30	B29	B28	B27	B26	B25	B24	B23 B22 B21 B20 B19 B18 B17 B16	B15 B14 B13 B12 B11 B10 B9 B8	B7 B6 B5 B4 B3 B2 B1 B0
MOSI	M/FS	REG_ADDRESS [5:0]						R/W	DATA_MSB[7:0]	DATA_LSB[7:0]	CRC[7:0]
MISO	M_AVAL	FS_EN	FS_G	COM_G	WIO_G	VSUP_G	REG_G	TSD_G			CRC[7:0] - response

aaa-045511

Figure 21. SPI write operation protocol

	B31	B30	B29	B28	B27	B26	B25	B24	B23 B22 B21 B20 B19 B18 B17 B16	B15 B14 B13 B12 B11 B10 B9 B8	B7 B6 B5 B4 B3 B2 B1 B0
MOSI	M/FS	REG_ADDRESS [5:0]						R/W			CRC[7:0]
MISO	M_AVAL	FS_EN	FS_G	COM_G	WIO_G	VSUP_G	REG_G	TSD_G	READ_DATA_MSB[7:0]	READ_DATA_LSB[7:0]	CRC[7:0] - response

aaa-045512

Figure 22. SPI read operation protocol

Table 12. MOSI general bit description

Bit	Symbol	Description	
31	M/FS	**Device domain access**	
		0	Main domain register map
		1	Fail-safe domain register map
30 to 25	REG_ADDESS[5:0]	**Register address**	
		See Table 16 for main domain register mapping See Table 17 fail-safe domain register mapping	
24	R/W	**Operation requested**	
		0	Read
		1	Write
23 to 8	DATA[15:0]	**Register data**	

Table 12. MOSI general bit description*...continued*

Bit	Symbol	Description
7 to 0	CRC[7:0]	**Cyclic redundancy check data sent by MCU**

Table 13. MISO general device status bit descriptions

Bit	Symbol	Description	
31	M_AVAL	**Main state machine availability**	
		0	Not available (the main state machine is not in *normal mode*)
		1	Available and able to respond (the main state machine is in *normal mode*)
		Reset on power-on reset (POR_M)	
30	FS_EN	**Fail-safe state machine status**	
		0	Fail-safe state machine is not available.
		1	Fail-safe state machine is available and able to respond
		Reset on power-on reset (POR_M)	
29	FS_G	**Event notification from the fail-safe domain**	
		0	No event reported in the fail-safe domain
		1	Event reported in the fail-safe domain
		Reset on power-on reset (POR_M), cleared when all individual bits are cleared	
		Flags Reporting: VPRE_OV, VPRE_UV, CORE_OV, CORE_UV, LDO1_OV, LDO1_UV, LDO2_OV, LDO2_UV, TRK1_OV, TRK1_UV, TRK2_OV, TRK2_UV, REF_OV, REF_UV, EXT_OV, EXT_UV, BAD_WD_DATA, BAD_WD_TIMING, FCCU12, FCCU1, FCCU2, ERRMON, ABIST1_PASS, ABIST2_PASS, LBIST_STATUS[1:0]	
28	COM_G	**Event notification from the M_COM_FLG or FS_DIAG_SAFETY1 registers**	
		0	No event reported in M_COM_FLG or FS_DIAG_SAFETY1 registers
		1	Event reported in the M_COM_FLG or FS_DIAG_SAFETY1 registers
		Reset on power-on reset (POR_M), cleared when all individual bits are cleared	
		Source Register: M_COM_FLG	
		Flags Reporting: MSPI_CRC_I, MSPI_CLK_I, MSPI_REQ_I	
27	WIO_G	**Event notification from the M_WIO_FLG register**	
		0	No event reported ino M_WIO_FLG register
		1	Event reported in the M_WIO_FLG register
		Reset on power-on reset (POR_M), cleared when all individual bits are cleared	
		Source Register: M_WIO_FLG	
		Flags Reporting: WUEVENT[3:0], LDT_I, GPIO2_I, GPIO1_I, WK2_I, WK1_I	

Table 13. MISO general device status bit descriptions*...continued*

Bit	Symbol	Description	
26	VSUP_G	**Event notification from the M_VSUP_FLG register**	
		0	No event reported in M_VSUP_FLG register
		1	Event reported in the M_VSUP_FLG register
		Reset on power-on reset (POR_M), cleared when all individual bits are cleared	
		Source Register: M_VSUP_FLG	
		Flags Reporting: VBOSUVH_I, VSUPOV_I, VSUPUV6_I, VSUPUVH_I	
25	REG_G	**Event notification from the M_REG_FLG register**	
		0	No event reported in M_REG_FLG register
		1	Event reported in the M_REG_FLG register
		Reset on power-on reset (POR_M), cleared when all individual bits are cleared	
		Source Register: M_REG_FLG	
		Flags Reporting: VBSTOV_I, VPREUVH_I, VPREOC_I, TRK2OC_I, TRK1OC_I, COREOC_I, LDO2OC_I, LDO1OC_I, VBSTOC_I	
24	TSD_G	**Event notification from the M_TSD_FLG register**	
		0	No event reported in M_TSD_FLG register
		1	Event reported in the M_TSD_FLG register
		Reset on power-on reset (POR_M), cleared when all individual bits are cleared	
		Source Register: M_TSD_FLG	
		Flags Reporting: TWARN_I, GPIO1TSD_I, VPRETSD_I, TRK2TSD_I, TRK1TSD_I, CORETSD_I, LDO2TSD_I, LDO1TSD_I	

15.8.1 Cyclic redundancy check

An 8-bit cyclic redundancy check (CRC) is required for each Write and Read SPI command. Computation of a cyclic redundancy check is derived from the mathematics of polynomial division, modulo two. The CRC polynomial used is x^8+x^4+x^3+x^2+1 (identified by 0x1D) with a SEED value of hexadecimal '0xFF'.

Figure 23 is an example of CRC encoding HW implementation:

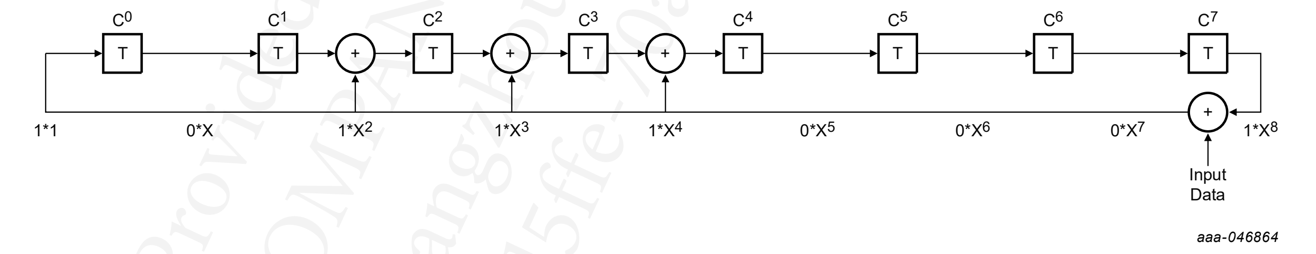

Figure 23. CRC encoder example

The effect of the CRC encoding procedure is shown in Table 14. The seed value is appended into the most significant bits of the shift register.

Table 14. Data preparation for CRC encoding

Seed	M/FS	Register Address	Read/Write	DATA_MSB	Data_LSB
0xFF	Bit[31]	Bits[30:25]	Bit[24]	Bits[23:16]	Bits[15:8]

1. Using a serial CRC calculation method, the transmitter rotates the seed and data into the least significant bits of the shift register.
2. During the serial CRC calculation, the seed and the data bits are XOR compared with the polynomial data bits. When the MSB is logic 1, the comparison result is loaded in the register, otherwise the data bits are simply shifted. It must be noted the 32-bit message to be processed must have the bits corresponding to the CRC byte all equal to zero (00000000).
3. Once the CRC is calculated, the initial CRC byte composed of zeros is replaced and the CRC is transmitted.

Procedure for CRC decoding:

1. The seed value is loaded into the most significant bits of the receive register.
2. Using a serial CRC calculation method, the receiver rotates the received message and CRC into the least significant bits of the shift register in the order received (MSB first).
3. When the calculation on the last bit of the CRC is rotated into the shift register, the shift register contains the CRC check result.

- If the shift register contains all zeros, the CRC is correct.
- If the shift register contains a value other than zero, the CRC is incorrect.

15.8.2 SPI electrical characteristics and timing diagram

Table 15. SPI Electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. $V_{SUP\_UVH} < V_{SUP} < 36$ V, $V_{PRE\_PWM} + V_{PRE\_HDR} < V_{SUP\_PWR} < 36$ V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Interface I/O input supply					
V_{DDIO}	VDDIO supply voltage range	3.0	—	5.5	V
Static Electrical Characteristics					
V_{SPI_VIL}	CSB, SCLK, MOSI low level input voltage	0.3 x V_{DDIO}	—	—	V
V_{SPI_VIH}	CSB, SCLK, MOSI high level input voltage	—	—	0.7 x V_{DDIO}	V
R_{SCLK_IPD}	SCLK internal pull-down current source	7	10	13	µA
V_{MISO_VOH}	MISO high output voltage (I = 2.0 mA)	V_{DDIO} - 0.4	—	—	V
V_{MISO_VOL}	MISO low output voltage (I = 2.0 mA)	—	—	0.4	V
I_{MISO_LEAK}	3-state leakage current (VDDIO = 5.0 V)	- 5.0	—	5.0	µA
R_{SPI_PU}	CSB, MOSI internal pull-up (pull-up to VDDIO)	190	450	800	kΩ
C_{SPI}	Input capacitor at CSB, SCLK, MOSI	—	—	10	pF

Table 15. SPI Electrical characteristics*...continued*

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < V_{SUP} < 36 V, V_{PRE_PWM} + V_{PRE_HDR} < V_{SUP_PWR} < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Dynamic Electrical Characteristics					
F_{SPI}	SPI operation frequency (50 % DC)	0.5	—	10	MHz
t_{CLH}	Minimum time SCLK = HIGH	50	—	—	ns
t_{CLL}	Minimum time SCLK = LOW	50	—	—	ns
t_{PCLD}	Propagation delay (SCLK to data at 10 % of MISO rising edge)	—	—	30	ns
t_{CSDV}	CSB = low to data at MISO active	—	—	70	ns
t_{SCLCH}	SCLK low before CSB low (setup time SCLK to CSB change H/L)	70	—	—	ns
t_{HCLCL}	SCLK change L/H after CSB = low	70	—	—	ns
t_{SCLD}	SDI input setup time (SCLK change H/L after MOSI data valid)	35	—	—	ns
t_{HCLD}	SDI input hold time (MOSI data hold after SCLK change H/L)	35	—	—	ns
t_{SCLCL}	SCLK low before CSB high	90	—	—	ns
t_{HCLCH}	SCLK high after CSB high	90	—	—	ns
t_{PCHD}	CSB L/H to MISO at high-impedance	—	—	75	ns
t_{ONCSB}	CSB min. high time	500	—	—	ns
t_{CBS_MIN}	CSB filter time	10	—	40	ns

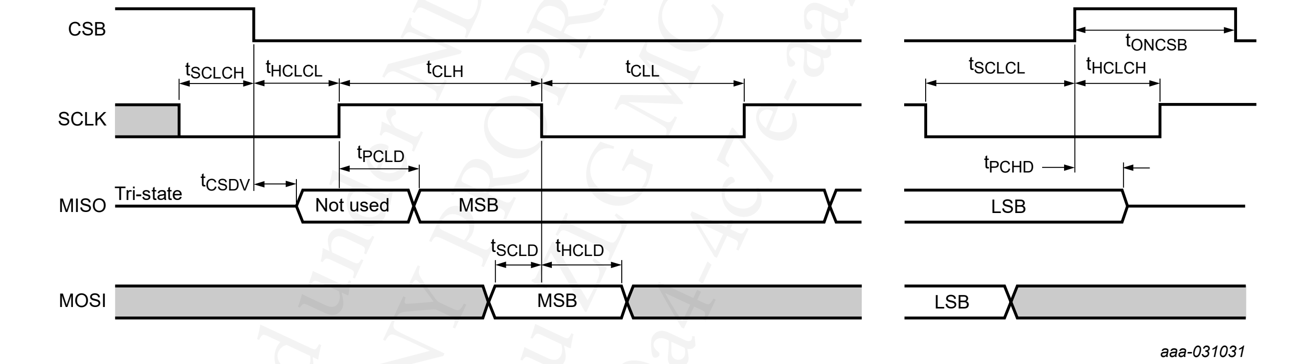

Figure 24. SPI timing diagram

16 Register mapping

16.1 Register map overview

Table 16. Main SPI register map overview

Domain	Address (Hex)	Register Name	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Main	00	Section 17.1	FULL_LAYER_REV [15:13]			METAL_LAYER_REV [12:10]			FAM_ID [9:6]				DEV_ID [5:0]					
Main	01	Section 17.2	PROG_IDH [15:8]								PROG_IDL [7:0]							
Main	02	Section 17.3	TWARN_S	VDBG_VOLT_S	VBST_ACTIVE_S	VBSTFB_UV_S	WK2_S	WK1_S	GPIO2_S	GPIO1_S	VREF_S	VBST_S	VPRE_S	TRK2_S	TRK1_S	CORE_S	LDO2_S	LDO1_S
Main	03	Section 17.4	TWARN_I	0	0	0	0	0	0	0	0	GPIO1 TSD_I	VPRETSD_I	TRK2 TSD_I	TRK1TSD_I	CORETSD_I	LDO2TSD_I	LDO1TSD_I
Main	04	Section 17.5	TWARN_M	0	0	0	0	0	0	0	0	GPIO1 TSD_M	VPRETSD_M	TRK2 TSD_M	TRK1 TSD_M	CORETSD_M	LDO2 TSD_M	LDO1 TSD_M
Main	05	Section 17.6	0	0	0	0	0	0	0	VBSTOV_I	VPREUVH_I	VBSTOC_I	VPREOC_I	TRK2OC_I	TRK1OC_I	COREOC_I	LDO2OC_I	LDO1OC_I
Main	06	Section 17.7	0	0	0	0	0	0	0	VBSTOV_M	VPREUVH_M	VBSTOC_M	VPREOC_M	TRK2 OC_M	TRK1OC_M	COREOC_M	LDO2OC_M	LDO1OC_M
Main	07	Section 17.8	0	0	0	0	0	0	0	0	0	0	0	0	VBOSUVH_I	VSUPOV_I	VSUPUV6_I	VSUPUVH_I
Main	08	Section 17.9	0	0	0	0	0	0	0	0	0	0	0	0	VBOSUVH_M	VSUPOV_M	VSUPUV6_M	VSUPUVH_M
Main	09	Section 17.10	WU_CLR	0	0	0	WUEVENT [11:8]				0	0	0	LDT_I	IO2_I	IO1_I	WK2_I	WK1_I
Main	0A	Section 17.11	0	0	0	0	0	0	0	0	0	0	0	LDT_M	IO2_M	IO1_M	WK2_M	WK1_M
Main	0B	Section 17.12	0	0	0	0	0	0	0	0	0	0	0	0	0	MSPI_CRC_I	MSPI_CLK_I	MSPI_REQ_I
Main	0C	Section 17.13	0	0	0	0	0	0	0	0	0	0	0	0	0	MSPI_CRC_M	MSPI_CLK_M	MSPI_REQ_M
Main	0D	Section 17.14	RETRY_CNT [15:8]								RETRY_CLR	0	0	INTB_TEST	INT_PWIDTH	FSS_FMOD	0	FSS_EN
Main	0E	Section 17.15	0	0	0	0	0	0	0	0	0	0	VPRETDFS	TRK2 TDFS	TRK1TDFS	CORETDFS	LDO2TDFS	LDO1TDFS
Main	0F	Section 17.16	0	0	0	0	0	0	0	0	0	0	0	0	0	0	VREF_PD	VBST_TMD
Main	10	Section 17.17	0	0	0	0	GPIO2 WUPOL	GPIO1 WUPOL	WAKE2 POL	WAKE1 POL	0	0	CSBWUEN	LDTWUEN	GPIO2 WUEN	GPIO1 WUEN	WK2WUEN	WK1WUEN
Main	11	Section 17.18	0	0	GPIO2LP_ON	GPIO1 LP_ON	0	0	GPIO2HI	GPIO1HI	VREFEN	VBSTEN	0	TRK2EN	TRK1EN	COREEN	LDO2EN	LDO1EN
Main	12	Section 17.19	0						IO2LO	IO1LO	VREFDIS	VBSTDIS	0	TRK2DIS	TRK1DIS	COREDIS	LDO2DIS	LDO1DIS
Main	13	Section 17.20	0	0	0	0	0	0	0	0	0	AMUX_EN	AMUX_DIV	AMUX [4:0]				
Main	14	Section 17.21	LDT_AFTER_RUN [15:0]															
Main	15	Section 17.22	LDT_WUP_H [15:0]															
Main	16	Section 17.23	0	0	0	0	0	0	0	0	LDT_WUP_L [7:0]							

Table 16. Main SPI register map overview*...continued*

Main	17	Section 17.24	0	0	0	0	0	0	0	0	0	LDT_FNCT [6:4]			LDT_SEL	LDT_MODE	LDT_EN	LDT_RUN
Main	18	Section 17.25	MEM0 [15:0]															
Main	19	Section 17.26	MEM1 [15:0]															

Table 17. Fail-safe SPI register map overview

Domain	Address (Hex)	Register Name	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Fail-safe	40	Section 18.1	FS_COM_G	FS_WD_G	FS_IO_G	FS_REG_OVUV_G	FS_BIST_G	0	0	0	0	0	0	0	0	0	0	0
Fail-safe	41	Section 18.2	VMON_PRE_OV_FS_REACTION		VMON_PRE_UV_FS_REACTION		VMON_CORE_OV_FS_REACTION		VMON_CORE_UV_FS_REACTION		VMON_LDO1_OV_FS_REACTION		VMON_LDO1_UV_FS_REACTION		VMON_LDO2_OV_FS_REACTION		VMON_LDO2_UV_FS_REACTION	
Fail-safe	42		NOT_VMON_PRE_OV_FS_REACTION		NOT_VMON_PRE_UV_FS_REACTION		NOT_VMON_CORE_OV_FS_REACTION		NOT_VMON_CORE_UV_FS_REACTION		NOT_VMON_LDO1_OV_FS_REACTION		NOT_VMON_LDO1_UV_FS_REACTION		NOT_VMON_LDO2_OV_FS_REACTION		NOT_VMON_LDO2_UV_FS_REACTION	
Fail-safe	43	Section 18.3	VMON_EXT_OV_FS_REACTION		VMON_EXT_UV_FS_REACTION		VMON_REF_OV_FS_REACTION		VMON_REF_UV_FS_REACTION		VMON_TRK2_OV_FS_REACTION		VMON_TRK2_UV_FS_REACTION		VMON_TRK1_OV_FS_REACTION		VMON_TRK1_UV_FS_REACTION	
Fail-safe	44		NOT_VMON_EXT_OV_FS_REACTION		NOT_VMON_EXT_UV_FS_REACTION		NOT_VMON_REF_OV_FS_REACTION		NOT_VMON_REF_UV_FS_REACTION		NOT_VMON_TRK2_OV_FS_REACTION		NOT_VMON_TRK2_UV_FS_REACTION		NOT_VMON_TRK1_OV_FS_REACTION		NOT_VMON_TRK1_UV_FS_REACTION	
Fail-safe	45	Section 18.4	WD_ERR_LIMIT		0	WD_RFR_LIMIT		0	WD_FS_REACTION		0	WD_RFR_CNT [6:4]			WD_ERR_CNT [3:0]			
Fail-safe	46		NOT_WD_ERR_LIMIT		0	NOT_WD_RFR_LIMIT		0	NOT_WD_FS_REACTION		0	NOT_WD_RFR_CNT [6:4]			NOT_WD_ERR_CNT [3:0]			
Fail-safe	47	Section 18.5	FCCU_CFG [15:13]			FCCU12_FLT_POL	FCCU1_FLT_POL	FCCU2_FLT_POL	FCCU12_FS_REACTION	FCCU1_FS_REACTION	FCCU2_FS_REACTION	0	ERRMON_FLT_POLARITY	ERRMON_ACK_TIME [4:3]		ERRMON_FS_REACTION	FCCU12_FILT [1:0]	
Fail-safe	48		NO_FCCU_CFG [15:13]			NO_FCCU12_FLT_POL	NO_FCCU1_FLT_POL	NO_FCCU2_FLT_POL	NO_FCCU12_FS_REACTION	NO_FCCU1_FS_REACTION	NO_FCCU2_FS_REACTION	1	NO_ERRMON_FLT_POLARITY	NO_ERRMON_ACK_TIME [4:3]		NO_ERRMON_FS_REACTION	NO_FCCU12_FILT [1:0]	
Fail-safe	49	Section 18.6	FLT_ERR_CNT_LIMIT [15:14]		0	FLT_ERR_REACTION [12:11]		0	RSTB_DUR	0	BACKUP_SAFETY_PATH_FS0B	0	CLK_MON_DIS	DIS8S	FLT_ERR_CNT [3:0]			
Fail-safe	4A		NO_FLT_ERR_CNT_LIMIT [15:14]		0	NO_FLT_ERR_REACTION [12:11]		0	NO_RSTB_DUR	0	NO_BACKUP_SAFETY_PATH_FS0B	1	NO_CLK_MON_DIS	NO_DIS8S	NO_FLT_ERR_CNT [3:0]			
Fail-safe	4B	Section 18.7	WDW_PERIOD				0	0	0	WDW_DC		0	0	0	WDW_RECOVERY			
Fail-safe	4C		NO_WDW_PERIOD				0	0	0	NO_WDW_DC		0	0	0	NO_WDW_RECOVERY			
Fail-safe	4D	Section 18.8	WD_ANSWER [15:0]															
Fail-safe	4E	Section 18.9	WD_TOKEN [15:0]															
Fail-safe	4F	Section 18.10	LAUNCH_ABIST2	0	0	0	0	0	0	0	ABIST2_EXT	ABIST2_REF	ABIST2_TRK2	ABIST2_TRK1	ABIST2_LDO2	ABIST2_LDO1	ABIST2_CORE	ABIST2_VPRE
Fail-safe	50	Section 18.11	VPRE_OV	VPRE_UV	CORE_OV	CORE_UV	LDO1_OV	LDO1_UV	LDO2_OV	LDO2_UV	TRK1_OV	TRK1_UV	TRK2_OV	TRK2_UV	REF_OV	REF_UV	EXT_OV	EXT_UV
Fail-safe	51	Section 18.12	RELEASE_FS0B_FS1B															

Table 17. Fail-safe SPI register map overview...*continued*

Fail-safe	52	Section 18.13	EXT_ RSTB	RSTB_ DRV	RSTB_ SNS	RSTB_ EVENT	RSTB_DIAG	RSTB_REQ	FS0B_DRV	FS0B_SNS	FS0B_DIAG	FS0B_ REQ	FS1B_DRV	FS1B_ SNS	FS1N_ DIAG	FS1B_REQ	GOTO_ INIT	0
Fail-safe	53	Section 18.14	0	0	0	0	0	0	FS1B_TDELAY [9:5]					FS1B_TDUR [4:0]				
Fail-safe	54	Section 18.15	0	0	0	0	0	BAD_ WD_DATA	BAD_WD_ TIMING	ABIST1_PASS	ABIST2_PASS	ABIST2_ DONE	SPI_FS_CLK	SPI_ FS_ REQ	SPI_ FS_ CRC	FS_OSC_ DRIFT	LBIST_STATUS [1:0]	
Fail-safe	55	Section 18.16	0	0	0	0	0	0	0	0	FCCU12	FCCU1	FCCU2	FCCU1_ RT	FCCU2_ RT	ERRMON_ ACK	ERRMON	ERRMON_ PIN_STATUS
Fail-safe	56	Section 18.17	VPRE_M	CORE_M	LDO1_M	LDO2_M	TRK1_M	TRK2_M	REF_M	EXT_M	FCCU1_M	FCCU2_M	BAD_WD_M	ERRMON_ M	0	0	0	0
Fail-safe	57	Section 18.18	0	EXIT_ DBG_ MODE	DBG_ MODE	OTP_ CORRUPT	REG_ CORRUPT	0	0	0	0	0	0	FS_STATES				
Fail-safe	58	Section 18.19	0	0	0	0	0	0	0	STBY_ WAKE_UP	FS_LP_REQ							
Fail-safe	59	Section 18.20	0	0	0	0	0	0	0	0	LDT_SEL							

Register map overview legend

Bit types	READ / WRITE	READ	WRITE

17 Main register mapping

17.1 M_DEVICEID

Table 18. M_DEVICEID register bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	FULL_LAYER_REV[2:0]			METAL_LAYER_REV[2:0]			FAM_ID[3:0]				DEV_ID[5:0]					
Reset	0	1	1	0	0	1	0	1	1	1	OTP	OTP	OTP	OTP	OTP	OTP

Go to main register map

Table 19. M_DEVICEID register bit description

Bit	Symbol	Value	Description
15 to 13	FULL_LAYER_REV[2:0]	Full layer mask revision	
		3	Pass C silicon
		Reset condition: N/A	
12 to 10	METAL_LAYER_REV[2:0]	Metal mask revision	
		1	Rev X.1
		Reset condition: N/A	
9 to 6	FAM_ID[3:0]	Device family Identification	
		7	FS2630 family. Defined on metal mask.
		Reset condition: N/A	
5 to 0	DEV_ID[5:0]	Device ID	
		FS2630 version dependent. See Table 1	
		Reset condition: N/A	

17.2 M_PROGID

Table 20. M_PROGID register bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	PROG_IDH[7:0]								PROG_IDL[7:0]							
Reset	OTP								OTP							

Go to main register map

Table 21. M_PROGID register bit description

Bit	Symbol	Description
15 to 8	PROG_IDH[7:0]	Higher byte to set the first letter for the OTP ID code (A-Z)
		PROG_IDH_OTP[7:0]
		Reset condition: N/A
7 to 0	PROG_IDL[7:0]	Lower byte to set the second letter for OTP ID code (A-Z)
		PROG_IDL_OTP[7:0]
		Reset condition: N/A

17.3 M_STATUS

Table 22. M_STATUS register bit allocation

Bit	15	14	13	12	11	10	9	8
Read	TWARN_S	VDBG_VOLT_S	VBST_ ACTIVE_S	VBSTFB_UV_S	WK2_S	WK1_S	GPIO2_S	GPIO1_S

Table 22. M_STATUS register bit allocation*...continued*

Bit	15	14	13	12	11	10	9	8
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read	VREF_S	VBST_S	VPRE_S	TRK2_S	TRK1_S	CORE_S	LDO2_S	LDO1_S
Reset	0	0	0	0	0	0	0	0

Go to main register map

Table 23. M_STATUS register bit description

Bit	Symbol	Value	Description
15	TWARN_S	Real-time status of Thermal Warning flag	
		0	$T_J < T_{WARN}$
		1	$T_J > T_{WARN}$
		Real-time information	
14	VDBG_VOLT_S	Real-time status of DEBUG pin voltage	
		0	DEBUG pin voltage $V_{DEBUG} < V_{NORM}$
		1	DEBUG pin voltage $V_{DEBUG} > V_{DBG}$
		Real-time information	
13	VBST_ACTIVE_S	Real-time status of VBST switching status	
		0	VBST switching node is not switching
		1	VBST switching node is switching
		Real-time information	
12	VBSTFB_UV_S	Real-time status of VBST_FB pin	
		0	VBST_FB pin voltage $V_{BST} > V_{BST\_UV\_TH}$
		1	VBST_FB pin voltage $V_{BST} < V_{BST\_UV\_TH}$
		Real-time information	
11	WK2_S	Real-time status of WAKE2 pin	
		0	WAKE2 is low (V_{IL_WAKEx})
		1	WAKE2 is high (V_{IH_WAKEx})
		Real-time information	
10	WK1_S	Real-time status of WAKE1 pin	
		0	WAKE1 is low (V_{IL_WAKEx})
		1	WAKE1 is high (V_{IH_WAKEx})
		Real-time information	
9	GPIO2_S	GPIO2 pin status	
		0	GPIO2 is low (V_{IL_GPIOx})
		1	GPIO2 is high (V_{IH_GPIOx})
		Real-time information	
8	GPIO1_S	GPIO1 pin status	
		0	GPIO1 is low (V_{IL_GPIOx})
		1	GPIO1 is high (V_{IH_GPIOx})
		Real-time information	
7	VREF_S	Real time status of VREF regulator	
		0	VREF is disabled
		1	VREF is enabled
		Real-time information	

Table 23. M_STATUS register bit description...*continued*

Bit	Symbol	Value	Description
6	VBST_S		Real time status of VBST regulator
		0	VBST is disabled
		1	VBST is enabled
			Real-time information
5	VPRE_S		Real time status of VPRE regulator
		0	VPRE is disabled
		1	VPRE is enabled
			Real-time information
4	TRK2_S		Real time status of TRK2 regulator
		0	TRK2 is disabled
		1	TRK2 is enabled
			Real-time information
3	TRK1_S		Real time status of TRK1 regulator
		0	TRK1 is disabled
		1	TRK1 is enabled
			Real-time information
2	CORE_S		Real time status of VCORE regulator
		0	VCORE is disabled
		1	VCORE is enabled
			Real-time information
1	LDO2_S		Real time status of LDO2 regulator
		0	LDO2 is disabled
		1	LDO2 is enabled
			Real-time information
0	LDO1_S		Real time Status of LDO1 regulator
		0	LDO1 is disabled
		1	LDO1 is enabled
			Real-time information

17.4 M_TSD_FLG

Table 24. M_TSD_FLG register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	TWARN_I	0	0	0	0	0	0	0
Read	TWARN_I	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	0	GPIO1TSD_I	VPRETSD_I	TRK2TSD_I	TRK1TSD_I	CORETSD_I	LDO2TSD_I	LDO1TSD_I
Read	RESERVED	GPIO1TSD_I	VPRETSD_I	TRK2TSD_I	TRK1TSD_I	CORETSD_I	LDO2TSD_I	LDO1TSD_I
Reset	0	0	0	0	0	0	0	0

Go to main register map

Table 25. M_TSD_FLG register bit description

Bit	Symbol	Value	Description
15	TWARN_I	Central temperature sensor thermal warning flag Set when $T_J > T_{WARN}$	
		0	Event not detected
		1	Event detected. Generates interrupt (INTB pulse)
		Reset on power-on reset (POR_M) or clear on write 1	
6	GPIO1TSD_I	GPIO1 thermal shutdown flag. Set when local $T_J > TSD_{GPIO1}$	
		0	Event not detected
		1	Event detected. Generates interrupt (INTB pulse)
		Reset on power-on reset (POR_M) or clear on write 1	
5	VPRETSD_I	VPRE thermal shutdown flag. Set when local $T_J > TSD_{PRE}$	
		0	Event not detected
		1	Event detected. Generates interrupt (INTB pulse)
		Reset on power-on reset (POR_M) or clear on write 1	
4	TRK2TSD_I	TRK2 thermal shutdown flag. Set when local $T_J > TSD_{TRKx}$	
		0	Event not detected
		1	Event detected. Generates interrupt (INTB pulse)
		Reset on power-on reset (POR_M) or clear on write 1	
3	TRK1TSD_I	TRK1 thermal shutdown flag. Set when local $T_J > TSD_{TRKx}$	
		0	Event not detected
		1	Event detected. Generates interrupt (INTB pulse)
		Reset on power-on reset (POR_M) or clear on write 1	
2	CORETSD_I	VCORE thermal shutdown flag. Set when local $T_J > TSD_{CORE}$	
		0	Event not detected
		1	Event detected. Generates interrupt (INTB pulse)
		Reset on power-on reset (POR_M) or clear on write 1	
1	LDO2TSD_I	LDO2 thermal shutdown flag. Set when local $T_J > TSD_{LDOx}$	
		0	Event not detected
		1	Event detected. Generates interrupt (INTB pulse)
		Reset on power-on reset (POR_M) or clear on write 1	
0	LDO1TSD_I	LDO1 thermal shutdown flag. Set when local $T_J > TSD_{LDOx}$	
		0	Event not detected
		1	Event detected. Generates interrupt (INTB pulse)
		Reset on power-on reset (POR_M) or clear on write 1	

17.5 M_TSD_MSK

Table 26. M_TSD_MSK register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	TWARN_M	0	0	0	0	0	0	0
Read	TWARN_M	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	0	GPIO1TSD_M	VPRETSD_M	TRK2TSD_M	TRK1TSD_M	CORETSD_M	LDO2TSD_M	LDO1TSD_M
Read	RESERVED	GPIO1TSD_M	VPRETSD_M	TRK2TSD_M	TRK1TSD_M	CORETSD_M	LDO2TSD_M	LDO1TSD_M
Reset	0	0	0	0	0	0	0	0

Go to main register map

Table 27. M_TSD_MSK register bit description (default value in bold)

Bit	Symbol	Value	Description
15	TWARN_M	Inhibit interrupt (INTB pulse) related to TWARN_I event	
		0	**Interrupt NOT MASKED**
		1	Interrupt MASKED
		Reset on power-on reset (POR_M)	
6	GPIO1TSD_M	Inhibit interrupt (INTB pulse) related to GPIO1TSD_I event	
		0	**Interrupt NOT MASKED**
		1	Interrupt MASKED
		Reset on power-on reset (POR_M)	
5	VPRETSD_M	Inhibit interrupt (INTB pulse) related to VPRETSD_I event	
		0	**Interrupt NOT MASKED**
		1	Interrupt MASKED
		Reset on power-on reset (POR_M)	
4	TRK2TSD_M	Inhibit interrupt (INTB pulse) related to TRK2TSD_I event	
		0	**Interrupt NOT MASKED**
		1	Interrupt MASKED
		Reset on power-on reset (POR_M)	
3	TRK1TSD_M	Inhibit interrupt (INTB pulse) related to TRK1TSD_I event	
		0	**Interrupt NOT MASKED**
		1	Interrupt MASKED
		Reset on power-on reset (POR_M)	
2	CORETSD_M	Inhibit interrupt (INTB pulse) related to CORETSD_I event	
		0	**Interrupt NOT MASKED**
		1	Interrupt MASKED
		Reset on power-on reset (POR_M)	
1	LDO2TSD_M	Inhibit interrupt (INTB pulse) related to LDO2TSD_I event	
		0	**Interrupt NOT MASKED**
		1	Interrupt MASKED
		Reset on power-on reset (POR_M)	
0	LDO1TSD_M	Inhibit interrupt (INTB pulse) related to LDO1TSD_I event	
		0	**Interrupt NOT MASKED**
		1	Interrupt MASKED
		Reset on power-on reset (POR_M)	

17.6 M_REG_FLG

Table 28. M_REG_FLG register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	0	0	0	VBSTOV_I
Read	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	VBSTOV_I
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	VPREUVH_I	VBSTOC_I	VPREOC_I	TRK2OC_I	TRK1OC_I	COREOC_I	LDO2OC_I	LDO1OC_I
Read	VPREUVH_I	VBSTOC_I	VPREOC_I	TRK2OC_I	TRK1OC_I	COREOC_I	LDO2OC_I	LDO1OC_I

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0

Go to main register map

Table 29. M_REG_FLG register bit description

Bit	Symbol	Value	Description
8	VBSTOV_I	VBST overvoltage flag. Set when $V_{BST} > V_{BST\_OV\_TH}$	
		0	Event not detected
		1	Event detected. Generates interrupt (INTB pulse)
		Reset on power-on reset (POR_M) or clear on write 1	
7	VPREUVH_I	VPRE undervoltage flag. Set when $V_{PRE\_PWM} < V_{PRE\_UVH}$	
		0	Event not detected
		1	Event detected. Generates interrupt (INTB pulse)
		Reset on power-on reset (POR_M) or clear on write 1	
6	VBSTOC_I	VBST overcurrent event. Set when VBST_ISH pin voltage minus VBST_ISL pin voltage > $V_{BST\_ILIM\_TH}$	
		0	Event not detected
		1	Event detected. Generates interrupt (INTB pulse)
		Reset on power-on reset (POR_M) or clear on write 1	
5	VPREOC_I	VPRE overcurrent event. Set when $I_{PRE\_PWM} > I_{PRE\_OC\_FLAG}$	
		0	Event not detected
		1	Event detected. Generates interrupt (INTB pulse)
		Reset on power-on reset (POR_M) or clear on write 1	
4	TRK2OC_I	TRK2 overcurrent event. Set when $I_{TRK2} > I_{LIM\_TRKx}$	
		0	Event not detected
		1	Event detected. Generates interrupt (INTB pulse)
		Reset on power-on reset (POR_M) or clear on write 1	
3	TRK1OC_I	TRK1 overcurrent event. Set when $I_{TRK1} > I_{LIM\_TRKx}$	
		0	Event not detected
		1	Event detected. Generates interrupt (INTB pulse)
		Reset on power-on reset (POR_M) or clear on write 1	
2	COREOC_I	VCORE overcurrent event. Set when $I_{CORE} > I_{CORE\_PEAK\_0A8}$ (for FS260x and FS261x) or $I_{CORE} > I_{CORE\_PEAK\_1A65}$ (for FS262x and FS263x)	
		0	Event not detected
		1	Event detected. Generates interrupt (INTB pulse)
		Reset on power-on reset (POR_M) or clear on write 1	
1	LDO2OC_I	LDO2 overcurrent event. Set when $I_{LDO2} > I_{LIM\_LDOx}$	
		0	Event not detected
		1	Event detected. Generates interrupt (INTB pulse)
		Reset on power-on reset (POR_M) or clear on write 1	
0	LDO1OC_I	LDO1 overcurrent event. Set when $I_{LDO1} > I_{LIM\_LDOx}$	
		0	Event not detected
		1	Event detected. Generates interrupt (INTB pulse)
		Reset on power-on reset (POR_M) or clear on write 1	

17.7 M_REG_MSK

Table 30. M_REG_MSK register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	0	0	0	VBSTOV_M
Read	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	VBSTOV_M
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	VPREUVH_M	VBSTOC_M	VPREOC_M	TRK2OC_M	TRK1OC_M	COREOC_M	LDO2OC_M	LDO1OC_M
Read	VPREUVH_M	VBSTOC_M	VPREOC_M	TRK2OC_M	TRK1OC_M	COREOC_M	LDO2OC_M	LDO1OC_M
Reset	0	0	0	0	0	0	0	0

Go to main register map

Table 31. M_REG_MSK register bit description

Bit	Symbol	Value	Description
8	VBSTOV_M	Inhibit interrupt (INTB pulse) related to VBSTOV_I event	
		0	**Interrupt NOT MASKED (default)**
		1	Interrupt MASKED
		Reset on power-on reset (POR_M)	
7	VPREUVH_M	Inhibit interrupt (INTB pulse) related to VPREUVH_I event	
		0	**Interrupt NOT MASKED (default)**
		1	Interrupt MASKED
		Reset on power-on reset (POR_M)	
6	VBSTOC_M	Inhibit interrupt (INTB pulse) related to VBSTOC_I event	
		0	**Interrupt NOT MASKED (default)**
		1	Interrupt MASKED
		Reset on power-on reset (POR_M)	
5	VPREOC_M	Inhibit interrupt (INTB pulse) related to VPREOC_I event	
		0	**Interrupt NOT MASKED (default)**
		1	Interrupt MASKED
		Reset on power-on reset (POR_M)	
4	TRK2OC_M	Inhibit interrupt (INTB pulse) related to TRK2OC_I event	
		0	**Interrupt NOT MASKED (default)**
		1	Interrupt MASKED
		Reset on power-on reset (POR_M)	
3	TRK1OC_M	Inhibit interrupt (INTB pulse) related to TRK1OC_I event	
		0	**Interrupt NOT MASKED (default)**
		1	Interrupt MASKED
		Reset on power-on reset (POR_M)	
2	COREOC_M	Inhibit interrupt (INTB pulse) related to COREOC_I event	
		0	**Interrupt NOT MASKED (default)**
		1	Interrupt MASKED
		Reset on power-on reset (POR_M)	

Table 31. M_REG_MSK register bit description*...continued*

Bit	Symbol	Value	Description
1	LDO2OC_M	Inhibit interrupt (INTB pulse) related to LDO2OC_I event	
		0	**Interrupt NOT MASKED (default)**
		1	Interrupt MASKED
		Reset on power-on reset (POR_M)	
0	LDO1OC_M	Inhibit interrupt (INTB pulse) related to LDO1OC_I event	
		0	**Interrupt NOT MASKED (default)**
		1	Interrupt MASKED
		Reset on power-on reset (POR_M)	

17.8 M_VSUP_FLG

Table 32. M_VSUP_FLG register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	0	0	0	0
Read	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	0	0	0	0	VBOSUVH_I	VSUPOV_I	VSUPUV6_I	VSUPUVH_I
Read	RESERVED	RESERVED	RESERVED	RESERVED	VBOSUVH_I	VSUPOV_I	VSUPUV6_I	VSUPUVH_I
Reset	0	0	0	0	0	0	0	0

Go to main register map

Table 33. M_VSUP_FLG register bit description

Bit	Symbol	Value	Description
3	VBOSUVH_I	VBOS undervoltage flag. Set when $V_{BOS} < V_{BOS\_UVH}$	
		0	Event not detected
		1	Event detected. Generates interrupt (INTB pulse)
		Reset on power-on reset (POR_M) or clear on Write (write 1)	
2	VSUPOV_I	VSUP overvoltage flag. Set when $V_{SUP} > V_{SUP\_OV}$	
		0	Event not detected
		1	Event detected. Generates interrupt (INTB pulse)
		Reset on power-on reset (POR_M) or clear on Write (write 1)	
1	VSUPUV6_I	VSUP undervoltage (6 V) flag. Set when $V_{SUP} < V_{SUP\_UV6}$	
		0	Event not detected
		1	Event detected. Generates interrupt (INTB pulse)
		Reset on power-on reset (POR_M) or clear on Write (write 1)	
0	VSUPUVH_I	VSUP undervoltage flag. Set when $V_{SUP} < V_{SUP\_UVH}$	
		0	Event not detected
		1	Event detected. Generates interrupt (INTB pulse)
		Reset on power-on reset (POR_M) or clear on Write (write 1)	

17.9 M_VSUP_MSK

Table 34. M_VSUP_MSK register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	0	0	0	0
Read	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	0	0	0	0	VBOSUVH_M	VSUPOV_M	VSUPUV6_M	VSUPUVH_M
Read	RESERVED	RESERVED	RESERVED	RESERVED	VBOSUVH_M	VSUPOV_M	VSUPUV6_M	VSUPUVH_M
Reset	0	0	0	0	0	0	0	0

Go to main register map

Table 35. M_VSUP_MSK register bit description

Bit	Symbol	Value	Description
3	VBOSUVH_M	Inhibit interrupt (INTB pulse) related to VBOSUVH_I event	
		0	**Interrupt NOT MASKED (default)**
		1	Interrupt MASKED
		Reset on power-on reset (POR_M)	
2	VSUPOV_M	Inhibit interrupt (INTB pulse) related to VSUPOV_I event	
		0	**Interrupt NOT MASKED (default)**
		1	Interrupt MASKED
		Reset on power-on reset (POR_M)	
1	VSUPUV6_M	Inhibit interrupt (INTB pulse) related to VSUPUV6_I event	
		0	**Interrupt NOT MASKED (default)**
		1	Interrupt MASKED
		Reset on power-on reset (POR_M)	
0	VSUPUVH_M	Inhibit interrupt (INTB pulse) related to VSUPUVH_I event	
		0	**Interrupt NOT MASKED (default)**
		1	Interrupt MASKED
		Reset on power-on reset (POR_M)	

17.10 M_WIO_FLG

Table 36. M_WIO_FLG register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	WU_CLR	0	0	0	0	0	0	0
Read	RESERVED	RESERVED	RESERVED	RESERVED	WUEVENT[3:0]			
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	0	0	0	0	0	0	0	0
Read	RESERVED	RESERVED	RESERVED	LDT_I	GPIO2_I	GPIO1_I	WK2_I	WK1_I
Reset	0	0	0	0	0	0	0	0

Go to main register map

Table 37. M_WIO_FLG register bit description

Bit	Symbol	Value	Description
15	WU_CLR	Clear wake-up flags	
		0	Do nothing
		1	Clear all wake-up flags
		Reset on power-on reset (POR_M), self-clear	
11 to 8	WUEVENT[3:0]	Wake-up event source. Generates interrupt (INTB pulse)	
		0h	No wake up detected
		1h	WAKE1
		2h	WAKE2
		3h	GPIO1
		4h	GPIO2
		5h	LDT expired
		6h	SPI activity
		8h	DFS Recovery
		Fh	BATTERY fail: Reports when the device has lost valid V_{SUP} and Main state machine is reset.
		Reset on power-on reset (POR_M), go to *standby mode*, go to *LPOFF mode*, or WU_CLR write 1	
4	LDT_I	LDT expired event flag	
		0	Event not detected
		1	Event detected. Generates interrupt (INTB pulse)
		Reset on power-on reset (POR_M), go to *standby mode*, go to *LPOFF mode*, or WU_CLR write 1	
3	GPIO2_I	GPIO2 event flag	
		0	No event on GPIO2
		1	Event on GPIO2 has occurred. Generates interrupt (INTB pulse)
		Reset on power-on reset (POR_M), go to *standby mode*, go to *LPOFF mode*, or WU_CLR write 1	
2	GPIO1_I	GPIO1 event flag	
		0	No event on GPIO1
		1	Event on GPIO1 has occurred. Generates interrupt (INTB pulse)
		Reset on power-on reset (POR_M), go to *standby mode*, go to *LPOFF mode*, or WU_CLR write 1	
1	WK2_I	WAKE2 event flag	
		0	No event on WAKE2
		1	Event on WAKE2 has occurred. Generates interrupt (INTB pulse)
		Reset on power-on reset (POR_M), go to *standby mode*, go to *LPOFF mode*, or WU_CLR write 1	
0	WK1_I	WAKE1 event flag	
		0	No event on WAKE1
		1	Event on WAKE1 has occurred. Generates interrupt (INTB pulse)
		Reset on power-on reset (POR_M), go to *standby mode*, go to *LPOFF mode*, or WU_CLR write 1	

17.11 M_WIO_MSK

Table 38. M_WIO_MSK register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	0	0	0	0
Read	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	0	0	0	LDT_M	GPIO2_M	GPIO1_M	WK2_M	WK1_M

Bit	7	6	5	4	3	2	1	0
Read	RESERVED	RESERVED	RESERVED	LDT_M	GPIO2_M	GPIO1_M	WK2_M	WK1_M
Reset	0	0	0	0	0	0	0	0

Go to main register map

Table 39. M_WIO_MSK register bit description (default)

Bit	Symbol	Value	Description
4	LDT_M	Inhibit interrupt (INTB pulse) related to LDT_I event	
		0	**Interrupt NOT MASKED (default)**
		1	Interrupt MASKED
		Reset on power-on reset (POR_M)	
3	GPIO2_M	Inhibit interrupt (INTB pulse) related to GPIO2_I event	
		0	**Interrupt NOT MASKED (default)**
		1	Interrupt MASKED
		Reset on power-on reset (POR_M)	
2	GPIO1_M	Inhibit interrupt (INTB pulse) related to GPIO1_I event	
		0	**Interrupt NOT MASKED (default)**
		1	Interrupt MASKED
		Reset on power-on reset (POR_M)	
1	WK2_M	Inhibit interrupt (INTB pulse) related to WK2_I event	
		0	**Interrupt NOT MASKED (default)**
		1	Interrupt MASKED
		Reset on power-on reset (POR_M)	
0	WK1_M	Inhibit interrupt (INTB pulse) related to WK1_I event	
		0	**interrupt NOT MASKED (default)**
		1	Interrupt MASKED
		Reset on power-on reset (POR_M)	

17.12 M_COM_FLG

Table 40. M_COM_FLG register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	0	0	0	0
Read	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	0	0	0	0	0	MSPI_CRC_I	MSPI_CLK_I	MSPI_REQ_I
Read	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	MSPI_CRC_I	MSPI_CLK_I	MSPI_REQ_I
Reset	0	0	0	0	0	0	0	0

Go to main register map

Table 41. M_COM_FLG register bit description

Bit	Symbol	Value	Description
2	MSPI_CRC_I	Main domain SPI message corrupted (CRC not valid) flag	
		0	Event not detected
		1	Event detected. Generates interrupt (INTB pulse)
		Reset on power-on reset (POR_M), or clear on write 1	
1	MSPI_CLK_I	Main domain SPI wrong number of clock pulses flag	
		0	Event not detected
		1	Event detected. Generates interrupt (INTB pulse)
		Reset on power-on reset (POR_M), or clear on write 1	
0	MSPI_REQ_I	Main domain SPI access violation (write to an invalid register) flag	
		0	Event not detected
		1	Event detected. Generates interrupt (INTB pulse)
		Reset on power-on reset (POR_M), or clear on write 1	

17.13 M_COM_MSK

Table 42. M_COM_MSK register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	0	0	0	0
Read	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	0	0	0	0	0	MSPI_CRC_M	MSPI_CLK_M	MSPI_REQ_M
Read	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	MSPI_CRC_M	MSPI_CLK_M	MSPI_REQ_M
Reset	0	0	0	0	0	0	0	0

Go to main register map

Table 43. M_COM_MSK register bit description (default value in bold)

Bit	Symbol	Value	Description
2	MSPI_CRC_M	Inhibit interrupt (INTB pulse) related to MSPI_CRC_I event	
		0	**Interrupt NOT MASKED**
		1	Interrupt MASKED
		Reset on power-on reset (POR_M)	
1	MSPI_CLK_M	Inhibit interrupt (INTB pulse) related to MSPI_CLK_I event	
		0	**Interrupt NOT MASKED**
		1	Interrupt MASKED
		Reset on power-on reset (POR_M)	
0	MSPI_REQ_M	Inhibit interrupt (INTB pulse) related to MSPI_REQ_I event	
		0	**Interrupt NOT MASKED**
		1	Interrupt MASKED
		Reset on power-on reset (POR_M)	

17.14 M_SYS_CFG

Table 44. M_SYS_CFG register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	0	0	0	0
Read	RETRY_CNT[7:0]							
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	RETRY_CLR	0	0	INTB_TEST	INT_PWIDTH	FSS_FMOD	0	FSS_EN
Read	RESERVED	RESERVED	RESERVED	RESERVED	INT_PWIDTH	FSS_FMOD	RESERVED	FSS_EN
Reset	0	0	0	0	0	0	0	0

Go to main register map

Table 45. M_SYS_CFG register bit description

Bit	Symbol	Value	Description
15 to 8	RETRY_CNT[7:0]	Retry counter (value) and retry interval (description) Number of retries attempts / time between each retry attempt	
		0xh	**100 ms (default)**
		1xh	200 ms
		2xh	400 ms
		3xh	800 ms
		4xh	1600 ms
		5xh	3200 ms
		6xh	6400 ms
		7xh	12800 ms
		8xh	25600 ms
		9xh	51200 ms
		Axh	102400 ms
		Bxh	204800 ms
		Cxh	409600 ms
		Dxh	819200 ms
		Exh	1638400 ms
		Fxh	3276800 ms
		Reset on power-on reset (POR_M) or RETRY_CLR write 1	
7	RETRY_CLR	Clear retry counter RETRY_CNT[7:0]	
		0	No effect
		1	Clear retry counter
		Reset on power-on reset (POR_M), self-clear	
4	INTB_TEST	Manual test of INTB	
		0	No effect
		1	Enable manual test. Generate a pulse of duration t_{INTB_PULSE} at INTB pin for test purpose.
		Reset on power-on reset (POR_M), self-clear	
3	INT_PWIDTH	INTB pulse duration t_{INTB_PULSE}	
		0	**25 µs (default)**
		1	100 µs
		Reset on power-on reset (POR_M)	

Table 45. M_SYS_CFG register bit description...*continued*

Bit	Symbol	Value	Description
2	FSS_FMOD	Frequency modulation F_{OSC_MOD} during Frequency Spread Spectrum Operation	
		0	**High-frequency oscillator divided by 896 (default)**
		1	High-frequency oscillator divided by 224
		Reset on power-on reset (POR_M)	
0	FSS_EN	Frequency Spread Spectrum enable	
		0	**FSS is disabled (default)**
		1	FSS is enabled
		Reset on power-on reset (POR_M)	

17.15 M_TSD_CFG

Table 46. M_TSD_CFG register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	0	0	0	0
Read	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	0	0	VPRETDFS	TRK2TDFS	TRK1TDFS	CORETDFS	LDO2TDFS	LDO1TDFS
Read	RESERVED	RESERVED	VPRETDFS	TRK2TDFS	TRK1TDFS	CORETDFS	LDO2TDFS	LDO1TDFS
Reset	0	0	OTP	OTP	OTP	OTP	OTP	OTP

Go to main register map

Table 47. M_TSD_CFG register bit description

Bit	Symbol	Value	Description
5	VPRETDFS	*Deep Fail Safe* request in case of VPRE Thermal Shutdown	
		0	Regulator disabled
		1	Transition to DFS
		Load fuse state (VPRETDFS_OTP)	
4	TRK2TDFS	*Deep Fail Safe* request in case of TRK2 Thermal Shutdown	
		0	Regulator disabled
		1	Transition to DFS
		Load fuse state (TRK1TDFS_OTP)	
3	TRK1TDFS	*Deep Fail Safe* request in case of TRK1 Thermal Shutdown	
		0	Regulator disabled
		1	Transition to DFS
		Load fuse state (TRK1TDFS_OTP)	
2	CORETDFS	*Deep Fail Safe* request in case of VCORE Thermal Shutdown	
		0	Regulator disabled
		1	Transition to DFS
		Load fuse state (CORETDFS_OTP)	
1	LDO2TDFS	*Deep Fail Safe* request in case of LDO2 Thermal Shutdown	
		0	Regulator disabled
		1	Transition to DFS
		Load fuse state (LDO1TDFS_OTP)	

Table 47. M_TSD_CFG register bit description*...continued*

Bit	Symbol	Value	Description
0	LDO1TDFS	*Deep Fail Safe* request in case of LDO1 Thermal Shutdown	
		0	Regulator disabled
		1	Transition to DFS
		Load fuse state (LDO1TDFS_OTP)	

17.16 M_REG_CFG (0x0F)

Table 48. M_REG_CFG register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	0	0	0	0
Read	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	0	0	0	0	0	0	VREF_PD	VBST_TMD
Read	0	0	0	0	0	0	VREF_PD	VBST_TMD
Reset	0	0	0	0	0	0	1	0

Table 49. M_REG_CFG register bit description (default value in bold)

Bit	Symbol	Description
1	VREF_PD	VREF Internal pull-down configuration (R_{REF_DIS})
		0 Disable internal pull-down when VREF output is disabled
		1 Enable internal pull-down when VREF output is disabled
		Reset on power-on reset (POR_M)
0	VBST_TMD	VBST output verification mode
		0 VBST output is regulated to the configured voltage set by OTP
		1 VBST regulate to 17 V to verify availability
		Reset on power-on reset (POR_M)

17.17 M_WIO_CFG (0x10)

Table 50. M_WIO_CFG register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	GPIO2WUPOL	GPIO1WUPOL	WAKE2POL	WAKE1POL
Read	0	0	0	0	GPIO2WUPOL	GPIO1WUPOL	WAKE2POL	WAKE1POL
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	0	0	CSBWUEN	LDTWUEN	GPIO2WUEN	GPIO1WUEN	WK2WUEN	WK1WUEN
Read	0	0	CSBWUEN	LDTWUEN	GPIO2WUEN	GPIO1WUEN	WK2WUEN	WK1WUEN
Reset	0	0	0	0	0	0	0	0

Table 51. M_WIO_CFG register bit description (default value in bold)

Bit	Symbol	Description
11	GPIO2WUPOL	GPIO2 event detection polarity
		0 High level on GPIO2 will wake up the part
		1 Low level on GPIO2 will wake up the part
		Reset on power-on reset (POR_M)
10	GPIO1WUPOL	GPIO1 event detection polarity
		0 High level on GPIO1 will wake up the part
		1 Low level on GPIO1 will wake up the part
		Reset on power-on reset (POR_M)
9	WAKE2POL	WAKE2 event detection polarity
		0 High level on WAKE2 will wake up the part
		1 Low level on WAKE2 will wake up the part
		Reset on power-on reset (POR_M)
8	WAKE1POL	WAKE1 event detection polarity
		0 High level on WAKE1 will wake up the part
		1 Low level on WAKE1 will wake up the part
		Reset on power-on reset (POR_M)
5	CSBWUEN	CSB Transition wake-up enabled
		0 Disabled
		1 Enabled
		Reset on power-on reset (POR_M)
4	LDTWUEN	Long Duration Timer wake-up enabled
		0 Disabled
		1 Enabled
		Reset on power-on reset (POR_M)
3	GPIO2WUEN	GPIO2 wake-up enabled
		0 Disabled
		1 Enabled
		Reset on power-on reset (POR_M)
2	GPIO1WUEN	GPIO1 wake-up enabled
		0 Disabled
		1 Enabled
		Reset on power-on reset (POR_M)
1	WK2WUEN	WAKE2 wake-up enabled
		0 Disabled
		1 Enabled
		Reset on power-on reset (POR_M)
0	WK1WUEN	WAKE1 wake-up enabled
		0 Disabled
		1 Enabled
		Reset on power-on reset (POR_M)

17.18 M_REG_CTRL1

Table 52. M_REG_CTRL1 register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	GPIO2LP_ON	GPIO1LP_ON	0	0	GPIO2HI	GPIO1HI
Read	RESERVED	RESERVED	GPIO2LP_ON	GPIO1LP_ON	RESERVED	RESERVED	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	VREFEN	VBSTEN	0	TRK2EN	TRK1EN	COREEN	LDO2EN	LDO1EN
Read	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

Go to main register map

Table 53. M_REG_CTRL1 register bit description

Bit	Symbol	Value	Description
13	GPIO2LP_ON	Configure GPIO2 state in *standby mode*	
		0	Follow the power down slot configuration
		1	Keep GPIO2 in the same state as it was in *normal mode*
		Reset on power-on reset (POR_M),	
12	GPIO1LP_ON	Configure GPIO1 state in *standby mode* and in *LPOFF mode*	
		0	Follow the power down slot configuration
		1	Keep GPIO1 in the same state as it was in *normal mode*
		Reset on power-on reset (POR_M),	
9	GPIO2HI	Request GPIO2 pin high	
		0	No effect (GPIO2 remains in current state)
		1	GPIO2 set high
		Reset on power-on reset (POR_M), self-cleared	
8	GPIO1HI	Request GPIO1 pin high	
		0	No effect (GPIO1 remains in current state)
		1	GPIO1 set high
		Reset on power-on reset (POR_M), self-cleared	
7	VREFEN	VREF enable request	
		0	No effect (regulator remain in its current state)
		1	VREF enable request
		Reset on power-on reset (POR_M), self-cleared	
6	VBSTEN	VBST enable request	
		0	No effect (regulator remain in its current state)
		1	VBST enable request
		Reset on power-on reset (POR_M), self-cleared	
4	TRK2EN	TRK2 enable request	
		0	No effect (regulator remain in its current state)
		1	TRK2 enable request
		Reset on power-on reset (POR_M), self-cleared	

Table 53. M_REG_CTRL1 register bit description...*continued*

Bit	Symbol	Value	Description
3	TRK1EN	TRK1 enable request	
		0	No effect (regulator remain in its current state)
		1	TRK1 enable request
		Reset on power-on reset (POR_M), self-cleared	
2	COREEN	VCORE enable request	
		0	No effect (regulator remain in its current state)
		1	VCORE enable request
		Reset on power-on reset (POR_M), self-cleared	
1	LDO2EN	LDO2 enable request	
		0	No effect (regulator remain in its current state)
		1	LDO2 enable request
		Reset on power-on reset (POR_M), self-cleared	
0	LDO1EN	LDO1 enable request	
		0	No effect (regulator remain in its current state)
		1	LDO1 enable request
		Reset on power-on reset (POR_M), self-cleared	

17.19 M_REG_CTRL2

Table 54. M_REG_CTRL2 register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	0	0	GPIO2LO	GPIO1LO
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	VREFDIS	VBSTDIS	0	TRK2DIS	TRK1DIS	COREDIS	LDO2DIS	LDO1DIS
Reset	0	0	0	0	0	0	0	0

Go to main register map

Table 55. M_REG_CTRL2 register bit description

Bit	Symbol	Value	Description
9	GPIO2LO	Request GPIO2 pin low	
		0	No effect (GPIO2 remains in current state)
		1	GPIO2 set low
		Reset on power-on reset (POR_M), self-cleared	
8	GPIO1LO	Request GPIO1 pin low	
		0	No effect (GPIO1 remains in current state)
		1	GPIO1 set low
		Reset on power-on reset (POR_M), self-cleared	
7	VREFDIS	VREF disable request	
		0	No effect (regulator remain in its current state)
		1	VREF disable request
		Reset on power-on reset (POR_M), self-cleared	

Table 55. M_REG_CTRL2 register bit description*...continued*

Bit	Symbol	Value	Description
6	VBSTDIS	VBST disable request	
		0	No effect (regulator remain in its current state)
		1	VBST disable request
		Reset on power-on reset (POR_M), self-cleared	
4	TRK2DIS	TRK2 disable request	
		0	No effect (regulator remain in its current state)
		1	TRK2 Disable request
		Reset on power-on reset (POR_M), self-cleared	
3	TRK1DIS	TRK1 disable request	
		0	No effect (regulator remain in its current state)
		1	TRK1 disable request
		Reset on power-on reset (POR_M), self-cleared	
2	COREDIS	VCORE disable request	
		0	No effect (regulator remain in its current state)
		1	VCORE disable request
		Reset on power-on reset (POR_M), self-cleared	
1	LDO2DIS	LDO2 disable request	
		0	No effect (regulator remain in its current state)
		1	LDO2 disable request
		Reset on power-on reset (POR_M), self-cleared	
0	LDO1DIS	LDO1 disable request	
		0	No effect (regulator remain in its current state)
		1	LDO1 disable request
		Reset on power-on reset (POR_M), self-cleared	

17.20 M_AMUX_CTRL

Table 56. M_AMUX_CTRL register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	0	0	0	0
Read	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	0	AMUX_EN	AMUX_DIV	AMUX[4:0]				
Read	RESERVED	AMUX_EN	AMUX_DIV	AMUX[4:0]				
Reset	0	0	0	0	0	0	0	0

Go to main register map

Table 57. M_AMUX_CTRL register bit description

Bit	Symbol	Value	Description
6	AMUX_EN	Enable AMUX block	
		0	**Disable AMUX block and pin is pulled down to ground (default)**
		1	Enable AMUX block
		Reset on power-on reset (POR_M), Go to *LPOFF mode*, Go to *standby mode*	

Table 57. M_AMUX_CTRL register bit description *...continued*

Bit	Symbol	Value	Description
5	AMUX_DIV	Selection of divider ratio V_{AMUX_RATIO}. See Table 174	
		0	**Divider ratio is 7.5 (default)**
		1	Divider ratio is 14
		Reset on power-on reset (POR_M)	
4 to 0	AMUX[4:0]	AMUX input channel selection	
		00h	**Disabled with AMUX pin in Hi-Z (default)**
		01h	Low Power bandgap (voltage reference)
		02h	Main bandgap (voltage reference)
		03h	Fail-safe bandgap (voltage reference)
		04h	V_{ANA}: Internal main analog voltage supply
		05h	V_{DIG}: internal main digital voltage supply
		06h	V_{DIG_FS}: internal fail-safe digital voltage supply
		07h	VCORE feedback pin CORE_FB voltage
		08h	VPRE feedback pin VPRE_FB voltage
		09h	LDO1 feedback pin LDO1OUT voltage
		0Ah	LDO2 feedback pin LDO1OUT voltage
		0Bh	VREF feedback pin voltage
		0Ch	TRK1 feedback pin voltage
		0Dh	TRK2 feedback pin voltage
		0Eh	VDDIO feedback voltage
		0Fh	VBOS internal pin voltage
		10h	VBST feedback pin VBST_FB voltage (divider ratio configurable with AMUX_DIV)
		11h	VSUP pin voltage V_{SUP} (divider ratio configurable with AMUX_DIV)
		12h	WAKE1 pin voltage (divider ratio configurable with AMUX_DIV)
		13h	WAKE2 pin voltage (divider ratio configurable with AMUX_DIV)
		14h	GPIO1 pin voltage (divider ratio configurable with AMUX_DIV)
		15h	GPIO2 pin voltage (divider ratio configurable with AMUX_DIV)
		16h	BATSENSE pin voltage (divider ratio configurable with AMUX_DIV)
		17h	Die temperature sensor[1]
		18h	VCORE temperature sensor[1]
		19h	VPRE temperature sensor[1]
		1Ah	LDO1 temperature sensor[1]
		1Bh	LDO2 temperature sensor[1]
		1Ch	TRK1 temperature sensor[1]
		1Dh	TRK2 temperature sensor[1]
		1Eh	GPIO1 temperature sensor[1]
		1Fh	Reserved
		Reset on power-on reset (POR_M)	

[1] Temp (°C) = $(V_{AMUX\_OUT} - V_{TEMP25}) / V_{TEMP\_COEFF} + 25$

17.21 M_LDT_CFG1

Table 58. M_LDT_CFG1 register bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	LDT_AFTER_RUN[15:0]															

Table 58. M_LDT_CFG1 register bit allocation*...continued*

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	LDT_AFTER_RUN[15:0]															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Go to main register map

Table 59. M_LDT_CFG1 register bit description

Bit	Symbol	Description
15 to 0	LDT_AFTER_RUN[15:0]	Long Duration Timer (LDT) after-run configuration register
		LDT after-run **target** value in *normal mode*
		Reset on power-on reset (POR_M), LDT count started

17.22 M_LDT_CFG2 (0x15)

Table 60. M_LDT_CFG2 register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	LDT_WUP_L[15:8]							
Read	LDT_WUP_L[15:8]							
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	LDT_WUP_L[7:0]							
Read	LDT_WUP_L[7:0]							
Reset	0	0	0	0	0	0	0	0

Table 61. M_LDT_CFG2 register bit description

Bit	Symbol	Description
15 to 0	LDT_WUP_L[15:0]	16 less significant bits of Wake-up with Long Duration Timer
		16 less significant bits for the wake up with the Long Duration Timer
		Reset on power-on reset (POR_M), LDT Count started

17.23 M_LDT_CFG3 (0x16)

Table 62. M_LDT_CFG3 register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	0	0	0	0
Read	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	LDT_WUP_H[7:0]							
Read	LDT_WUP_H[7:0]							
Reset	0	0	0	0	0	0	0	0

Table 63. M_LDT_CFG3 register bit description

Bit	Symbol	Description
7 to 0	LDT_WUP_H[7:0]	8 more significant bits of Long Duration Timer Wake-up Timer
		8 most significant bit for the wake up with the Long Duration Timer
		Reset on power-on reset (POR_M), LDT Count started

17.24 M_LDT_CTRL

Table 64. M_LDT_CTRL register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	0	0	0	0
Read	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	0	LDT_FNCT[2:0]			LDT_SEL	LDT_MODE	LDT_EN	0
Read	RESERVED	LDT_FNCT[2:0]			LDT_SEL	LDT_MODE	LDT_EN	LDT_RUN
Reset	0	0	0	0	0	0	0	0

Go to main register map

Table 65. M_LDT_CTRL register bit description

Bit	Symbol	Value	Description
6 to 4	LDT_FNCT[2:0]	Long Duration Timer (LDT) function selection	
		0	**Function 1 (default)**
		1	Function 2
		2	Function 3
		3	Function 4
		4	Function 5
		Reset on power-on reset (POR_M)	
3	LDT_SEL	Long Duration Timer (LDT) register (LDT_WUP_H[7:0] / LDT_WUP_L[15:0]) content selection	
		0	**Read / set LDT wake-up target value (default)**
		1	Read LDT 24-bit real time counter value
		Reset on power-on reset (POR_M)	
2	LDT_MODE	Set Long Duration Timer (LDT) operation mode	
		0	**Set LDT to long count (default)**
		1	Set LDT to short count
		Reset on power-on reset (POR_M)	
1	LDT_EN	Start Long Duration Timer (LDT) operation	
		0	**Disable LDT (default)**
		1	LDT starts counting
		Reset on power-on reset (POR_M)	
0	LDT_RUN	LDT status	
		0	**LDT is disabled or not counting (default)**
		1	LDT is enabled and count is in progress
		Reset on power-on reset (POR_M), LDT stopped	

17.25 M_MEMORY0 (0x18)

Table 66. M_MEMORY0 register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	MEM0[15:8]							
Read	MEM0[15:8]							
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	MEM0[7:0]							
Read	MEM0[7:0]							
Reset	0	0	0	0	0	0	0	0

Table 67. M_MEMORY0 register bit description

Bit	Symbol	Description
15 to 0	MEM0[15:0]	Free 16 bits for application data storage
		MEM0 stored data
		Reset on power-on reset (POR_M)

17.26 M_MEMORY1 (0x19)

Table 68. M_MEMORY1 register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	MEM1[15:8]							
Read	MEM1[15:8]							
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	MEM1[7:0]							
Read	MEM1[7:0]							
Reset	0	0	0	0	0	0	0	0

Table 69. M_MEMORY1 register bit description

Bit	Symbol	Description
15 to 0	MEM1[15:0]	Free 16 bits for application data storage
		MEM1 stored data
		Reset on power-on reset (POR_M)

18 Fail-safe register mapping

18.1 FS_GRL_FLAGS (0x40)

Table 70. FS_GRL_FLAGS register bit allocation

Bit	15	14	13	12	11	10	9	8
Read	FS_COM_G	FS_WD_G	FS_IO_G	FS_REG_OVUV_G	FS_BIST_G	0	0	0
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0

Table 71. FS_GRL_FLAGS register bit description

Bit	Symbol	Description
15	FS_COM_G	Report an issue in the communication (SPI)
		0 No Failure
		1 Failure
		Reset on power-on reset (POR_FS), cleared when all individual bits are cleared
		Source register: FS_DIAG_SAFETY1
		Flags Reporting: SPI_FS_CLK, SPI_FS_REQ, SPI_FS_CRC
14	FS_WD_G	Report an issue on the Watchdog Refresh
		0 No Failure
		1 Failure
		Reset on power-on reset (POR_FS), cleared when all individual bits are cleared
		Source register: FS_DIAG_SAFETY1
		Flags Reporting: BAD_WD_DATA, BAD_WD_TIMING
13	FS_IO_G	Report an issue in one of the Fail Safe IOs
		0 No Failure
		1 Failure
		Reset on power-on reset (POR_FS), cleared when all individual bits are cleared
		Source register: FS_SAFE_IOS_1
		Flags Reporting: RSTB_DIAG, FS0B_DIAG, FS1B_DIAG
12	FS_REG_OVUV_G	Report an issue on one of the voltage monitoring (OV or UV)
		0 No Failure
		1 Failure
		Reset on power-on reset (POR_FS), cleared when all individual bits are cleared
		Source register: FS_OVUV_REG_STATUS
		Flags Reporting: VPRE_OV, VPRE_UV, CORE_OV, CORE_UV, LDO1_OV, LDO1_UV, LDO2_OV, LDO2_UV, TRK1_OV, TRK1_UV, TRK2_OV, TRK2_UV, REF_OV, REF_UV, EXT_OV, EXT_UV

Table 71. FS_GRL_FLAGS register bit description*...continued*

Bit	Symbol	Description
11	FS_BIST_G	Report an issue on BIST (Logical or Analog)
		0 No Failure
		1 Failure
		Reset on power-on reset (POR_FS), cleared when all individual bits are cleared
		Source register: FS_DIAG_SAFETY1
		Flags Reporting: ABIST1_PASS, ABIST2_PASS, LBIST_STATUS[1:0]

18.2 FS_I_OVUV_SAFE_REACTION1

Table 72. FS_I_OVUV_SAFE_REACTION1 register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	VMON_PRE_OV_ FS_REACTION[1:0]		VMON_PRE_UV_ FS_REACTION[1:0]		VMON_CORE_OV_ FS_REACTION[1:0]		VMON_CORE_UV_ FS_REACTION[1:0]	
Read	VMON_PRE_OV_ FS_REACTION[1:0]		VMON_PRE_UV_ FS_REACTION[1:0]		VMON_CORE_OV_ FS_REACTION[1:0]		VMON_CORE_UV_ FS_REACTION[1:0]	
Reset	1	0	0	1	1	0	0	1

Bit	7	6	5	4	3	2	1	0
Write	VMON_LDO1_OV_ FS_REACTION[1:0]		VMON_LDO1_UV_ FS_REACTION[1:0]		VMON_LDO2_OV_ FS_REACTION[1:0]		VMON_LDO2_UV_ FS_REACTION[1:0]	
Read	VMON_LDO1_OV_ FS_REACTION[1:0]		VMON_LDO1_UV_ FS_REACTION[1:0]		VMON_LDO2_OV_ FS_REACTION[1:0]		VMON_LDO2_UV_ FS_REACTION[1:0]	
Reset	1	0	0	1	1	0	0	1

Go to fail-safe register map

Table 73. FS_I_OVUV_SAFE_REACTION1 register bit description

Bit	Symbol	Value	Description
15 to 14	VMON_PRE_OV_ FS_REACTION[1:0]	Reaction on RSTB or fail-safe outputs in case of OV detection on VMON_PRE	
		0	No effect on RSTB and FS0B
		1	VMON_PRE OV asserts FS0B only
		2	**VMON_PRE OV asserts RSTB and FS0B (default)**
		3	VMON_PRE OV asserts RSTB and FS0B
		Reset on power-on reset (POR_FS)	
13 to 12	VMON_PRE_UV_ FS_REACTION[1:0]	Reaction on RSTB or fail-safe outputs in case of UV detection on VMON_PRE	
		0	No effect on RSTB and FS0B
		1	**VMON_PRE UV asserts FS0B only (default)**
		2	VMON_PRE UV asserts RSTB and FS0B
		3	VMON_PRE UV asserts RSTB and FS0B
		Reset on power-on reset (POR_FS)	
11 to 10	VMON_CORE_OV_ FS_REACTION[1:0]	Reaction on RSTB or fail-safe outputs in case of OV detection on VMON_CORE	
		0	No effect on RSTB and FS0B
		1	VMON_CORE OV asserts FS0B only
		2	**VMON_CORE OV asserts RSTB and FS0B (default)**
		3	VMON_CORE OV asserts RSTB and FS0B
		Reset on power-on reset (POR_FS)	

Table 73. FS_I_OVUV_SAFE_REACTION1 register bit description...*continued*

Bit	Symbol	Value	Description
9 to 8	VMON_CORE_UV_ FS_REACTION[1:0]	Reaction on RSTB or fail-safe outputs in case of UV detection on VMON_CORE	
		0	No effect on RSTB and FS0B
		1	**VMON_CORE UV asserts FS0B only (default)**
		2	VMON_CORE UV asserts RSTB and FS0B
		3	VMON_CORE UV asserts RSTB and FS0B
		Reset on power-on reset (POR_FS)	
7 to 6	VMON_LDO1_OV_ FS_REACTION[1:0]	Reaction on RSTB or fail-safe outputs in case of OV detection on VMON_LDO1	
		0	No effect on RSTB and FS0B
		1	VMON_LDO1 OV asserts FS0B only
		2	**VMON_LDO1 OV asserts RSTB and FS0B**
		3	VMON_LDO1 OV asserts RSTB and FS0B
		Reset on power-on reset (POR_FS)	
5 to 4	VMON_LDO1_UV_ FS_REACTION[1:0]	Reaction on RSTB or fail-safe outputs in case of UV detection on VMON_LDO1	
		0	No effect on RSTB and FS0B
		1	**VMON_LDO1 UV asserts FS0B only (default)**
		2	VMON_LDO1 UV asserts RSTB and FS0B
		3	VMON_LDO1 UV asserts RSTB and FS0B
		Reset on power-on reset (POR_FS)	
3 to 2	VMON_LDO2_OV_ FS_REACTION[1:0]	Reaction on RSTB or fail-safe outputs in case of OV detection on VMON_LDO2	
		0	No effect on RSTB and FS0B
		1	VMON_LDO2 OV asserts FS0B only
		2	**VMON_LDO2 OV asserts RSTB and FS0B (default)**
		3	VMON_LDO2 OV asserts RSTB and FS0B
		Reset on power-on reset (POR_FS)	
1 to 0	VMON_LDO2_UV_ FS_REACTION[1:0]	Reaction on RSTB or fail-safe outputs in case of UV detection on VMON_LDO2	
		0	No effect on RSTB and FS0B
		1	**VMON_LDO2 UV asserts FS0B only (default)**
		2	VMON_LDO2 UV asserts RSTB and FS0B
		3	VMON_LDO2 UV asserts RSTB and FS0B
		Reset on power-on reset (POR_FS)	

18.3 FS_I_OVUV_SAFE_REACTION2

Table 74. FS_I_OVUV_SAFE_REACTION2 register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	VMON_EXT_OV_ FS_REACTION[1:0]		VMON_EXT_UV_ FS_REACTION[1:0]		VMON_REF_OV_ FS_REACTION[1:0]		VMON_REF_UV_ FS_REACTION[1:0]	
Read	VMON_EXT_OV_ FS_REACTION[1:0]		VMON_EXT_UV_ FS_REACTION[1:0]		VMON_REF_OV_ FS_REACTION[1:0]		VMON_REF_UV_ FS_REACTION[1:0]	
Reset	1	0	0	1	1	0	0	1

Bit	7	6	5	4	3	2	1	0
Write	VMON_TRK2_OV_ FS_REACTION[1:0]		VMON_TRK2_UV_ FS_REACTION[1:0]		VMON_TRK1_OV_ FS_REACTION[1:0]		VMON_TRK1_UV_ FS_REACTION[1:0]	
Read	VMON_TRK2_OV_ FS_REACTION[1:0]		VMON_TRK2_UV_ FS_REACTION[1:0]		VMON_TRK1_OV_ FS_REACTION[1:0]		VMON_TRK1_UV_ FS_REACTION[1:0]	
Reset	1	0	0	1	1	0	0	1

Go to fail-safe register map

Table 75. FS_I_OVUV_SAFE_REACTION2 register bit description (default)

Bit	Symbol	Value	Description
15 to 14	VMON_EXT_OV_ FS_REACTION[1:0]	Reaction on RSTB or fail-safe outputs in case of OV detection on VMON_EXT	
		0	No effect on RSTB and FS0B
		1	VMON_EXT OV asserts FS0B only
		2	**VMON_EXT OV asserts RSTB and FS0B (default)**
		3	VMON_EXT OV asserts RSTB and FS0B
		Reset on power-on reset (POR_FS)	
13 to 12	VMON_EXT_UV_ FS_REACTION[1:0]	Reaction on RSTB or fail-safe outputs in case of UV detection on VMON_EXT	
		0	No effect on RSTB and FS0B
		1	**VMON_EXT UV asserts FS0B only (default)**
		2	VMON_EXT UV asserts RSTB and FS0B
		3	VMON_EXT UV asserts RSTB and FS0B
		Reset on power-on reset (POR_FS)	
11 to 10	VMON_REF_OV_ FS_REACTION[1:0]	Reaction on RSTB or fail-safe outputs in case of OV detection on VMON_REF	
		0	No effect on RSTB and FS0B
		1	VMON_REF OV asserts FS0B only
		2	**VMON_REF OV asserts RSTB and FS0B (default)**
		3	VMON_REF OV asserts RSTB and FS0B
		Reset on power-on reset (POR_FS)	
9 to 8	VMON_REF_UV_ FS_REACTION[1:0]	Reaction on RSTB or fail-safe outputs in case of UV detection on VMON_REF	
		0	No effect on RSTB and FS0B
		1	**VMON_REF UV asserts FS0B only (default)**
		2	VMON_REF UV asserts RSTB and FS0B
		3	VMON_REF UV asserts RSTB and FS0B
		Reset on power-on reset (POR_FS)	
7 to 6	VMON_TRK2_OV_ FS_REACTION[1:0]	Reaction on RSTB or fail-safe outputs in case of OV detection on VMON_TRK2	
		0	No effect on RSTB and FS0B
		1	VMON_TRK2 OV asserts FS0B only
		2	**VMON_TRK2 OV asserts RSTB and FS0B (default)**
		3	VMON_TRK2 OV asserts RSTB and FS0B
		Reset on power-on reset (POR_FS)	
5 to 4	VMON_TRK2_UV_ FS_REACTION[1:0]	Reaction on RSTB or fail-safe outputs in case of UV detection on VMON_TRK2	
		0	No effect on RSTB and FS0B
		1	**VMON_TRK2 UV asserts FS0B only (default)**
		2	VMON_TRK2 UV asserts RSTB and FS0B
		3	VMON_TRK2 UV asserts RSTB and FS0B
		Reset on power-on reset (POR_FS)	
3 to 2	VMON_TRK1_OV_ FS_REACTION[1:0]	Reaction on RSTB or fail-safe outputs in case of OV detection on VMON_TRK1	
		0	No effect on RSTB and FS0B
		1	VMON_TRK1 OV asserts FS0B only
		2	**VMON_TRK1 OV asserts RSTB and FS0B (default)**
		3	VMON_TRK1 OV asserts RSTB and FS0B
		Reset on power-on reset (POR_FS)	

Table 75. FS_I_OVUV_SAFE_REACTION2 register bit description (default)*...continued*

Bit	Symbol	Value	Description
1 to 0	VMON_TRK1_UV_ FS_REACTION[1:0]	Reaction on RSTB or fail-safe outputs in case of UV detection on VMON_TRK1	
		0	No effect on RSTB and FS0B
		1	**VMON_TRK1 UV asserts FS0B only (default)**
		2	VMON_TRK1 UV asserts RSTB and FS0B
		3	VMON_TRK1 UV asserts RSTB and FS0B
		Reset on power-on reset (POR_FS)	

18.4 FS_I_WD_CFG

Table 76. FS_I_WD_CFG register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	WD_ERR_LIMIT[1:0]		0	WD_RFR_LIMIT[1:0]		0	WD_FS_REACTION[1:0]	
Read	WD_ERR_LIMIT[1:0]		0	WD_RFR_LIMIT[1:0]		0	WD_FS_REACTION[1:0]	
Reset	0	1	0	0	0	0	1	0

Bit	7	6	5	4	3	2	1	0
Write	0	0	0	0	0	0	0	0
Read		WD_RFR_CNT[2:0]			WD_ERR_CNT[3:0]			
Reset	0	0	0	0	0	0	0	0

Go to fail-safe register map

Table 77. FS_I_WD_CFG register bit description

Bit	Symbol	Value	Description
15 to 14	WD_ERR_LIMIT[1:0]	Watchdog error counter configuration	
		0	8
		1	**6 (default)**
		2	4
		3	2
		Reset on power-on reset (POR_FS)	
12 to 11	WD_RFR_LIMIT[1:0]	Watchdog refresh counter configuration	
		0	**6 (default)**
		1	4
		2	2
		3	1
		Reset on power-on reset (POR_FS)	
9 to 8	WD_FS_REACTION[1:0]	Reaction on RSTB or FAIL SAFE output in case of BAD watchdog (data or timing)	
		0	No action on RSTB and FS0B
		1	FS0B only is asserted low if WD Error counter value = WD_ERR_LIMIT[1:0]
		2	**RSTB and FS0B are asserted low if WD_ERR_CNT[3:0] = @WD_ERR_LIMIT[1:0] (default)**
		3	RSTB and FS0B are asserted low if WD_ERR_CNT[3:0] = @WD_ERR_LIMIT[1:0]
		Reset on power-on reset (POR_FS)	

Table 77. FS_I_WD_CFG register bit description*...continued*

Bit	Symbol	Value	Description
6 to 4	WD_RFR_CNT[2:0]	Reflect the value of the Watchdog Refresh Counter	
		0	**0 (default)**
		1	1
		2	2
		3	3
		4	4
		5	5
		6	6
		7	7
		Reset on power-on reset (POR_FS) and on RSTB assertion	
3 to 0	WD_ERR_CNT[3:0]	Reflect the value of the Watchdog Error Counter	
		0h	**0 (default)**
		1h	1
		2h	2
		3h	3
		4h	4
		5h	5
		6h	6
		7h	7
		8h	8
		9h	9
		Ah	10
		Bh	11
		Ch	12
		Dh	12
		Eh	12
		Fh	12
		Reset on power-on reset (POR_FS) and on RSTB assertion	

18.5 FS_I_SAFE_INPUTS

Table 78. FS_I_SAFE_INPUTS register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	FCCU_CFG[2:0]			FCCU12_ FLT_POL	FCCU1_ FLT_POL	FCCU2_ FLT_POL	FCCU12_FS_ REACTION	FCCU1_FS_ REACTION
Read	FCCU_CFG[2:0]			FCCU12_ FLT_POL	FCCU1_ FLT_POL	FCCU2_ FLT_POL	FCCU12_FS_ REACTION	FCCU1_FS_ REACTION
Reset	0	0	1	0	0	0	1	1

Bit	7	6	5	4	3	2	1	0
Write	FCCU2_FS_ REACTION	**0**[1]	ERRMON_ FLT_POLARITY	ERRMON_ACK_TIME[1:0]		ERRMON_FS_ REACTION	FCCU12_FILT[1:0]	
Read	FCCU2_FS_ REACTION	RESERVED	ERRMON_ FLT_POLARITY	ERRMON_ACK_TIME[1:0]		ERRMON_FS_ REACTION	FCCU12_FILT[1:0]	
Reset	1	0	0	0	1	1	0	1

[1] Must be set to 1 in FS_I_NOT_SAFE_INPUTS.

Go to fail-safe register map

Table 79. FS_I_SAFE_INPUTS register bit description

Bit	Symbol	Value	Description
15 to 13	FCCU_CFG[2:0]	FCCU monitoring configuration	
		0	No monitoring
		1	**FCCU1 and FCCU2 inputs monitoring activated by pair (bi-stable protocol) (default)**
		2	FCCU1 and FCCU2 single input monitoring activated
		3	FCCU1 input monitoring only, FCCU2 input not used
		4	FCCU2 input monitoring only, FCCU1 input not used
		5	FCCU1 and FCCU2 single input PWM monitoring activated
		6	FCCU1 input PWM monitoring only, FCCU2 input level monitoring
		7	FCCU2 input PWM monitoring only, FCCU1 input level monitoring
		Reset on power-on reset (POR_FS)	
12	FCCU12_FLT_POL	FCCU12 fault polarity	
		0	**FCCU1_RT = 0 or FCCU2_RT = 1 is a fault (default)**
		1	FCCU1_RT = 1 or FCCU2_RT = 0 is a fault
		Reset on power-on reset (POR_FS)	
11	FCCU1_FLT_POL	FCCU1 fault polarity	
		0	**FCCU1_RT = 0 is a fault (default)**
		1	FCCU1_RT = 1 is a fault
		Reset on power-on reset (POR_FS)	
10	FCCU2_FLT_POL	FCCU2 fault polarity	
		0	**FCCU2_RT = 0 is a fault (default)**
		1	FCCU2_RT = 1 is a fault
		Reset on power-on reset (POR_FS)	
9	FCCU12_FS_REACTION	Reaction on RSTB or fail-safe output in case of FAULT DETECTION ON FCCU12 bit	
		0	FS0B only is asserted low in case of fault on FCCU1 and FCCU2
		1	**RSTB and FS0B only is asserted low in case of fault on FCCU1 and FCCU2 (default)**
		Reset on power-on reset (POR_FS)	
8	FCCU1_FS_REACTION	Reaction on RSTB or fail-safe output in case of FAULT DETECTION ON FCCU1 bit	
		0	FS0B only is asserted low in case of fault on FCCU1 bit
		1	**RSTB and FS0B are asserted low in case of fault on FCCU1 (default)**
		Reset on power-on reset (POR_FS)	
7	FCCU2_FS_REACTION	Reaction on RSTB or fail-safe output in case of FAULT DETECTION ON FCCU2 bit	
		0	FS0B only is asserted low in case of fault on FCCU2 bit
		1	**RSTB and FS0B are asserted low in case of fault on FCCU2 (default)**
		Reset on power-on reset (POR_FS)	
5	ERRMON_FLT_POLARITY	ERRMON fault polarity	
		0	**ERRMON_PIN_STATUS = 0 is a fault after a negative edge transition (default)**
		1	ERRMON_PIN_STATUS = 1 is a fault after a positive edge transition
		Reset on power-on reset (POR_FS)	

Table 79. FS_I_SAFE_INPUTS register bit description...*continued*

Bit	Symbol	Value	Description
4 to 3	ERRMON_ACK_TIME[1:0]	Acknowledge timing following a fault detection on ERRMON	
		0	1 ms
		1	**8 ms (default)**
		2	16 ms
		3	32 ms
		Reset on power-on reset (POR_FS)	
2	ERRMON_FS_REACTION	Reaction on RSTB or fail-safe output in case of fault detection on ERRMON bit	
		0	FS0B only is asserted low in case of fault detection on ERRMON
		1	**RSTB and FS0B are asserted low in case of fault detected on ERRMON (default)**
		Reset on power-on reset (POR_FS)	
1 to 0	FCCU12_FILT[1:0]	FCCU pin filtering time settings	
		0	3 µs
		1	**6 µs (default)**
		2	10 µs
		3	20 µs
		Reset on power-on reset (POR_FS)	

18.6 FS_I_FSSM

Table 80. FS_I_FSSM register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	FLT_ERR_CNT_LIMIT[1:0]		0	FLT_ERR_REACTION[1:0]		0	RSTB_DUR	0
Read	FLT_ERR_CNT_LIMIT[1:0]		RESERVED	FLT_ERR_REACTION[1:0]		RESERVED	RSTB_DUR	RESERVED
Reset	0	1	0	1	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	BACKUP_ SAFETY_ PATH_FS0B	BACKUP_ SAFETY_ PATH_FS1B	**0**[1]	DIS8S	0	0	0	0
Read	BACKUP_ SAFETY_ PATH_FS0B	BACKUP_ SAFETY_ PATH_FS1B	RESERVED	DIS8S	FLT_ERR_CNT[3:0]			
Reset	1	1	0	OTP	0	0	0	1

[1] Must be set to 1 in FS_I_NOT_FSSM.

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Table 81. FS_I_FSSM register bit description

Bit	Symbol	Value	Description
15 to 14	FLT_ERR_CNT_LIMIT[1:0]	Configure the maximum value of the fault counter	
		0	Maximum value = 2
		1	**Maximum value = 6 (default)**
		2	Maximum value = 8
		3	Maximum value = 12
		Reset on power-on reset (POR_FS)	

Table 81. FS_I_FSSM register bit description *...continued*

Bit	Symbol	Value	Description
12 to 11	FLT_ERR_REACTION[1:0]		Configure the RSTB and FS0B behavior when fault error counter ≥ intermediate value
		0	No effect on RSTB and FS0B
		1	FS0B is asserted low if FLT_ERR_CNT[3:0] ≥ intermediate value
		2	**RSTB and FS0B are asserted low if FLT_ERR_CNT[3:0] ≥ intermediate value (default)**
		3	RSTB and FS0B are asserted low if FLT_ERR_CNT[3:0] ≥ intermediate value
			Reset on power-on reset (POR_FS)
9	RSTB_DUR		RSTB low pulse duration t_{RSTB_PULSE} configuration
		0	**10 ms (default)**
		1	1 ms
			Reset on power-on reset (POR_FS)
7	BACKUP_SAFETY_PATH_FS0B		Assert RSTB in case a short to high is detected on FS0B
		0	No assertion of the RSTB
		1	**RSTB assertion (default)**
			Reset on power-on reset (POR_FS)
6	BACKUP_SAFETY_PATH_FS1B		Assert RSTB in case a short to high is detected on FS1B
		0	No assertion of the RSTB
		1	**RSTB assertion (default)**
			Reset on power-on reset (POR_FS)
4	DIS8S		Disable 8 s RSTB timer
		0	**RSTB LOW 8 s counter enabled (default)**
		1	RSTB LOW 8 s Counter disabled
			Reset on power-on reset (POR_FS)
3 to 0	FLT_ERR_CNT[3:0]		Reflect the value of the Fault Error Counter
		0h	0
		1h	**1 (default)**
		2h	2
		3h	3
		4h	4
		5h	5
		6h	6
		7h	7
		8h	8
		9h	9
		Ah	10
		Bh	11
		Ch	12
		Dh	12
			Reset on power-on reset (POR_FS)

18.7 FS_WDW_DURATION

Table 82. FS_WDW_DURATION register bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	WDW_PERIOD[3:0]				0	0	0	WDW_DC[2:0]			0	0	WDW_RECOVERY[3:0]			
Read	WDW_PERIOD[3:0]				RESERVED			WDW_DC[2:0]			RESERVED		WDW_RECOVERY[3:0]			

Table 82. FS_WDW_DURATION register bit allocation*...continued*

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0	0	1	1	0	0	0	0	1	0	0	0	1	0	1	1

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Table 83. FS_WDW_DURATION register bit description

Bit	Symbol	Value	Description
15 to 12	WDW_PERIOD[3:0]	Watchdog window period configuration	
		0h	Infinite open window (can be set during *initialization phase* and *debug mode* only)
		1h	1 ms
		2h	2 ms
		3h	**3 ms (default)**
		4h	4 ms
		5h	6 ms
		6h	8 ms
		7h	12 ms
		8h	16 ms
		9h	24 ms
		Ah	32 ms
		Bh	64 ms
		Ch	128 ms
		Dh	256 ms
		Eh	512 ms
		Fh	1024 ms
		Reset on power-on reset (POR_FS)	
8 to 6	WDW_DC[2:0]	Watchdog window duty cycle	
		0	Closed window : 31.25 % / open window : 68.75 %
		1	Closed window : 37.50 % / open window : 62.50 %
		2	**Closed window : 50 % / open window : 50 % (default)**
		3	Closed window : 62.50 % / open window : 37.50 %
		4	Closed window : 68.75 % / open window : 31.25 %
		5	Closed window : 75 % / open window : 25 %
		6	Closed window : 81.25 % / open window : 18.75 %
		7	Closed window : 50 % / open window : 50 %
		Reset on power-on reset (POR_FS)	

Table 83. FS_WDW_DURATION register bit description...*continued*

Bit	Symbol	Value	Description
3 to 0	WDW_RECOVERY[3:0]	Watchdog window recovery period configuration	
		0h	Infinite open window (can be set during *initialization phase* and *debug mode* only)
		1h	1 ms
		2h	2 ms
		3h	3 ms
		4h	4 ms
		5h	6 ms
		6h	8 ms
		7h	12 ms
		8h	16 ms
		9h	24 ms
		Ah	32 ms
		Bh	**64 ms (default)**
		Ch	128 ms
		Dh	256 ms
		Eh	512 ms
		Fh	1024 ms
		Reset on power-on reset (POR_FS)	

18.8 FS_WD_ANSWER (0x4D)

Table 84. FS_WD_ANSWER register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	WD_ANSWER[15:8]							
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	WD_ANSWER[7:0]							
Reset	0	0	0	0	0	0	0	0

Table 85. FS_WD_ANSWER register bit description

Bit	Symbol	Description
15 to 0	WD_ANSWER[15:0]	Watchdog answer from MCU
		16 bits watchdog answer from the MCU needs to be written here
		Reset on power-on reset (POR_FS)

18.9 FS_WD_TOKEN (0x4E)

Table 86. FS_WD_TOKEN register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	WD_TOKEN[15:8]							
Read	WD_TOKEN[15:8]							
Reset	0	1	0	1	1	0	1	0

Bit	7	6	5	4	3	2	1	0
Write	WD_TOKEN[7:0]							
Read	WD_TOKEN[7:0]							
Reset	1	0	1	1	0	0	1	0

Table 87. FS_WD_TOKEN register bit description

Bit	Symbol	Description
15 to 0	WD_TOKEN[15:0]	WD Token code
		Token value can be written by the MCU here. Default value is 0x5AB2
		Reset on power-on reset (POR_FS)

18.10 FS_ABIST_ON_DEMAND (0x4F)

Table 88. FS_ABIST_ON_DEMAND register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	LAUNCH_ABIST2	0	0	0	0	0	0	0
Read	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	ABIST2_EXT	ABIST2_REF	ABIST2_TRK2	ABIST2_TRK1	ABIST2_LDO2	ABIST2_LDO1	ABIST2_CORE	ABIST2_VPRE
Read	ABIST2_EXT	ABIST2_REF	ABIST2_TRK2	ABIST2_TRK1	ABIST2_LDO2	ABIST2_LDO1	ABIST2_CORE	ABIST2_VPRE
Reset	0	0	0	0	0	0	0	0

Table 89. FS_ABIST_ON_DEMAND register bit description (default value in bold)

Bit	Symbol	Description
15	LAUNCH_ABIST2	Launch ABIST on selected VMONs
		0 No action
		1 ABIST launched
		Reset on power-on reset (POR_FS), Self-clear
7	ABIST2_EXT	Request ABIST on VMON_EXT
		0 No ABIST
		1 ABIST on VMON_EXT Requested
		Reset on power-on reset (POR_FS)
6	ABIST2_REF	Request ABIST on VMON_REF
		0 No ABIST
		1 ABIST on VMON_REF Requested
		Reset on power-on reset (POR_FS)
5	ABIST2_TRK2	Request ABIST on VMON_TRK2
		0 No ABIST
		1 ABIST on VMON_TRK2 Requested
		Reset on power-on reset (POR_FS)

Table 89. FS_ABIST_ON_DEMAND register bit description (default value in bold)...*continued*

Bit	Symbol	Description
4	ABIST2_TRK1	Request ABIST on VMON_TRK1
		0 No ABIST
		1 ABIST on VMON_TRK1 Requested
		Reset on power-on reset (POR_FS)
3	ABIST2_LDO2	Request ABIST on VMON_LDO2
		0 No ABIST
		1 ABIST on VMON_LDO2 Requested
		Reset on power-on reset (POR_FS)
2	ABIST2_LDO1	Request ABIST on VMON_LDO1
		0 No ABIST
		1 ABIST on VMON_LDO1 Requested
		Reset on power-on reset (POR_FS)
1	ABIST2_CORE	Request ABIST on VMON_CORE
		0 No ABIST
		1 ABIST on VMON_CORE Requested
		Reset on power-on reset (POR_FS)
0	ABIST2_VPRE	Request ABIST on VMON_PRE
		0 No ABIST
		1 ABIST on VMON_PRE Requested
		Reset on power-on reset (POR_FS)

18.11 FS_OVUV_REG_STATUS

Table 90. FS_OVUV_REG_STATUS register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	VPRE_OV	VPRE_UV	CORE_OV	CORE_UV	LDO1_OV	LDO1_UV	LDO2_OV	LDO2_UV
Read	VPRE_OV	VPRE_UV	CORE_OV	CORE_UV	LDO1_OV	LDO1_UV	LDO2_OV	LDO2_UV
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	TRK1_OV	TRK1_UV	TRK2_OV	TRK2_UV	REF_OV	REF_UV	EXT_OV	EXT_UV
Read	TRK1_OV	TRK1_UV	TRK2_OV	TRK2_UV	REF_OV	REF_UV	EXT_OV	EXT_UV
Reset	0	0	0	0	0	0	0	0

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Table 91. FS_OVUV_REG_STATUS register bit description

Bit	Symbol	Value	Description
15	VPRE_OV	Overvoltage monitoring on VMON_PRE	
		0	No overvoltage
		1	Overvoltage reported on VMON_PRE
		Reset on power-on reset (POR_FS) or clear on write 1	
14	VPRE_UV	Undervoltage monitoring on VMON_PRE	
		0	No undervoltage
		1	Undervoltage reported on VMON_PRE
		Reset on power-on reset (POR_FS) or clear on write 1	

Table 91. FS_OVUV_REG_STATUS register bit description...*continued*

Bit	Symbol	Value	Description
13	CORE_OV	Overvoltage monitoring on VMON_CORE	
		0	No overvoltage
		1	Overvoltage reported on VMON_CORE
		Reset on power-on reset (POR_FS) or clear on write 1	
12	CORE_UV	Undervoltage monitoring on VMON_CORE	
		0	No undervoltage
		1	Undervoltage reported on VMON_CORE
		Reset on power-on reset (POR_FS) or clear on write 1	
11	LDO1_OV	Overvoltage monitoring on VMON_LDO1	
		0	No overvoltage
		1	Overvoltage reported on VMON_LDO1
		Reset on power-on reset (POR_FS) or clear on write 1	
10	LDO1_UV	Undervoltage monitoring on VMON_LDO1	
		0	No undervoltage
		0	Undervoltage reported on VMON_LDO1
		Reset on power-on reset (POR_FS) or clear on write 1	
9	LDO2_OV	Overvoltage monitoring on VMON_LDO2	
		0	No overvoltage
		1	Overvoltage reported on VMON_LDO2
		Reset on power-on reset (POR_FS) or clear on write 1	
8	LDO2_UV	Undervoltage monitoring on VMON_LDO2	
		0	No undervoltage
		1	Undervoltage reported on VMON_LDO2
		Reset on power-on reset (POR_FS) or clear on write 1	
7	TRK1_OV	Overvoltage monitoring on VMON_TRK1	
		0	No overvoltage
		1	Overvoltage reported on VMON_TRK1
		Reset on power-on reset (POR_FS) or clear on write 1	
6	TRK1_UV	Undervoltage monitoring on VMON_TRK1	
		0	No undervoltage
		1	Undervoltage reported on VMON_TRK1
		Reset on power-on reset (POR_FS) or clear on write 1	
5	TRK2_OV	Overvoltage monitoring on VMON_TRK2	
		0	No overvoltage
		1	Overvoltage reported on VMON_TRK2
		Reset on power-on reset (POR_FS) or clear on write 1	
4	TRK2_UV	Undervoltage Monitoring on VMON_TRK2	
		0	No Undervoltage
		1	Undervoltage reported on VMON_TRK2
		Reset on power-on reset (POR_FS) or clear on write 1	
3	REF_OV	Overvoltage Monitoring on VMON_REF	
		0	No Overvoltage
		1	Overvoltage reported on VMON_REF
		Reset on power-on reset (POR_FS) or clear on write 1	

Table 91. FS_OVUV_REG_STATUS register bit description...*continued*

Bit	Symbol	Value	Description
2	REF_UV	Undervoltage Monitoring on VMON_REF	
		0	No Undervoltage
		1	Undervoltage reported on VMON_REF
		Reset on power-on reset (POR_FS) or clear on write 1	
1	EXT_OV	Overvoltage Monitoring on VMON_EXT	
		0	No Overvoltage
		1	Overvoltage reported on VMON_EXT
		Reset on power-on reset (POR_FS) or clear on write 1	
0	EXT_UV	Undervoltage Monitoring on VMON_EXT	
		0	No Undervoltage
		1	Undervoltage reported on VMON_EXT
		Reset on power-on reset (POR_FS) or clear on write 1	

18.12 FS_RELEASE_FS0B_FS1B (0x51)

Table 92. FS_RELEASE_FS0B_FS1B register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	RELEASE_FS0B_FS1B[15:8]							
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	RELEASE_FS0B_FS1B[7:0]							
Reset	0	0	0	0	0	0	0	0

Table 93. FS_RELEASE_FS0B_FS1B register bit description

Bit	Symbol	Description
15 to 0	RELEASE_FS0B_FS1B[15:0]	Secure 16 bits word to release FS0B and/or FS1B
		Depends on LFSR or WD key (if simple WD used), and FS outputs code
		Reset on power-on reset (POR_FS)

18.13 FS_SAFE_IOS_1

Table 94. FS_SAFE_IOS_1 register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	EXT_RSTB	0	0	RSTB_EVENT	RSTB_DIAG	RSTB_REQ	0	0
Read	EXT_RSTB	RSTB_DRV	RSTB_SNS	RSTB_EVENT	RSTB_DIAG	RESERVED	FS0B_DRV	FS0B_SNS
Reset	0	0	0	1	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	FS0B_DIAG	FS0B_REQ	0	0	FS1B_DIAG	FS1B_REQ	GOTO_INIT	0
Read	FS0B_DIAG	RESERVED	FS1B_DRV	FS1B_SNS	FS1B_DIAG	RESERVED	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

Go to fail-safe register map

Table 95. FS_SAFE_IOS_1 register bit description

Bit	Symbol	Value	Description
15	EXT_RSTB	Report an external reset	
		0	No external reset
		1	External reset
		Reset on power-on reset (POR_FS) or clear on write 1	
14	RSTB_DRV	RSTB driver - digital command	
		0	RSTB driver command sensed low
		1	RSTB driver command sensed high
		Reset on power-on reset (POR_FS)	
13	RSTB_SNS	Sense of RSTB pad	
		0	RSTB pad sensed low
		1	RSTB pad sensed High
		Reset on power-on reset (POR_FS)	
12	RSTB_EVENT	Report a reset event (latched)	
		0	No reset
		1	Reset occurred (reset assertion by device or external reset by MCU)
		Reset on power-on reset (POR_FS) or clear on write 1	
11	RSTB_DIAG	Report a reset short to HIGH	
		0	No failure
		1	Short to high detected
		Reset on power-on reset (POR_FS) or clear on write 1	
10	RSTB_REQ	Request an assertion of reset	
		0	No action
		1	RSTB assertion (pulse)
		Reset on power-on reset (POR_FS), self-clear	
9	FS0B_DRV	FS0B driver - digital command	
		0	FS0B driver command is low
		1	FS0B driver command is high
		Reset on power-on reset (POR_FS)	
8	FS0B_SNS	Sense of FS0B pad	
		0	FS0B pad sensed low
		1	FS0B pad sensed high
		Reset on power-on reset (POR_FS)	
7	FS0B_DIAG	Report a FS0B short to high	
		0	No failure
		1	Short to high detected
		Reset on power-on reset (POR_FS) or clear on write 1	
6	FS0B_REQ	Request an assertion of FS0B	
		0	No action
		1	FS0B assertion
		Reset on power-on reset (POR_FS), self-clear	
5	FS1B_DRV	FS1B driver - digital Command	
		0	FS1B driver command is low
		1	FS1B driver command is high
		Reset on power-on reset (POR_FS)	

Table 95. FS_SAFE_IOS_1 register bit description...*continued*

Bit	Symbol	Value	Description
4	FS1B_SNS	Sense of FS1B pad	
		0	FS1B pad sensed low
		1	FS1B pad sensed high
		Reset on power-on reset (POR_FS)	
3	FS1B_DIAG	Report a FS1B short to high	
		0	No Failure
		1	Short to high detected
		Reset on power-on reset (POR_FS) or clear on write 1	
2	FS1B_REQ	Request an assertion of FS1B	
		0	No action
		1	FS1B assertion
		Reset on power-on reset (POR_FS), self-clear	
1	GOTO_INIT	Go back to *initialization phase* request	
		0	No action
		1	Go back to fail-safe state machine *Safety Initialization Phase* state
		Reset on power-on reset (POR_FS), self-clear	

18.14 FS_SAFE_IOS_2

Table 96. FS_SAFE_IOS_2 register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	0	0	FS1B_TDELAY[4:3]	
Read	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	FS1B_TDELAY[4:3]	
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	FS1B_TDELAY[2:0]			FS1B_TDUR[4:0]				
Read	FS1B_TDELAY[2:0]			FS1B_TDUR[4:0]				
Reset	0	0	0	0	1	0	1	1

Go to fail-safe register map

Table 97. FS_SAFE_IOS_2 register bit description

Bit	Symbol	Value	Description
9 to 5	FS1B_TDELAY[4:0]	FS1B assertion delay t_{DELAY} after assertion of FS0B	
		00h	**FA1B asserted with FS0B - no delay (default)**
		01h	5 ms
		02h	10 ms
		03h	15 ms
		04h	20 ms
		05h	25 ms
		06h	30 ms
		07h	40 ms
		08h	50 ms
		09h	60 ms
		0Ah	80 ms
		0Bh	100 ms
		0Ch	125 ms
		0Dh	150 ms
		0Eh	175 ms
		0Fh	200 ms
		10h	225 ms
		11h	250 ms
		12h	300 ms
		13h	400 ms
		14h	500 ms
		15h	600 ms
		16h	700 ms
		17h	800 ms
		18h	900 ms
		19h	1 s
		1Ah	2 s
		1Bh	4 s
		1Ch	5 s
		1Dh	6 s
		1Eh	8 s
		1Fh	10 s
		Reset on power-on reset (POR_FS)	

Table 97. FS_SAFE_IOS_2 register bit description*...continued*

Bit	Symbol	Value	Description
4 to 0	FS1B_TDUR[4:0]	FS1B assertion pulse duration t_{DUR}	
		00h	No assertion of FS1B
		01h	5 ms
		02h	10 ms
		03h	15 ms
		04h	20 ms
		05h	25 ms
		06h	30 ms
		07h	40 ms
		08h	50 ms
		09h	60 ms
		0Ah	80 ms
		0Bh	**100 ms (default)**
		0Ch	125 ms
		0Dh	150 ms
		0Eh	175 ms
		0Fh	200 ms
		10h	225 ms
		11h	250 ms
		12h	300 ms
		13h	400 ms
		14h	500 ms
		15h	600 ms
		16h	700 ms
		17h	800 ms
		18h	1 s
		19h	2 s
		1Ah	4 s
		1Bh	5 s
		1Ch	6 s
		1Dh	8 s
		1Eh	10 s
		1Fh	Infinite (FS1B released by MCU)
		Reset on power-on reset (POR_FS)	

18.15 FS_DIAG_SAFETY1 (0x54)

Table 98. FS_DIAG_SAFETY1 register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	0	BAD_WD_DATA	BAD_WD_TIMING	0
Read	0	0	0	0	0	BAD_WD_DATA	BAD_WD_TIMING	ABIST1_PASS
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	ABIST2_PASS	ABIST2_DONE	SPI_FS_CLK	SPI_FS_REQ	SPI_FS_CRC	FS_OSC_DRIFT	0	0
Read	ABIST2_PASS	ABIST2_DONE	SPI_FS_CLK	SPI_FS_REQ	SPI_FS_CRC	FS_OSC_DRIFT	LBIST_STATUS[1:0]	
Reset	0	0	0	0	0	0	0	0

Table 99. FS_DIAG_SAFETY1 register bit description

Bit	Symbol	Description
10	BAD_WD_DATA	WD Refresh status - Data
		0 Good WD Refresh
		1 Bad WD refresh, Error in the Data
		Reset on power-on reset (POR_FS) or clear on Write (write '1')
9	BAD_WD_TIMING	WD Refresh status - Timing
		0 Good WD Refresh
		1 Bad WD refresh, Error in the Timing (window)
		Reset on power-on reset (POR_FS) or clear on Write (write '1')
8	ABIST1_PASS	Diagnostic on ABIST 1
		0 ABIST1 Fail or not executed
		1 ABIST 1 Pass
		Reset on power-on reset (POR_FS)
7	ABIST2_PASS	Report ABIST2 status
		0 ABIST2 Fail or not executed
		1 ABIST2 Pass
		Reset on power-on reset (POR_FS) or clear on Write (write '1')
6	ABIST2_DONE	Diagnostic on ABIST2 on Demand
		0 ABIST2 not finished
		1 ABIST2 done
		Reset on power-on reset (POR_FS) or clear on Write (write '1')
5	SPI_FS_CLK	FS SPI SCLK Error detection
		0 No Error
		1 Wrong number of CLK Cycles < 32 or > 32
		Reset on power-on reset (POR_FS) or clear on Write (write '1')
4	SPI_FS_REQ	Invalid FS SPI access (wrong write or read, Write to INIT registers in normal mode, or Wrong address)
		0 No Error
		1 SPI Violation
		Reset on power-on reset (POR_FS) or clear on Write (write '1')
3	SPI_FS_CRC	FS SPI communication error - CRC
		0 No Error
		1 Error detected in the CRC
		Reset on power-on reset (POR_FS) or clear on Write (write '1')
2	FS_OSC_DRIFT	Drift of the Fail Safe Oscillator
		0 No Drift
		1 Oscillator Drift
		Reset on power-on reset (POR_FS) or clear on Write (write '1')

Table 99. FS_DIAG_SAFETY1 register bit description...*continued*

Bit	Symbol	Description
1 to 0	LBIST_STATUS[1:0]	LBIST Status (MSB = LBIST_CHK_PAT_OK, LSB = LBIST_CHECKER_OK)
		00 Reserved (Not used)
		01 LBIST BYPASSED
		10 LBIST FAIL
		11 LBIST OK
		Reset on power-on reset (POR_FS)

18.16 FS_DIAG_SAFETY2

Table 100. FS_DIAG_SAFETY2 register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	0	0	0	0
Read	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	FCCU12	FCCU1	FCCU2	0	0	ERRMON_ACK	ERRMON	0
Read	FCCU12	FCCU1	FCCU2	FCCU1_RT	FCCU2_RT	RESERVED	ERRMON	ERRMON_ PIN_STATUS
Reset	0	0	0	0	0	0	0	0

Go to fail-safe register map

Table 101. FS_DIAG_SAFETY2 register bit description

Bit	Symbol	Value	Description
7	FCCU12	Report an error in the FCCU1,2 if FCCU_CFG[2:0] = 1	
		0	No error
		1	Error detected
		Reset on power-on reset (POR_FS) or clear on write 1	
6	FCCU1	Report an error in the FCCU1 input	
		0	No error
		1	Error detected
		Reset on power-on reset (POR_FS) or clear on write 1	
5	FCCU2	Report an error in the FCCU2 input	
		0	No error
		1	Error detected
		Reset on power-on reset (POR_FS) or clear on write 1	
4	FCCU1_RT	Sense of FCCU1 pin	
		0	FCCU1 low (V_{IL_FCCU})
		1	FCCU1 high (V_{IH_FCCU})
		Reset on power-on reset (POR_FS), real time value	

Table 101. FS_DIAG_SAFETY2 register bit description...*continued*

Bit	Symbol	Value	Description
3	FCCU2_RT	Sense of FCCU2 pin	
		0	FCCU2 low (V_{IL_FCCU})
		1	FCCU2 high (V_{IH_FCCU})
		Reset on power-on reset (POR_FS), real time value	
2	ERRMON_ACK	Acknowledge ERRMON failure timer	
		0	No effect
		1	MCU acknowledge ERRMON (WAKE2 pin) failure detection, timer is disabled, see ERRMON_ACK_TIME[1:0]
		Reset on power-on reset (POR_FS), self-clear	
1	ERRMON	Report an error in the ERRMON (WAKE2 pin) input	
		0	No error
		1	Error detected
		Reset on power-on reset (POR_FS) or clear on write 1	
0	ERRMON_PIN_STATUS	Report ERRMON (WAKE2 pin) pin status	
		0	Low level (V_{IL_WAKEx})
		1	High level (V_{IH_WAKEx})
		Reset on power-on reset (POR_FS), real time value	

18.17 FS_INTB_MASK

Table 102. FS_INTB_MASK register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	VPRE_M	CORE_M	LDO1_M	LDO2_M	TRK1_M	TRK2_M	REF_M	EXT_M
Read	VPRE_M	CORE_M	LDO1_M	LDO2_M	TRK1_M	TRK2_M	REF_M	EXT_M
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	FCCU1_M	FCCU2_M	BAD_WD_M	ERRMON_M	0	0	0	0
Read	FCCU1_M	FCCU2_M	BAD_WD_M	ERRMON_M	RESERVED	RESERVED	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

Go to fail-safe register map

Table 103. FS_INTB_MASK register bit description

Bit	Symbol	Value	Description
15	VPRE_M	Inhibit interrupt (INTB pulse) related to VMON_PRE event (VPRE_OV and VPRE_UV)	
		0	**Interrupt not masked (default)**
		1	Interrupt masked
		Reset on power-on reset (POR_FS)	
14	CORE_M	Inhibit interrupt (INTB pulse) related to VMON_CORE event (CORE_OV and CORE_UV)	
		0	**Interrupt not masked (default)**
		1	Interrupt masked
		Reset on power-on reset (POR_FS)	

Table 103. FS_INTB_MASK register bit description*...continued*

Bit	Symbol	Value	Description
13	LDO1_M	Inhibit interrupt (INTB pulse) related to VMON_LDO1 event (LDO1_OV and LDO1_UV)	
		0	**Interrupt not masked (default)**
		1	Interrupt masked
		Reset on power-on reset (POR_FS)	
12	LDO2_M	Inhibit interrupt (INTB pulse) related to VMON_LDO2 event (LDO2_OV and LDO2_UV)	
		0	**Interrupt not masked (default)**
		1	Interrupt masked
		Reset on power-on reset (POR_FS)	
11	TRK1_M	Inhibit interrupt (INTB pulse) related to VMON_TRK1 event (TRK1_OV and TRK1_UV)	
		0	**Interrupt not masked (default)**
		1	Interrupt masked
		Reset on power-on reset (POR_FS)	
10	TRK2_M	Inhibit interrupt (INTB pulse) related to VMON_TRK2 event (TRK2_OV and TRK2_UV)	
		0	**Interrupt not masked (default)**
		1	Interrupt masked
		Reset on power-on reset (POR_FS)	
9	REF_M	Inhibit interrupt (INTB pulse) related to VMON_REF event (REF_OV and REF_UV)	
		0	**Interrupt not masked (default)**
		1	Interrupt masked
		Reset on power-on reset (POR_FS)	
8	EXT_M	Inhibit interrupt (INTB pulse) related to VMON_EXT event (EXT_OV and EXT_UV)	
		0	**Interrupt not masked (default)**
		1	Interrupt masked
		Reset on power-on reset (POR_FS)	
7	FCCU1_M	Inhibit interrupt (INTB pulse) related to FCCU1 bit, and FCCU12 bit if FCCU_CFG[2:0] = 1	
		0	**Interrupt not masked (default)**
		1	Interrupt masked
		Reset on power-on reset (POR_FS)	
6	FCCU2_M	Inhibit interrupt (INTB pulse) related to FCCU2 bit, and FCCU12 bit if FCCU_CFG[2:0] = 1	
		0	**Interrupt not masked (default)**
		1	Interrupt masked
		Reset on power-on reset (POR_FS)	
5	BAD_WD_M	Inhibit interrupt (INTB pulse) related to bad watchdog refresh (BAD_WD_DATA or BAD_WD_TIMING)	
		0	**Interrupt not masked (default)**
		1	Interrupt masked
		Reset on power-on reset (POR_FS)	
4	ERRMON_M	Inhibit interrupt (INTB pulse) related to ERRMON bit	
		0	**Interrupt not masked (default)**
		1	Interrupt masked
		Reset on power-on reset (POR_FS)	

18.18 FS_STATES (0x57)

Table 104. FS_STATES register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	EXIT_DBG_MODE	0	OTP_ CORRUPT	REG_ CORRUPT	0	0	0
Read	0	0	DBG_MODE	OTP_ CORRUPT	REG_ CORRUPT	0	0	0
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	0	0	0	0	0	0	0	0
Read	0	0	0	FS_STATES				
Reset	0	0	0	0	0	0	0	0

Table 105. FS_STATES register bit description

Bit	Symbol	Description
14	EXIT_DBG_MODE	Leave Debug Mode
		0 No action
		1 Leave Debug mode
		Reset on power-on reset (POR_FS), Self-clear
13	DBG_MODE	DEBUG MODE Status
		0 Not in DEBUG MODE
		1 In DEBUG MODE
		Reset on power-on reset (POR_FS)
12	OTP_CORRUPT	OTP bits corruption detection (5 ms cyclic check)
		0 No OTP content CRC error Detected
		1 OTP Content CRC error detected
		Reset on power-on reset (POR_FS) or clear on Write (write '1')
11	REG_CORRUPT	INIT Register Corruption detection
		0 No corruption detected in init registers (i.e. no mismatch between register/register_NOT) pair
		1 Data content corruption detected in init registers (i.e. mismatch between register/register_NOT) pair
		Reset on power-on reset (POR_FS) or clear on Write (write '1')
4 to 0	FS_STATES	Actual Sate of the Fail Safe State machine
		00100 Debug entry
		00110 Enable Monitoring
		01000 RSTB Release
		01001 Init FS
		01010 Safety Outputs not released
		01011 Normal
		Reset on power-on reset (POR_FS)

18.19 FS_LP_REQ

Table 106. FS_LP_REQ register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	0	0	0	0
Read	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	STBY_WAKE_UP
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	FS_LP_REQ[7:0]							
Read	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

Go to fail-safe register map

Table 107. FS_LP_REQ register bit description

Bit	Symbol	Value	Description
8	STBY_WAKE_UP	Wake up source	
		0	Wake-up from POR_FS or wake-up from *LPOFF mode*
		1	Wake-up from *standby mode*
		Reset on power-on reset (POR_FS)	
7 to 0	FS_LP_REQ[7:0]	Low power command	
		A5h	Transition to Pre-LPOFF mode
		5Ah	Transition to *LPOFF mode* / Fail-safe off
		AAh	Transition to Pre-standby mode
		55h	Transition to *standby mode* / Fail-safe off
		Reset on power-on reset (POR_FS)	

18.20 FS_LDT_LPSEL

Table 108. FS_LDT_LPSEL register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	0	0	0	0
Read	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	LDT_LPSEL[7:0]							
Read	LDT_LPSEL[7:0]							
Reset	0	0	0	0	0	0	0	0

Go to fail-safe register map

Table 109. FS_LDT_LPSEL register bit description

Bit	Symbol	Value	Description
7 to 0	LDT_LPSEL[7:0]	Low power command	
		A5h	Transition to go to *LPOFF mode* when LDT_EN = 1
		AAh	Transition to go to *standby mode* when LDT_EN = 1
		Reset on power-on reset (POR_FS)	

19 OTP bits description

19.1 Main OTP overview

Table 110. Main OTP configuration map

Register Name	ADDRESS	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
OTP_SYS_CFG1	20	RETRY_MSK_OTP[3:0]				RETRY_MODE_OTP	RETRY_DIS_OTP	WK1DFS_DIS_OTP	VSUP_UVTH_OTP
OTP_SYS_CFG2	21	MDFS_DIS_OTP	CLK_FREQ_OTP[1:0]		SLOT_BYP_OTP[2:0]			TSLOT_OTP[1:0]	
OTP_SYS_CFG3	22	GPIO2_VCORE_PGOOD_OTP	GPIO2_MODE_OTP	GPIO1_MODE_OTP	VREF_PLIFT_DIS_OTP	LDO2_PLIFT_DIS_OTP	LDO1_PLIFT_DIS_OTP	BOS_IN_OTP[1:0]	
OTP_VBST_CFG1	23	VBST_MAX_DC_OTP[1:0]		—	VBSTLS_SR_OTP	VBST_PH_OTP[1:0]		VBST_OV_OTP	VBST_CFG_OTP
OTP_VBST_CFG2	24	VBST_TON_MIN_OTP[1:0]		VBST_RCOMP_OTP[1:0]		VBST_CCOMP_OTP[1:0]		VBST_GMCOMP_OTP[1:0]	
OTP_VBST_CFG3	25	VBST_ILIM_OTP[1:0]		VBST_SC_OTP[5:0]					
OTP_VBST_VOLT	26	VBST_SS_OTP[1:0]		—	VBST_OTP[4:0]				
OTP_VPRE_CFG1	27	VPRE_OC_OTP[2:0]			VPRE_SR_OTP	VPRE_PH_OTP[1:0]		VPRE_SS_OTP[1:0]	
OTP_VPRE_CFG2	28	—	VPRE_RCOMP_OTP[2:0]			VPRE_CCOMP_OTP[1:0]		VPRE_GM_OTP[1:0]	
OTP_VPRE_CFG3	29	VPRE_OC_DGLT_OTP[1:0]		VPRE_SC_OTP[5:0]					
OTP_VPRE_CFG4	2A	VPRETSD_PD_OTP	VPRETDFS_OTP	VPRE_CLK_OTP	—	VPRE_PFM_TOFF_OTP[1:0]		VPRE_PFM_TON_OTP[1:0]	
OTP_VPRE_VOLT1	2B	—		VPRE_OTP[5:0]					
OTP_VPRE_VOLT2	2C	VPRE_LP_DVS_OTP[1:0]		VPRE_LP_OTP[5:0]					
OTP_VPRE_VOLT3	2D	VPRE_PDWN_DLY_OTP[1:0]		VPRE_BOS_OTP[5:0]					
OTP_CORE_CFG1	2E	—		COREHS_SR_OTP[1:0]		CORE_PH_OTP[1:0]		CORE_ILIM_OTP[1:0]	
OTP_CORE_CFG2	2F	—		CORE_RCOMP_OTP[1:0]		CORE_CCOMP_OTP[1:0]		CORE_GM_OTP[1:0]	
OTP_CORE_CFG3	30	—		CORE_SS_OTP[1:0]		0	CORE_CTRL_OTP	CORE_LSEL_OTP[1:0]	
OTP_CORE_VOLT1	31	VCORE_OTP[7:0]							
OTP_CORE_CFG5	32	CORETSD_PD_OTP	CORETDFS_OTP	—			CORE_SLOT_OTP[2:0]		
OTP_LDO1_CFG	33	LDO1TSD_PD_OTP	LDO1 TDFS_OTP	LDO1_LP_EN_OTP	VLDO1_LP_OTP	VLDO1_OTP	LDO1_SLOT_OTP[2:0]		
OTP_LDO2_CFG	34	LDO2TSD_PD_OTP	LDO2 TDFS_OTP	LDO2_LP_EN_OTP	VLDO2_LP_OTP	VLDO2_OTP	LDO2_SLOT_OTP[2:0]		
OTP_TRK1_CFG	35	TRK1TSD_PD_OTP	TRK1 TDFS_OTP	TRK1_SEL_OTP[1:0]		—	TRK1_SLOT_OTP[2:0]		
OTP_TRK2_CFG	36	TRK2TSD_PD_OTP	TRK2 TDFS_OTP	TRK2_SEL_OTP[1:0]		—	TRK2_SLOT_OTP[2:0]		
OTP_VREF_CFG	37	—		VLDO_REF_OTP[1:0]		VREF_OTP	VREF_SLOT_OTP[2:0]		
OTP_GPIO1_CFG	38	GPIO1TSD_PD_OTP	GPIO1 PD_OTP	GPIO1 PU_OTP	GPIO1STAGE_OTP[1:0]		GPIO1_SLOT_OTP[2:0]		

Table 110. Main OTP configuration map *...continued*

Register Name	ADDRESS	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
OTP_ GPIO2_CFG	39	—	GPIO2 PD_OTP	GPIO2 PU_OTP	GPIO2STAGE_OTP[1:0]		GPIO2_SLOT_OTP[2:0]		
OTP_ INPUT_CFG	3A	WK2PD_ SEL_OTP	WK1PD_ SEL_OTP	GPIO2 TH_OTP	GPIO1TH_OTP	WK2PD_OTP	WK1PD_OTP	WK2 TH_OTP	WK1 TH_OTP
OTP_ PROG_IDH	3B	PROG_IDH_OTP[7:0]							
OTP_ PROG_IDL	3C	PROG_IDL_OTP[7:0]							

19.2 Main OTP registers bit description

Table 111. OTP_SYS_CFG1 register bit description

Bit	Bit Group Name	Description	Value	Settings
7 to 4	RETRY_MSK_OTP[3:0]	Retry counter time limit	1h	200 ms
			2h	400 ms
			3h	800 ms
			4h	1600 ms
			5h	3200 ms
			6h	6400 ms
			7h	12800 ms
			8h	25600 ms
			9h	51200 ms
			Ah	102400 ms
			Bh	204800 ms
			Ch	409600 ms
			Dh	819200 ms
			Eh	1638400 ms
			Fh	3276800 ms
3	RETRY_MODE_OTP	Auto-retry mode	0	Limited retry
			1	Infinite retry
2	RETRY_DIS_OTP	Auto-retry power up from DFS	0	Enabled
			1	Disabled
1	WK1DFS_DIS_OTP	Exit DFS on WAKE1 event	0	Enabled
			1	Disabled
0	VSUP_UVTH_OTP	VSUP UV threshold V_{SUP_UVL} / V_{SUP_UVH}	0	4.3 V / 4.8 V
			1	5.65 V / 6.1 V

Go to main OTP register map

Table 112. OTP_SYS_CFG2 register bit description

Bit	Bit Group Name	Description	Value	Settings
7	MDFS_DIS_OTP	Disable *Deep Fail Safe* entry	0	DFS entry enabled
			1	DFS entry disabled
6 to 5	CLK_FREQ_OTP[1:0]	Clock frequency selection F_{OSC_HIGH}	0	16 MHz
			1	17 MHz
			2	18 MHz
			3	19 MHz

Table 112. OTP_SYS_CFG2 register bit description*...continued*

Bit	Bit Group Name	Description	Value	Settings
4 to 2	SLOT_BYP_OTP[2:0]	Power-up slot bypass	0	Bypass disabled
			1	Bypass slot 1 to 6
			2	Bypass slot 2 to 6
			3	Bypass slot 3 to 6
			4	Bypass slot 4 to 6
			5	Bypass slot 5 to 6
			6	Bypass slot 6
			7	Bypass disabled
1 to 0	TSLOT_OTP[1:0]	Power up slot time	0	250 µs
			1	500 µs
			2	1000 µs
			3	2000 µs

Go to main OTP register map

Table 113. OTP_SYS_CFG3 register bit description

Bit	Bit Group Name	Description	Value	Settings
7	GPIO2_VCORE_PGOOD_OTP	GPIO2 VCORE_PGOOD	0	GPIO2 is not driven by VCORE_PGOOD
			1	GPIO2 is driven by VCORE_PGOOD
6	GPIO2_MODE_OTP	GPIO2 Low Side polarity	0	GPIO2 LS active high
			1	GPIO2 LS active low
5	GPIO1_MODE_OTP	GPIO1 Low Side polarity	0	GPIO1 LS active high
			1	GPIO1 LS active low
4	VREF_PLIFT_DIS_OTP	VREF pin lift detection	0	VREF pin lift detection enabled
			1	VREF pin lift detection disabled
3	LDO2_PLIFT_DIS_OTP	LDO2 pin lift detection	0	LDO2 pin lift detection enabled
			1	LDO2 pin lift detection disabled
2	LDO1_PLIFT_DIS_OTP	LDO1 pin lift detection	0	LDO1 pin lift detection enabled
			1	LDO1 pin lift detection disabled
1 to 0	BOS_IN_OTP[1:0]	BOS input selection	0	Auto Transition from VPRE to VSUP when $V_{PRE} < V_{PRE\_UVBOS}$
			1	Force BOS input to VSUP always

Go to main OTP register map

Table 114. OTP_VBST_CFG1 register bit description

Bit	Bit Group Name	Description	Value	Settings
7 to 6	VBST_MAX_DC_OTP[1:0]	VBST maximum duty cycle DC_{BST_MAX}	0	72.5 %
			1	77.5 %
			2	82.5 %
			3	87.5 %
4	VBSTLS_SR_OTP	VBST low-side slew rate I_{BSTG}	0	PU = 2 Ω / PD = 1.7 Ω
			1	PU = 1.5 Ω / PD = 1.0 Ω
3 to 2	VBST_PH_OTP[1:0]	VBST phase delay	0	No delay
			1	1 clock cycle
			2	2 clock cycles
			3	3 clock cycles

Table 114. OTP_VBST_CFG1 register bit description*...continued*

Bit	Bit Group Name	Description	Value	Settings
1	VBST_OV_OTP	VBST_FB OV monitor mode	0	Auto-enable mode
			1	Overvoltage protection mode
0	VBST_CFG_OTP	VBST configuration	0	Front-end boost
			1	Back-end boost

Go to main OTP register map

Table 115. OTP_VBST_CFG2 register bit description

Bit	Bit Group Name	Description	Value	Settings
7 to 6	VBST_TON_MIN_OTP[1:0]	VBST minimum on time t_{ON_MIN}	0	200 ns
5 to 4	VBST_RCOMP_OTP[1:0]	VBST comp resistance	0	1000 kΩ
			1	740 kΩ
			2	500 kΩ
			3	250 kΩ
3 to 2	VBST_CCOMP_OTP[1:0]	VBST comp capacitor	0	200 pF
			1	150 pF
			2	100 pF
			3	50 pF
1 to 0	VBST_GMCOMP_OTP[1:0]	VBST comp transconductance	0	3.9 µS
			1	5.1 µS
			2	7.7 µS
			3	15.3 µS

Go to main OTP register map

Table 116. OTP_VBST_CFG3 register bit description

Bit	Bit Group Name	Description	Value	Settings
7 to 6	VBST_ILIM_OTP[1:0]	VBST current limit $V_{BST\_ILIM\_TH}$ / R_{SNS_BST}	0	60 mV / R_{SNS_BST}
			1	120 mV / R_{SNS_BST}
			2	150 mV / R_{SNS_BST}
			3	180 mV / R_{SNS_BST}
5 to 0	VBST_SC_OTP[5:0]	VBST slope compensation	00h	0 mV/µs
			01h	14 mV/µs
			02h	28 mV/µs
			03h	42 mV/µs
			04h	56 mV/µs
			05h	70 mV/µs
			06h	84 mV/µs
			07h	99 mV/µs
			08h	113 mV/µs
			09h	127 mV/µs
			0Ah	141 mV/µs
			0Bh	155 mV/µs
			0Ch	169 mV/µs
			0Dh	183 mV/µs
			0Eh	197 mV/µs
			0Fh	211 mV/µs

Table 116. OTP_VBST_CFG3 register bit description*...continued*

Bit	Bit Group Name	Description	Value	Settings
			10h	225 mV/μs
			11h	239 mV/μs
			12h	253 mV/μs
			13h	268 mV/μs
			14h	282 mV/μs
			15h	296 mV/μs
			16h	310 mV/μs
			17h	324 mV/μs
			18h	338 mV/μs
			19h	352 mV/μs
			1Ah	366 mV/μs
			1Bh	380 mV/μs
			1Ch	394 mV/μs
			1Dh	408 mV/μs
			1Eh	422 mV/μs
			1Fh	436 mV/μs
			20h	451 mV/μs
			21h	465 mV/μs
			22h	479 mV/μs
			23h	493 mV/μs
			24h	507 mV/μs
			25h	521 mV/μs
			26h	535 mV/μs
			27h	549 mV/μs
			28h	563 mV/μs
			29h	577 mV/μs
			2Ah	591 mV/μs
			2Bh	605 mV/μs
			2Ch	620 mV/μs
			2Dh	634 mV/μs
			2Eh	648 mV/μs
			2Fh	662 mV/μs
			30h	676 mV/μs
			31h	690 mV/μs
			32h	704 mV/μs
			33h	718 mV/μs
			34h	732 mV/μs
			35h	746 mV/μs
			36h	760 mV/μs
			37h	774 mV/μs
			38h	788 mV/μs
			39h	803 mV/μs
			3Ah	817 mV/μs
			3Bh	831 mV/μs
			3Ch	845 mV/μs

Table 116. OTP_VBST_CFG3 register bit description*...continued*

Bit	Bit Group Name	Description	Value	Settings
			3Dh	859 mV/µs
			3Eh	873 mV/µs
			3Fh	887 mV/µs

Go to main OTP register map

Table 117. OTP_VBST_VOLT register bit description

Bit	Bit Group Name	Description	Value	Settings
7 to 6	VBST_SS_OTP[1:0]	VBST soft start t_{BST_SS}	0	425 µs
			1	850 µs
			2	1.7 ms
			3	3.4 ms
4 to 0	VBST_OTP[4:0]	VBST voltage V_{BST}	00h	5.00 V
			01h	5.25 V
			02h	5.50 V
			03h	5.75 V
			04h	6.00 V
			05h	6.25 V
			06h	6.50 V
			07h	6.75 V
			08h	7.00 V
			09h	7.50 V
			0Ah	8.00 V
			0Bh	8.50 V
			0Ch	9.00 V
			0Dh	9.50 V
			0Eh	10.0 V
			0Fh	10.5 V
			10h	11.0 V
			11h	11.5 V
			12h	12.0 V
			13h	12.5 V
			14h	13.0 V
			15h	13.5 V
			16h	14.0 V
			17h	14.5 V
			18h	15.0 V
			19h	15.5 V
			1Ah	16.0 V
			1Bh	16.5 V
			1Ch	17.0 V
			1Dh	17.5 V
			1Eh	18.0 V
			1Fh	18.0 V

Go to main OTP register map

Table 118. OTP_VPRE_CFG1 register bit description

Bit	Bit Group Name	Description	Value	Settings
7 to 5	VPRE_OC_OTP[2:0]	VPRE overcurrent flag $I_{PRE\_OC\_FLAG}$	0	0.66 A
			1	0.88 A
			2	1.1 A
			3	1.32 A
			4	1.54 A
			5	1.76 A
			6	1.98 A
			7	2.2 A
4	VPRE_SR_OTP	VPRE LX slew rate t_{PRESW_SLR}	0	2 ns - Fast mode
			1	4 ns - Slow mode
3 to 2	VPRE_PH_OTP[1:0]	VPRE phase delay	0	No delay
			1	1 clock cycle
			2	2 clock cycles
			3	3 clock cycles
1 to 0	VPRE_SS_OTP[1:0]	VPRE soft start t_{PRE_SS}	0	269 µs
			1	538 µs
			2	1077 µs
			3	2150 µs

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Table 119. OTP_VPRE_CFG2 register bit description

Bit	Bit Group Name	Description	Value	Settings
6 to 4	VPRE_RCOMP_OTP[2:0]	VPRE comp resistance	0	1300 kΩ
			1	1137 kΩ
			2	975 kΩ
			3	812 kΩ
			4	650 kΩ
			5	512 kΩ
			6	325 kΩ
			7	162 kΩ
3 to 2	VPRE_CCOMP_OTP[1:0]	VPRE comp capacitor	0	12.0 pF
			1	23.0 pF
			2	33.5 pF
			3	44.5 pF
1 to 0	VPRE_GM_OTP[1:0]	VPRE transconductance amp	0	10 µS
			1	15 µS
			2	20 µS
			3	25 µS

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Table 120. OTP_VPRE_CFG3 register bit description

Bit	Bit Group Name	Description	Value	Settings
7 to 6	VPRE_OC_DGLT_OTP[1:0]	VPRE overcurrent deglitch	0	250 μs
			1	500 μs
			2	1000 μs
			3	2000 μs
5 to 0	VPRE_SC_OTP[5:0]	VPRE slope compensation	2Ah	279 mV/μs
			2Bh	266 mV/μs
			2Ch	254 mV/μs
			2Dh	241 mV/μs
			2Eh	228 mV/μs
			2Fh	214 mV/μs
			30h	201 mV/μs
			31h	189 mV/μs
			32h	176 mV/μs
			33h	163 mV/μs

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Table 121. OTP_VPRE_CFG4 register bit description

Bit	Bit Group Name	Description	Value	Settings
7	VPRETSD_PD_OTP	VPRE TSD pull-down	0	pull-down enabled in TSD
6	VPRETDFS_OTP	VPRE TSD behavior Default value of VPRETDFS	0	VPRE disabled only
			1	Go to DFS
5	VPRE_CLK_OTP	VPRE clock selection F_{PRE}	0	F_{OSC_HIGH} / 40
			1	F_{OSC_HIGH} / 8
3 to 2	VPRE_PFM_TOFF_OTP[1:0]	VPRE high-side minimum off time in PFM $t_{PRE\_OFF\_MIN}$	2	720 ns
1 to 0	VPRE_PFM_TON_OTP[1:0]	VPRE high-side minimum on time in PFM $t_{PRE\_ON\_MIN\_450K}$ / $t_{PRE\_ON\_MIN\_2M2}$	0	900 ns / 440 ns
			1	1000 ns / 500 ns
			2	1125 ns / 550 ns
			3	1250 ns / 600 ns

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Table 122. OTP_VPRE_VOLT1 register bit description

Bit	Bit Group Name	Description	Value	Settings
5 to 0	VPRE_OTP[5:0]	VPRE output voltage in *normal mode* V_{PRE_PWM}	0Ah	3.70 V
			0Bh	3.75 V
			0Ch	3.80 V
			0Dh	3.85 V
			0Eh	3.90 V
			0Fh	3.95 V
			10h	4.00 V
			11h	4.05 V
			12h	4.10 V
			13h	4.15 V
			14h	4.20 V
			15h	4.25 V

Table 122. OTP_VPRE_VOLT1 register bit description*...continued*

Bit	Bit Group Name	Description	Value	Settings
			16h	4.30 V
			17h	4.35 V
			18h	4.40 V
			19h	4.45 V
			1Ah	4.50 V
			1Bh	4.55 V
			1Ch	4.60 V
			1Dh	4.65 V
			1Eh	4.70 V
			1Fh	4.75 V
			20h	4.80 V
			21h	4.85 V
			22h	4.90 V
			23h	4.95 V
			24h	5.00 V
			25h	5.05 V
			26h	5.10 V
			27h	5.15 V
			28h	5.20 V
			29h	5.25 V
			2Ah	5.30 V
			2Bh	5.35 V
			2Ch	5.40 V
			2Dh	5.45 V
			2Eh	5.50 V
			2Fh	5.55 V
			30h	5.60 V
			31h	5.65 V
			32h	5.70 V
			33h	5.75 V
			34h	5.80 V
			35h	5.85 V
			36h	5.90 V
			37h	5.95 V
			38h	6.00 V
			39h	6.05 V
			3Ah	6.10 V
			3Bh	6.15 V
			3Ch	6.20 V
			3Dh	6.25 V
			3Eh	6.30 V
			3Fh	6.35 V

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Table 123. OTP_VPRE_VOLT2 register bit description

Bit	Bit Group Name	Description	Value	Settings
7 to 6	VPRE_LP_DVS_OTP[1:0]	VPRE DVS ramp rate $V_{PRE\_DVS\_DOWN}$	0	22 mV/µs
			1	11 mV/µs
			2	5.5 mV/µs
			3	2.75 mV/µs
5 to 0	VPRE_LP_OTP[5:0]	VPRE output voltage in *standby mode* V_{PRE_PFM}	0Ah	3.70 V
			0Bh	3.75 V
			0Ch	3.80 V
			0Dh	3.85 V
			0Eh	3.90 V
			0Fh	3.95 V
			10h	4.00 V
			11h	4.05 V
			12h	4.10 V
			13h	4.15 V
			14h	4.20 V
			15h	4.25 V
			16h	4.30 V
			17h	4.35 V
			18h	4.40 V
			19h	4.45 V
			1Ah	4.50 V
			1Bh	4.55 V
			1Ch	4.60 V
			1Dh	4.65 V
			1Eh	4.70 V
			1Fh	4.75 V
			20h	4.80 V
			21h	4.85 V
			22h	4.90 V
			23h	4.95 V
			24h	5.00 V
			25h	5.05 V
			26h	5.10 V
			27h	5.15 V
			28h	5.20 V
			29h	5.25 V
			2Ah	5.30 V
			2Bh	5.35 V

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Table 124. OTP_VPRE_VOLT3 register bit description

Bit	Bit Group Name	Description	Value	Settings
7 to 6	VPRE_PDWN_DLY_OTP[1:0]	VPRE power down delay	0	100 μs
			1	1 ms
			2	2 ms
			3	5 ms
5 to 0	VPRE_BOS_OTP[5:0]	VPRE transition voltage	0Ah	3.70 V
			0Bh	3.75 V
			0Ch	3.80 V
			0Dh	3.85 V
			0Eh	3.90 V
			0Fh	3.95 V
			10h	4.00 V
			11h	4.05 V
			12h	4.10 V
			13h	4.15 V
			14h	4.20 V
			15h	4.25 V
			16h	4.30 V
			17h	4.35 V
			18h	4.40 V
			19h	4.45 V
			1Ah	4.50 V
			1Bh	4.55 V
			1Ch	4.60 V
			1Dh	4.65 V
			1Eh	4.70 V
			1Fh	4.75 V
			20h	4.80 V
			21h	4.85 V
			22h	4.90 V
			23h	4.95 V
			24h	5.00 V
			25h	5.05 V
			26h	5.10 V
			27h	5.15 V
			28h	5.20 V
			29h	5.25 V
			2Ah	5.30 V
			2Bh	5.35 V

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Table 125. OTP_CORE_CFG1 register bit description

Bit	Bit Group Name	Description	Value	Settings
5 to 4	COREHS_SR_OTP[1:0]	VCORE high-side slew rate t_{CORESW_HSSRR} / t_{CORESW_HSSRF}	0	Rise = 5 V/ns; Fall = 2.2 V/ns
			1	Rise = 4 V/ns; Fall = 0.6 V/ns
			2	Rise = 4.5 V/ns; Fall = 1.2 V/ns
			3	Rise = 5 V/ns; Fall = 2.2 V/ns
3 to 2	CORE_PH_OTP[1:0]	VCORE phase delay	0	No delay
			1	1 clock cycle
			2	2 clock cycles
			3	3 clock cycles
1 to 0	CORE_ILIM_OTP[1:0]	VCORE current limit $I_{CORE\_PEAK\_0A8}$ $I_{CORE\_PEAK\_1A65}$	0	1.4 A
			1	1.7 A
			2	2.7 A
			3	3.4 A

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Table 126. OTP_CORE_CFG2 register bit description

Bit	Bit Group Name	Description	Value	Settings
5 to 4	CORE_RCOMP_OTP[1:0]	VCORE comp resistance	0	150 kΩ
			1	200 kΩ
			2	300 kΩ
			3	450 kΩ
3 to 2	CORE_CCOMP_OTP[1:0]	VCORE comp capacitor	0	50 pF
			1	60 pF
			2	90 pF
			3	120 pF
1 to 0	CORE_GM_OTP[1:0]	VCORE transconductance amp	0	26 µS
			1	26 µS
			2	53 µS
			3	107 µS

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Table 127. OTP_CORE_CFG3 register bit description

Bit	Bit Group Name	Description	Value	Settings
5 to 4	CORE_SS_OTP[1:0]	VCORE soft start V_{CORE_SS}	0	2.5 mV/µs
			1	5 mV/µs
			2	10 mV/µs
			3	20 mV/µs
2	CORE_CTRL_OTP	VCORE control type	0	Valley mode control
			1	Peak mode control
1 to 0	CORE_LSEL_OTP[1:0]	VCORE inductor L_{CORE}	0	1 µH
			1	1.5 µH
			2	2.2 µH
			3	2.2 µH

Table 128. OTP_CORE_VOLT1 register bit description

Bit	Bit Group Name	Description	Value	Settings
7 to 0	VCORE_OTP[7:0]	VCORE voltage LSB = 10 mV V_{CORE}	00h	0.80 V
			....	....
			FFh	3.35 V

Go to main OTP register map

Table 129. OTP_CORE_CFG5 register bit description

Bit	Bit Group Name	Description	Value	Settings
7	CORETSD_PD_OTP	VCORE TSD pull-down	0	Pull-down enabled in TSD
			1	Pull-down disabled in TSD
6	CORETDFS_OTP	VCORE TSD behavior Default value of CORETDFS	0	VCORE disabled only
			1	Go to DFS
2 to 0	CORE_SLOT_OTP[2:0]	VCORE power-up slot	0	Slot 0
			1	Slot 1
			2	Slot 2
			3	Slot 3
			4	Slot 4
			5	Slot 5
			6	Slot 6
			7	Slot 7 / OFF

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Table 130. OTP_LDO1_CFG register bit description

Bit	Bit Group Name	Description	Value	Settings
7	LDO1TSD_PD_OTP	LDO1 TSD pull-down	0	pull-down enabled in TSD
			1	pull-down disabled in TSD
6	LDO1TDFS_OTP	LDO1 TSD behavior Default value of LDO1TDFS	0	LDO1 disabled only
			1	Go to DFS
5	LDO1_LP_EN_OTP	LDO1 in *standby mode*	0	Disabled
			1	Enabled
4	VLDO1_LP_OTP	LDO1 voltage in *standby mode*	0	3.3 V
			1	5.0 V
3	VLDO1_OTP	LDO1 voltage in *normal mode* V_{LDOx}	0	3.3 V
			1	5.0 V
2 to 0	LDO1_SLOT_OTP[2:0]	LDO1 power-up slot	0	Slot 0
			1	Slot 1
			2	Slot 2
			3	Slot 3
			4	Slot 4
			5	Slot 5
			6	Slot 6
			7	Slot 7 / OFF

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Table 131. OTP_LDO2_CFG register bit description

Bit	Bit Group Name	Description	Value	Settings
7	LDO2TSD_PD_OTP	LDO2 TSD pull-down	0	pull-down enabled in TSD
			1	pull-down disabled in TSD
6	LDO2TDFS_OTP	LDO2 TSD behavior Default value of LDO2TDFS	0	LDO2 disabled only
			1	Go to DFS
5	LDO2_LP_EN_OTP	LDO2 in *standby mode*	0	Disabled
			1	Enabled
4	VLDO2_LP_OTP	LDO2 voltage in *standby mode*	0	3.3 V
			1	5.0 V
3	VLDO2_OTP	LDO2 voltage in *normal mode* V_{LDOx}	0	3.3 V
			1	5.0 V
2 to 0	LDO2_SLOT_OTP[2:0]	LDO2 power-up slot	0	Slot 0
			1	Slot 1
			2	Slot 2
			3	Slot 3
			4	Slot 4
			5	Slot 5
			6	Slot 6
			7	Slot 7 / OFF

Go to main OTP register map

Table 132. OTP_TRK1_CFG register bit description

Bit	Bit Group Name	Description	Value	Settings
7	TRK1TSD_PD_OTP	TRK1 TSD pull-down	0	pull-down enabled in TSD
			1	pull-down disabled in TSD
6	TRK1TDFS_OTP	TRK1 TSD behavior Default value of TRK1TDFS	0	TRK1 disabled only
			1	Go to DFS
5 to 4	TRK1_SEL_OTP[1:0]	TRK1 input selection	0	VREF
			1	Internal LDO Reference
			2	LDO2
			3	VREF
2 to 0	TRK1_SLOT_OTP[2:0]	TRK1 power-up slot	0	Slot 0
			1	Slot 1
			2	Slot 2
			3	Slot 3
			4	Slot 4
			5	Slot 5
			6	Slot 6
			7	Slot 7 / OFF

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Table 133. OTP_TRK2_CFG register bit description

Bit	Bit Group Name	Description	Value	Settings
7	TRK2TSD_PD_OTP	TRK2 TSD pull-down	0	pull-down enabled in TSD
			1	pull-down disabled in TSD

Table 133. OTP_TRK2_CFG register bit description*...continued*

Bit	Bit Group Name	Description	Value	Settings
6	TRK2TDFS_OTP	TRK2 TSD behavior Default value of TRK2TDFS	0	TRK2 disabled only
			1	Go to DFS
5 to 4	TRK2_SEL_OTP[1:0]	TRK2 input selection	0	VREF
			1	Internal LDO reference
			2	LDO2
			3	VREF
2 to 0	TRK2_SLOT_OTP[2:0]	TRK2 power-up slot	0	Slot 0
			1	Slot 1
			2	Slot 2
			3	Slot 3
			4	Slot 4
			5	Slot 5
			6	Slot 6
			7	Slot 7 / OFF

Go to main OTP register map

Table 134. OTP_VREF_CFG register bit description

Bit	Bit Group Name	Description	Value	Settings
5 to 4	VLDO_REF_OTP[1:0]	Internal LDO reference	0	1.2 V
			1	1.8 V
			2	3.3 V
			3	5.0 V
3	VREF_OTP	VREF voltage	0	3.3 V
			1	5.0 V
2 to 0	VREF_SLOT_OTP[2:0]	VREF power-up slot	0	Slot 0
			1	Slot 1
			2	Slot 2
			3	Slot 3
			4	Slot 4
			5	Slot 5
			6	Slot 6
			7	Slot 7 / OFF

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Table 135. OTP_GPIO1_CFG register bit description

Bit	Bit Group Name	Description	Value	Settings
7	GPIO1TSD_PD_OTP	GPIO1 TSD pull-down R_{PD_GPIOx}	0	Pull-down enabled in TSD
			1	Pull-down disabled in TSD
6	GPIO1PD_OTP	GPIO1 pull-down R_{PD_GPIOx}	0	Pull-down disabled
			1	Pull-down enabled
5	GPIO1PU_OTP	GPIO1 pull-up R_{PU_GPIOx}	0	Pull-up disabled
			1	Pull-up enabled

Table 135. OTP_GPIO1_CFG register bit description*...continued*

Bit	Bit Group Name	Description	Value	Settings
4 to 3	GPIO1STAGE_OTP[1:0]	GPIO1 configuration	0	Input configuration
			1	Low-side driver
			2	High-side driver
			3	Push-pull driver
2 to 0	GPIO1_SLOT_OTP[2:0]	GPIO1 power-up slot	0	Slot 0
			1	Slot 1
			2	Slot 2
			3	Slot 3
			4	Slot 4
			5	Slot 5
			6	Slot 6
			7	Slot 7 / OFF

Go to main OTP register map

Table 136. OTP_GPIO2_CFG register bit description

Bit	Bit Group Name	Description	Value	Settings
6	GPIO2PD_OTP	GPIO2 pull-down R_{PD_GPIOx}	0	Pull-down disabled
			1	Pull-down enabled
5	GPIO2PU_OTP	GPIO2 pull-up R_{PU_GPIOx}	0	Pull-up disabled
			1	Pull-up enabled
4 to 3	GPIO2STAGE_OTP[1:0]	GPIO2 configuration	0	Input configuration
			1	Low-side driver
			2	High-side driver
			3	Push-pull driver
2 to 0	GPIO2_SLOT_OTP[2:0]	GPIO2 power-up slot	0	Slot 0
			1	Slot 1
			2	Slot 2
			3	Slot 3
			4	Slot 4
			5	Slot 5
			6	Slot 6
			7	Slot 7 / OFF

Go to main OTP register map

Table 137. OTP_INPUT_CFG register bit description

Bit	Bit Group Name	Description	Value	Settings
7	WK2PD_SEL_OTP	WAKE2 pull-down value selection R_{PD_WAKE}	0	200 kΩ
			1	10 kΩ
6	WK1PD_SEL_OTP	WAKE1 pull-down value selection R_{PD_WAKE}	0	200 kΩ
			1	10 kΩ
5	GPIO2TH_OTP	GPIO2 detection threshold V_{IL_GPIOx} / V_{IH_GPIOx}	0	Low-voltage threshold
			1	High-voltage threshold
4	GPIO1TH_OTP	GPIO1 detection threshold V_{IL_GPIOx} / V_{IH_GPIOx}	0	Low-voltage threshold
			1	High-voltage threshold

Table 137. OTP_INPUT_CFG register bit description...*continued*

Bit	Bit Group Name	Description	Value	Settings
3	WK2PD_OTP	WAKE2 pull-down R_{PD_WAKE}	0	Disabled
			1	Enabled
2	WK1PD_OTP	WAKE1 pull-down R_{PD_WAKE}	0	Disabled
			1	Enabled
1	WK2TH_OTP	WAKE2 detection threshold V_{IL_WAKEx} / V_{IH_WAKEx}	0	Low-voltage threshold
			1	High-voltage threshold
0	WK1TH_OTP	WAKE1 detection threshold V_{IL_WAKEx} / V_{IH_WAKEx}	0	Low-voltage threshold
			1	High-voltage threshold

Go to main OTP register map

Table 138. OTP_PROG_IDH register bit description

Bit	Bit Group Name	Description	Value	Settings
7 to 0	PROG_IDH_OTP[7:0]	Program ID high decoding	00h	A
			01h	B
			02h	C
			03h	D
			04h	E
			05h	F
			06h	G
			07h	H
			08h	J
			09h	K
			0Ah	L
			0Bh	M
			0Ch	N
			0Dh	P
			0Eh	Q
			0Fh	R
			10h	S
			11h	T
			12h	U
			13h	V
			14h	W
			15h	X
			16h	Y
			17h	Z

Go to main OTP register map

Table 139. OTP_PROG_IDL register bit description

Bit	Bit Group Name	Description	Value	Settings
7 to 0	PROG_IDL_OTP[7:0]	Program ID low decoding	00h	0
			01h	1
			02h	2
			03h	3
			04h	4
			05h	5
			06h	6
			07h	7
			08h	8
			09h	9
			0Ah	A
			0Bh	B
			0Ch	C
			0Dh	D
			0Eh	E
			0Fh	F
			10h	G
			11h	H
			12h	J
			13h	K
			14h	L
			15h	M
			16h	N
			17h	P
			18h	Q
			19h	R
			1Ah	S
			1Bh	T
			1Ch	U
			1Dh	V
			1Eh	W
			1Fh	X
			20h	Y
			21h	Z

19.3 Fail-safe OTP overview

Table 140. Fail-safe OTP configuration map

Register Name	ADDRESS	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CFG_OVUV_1_OTP	0F	VMON_LDO2_ UVDTH_OTP	VMON_LDO1_ UVDTH_OTP	VPRE_V_OTP[5:0]					
CFG_OVUV_2_OTP	10	VCORE_V_OTP[7:0]							
CFG_OVUV_3_OTP	11	DFS_DIS_OTP	TRK2_V_OTP[1:0]		TRK1_V_OTP[1:0]		LDO1_V_OTP	LDO2_V_OTP	VREF_V_OTP
CFG_OVUV_4_OTP	12	VMON_PRE_UVTH_OTP[3:0]				VMON_PRE_OVTH_OTP[3:0]			
CFG_OVUV_5_OTP	13	VMON_CORE_UVTH_OTP[3:0]				VMON_CORE_OVTH_OTP[3:0]			
CFG_OVUV_6_OTP	14	VMON_LDO1_UVTH_OTP[3:0]				VMON_LDO1_OVTH_OTP[3:0]			
CFG_OVUV_7_OTP	15	VMON_LDO2_UVTH_OTP[3:0]				VMON_LDO2_OVTH_OTP[3:0]			
CFG_OVUV_8_OTP	16	VMON_TRK1_UVTH_OTP[3:0]				VMON_TRK1_OVTH_OTP[3:0]			
CFG_OVUV_9_OTP	17	VMON_TRK2_UVTH_OTP[3:0]				VMON_TRK2_OVTH_OTP[3:0]			
CFG_OVUV_10_OTP	18	VMON_VREF_UVTH_OTP[3:0]				VMON_VREF_OVTH_OTP[3:0]			
CFG_OVUV_11_OTP	19	VMON_EXT_UVTH_OTP[3:0]				VMON_EXT_OVTH_OTP[3:0]			
CFG_OV_DGLT_OTP	1A	VMON_EXT_ OVDGLT_OTP	VMON_REF_ OVDGLT_OTP	VMON_TRK2_ OVDGLT_OTP	VMON_TRK1_ OVDGLT_OTP	VMON_LDO2_ OVDGLT_OTP	VMON_LDO1_ OVDGLT_OTP	VMON_PRE_ OVDGLT_OTP	VMON_CORE_ OVDGLT_OTP
CFG_UV_DGLT1_OTP	1B	VMON_LDO2_ UVDGLT_OTP[1:0]		VMON_LDO1_ UVDGLT_OTP[1:0]		VMON_PRE_UVDGLT_OTP[1:0]		VMON_CORE_UVDGLT_OTP[1:0]	
CFG_UV_DGLT2_OTP	1C	VMON_EXT_UVDGLT_OTP[1:0]		VMON_REF_UVDGLT_OTP[1:0]		VMON_TRK2_ UVDGLT_OTP[1:0]		VMON_TRK1_UVDGLT_OTP[1:0]	
CFG_ABIST1_OTP	1D	ABIST1_ EXT_EN_OTP	ABIST1_ VREF_ EN_OTP	ABIST1_ TRK2_EN_OTP	ABIST1_ TRK1_EN_OTP	ABIST1_ LDO2_ EN_OTP	ABIST1_ LDO1_EN_OTP	ABIST1_ VCORE_ EN_OTP	ABIST1_VPRE_ EN_OTP
CFG_MODE_OTP	1E	—		WD_DIS_OTP	DIS8S_ DIS_OTP	PRE_RSTB_ DLY_EN_OTP	FS1B_FS0 B_EN_OTP	FAULT_DFS_ EN_OTP	—
CFG_LBIST_ STDBY_OTP	1F	LBIST_STDBY_OTP[7:0]							

19.4 Fail-safe OTP register bits description

Table 141. CFG_OVUV_1_OTP register bit description

Bit	Bit Group Name	Description	Value	Settings
7	VMON_LDO2_UVDTH_OTP	VMON_LDO2 degraded UV monitoring	0	Normal UV
			1	Degraded UV
6	VMON_LDO1_UVDTH_OTP	VMON_LDO1 degraded UV monitoring	0	Normal UV
			1	Degraded UV
5 to 0	VPRE_V_OTP[5:0]	VMON_PRE monitoring voltage $VMON_{PRE\_RANGE}$ $VMON_{PRE\_STEP}$	0Ah	3.70 V
			0Bh	3.75 V
			0Ch	3.80 V
			0Dh	3.85 V
			0Eh	3.90 V
			0Fh	3.95 V
			10h	4.00 V
			11h	4.05 V
			12h	4.10 V
			13h	4.15 V
			14h	4.20 V
			15h	4.25 V
			16h	4.30 V
			17h	4.35 V
			18h	4.40 V

Table 141. CFG_OVUV_1_OTP register bit description*...continued*

Bit	Bit Group Name	Description	Value	Settings
			19h	4.45 V
			1Ah	4.50 V
			1Bh	4.55 V
			1Ch	4.60 V
			1Dh	4.65 V
			1Eh	4.70 V
			1Fh	4.75 V
			20h	4.80 V
			21h	4.85 V
			22h	4.90 V
			23h	4.95 V
			24h	5.00 V
			25h	5.05 V
			26h	5.10 V
			27h	5.15 V
			28h	5.20 V
			29h	5.25 V
			2Ah	5.30 V
			2Bh	5.35 V
			2Ch	5.40 V
			2Dh	5.45 V
			2Eh	5.50 V
			2Fh	5.55 V
			30h	5.60 V
			31h	5.65 V
			32h	5.70 V
			33h	5.75 V
			34h	5.80 V
			35h	5.85 V
			36h	5.90 V
			37h	5.95 V
			38h	6.00 V
			39h	6.05 V
			3Ah	6.10 V
			3Bh	6.15 V
			3Ch	6.20 V
			3Dh	6.25 V
			3Eh	6.30 V
			3Fh	6.35 V

Go to fail-safe OTP register map

Table 142. CFG_OVUV_2_OTP register bit description

Bit	Bit Group Name	Description	Value	Settings
7 to 0	VCORE_V_OTP[7:0]	VMON_CORE monitoring voltage $VMON_{CORE\_RANGE}$	00h	0.80 V
			01h	0.81 V

Table 142. CFG_OVUV_2_OTP register bit description*...continued*

Bit	Bit Group Name	Description	Value	Settings
		$VMON_{CORE\_STEP}$	02h	0.82 V
			03h	0.83 V
			04h	0.84 V
			05h	0.85 V
			06h	0.86 V
			07h	0.87 V
			08h	0.88 V
			09h	0.89 V
			0Ah	0.90 V
			0Bh	0.91 V
			0Ch	0.92 V
			0Dh	0.93 V
			0Eh	0.94 V
			0Fh	0.95 V
			10h	0.96 V
			11h	0.97 V
			12h	0.98 V
			13h	0.99 V
			14h	1.00 V
			15h	1.01 V
			16h	1.02 V
			17h	1.03 V
			18h	1.04 V
			19h	1.05 V
			1Ah	1.06 V
			1Bh	1.07 V
			1Ch	1.08 V
			1Dh	1.09 V
			1Eh	1.10 V
			1Fh	1.11 V
			20h	1.12 V
			21h	1.13 V
			22h	1.14 V
			23h	1.15 V
			24h	1.16 V
			25h	1.17 V
			26h	1.18 V
			27h	1.19 V
			28h	1.20 V
			29h	1.21 V
			2Ah	1.22 V
			2Bh	1.23 V
			2Ch	1.24 V
			2Dh	1.25 V
			2Eh	1.26 V

Table 142. CFG_OVUV_2_OTP register bit description*...continued*

Bit	Bit Group Name	Description	Value	Settings
			2Fh	1.27 V
			30h	1.28 V
			31h	1.29 V
			32h	1.30 V
			33h	1.31 V
			34h	1.32 V
			35h	1.33 V
			36h	1.34 V
			37h	1.35 V
			38h	1.36 V
			39h	1.37 V
			3Ah	1.38 V
			3Bh	1.39 V
			3Ch	1.40 V
			3Dh	1.41 V
			3Eh	1.42 V
			3Fh	1.43 V
			40h	1.44 V
			41h	1.45 V
			42h	1.46 V
			43h	1.47 V
			44h	1.48 V
			45h	1.49 V
			46h	1.50 V
			47h	1.51 V
			48h	1.52 V
			49h	1.53 V
			4Ah	1.54 V
			4Bh	1.55 V
			4Ch	1.56 V
			4Dh	1.57 V
			4Eh	1.58 V
			4Fh	1.59 V
			50h	1.60 V
			51h	1.61 V
			52h	1.62 V
			53h	1.63 V
			54h	1.64 V
			55h	1.65 V
			56h	1.66 V
			57h	1.67 V
			58h	1.68 V
			59h	1.69 V
			5Ah	1.70 V
			5Bh	1.71 V

Table 142. CFG_OVUV_2_OTP register bit description*...continued*

Bit	Bit Group Name	Description	Value	Settings
			5Ch	1.72 V
			5Dh	1.73 V
			5Eh	1.74 V
			5Fh	1.75 V
			60h	1.76 V
			61h	1.77 V
			62h	1.78 V
			63h	1.79 V
			64h	1.80 V
			65h	1.81 V
			66h	1.82 V
			67h	1.83 V
			68h	1.84 V
			69h	1.85 V
			6Ah	1.86 V
			6Bh	1.87 V
			6Ch	1.88 V
			6Dh	1.89 V
			6Eh	1.90 V
			6Fh	1.91 V
			70h	1.92 V
			71h	1.93 V
			72h	1.94 V
			73h	1.95 V
			74h	1.96 V
			75h	1.97 V
			76h	1.98 V
			77h	1.99 V
			78h	2.00 V
			79h	2.01 V
			7Ah	2.02 V
			7Bh	2.03 V
			7Ch	2.04 V
			7Dh	2.05 V
			7Eh	2.06 V
			7Fh	2.07 V
			80h	2.08 V
			81h	2.09 V
			82h	2.10 V
			83h	2.11 V
			84h	2.12 V
			85h	2.13 V
			86h	2.14 V
			87h	2.15 V
			88h	2.16 V

Table 142. CFG_OVUV_2_OTP register bit description*...continued*

Bit	Bit Group Name	Description	Value	Settings
			89h	2.17 V
			8Ah	2.18 V
			8Bh	2.19 V
			8Ch	2.20 V
			8Dh	2.21 V
			8Eh	2.22 V
			8Fh	2.23 V
			90h	2.24 V
			91h	2.25 V
			92h	2.26 V
			93h	2.27 V
			94h	2.28 V
			95h	2.29 V
			96h	2.30 V
			97h	2.31 V
			98h	2.32 V
			99h	2.33 V
			9Ah	2.34 V
			9Bh	2.35 V
			9Ch	2.36 V
			9Dh	2.37 V
			9Eh	2.38 V
			9Fh	2.39 V
			A0h	2.40 V
			A1h	2.41 V
			A2h	2.42 V
			A3h	2.43 V
			A4h	2.44 V
			A5h	2.45 V
			A6h	2.46 V
			A7h	2.47 V
			A8h	2.48 V
			A9h	2.49 V
			AAh	2.50 V
			ABh	2.51 V
			ACh	2.52 V
			ADh	2.53 V
			AEh	2.54 V
			AFh	2.55 V
			B0h	2.56 V
			B1h	2.57 V
			B2h	2.58 V
			B3h	2.59 V
			B4h	2.60 V
			B5h	2.61 V

Table 142. CFG_OVUV_2_OTP register bit description*...continued*

Bit	Bit Group Name	Description	Value	Settings
			B6h	2.62 V
			B7h	2.63 V
			B8h	2.64 V
			B9h	2.65 V
			BAh	2.66 V
			BBh	2.67 V
			BCh	2.68 V
			BDh	2.69 V
			BEh	2.70 V
			BFh	2.71 V
			C0h	2.72 V
			C1h	2.73 V
			C2h	2.74 V
			C3h	2.75 V
			C4h	2.76 V
			C5h	2.77 V
			C6h	2.78 V
			C7h	2.79 V
			C8h	2.80 V
			C9h	2.81 V
			CAh	2.82 V
			CBh	2.83 V
			CCh	2.84 V
			CDh	2.85 V
			CEh	2.86 V
			CFh	2.87 V
			D0h	2.88 V
			D1h	2.89 V
			D2h	2.90 V
			D3h	2.91 V
			D4h	2.92 V
			D5h	2.93 V
			D6h	2.94 V
			D7h	2.95 V
			D8h	2.96 V
			D9h	2.97 V
			DAh	2.98 V
			DBh	2.99 V
			DCh	3.00 V
			DDh	3.01 V
			DEh	3.02 V
			DFh	3.03 V
			E0h	3.04 V
			E1h	3.05 V
			E2h	3.06 V

Table 142. CFG_OVUV_2_OTP register bit description...*continued*

Bit	Bit Group Name	Description	Value	Settings
			E3h	3.07 V
			E4h	3.08 V
			E5h	3.09 V
			E6h	3.10 V
			E7h	3.11 V
			E8h	3.12 V
			E9h	3.13 V
			EAh	3.14 V
			EBh	3.15 V
			ECh	3.16 V
			EDh	3.17 V
			EEh	3.18 V
			EFh	3.19 V
			F0h	3.20 V
			F1h	3.21 V
			F2h	3.22 V
			F3h	3.23 V
			F4h	3.24 V
			F5h	3.25 V
			F6h	3.26 V
			F7h	3.27 V
			F8h	3.28 V
			F9h	3.29 V
			FAh	3.30 V
			FBh	3.31 V
			FCh	3.32 V
			FDh	3.33 V
			FEh	3.34 V
			FFh	3.35 V

Go to fail-safe OTP register map

Table 143. CFG_OVUV_3_OTP register bit description

Bit	Bit Group Name	Description	Value	Settings
7	DFS_DIS_OTP	Disable Deep Fail Safe entry	0	DFS entry enabled
			1	DFS entry disabled
6	TRK2_V_OTP[1:0]	VMON_TRK2 monitoring voltage $VMON_{TRK2\_CFG}$	0	1.2 V
			1	1.8 V
			2	3.3 V
			3	5.0 V
5 to 4	TRK1_V_OTP[1:0]	VMON_TRK1 monitoring voltage $VMON_{TRK1\_CFG}$	0	1.2 V
			1	1.8 V
			2	3.3 V
			3	5.0 V
3 to 2	LDO1_V_OTP	VMON_LDO1 monitoring voltage $VMON_{LDO1\_CFG}$	0	3.3 V
			1	5.0 V

Table 143. CFG_OVUV_3_OTP register bit description*...continued*

Bit	Bit Group Name	Description	Value	Settings
1	LDO2_V_OTP	VMON_LDO2 monitoring voltage $VMON_{LDO2\_CFG}$	0	3.3 V
			1	5.0 V
0	VREF_V_OTP	VMON_REF monitoring voltage $VMON_{REF\_V}$	0	3.3 V
			1	5.0 V

Go to fail-safe OTP register map

Table 144. CFG_OVUV_4_OTP register bit description

Bit	Bit Group Name	Description	Value	Settings
7 to 4	VMON_PRE_UVTH_OTP[3:0]	VMON_PRE UV threshold $VMON_{PRE\_UVTH\_RANGE}$	3h	94.0 %
			4h	93.5 %
			5h	93.0 %
			6h	92.5 %
			7h	92.0 %
			8h	91.5 %
			9h	91.0 %
			Ah	90.5 %
			Bh	90.0 %
			Ch	89.5 %
			Dh	89.0 %
			Eh	88.5 %
			Fh	88.0 %
3 to 0	VMON_PRE_OVTH_OTP[3:0]	VMON_PRE OV threshold $VMON_{PRE\_OVTH\_RANGE}$	3h	106.0 %
			4h	106.5 %
			5h	107.0 %
			6h	107.5 %
			7h	108.0 %
			8h	108.5 %
			9h	109.0 %
			Ah	109.5 %
			Bh	110.0 %
			Ch	110.5 %
			Dh	111.0 %
			Eh	111.5 %
			Fh	112.0 %

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Table 145. CFG_OVUV_5_OTP register bit description

Bit	Bit Group Name	Description	Value	Settings
7 to 4	VMON_CORE_UVTH_OTP[3:0]	VMON_CORE UV threshold $VMON_{CORE\_UVTH\_RANGE}$	0h	95.5 %
			1h	95.0 %
			2h	94.5 %
			3h	94.0 %
			4h	93.5 %
			5h	93.0 %
			6h	92.5 %
			7h	92.0 %
			8h	91.5 %
			9h	91.0 %
			Ah	90.5 %
			Bh	90.0 %
			Ch	89.5 %
			Dh	89.0 %
			Eh	88.5 %
			Fh	88.0 %
3 to 0	VMON_CORE_OVTH_OTP[3:0]	VMON_CORE OV threshold $VMON_{CORE\_OVTH\_RANGE}$	0h	104.5 %
			1h	105.0 %
			2h	105.5 %
			3h	106.0 %
			4h	106.5 %
			5h	107.0 %
			6h	107.5 %
			7h	108.0 %
			8h	108.5 %
			9h	109.0 %
			Ah	109.5 %
			Bh	110.0 %
			Ch	110.5 %
			Dh	111.0 %
			Eh	111.5 %
			Fh	112.0 %

Go to fail-safe OTP register map

Table 146. CFG_OVUV_6_OTP register bit description

Bit	Bit Group Name	Description	Value	Settings
7 to 4	VMON_LDO1_UVTH_OTP[3:0]	VMON_LDO1 UV threshold $VMON_{LDO1\_UVTH\_RANGE}$	0h	95.5 %
			1h	95.0 %
			2h	94.5 %
			3h	94.0 %
			4h	93.5 %
			5h	93.0 %
			6h	92.5 %
			7h	92.0 %
			8h	91.5 %
			9h	91.0 %
			Ah	90.5 %
			Bh	90.0 %
			Ch	89.5 %
			Dh	89.0 %
			Eh	88.5 %
			Fh	88.0 %
3 to 0	VMON_LDO1_OVTH_OTP[3:0]	VMON_LDO1 OV threshold $VMON_{LDO1\_OVTH\_RANGE}$	0h	104.5 %
			1h	105.0 %
			2h	105.5 %
			3h	106.0 %
			4h	106.5 %
			5h	107.0 %
			6h	107.5 %
			7h	108.0 %
			8h	108.5 %
			9h	109.0 %
			Ah	109.5 %
			Bh	110.0 %
			Ch	110.5 %
			Dh	111.0 %
			Eh	111.5 %
			Fh	112.0 %

Go to fail-safe OTP register map

Table 147. CFG_OVUV_7_OTP register bit description

Bit	Bit Group Name	Description	Value	Settings
7 to 4	VMON_LDO2_UVTH_OTP[3:0]	VMON_LDO2 UV threshold $VMON_{LDO2\_UVTH\_RANGE}$	0h	95.5 %
			1h	95.0 %
			2h	94.5 %
			3h	94.0 %
			4h	93.5 %
			5h	93.0 %
			6h	92.5 %
			7h	92.0 %
			8h	91.5 %
			9h	91.0 %
			Ah	90.5 %
			Bh	90.0 %
			Ch	89.5 %
			Dh	89.0 %
			Eh	88.5 %
			Fh	88.0 %
3 to 0	VMON_LDO2_OVTH_OTP[3:0]	VMON_LDO2 OV threshold $VMON_{LDO2\_OVTH\_RANGE}$	0h	104.5 %
			1h	105.0 %
			2h	105.5 %
			3h	106.0 %
			4h	106.5 %
			5h	107.0 %
			6h	107.5 %
			7h	108.0 %
			8h	108.5 %
			9h	109.0 %
			Ah	109.5 %
			Bh	110.0 %
			Ch	110.5 %
			Dh	111.0 %
			Eh	111.5 %
			Fh	112.0 %

Go to fail-safe OTP register map

Table 148. CFG_OVUV_8_OTP register bit description

Bit	Bit Group Name	Description	Value	Settings
7 to 4	VMON_TRK1_UVTH_OTP[3:0]	VMON_TRK1 UV threshold $VMON_{TRK1\_UVTH\_RANGE}$	0h	95.5 %
			1h	95.0 %
			2h	94.5 %
			3h	94.0 %
			4h	93.5 %
			5h	93.0 %
			6h	92.5 %
			7h	92.0 %
			8h	91.5 %
			9h	91.0 %
			Ah	90.5 %
			Bh	90.0 %
			Ch	89.5 %
			Dh	89.0 %
			Eh	88.5 %
			Fh	88.0 %
3 to 0	VMON_TRK1_OVTH_OTP[3:0]	VMON_TRK1 OV threshold $VMON_{TRK1\_OVTH\_RANGE}$	0h	104.5 %
			1h	105.0 %
			2h	105.5 %
			3h	106.0 %
			4h	106.5 %
			5h	107.0 %
			6h	107.5 %
			7h	108.0 %
			8h	108.5 %
			9h	109.0 %
			Ah	109.5 %
			Bh	110.0 %
			Ch	110.5 %
			Dh	111.0 %
			Eh	111.5 %
			Fh	112.0 %

Go to fail-safe OTP register map

Table 149. CFG_OVUV_9_OTP register bit description

Bit	Bit Group Name	Description	Value	Settings
7 to 4	VMON_TRK2_UVTH_OTP[3:0]	VMON_TRK2 UV threshold $VMON_{TRK2\_UVTH\_RANGE}$	0h	95.5 %
			1h	95.0 %
			2h	94.5 %
			3h	94.0 %
			4h	93.5 %
			5h	93.0 %
			6h	92.5 %
			7h	92.0 %
			8h	91.5 %
			9h	91.0 %
			Ah	90.5 %
			Bh	90.0 %
			Ch	89.5 %
			Dh	89.0 %
			Eh	88.5 %
			Fh	88.0 %
3 to 0	VMON_TRK2_OVTH_OTP[3:0]	VMON_TRK2 OV threshold $VMON_{TRK2\_OVTH\_RANGE}$	0h	104.5 %
			1h	105.0 %
			2h	105.5 %
			3h	106.0 %
			4h	106.5 %
			5h	107.0 %
			6h	107.5 %
			7h	108.0 %
			8h	108.5 %
			9h	109.0 %
			Ah	109.5 %
			Bh	110.0 %
			Ch	110.5 %
			Dh	111.0 %
			Eh	111.5 %
			Fh	112.0 %

Go to fail-safe OTP register map

Table 150. CFG_OVUV_10_OTP register bit description

Bit	Bit Group Name	Description	Value	Settings
7 to 4	VMON_REF_UVTH_OTP[3:0]	VMON_REF UV threshold $VMON_{REF\_UVTH\_RANGE}$	0h	95.5 %
			1h	95.0 %
			2h	94.5 %
			3h	94.0 %
			4h	93.5 %
			5h	93.0 %
			6h	92.5 %
			7h	92.0 %
			8h	91.5 %
			9h	91.0 %
			Ah	90.5 %
			Bh	90.0 %
			Ch	89.5 %
			Dh	89.0 %
			Eh	88.5 %
			Fh	88.0 %
3 to 0	VMON_REF_OVTH_OTP[3:0]	VMON_REF OV threshold $VMON_{REF\_OVTH\_RANGE}$	0h	104.5 %
			1h	105.0 %
			2h	105.5 %
			3h	106.0 %
			4h	106.5 %
			5h	107.0 %
			6h	107.5 %
			7h	108.0 %
			8h	108.5 %
			9h	109.0 %
			Ah	109.5 %
			Bh	110.0 %
			Ch	110.5 %
			Dh	111.0 %
			Eh	111.5 %
			Fh	112.0 %

Go to fail-safe OTP register map

Table 151. CFG_OVUV_11_OTP register bit description

Bit	Bit Group Name	Description	Value	Settings
7 to 4	VMON_EXT_UVTH_OTP[3:0]	VMON_EXT UV threshold $VMON_{EXT\_UVTH\_RANGE}$	0h	95.5 %
			1h	95.0 %
			2h	94.5 %
			3h	94.0 %
			4h	93.5 %
			5h	93.0 %
			6h	92.5 %
			7h	92.0 %
			8h	91.5 %
			9h	91.0 %
			Ah	90.5 %
			Bh	90.0 %
			Ch	89.5 %
			Dh	89.0 %
			Eh	88.5 %
			Fh	88.0 %
3 to 0	VMON_EXT_OVTH_OTP[3:0]	VMON_EXT OV threshold $VMON_{EXT\_OVTH\_RANGE}$	0h	104.5 %
			1h	105.0 %
			2h	105.5 %
			3h	106.0 %
			4h	106.5 %
			5h	107.0 %
			6h	107.5 %
			7h	108.0 %
			8h	108.5 %
			9h	109.0 %
			Ah	109.5 %
			Bh	110.0 %
			Ch	110.5 %
			Dh	111.0 %
			Eh	111.5 %
			Fh	112.0 %

Go to fail-safe OTP register map

Table 152. CFG_OV_DGLT_OTP register bit description

Bit	Bit Group Name	Description	Value	Settings
7	VMON_EXT_OVDGLT_OTP	VMON_EXT OV deglitch $t_{VMON\_EXT\_OV\_DGLT}$	0	25 µs
			1	45 µs
6	VMON_REF_OVDGLT_OTP	VMON_REF OV deglitch $t_{VMON\_REF\_OV\_DGLT}$	0	25 µs
			1	45 µs
5	VMON_TRK2_OVDGLT_OTP	VMON_TRK2 OV deglitch $t_{VMON\_TRK2\_OV\_DGLT}$	0	25 µs
			1	45 µs
4	VMON_TRK1_OVDGLT_OTP	VMON_TRK1 OV deglitch $t_{VMON\_TRK1\_OV\_DGLT}$	0	25 µs
			1	45 µs

Table 152. CFG_OV_DGLT_OTP register bit description*...continued*

Bit	Bit Group Name	Description	Value	Settings
3	VMON_LDO2_OVDGLT_OTP	VMON_LDO2 OV deglitch $t_{VMON\_LDO2\_OV\_DGLT}$	0	25 µs
			1	45 µs
2	VMON_LDO1_OVDGLT_OTP	VMON_LDO1 OV deglitch $t_{VMON\_LDO1\_OV\_DGLT}$	0	25 µs
			1	45 µs
1	VMON_PRE_OVDGLT_OTP	VMON_PRE OV deglitch $t_{VMON\_PRE\_OV\_DGLT}$	0	25 µs
			1	45 µs
0	VMON_CORE_OVDGLT_OTP	VMON_CORE OV deglitch $t_{VMON\_CORE\_OV\_DGLT}$	0	25 µs
			1	45 µs

Go to fail-safe OTP register map

Table 153. CFG_UV_DGLT1_OTP register bit description

Bit	Bit Group Name	Description	Value	Settings
7 to 6	VMON_LDO2_UVDGLT_OTP[1:0]	VMON_LDO2 UV deglitch $t_{VMON\_LDO2\_UV\_DGLT}$	0	5 µs
			1	15 µs
			2	25 µs
			3	40 µs
5 to 4	VMON_LDO1_UVDGLT_OTP[1:0]	VMON_LDO1 UV deglitch $t_{VMON\_LDO1\_UV\_DGLT}$	0	5 µs
			1	15 µs
			2	25 µs
			3	40 µs
3 to 2	VMON_PRE_UVDGLT_OTP[1:0]	VMON_PRE UV deglitch $t_{VMON\_PRE\_UV\_DGLT}$	0	5 µs
			1	15 µs
			2	25 µs
			3	40 µs
1 to 0	VMON_CORE_UVDGLT_OTP[1:0]	VMON_CORE UV deglitch $t_{VMON\_CORE\_OV\_DGLT}$	0	5 µs
			1	15 µs
			2	25 µs
			3	40 µs

Go to fail-safe OTP register map

Table 154. CFG_UV_DGLT2_OTP register bit description

Bit	Bit Group Name	Description	Value	Settings
7 to 6	VMON_EXT_UVDGLT_OTP[1:0]	VMON_EXT UV deglitch $t_{VMON\_EXT\_UV\_DGLT}$	0	5 µs
			1	15 µs
			2	25 µs
			3	40 µs
5 to 4	VMON_REF_UVDGLT_OTP[1:0]	VMON_REF UV deglitch $t_{VMON\_REF\_UV\_DGLT}$	0	5 µs
			1	15 µs
			2	25 µs
			3	40 µs

Table 154. CFG_UV_DGLT2_OTP register bit description*...continued*

Bit	Bit Group Name	Description	Value	Settings
3 to 2	VMON_TRK2_UVDGLT_OTP[1:0]	VMON_TRK2 UV deglitch $t_{VMON\_TRK2\_UV\_DGLT}$	0	5 µs
			1	15 µs
			2	25 µs
			3	40 µs
1 to 0	VMON_TRK1_UVDGLT_OTP[1:0]	VMON_TRK1 UV deglitch $t_{VMON\_TRK1\_UV\_DGLT}$	0	5 µs
			1	15 µs
			2	25 µs
			3	40 µs

Go to fail-safe OTP register map

Table 155. CFG_ABIST1_OTP register bit description

Bit	Bit Group Name	Description	Value	Settings
7	ABIST1_EXT_EN_OTP	ABIST1 on VMON_EXT	0	Disabled
			1	Enabled
6	ABIST1_VREF_EN_OTP	ABIST1 on VMON_REF	0	Disabled
			1	Enabled
5	ABIST1_TRK2_EN_OTP	ABIST1 on VMON_TRK2	0	Disabled
			1	Enabled
4	ABIST1_TRK1_EN_OTP	ABIST1 on VMON_TRK1	0	Disabled
			1	Enabled
3	ABIST1_LDO2_EN_OTP	ABIST1 on VMON_LDO2	0	Disabled
			1	Enabled
2	ABIST1_LDO1_EN_OTP	ABIST1 on VMON_LDO1	0	Disabled
			1	Enabled
1	ABIST1_VCORE_EN_OTP	ABIST1 on VMON_CORE	0	Disabled
			1	Enabled
0	ABIST1_VPRE_EN_OTP	ABIST1 on VMON_PRE	0	Disabled
			1	Enabled

Go to fail-safe OTP register map

Table 156. CFG_MODE_OTP register bit description

Bit	Bit Group Name	Description	Value	Settings
5	WD_DIS_OTP	Watchdog timer	0	Watchdog timer enable
			1	Watchdog timer disabled
4	DIS8S_DIS_OTP	RSTB low detection timer Defatult value of DIS8S	0	8 second timer t_{RSTB_8S} enabled
			1	Timer disabled
3	PRE_RSTB_DLY_EN_OTP	RSTB delay from FS0B	0	0 µs
			1	100 µs
2	FS1B_FS0B_EN_OTP	FS1B assertion mode	0	Delayed assertion enabled
			1	Delayed assertion disabled
1	FAULT_DFS_EN_OTP	DFS entry mode	0	Go to DFS when FLT_ERR_CNT[3:0] = @FLT_ERR_CNT_LIMIT[1:0]
			1	Go to DFS when FS0B or RSTB asserted

Go to fail-safe OTP register map

Table 157. CFG_LBIST_STDBY_OTP register bit description

Bit	Bit Group Name	Description	Value	Settings
7 to 0	LBIST_STDBY_OTP[7:0]	Bypass LBIST from *standby mode*	00h	Always perform LBIST
			C9h	Bypass LBIST from *standby mode*

20 Power management

20.1 BOS: Best of supply regulator for internal biasing

The BOS regulator manages the Best Of Supply (BOS) from VSUP or VPRE to efficiently generate 5.0 V output and to supply the internal biasing of the device. BOS supplies the high-side and low-side gate drivers of switching regulators.

The V_{BOS_UVL} detection threshold powers down the device.

When the device is starting up, BOS voltage, which is supplied by VSUP until *normal mode* state, needs to rise above the V_{BOS_UVH} threshold to move to *load fuse* state.

The BOS_IN_OTP[1:0] bits define the BOS supply voltage source when the device is in *normal mode* state:

- When the VPRE output voltage setting is above or equal to 5.0 V, it is recommended to BOS_IN_OTP[1:0] = 0 (auto transition). This setting will ensure an optimized power dissipation of the internal biasing.
- When the VPRE output voltage setting is below 5.0 V, it is recommended to have the BOS_IN_OTP[1:0] = 1 (force VBOS_IN = VSUP). This setting is not optimized for BOS power dissipation but will guarantee correct operation of all switching mode power supplies (SMPS).

Table 158. BOS electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < V_{SUP} < 36 V, V_{PRE_PWM} + V_{PRE_HDR} < V_{SUP_PWR} < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Static electrical characteristics					
V_{BOS_NORM}	V_{BOS} voltage range in *normal mode* (V_{SUP} > 4.5 V and V_{PRE_PWM} > V_{PRE_UVBOS})	V_{PRE_UVBOS} - 0.2	5	5.5	V
V_{BOS_STBY}	V_{BOS} voltage range in *standby mode* (V_{SUP} > 4.5 V, 3.7 V < V_{PRE_PFM} < 5.0 V)	V_{PRE_PFM} - 0.2	—	V_{PRE_PFM}	V
V_{BOS_LPOFF}	V_{BOS} voltage range in *LPOFF mode* (V_{SUP} > 4.5 V)	2.9	4.5	5.5	V
V_{BOS_UVH}	V_{BOS} undervoltage threshold (rising edge)	3.8	4.0	4.2	V
V_{BOS_UVL}	V_{BOS} undervoltage threshold (falling edge)	3	3.2	3.4	V
V_{BOS_POR}	V_{BOS} power-on reset threshold	2.5	—	3.2	V
V_{DIG_POR}	V_{DIG} power-on reset threshold (POR_M condition)	1.35	—	1.54	V
$V_{DIG\_FS\_POR}$	V_{DIG_FS} power-on reset threshold (POR_FS condition)	1.35	—	1.54	V
External components					
C_{BOS_OUT}	BOS output capacitor at VBOS pin Nominal[1] value Effective[2] value	 4.7 3.3	 4.7 —	 4.7 6.1	µF
C_{DIG_OUT}	VDIG output capacitor Nominal[1] value Effective[2] value	 1 0.75	 1 —	 1 1.25	µF

[1] For all regulators, the nominal value is the value normalized.
[2] For all regulators, the effective value is the value after tolerance, temperature, DC bias and aging removal.

20.2 VPRE: High-voltage buck regulator

The VPRE block is a high-voltage integrated synchronous buck. It operates in forced PWM or PFM modes, and uses internal FETs. The output voltage and the switching frequency (450 kHz or 2.25 MHz) are configurable by OTP. Compensation is ensured by internal circuitry.

VPRE can be used to supply VCORE, LDO1, LDO2, TRK1, TRK2, VREF, and the VBST. VPRE can also supply local loads inside the ECU.

At startup, VPRE soft start can be configured through VPRE_SS_OTP[1:0] bits. In case VPRE is supplied by a pre-regulator (not FS2630 VBST), the slowest soft start must be used VPRE_SS_OTP[1:0] = 11.

VPRE operates in PWM (pulse width modulation) when the FS2630 is in *normal mode* and in PFM (pulsed frequency modulation) when the FS2630 is in *standby mode*. The transition from PWM mode to PFM mode is ensured by a controlled DVS down ramp configurable by OTP ($V_{PRE\_DVS\_DOWN}$).

The current in the inductor is sensed through both high-side and low-side switches. The output DC current is then deducted for internal treatment. When the current in the inductor is rising above the I_{OCPRE_FLAG} threshold, the SPI bit VPREOC_I is set. This overcurrent detection does not affect VPRE regulation.

VPRE has a DC current limitation protection feature I_{LIM_PRE}. When VPRE reaches its current limitation, it induces a duty cycle reduction and therefore an output voltage drop. If the overcurrent disappears before reaching V_{PRE_UVL}, the regulator restarts by doing a soft start toward its nominal output voltage.

To protect the circuitry that is supplied by the VPRE power rail, an additional overvoltage protection is integrated in the main domain. If $V_{PRE\_PWM} > V_{PRE\_OVP}$ for a time longer than t_{PRE_OVP}, the FS2630 goes directly into the *Deep Fail Safe* state.

V_{PRE_IN} (V_{SUP_PWR}) must be above $V_{PRE\_PWM} + V_{PRE\_HDR}$ to guarantee VPRE output voltage regulation and its trip level can be configured through VPRE_OC_OTP[2:0] bits.

A thermal shutdown protection is integrated to protect the internal MOSFETs from damage. In case of a TSD event, a pull-down resistor (R_{PRE_DIS}) is enabled to discharge VPRE output capacitors.

The transition from *normal mode* to *LPOFF mode* is ensured by a controlled DVS down ramp ($V_{PRE\_DVS\_DOWN}$) until VPRE is disabled. A power down delay can be configured through VPRE_PDWN_DLY_OTP[1:0] bit to avoid immediate restart. The delay is executed as soon as VPRE DVS down is completed. VPRE regulator is not intended to restart with residual voltage. Therefore, when VPRE is operating at 2.25 MHz, VPRE_PDWN_DLY_OTP[1:0] bit must be configured according to NXP recommendations, as shown in Table 159.

Table 159. VPRE power-down delay configuration when F_{PRE} = 2.25 MHz

ASIL level	VBST configuration	@VPRE_PDWN_DLY_OTP[1:0]
D	Front-end	—
	Back-end / not used	≥ 1 ms
B	Front-end	≥ 2 ms
	Back-end / not used	5 ms

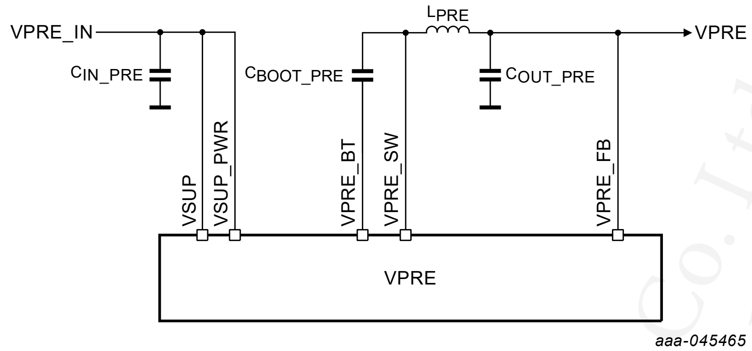

Figure 25. VPRE schematic with connection to V_{SUP}

20.2.1 VPRE electrical characteristics

Table 160. VPRE electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. $V_{SUP\_UVH} < V_{SUP} <$ 36 V, $V_{PRE\_PWM} + V_{PRE\_HDR} < V_{SUP\_PWR} <$ 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Static Electrical Characteristics					
V_{PRE_IN}	Input voltage range With $I_{PRE\_PWM} \leq$ 1.5 A and V_{BOS} = 5 V	V_{PRE_PWM} + V_{PRE_HDR}	—	36	V
V_{PRE_HDR}	Input voltage headroom range, 600 mA < $I_{PRE\_PWM} \leq$ 1.5 A	(Max R_{HS_PRE} + Max R_{DCR_LPRE}) x I_{PRE_PWM} x 1.25	—	—	V
	Input voltage headroom range, $I_{PRE\_PWM} \leq$ 600 mA	400	—	—	mV
V_{PRE_PWM}	Output voltage in *normal mode* (VPRE_OTP[5:0] configuration, 50 mV step)	3.7	—	6.35	V
V_{PRE_PFM}	Output voltage in *standby mode* (VPRE_LP_OTP[5:0] configuration, 50 mV step)	3.7	—	5.35	V
$V_{PRE\_ACC\_PWM}$	Output voltage accuracy in PWM mode for $I_{PRE\_PWM} \leq$ 1.5 A	-2	—	2	%
$V_{PRE\_ACC\_PFM\_150m}$ [1]	Output voltage accuracy in PFM mode 10 mA ≤ $I_{PRE\_PFM} \leq$ 100 mA $V_{SUP} = V_{SUP\_PWR}$ = 12 V V_{PRE_PFM} = 3.7 V VPRE_PFM_TON_OTP[1:0] = 10 $C_{OUT\_PRE} \geq$ 20 µF (effective value) L_{PRE} = 2.2 µH at F_{PRE} = 2.25 MHz and L_{PRE} = 10 µH at F_{PRE} = 450 kHz	-4	—	4	%
$V_{PRE\_ACC\_PFM\_10m}$ [1]	Output voltage accuracy in PFM mode $I_{PRE\_PFM} \leq$ 10 mA $V_{SUP} = V_{SUP\_PWR}$ = 12 V V_{PRE_PFM} = 5.05 V VPRE_PFM_TON_OTP[1:0] = 10 $C_{OUT\_PRE} \geq$ 20 µF (effective value) L_{PRE} = 2.2 µH at F_{PRE} = 2.25 MHz and L_{PRE} = 10 µH at F_{PRE} = 450 kHz	-1.5	—	1.5	%
I_{PRE_PWM}	Output current capability in PWM mode	—	—	1.5	A
I_{PRE_PFM}	Current capability in PFM mode (*standby mode* only)	—	—	150	mA
$\eta_{PRE\_PWM\_PEAK}$	Efficiency in PWM mode C_{OUT_PRE} = 22 µF with ESR = 2 mΩ L_{PRE} = 10 µH with R_{DCR_LPRE} = 60 mΩ F_{PRE} = 450 kHz $V_{SUP} = V_{SUP\_PWR}$ = 12 V V_{PRE_PWM} = 5.4 V with I_{PRE_PWM} = 600 mA	—	95	—	%

Table 160. VPRE electrical characteristics...*continued*

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < V_{SUP} < 36 V, V_{PRE_PWM} + V_{PRE_HDR} < V_{SUP_PWR} < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
$\eta_{PRE\_PWM\_PEAK}$[1]	Efficiency in PFM mode C_{OUT_PRE} = 22 µF with ESR = 2 mΩ, L_{PRE} = 10 µH with R_{DCR_LPRE} = 60 mΩ, F_{PRE} = 450 kHz V_{SUP} = V_{SUP_PWR} = 12 V and 5.4 V V_{PRE_PFM} = 5.05 V with I_{PRE_PFM} = 1 mA VPRE_PFM_TON_OTP[1:0] = 10	—	90	—	%
R_{HS_PRE}	High-side on-resistance (V_{BOS} = 5 V, including bonding)	—	310	500	mΩ
R_{LS_PRE}	Low-side on-resistance (V_{BOS} = 5 V, including bonding)	—	170	300	mΩ
R_{PRE_DIS}	Discharge resistor (when VPRE is disabled – LPOFF)	20	40	60	Ω
TSD_{PRE}	Thermal shutdown threshold	175	—	—	°C
TSD_{PRE_HYST}	Thermal shutdown threshold hysteresis	5	—	12	°C
$I_{PRE\_OC\_FLAG}$[2]	DC overcurrent flag threshold in PWM mode (set VPREOC_I) VPRE_OC_OTP[2:0] = 0 VPRE_OC_OTP[2:0] = 1 VPRE_OC_OTP[2:0] = 2 VPRE_OC_OTP[2:0] = 3 VPRE_OC_OTP[2:0] = 4 VPRE_OC_OTP[2:0] = 5 VPRE_OC_OTP[2:0] = 6 VPRE_OC_OTP[2:0] = 7	 0.45 0.65 0.85 1.12 1.30 1.49 1.68 1.87	 0.66 0.88 1.1 1.32 1.54 1.76 1.98 2.2	 1.0 1.25 1.45 1.70 1.95 2.12 2.38 2.64	A
I_{LIM_PRE}	VPRE output DC current limitation threshold in PWM mode	1.95	2.42	2.9	A
V_{PRE_OVP}	Main overvoltage protection on VPRE output (relative to VPRE output voltage setting)	20	25	30	%
Dynamic electrical characteristics					
t_{PRE_OVP}	Overvoltage deglitch time	1	2	3	µs
t_{PRE_DEAD}	Dead time to avoid cross conduction	1	—	20	ns
t_{PRE_SS}	Soft start ramp from 0 % to 100 % defined at I_{PRE_PWM} = 0 A VPRE_SS_OTP[1:0] = 0 (C_{OUT_PRE} ≤ 44 µF nominal) VPRE_SS_OTP[1:0] = 1 VPRE_SS_OTP[1:0] = 2 VPRE_SS_OTP[1:0] = 3	 200 431 873 1753	 269 538 1077 2150	 410 645 1281 2547	µs
$V_{PRE\_DVS\_DOWN}$	DVS down ramp rate during low-power mode transition VPRE_LP_DVS_OTP[1:0] = 0 (C_{OUT_PRE} ≤ 44 µF nominal) VPRE_LP_DVS_OTP[1:0] = 1 VPRE_LP_DVS_OTP[1:0] = 2 VPRE_LP_DVS_OTP[1:0] = 3	 18 9 4.5 2.25	 22 11 5.5 2.75	 27 13.5 6.75 3.375	mV/µs
$V_{PRE\_LINE\_REG\_450K\_PWM}$	Transient line in PWM mode with F_{PRE} = 450 kHz V_{BAT} = 6 V - 18 V – 6 V and 14 V - 35 V - 14 V I_{PRE_PWM} = 0 A and 1.5 A for V_{PRE_PWM} = 3.3 V I_{PRE_PWM} = 0 A and 0.6 A for V_{PRE_PWM} = 5.0 V dV/dt = 100 mV/µs, L_{PRE} = 10 µH, C_{IN_PRE} = 47 µF + PI filter, C_{OUT_PRE} = 44 µF	-1.5	—	1.5	%
$V_{PRE\_LINE\_REG\_450K\_DO}$	Transient line after drop out exit with F_{PRE} = 450 kHz V_{BAT} = V_{PRE_PWM} - 0.4 V to 14 V I_{PRE_PWM} = 0 A and 0.6 A for V_{PRE_PWM} = 5.0 V dV/dt = 100 mV/µs, L_{PRE} = 10 µH, C_{IN_PRE} = 47 µF + PI filter, C_{OUT_PRE} = 44 µF	-3	—	3	%
$V_{PRE\_LOTR\_450K\_PWM}$	Transient load response in PWM mode with F_{PRE} = 450 kHz 10 mA to 800 mA step and 800 mA to 10 mA step 800 mA to 1.5 A step and 1.5 A to 800 mA step di/dt = 300 mA/µs, C_{OUT_PRE} ≥ 22 µF, L_{PRE} = 10 µH	-3	—	3	%

Table 160. VPRE electrical characteristics*...continued*

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < V_{SUP} < 36 V, V_{PRE_PWM} + V_{PRE_HDR} < V_{SUP_PWR} < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
$V_{PRE\_LINE\_REG\_2M2\_PWM}$	Transient line in PWM mode with F_{PRE} = 2.25 MHz V_{BAT} = 6 V - 18 V - 6 V and 14 V - 35 V - 14 V I_{PRE_PWM} = 0 A and 1.5 A for V_{PRE_PWM} = 3.3 V I_{PRE_PWM} = 0 A and 0.6 A for V_{PRE_PWM} = 5.0 V dV/dt = 100 mV/µs, L_{PRE} = 2.2 µH, C_{IN_PRE} = 47 µF + PI filter, C_{OUT_PRE} = 44 µF	-1.5	—	1.5	%
$V_{PRE\_LINE\_REG\_2M2\_DO}$	Transient line after drop out exit F_{PRE} = 2.25 MHz V_{BAT} = V_{PRE_PWM} - 0.4 V to 14 V I_{PRE_PWM} = 0 A and 0.6 A for V_{PRE_PWM} = 5.0 V dV/dt = 100 mV/µs, L_{PRE} = 2.2 µH, C_{IN_PRE} = 47 µF + PI filter, C_{OUT_PRE} = 44 µF	-3	—	3	%
$V_{PRE\_LOTR\_2M2\_PWM}$	Transient load response in PWM mode F_{PRE} = 2.25 MHz 10 mA to 800 mA step and 800 mA to 10 mA step 800 mA to 1.5 A step and 1.5 A to 800 mA step di/dt = 300 mA/µs, C_{OUT_PRE} ≥ 22 µF, L_{PRE} = 2.2 µH	-3	—	3	%
$V_{PRE\_LINE\_REG\_450K\_PFM\_HV}$ [1]	Transient line in PFM mode with F_{PRE} = 450 kHz V_{BAT} = 12 V - 28 V – 12 V VPRE_PFM_TON_OTP[1:0] = 2 I_{PRE_PWM} = 10 µA and 10 mA for V_{PRE_PFM} = 5.05 V dV/dt = 100 mV/µs, L_{PRE} = 10 µH, C_{IN_PRE} = 47 µF + PI filter, C_{OUT_PRE} = 44 µF	-3	—	3	%
$V_{PRE\_LINE\_REG\_450K\_PFM\_LV}$ [1]	Transient line in PFM mode with F_{PRE} = 450 kHz V_{BAT} = 12 V - 28 V – 12 V VPRE_PFM_TON_OTP[1:0] = 10 I_{PRE_PFM} = 10 µA and 10 mA for V_{PRE_PFM} = 5.05 V dV/dt = 100 mV/µs, L_{PRE} = 10 µH, C_{IN_PRE} = 47 µF + PI filter, C_{OUT_PRE} = 44 µF	-3	—	3	%
$V_{PRE\_LINE\_REG\_450K\_PFM\_DO}$ [1]	Transient line after drop out exit with F_{PRE} = 450 kHz V_{BAT} = V_{PRE} - 0.4 V to 12 V VPRE_PFM_TON_OTP[1:0] = 2 I_{PRE_PFM} = 10 µA and 10 mA for V_{PRE_PFM} = 5.05 V dV/dt = 100 mV/µs, L_{PRE} = 2.2 µH, C_{IN_PRE} = 47 µF + PI filter, C_{OUT_PRE} = 44 µF	-3	—	3	%
$V_{PRE\_LOTR\_450K\_PFM\_150m}$ [1]	Transient load response in PFM mode with F_{PRE} = 450 kHz 10 mA to 100 mA step and 100 mA to 10 mA step di/dt = 300 mA/µs, C_{OUT_PRE} ≥ 22 µF, L_{PRE} = 10 µH VPRE_PFM_TON_OTP[1:0] = 2	-3	—	3	%
$V_{PRE\_LOTR\_450K\_PFM\_10m}$ [1]	Transient load response in PFM mode with F_{PRE} = 450 kHz VSUP = V_{SUP_PWR} = 5.4 V, V_{PRE} = 5.05 V 10 µA to 10 mA step and 10 mA to 10 µA step di/dt = 10 mA/µs, C_{OUT_PRE} ≥ 22 µF, L_{PRE} = 10 µH VPRE_PFM_TON_OTP[1:0] = 2	-1.5	—	1.5	%
$V_{PRE\_LINE\_REG\_2M2\_PFM\_HV}$ [1]	Transient line in PFM mode with F_{PRE} = 2.25 MHz V_{BAT} = 12 V - 28 V – 12 V VPRE_PFM_TON_OTP[1:0] = 2 I_{PRE_PFM} = 10 µA and 10 mA for V_{PRE_PFM} = 5.05 V dV/dt = 100 mV/µs, L_{PRE} = 2.2 µH, C_{IN_PRE} = 47 µF + PI filter, C_{OUT_PRE} = 44 µF	-3	—	3	%
$V_{PRE\_LINE\_REG\_2M2\_PFM\_LV}$ [1]	Transient line in PFM mode with F_{PRE} = 2.25 MHz V_{BAT} = 6 V - 12 V – 6 V VPRE_PFM_TON_OTP[1:0] = 2 I_{PRE_PFM} = 10 µA and 10 mA for V_{PRE_PFM} = 5.05 V dV/dt = 100 mV/µs, L_{PRE} = 2.2 µH, C_{IN_PRE} = 47 µF + PI filter, C_{OUT_PRE} = 44 µF	-3	—	3	%

Table 160. VPRE electrical characteristics*...continued*

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < V_{SUP} < 36 V, V_{PRE_PWM} + V_{PRE_HDR} < V_{SUP_PWR} < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
$V_{PRE\_LINE\_REG\_2M2\_PFM\_DO}$ [1]	Transient line after drop out exit with F_{PRE} = 2.25 MHz V_{BAT} = V_{PRE} - 0.4 V to 12 V VPRE_PFM_TON_OTP[1:0] = 2 I_{PRE_PFM} = 10 µA and 10 mA for V_{PRE_PFM} = 5.05 V dV/dt = 100 mV/µs, L_{PRE} = 2.2 µH, C_{IN_PRE} = 47 µF + PI filter, C_{OUT_PRE} = 44 µF	-3	—	3	%
$V_{PRE\_LOTR\_2M2\_PFM\_100m}$ [1]	Transient load response in PFM mode with F_{PRE} = 2.25 MHz 10 mA to 100 mA step and 100 mA to 10 mA step di/dt = 300 mA/µs, C_{OUT_PRE} ≥ 22 µF, L_{PRE} = 2.2 µH VPRE_PFM_TON_OTP[1:0] = 2	-3	—	3	%
$V_{PRE\_LOTR\_2M2\_PFM\_10m}$ [1]	Transient load response in PFM mode with F_{PRE} = 2.25 MHz V_{SUP} = V_{SUP_PWR} = 5.4 V, V_{PRE} = 5.05 V 10 µA to 10 mA step and 10 mA to 10 µA step di/dt = 10 mA/µs, C_{OUT_PRE} ≥ 22 µF, L_{PRE} = 2.2 µH VPRE_PFM_TON_OTP[1:0] = 2	-1.5	—	1.5	%
F_{PRE}	Operating frequency in PWM mode VPRE_CLK_OTP = 0 VPRE_CLK_OTP = 1	 390 1.90	 450 2.25	 500 2.5	 kHz MHz
t_{PRESW_SLR}	Switching node rising and falling edge setting VPRE_SR_OTP = 0 VPRE_SR_OTP = 1	 — —	 — —	 2 4	ns
$t_{PRE\_ON\_MIN\_450K}$	HS minimum ON time in PFM mode with F_{PRE} = 450 kHz VPRE_CLK_OTP = 0, V_{PRE_IN} = 12 V VPRE_PFM_TON_OTP[1:0] = 0 VPRE_PFM_TON_OTP[1:0] = 1 VPRE_PFM_TON_OTP[1:0] = 2 VPRE_PFM_TON_OTP[1:0] = 3	 715 800 875 975	 900 1000 1125 1250	 1080 1250 1375 1525	ns
$t_{PRE\_ON\_MIN\_2M2}$	HS minimum ON time in PFM mode with F_{PRE} = 2.25 MHz VPRE_CLK_OTP = 1, V_{PRE_IN} = 12 V VPRE_PFM_TON_OTP[1:0] = 0 VPRE_PFM_TON_OTP[1:0] = 1 VPRE_PFM_TON_OTP[1:0] = 2 VPRE_PFM_TON_OTP[1:0] = 3	 350 385 420 470	 440 500 550 600	 530 620 690 755	ns
$t_{PRE\_OFF\_MIN}$	HS minimum OFF time in PFM mode V_{PRE_IN} = 12 V VPRE_PFM_TOFF_OTP[1:0] = 2	465	720	1035	ns
External components					
L_{PRE}	Inductor value for F_{PRE} = 450 kHz Nominal[3] Effective[4]	 8.2 5.8	 10 —	 10 13	µH
	Inductor value for F_{PRE} = 2.25 MHz Nominal[3] Effective[4]	 2.2 1.5	 2.2 —	 4.7 6.1	µH
R_{DCR_LPRE}	Inductor DC resistance	—	60	—	mΩ
C_{IN_PRE}	Effective[4] input capacitor value	10	—	—	µF
C_{BOOT_PRE}	Nominal[3] bootstrap capacitor value Effective[4] bootstrap capacitor value	22 15	 —	68 89	nF
C_{OUT_PRE}	Effective[4] output capacitor value with F_{PRE} = 450 kHz Effective[4] output capacitor value with F_{PRE} = 2.25 MHz	20 20	— —	100 50	µF

[1] For all these parameters, the maximum ambient temperature is T_A = 85 °C.
[2] VPREOC_I flag is correctly reported when V_{PRE_PWM} + V_{PRE_HDR} < V_{SUP_PWR} < 18 V.

[3] For all regulators, the nominal value is the value normalized.
[4] For all regulators, the effective value is the value after tolerance, temperature, DC bias and aging removal.

20.2.2 VPRE efficiency in forced PWM mode

For information, VPRE efficiency versus current load measurement is given based on external components and configuration listed below. If the conditions are different, the new efficiency should be calculated using the FS26 power dissipation tool calculator.

Table 161. VPRE efficiency in forced PWM mode

Ext. C and L		
C_{IN_PRE}	20	µF
$C_{IN\_PRE\_ESR}$	5	mΩ
C_{OUT_PRE}	44	µF
$C_{OUT\_PRE\_ESR}$	2.5	mΩ
L_{VPRE_450kHz}	10	µH
$L_{VPRE\_DCR\_450kHz}$	75	mΩ
$L_{VPRE\_2.25MHz}$	2.2	µH
$L_{VPRE\_DCR\_2.25MHz}$	40	mΩ
C_{BOOT_PRE}	22	nF
Int. MOSFETs		
R_{HS_VPRE}	310	mΩ
Q_{HS}	0.8	nC
R_{LS_VPRE}	170	mΩ
Q_{LS}	1	nC
LS_{BODY_DIODE}	0.8	V
V_{DRIVE}	V_{BOS}	V
Configuration		
V_{PRE_IN}	14	V
VPRE_SR_OTP		0b00

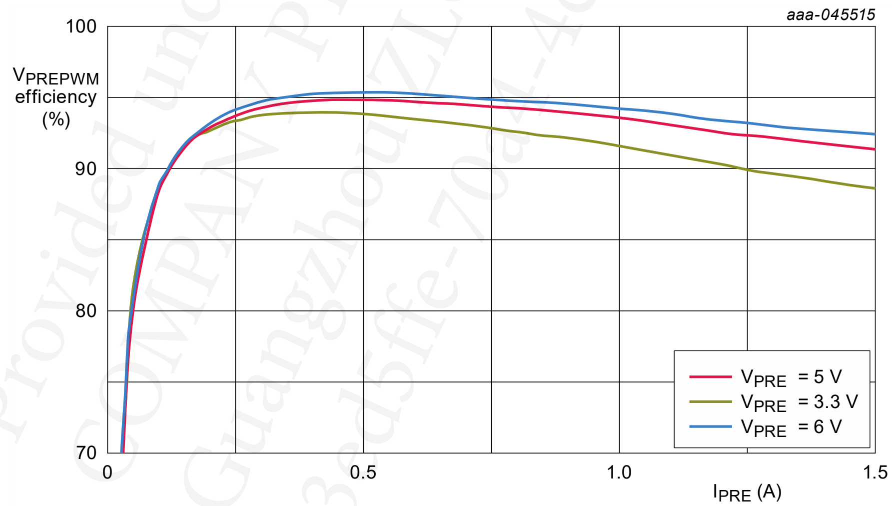

Figure 26. VPRE efficiency at VPRE_CLK_OTP = 0

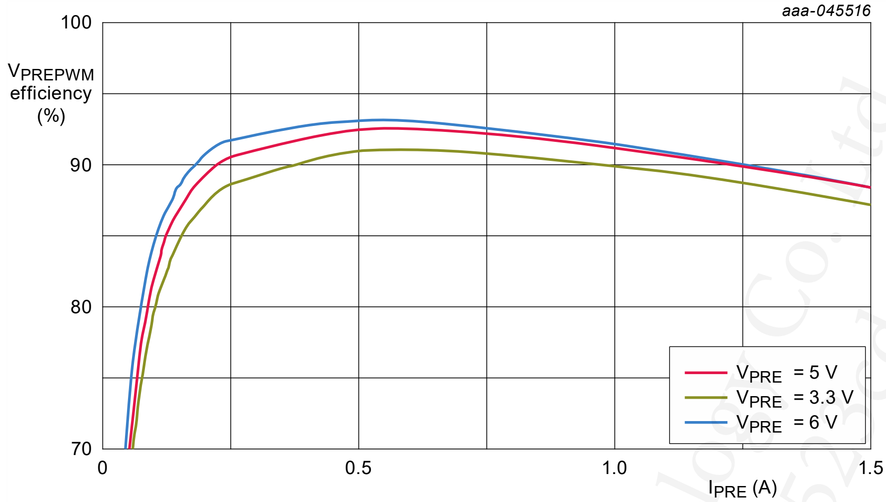

Figure 27. VPRE efficiency at VPRE_CLK_OTP = 1

20.3 VBST: Boost controller

The VBST block is an asynchronous, current mode boost controller. VBST works in forced PWM mode. The output voltage is configurable by OTP and the switching frequency is 450 kHz. A peak overcurrent detection is implemented using the voltage sensed across R_{SNS_BST}. The overcurrent detection can be selected with VBST_ILIM_OTP[1:0] bitfield and the value is equal to $V_{BST\_ILIM\_TH}$ divided by R_{SNS_BST}.

When the VBST_FB pin is disconnected, by means of $V_{BST\_FB} < V_{BST\_UV\_TH}$, the boost controller is stopped after t_{BST_UVOV}. VBST will restart automatically when $V_{BST\_FB} > V_{BST\_UV\_TH}$.

A maximum duty cycle protection is implemented in order to protect the boost controller in case of bad component selection.

Two boost topologies (front-end and back-end) are supported:

1. **In front-end mode (VBST_CFG_OTP = 0):**
   When VBST is used as the front-end supply, the battery voltage (V_{BAT}) is applied at the input of the boost controller. During normal operation with $V_{SUP} > V_{BST}$, the boost controller stops switching and operates in Pass-Through mode. When V_{SUP} drops below the VBST regulation threshold, the boost controller will start switching to regulate the V_{SUP} node to V_{BST}.
   NXP recommends setting the V_{BST} output voltage between 6 V and 10 V maximum, to supply VPRE with enough headroom during cranking pulses. If a higher output voltage is required for the application, the boost should be used in back-end mode.
   In the front-end configuration, VBST_OV_OTP must be set to 0 (Auto-enable). In Auto-enable mode, VBST will stop switching automatically when $V_{BST} > V_{BST\_OV\_TH}$, and will resume switching when V_{BST} drops below V_{BST_OTP}.
   In the front-end configuration, the boost will be enabled only during cranking events. To avoid a latent fault, the VBST_TMD bit can be used to force VBST to regulate at 17 V, no matter what the battery voltage is. This allows verification of VBST availability using the VBST_S status flag.
   An open drain output pin called VBST_PG is available to indicate the boost controller activity. This open drain pin should be connected externally to the VDDIO voltage through a resistor. When VBST_PG is high (open drain OFF) it indicates that the boost controller is switching. When VBST is operating in pulse skipping mode, VBST_PG behavior may not be guaranteed. When VBST_PG is low (open drain ON) it indicates that the boost controller is not switching or disabled.
   The VBST current limitation is sensed at the input and therefore the current capability can be estimated depending on V_{BST_IN}, the VBST voltage configuration and the external components (L_{BST}, R_{SNS_BST}, D_{BST}). As an example, Table 162 summarizes the maximum current capability during a cranking operation using L_{BST} = 4.7 µH and the recommended R_{SNS_BST} for C_{OUT_BST} = 40 µF.

Table 162. Maximum VBST output current in front-end configuration (DC_{BST_MAX} = 87.5 %, D_{BST} = 0.7 V, LS_{RDSON} = 50 mΩ, L_{BST_DCR} = 60 mΩ)

V_{BST_IN}	V_{BST}	$V_{BST\_ILIM\_TH}$ / R_{SNS_BST}	Maximum I_{BST}
2.7 V	6 V	180 mV / 20 mΩ	1.9 A
		150 mV / 20 mΩ	1.7 A
		120 mV / 20 mΩ	1.4 A
		60 mV / 20 mΩ	0.7 A
	7 V	180 mV / 20 mΩ	1.65 A
		150 mV / 20 mΩ	1.45 A
		120 mV / 20 mΩ	1.2 A
		60 mV / 20 mΩ	0.6 A
	8 V	180 mV / 20 mΩ	1.45 A
		150 mV / 20 mΩ	1.25 A
		120 mV / 20 mΩ	1.05 A
		60 mV / 20 mΩ	0.5 A

2. **In back-end mode or boost not used (VBST_CFG_OTP = 1):**
In the back-end configuration, VBST can be supplied by VPRE or by an external supply. When VBST is supplied by an external supply (VSUP, for example), the maximum duty cycle could limit the output current capability and/or the delta voltage between V_{BST_IN} and V_{BST}.
In the back-end configuration, the output voltage is set by VBST_OTP[4:0] and NXP recommends setting VBST_OV_OTP = 1 (overvoltage protection). In Overvoltage Protection mode, VBST will be disabled if an overvoltage is detected (V_{BST} > $V_{BST\_OV\_TH}$). A SPI command is needed to turn on VBST again.
VBST_PG is indicating a boost overload during soft start or in normal operation. The power good pin (VBST_PG) can be used to avoid an undervoltage cascading effect at the VBST input (VPRE) by opening the VBST current path. This overload protection feature will require the external circuitry described in the application note AN12995.
During a soft start, VBST_PG is at the high level (open drain OFF) to enable the external switch and propagate the output voltage to the load. If an overload condition is detected (V_{BST} < $V_{BST\_UV\_PG}$), while the minimum duty cycle is not reached, the VBST power good pin is asserted low to warn of the overload event. The BOOST controller remains enabled until completion of soft start.
In normal operation, VBST_PG is at the high level (open drain OFF) when the output voltage remains in an acceptable range and at the low level (open drain ON) when the output voltage is 25 % below its nominal voltage (V_{BST} < $V_{BST\_UV\_PG}$).
The VBST current limitation is sensed at the input, and therefore the current capability can be estimated depending on V_{BST_IN}, VBST voltage configuration and the external components (L_{BST}, R_{SNS_BST}, D_{BST}). As an example, Table 163 summarizes the maximum current capability for an input average current of 500 mA using L_{BST} = 4.7 µH and the recommended R_{SNS_BST} for C_{OUT_BST} = 40 µF.
When the boost controller is not used in the application, VBST_CFG_OTP and VSUP_UVTH_OTP should both be set to 1. The unused pins should be handled as described in Section 8.

Table 163. Maximum V_{BST} output current in back-end configuration for an input average current of 500 mA (DC_{BST_MAX} = 87.5 %, Efficiency = 85 %)

V_{BST_IN}	V_{BST}	R_{SNS_BST}	Maximum I_{BST}
3.3 V	7 V	60 mΩ	200 mA
	10 V	40 mΩ	140 mA
	12 V	20 mΩ	115 mA
5 V	7 V	80 mΩ	300 mA
	10 V	60 mΩ	210 mA
	12 V	40 mΩ	175 mA
	15 V	20 mΩ	140 mA
6 V	7 V	100 mΩ	360 mA
	10 V	80 mΩ	250 mA
	12 V	60 mΩ	210 mA
	15 V	40 mΩ	170 mA
	18 V	20 mΩ	140 mA

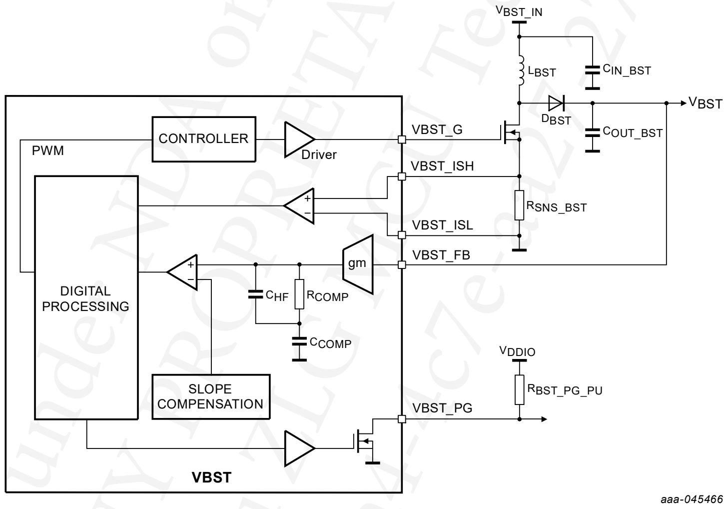

Figure 28. VBST schematic with configuration from VPRE

20.3.1 VBST electrical characteristics

Table 164. VBST electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. $V_{SUP\_UVH} < V_{SUP}$ < 36 V, $V_{PRE\_PWM} + V_{PRE\_HDR} < V_{SUP\_PWR}$ < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Static electrical characteristics					
V_{BST_IN}	Input voltage range	2.7	—	40	V
V_{BST}	Output voltage (OTP configuration, 250 mV step)	5	—	18	V
V_{BST_ACC}	Output voltage accuracy	-3	—	3	%

Table 164. VBST electrical characteristics*...continued*

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < V_{SUP} < 36 V, V_{PRE_PWM} + V_{PRE_HDR} < V_{SUP_PWR} < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
I_{BST}	Nominal output current in front-end VBST_CFG_OTP = 0 (VBST configured as front-end supply) V_{BST} ≤ 10 V and V_{BST_IN} ≥ 2.7 V	—	1	—	A
	Nominal output current in back-end VBST_CFG_OTP = 1 (VBST configured in back-end) V_{BST} ≤ 18 V and V_{BST_IN} ≥ 3.6 V (powered by VPRE)	—	—	0.5	A
$V_{BST\_ILIM\_TH}$	Voltage threshold to detect an inductor peak current limit condition Differential measurement at VBST_ISH pin and VBST_ISL pin VBST_ILIM_OTP[1:0] = 0 VBST_ILIM_OTP[1:0] = 1 VBST_ILIM_OTP[1:0] = 2 VBST_ILIM_OTP[1:0] = 3	48 96 120 144	60 120 150 180	72 144 180 216	mV
$V_{BST\_OV\_TH}$	Overvoltage threshold range (sensed on VBST_FB pin)	105	110	115	%
V_{BSTG}	VBST_G driver output voltage	V_{PRE_UVBOS} - 0.2	V_{BOS}	5.5	V
R_{BSTG}	VBST_G driver pull-down (when VBST is disabled)	6	14.5	23	kΩ
I_{BSTG}	VBST_G current drive at V_{BOS} = 5 V and V_{BSTG} = V_{BOS} / 2 VBSTLS_SR_OTP = 0 VBSTLS_SR_OTP = 1	0.7 0.9	— —	2.0 3.4	A
$V_{BST\_UV\_TH}$	Undervoltage threshold range (sensed on VBST_FB pin)	1.3	1.5	1.7	V
$V_{BST\_UV\_PG}$	VBST undervoltage threshold range to assert VBST_PG pin in back-end mode (sensed on VBST_FB pin)	72.5	75	77.5	%
$R_{BST\_PG\_PU}$	External pull-up resistor to VDDIO pin	5	10	20	kΩ
$V_{BST\_PG\_VOL}$	Low output level threshold (I_{BST_PG} = 2.0 mA)	—	—	0.4	V
$I_{BST\_PG\_LEAK}$	Input leakage current	—	—	1.0	μA
Dynamic electrical characteristics					
F_{BST}	Switching frequency range	380	450	500	kHz
t_{BST_UVOV}	$V_{BST\_UV\_TH}$, $V_{BST\_OV\_TH}$ filtering time	5	10	15	μs
DC_{BST_MAX}	Maximum duty cycle VBST_MAX_DC_OTP[1:0] = 0 VBST_MAX_DC_OTP[1:0] = 1 VBST_MAX_DC_OTP[1:0] = 2 VBST_MAX_DC_OTP[1:0] = 3	— — — —	72.5 77.5 82.5 87.5	— — — —	%
t_{BST_SS}	Soft start from VBST enable to 90 % VBST_SS_OTP[1:0] = 0 VBST_SS_OTP[1:0] = 1 VBST_SS_OTP[1:0] = 2 VBST_SS_OTP[1:0] = 3	—	425 850 1700 3400	600 1200 2400 4800	μs
$t_{BST\_SS\_DAC}$	Digital DAC soft start completion (delay from VBST enable in front-end to VPRE enable) VBST_SS_OTP[1:0] = 0 VBST_SS_OTP[1:0] = 1 VBST_SS_OTP[1:0] = 2 VBST_SS_OTP[1:0] = 3	—	1150 2300 4600 9200	1250 2500 5000 10100	μs
$V_{BST\_LINE\_ON}$	VBST transient line in front end configuration always ON V_{BAT} = 3.2 V - 6.5 V - 3.2 V dV/dt = 100 mV/μs , L_{BST} = 4.7 μH, I_{BST} = 0 A and 1 A $C_{IN\_BST\_FE}$ = 47 μF, $C_{OUT\_BST\_FE}$ = 50 μF	-5	—	5	%

Table 164. VBST electrical characteristics*...continued*

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < V_{SUP} < 36 V, V_{PRE_PWM} + V_{PRE_HDR} < V_{SUP_PWR} < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
$V_{BST\_LINE\_OFF\_ON}$	VBST transient line in front end configuration with OFF/ON transition V_{BAT} = 12.5 V - 6.5 V dV/dt = 100 mV/µs , L_{BST} = 4.7 µH, I_{BST} = 0 A and 1 A $C_{IN\_BST\_FE}$ = 47 µF, $C_{OUT\_BST\_FE}$ = 50 µF	-5	—	—	%
$V_{BST\_LINE\_ON\_OFF}$	VBST transient line in front end configuration with ON/OFF transition V_{BAT} = 6.5 V - 12.5 V dV/dt = 100 mV/µs , L_{BST} = 4.7 µH, I_{BST} = 0 A and 1 A $C_{IN\_BST\_FE}$ = 47 µF, $C_{OUT\_BST\_FE}$ = 50 µF	—	—	1.5	V
$V_{BST\_LOTR\_FE}$	Transient load response in Front end mode 200 mA to 1 A step and 1 A to 200 mA step, di/dt = 800 mA/µs $C_{OUT\_BST\_FE}$ = 40 µF, L_{BST} = 4.7 µH, $C_{IN\_BST\_FE}$ = 20 µF 2.7 V ≤ V_{BST_IN} ≤ V_{BST} - 1 V, V_{BST} = 7 V	-10	—	10	%
$V_{BST\_LOTR\_BE}$	Transient load response in Back end mode 50 mA to 200 mA step and 200 mA to 50 mA step, di/dt = 150 mA/µs $C_{OUT\_BST\_BE}$ = 22 µF, L_{BST} = 4.7 µH, $C_{IN\_BST\_BE}$ = 44 µF V_{BST_IN} = 4.5 V, V_{BST} = 14 V	-5	—	5	%
t_{ON_MIN}	LS minimum ON time VBST_TON_MIN_OTP[1:0] = 0	153	200	235	ns
External components					
L_{BST}	Inductor value Nominal[1] Effective[2]	 4.7 3.3	 4.7 —	 4.7 6.1	µH
L_{BST_DCR}	Inductor DC resistance	—	60	—	mΩ
R_{SNS_BST}	Nominal[1] current sense resistor value (±1 %)	20	—	100	mΩ
D_{BST}	Diode forward voltage drop	—	0.4	—	V
LS_{RDSON}	Low-side MOSFET $R_{DS(on)}$	—	50	—	mΩ
$C_{IN\_BST\_FE}$	Effective[2] input capacitor value for VBST in front-end	10	—	—	µF
$C_{IN\_BST\_BE}$	Effective[2] input capacitor value for VBST in back-end (in addition to C_{OUT_PRE})	10	—	—	µF
$C_{OUT\_BST\_FE}$	Effective[2] output capacitor value for VBST in front-end	20	—	150	µF
$C_{OUT\_BST\_BE}$	Effective[2] output capacitor value for VBST in back-end	20	—	80	µF

[1] For all regulators, the nominal value is the value normalized.
[2] For all regulators, the effective value is the value after tolerance, temperature, DC bias and aging removal.

20.3.2 VBST efficiency

VBST efficiency vs. current load measurement is shown in Table 165 based on external components and the configuration listed below. If the conditions are different, calculate the efficiency using the FS26 power dissipation tool calculator.

Table 165. VBST efficiency measurement settings

Ext. Components		
$C_{IN\_BST\_BE}$	22	µF
$C_{IN\_BST\_BE\_ESR}$	2.5	mΩ
$C_{OUT\_BST\_BE}$	44	µF
$C_{OUT\_BST\_BE\_ESR}$	1	mΩ
L_{BST}	4.7	µH
L_{BST_DCR}	60	mΩ
R_{SNS_BST}	20	mΩ
D_{BST}	0.5	V

Table 165. VBST efficiency measurement settings*...continued*

Ext. Components		
Ext. MOSFET		
LS_{RDSON}	30	mΩ
Q_{LS}	7	nC
LS_{BODY_DIODE}	0.7	V
V_{DRIVE}	V_{BOS}	V
Configuration		
V_{BST_IN}	6	V
F_{BST}	450	kHz
VBSTLS_SR_OTP		0b01
VBST_ILIM_OTP		0b11
VBST_MAX_DC_OTP		0b11

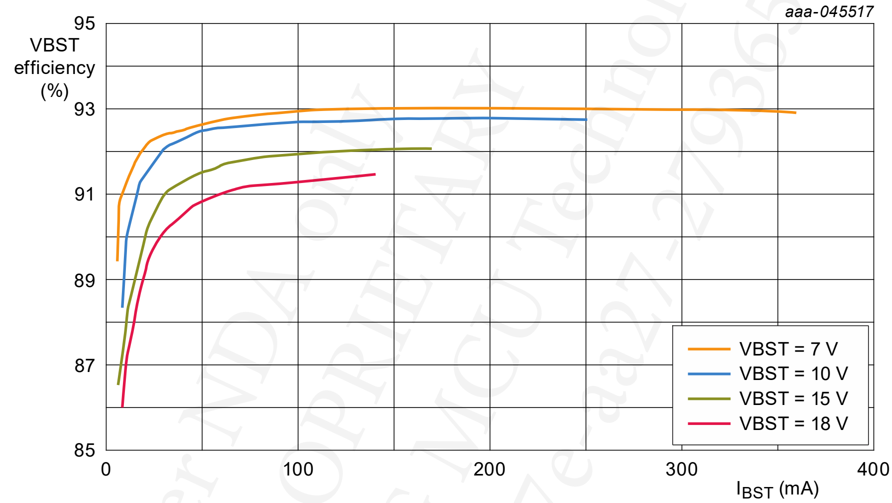

Figure 29. VBST efficiency in back-end mode

20.4 VCORE: low-voltage buck regulator

The VCORE block is a low-voltage integrated synchronous buck operating in forced PWM mode and using internal FETs. The output voltage is configurable by OTP in a range from 0.8 V to 3.35 V, and the switching frequency is 2.25 MHz. Compensation is ensured by internal circuitry.

A dynamic voltage scaling (DVS) feature is configurable by OTP, to control the ramp-up and ramp-down of the regulator. The passive pull-down resistor is enabled during the ramp down.

The current in the inductor is sensed via the internal FETs. A thermal shutdown is implemented to protect the internal FETs. When the current in the inductor rises above the I_{CORE_PEAK} threshold configured with the CORE_ILIM_OTP[1:0] bits, the SPI bit COREOC_I is set. This overcurrent detection does not turn OFF the VCORE but will induce a duty cycle reduction and therefore an output voltage drop.

During the overcurrent condition, the regulator switching frequency may be divided by 2. The regulator will be back to its nominal switching frequency when the overcurrent condition is removed. When the lower CORE_ILIM_OTP[1:0] setting is selected, it is recommended to select L_{CORE} at 1.5 μH or 2.2 μH.

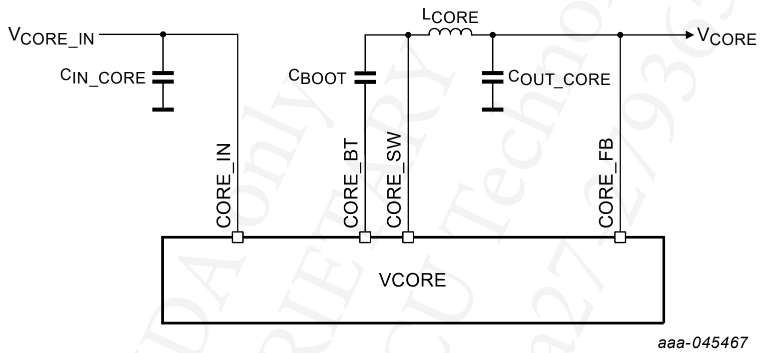

Figure 30. VCORE schematic

Table 166. VCORE electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. $V_{SUP\_UVH} < V_{SUP} < 36$ V, $V_{PRE\_PWM} + V_{PRE\_HDR} < V_{SUP\_PWR} < 36$ V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Static electrical characteristics					
V_{CORE_IN}	Input voltage range	2.5	—	6.35	V
V_{CORE}	Output voltage (OTP configuration, 10 mV step)	0.8	—	3.35	V
I_{CORE}	Output current capability FS260x and FS261x FS262x and FS263x	 — —	 — —	 0.8 1.65	A
V_{CORE_ACC}	Output voltage accuracy $I_{OUT} \le 1.5$ A 1.5 A < $I_{OUT} \le 1.65$ A	 -2 -2.5	 — —	 2 2.5	%
V_{CORE_HDR}	Minimum headroom ($V_{CORE\_IN} – V_{CORE}$) $I_{CORE} \le 800$ mA $I_{CORE} \le 1.5$ A $I_{CORE} \le 1.65$ A	 400 800 900	 — — —	 — — —	mV
$I_{CORE\_PEAK\_0A8}$	Inductor peak current limitation for FS260x and FS261x CORE_ILIM_OTP[1:0] = 0 CORE_ILIM_OTP[1:0] = 1, 2 or 3	 0.9 1.15	 1.4 1.7	 1.9 2.3	A

Table 166. VCORE electrical characteristics*...continued*

T_A = –40 °C to 125 °C, unless otherwise specified. $V_{SUP\_UVH} < V_{SUP} <$ 36 V, $V_{PRE\_PWM} + V_{PRE\_HDR} < V_{SUP\_PWR} <$ 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
$I_{CORE\_PEAK\_1A65}$	VCORE inductor peak current limitation for FS262x and FS263x CORE_ILIM_OTP[1:0] = 0 CORE_ILIM_OTP[1:0] = 1 CORE_ILIM_OTP[1:0] = 2 CORE_ILIM_OTP[1:0] = 3	 0.9 1.15 2.0 2.5	 1.4 1.7 2.7 3.4	 1.9 2.2 3.4 4.3	A
η_{CORE_PEAK}	Peak efficiency in PWM mode V_{PRE_PWM} = 5.5 V, V_{CORE} = 1.5 V, I_{CORE} = 800 mA L_{CORE} = 1 μH with DCR = 30 mΩ C_{OUT_CORE} = 20 μF (effective capacitance)	—	87	—	%
R_{HS_CORE}	High-side on-resistance (V_{BOS} = 5 V, including bonding)	—	75	150	mΩ
R_{LS_CORE}	Low-side on-resistance (V_{BOS} = 5 V, including bonding)	—	75	150	mΩ
R_{CORE_DIS}	Discharge resistor (when V_{CORE} is disabled – LP OFF)	50	100	200	Ω
TSD_{CORE}	Thermal shutdown threshold	175	—	—	°C
TSD_{CORE_HYS}	Thermal shutdown threshold hysteresis	5	—	12	°C
Dynamic electrical characteristics					
t_{VCORE_DEAD}	Dead time to avoid cross conduction COREHS_SR_OTP[1:0] = 1 COREHS_SR_OTP[1:0] = 2 COREHS_SR_OTP[1:0] = 0 or 3	 10 5 5	 — — —	 40 30 25	ns
t_{CORESW_HSSRR}[1]	Switching node slew rate (rising) COREHS_SR_OTP[1:0] = 0 COREHS_SR_OTP[1:0] = 1 COREHS_SR_OTP[1:0] = 2 COREHS_SR_OTP[1:0] = 3	 2.5 2 2.25 2.5	 5 4 4.5 5	 — — — —	V/ns
t_{CORESW_HSSRF}[1]	Switching node slew rate (falling) COREHS_SR_OTP[1:0] = 0 COREHS_SR_OTP[1:0] = 1 COREHS_SR_OTP[1:0] = 2 COREHS_SR_OTP[1:0] = 3	 1 0.25 0.5 1	 2.2 0.6 1.2 2.2	 — — — —	V/ns
V_{CORE_SS}	Soft start ramp rate from 10 % to 90 % (DVS up and down) CORE_SS_OTP[1:0] = 0 CORE_SS_OTP[1:0] = 1 CORE_SS_OTP[1:0] = 2 CORE_SS_OTP[1:0] = 3 (C_{OUT_CORE} < 80 μF nominal)	 2 4 8 16	 2.5 5 10 20	 3 6 12 24	mV/μs
V_{CORE_LOTR1}	Transient load response for V_{CORE} ≥ 1.0 V 10 mA to 800 mA step and 800 mA to 10 mA step with di/dt = 300 mA/μs, C_{OUT_CORE} ≥ 22 μF, L_{CORE} = 1.0 μH	-3	—	3	%
V_{CORE_LOTR2}	Transient load response for VCORE ≤ 1.0 V 10 mA to 800 mA step and 800 mA to 10 mA step with di/dt = 300 mA/μs, C_{OUT_CORE} ≥ 40 μF, L_{CORE} = 1.0 μH	-30	—	30	mV
F_{CORE}	Operating frequency in PWM mode	2.0	2.25	2.50	MHz
$t_{CORE\_ONOFF\_MIN\_P}$	HS minimum ON and OFF time in peak current mode F_{OSC_HIGH} = 18 MHz (CLK_FREQ_OTP[1:0] = 10)	10	45	72	ns

Table 166. VCORE electrical characteristics*...continued*

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < V_{SUP} < 36 V, V_{PRE_PWM} + V_{PRE_HDR} < V_{SUP_PWR} < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
$t_{CORE\_ONOFF\_MIN\_V}$	HS minimum ON and OFF time in valley current mode F_{OSC_HIGH} = 18 MHz (CLK_FREQ_OTP[1:0] = 10)	30	55	72	ns
External Components					
L_{CORE}	CORE_LSEL_OTP[1:0] = 0 Nominal[2] inductor value Effective[3] inductor value	1 0.68	1 —	1 1.5	µH
	CORE_LSEL_OTP[1:0] = 1 Nominal[2] inductor value Effective[3] inductor value	1.5 1	1.5 —	1.5 2	µH
	CORE_LSEL_OTP[1:0] = 2 or 3 Nominal[2] inductor value Effective[3] inductor value	2.2 1.5	2.2 —	2.2 2.9	µH
R_{DCR_LCORE}	Inductor DC resistance	—	30	—	mΩ
C_{IN_CORE}	Effective[3] input capacitor value	2.2	—	—	µF
C_{BOOT_CORE}	Bootstrap capacitor Nominal[2] Effective[3]	47 33	47 —	47 62	nF
C_{OUT_CORE}	Effective[3] output capacitor	20	—	100	µF

[1] Covered by characterization only, at I_{CORE} = 1 A, with KITFS26AEEVM.
[2] For all regulators, the nominal value is the value normalized.
[3] For all regulators, the effective value is the value after tolerance, temperature, DC bias and aging removal.

20.4.1 VCORE efficiency

VCORE efficiency vs. current load measurement is shown in Table 167 based on external components and the configuration listed below. If the conditions are different, calculate the efficiency using the FS2630 power dissipation tool calculator.

Table 167. VCORE efficiency measurement settings

Ext. C and L		
C_{IN_CORE}	10	µF
$C_{IN\_CORE\_ESR}$	2.5	mΩ
C_{OUT_CORE}	44	µF
$C_{OUT\_CORE\_ESR}$	2.5	mΩ
L_{CORE}	1	µH
L_{CORE_DCR}	50	mΩ
C_{BOOT_CORE}	47	nF
Internal MOSFETs		
R_{HS_CORE}	75	mΩ
Q_{HS}	1.2	nC
R_{LS_CORE}	75	mΩ

Table 167. VCORE efficiency measurement settings...*continued*

Ext. C and L		
Q_{LS}	0.7	nC
LS_{BODY_DIODE}	0.8	V
V_{DRIVE}	V_{BOS}	V
Configuration		
V_{CORE_IN}	6	V
F_{CORE}	2.25	MHz
COREHS_SR_OTP[1:0]		0
CORE_CTRL_OTP		0

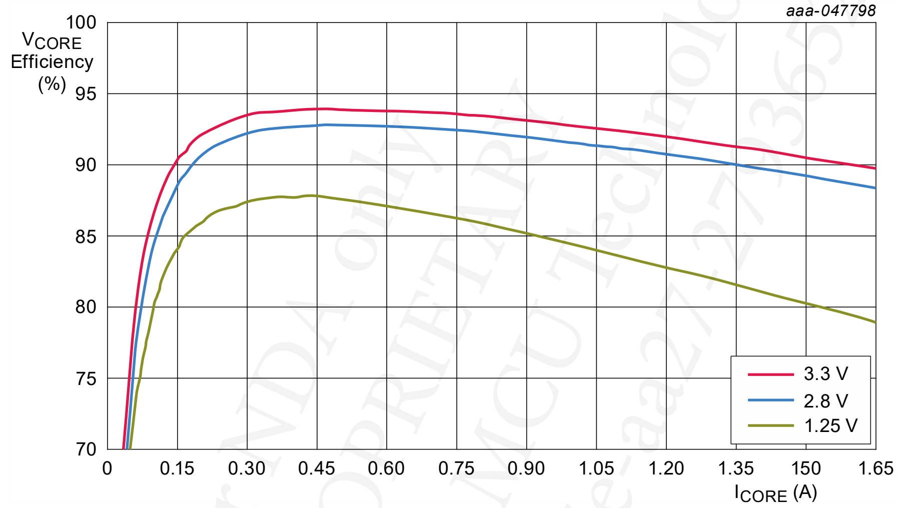

Figure 31. VCORE efficiency

20.5 LDO1 and LDO2: LDO regulators

LDO1 and LDO2 are linear voltage regulators with output voltage between 3.3 V and 5.0 V selectable via OTP, and with up to 400 mA output current capability.

The LDOIN pin is the input voltage supply for both LDO1 and LDO2, and it is intended to be connected to the VPRE output. An overcurrent detection and a thermal shutdown protection are integrated in each LDO.

These regulators are intended to supply microcontroller rails, CAN or FLEXRAY transceivers, as well as other integrated circuits within the ECU.

During *standby mode*, LDOs can be enabled (based on OTP configuration) with minimum additional power consumption.

When the output current rises above the I_{LIM_LDOx} threshold, the corresponding SPI bit LDOxOC_I is set. An overcurrent detection does not turn OFF the corresponding LDO, but will induce an output voltage drop.

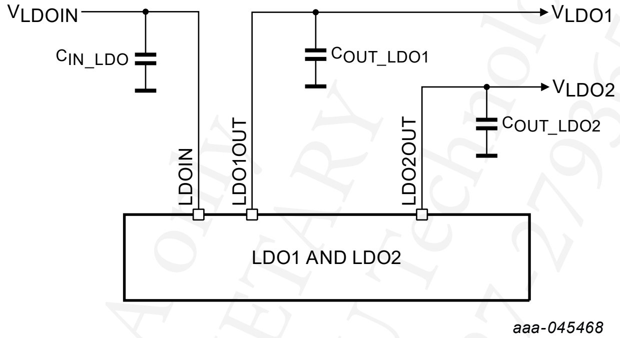

Figure 32. LDOx block diagram

Table 168. LDOx Electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < V_{SUP} < 36 V, V_{PRE_PWM} + V_{PRE_HDR} < V_{SUP_PWR} < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Static electrical characteristics					
V_{LDOIN}	Input voltage range	V_{LDOx} + $V_{LDOx\_HDR\_NORMAL}$	—	6.35	V
$V_{LDOx\_HDR\_NORMAL}$	Minimum headroom in *normal mode* (V_{LDOIN} – V_{LDOx}) 0 mA ≤ I_{LDOx} ≤ 400 mA	350	—	—	mV
$V_{LDOx\_HDR\_STBY}$ [1]	Minimum headroom in *standby mode* (V_{LDOIN} – V_{LDOx}) 0 mA ≤ I_{LDOx} ≤ 10 mA	50	—	—	mV
V_{LDOx}	Output voltage in *normal mode* VLDOx_OTP = 0 VLDOx_OTP = 1	 — —	 3.3 5.0	 — —	V
$V_{LDOx\_ACC\_NORMAL}$	Output voltage accuracy in *normal mode* 0 mA ≤ I_{LDOx} ≤ 400 mA , $V_{LDOx\_HDR\_NORMAL}$ = 350 mV	-1.75	—	1.75	%
$V_{LDOx\_ACC\_STBY}$ [1]	Output voltage accuracy in *Ssandby mode* 0 mA ≤ I_{LDOx} ≤ 10 mA , $V_{LDOx\_HDR\_STBY}$ = 50 mV	-1	—	1	%
$V_{LDOx\_VREF\_MATCH}$	LDOx versus VREF matching factor in *normal mode* 0 mA ≤ I_{LDOx} ≤ 400 mA , 0 mA ≤ I_{REF} ≤ 30 mA	-1	—	1	%
I_{LDOx}	Nominal current at V_{LDOx} = 5 V V_{LDOx} = 3.3 V and V_{LDOIN} ≤ 5.5 V V_{LDOx} = 3.3 V and V_{LDOIN} > 5.5 V	 — — —	 — — —	 400 400 300	mA
I_{Q_LDOx} [1]	Quiescent current consumption in Low-power modes $V_{LDOx\_HDR\_STBY}$ = 50 mV or 350 mV	—	7	55	µA
I_{LIM_LDOx}	Current limitation threshold reported in LDOxOC_I	450		1750	mA
$PSRR_{LDOx\_450kHz}$	Power supply rejection ratio V_{LDOx_HDR} = 350 mV, 1 µA < I_{LDOx} < 400 mA @ 450 kHz	22	—	—	dB
$PSRR_{LDOx\_2.2MHz}$	Power supply rejection ratio V_{LDOx_HDR} = 350 mV, 1 µA < I_{LDOx} < 400 mA @ 2.25 MHz	32	—	—	dB
R_{LDOxOC_I}	Discharge resistance (when V_{LDOx} is disabled)	—	20	60	Ω
R_{ON_LDOx}	Dropout resistance including bounding			600	mΩ
TSD_{LDOx}	Thermal shutdown threshold	175	—	—	°C
TSD_{LDOx_HYS}	Thermal shutdown threshold hysteresis	5	—	12	°C
Dynamic electrical characteristics					
t_{LDOx_TSD}	Thermal shutdown filtering time	3	5	8	µs
V_{LDOx_SS}	Soft start ramp rate	10	20	30	mV/µs

Table 168. LDOx Electrical characteristics*...continued*

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < V_{SUP} < 36 V, V_{PRE_PWM} + V_{PRE_HDR} < V_{SUP_PWR} < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
V_{LDOx_LOTR}	Transient load response I_{LDOx} = 10 mA to 200 mA step and 200 mA to 10 mA di/dt = 100 mA/µs C_{OUT_LDOx} = 4.7 µF, C_{IN_LDO} = 1 µF	-3	—	3	%
$V_{LDOx\_LOTR\_STBY\_HI}$	Transient load response in *standby mode* I_{LDOx} = 10 mA to 100 mA step and 100 mA to 10 mA di/dt = 100 mA/µs V_{PRE_PFM} = 5.35 V, V_{LDOx} = 5 V C_{OUT_LDOx} = 4.7 µF, C_{IN_LDO} = 1 µF	-100	—	100	mV
$V_{LDOx\_LOTR\_STBY\_LO}$[1]	Transient load response in *standby mode* with reduced headroom I_{LDOx} = 10 µA to 10 mA step and 10 µA to 10 mA di/dt = 10 mA/µs V_{PRE_PFM} = 5.05 V , V_{LDOx} = 5 V C_{OUT_LDOx} = 4.7 µF , C_{IN_LDO} = 1 µF	-1.5	—	1.5	%
t_{ON_LDOx}	Turn on rise time (soft start ramp)	—	—	500	µs
External components					
C_{IN_LDO}	Effective[2] input capacitor (close to LDOIN pin)	0.5	—	—	µF
C_{OUT_LDOx}	Effective[2] output capacitance	2.35	4.7	15	µF

[1] For all these parameters, the maximum ambient temperature is T_A = 85 °C.
[2] For all regulators, the effective capacitor value is the capacitor value after tolerance, DC bias and aging removal.

20.6 VREF: voltage reference

The VREF block is a high accuracy linear voltage regulator with 0.75 % accuracy over the device operating voltage and temperature range. The VREF output voltage is selectable between 3.3 V and 5.0 V via OTP, with 30 mA output current capability.

The TRKIN pin is the input voltage supply for VREF, and it is intended to be connected to the VPRE output. An overcurrent detection is integrated. When the output current rises above the I_{LIM_REF} threshold, the overcurrent detection does not turn OFF the VREF but will induce an output voltage drop.

VREF is intended to supply the microcontroller ADC reference, and to be the reference for the voltage tracking regulators (TRKx) in the FS2630 device.

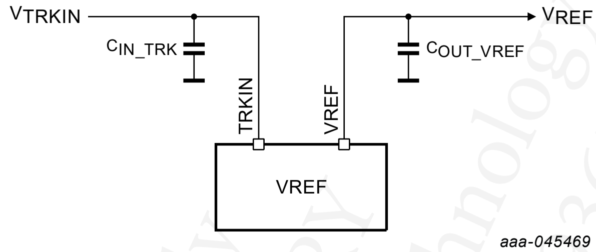

Figure 33. VREF block diagram

Table 169. VREF electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. $V_{SUP\_UVH} < V_{SUP} <$ 36 V, $V_{PRE\_PWM} + V_{PRE\_HDR} < V_{SUP\_PWR} <$ 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Static electrical characteristics					
V_{TRKIN}	Input voltage range	V_{REF} + V_{REF_HDR}	—	6.35	V
V_{REF}	Output voltage VREF_OTP = 0 VREF_OTP = 1	 — —	 3.3 5.0	 — —	V
V_{REF_HDR}	Minimum headroom ($V_{TRKIN} – V_{REF}$)	350	—	—	mV
V_{REF_ACC}	Output voltage accuracy, I_{REF} ≤ 30 mA	-0.75	—	0.75	%
I_{REF}	Nominal current capability	—	—	30	mA
I_{LIM_REF}	Output current limitation	38	—	95	mA
R_{REF_DIS}	Discharge resistor (when V_{REF} is disabled)	80	—	220	Ω
Dynamic electrical characteristics					
V_{REF_SS}	Soft start ramp rate from 10 % to 90 % V_{REF} = 3.3 V V_{REF} = 5.0 V	3.2	—	58	mV/µs
$PSRR_{VREF\_450kHz}$	Power supply rejection ratio V_{REF_HDR} = 350 mV, 100 µA < I_{REF} < 30 mA @ 450 kHz	25	—	—	dB
$PSRR_{VREF\_2.2MHz}$	Power supply rejection ratio V_{REF_HDR} = 350 mV, 100 µA < I_{REF} < 30 mA @ 2.25 MHz	35	—	—	dB

Table 169. VREF electrical characteristics*...continued*

T_A = –40 °C to 125 °C, unless otherwise specified. $V_{SUP\_UVH} < V_{SUP}$ < 36 V, $V_{PRE\_PWM} + V_{PRE\_HDR} < V_{SUP\_PWR}$ < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
V_{REF_LOTR}	Transient load response I_{REF} = 100 µA to 10 mA step and 10 mA to 100 µA di/dt = 100 mA/µs	-0.5	—	0.5	%
External components					
C_{OUT_VREF}	V_{REF} effective[1] output capacitance	1.1	2.2	3.3	µF

[1] For all regulators, the effective capacitor value is the capacitor value after tolerance, DC bias and aging removal.

20.7 TRK1 and TRK2: voltage tracking regulators

TRK1 and TRK2 are linear voltage regulators following a known voltage reference. The output voltage of the tracking regulators can track either VREF, LDO2, or an internal LDO reference.

TRK1 and TRK2 are intended to supply sensors located outside the ECU, therefore each voltage tracker is independently protected against short circuit to ground and short circuit to battery. An overcurrent detection and a thermal shutdown protection are integrated in each tracker.

When the output current rises above the I_{LIM_TRKx} threshold, the corresponding SPI bit TRKxOC_I is set. An overcurrent detection does not turn OFF the corresponding tracker but will induce an output voltage drop.

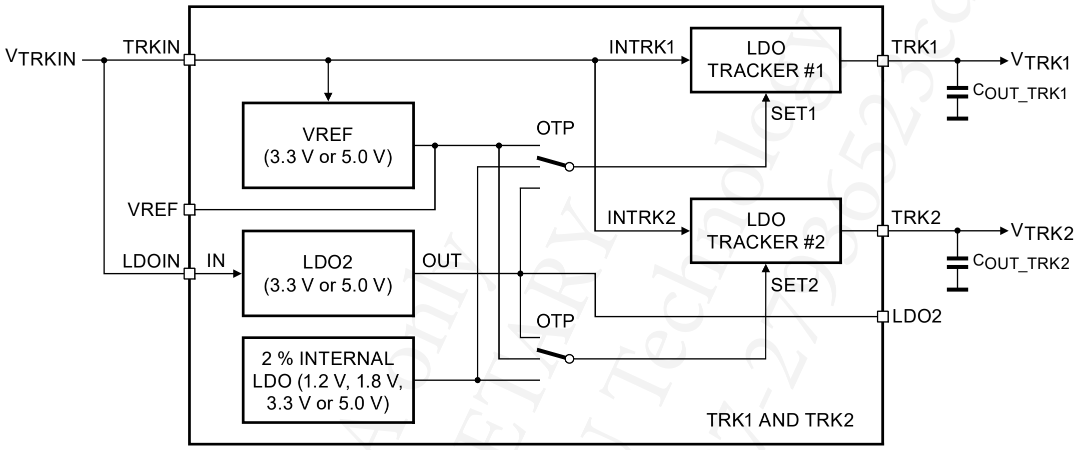

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Figure 34. TRK1 and TRK2 block diagram

Table 170. TRKx Electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < V_{SUP} < 36 V, V_{PRE_PWM} + V_{PRE_HDR} < V_{SUP_PWR} < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Static electrical conditions					
V_{TRKIN}	Input reference voltage range	V_{TRKx} + V_{TRKx_HDR}	—	6.35	V
$V_{TRKx\_HDR\_125}$	Minimum headroom (V_{TRKIN} – V_{TRKx}) for I_{TRKx} = 125 mA	350	—	—	mV
$V_{TRKx\_HDR\_150}$	Minimum headroom (V_{TRKIN} – V_{TRKx}) for I_{TRKx} = 150 mA	500	—	—	mV
V_{TRKx}	Output voltage V_{SETx} = V_{REF} = 3.3 V V_{SETx} = V_{REF} = 5.0 V V_{SETx} = Internal LDO = 1.2 V V_{SETx} = Internal LDO = 1.8 V V_{SETx} = Internal LDO = 3.3 V V_{SETx} = Internal LDO = 5.0 V V_{SETx} = V_{LDO2} = 3.3 V V_{SETx} = V_{LDO2} = 5.0 V	 — — — — — — — —	 3.3 5.0 1.2 1.8 3.3 5.0 3.3 5.0	 — — — — — — — —	V
V_{TRKx_ACC}	Tracker output voltage accuracy when V_{SETx} = Internal LDO	-2	—	2	%
V_{TRKx_OFF}	Offset voltage between tracker output voltage and tracking reference (V_{TRKx} - V_{SETx}) V_{SETx} = V_{REF} or V_{LDO2} 0 mA < I_{TRKx} < 150 mA	-10	—	10	mV

Table 170. TRKx Electrical characteristics*...continued*

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < V_{SUP} < 36 V, V_{PRE_PWM} + V_{PRE_HDR} < V_{SUP_PWR} < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
I_{TRKx}	Output current capability V_{TRKx_HDR} = 500 mV, V_{TRKx} = 3.3 V or 5 V V_{TRKx_HDR} = 350 mV, V_{TRKx} = 3.3 V or 5 V V_{TRKx} = 1.2 V or 1.8 V	 — — —	 — — —	 150 125 65	mA
I_{LIM_TRKx}	Output current limitation	160	—	360	mA
I_{TRKx_LEAK}	Reverse current leakage (V_{TRKx} = 40 V). Valid when TRKx is disabled and also in *standby mode* and *LPOFF mode*.	—	—	1.7	mA
$PSRR_{TRKx\_450KHz}$	Power supply rejection ratio V_{TRKx_HDR} = 350 mV, 100 µA < I_{TRKx} < 125 mA @ 450 kHz C_{OUT_TRKx}[1] = 2.2 µF	20	—	—	dB
$PSRR_{TRKx\_2.2MHz}$	Power supply rejection ratio V_{TRKx_HDR} = 350 mV, 100 µA < I_{TRKx} < 125 mA @ 2.2 MHz C_{OUT_TRKx}[1] = 2.2 µF	25	—	—	dB
R_{TRKx_DIS}	Discharge resistance (when TRKx is disabled)	-	100	155	Ω
TSD_{TRKx}	Thermal shutdown threshold	175	—	—	°C
TSD_{TRKx_HYS}	Thermal shutdown threshold hysteresis	5	—	12	°C
Dynamic electrical conditions					
t_{TRKx_TSD}	Thermal shutdown filtering time	3	5	8	µs
V_{TRKx_SLR}	Output voltage ramp rate from 10 % to 90 %	6		15	mV/µs
V_{TRKx_LOTR}	Transient load response I_{TRKx} = 100 µA to 125 mA step and 125 mA to 100 µA di/dt = 125 mA/µs	-3	—	3	%
External components					
C_{IN_TRKx}	Effective[1] input capacitor (close to TRKIN pin)	0.5	—	—	µF
C_{OUT_TRKx}	Effective[1] output capacitance	1.1	2.2	10	µF

[1] For all regulators, the effective capacitor value is the capacitor value after tolerance, DC bias and aging removal.

21 System enhancement functions

21.1 Clock management of the Main domain

The main clock management block is comprised of one high-frequency oscillator, one low-frequency system oscillator, and multiple dividers to generate clocking for the internal main digital state machine, for the low power clock, and for the switching regulators.

The low-frequency oscillator runs at 98 kHz. This oscillator is used for the Long Duration Timer (LDT) and remains ON in Low Power modes to filter the wake-up sources.

The high-frequency oscillator runs at 18 MHz by default. The frequency and the spread spectrum can be configured by SPI to reduce the emission of the oscillator fundamental frequency. The oscillator is used for the SMPS regulators and all the main domain timings. This oscillator is OFF in Low Power modes to reduce the current consumption.

Two frequency dividers provide lower frequency clocks for the switching regulators:

- CLK1 is set at the high-frequency oscillator divided by 8.
- CLK2 is set at the high-frequency oscillator divided by 40.

The frequency of the switching voltage regulators is assigned as shown in Table 171.

Table 171. Switching clock assignment

Regulator	CLK1	CLK2
VBST	No	Yes
VCORE	Yes	No
VPRE	VPRE_CLK_OTP = 1	VPRE_CLK_OTP = 0

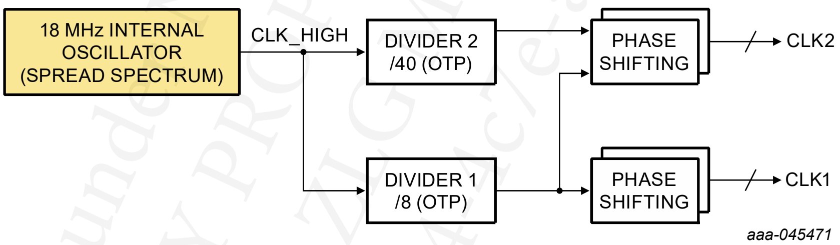

Figure 35. Clock management block diagram

21.1.1 Manual frequency tuning

The internal oscillator frequency runs at 18 MHz by default, and it is configurable via OTP from 16 MHz to 19 MHz with a 1 MHz frequency step. NXP recommends using 18 MHz as a reference value.

Table 172. Manual frequency tuning configuration

CLK_FREQ_OTP[1:0]	High-frequency oscillator	CLK1	CLK2
00	16 MHz	2.000 MHz	400 kHz
01	17 MHz	2.125 MHz	425 kHz
10 (default)	**18 MHz**	**2.250 MHz**	**450 kHz**
11	19 MHz	2.375 MHz	475 kHz

21.1.2 Phase shifting

The clocks of the switching regulators VPRE, VCORE, and VBST can be delayed to keep all the regulators from turning ON at once. This can reduce peak current and improve EMC performance. Each regulator's clock can be shifted from 1 to 3 clock cycles of the high-frequency clock (configurable by OTP).

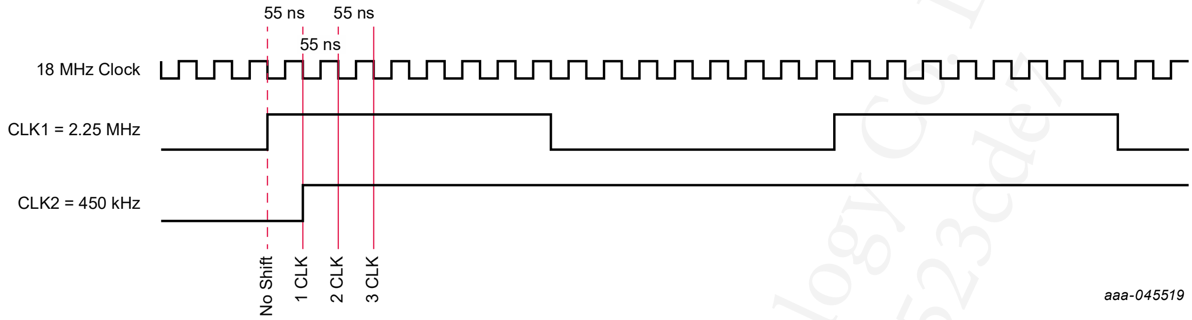

Figure 36. Clock phase shifting examples

21.1.3 Spread spectrum

The internal oscillator can be modulated with a triangular carrier frequency of 23 kHz or 94 kHz, with a ±6 % deviation range around the oscillator frequency. The spread spectrum feature and the carrier frequency can be selected by SPI. The FSS_EN bit enables the spread spectrum feature and the FSS_FMOD bit selects high- or low-frequency modulation. These two bits are in the M_SYS_CFG SPI register. By default, the spread spectrum feature is disabled.

The main purpose of the spread spectrum feature is to improve EMC performance by spreading out the energy of the internal oscillator and VPRE frequency. Because of this, NXP recommends enabling spread spectrum and selecting the 23 kHz carrier frequency as the default for both VPRE switching frequencies.

Table 173. Clock management electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < V_{SUP} < 36 V, V_{PRE_PWM} + V_{PRE_HDR} < V_{SUP_PWR} < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Internal oscillator					
F_{OSC_HIGH}	High-frequency oscillator (OTP programmable)				
	CLK_FREQ_OTP[1:0] = 00	—	16	—	MHz
	CLK_FREQ_OTP[1:0] = 01	—	17	—	MHz
	CLK_FREQ_OTP[1:0] = 10	—	**18**	—	MHz
	CLK_FREQ_OTP[1:0] = 11	—	19	—	MHz
$F_{OSC\_HIGH\_ACC}$	High-frequency oscillator accuracy	-6	—	6	%
F_{OSC_LOW}	Low-frequency oscillator	—	98	—	kHz
$F_{OSC\_LOW\_ACC}$	Low-frequency oscillator accuracy	-5	—	5	%
Spread spectrum					
F_{OSC_MOD}	Spread spectrum frequency modulation for 450 kHz				
	CLK_FREQ_OTP[1:0] = 00 (FSS_FMOD = 0, FSS_EN = 1)	19.5	20.8	22.1	kHz
	CLK_FREQ_OTP[1:0] = 01 (FSS_FMOD = 0, FSS_EN = 1)	20.8	22.1	23.5	kHz
	CLK_FREQ_OTP[1:0] = 10 (FSS_FMOD = 0, FSS_EN = 1)	22.1	23.4	24.9	kHz
	CLK_FREQ_OTP[1:0] = 11 (FSS_FMOD = 0, FSS_EN = 1)	23.3	24.7	26.3	kHz
	Spread spectrum frequency modulation for 2.25 MHz				
	CLK_FREQ_OTP[1:0] = 00 (FSS_FMOD = 1, FSS_EN = 1)	78.4	83.3	88.4	kHz
	CLK_FREQ_OTP[1:0] = 01 (FSS_FMOD = 1, FSS_EN = 1)	83.3	88.5	93.9	kHz
	CLK_FREQ_OTP[1:0] = 10 (FSS_FMOD = 1, FSS_EN = 1)	88.2	93.8	99.4	kHz
	CLK_FREQ_OTP[1:0] = 11 (FSS_FMOD = 1, FSS_EN = 1)	93.1	99	105	kHz

Table 173. Clock management electrical characteristics*...continued*

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < V_{SUP} < 36 V, V_{PRE_PWM} + V_{PRE_HDR} < V_{SUP_PWR} < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
$F_{OSC\_MOD\_RANGE}$	Spread spectrum range (around the nominal frequency)	-6	—	6	%

21.2 Analog multiplexer: AMUX

Various internal and application voltages can be monitored through the AMUX pin. Examples include critical FS26 parameters and system level safety parameters. The channel to be monitored can be selected via the SPI. The maximum AMUX output voltage range is V_{DDIO}.

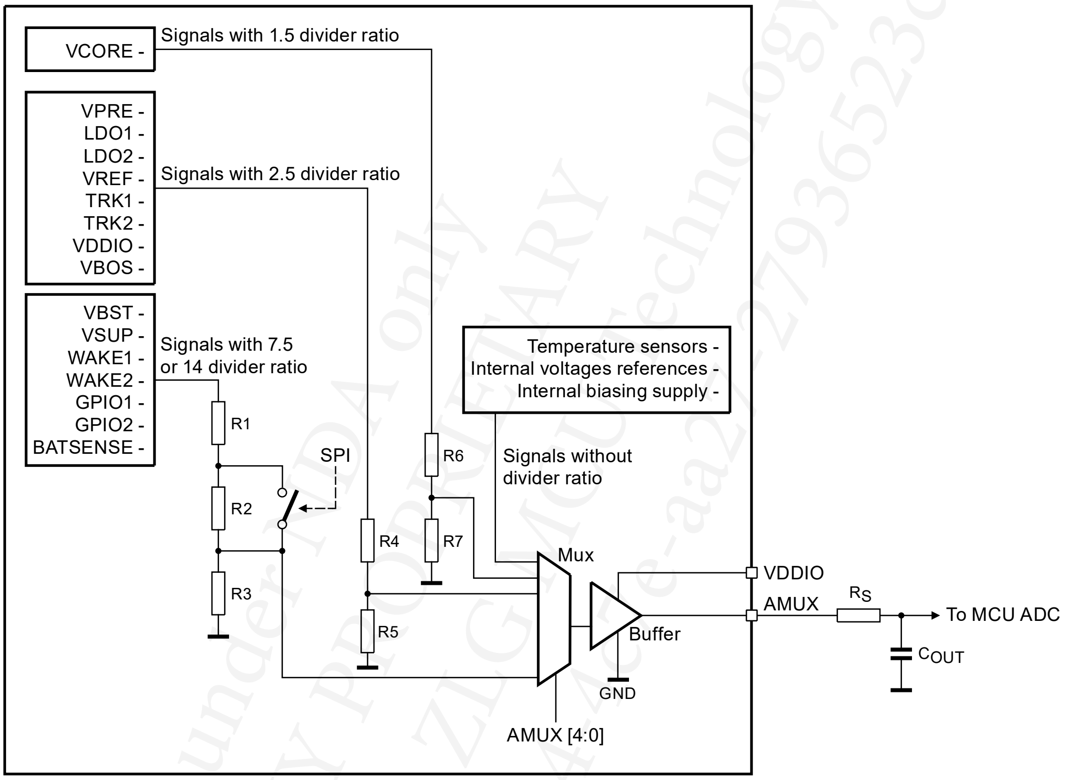

Figure 37. AMUX block diagram

21.2.1 AMUX channel selection

Table 174. AMUX output selection

AMUX_EN	AMUX[4:0]	Signal selection for AMUX output	AMUX_DIV = 0	AMUX_DIV = 1
0	xxxxx	Disabled with AMUX pin pulled to ground	N/A	N/A
1	**00000 (default)**	**Disabled with AMUX pin in Hi-Z**	N/A	N/A
1	00001	Low power bandgap for main domain (1.0 V ± 0.5 %)	1	1
1	00010	Bandgap for main domain (1.0 V ± 0.5 %)	1	1
1	00011	Bandgap for fail-safe domain (1.0 V ± 0.5 %)	1	1
1	00100	Analog voltage supply for main domain (1.6 V ± 50 mV)	1	1

Table 174. AMUX output selection*...continued*

AMUX_EN	AMUX[4:0]	Signal selection for AMUX output	AMUX_DIV = 0	AMUX_DIV = 1
1	00101	Digital voltage supply for main domain (1.6 V ± 50 mV)	1	1
1	00110	Digital voltage supply for fail-safe domain (1.6 V ± 50 mV)	1	1
1	00111	VCORE voltage	1.5	1.5
1	01000	VPRE voltage	2.5	2.5
1	01001	LDO1 voltage	2.5	2.5
1	01010	LDO2 voltage	2.5	2.5
1	01011	VREF voltage	2.5	2.5
1	01100	TRK1 voltage	2.5	2.5
1	01101	TRK2 voltage	2.5	2.5
1	01110	VDDIO voltage	2.5	2.5
1	01111	VBOS internal voltage	2.5	2.5
1	10000	VBST voltage (divider ratio configurable by SPI)	7.5	14
1	10001	VSUP voltage (divider ratio configurable by SPI)	7.5	14
1	10010	WAKE1 voltage (divider ratio configurable by SPI)	7.5	14
1	10011	WAKE2 voltage (divider ratio configurable by SPI)	7.5	14
1	10100	GPIO1 voltage (divider ratio configurable by SPI)	7.5	14
1	10101	GPIO2 voltage (divider ratio configurable by SPI)	7.5	14
1	10110	BATSENSE pin voltage (divider ratio configurable by SPI)	7.5	14
1	10111	Central die temperature sensor.[1]	1	1
1	11000	VCORE temperature sensor.[1]	1	1
1	11001	VPRE temperature sensor.[1]	1	1
1	11010	LDO1 temperature sensor.[1]	1	1
1	11011	LDO2 temperature sensor.[1]	1	1
1	11100	TRK1 temperature sensor.[1]	1	1
1	11101	TRK2 temperature sensor.[1]	1	1
1	11110	GPIO1 temperature sensor.[1]	1	1
1	11111	Reserved	N/A	N/A

[1] Temp (°C) = (V_{AMUX_OUT} – V_{TEMP25}) / V_{TEMP_COEFF} + 25

Table 175. AMUX Electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < V_{SUP} < 36 V, V_{PRE_PWM} + V_{PRE_HDR} < V_{SUP_PWR} < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Electrical characteristics					
V_{AMUX_VDDIO}	VDDIO operating voltage range	3.0	—	5.5	V
V_{AMUX_OUT}	Output voltage range	0.3	—	3.0	V
V_{AMUX_IN}	Input voltage range for VSUP, BATSENSE, VBST, WAKE1, WAKE2, GPIO1, GPIO2 Ratio 7.5 Ratio 14	 2.5 4.2	—	 21 36	V
I_{AMUX}	Output buffer current capability	—	—	1	mA

Table 175. AMUX Electrical characteristics*...continued*

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < V_{SUP} < 36 V, V_{PRE_PWM} + V_{PRE_HDR} < V_{SUP_PWR} < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
V_{AMUX_OFF}	Offset voltage (I_{AMUX} = 1 mA)	-7	—	7	mV
V_{AMUX_RATIO}	Ratio accuracy Ratio 1 Ratio 1.5 Ratio 2.5 Ratio 7.5 Ratio 14	 -0.5 -1.5 -1.5 -1.5 -1.5	 — — — — —	 0.5 1.5 1.5 1.5 1.5	%
R_{AMUX_DIV}	Analog multiplexer total bridge resistance for BATSENSE, VSUP, VBST, WAKE1, WAKE2, GPIO1, GPIO2	0.75	1.5	3	MΩ
R_{AMUX_PD}	Analog multiplexer internal pull-down resistance	5	10	20	kΩ
V_{TEMP25}	Temperature sensor voltage at 25 °C	2.01	2.055	2.1	V
V_{TEMP_COEFF}	Temperature sensor coefficient	-6.25	-5.88	-5.5	mV/°C
T_{AMUX_SET}	Settling time (from 10 % to 90 % of V_{DDIO}, R_S = 220 Ω, C_{OUT} = 10 nF)	—	—	10	µs
External components					
R_S	Nominal output resistor (±10 %)	—	220	—	Ω
C_{OUT}	Nominal[1] output capacitance	2.2	2.2	10	nF
	Effective[2] output capacitance	1.1	—	15	

[1] For all regulators, the nominal value is the value normalized.
[2] For all regulators, the effective capacitor value is the capacitor value after tolerance, DC bias and aging removal.

21.3 System I/O pins

21.3.1 WAKE1 and WAKE2: wake-up inputs

WAKE1 pin and WAKE2 pin are programmable inputs used to detect wake-up events on either high or low levels. Both WAKEx pins are protected up to 40 V and are suitable to connect to a wake-up signal outside the ECU.

For each pin, an internal pull-down can be enabled with WKxPD_OTP and its value chosen with WKxPD_SEL_OTP.

Additionally, the VIL / VIH theresholds V_{IL_WAKEx} / V_{IH_WAKEx} can be chosen with WKxTH_OTP and status is reported on WKx_S.

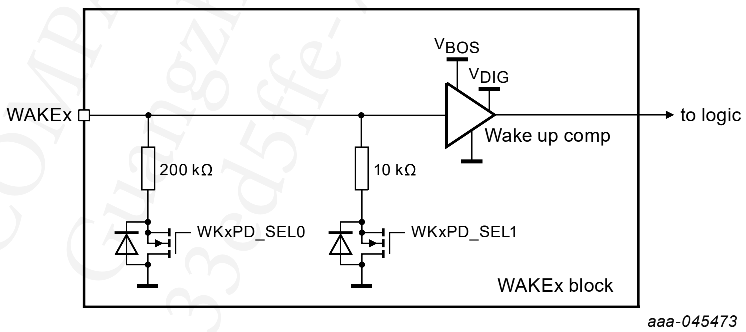

Figure 38. WAKEx pin block diagram

Table 176. Electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < V_{SUP} < 36 V, V_{PRE_PWM} + V_{PRE_HDR} < V_{SUP_PWR} < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Electrical characteristics					
V_{IL_WAKEx}	Low input voltage detection Low voltage detection (WKxTH_OTP = 0) High-voltage detection (WKxTH_OTP = 1)	— —	— —	0.8 0.3 * V_{BOS}	V
V_{IH_WAKEx}	High input voltage detection threshold Low input threshold (WKxTH_OTP = 0) High input threshold (WKxTH_OTP = 1)	2 0.7 * V_{BOS}	— —	— —	V
V_{IN_HYS}	Threshold hysteresis	50	120	500	mV
I_{IN_WAKE}	Input current on WAKEx pins (No pull-down resistor, wake-up enabled)	—	5	10	µA
t_{WAKE}	Wake-up filtering time	50	70	100	µs
R_{PD_WAKE}	Pull-down resistor on WAKE1 and WAKE2 pins WKxPD_SEL_OTP = 0 WKxPD_SEL_OTP = 1	100 5	200 10	320 15	kΩ

21.3.2 GPIO1 and GPIO2: general purpose input/output

GPIO1 pin and GPIO2 pin are general purpose input/output. They can be configured to operate as wake-up inputs, as high-side drivers with up to 20 mA capability, or as low-side drivers with up to 2 mA capability, for use within the ECU. GPIOx configuration can be selected with the GPIOxSTAGE_OTP[1:0] bits.

GPIO1 and GPIO2 low-side drivers can be configured to be either active high or active low with the GPIOx_MODE_OTP bit. Active Low mode can be used to directly drive a PMOS gate without inverting the command.

A thermal shutdown protection is implemented on GPIO1. When a thermal shutdown is triggered, GPIO1 is automatically disabled and will remain disabled until the TSD is present (GPIO1TSD_I = 1). When the TSD is gone (GPIO1TSD_I = 0), a SPI command is mandatory to re-enable GPIO1.

Table 177. GPIO mode configuration

GPIOxSTAGE_OTP[1:0]		GPIOx_MODE_OTP		GPIO Configuration
0	Input configuration	x	—	Output disabled
1	Low-side driver	0	Active High mode	Low-side driver (Active High)
		1	Active Low mode	Low-side driver (Active Low)
2	High-side driver	x	—	High-side driver (Active High)
3	Push-pull	x	—	Push-pull (Active High)

An internal pull-up or pull-down can be enabled by OTP for each GPIO, depending on the GPIOxSTAGE_OTP[1:0] configuration.. The pull-up resistor is always connected to V_{DDIO}.

GPIO1 can be configured to keep its state in *LPOFF mode* or in *standby mode* with GPIO1LP_ON SPI bit. GPIO2 can be configured to keep its state in *standby mode* with the GPIO2LP_ON bit.

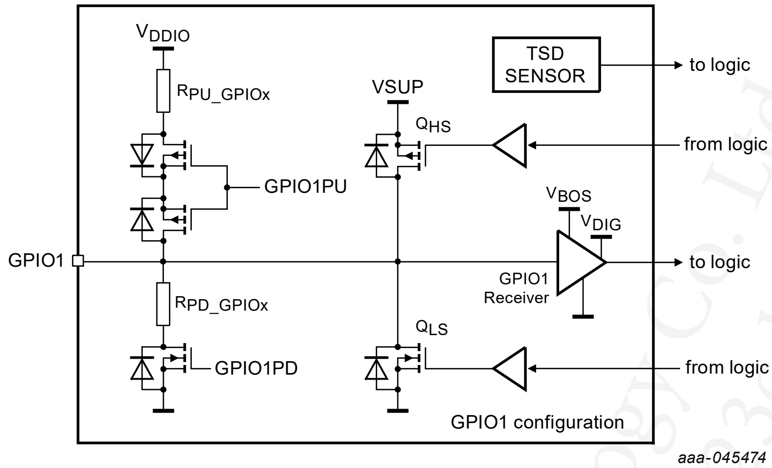

Figure 39. GPIO1 block diagram

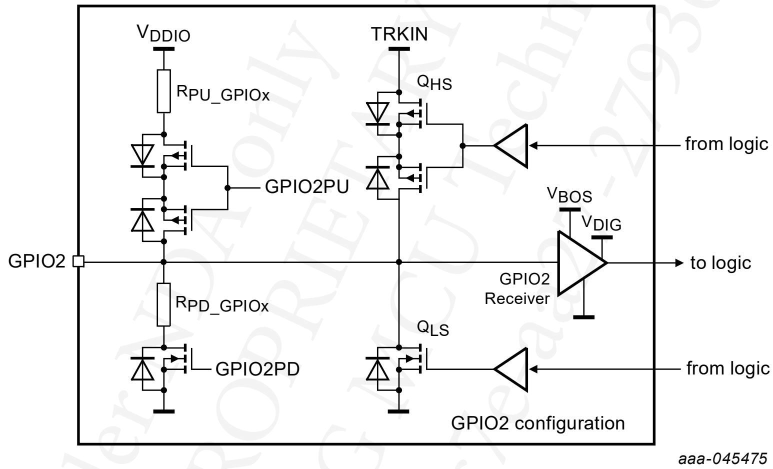

Figure 40. GPIO2 block diagram

21.3.2.1 GPIO input configuration

When GPIOx is set as input configuration, the pin is set to Hi-Z or Low depending on the GPIOxPD_OTP bit. The internal pull-up is disabled regardless of the GPIOxPD_OTP bit.

GPIOx pins are protected up to 40 V, and are suitable to connect a wake-up signal outside the ECU.

When a GPIO is used as a global input pin, an RC protection network is required to protect the input. When a GPIO is used as local input pin, a capacitor is required for immunity. Each GPIO voltage can be sensed through the analog multiplexer.

21.3.2.2 GPIO active high mode

When GPIOx is set as active high, as soon as the OTP is loaded, the pin is set to Hi-Z or Low, depending on the GPIOxPD_OTP bit. If the GPIOx is assigned to a slot in the power-up sequence, the pin remains Hi-Z or Low until it reaches the selected slot. Once the selected slot is reached, the GPIOx is asserted high.

In *normal mode*, the internal pull-down resistor is disabled regardless of the GPIOxPD_OTP bit when the GPIOx is set as low-side driver.

If the internal pull-down is enabled by OTP, the resistor remains enabled in Low Power modes to avoid floating nodes. The internal pull-up resistor should be disabled if the GPIOx is used as a high-side or push-pull driver. Table 178 describes the GPIOx behavior based on the OTP configuration.

Table 178. GPIO Active High mode behavior summary

Configuration	GPIOx PU_OTP	GPIOx PD_OTP	Default state after OTP loaded			*Normal mode*			*Standby mode* GPIOxLP_ON = 0			*LPOFF mode / Deep Fail Safe* GPIOxLP_ON = 0		
			PIN	HS	LS	PIN	HS	LS	PIN	HS	LS	PIN	HS	LS
Low-side driver	0	0	Low	OFF	ON	Hi-Z	OFF	OFF	Hi-Z	OFF	OFF	Hi-Z	OFF	OFF
	1	0	Low	OFF	ON	High	OFF	OFF	Hi-Z	OFF	OFF	Hi-Z	OFF	OFF
	0	1	Low	OFF	ON	Hi-Z	OFF	OFF	Low	OFF	OFF	Low	OFF	OFF
	1	1	Low	OFF	ON	High	OFF	OFF	Low	OFF	OFF	Low	OFF	OFF
High-side driver	-	0	Hi-Z	OFF	OFF	High	ON	OFF	Hi-Z	OFF	OFF	Hi-Z	OFF	OFF
	-	1	Low	OFF	OFF	High	ON	OFF	Low	OFF	OFF	Low	OFF	OFF
Push-pull driver	-	0	Low	OFF	ON	High	ON	OFF	Hi-Z	OFF	OFF	Hi-Z	OFF	OFF
	-	1	Low	OFF	ON	High	ON	OFF	Low	OFF	OFF	Low	OFF	OFF

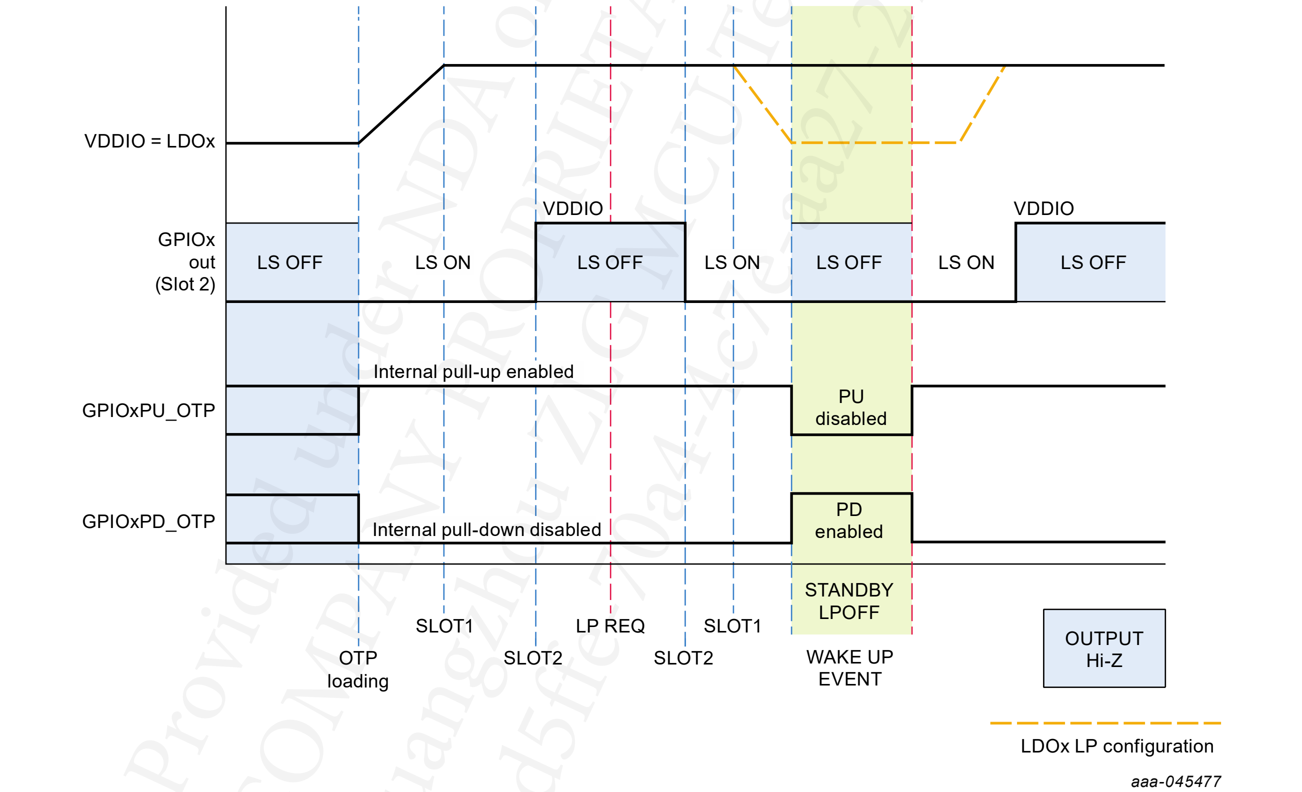

Figure 41. GPIO low-side active high operation. GPIOx_MODE_OTP = 0

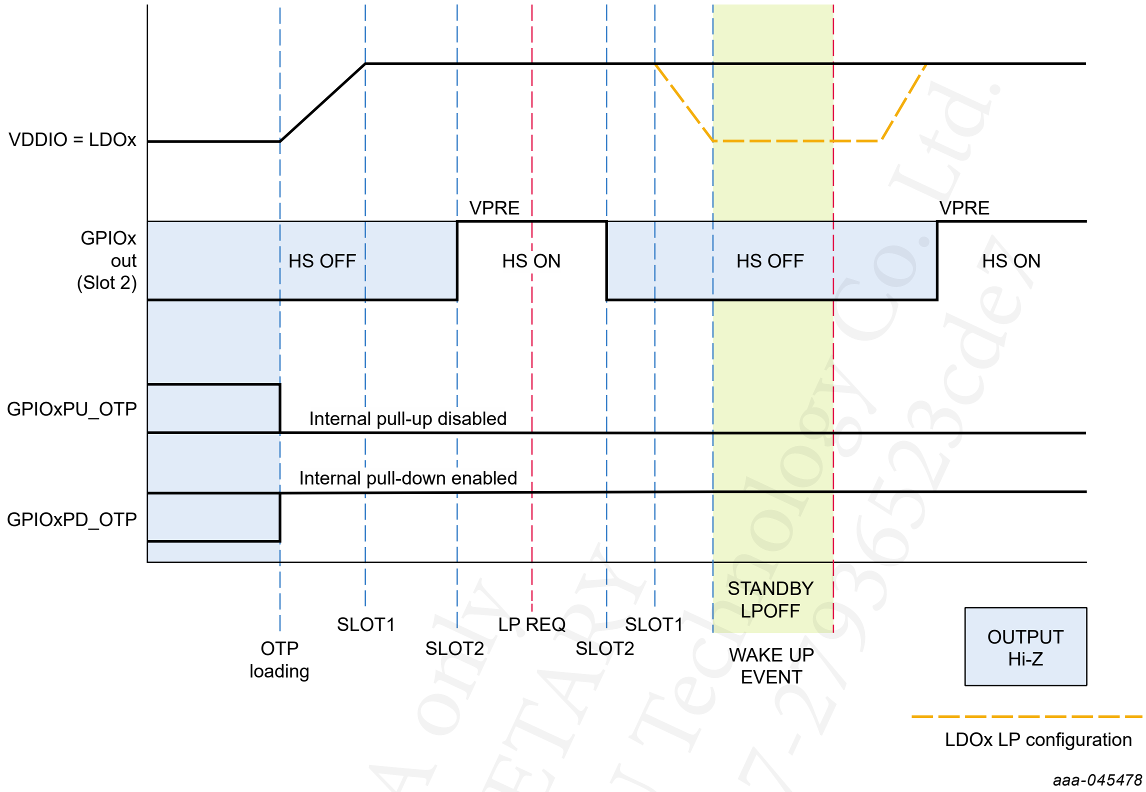

Figure 42. GPIO High-side Active High operation. GPIOx_MODE_OTP = 0

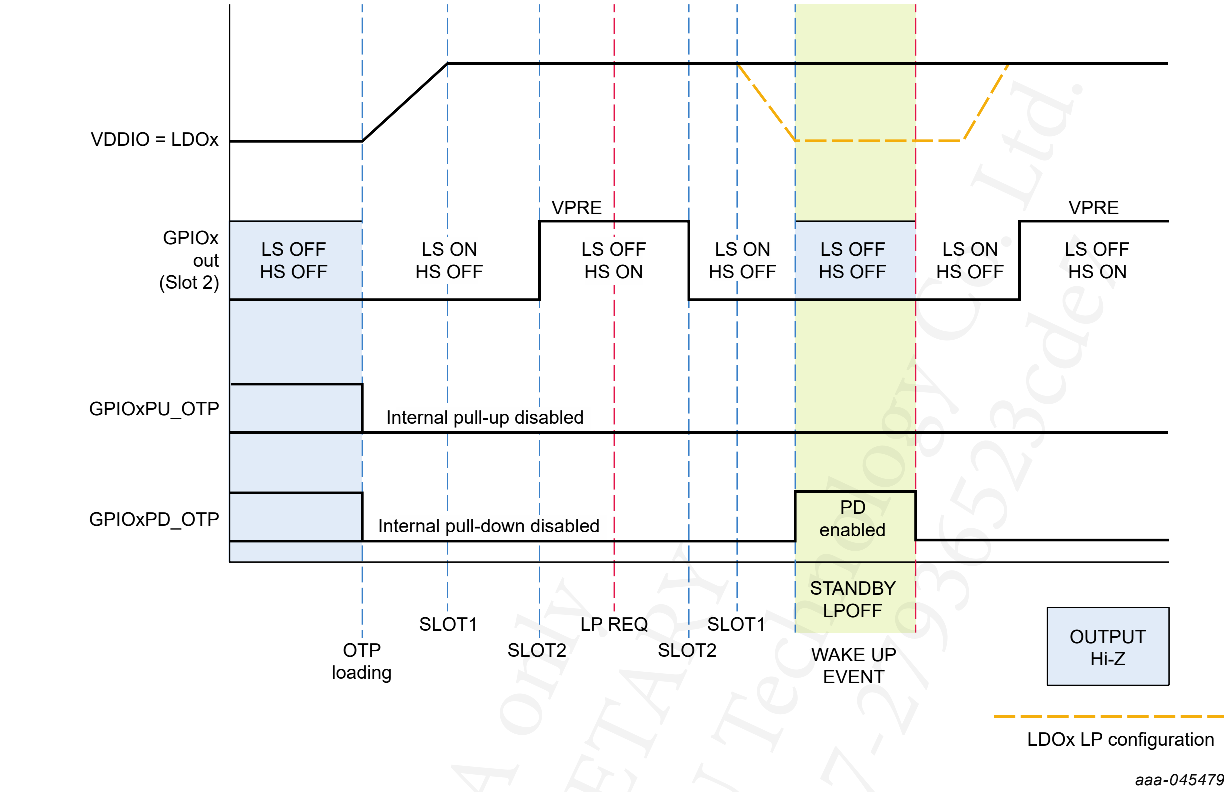

Figure 43. GPIO Push-pull Active High operation. GPIOx_MODE_OTP = 0

21.3.2.3 GPIO active low mode

The active low mode is available only when the GPIOx is configured as a low-side driver.

When GPIOx is set as Active Low, as soon as the OTP is loaded, the pin is set to Hi-Z or High, depending on the GPIOxPU_OTP bit. If the GPIOx is assigned to a slot in the power-up sequence, the pin remains High or Hi-Z until it reaches the selected slot. Once the selected slot is reached, the GPIOx low-side driver is asserted low.

In *normal mode*, the internal pull-down resistor is disabled regardless of the GPIOxPD_OTP bit when the GPIOx is set as low-side driver. If the internal pull-down is enabled by OTP, the resistor remains enabled in Low Power modes, except in *standby mode*, to avoid floating nodes.

Table 179. GPIO Active Low mode behavior summary

Configuration	GPIOx PU_OTP	GPIOx PD_OTP	Default state after OTP loaded			*Normal mode*			*Standby mode* GPIOxLP_ON = 0			*LPOFF mode / Deep Fail Safe* GPIOxLP_ON = 0		
			PIN	HS	LS	PIN	HS	LS	PIN	HS	LS	PIN	HS	LS
Low-side driver	0	0	Hi-Z	OFF	OFF	Low	OFF	ON	Hi-Z	OFF	OFF	Hi-Z	OFF	OFF
	1	0	High	OFF	OFF	Low	OFF	ON	High	OFF	OFF	Hi-Z	OFF	OFF
	0	1	Hi-Z	OFF	OFF	Low	OFF	ON	Hi-Z	OFF	OFF	Low	OFF	OFF
	1	1	High	OFF	OFF	Low	OFF	ON	High	OFF	OFF	Low	OFF	OFF

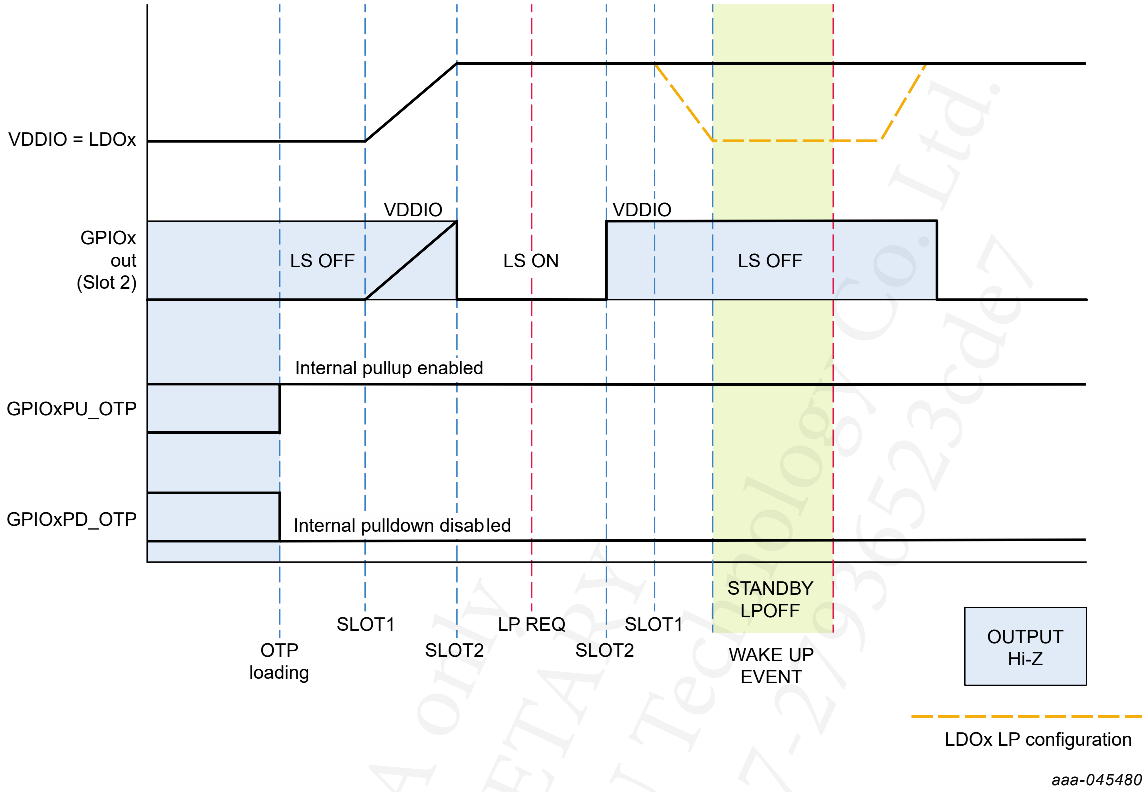

Figure 44. GPIO low-side driver Active Low operation. GPIOx_MODE_OTP = 1

21.3.2.4 VCORE_PGOOD: VMON_CORE power good status

GPIO2 can be used to generate a power good signal from VMON_CORE monitoring to drive an external N-type MOSFET to be able to start with a pre-biased voltage for a non-NXP MCU.

NXP recommends using an external load switch between FS2630 VCORE and the MCU input supply. The VCORE power good feature can be enabled by OTP using the GPIO2_VCORE_PGOOD_OTP bit.

When GPIO2 is used as VCORE_PGOOD, the HS switch (connected internally to VPRE) is used to close the external N-type MOSFET. The power good signal is released as soon as VMON_CORE crosses its undervoltage threshold. VCORE_PGOOD is asserted low when VCORE is disabled, or when an error is reported from VMON_CORE voltage monitoring (undervoltage or overvoltage). Therefore, VCORE_PGOOD will be asserted low when entering Low power mode setting CORE_UV flag, as soon as the Fail-safe state machine disables VMON_CORE voltage monitoring block, despite VCORE still up and running.

An external pull-down is mandatory to assert the pin low when the high-side switch is turned off.

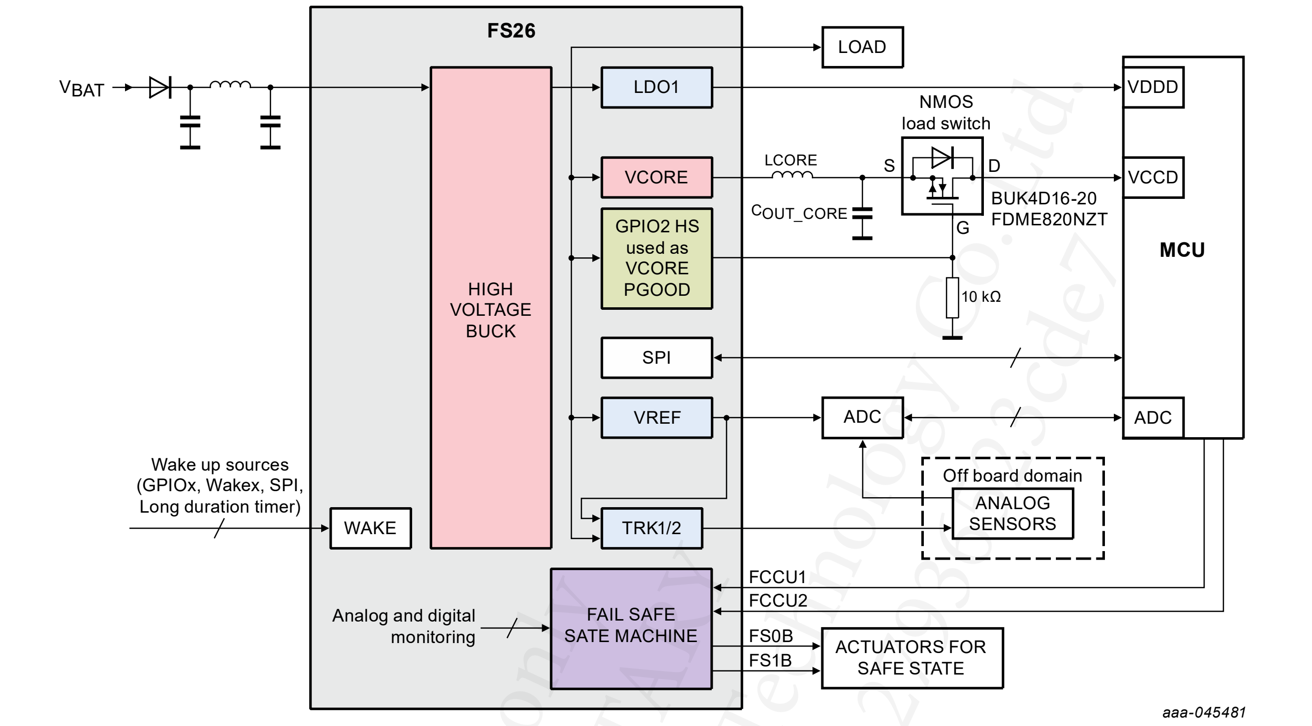

Figure 45. VCORE PGOOD load switch

21.3.2.5 GPIO electrical characteristics

Table 180. GPIO electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. $V_{SUP\_UVH} < V_{SUP} <$ 36 V, $V_{PRE\_PWM} + V_{PRE\_HDR} < V_{SUP\_PWR} <$ 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Electrical characteristics					
V_{IL_GPIOx}	Low input voltage detection Low voltage detection (GPIOxTH_OTP = 0) High-voltage detection (GPIOxTH_OTP = 1)	— —	— —	0.8 0.3 * V_{BOS}	V
V_{IH_GPIOx}	High input voltage detection threshold Low input threshold (GPIOxTH_OTP = 0) High input threshold (GPIOxTH_OTP = 1)	2 0.7 * V_{BOS}	— —	— —	V
V_{IN_HYS}	Threshold hysteresis	50	120	500	mV
I_{IN_GPIO}	Input current on GPIOx pins (LS OFF, HS OFF, No pull-down resistor, wake-up enabled)	—	5	10	µA
t_{WAKE}	Wake-up filtering time	50	70	100	µs
I_{HS_GPIOx}	High-side drive current capability	—	—	20	mA
I_{HS_ILIM}	High-side current limitation threshold	25	50	75	mA
I_{LS_GPIOx}	Low-side drive current capability	—	—	2	mA
I_{LS_ILIM}	Low-side current limitation threshold	3	5	7.5	mA
I_{LEAK_GPIOx}	Input current leakage HS and LS disabled, PU and PD disabled	—	—	10	µA
R_{PU_GPIOx}	Internal pull-up resistor value	100	200	320	kΩ
R_{PD_GPIOx}	Internal pull-down resistor value	100	200	320	kΩ

Table 180. GPIO electrical characteristics*...continued*

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < V_{SUP} < 36 V, V_{PRE_PWM} + V_{PRE_HDR} < V_{SUP_PWR} < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
V_{DROP_GPIO}	Drop voltage I = 20 mA high-side source I = 2 mA low-side sink	 — —	 0.2 0.2	 0.6 0.4	V
TSD_{GPIO1}	Thermal shutdown threshold for GPIO1	175	—	—	°C
TSD_{GPIO1_HYS}	Thermal shutdown threshold hysteresis for GPIO1	5	—	12	°C

21.3.3 INTB: interrupt output

INTB is an open drain output pin with an internal pull-up to VDDIO. When an internal interrupt occurs, this pin generates a pulse to inform the microcontroller.

Main interrupts, listed in Table 181, generate a pulse on INTB, if the flag is cleared, and fail-safe interrupts, listed in Table 182, generate a pulse on INTB even if the flag is already set. Each interrupt can be masked by setting the corresponding inhibit interrupt bit in the M_xxx_MASK and FS_INTB_MASK registers.

When the RSTB pin is asserted, interrupts are no longer sent to the MCU until the product goes back to the *initialization phase*.

Table 181 and Table 182 list all interrupt sources that can generate a pulse on the INTB pin.

Table 181. List of Interrupt sources from Main logic

SPI flag	Interrupt mask	Interrupt flag	Corresponding event description
TSD_G	TWARN_M	TWARN_I	Central Temp sensor has crossed the thermal warning threshold on the rising edge
	GPIO1TSD_M	GPIO1TSD_I	GPIO1 thermal shutdown event occurred
	VPRETSD_M	VPRETSD_I	VPRE thermal shutdown event occurred
	TRK2TSD_M	TRK2TSD_I	TRK2 thermal shutdown event occurred
	TRK1TSD_M	TRK1TSD_I	TRK1 thermal shutdown event occurred
	CORETSD_M	CORETSD_I	VCORE thermal shutdown event occurred
	LDO2TSD_M	LDO2TSD_I	LDO2 thermal shutdown event occurred
	LDO1TSD_M	LDO1TSD_I	LDO1 thermal shutdown event occurred
REG_G	VBSTOV_M	VBSTOV_I	V_{BST} has crossed $V_{BST\_OV\_TH}$ on the rising edge
	VPREUVH_M	VPREUVH_I	V_{PRE} has crossed V_{PRE_UVH} on the falling edge
	VBSTOC_M	VBSTOC_I	VBST overcurrent event occurred
	VPREOC_M	VPREOC_I	VPRE overcurrent event occurred
	TRK2OC_M	TRK2OC_I	TRK2 overcurrent event occurred
	TRK1OC_M	TRK1OC_I	TRK1 overcurrent event occurred
	COREOC_M	COREOC_I	VCORE overcurrent event occurred
	LDO2OC_M	LDO2OC_I	LDO2 overcurrent event occurred
	LDO1OC_M	LDO1OC_I	LDO1 overcurrent event occurred
VSUP_G	VBOSUVH_M	VBOSUVH_I	V_{BOS} has crossed V_{BOS_UVH} on the falling edge
	VSUPOV_M	VSUPOV_I	V_{SUP} has crossed V_{SUP_OV} on the rising edge
	VSUPUV6_M	VSUPUV6_I	V_{SUP} has crossed V_{SUP_UV6} on the falling edge
	VSUPUVH_M	VSUPUVH_I	V_{SUP} has crossed V_{SUP_UVH} on the falling edge

Table 181. List of Interrupt sources from Main logic...*continued*

SPI flag	Interrupt mask	Interrupt flag	Corresponding event description
WIO_G	LDT_M	LDT_I	LDT event occurred (Function 1 only)
	GPIO2_M	GPIO2_I	GPIO2 event occurred
	GPIO1_M	GPIO1_I	GPIO1 event occurred
	WK2_M	WK2_I	WAKE2 event occurred
	WK1_M	WK1_I	WAKE1 event occurred
	—	WUEVENT[3:0]	Wake-up event occurred
COM_G	MSPI_CRC_M	MSPI_CRC_I	Main SPI CRC calculation is incorrect
	MSPI_CLK_M	MSPI_CLK_I	Main SPI clock provided wrong number of clock pulses
	MSPI_REQ_M	MSPI_REQ_I	MCU writes to an invalid register in the Main domain
—	—	—	Main state machine entered in *normal mode*

Table 182. List of Interrupt sources from the fail-safe domain

SPI flag	Interrupt global flag	Interrupt mask	Interrupt flag	Corresponding event description
FS_G	FS_REG_ OVUV_G	VPRE_M	VPRE_OV	An overvoltage event occurred on VMON_PRE monitoring
			VPRE_UV	An undervoltage event occurred on VMON_PRE monitoring
		CORE_M	CORE_OV	An overvoltage event occurred on VMON_CORE monitoring
			CORE_UV	An undervoltage event occurred on VMON_CORE monitoring
		LDO1_M	LDO1_OV	An overvoltage event occurred on VMON_LDO1 monitoring
			LDO1_UV	An undervoltage event occurred on VMON_LDO1 monitoring
		LDO2_M	LDO2_OV	An overvoltage event occurred on VMON_LDO2 monitoring
			LDO2_UV	An undervoltage event occurred on VMON_LDO2 monitoring
		TRK1_M	TRK1_OV	An overvoltage event occurred on VMON_TRK1 monitoring
			TRK1_UV	An undervoltage event occurred on VMON_TRK1 monitoring
		TRK2_M	TRK2_OV	An overvoltage event occurred on VMON_TRK2 monitoring
			TRK2_UV	An undervoltage event occurred on VMON_TRK2 monitoring
		REF_M	REF_OV	An overvoltage event occurred on VMON_REF monitoring
			REF_UV	An undervoltage event occurred on VMON_REF monitoring
		EXT_M	EXT_OV	An overvoltage event occurred on VMON_EXT monitoring
			EXT_UV	An undervoltage event occurred on VMON_EXT monitoring
	—	FCCU1_M / FCCU2_M	FCCU12	An event occurred on FCCU1 monitoring
		FCCU1_M	FCCU1 bit	An event occurred on FCCU1 monitoring
		FCCU2_M	FCCU2 bit	An event occurred on FCCU2 monitoring
		ERRMON_M	ERRMON bit	An event occurred on external IC monitoring
FS_G / COM_G	FS_WD_G	BAD_WD_M	BAD_WD_DATA	A bad watchdog data refresh occurred
			BAD_WD_TIMING	A bad watchdog timing refresh occurred
—	—	—	—	Fail-safe state machine entered in *initialization phase*

Table 183. INTB Electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. $V_{SUP\_UVH} < V_{SUP} < 36$ V, $V_{PRE\_PWM} + V_{PRE\_HDR} < V_{SUP\_PWR} < 36$ V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Electrical characteristics					
R_{INTB_PU}	Internal pull-up resistor to V_{DDIO}	5	10	20	kΩ
V_{INTB_VOL}	Low output level threshold I_{INTB} = 2.0 mA	—	—	0.4	V
I_{NTB_LEAK}	Input leakage current V_{DDIO} = 5.5 V	—	—	1.0	µA
I_{INTB_ILIM}	INTB current limitation	4	—	20	mA
t_{INTB_PULSE}	Interrupt pulse duration Short pulse (INT_PWIDTH = 0) Long pulse (INT_PWIDTH = 1)	 17.5 70	 25 100	 32.5 130	µs

21.4 LDT: long duration timer

The FS2630 features a long duration timer (LDT) with an integrated oscillator. The timer is configurable by the SPI and can operate in *normal mode* and in Low Power modes. It provides several functions and offers a wide range of configurable counting periods, as well as a calibration mechanism for internal oscillator compensation.

The timer is not part of the safety circuitry and is not covered by LBIST (logic built-in self-test). It can be activated in *normal mode*, though, and all prescaler options can be selected to allow timer circuitry verification. The timer is based on a 24 bit counter, with a 32768 Hz oscillator, allowing a 1.0 second time base.

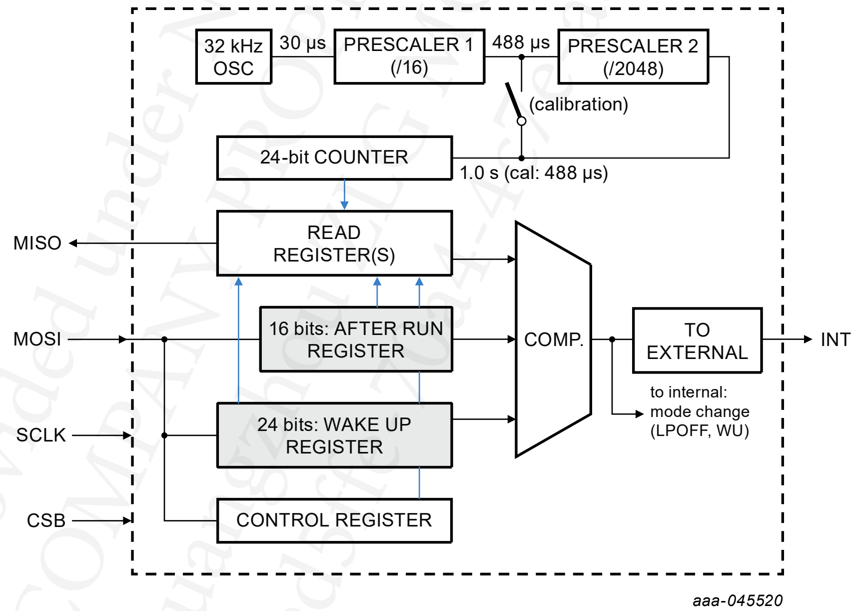

Figure 46. Long Duration Timer block diagram

21.4.1 Timer characteristics

In *normal mode* operation, the timer can count up to 194 days, with a 1 second resolution. In Calibration mode, the prescaler 2 is bypassed and the timer can count up to 2.28 hours, with a 488 µs resolution.

Table 184. Long Duration Timer characteristics

	Oscillator frequency	Oscillator period	Prescaler	Counter resolution	Max count	
Operation	32.768 kHz	30.52 µs	16 x 2048	1 s	4660 hours	194 days
Calibration	32.768 kHz	30.52 µs	16	488 µs	8192 s	2.28 hours

The LDT has two modes of operation, based on the prescaler used during the count:

- When LDT_MODE = 0, the LDT is set in Long Count mode.
- When LDT_MODE = 1, the LDT is set in Short Count mode.

The LDT_AFTER_RUN[15:0] bits is used to set or to read the after run target value in *normal mode*.

The LDT_WUP_H[7:0] and the LDT_WUP_L[15:0] bits is used to set or to read the wake-up target value, in combination with the LDT_SEL bit:

- LDT_WUP_H[7:0] contains the 8 most significant bits of the wake-up target value.
- LDT_WUP_L[15:0] contains the 16 least significant bits of the wake-up target value.

The LDT_SEL bit allows the MCU to either set/read the wake-up target value or to read the current value of the 24 bit LDT counter in the LDT_WUP_H[7:0] and the LDT_WUP_L[15:0] bits.

- When LDT_SEL = 0, the MCU can read or write the wake-up target value in the LDT_WUP_H[7:0] and the LDT_WUP_L[15:0] bits.
- When LDT_SEL = 1, the MCU can read the counter current value (running or not).

The LDT_EN bit is provided to start the LDT timer operation:

- When LDT_EN = 0, the LDT is disabled.
- When LDT_EN = 1, the LDT starts counting as defined in the M_LDT_CTRL and M_LDT_CFGx registers.

The LDT_LPSEL[7:0] bits indicate the appropriate Low Power mode. The LDT_LPSEL[7:0] bits reset to 0 every time the device enters the *normal mode*. When timer function 2 or 3 is selected, the MCU must first write the safe key value on the LDT_LPSEL[7:0] bits to confirm that the device will go into the corresponding Low Power mode after the run timer has expired.

- When LDT_LPSEL[7:0] = AAh, the device goes into *standby mode* after the run timer expires.
- When LDT_LPSEL[7:0] = A5h, the device goes into *LPOFF mode* after the run timer expires.
- When timer function 4 or 5 is selected and LDT_EN = 1, the LDT does not start any count until the device enters the corresponding Low Power mode.

21.4.2 Calibration procedure

The calibration procedure consists of activating the counter for a specific duration and comparing the result with the MCU's accurate clock and timing. Once the timer expires, the MCU reads back its final value to compare with its own accurate time of activation and to calculate a time offset.

NXP recommends performing the calibration between -20 °C and 85 °C. Calibration example:

- Select the timer function 1 and set the after run value to 65535 (~32 s).
- Start the counter.
- Read the counter when the MCU RTC reaches 20 s (must be less than 30 s with ±5.0 % oscillator accuracy).
- If the oscillator period is at exact typical value (absolutely no deviation error), expected reading is 40960.
- The exact reading calculates the error correction factor ECF = exact_reading/expected_reading.
- ECF < 1 if the oscillator is faster than the exact typical value.
- ECF > 1 if the oscillator is slower than the exact typical value.
- After calibration, the new after run or wake-up values to set the counter are "after run x ECF" and "wake-up x ECF".

21.4.3 Timer functions

Table 185. Long Duration Timer functions

LDT_FNCT[2:0]	Long Duration Timer Function
0	**Function 1:** In *normal mode*, count and generate a flag or an interrupt when the counter reaches the after run value.
1	**Function 2:** In *normal mode*, count until the counter reaches the after run value and enters Low Power mode.
2	**Function 3:** In *normal mode*, count until the counter reaches the after run value and enters low power mode. Once in Low Power mode, count until the counter reaches the wake-up value or until another wake-up event occurs, and wakes up.
3	**Function 4:** In Low Power mode, count until the counter reaches the wake-up value or until another wake-up event occurs, and wakes up.
4	**Function 5:** In Low Power mode, count and do not wake up unless the counter overflow occurs or if the device wakes up by another wake-up input source.

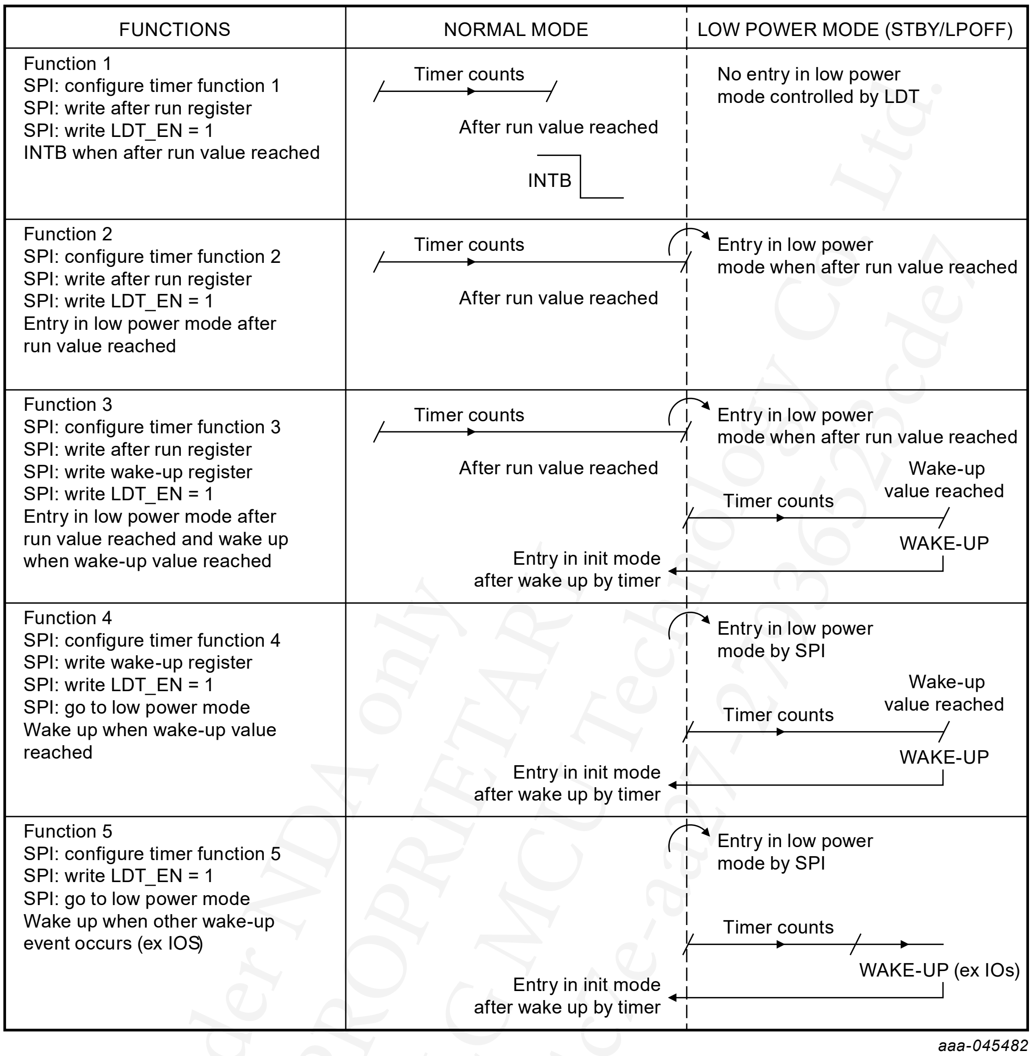

Figure 47. Long Duration Timer functions

21.4.4 Timer operation

The timer is configured and operates with the M_LDT_CFG1, M_LDT_CFG2, M_LDT_CFG3 and M_LDT_CTRL registers.

The 16-bit after-run value is configured and read with M_LDT_CFG1 register and the 24-bit wake-up value is configured and read in the corresponding M_LDT_CFG2 and M_LDT_CFG3 registers.

Figure 48 describes the independent state machine for the long duration timer (LDT). After a POR_M of the device, the LDT is in idle mode waiting for configuration. The after-run timer function starts when the LDT_EN bit is set by SPI. The wake-up timer function starts when the device enters Low Power mode.

- When function 1 is selected and the counter is launched, once the after run value is reached (EOT: End of timer) an interrupt is generated and the counter is stopped. In order to reset the counter, it must be disabled (LDT_EN = 0) before it is enabled again (LDT_EN = 1).
- When function 2 is selected and the counter is launched, once the after run value is reached (EOT) the device goes to Low Power mode and the counter is stopped. In order to reset the counter, it must be disabled (LDT_EN = 0) before it is enabled again (LDT_EN = 1).

- When function 3 is selected and the counter is launched, once the after run value is reached (EOT) the device goes to Low Power mode. The counter is reset and restarts. When the counter reaches the wake-up value (EOT), the device wakes up and the counter is stopped. If the device is awakened by another wake-up source, the counter is stopped. In order to reset the counter, it must be disabled (LDT_EN = 0) before enabling it again (LDT_EN = 1).
- When function 4 is selected and the counter is launched, once the wake-up value is reached (EOT) the device wakes up and the counter is stopped. If the device is awakened by another wake-up source, the counter is stopped. In order to reset the counter, it must be disabled (LDT_EN = 0) before it is enabled again (LDT_EN = 1).
- When function 5 is selected and the counter overflows (OVRFLW), the device wakes up and the counter is stopped. The counter must be disabled (LDT_EN = 0) before reading its value and enabled again. Overflow means that the counter maximum value is reached (all 24 bits at logic 1).
- When function 5 is selected and the devices is awakened by a GPIO, the counter is still running. In order to reset the counter, it must be disabled (LDT_EN = 0) before it is enabled again (LDT_EN = 1).

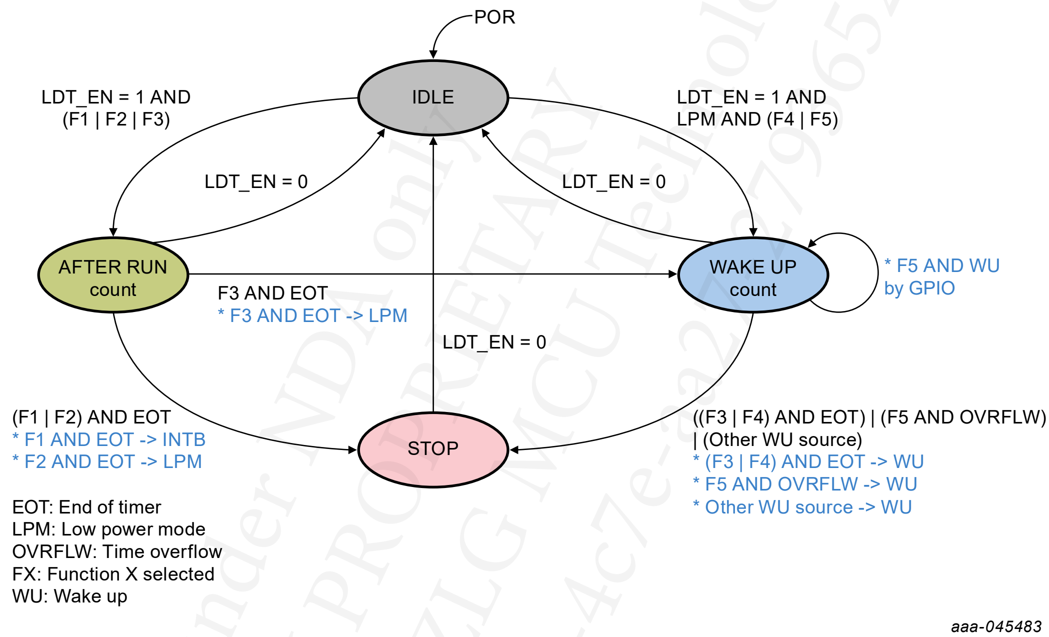

Figure 48. Long Duration Timer state machine

Table 186. Long Duration Timer characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < V_{SUP} < 36 V, V_{PRE_PWM} + V_{PRE_HDR} < V_{SUP_PWR} < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Electrical characteristics					
T_{BASE_LDT}	Long Duration Timer time base LDT_MODE = 0 LDT_MODE = 1	 — —	 1 488	 — —	 s µs
I_{Q_LDT}	Long Duration Timer quiescent current consumption	—	1	2	µA
LDT_{ACC1}	Long Duration Timer accuracy without calibration	-5	—	5	%
LDT_{ACC2}	Long Duration Timer accuracy with calibration Including 1 month aging Including temperature drift 0 °C < T_A < 80 °C	-2	—	2	%

22 Functional safety

22.1 General description

The FS26 provides capabilities to enable functional safety in the application, in addition to power management and system enhancement functions. This part of the integrated circuit has its own biasing and clocking circuitries.

This creates an appropriate level of independence between the FS26 main functions and its safety mechanisms. FS26 is compliant with Automotive Safety Integrity Levels (ASIL) B and D, depending on the device part number.

This functional safety block provides three main capability sets: voltage monitoring of power management circuitry, software and hardware monitoring of the microcontroller, and control signals to place the system in a safe state in case of error.

Figure 49 illustrates functional blocks that pertain to functional safety.

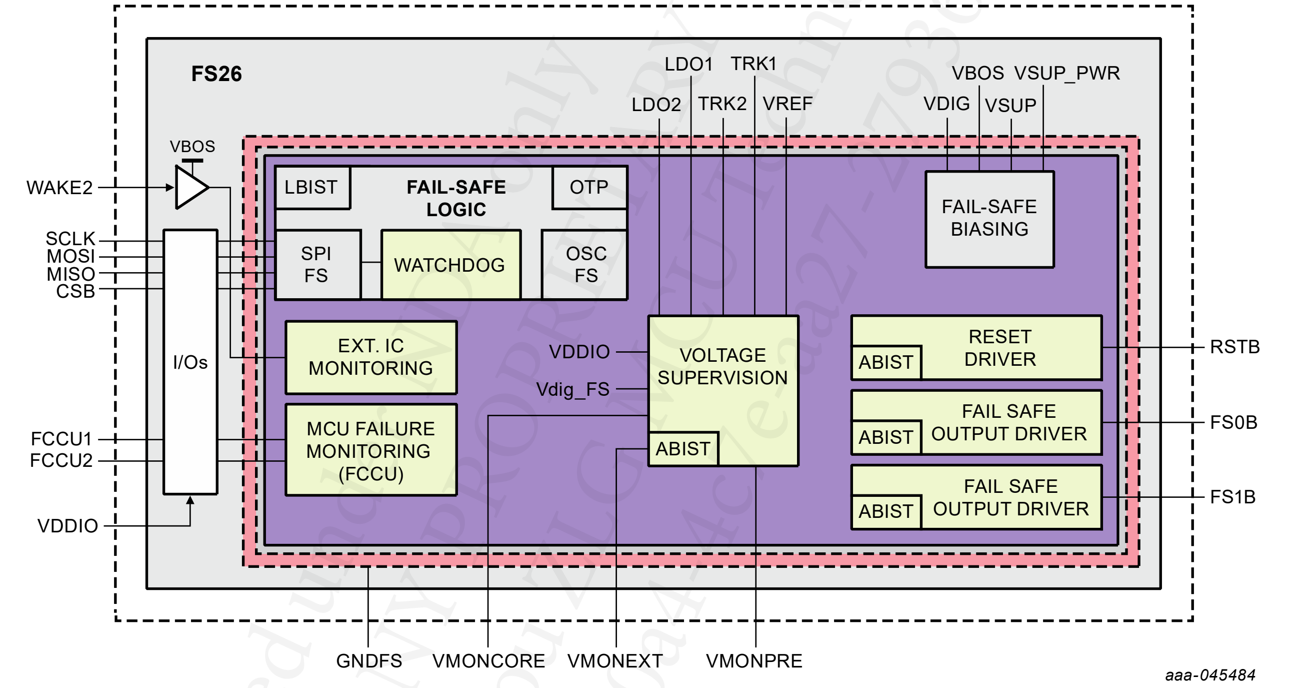

Figure 49. Fail-safe block diagram

22.2 Fail-safe logic

The dedicated fail-safe logic consists of OTP data to store the desired configuration, dedicated SPI registers, the watchdog mechanism, and an independent state machine.

22.3 ASIL B versus ASIL D

Table 187 lists the primary differences between the ASIL B and ASIL D versions of the FS2630.

Table 187. ASIL B vs. ASIL D safety features

Safety Features	ASIL B (FS26xyB)	ASIL D (FS26xyD)
RSTB output pin	Yes	Yes
FS0B output pin	Yes	Yes
FS1B output pin	Optional	Optional
VMON_PRE voltage monitoring	Yes	Yes
VMON_CORE voltage monitoring	Yes	Yes
VMON_LDO1 voltage monitoring	Yes	Yes
VMON_LDO2 voltage monitoring	Yes	Yes
VMON_TRK1 voltage monitoring	Yes	Yes – C(D)
VMON_TRK2 voltage monitoring	Yes	Yes – C(D)
VMON_REF voltage monitoring	Yes	Yes
VMON_EXT voltage monitoring	Yes	Yes
Watchdog monitoring	Simple watchdog	Challenger watchdog
FCCU monitoring	Optional	Yes
MCU fault recovery strategy	No	Yes
External IC monitoring (ERRMON)	Optional	Optional
Analog BIST (ABIST)	Yes	Yes
Logical BIST (LBIST)	No	Yes

22.4 Fail-safe initialization phase

Initialization phase is the period where device stays in the fail-safe state called ***Safety Initialization Phase***. All the safety reactions are set and can only be set during this period for safety porpuses, that is, avoid unintended changes on safety reaction configuration.

After a POR_FS, a wake-up from Low Power mode, of RSTB pulse, when the RSTB pin is released, device enters the initialization phase. An interrupt pulse is automatically generated.

To secure the writing process during the initialization phase registers, in addition to CRC computation during SPI transfer, the MCU must perform the following sequence for all initialization phase registers (FS_I_xxxx):

1. Write the desired data in the FS_I_Register_A (DATA).
2. Write the opposite in the FS_I_NOT_Register_A (DATA_NOT).

As an example, if the data of FS_I_Register_A = ABCDh, the data not of FS_I_NOT_Register_A = 5432h. A real-time comparison process (XOR) is performed by the FS2630 to ensure DATA FS_I_Register_A = DATA_NOT FS_I_NOT_Register_A. Only the utility bits must be inverted in the DATA_NOT content. The RESERVED bits are not considered and can be written as 0. If the comparison result is correct, then the REG_CORRUPT is set to 0. If the comparison result is wrong, then the REG_CORRUPT bit is set to 1. The REG_CORRUPT monitoring is active as soon as the initialization phase is closed by the first good watchdog refresh.

Initialization phase must be closed with a good watchdog refresh before the 256 ms timeout. In case no watchdog refresh or a bad watchdog is sent during the initialization phase, RSTB pulse is generated and the fault error counter is incremented by 1. A new initialization phase is automatically started when RSTB is released. After initialization phase closure, it is possible to come back with the GOTO_INIT bit in the FS_SAFE_IOS_1 register from any fail-safe state after *Safety Initialization Phase*. The GOTO_INIT request will not reset any of the different counters (WD_ERR_CNT, WD_RFR_CNT and FLT_ERR_CNT), nor their respective limits (WD_ERR_LIMIT, WD_RFR_LIMIT and FLT_ERR_CNT_LIMIT), and the RSTB pin will not be asserted.

In case the device is required to go back to initialization phase, NXP recommends sending the GOTO_INIT command immediately after a good watchdog refresh.

22.5 Fail-safe oscillator

A dedicated oscillator is implemented in the fail-safe circuitry. This oscillator is used for all time-based features implemented in the fail-safe domain.

The fail-safe domain is clocked by its own oscillator and is independent from the main domain. The clock has a monitoring feature for low and high-frequency enabled by default.

A SPI flag is available to report a drift on the fail-safe oscillator. If the clock's frequency drifts to the high or low level, safety outputs are asserted.

Table 188. Clock management for fail-safe electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. $V_{SUP\_UVH} < V_{SUP} < 36$ V, $V_{PRE\_PWM} + V_{PRE\_HDR} < V_{SUP\_PWR} < 36$ V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Internal oscillator					
F_{FSOSC}	Fail-safe oscillator nominal frequency	—	20	—	MHz
F_{FSOSC_ACC}	Fail-safe oscillator accuracy	-5	—	5	%
F_{FSOSC_MON}	Fail-safe oscillator failure detection range	-32	—	58	%
$t_{FSOSC\_DET\_TO}$	Fail-safe oscillator failure detection timeout	—	—	2	ms

22.6 Watchdog

A watchdog is implemented through the SPI bus to continuously check the microcontroller software activity and its ability to perform basic computing. The FS2630 performs this check by waiting for a specific answer from the microcontroller during a predefined period called the watchdog window. The first half of the watchdog window is said to be CLOSED and the second half is said to be OPEN.

A good watchdog refresh is a good watchdog answer during the OPEN window. A bad watchdog refresh is a bad watchdog answer during the OPEN window, no watchdog refresh during the OPEN window, or a good watchdog answer during the CLOSED window. After a good or a bad watchdog refresh, a new window period starts immediately for the microcontroller to keep the synchronization with the windowed watchdog. The first good watchdog refresh closes the *initialization phase* of the FS2630. After that, the watchdog window is running, and the microcontroller must refresh the watchdog in the OPEN window of the watchdog window period.

The duration of the watchdog window is configurable from 1.0 ms to 1024 ms with the WDW_PERIOD[3:0] SPI bits. The new watchdog window is effective after the next watchdog refresh. The watchdog window can be disabled only during the *initialization phase* of the FS2630. The watchdog disabling is effective when the *initialization phase* is closed.

The watchdog can be configured in the same way as the *initialization phase* registers: writing to FS_WDW_DURATION and FS_NOT_WDW_DURATION registers. This window concept is applicable for both simple and challenger watchdog types.

Table 189. Watchdog window period configuration

WDW_PERIOD[3:0]	Watchdog window duration
0h	Infinite open window (can be set only during *initialization phase* or *debug mode*)
1h	1.0 ms
2h	2.0 ms
3h (default)	**3.0 ms**
4h	4.0 ms
5h	6.0 ms
6h	8.0 ms
7h	12 ms
8h	16 ms
9h	24 ms
Ah	32 ms
Bh	64 ms
Ch	128 ms
Dh	256 ms
Eh	512 ms
Fh	1024 ms

The duty cycle of the watchdog window is configurable from 31.25 % to 81.25 % with the WDW_DC[2:0] bits. The new duty cycle is effective after the next watchdog refresh.

Table 190. Watchdog window period configuration

WDW_DC[2:0]	CLOSED window	OPEN window
0	31.25 %	68.75 %
1	37.5 %	62.5 %
2 (default)	**50 %**	**50 %**
3	62.5 %	37.5 %
4	68.75 %	31.25 %
5	75 %	25 %
6	81.25 %	18.75 %
7	50 %	50 %

22.6.1 Challenger watchdog

The Challenger watchdog monitoring feature is enabled for ASIL D devices. The Challenger watchdog is based on a question/answer process with the microcontroller. A 16-bit pseudo-random word is generated by implementing a Linear Feedback Shift Register (LFSR) in the FS26. During the initialization phase, the microcontroller can send its own seed for the LFSR, or it can use the default LFSR value generated by the FS26 (0x5AB2), available in the FS_WD_TOKEN register. With the LFSR value, the microcontroller performs a simple calculation based on the formula below and sends the results in the FS_WD_ANSWER register. The result is sent through the SPI bus during the OPEN watchdog window and is verified by the FS26. When the result is right, the watchdog window is restarted and a new LFSR is generated. When the result is wrong, the WD error counter is incremented, the watchdog window is restarted, and the LFSR value is not changed.

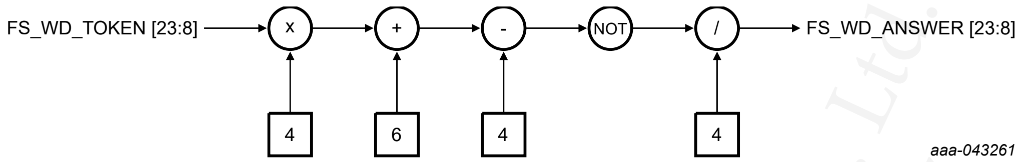

Figure 50. Fail-safe block diagram

In the Challenger watchdog configuration, it is impossible to write 0x0000 in the FS_WD_TOKEN register. If so, a communication error is reported and the configuration is ignored.

22.6.2 Simple watchdog

The Simple watchdog monitoring feature is enabled for ASIL B devices. The Simple watchdog uses a unique seed. The microcontroller can send its own seed in FS_WD_TOKEN register or can use the default value 0x5AB2. This seed must be written in the FS_WD_ANSWER register during the OPEN watchdog window. When the result is right, the watchdog window is restarted. When the result is wrong, the WD error counter is incremented and the watchdog window is restarted. In Simple watchdog configuration, it is impossible to write 0xFFFF and 0x0000 in FS_WD_TOKEN register. A communication error is reported in case of 0x0000 and 0xFFFF write tentative and the configuration is ignored.

22.6.3 Watchdog error counter

The following watchdog error strategy is available for both Challenger and Simple watchdog configurations. The watchdog error counter is implemented in the device to filter the incorrect watchdog refresh. Each time a watchdog failure occurs, the device increments this counter by 2. The watchdog error counter is decremented by 1 each time the watchdog is properly refreshed. This principle guarantees a cyclic 'OK/NOK' behavior, converging to a failure detection. To allow flexibility in the application, the maximum value of this counter is configurable using the WD_ERR_LIMIT[1:0] bits during the *initialization phase*., and will not be reset to the default value when the RSTB pin is asserted.

Table 191. Watchdog window period configuration

WD_ERR_LIMIT[1:0]	Watchdog error counter maximum value
0	8
1 (default)	**6**
2	4
3	2

The watchdog error counter value (WD_ERR_CNT[3:0] bits) can be read by the microcontroller for diagnostic purposes and reset when the RSTB pin is asserted..

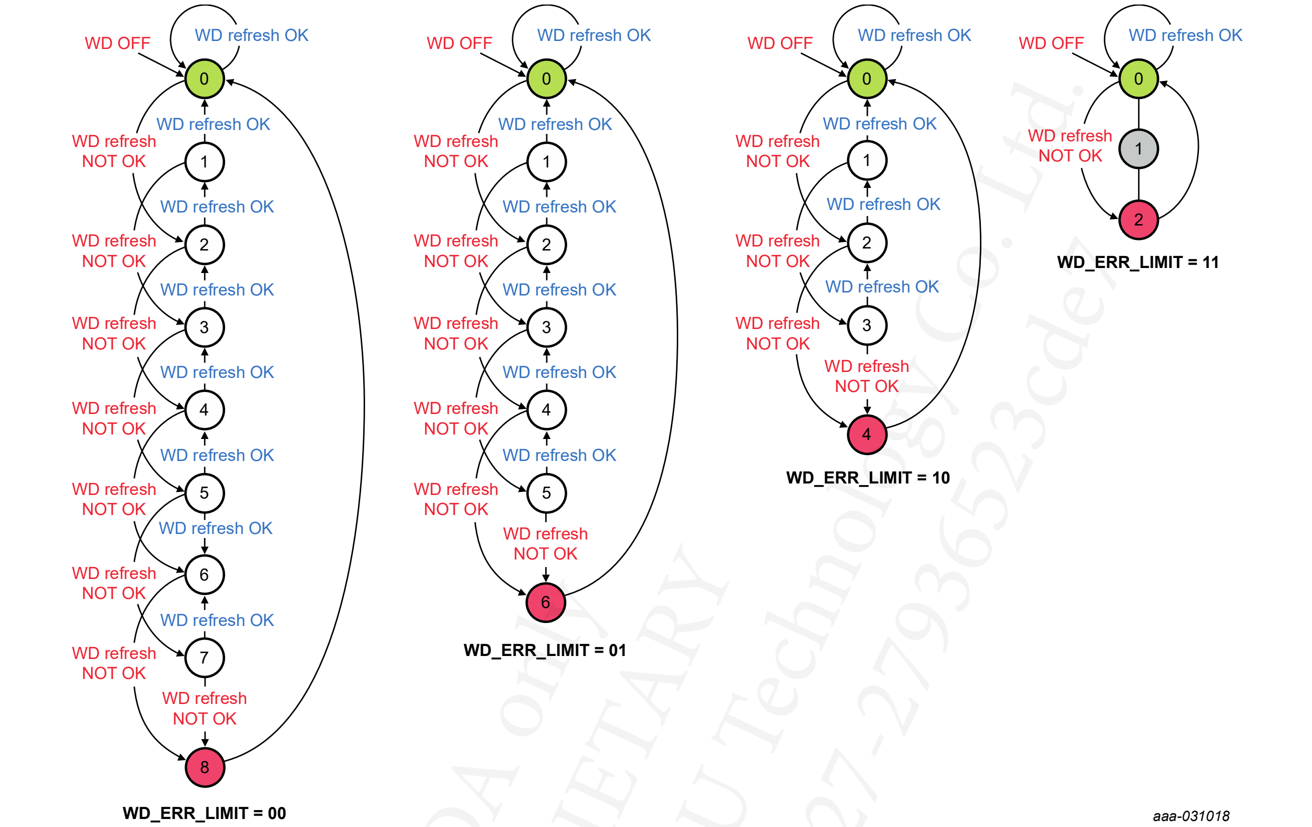

Figure 51. Watchdog error counter

22.6.4 Watchdog refresh counter

The watchdog refresh strategy is available for the Challenger watchdog and the Simple watchdog. The watchdog refresh counter is used to decrement the fault error counter. Each time the watchdog is properly refreshed, the watchdog refresh counter is incremented by '1'. Each time the watchdog refresh counter reaches its maximum value ('6' by default) and if the next WD refresh is also good, the fault error counter is decremented by '1'. Whatever position the watchdog refresh counter is in, each time there is a wrong refresh watchdog, the watchdog refresh counter is reset to '0'. To allow flexibility in the application, the maximum value of this watchdog refresh counter is configurable using the WD_RFR_LIMIT[1:0] bits during the *initialization phase*, and will not be reset to default value when the RSTB pin is asserted.

Table 192. Watchdog refresh counter configuration

WD_RFR_LIMIT[1:0]	Watchdog refresh counter value
00 (by default)	**6**
01	4
10	2
11	1

The watchdog error counter value (WD_RFR_CNT[2:0] bits) can be read by the microcontroller for diagnostic purposes and is reset when RSTB is asserted.

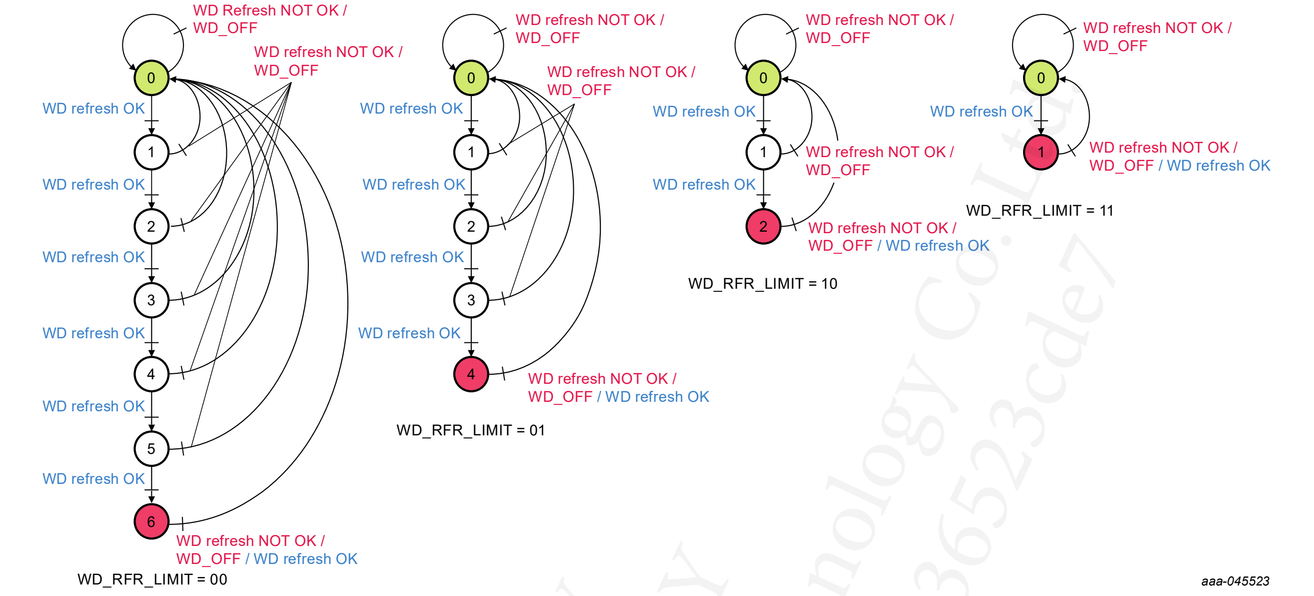

Figure 52. Watchdog refresh counter

22.6.5 Watchdog error impact

When the watchdog error counter reaches its maximum value, the fail-safe reaction on RSTB and/or the safety output(s) is configurable with the WD_FS_REACTION[1:0] bits during the *initialization phase*.

Table 193. Watchdog error impact configuration

WD_FS_REACTION[1:0]	Watchdog error impact on RSTB and FS0B
0	No action on RSTB and the safety output(s)
1	Safety output(s) only is (are) asserted low if WD error counter value = WD_ERR_ LIMIT[1:0]
2 (default) 3	**RSTB and safety output(s) are asserted low if WD error counter value = WD_ERR_ LIMIT[1:0]**

22.6.6 Microcontroller fault recovery strategy

The fault recovery strategy feature is only available for ASIL D part numbers.

This function extends the watchdog window to allow the microcontroller to perform a fault recovery strategy. The goal is to avoid resetting the microcontroller while it is trying to recover the application after a failure event. When a fault is triggered by the microcontroller via its FCCU pins, the safety output(s) pin(s) is (are) asserted by the device, and the watchdog window duration becomes automatically an OPEN window (no more duty cycle). This OPEN window duration is configurable using the WDW_RECOVERY[3:0] bits during the *initialization phase*.

To allow the fault recovery strategy to operate as expected, the user must change the default safety reaction settings from 'RSTB and FS0B are asserted low' to 'FS0B only is asserted in case of fault' with either FCCU12_FS_REACTION, FCCU1_FS_REACTION or FCCU2_FS_REACTION bit. Otherwise, the device asserts RSTB pin as soon as a fault is detected on its FCCU pins, thus preventing the MCU from recovering.

Table 194. Watchdog window duration with FCCU error and recovery strategy enabled

WDW_RECOVERY[3:0]	Watchdog window duration with FCCU error and recovery strategy enabled
0h	Infinite open window (can be set during *initialization phase* and *debug mode* only)
1h	1.0 ms
2h	2.0 ms
3h	3.0 ms
4h	4.0 ms
5h	6.0 ms
6h	8.0 ms
7h	12 ms
8h	16 ms
9h	24 ms
Ah	32 ms
Bh (default)	**64 ms**
Ch	128 ms
Dh	256 ms
Eh	512 ms
Fh	1024 ms

The transition from @WDW_PERIOD[3:0] to @WDW_RECOVERY[3:0] happens when the FCCU pin indicates an error and the safety output(s) is (are) asserted. If the microcontroller sends a good watchdog refresh before the end of the @WDW_RECOVERY[3:0] duration, the device switches back to the @WDW_PERIOD[3:0] duration and associated duty cycle, if the FCCU pins do not indicate an error anymore. Otherwise, a new @WDW_RECOVERY[3:0] period is started. If the microcontroller does not send a good watchdog refresh before the end of the @WDW_RECOVERY[3:0] duration, then a reset pulse is generated and the Fail-safe state machine moves back to the *initialization phase*.

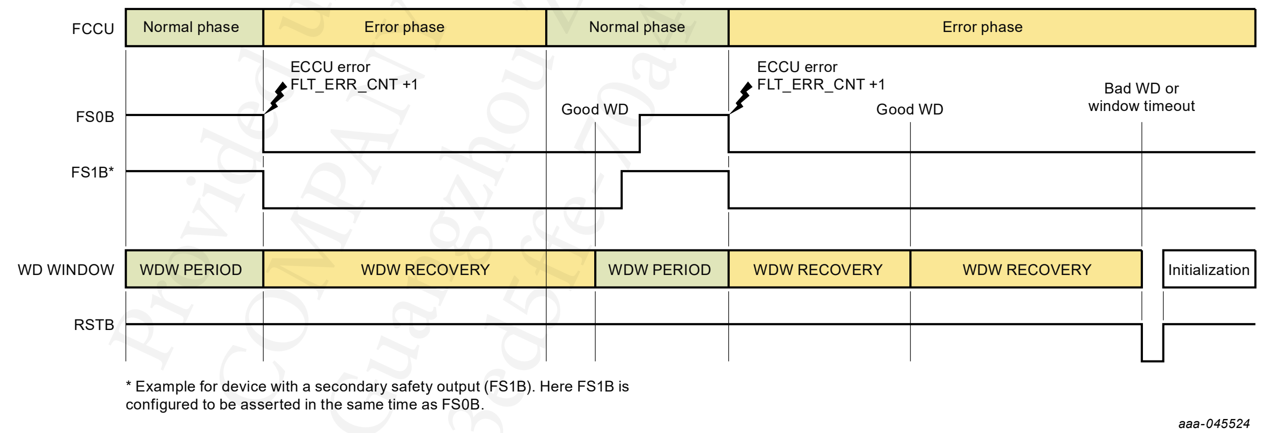

Figure 53. Fault recovery strategy

22.7 FCCU: fault collection and control unit

The FCCU monitoring feature is available for FS26xyD and FS26xyB devices, and can be activated with the OTP bit FCCU_DIS_VOTP. The FCCU input pins are in charge of monitoring hardware failures from the MCU. The FCCU input pins can be configured either by pair or as single independent inputs, and can monitor a PWM signal on one of FCCU1 or FCCU2. The FCCU monitoring is active as soon as the *initialization phase* is closed with good watchdog refresh. The FCCU input pins are configured with the FCCU_CFG[2:0] bits, as described in Table 195.

Table 195. FCCU pin monitoring configuration

FCCU_CFG[2:0]	FCCU monitoring configuration
0	No monitoring
1 (default)	**FCCU1 and FCCU2 inputs monitoring activated by pair (bi-stable protocol)**
2	FCCU1 and FCCU2 single inputs level monitoring activated
3	FCCU1 single input level monitoring only, FCCU2 input not used
4	FCCU1 input not used, FCCU2 single input level monitoring only
5	FCCU1 and FCCU2 single inputs PWM monitoring activated
6	FCCU1 single input PWM monitoring and FCCU2 single input level monitoring
7	FCCU1 single input level monitoring and FCCU2 single input PWM monitoring

22.7.1 FCCU inputs monitoring activated by pair

When this configuration is selected, both FCCU1 and FCCU2 levels are considered to monitor MCU error signals. These levels can be configured with the FCCU12_FLT_POL bit during the *initialization phase*.

Table 196. FCCU12 bi-stable protocol error state configuration

FCCU12_FLT_POL	FCCU monitoring configuration
0 (default)	**FCCU1 = 0 or FCCU2 = 1 level is a fault**
1	FCCU1 = 1 or FCCU2 = 0 level is a fault

The reaction on the safety outputs can be also configured using the FCCU12_FS_REACTION SPI bit during the initialization phase.

Table 197. FCCU12 error reaction configuration

FCCU12_FS_REACTION	Reaction
0	FS0B only is asserted low in case of fault on FCCU1 and FCCU2
1 (default)	**RSTB and FS0B are asserted low in case of fault on FCCU1 and FCCU2**

Figure 55 shows the FCCU pins' hardware connection by pair and the various phases that may occur in an application. This example is valid for FCCU12_FLT_POL = 1 and FCCU12_FS_REACTION = 1.

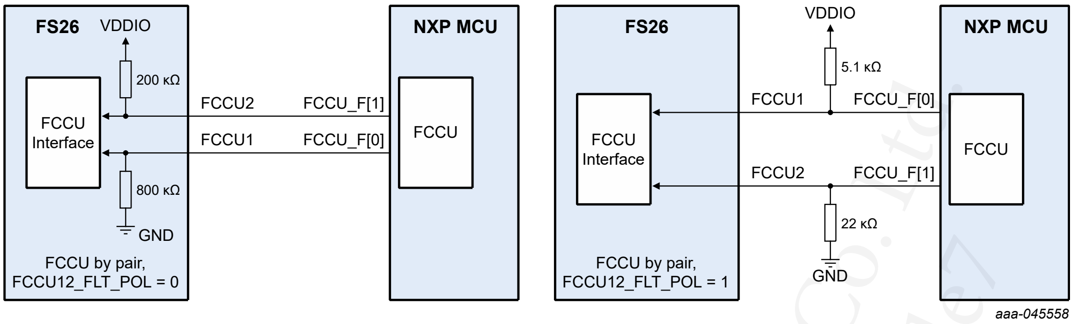

Figure 54. FCCU connection by pair

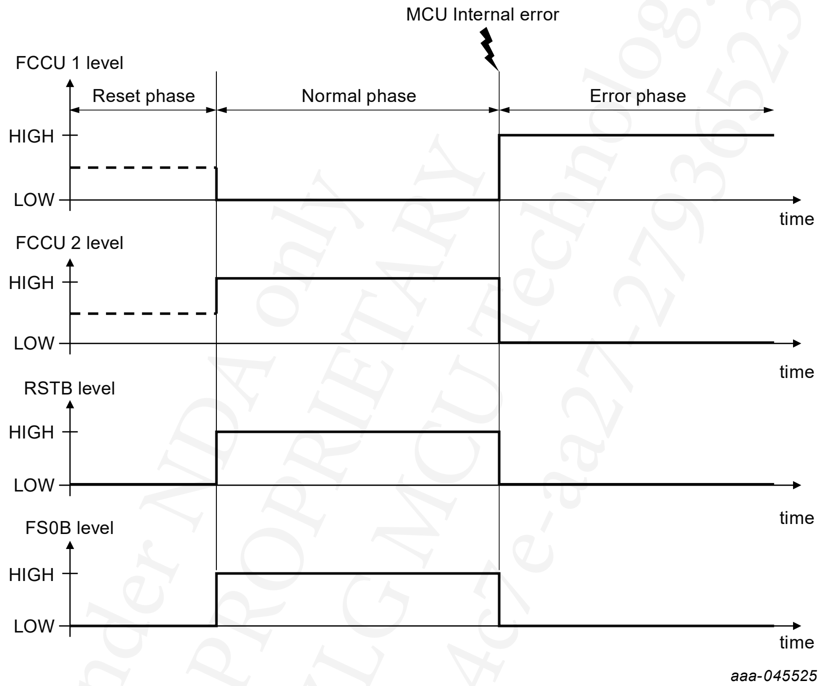

Figure 55. Bi-stable protocol monitored by FCCU pins

22.7.2 FCCU single input monitoring activated

When FCCU_CFG[2:0] = ‘010’, the FCCU inputs are used separately and monitor two different and independent level error signals.

When FCCU_CFG[2:0] = ‘011’, only the FCCU1 input level is monitored and the FCCU2 input is not used.

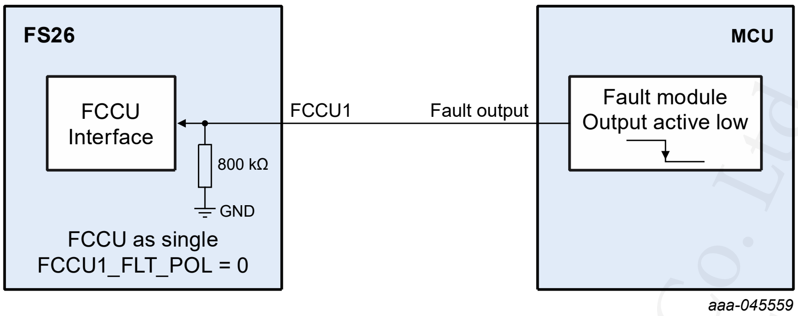

Figure 56. FCCU1 connection as a single independent input and FCCU1_FLT_POL = 0

When FCCU_CFG[2:0] = ‘100’, only the FCCU2 input level is monitored and the FCCU1 input is not used.

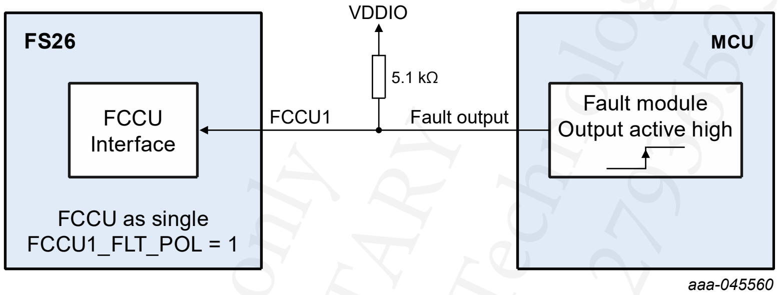

Figure 57. FCCU1 connection as a single independent input and FCCU1_FLT_POL = 1

The error level can be defined by the FCCU1_FLT_POL or FCCU2_FLT_POL bits. The description of SPI bits in this section is valid only if FCCU_CFG[2:0] ≠ ‘000’ or ‘001’.

Table 198. FCCU1 error state configuration

FCCU1_FLT_POL	FCCU1 monitoring configuration
0 (default)	**FCCU1 low level is a fault**
1	FCCU1 high level is a fault

Table 199. FCCU2 error state configuration

FCCU2_FLT_POL	FCCU2 monitoring configuration
0 (default)	**FCCU2 low level is a fault**
1	FCCU2 high level is a fault

The reaction on the safety outputs can be also configured using the FCCU1_FS_REACTION and FCCU2_FS_REACTION SPI bits during the initialization phase.

Table 200. FCCU1 error reaction configuration

FCCU1_FS_REACTION	Reaction
0	FS0B only is asserted low in case of fault on FCCU1
1 (default)	**RSTB and FS0B are asserted low in case of fault on FCCU1**

Table 201. FCCU2 error reaction configuration

FCCU2_FS_REACTION	Reaction
0	FS0B only is asserted low in case of fault on FCCU2
1 (default)	**RSTB and FS0B are asserted low in case of fault on FCCU2**

This Figure 58 timing diagram illustrates FCCU1 monitoring and the various phases that may occur in an application. This example is valid for FCCU_CFG[2:0] = ‘011’, FCCU1_FLT_POL = ‘0’ and FCCU1_FS_REACTION = ‘1’.

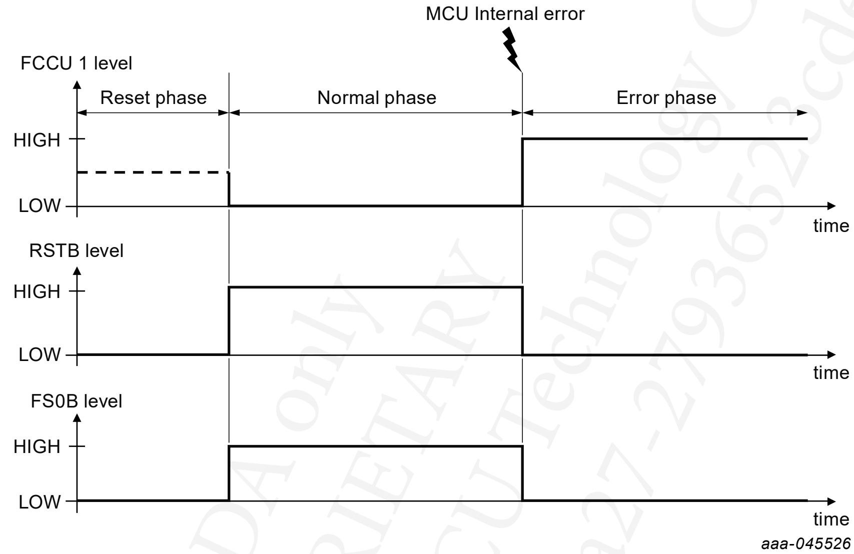

Figure 58. FCCU1 monitoring example

22.7.3 FCCU single PWM monitoring activated

When FCCU_CFG[2:0] = 5, the FCCU1,2 inputs are used separately and monitor two different and independent PWM error signals.

When FCCU_CFG[2:0] = 6, the FCCU1,2 inputs are used separately. FCCU1 monitors a PWM error signal and FCCU2 monitors a level error signal.

When FCCU_CFG[2:0] = 7, the FCCU1,2 inputs are used separately. FCCU2 monitors a PWM error signal and FCCU1 monitors a level error signal.

In this mode, a pulse width modulated waveform is expected to be seen on the FCCU1 or FCCU2 pin. Device monitors each high time and low time for both signals on its FCCU pins. When one of the high time or low times is outside the $t_{PULSE\_FCCU\_HF}$ or $t_{PULSE\_FCCU\_LF}$ limits, device considers that the MCU has an internal error. The reaction on the safety outputs can be also configured using the FCCU1_FS_REACTION or FCCU2_FS_REACTION bits during the *initialization phase*. The description of SPI bits in this section is valid only if FCCU_CFG[2:0] ≠ 0 or 1.

When an FCCU input pin is configured in PWM monitoring, $t_{FCCU\_ERR\_PWM}$ filtering time is automatically selected. When an FCCU input pin is configured in level monitoring, t_{FCCU_ERR} filtering time can be configured.

Table 202. FCCU1 error reaction configuration

FCCU1_FS_REACTION	Reaction
0	FS0B only is asserted low in case of fault on FCCU1
1 (default)	**RSTB and FS0B are asserted low in case of fault on FCCU1**

Table 203. FCCU2 error reaction configuration

FCCU2_FS_REACTION	Reaction
0	FS0B only is asserted low in case of fault on FCCU2
1 (default)	**RSTB and FS0B are asserted low in case of fault on FCCU2**

This Figure 59 timing diagram illustrates FCCU1 monitoring and the various phases that can occur with the application. This example is valid for FCCU_CFG[2:0] = 5 and FCCU1_FS_REACTION = 1.

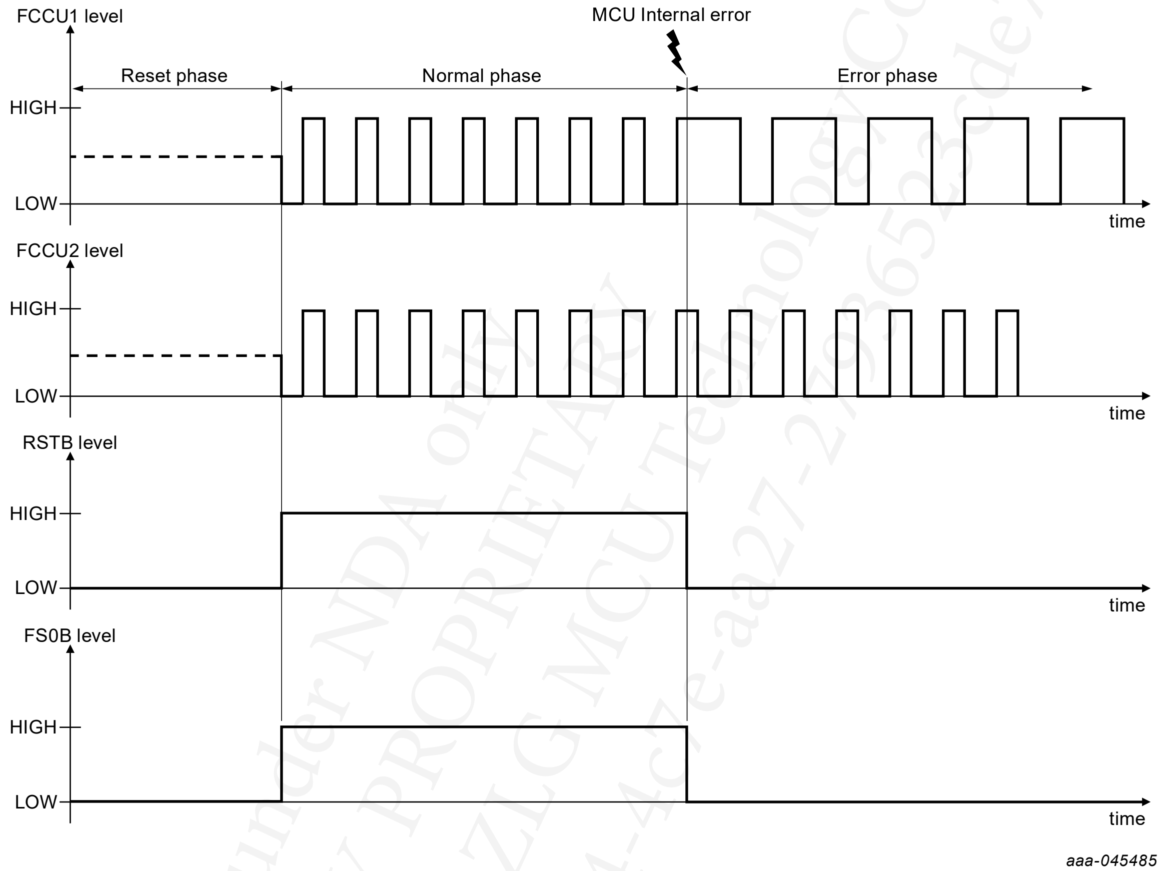

Figure 59. Dual input PWM monitoring example

The PWM monitoring functionality is constantly checking both high level and low level durations of pulses that are monitored on FCCU1 and FCCU2 input pins with regard to $t_{PULSE\_FCCU\_HF}$ or $t_{PULSE\_FCCU\_LF}$ limits.

Table 204. FCCU monitoring electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. $V_{SUP\_UVH} < V_{SUP} < 36$ V, $V_{PRE\_PWM} + V_{PRE\_HDR} < V_{SUP\_PWR} < 36$ V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Static electrical characteristics					
V_{IL_FCCU}	FCCU1,2 digital low input level threshold	0	—	0.3 * V_{DDIO}	V
V_{IH_FCCU}	FCCU1,2 digital high input level threshold	0.7 * V_{DDIO}	—	5.0	V
V_{HYST_FCCU}	FCCU1,2 input voltage hysteresis	0.1	—	0.6	V

Table 204. FCCU monitoring electrical characteristics*...continued*

T_A = –40 °C to 125 °C, unless otherwise specified. $V_{SUP\_UVH} < V_{SUP}$ < 36 V, $V_{PRE\_PWM} + V_{PRE\_HDR} < V_{SUP\_PWR}$ < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
R_{PD_FCCU1}	FCCU1 pin internal pull-down	400	800	1300	kΩ
R_{PU_FCCU2}	FCCU2 pin internal pull-up to VDDIO pin	100	200	400	kΩ
Dynamic electrical characteristics					
t_{FCCU_ERR}	FCCU inputs filtering time FCCU12_FILT[1:0] = 0 FCCU12_FILT[1:0] = 1 FCCU12_FILT[1:0] = 2 FCCU12_FILT[1:0] = 3	 1 4 8 16	 3 6 12 20	 4 8 16 24	 µs
$t_{FCCU\_ERR\_PWM}$	FCCU1,2 filtering time when configured in PWM monitoring	0.8	1	1.2	µs
F_{FCCU12_GF}	FCCU1,2 good frequency range (PWM detection)	10	—	45	kHz
F_{FCCU12_BLF}	FCCU1,2 bad low-frequency range (PWM detection)	—	—	5	kHz
F_{FCCU12_BHF}	FCCU1,2 bad high-frequency range (PWM detection)	90	—	—	kHz
$t_{PULSE\_FCCU\_HF}$	FCCU1,2 high and low level detection time (high-frequency) measured on both pulse polarity.	6	8	10	µs
$t_{PULSE\_FCCU\_LF}$	FCCU1,2 high and low level detection time (low-frequency) measured on both pulse polarity.	51	64	80	µs

22.8 Voltage supervision

The voltage supervisor is dedicated to monitoring the power rails generated by the FS26 for the application. For regulated voltages, an overvoltage detection and an undervoltage detection are embedded into the voltage supervisor. Thanks to these fault detections, a configurable reaction on the safety outputs and the RSTB pin can be programmed for each regulator. The VBST voltage output is not monitored by the voltage supervision. Dedicated pins are available to monitor synchronous bucks (VPRE and VCORE). Linear regulators (LDO1, LDO2, VREF, TRK1, and TRK2) are monitored through internal connections. When an overvoltage fault occurs, the corresponding regulator is switched off, and a SPI flag bit is set. As soon as the overvoltage goes away, the regulator restarts, doing a soft start toward the output voltage set by OTP.

One extra monitoring pin, called VMONEXT, can be used to monitor a voltage generated by another part into the application. When an overvoltage is detected on the VMONEXT pin, a SPI flag bit is set.

22.8.1 VMON_PRE: VPRE monitoring

FS2630 VMON_PRE can detect out of range operation on the VPRE output voltage using the VMONPRE pin. Overvoltage events are reported by VPRE_OV flag and undervoltage events are reported by VPRE_UV flag. The monitoring is enabled once the power-up sequence is completed and the *enable monitoring* state is reached.

To support various output voltages of VPRE, the target voltage value to monitor is set with VPRE_V_OTP[5:0] bitfield. The overvoltage threshold is set with VMON_PRE_OVTH_OTP[3:0] bitfield and the undervoltage threshold is set with VMON_PRE_UVTH_OTP[3:0] bitfield.

The reactions on safety pins (RSTB and FS0B) are configured during the *initialization phase*, overvoltage with VMON_PRE_OV_FS_REACTION[1:0] bitfield and undervoltage with VMON_PRE_UV_FS_REACTION[1:0] bitfield.

Table 205. VMON_PRE overvoltage reaction configuration

VMON_PRE_OV_FS_REACTION[1:0]	Overvoltage faults reaction
0	No action on Safety Output(s) and RSTB
1	An overvoltage detection asserts safety output(s) only
2 (default) 3	**An overvoltage detection asserts safety output(s) and RSTB**

Table 206. VMON_PRE undervoltage reaction configuration

VMON_PRE_UV_FS_REACTION[1:0]	Undervoltage faults reaction
0	No action on Safety Output(s) and RSTB
1 (default)	**An undervoltage detection asserts safety output(s) only**
2 3	An undervoltage detection asserts safety output(s) and RSTB

Table 207. VMON_PRE monitoring electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. $V_{SUP\_UVH} < V_{SUP} < 36$ V, $V_{PRE\_PWM} + V_{PRE\_HDR} < V_{SUP\_PWR} < 36$ V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Static electrical characteristics					
$VMON_{PRE\_RANGE}$	VMON_PRE monitoring target voltage setting range	3.7	—	6.35	V
$VMON_{PRE\_STEP}$	VMON_PRE overvoltage monitoring target voltage setting step with VPRE_V_OTP[5:0] bits	—	50	—	mV
$VMON_{PRE\_OVTH\_RANGE}$	VMON_PRE overvoltage monitoring threshold range setting with VMON_PRE_OVTH_OTP[3:0] bits	106	—	112	%
$VMON_{PRE\_OVTH\_STEP}$	VMON_PRE overvoltage monitoring OTP threshold setting step	—	0.5	—	%
$VMON_{PRE\_OVTH\_ACC}$	VMON_PRE overvoltage detection accuracy	-1	—	1	%
$VMON_{PRE\_UVTH\_RANGE}$	VMON_PRE undervoltage monitoring threshold range setting with VMON_PRE_UVTH_OTP[3:0] bits	88	—	94	%
$VMON_{PRE\_UVTH\_STEP}$	VMON_PRE undervoltage monitoring OTP threshold setting step	—	0.5	—	%
$VMON_{PRE\_UVTH\_ACC}$	VMON_PRE undervoltage detection accuracy	-1	—	1	%
Dynamic electrical characteristics					
$t_{VMON\_PRE\_OV\_DGLT}$	VMON_PRE overvoltage deglitch time VMON_PRE_OVDGLT_OTP = 0 VMON_PRE_OVDGLT_OTP = 1	 20 40	 25 45	 30 50	µs
$t_{VMON\_PRE\_UV\_DGLT}$	VMON_PRE undervoltage deglitch time VMON_PRE_UVDGLT_OTP[1:0] = 0 VMON_PRE_UVDGLT_OTP[1:0] = 1 VMON_PRE_UVDGLT_OTP[1:0] = 2 VMON_PRE_UVDGLT_OTP[1:0] = 3	 2.5 10 20 35	 5 15 25 40	 7.5 20 30 45	µs

22.8.2 VMON_CORE: VCORE monitoring

FS2630 VMON_CORE can detect out of range operation on the VCORE output voltage using the VMONCORE pin. Overvoltage events are reported by CORE_OV flag and undervoltage events are reported by CORE_UV flag. The monitoring is enabled once the power-up sequence is completed and the *Enable Monitoring* state is reached.

To support various output voltages of VCORE, the target voltage value to monitor is set with VCORE_V_OTP[7:0] bitfield. The overvoltage threshold is set with VMON_CORE_OVTH_OTP[3:0] bitfield and the undervoltage threshold is set with VMON_CORE_UVTH_OTP[3:0] bitfield.

The reactions on safety pins (RSTB and FS0B) are configured during the *initialization phase*, overvoltage with VMON_CORE_OV_FS_REACTION[1:0] bitfield and undervoltage with VMON_CORE_UV_FS_REACTION[1:0] bitfield.

Table 208. VMON_CORE overvoltage reaction configuration

VMON_CORE_OV_FS_REACTION[1:0]	Overvoltage faults reaction
0	No action on Safety Output(s) and RSTB
1	An overvoltage detection asserts safety output(s) only
2 (default) 3	**An overvoltage detection asserts safety output(s) and RSTB**

Table 209. VMON_CORE undervoltage reaction configuration

VMON_CORE_UV_FS_REACTION[1:0]	Undervoltage faults reaction
0	No action on Safety Output(s) and RSTB
1 (default)	**An undervoltage detection asserts safety output(s) only**
2 3	An undervoltage detection asserts Safety output(s) and RSTB

Table 210. VMON_CORE monitoring electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. $V_{SUP\_UVH} < V_{SUP} < 36$ V, $V_{PRE\_PWM} + V_{PRE\_HDR} < V_{SUP\_PWR} < 36$ V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Static electrical characteristics					
$VMON_{CORE\_RANGE}$	VMON_CORE monitoring target voltage setting range	0.8	—	3.35	V
$VMON_{CORE\_STEP}$	VMON_CORE overvoltage monitoring target voltage setting step with VCORE_V_OTP[7:0] bits	—	10	—	mV
$VMON_{CORE\_OVTH\_RANGE}$	VMON_CORE overvoltage monitoring threshold range setting with VMON_CORE_OVTH_OTP[3:0] bits	104.5	—	112	%
$VMON_{CORE\_OVTH\_STEP}$	VMON_CORE overvoltage monitoring OTP threshold setting step	—	0.5	—	%
$VMON_{CORE\_OVTH\_ACC}$	VMON_CORE overvoltage detection accuracy	-1	—	1	%
$VMON_{CORE\_UVTH\_RANGE}$	VMON_CORE undervoltage monitoring threshold range setting with VMON_CORE_UVTH_OTP[3:0] bits	88	—	95.5	%

Table 210. VMON_CORE monitoring electrical characteristics*...continued*

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < V_{SUP} < 36 V, V_{PRE_PWM} + V_{PRE_HDR} < V_{SUP_PWR} < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
$VMON_{CORE\_UVTH\_STEP}$	VMON_CORE undervoltage monitoring OTP threshold setting step	—	0.5	—	%
$VMON_{CORE\_UVTH\_ACC}$	VMON_CORE undervoltage detection accuracy	-1	—	1	%
Dynamic electrical characteristics					
$t_{VMON\_CORE\_OV\_DGLT}$	VMON_CORE overvoltage deglitch time VMON_CORE_OVDGLT_OTP = 0 VMON_CORE_OVDGLT_OTP = 1	20 40	25 45	30 50	µs
$t_{VMON\_CORE\_UV\_DGLT}$	VMON_CORE undervoltage deglitch time VMON_CORE_UVDGLT_OTP[1:0] = 0 VMON_CORE_UVDGLT_OTP[1:0] = 1 VMON_CORE_UVDGLT_OTP[1:0] = 2 VMON_CORE_UVDGLT_OTP[1:0] = 3	2.5 10 20 35	5 15 25 40	7.5 20 30 45	µs

22.8.3 VMON_LDO1: LDO1 monitoring

FS2630 VMON_LDO1 can detect out of range operation on the LDO1 output voltage using an internal dedicated connection to the LDO1OUT pin. Overvoltage events are reported by LDO1_OV flag and undervoltage events are reported by LDO1_UV flag. The monitoring is enabled once the power-up sequence is completed and the *enable monitoring* state is reached.

To support various output voltages of LDO1, the target voltage value to monitor is set with LDO1_V_OTP bit. The overvoltage threshold is set with VMON_LDO1_OVTH_OTP[3:0] bitfield and the undervoltage threshold is set with VMON_LDO1_UVTH_OTP[3:0] bitfield.

The reactions on safety pins (RSTB and FS0B) are configured during the *initialization phase*, overvoltage with VMON_LDO1_OV_FS_REACTION[1:0] bitfield and undervoltage with VMON_LDO1_UV_FS_REACTION[1:0] bitfield.

To reach ASIL D at the LDO1OUT pin level, the pin lift detection mechanism must be activated using the LDO1_PLIFT_DIS_OTP bit.

If the LDO1OUT pin is disconnected, the LDO1 output voltage will be pulled up to LDOIN within $t_{LDO1\_PINLIFT}$ to create an overvoltage, and the device will react as VMON_LDO1_OV_FS_REACTION[1:0]. A minimum headroom $V_{LDOIN\_MIN\_PINLIFT}$ is mandatory to guarantee the pin lift detection.

A degraded undervoltage threshold can be selected with VMON_LDO2_UVDTH_OTP bit to avoid an MCU reset during cranking event. The threshold is fixed at 62 %, and is not configurable by software. This feature must be used only when LDO1 is set to 5 V to supply the microcontroller.

Table 211. VMON_LDO1 degraded undervoltage configuration

VMON_LDO1_UVDTH_OTP	VLDO1_OTP	Undervoltage threshold configuration
0	x	Normal UV (Configuration using VMON_LDO1_UVTH_OTP[3:0])
1	1	Fixed Degraded UV

To allow flexibility in the application, both reactions to over and undervoltage faults are configurable with the VMON_LDO1_OV_FS_REACTION[1:0] and VMON_LDO1_UV_FS_REACTION[1:0] bits during the *initialization phase*.

The monitoring is able to report UV/OV flags as soon as the power up sequence is completed and the *enable monitoring* state is reached.

Table 212. VMON_LDO1 overvoltage reaction configuration

VMON_LDO1_OV_FS_REACTION[1:0]	Overvoltage faults reaction
0	No action on Safety Output(s) and RSTB
1	An overvoltage detection asserts safety output(s) only
2 (default) 3	**An overvoltage detection asserts safety output(s) and RSTB**

Table 213. LDO1 undervoltage reaction configuration

VMON_LDO1_UV_FS_REACTION[1:0]	Undervoltage faults reaction
0	No action on Safety Output(s) and RSTB
1 (default)	**An undervoltage detection asserts safety output(s) only**
2 3	An undervoltage detection asserts Safety output(s) and RSTB

Table 214. VMON_LDO1 monitoring electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. $V_{SUP\_UVH} < V_{SUP} < 36$ V, $V_{PRE\_PWM} + V_{PRE\_HDR} < V_{SUP\_PWR} < 36$ V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Static electrical characteristics					
$VMON_{LDO1\_CFG}$	VMON_LDO1 monitoring target voltage setting LDO1_V_OTP bit = 0 LDO1_V_OTP bit = 1	 — —	 3.3 5.0	 — —	V
$V_{LDOIN\_MIN\_PINLIFT}$	Minimum headroom to guarantee LDO1OUT pin lift detection	LDO1_V_OTP x (@VMON_ LDO1_OVTH_ OTP[3:0] + 1 %) + 0.5 V	—	—	V
$VMON_{LDO1\_OVTH\_RANGE}$	VMON_LDO1 overvoltage monitoring threshold range setting with VMON_LDO1_OVTH_OTP[3:0] bits	104.5	—	112	%
$VMON_{LDO1\_OVTH\_STEP}$	VMON_LDO1 overvoltage monitoring OTP threshold setting step	—	0.5	—	%
$VMON_{LDO1\_OVTH\_ACC}$	VMON_LDO1 overvoltage detection accuracy	-1	—	1	%
$VMON_{LDO1\_UVTH\_RANGE}$	VMON_LDO1 undervoltage monitoring threshold range setting with VMON_LDO1_UVTH_OTP[3:0] bits	88	—	95.5	%
$VMON_{LDO1\_UVTH\_STEP}$	VMON_LDO1 undervoltage monitoring OTP threshold setting step	—	0.5	—	%
$VMON_{LDO1\_UVTH\_ACC}$	VMON_LDO1 undervoltage detection accuracy	-1	—	1	%
$VMON_{\_LDO1\_UVDTH}$	Degraded undervoltage threshold	61	62	63	%

Table 214. VMON_LDO1 monitoring electrical characteristics...*continued*

T_A = –40 °C to 125 °C, unless otherwise specified. $V_{SUP\_UVH} < V_{SUP} < 36$ V, $V_{PRE\_PWM} + V_{PRE\_HDR} < V_{SUP\_PWR} < 36$ V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Dynamic electrical characteristics					
$t_{VMON\_LDO1\_OV\_DGLT}$	VMON_LDO1 overvoltage deglitch time: VMON_LDO1_OVDGLT_OTP = 0 VMON_LDO1_OVDGLT_OTP = 1	 20 40	 25 45	 30 50	µs
$t_{VMON\_LDO1\_UV\_DGLT}$	VMON_LDO1 undervoltage deglitch time: VMON_LDO1_UVDGLT_OTP[1:0] = 0 VMON_LDO1_UVDGLT_OTP[1:0] = 1 VMON_LDO1_UVDGLT_OTP[1:0] = 2 VMON_LDO1_UVDGLT_OTP[1:0] = 3	 2.5 10 20 35	 5 15 25 40	 7.5 20 30 45	µs
$t_{VMON\_LDO1\_PINLIFT}$	LDO1 pin lift detection time	—	—	5	ms

22.8.4 VMON_LDO2: LDO2 monitoring

FS2630 VMON_LDO2 can detect out of range operation on the LDO2 output voltage using an internal dedicated connection to the LDO2OUT pin. Overvoltage events are reported by LDO2_OV flag and undervoltage events are reported by LDO2_UV flag. The monitoring is enabled once the power-up sequence is completed and the *enable monitoring* state is reached.

To support various output voltages of LDO2, the target voltage value to monitor is set with LDO2_V_OTP bit. The overvoltage threshold is set with VMON_LDO2_OVTH_OTP[3:0] bitfield and the undervoltage threshold is set with VMON_LDO2_UVTH_OTP[3:0] bitfield.

The reactions on safety pins (RSTB and FS0B) are configured during the *initialization phase*, overvoltage with VMON_LDO2_OV_FS_REACTION[1:0] bitfield and undervoltage with VMON_LDO2_UV_FS_REACTION[1:0] bitfield.

To reach ASIL D at the LDO2OUT pin level, the pin lift detection mechanism must be activated using the LDO2_PLIFT_DIS_OTP bit.

If the LDO2OUT pin is disconnected, the LDO2 output voltage will be pulled up to LDOIN within $t_{LDO2\_PINLIFT}$ to create an overvoltage, and the device will react as VMON_LDO2_OV_FS_REACTION[1:0]. A minimum headroom $V_{LDOIN\_MIN\_PINLIFT}$ is mandatory to guarantee the pin lift detection.

A degraded undervoltage threshold can be selected with VMON_LDO2_UVDTH_OTP bit to avoid an MCU reset during cranking event. The threshold is fixed at 62 %, and is not configurable by software. This feature must be used only when LDO2 is set to 5 V to supply the microcontroller.

Table 215. VMON_LDO2 degraded undervoltage configuration

VMON_LDO2_UVDTH_OTP	VLDO2_OTP	Undervoltage threshold configuration
0	x	Normal UV (Configuration using VMON_LDO2_UVTH_OTP[3:0])
1	1	Fixed Degraded UV

To allow flexibility in the application, both reactions to over and undervoltage faults are configurable with the VMON_LDO2_OV_FS_REACTION[1:0] and VMON_LDO2_UV_FS_REACTION[1:0] bits during the *initialization phase*.

The monitoring is able to report UV/OV flags as soon as the power-up sequence is completed and the *enable monitoring* state is reached.

Table 216. VMON_LDO2 overvoltage reaction configuration

VMON_LDO2_OV_FS_REACTION[1:0]	Overvoltage faults reaction
0	No action on Safety Output(s) and RSTB
1	An overvoltage detection asserts safety output(s) only
2 (default) 3	**An overvoltage detection asserts safety output(s) and RSTB**

Table 217. VMON_LDO2 undervoltage reaction configuration

VMON_LDO2_UV_FS_REACTION[1:0]	Undervoltage faults reaction
0	No action on Safety Output(s) and RSTB
1 (default)	**An undervoltage detection asserts safety output(s) only**
2 3	An undervoltage detection asserts Safety output(s) and RSTB

Table 218. VMON_LDO2 monitoring electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. $V_{SUP\_UVH} < V_{SUP} <$ 36 V, $V_{PRE\_PWM} + V_{PRE\_HDR} < V_{SUP\_PWR} <$ 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Static electrical characteristics					
$VMON_{LDO2\_V}$	VMON_LDO2 monitoring target voltage setting LDO2_V_OTP = 0 LDO2_V_OTP = 1	— —	3.3 5.0	— —	V
$V_{LDOIN\_MIN\_PINLIFT}$	Minimum headroom to guarantee LDO2OUT pin lift detection	LDO2_V_OTP x (@VMON_ LDO2_OVTH_ OTP[3:0] + 1 %) + 0.5 V	—	—	V
$VMON_{LDO2\_OVTH\_RANGE}$	VMON_LDO2 overvoltage monitoring threshold range setting with VMON_LDO2_OVTH_OTP[3:0] bitfield	104.5	—	112	%
$VMON_{LDO2\_OVTH\_STEP}$	VMON_LDO2 overvoltage monitoring OTP threshold setting step	—	0.5	—	%
$VMON_{LDO2\_OVTH\_ACC}$	VMON_LDO2 overvoltage detection accuracy	-1	—	1	%
$VMON_{LDO2\_UVTH\_RANGE}$	VMON_LDO2 undervoltage monitoring threshold range setting with VMON_LDO2_UVTH_OTP[3:0] bitfield	88	—	95.5	%
$VMON_{LDO2\_UVTH\_STEP}$	VMON_LDO2 undervoltage monitoring OTP threshold setting step	—	0.5	—	%
$VMON_{LDO2\_UVTH\_ACC}$	VMON_LDO2 undervoltage detection accuracy	-1	—	1	%
$VMON_{\_LDO2\_UVDTH}$	Degraded undervoltage threshold	61	62	63	%

Table 218. VMON_LDO2 monitoring electrical characteristics*...continued*

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < V_{SUP} < 36 V, V_{PRE_PWM} + V_{PRE_HDR} < V_{SUP_PWR} < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Dynamic Electrical Characteristics					
$t_{VMON\_LDO2\_OV\_DGLT}$	VMON_LDO2 overvoltage deglitch time: VMON_LDO2_OVDGLT_OTP = 0 VMON_LDO2_OVDGLT_OTP = 1	 20 40	 25 45	 30 50	μs
$t_{VMON\_LDO2\_UV\_DGLT}$	VMON_LDO2 undervoltage deglitch time: VMON_LDO2_UVDGLT_OTP[1:0] = 0 VMON_LDO2_UVDGLT_OTP[1:0] = 1 VMON_LDO2_UVDGLT_OTP[1:0] = 2 VMON_LDO2_UVDGLT_OTP[1:0] = 3	 2.5 10 20 35	 5 15 25 40	 7.5 20 30 45	μs
$t_{VMON\_LDO2\_PINLIFT}$	LDO2 pin lift detection time	—	—	5	ms

22.8.5 VMON_TRK1: TRK1 monitoring

FS2630 VMON_TRK1 can detect out of range operation on the TRK1 output voltage using an internal dedicated connection to the TRK1 pin. Overvoltage events are reported by TRK1_OV flag and undervoltage events are reported by TRK1_UV flag. The monitoring is enabled once the power-up sequence is completed and the *enable monitoring* state is reached.

To support various output voltages of TRK1, the target voltage value to monitor is set with TRK1_V_OTP[1:0] bitfield. The overvoltage threshold is set with VMON_TRK1_OVTH_OTP[3:0] bitfield and the undervoltage threshold is set with VMON_TRK1_UVTH_OTP[3:0] bitfield.

The reactions on safety pins (RSTB and FS0B) are configured during the *initialization phase*, overvoltage with VMON_TRK1_OV_FS_REACTION[1:0] bitfield and undervoltage with VMON_TRK1_UV_FS_REACTION[1:0] bitfield. If a 'short to high' type of fault on TRK1 should not impact RSTB, NXP recommends configuring VMON_TRK1_OV_FS_REACTION[1:0] = 01 before enabling TRK1 by SPI.

If TRK1 is used as a supply, outside of the module, NXP recommends excluding it from the ABIST1 verification, avoiding a stuck in reset condition in case of a short circuit to ground.

If TRK1 is safety related in the application, the voltage monitoring should be checked with the ABIST on demand (ABIST2).

Table 219. VMON_TRK1 overvoltage reaction configuration

VMON_TRK1_OV_FS_REACTION[1:0]	Overvoltage faults reaction
0	No action on Safety Output(s) and RSTB
1	An overvoltage detection asserts safety output(s) only
2 (default) 3	**An overvoltage detection asserts safety output(s) and RSTB**

Table 220. VMON_TRK1 undervoltage reaction configuration

VMON_TRK1_UV_FS_REACTION[1:0]	Undervoltage faults reaction
0	No action on Safety Output(s) and RSTB
1 (default)	**An undervoltage detection asserts safety output(s) only**

Table 220. VMON_TRK1 undervoltage reaction configuration*...continued*

VMON_TRK1_UV_FS_REACTION[1:0]	Undervoltage faults reaction
2 3	An undervoltage detection asserts Safety output(s) and RSTB

Table 221. VMON_TRK1 monitoring electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. $V_{SUP\_UVH} < V_{SUP} <$ 36 V, $V_{PRE\_PWM} + V_{PRE\_HDR} < V_{SUP\_PWR} <$ 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Static electrical characteristics					
$VMON_{TRK1\_V}$	VMON_TRK1 monitoring target voltage setting TRK1_V_OTP[1:0] = 0 TRK1_V_OTP[1:0] = 1 TRK1_V_OTP[1:0] = 2 TRK1_V_OTP[1:0] = 3	 — — — —	 1.2 1.8 3.3 5	 — — — —	V
$VMON_{TRK1\_OVTH\_RANGE}$	VMON_TRK1 overvoltage monitoring threshold range setting with VMON_TRK1_OVTH_OTP[3:0] bitfield	104.5	—	112	%
$VMON_{TRK1\_OVTH\_STEP}$	VMON_TRK1 overvoltage monitoring OTP threshold setting step	—	0.5	—	%
$VMON_{TRK1\_OVTH\_ACC}$	VMON_TRK1 overvoltage detection accuracy	-1	—	1	%
$VMON_{TRK1\_UVTH\_RANGE}$	VMON_TRK1 undervoltage monitoring threshold range setting with VMON_TRK1_UVTH_OTP[3:0] bitfield	88	—	95.5	%
$VMON_{TRK1\_UVTH\_STEP}$	VMON_TRK1 undervoltage monitoring OTP threshold setting step	—	0.5	—	%
$VMON_{TRK1\_UVTH\_ACC}$	VMON_TRK1 undervoltage detection accuracy	-1	—	1	%
Dynamic electrical characteristics					
$t_{VMON\_TRK1\_OV\_DGLT}$	VMON_TRK1 overvoltage deglitch time VMON_TRK1_OVDGLT_OTP = 0 VMON_TRK1_OVDGLT_OTP = 1	 20 40	 25 45	 30 50	µs
$t_{VMON\_TRK1\_UV\_DGLT}$	VMON_TRK1 undervoltage deglitch time VMON_TRK1_UVDGLT_OTP[1:0] = 0 VMON_TRK1_UVDGLT_OTP[1:0] = 1 VMON_TRK1_UVDGLT_OTP[1:0] = 2 VMON_TRK1_UVDGLT_OTP[1:0] = 3	 2.5 10 20 35	 5 15 25 40	 7.5 20 30 45	µs

22.8.6 VMON_TRK2: TRK2 monitoring

FS2630 VMON_TRK2 can detect out of range operation on the TRK2 output voltage using an internal dedicated connection to the TRK2 pin. Overvoltage events are reported by TRK2_OV flag and undervoltage events are reported by TRK2_UV flag. The monitoring is enabled once the power-up sequence is completed and the *enable monitoring* state is reached.

To support various output voltages of TRK2, the target voltage value to monitor is set with TRK2_V_OTP[1:0] bitfield. The overvoltage threshold is set with VMON_TRK2_OVTH_OTP[3:0] bitfield and the undervoltage threshold is set with VMON_TRK2_UVTH_OTP[3:0] bitfield.

The reactions on safety pins (RSTB and FS0B) are configured during the *initialization phase*, overvoltage with VMON_TRK2_OV_FS_REACTION[1:0] bitfield and undervoltage with VMON_TRK2_UV_FS_REACTION[1:0] bitfield. If a 'short to high' type of fault on TRK2 should not impact RSTB, NXP recommends configuring VMON_TRK2_OV_FS_REACTION[1:0] = 01 before enabling TRK2 by SPI.

If TRK2 is used as a supply, outside of the module, NXP recommends excluding it from the ABIST1 verification, avoiding a stuck in reset condition in case of a short circuit to ground.

If TRK2 is safety related in the application, the voltage monitoring should be checked with the ABIST on demand (ABIST2).

Table 222. VMON_TRK2 overvoltage reaction configuration

VMON_TRK2_OV_FS_REACTION[1:0]	Overvoltage faults reaction
0	No action on Safety Output(s) and RSTB
1	An overvoltage detection asserts safety output(s) only
2 (default) 3	**An overvoltage detection asserts safety output(s) and RSTB**

Table 223. VMON_TRK2 undervoltage reaction configuration

VMON_TRK2_UV_FS_REACTION[1:0]	Undervoltage faults reaction
0	No action on Safety Output(s) and RSTB
1 (default)	**An undervoltage detection asserts safety output(s) only**
2 3	An undervoltage detection asserts Safety output(s) and RSTB

Table 224. VMON_TRK2 monitoring electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. $V_{SUP\_UVH} < V_{SUP} < 36$ V, $V_{PRE\_PWM} + V_{PRE\_HDR} < V_{SUP\_PWR} < 36$ V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Static electrical characteristics					
$VMON_{TRK2\_CFG}$	VMON_TRK2 monitoring target voltage setting TRK2_V_OTP[1:0] = 0 TRK2_V_OTP[1:0] = 1 TRK2_V_OTP[1:0] = 2 TRK2_V_OTP[1:0] = 3	 — — — —	 1.2 1.8 3.3 5	 — — — —	V
$VMON_{TRK2\_OVTH\_RANGE}$	VMON_TRK2 overvoltage monitoring threshold range setting with VMON_TRK2_OVTH_OTP[3:0] bitfield	104.5	—	112	%
$VMON_{TRK2\_OVTH\_STEP}$	VMON_TRK2 overvoltage monitoring OTP threshold setting step	—	0.5	—	%
$VMON_{TRK2\_OVTH\_ACC}$	VMON_TRK2 overvoltage detection accuracy	-1	—	1	%
$VMON_{TRK2\_UVTH\_RANGE}$	VMON_TRK2 undervoltage monitoring threshold range setting with VMON_TRK2_UVTH_OTP[3:0] bitfield	88	—	95.5	%
$VMON_{TRK2\_UVTH\_STEP}$	VMON_TRK2 undervoltage monitoring OTP threshold setting step	—	0.5	—	%

Table 224. VMON_TRK2 monitoring electrical characteristics*...continued*

T_A = –40 °C to 125 °C, unless otherwise specified. $V_{SUP\_UVH} < V_{SUP} <$ 36 V, $V_{PRE\_PWM} + V_{PRE\_HDR} < V_{SUP\_PWR} <$ 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
$VMON_{TRK2\_UVTH\_ACC}$	VMON_TRK2 undervoltage detection accuracy	-1	—	1	%
Dynamic electrical characteristics					
$t_{VMON\_TRK2\_OV\_DGLT}$	VMON_TRK2 overvoltage deglitch time VMON_TRK2_OVDGLT_OTP = 0 VMON_TRK2_OVDGLT_OTP = 1	 20 40	 25 45	 30 50	µs
$t_{VMON\_TRK2\_UV\_DGLT}$	VMON_TRK2 undervoltage deglitch time VMON_TRK2_UVDGLT_OTP[1:0] = 0 VMON_TRK2_UVDGLT_OTP[1:0] = 1 VMON_TRK2_UVDGLT_OTP[1:0] = 2 VMON_TRK2_UVDGLT_OTP[1:0] = 3	 2.5 10 20 35	 5 15 25 40	 7.5 20 30 45	µs

22.8.7 VMON_REF: VREF monitoring

Because of an internal dedicated connection to the VREF pin, the FS2630 can detect faults on the VREF output voltage. Both overvoltage and undervoltage conditions can be detected.

To support various system configurations, VMON_REF monitoring can be activated, or not activated, with an OTP bit. Also, to support both output voltages of the VREF, an OTP bit is available to set the target voltage value to monitor. To fit multiple system requirements, a wide range of upper and lower thresholds can be selected with OTP bits.

To allow flexibility in the application, reactions to both overvoltage and undervoltage faults are configurable with VMON_REF_OV_FS_REACTION[1:0] and VMON_REF_UV_FS_REACTION[1:0] bits during the *initialization phase*.

The monitoring is able to report UV/OV flags as soon as the power-up sequence is completed and the *enable monitoring* state is reached.

To reach ASIL D at the VREF pin level, the pin lift detection mechanism must be activated using the VREF_PLIFT_DIS_OTP bit.

If the VREF pin is disconnected, the VREF output voltage will be pulled to LDOIN pin within $t_{REF\_PINLIFT}$ and will create an overvoltage, and the device will react according to VMON_REF_OV_FS_REACTION[1:0]. A minimum headroom $V_{TRKIN\_MIN\_PINLIFT}$ is mandatory to guarantee the pin lift detection.

Table 225. VMON_REF overvoltage reaction configuration

VMON_REF_OV_FS_REACTION[1:0]	Overvoltage faults reaction
0	No action on Safety Output(s) and RSTB
1	An overvoltage detection asserts safety output(s) only
2 (default) 3	**An overvoltage detection asserts safety output(s) and RSTB**

Table 226. VMON_REF undervoltage reaction configuration

VMON_REF_UV_FS_REACTION[1:0]	Undervoltage faults reaction
0	No action on Safety Output(s) and RSTB

Table 226. VMON_REF undervoltage reaction configuration*...continued*

VMON_REF_UV_FS_REACTION[1:0]	Undervoltage faults reaction
1 (default)	**An undervoltage detection asserts safety output(s) only**
2 3	An undervoltage detection asserts Safety output(s) and RSTB

Table 227. VMON_REF monitoring electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. $V_{SUP\_UVH} < V_{SUP} <$ 36 V, $V_{PRE\_PWM} + V_{PRE\_HDR} < V_{SUP\_PWR} <$ 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Static electrical characteristics					
$VMON_{REF\_V}$	VMON_REF monitoring target voltage setting VREF_V_OTP = 0 VREF_V_OTP = 1	 — —	 3.3 5.0	 — —	V
$V_{TRKIN\_MIN\_PINLIFT}$	Minimum headroom to guarantee VREF pin lift detection	$VMON_{REF\_V}$ x (@VMON_REF_OVTH_OTP[3:0] + 1 %) + 0.5 V	—	—	V
$VMON_{REF\_OVTH\_RANGE}$	VMON_REF overvoltage monitoring threshold range setting with VMON_REF_OVTH_OTP[3:0] bits	104.5	—	112	%
$VMON_{REF\_OVTH\_STEP}$	VMON_REF overvoltage monitoring OTP threshold setting step	—	0.5	—	%
$VMON_{REF\_OVTH\_ACC}$	VMON_REF overvoltage detection accuracy	-1	—	1	%
$VMON_{REF\_UVTH\_RANGE}$	VMON_REF undervoltage monitoring threshold range setting with VMON_REF_UVTH_OTP[3:0] bits	88	—	95.5	%
$VMON_{REF\_UVTH\_STEP}$	VMON_REF undervoltage monitoring OTP threshold setting step	—	0.5	—	%
$VMON_{REF\_UVTH\_ACC}$	VMON_REF undervoltage detection accuracy	-1	—	1	%
Dynamic electrical characteristics					
$t_{VMON\_REF\_OV\_DGLT}$	VMON_REF overvoltage deglitch time VMON_REF_OVDGLT_OTP = 0 VMON_REF_OVDGLT_OTP = 1	 20 40	 25 45	 30 50	µs
$t_{VMON\_REF\_UV\_DGLT}$	VMON_REF undervoltage deglitch time VMON_REF_UVDGLT_OTP[1:0] = 0 VMON_REF_UVDGLT_OTP[1:0] = 1 VMON_REF_UVDGLT_OTP[1:0] = 2 VMON_REF_UVDGLT_OTP[1:0] = 3	 2.5 10 20 35	 5 15 25 40	 7.5 20 30 45	µs
$t_{VMON\_REF\_PINLIFT}$	VMON_REF monitoring VREF pin lift detection time	—	—	5	ms

22.8.8 VMON_EXT: external monitoring input

VMON_EXT is a FS2630 block dedicated to monitor an external voltage from another device inside the application thougth VMONEXT pin. Both overvoltage and undervoltage conditions can be detected.

The expected voltage value on VMONEXT pin is fixed and a proper resistor bridge to downscale it shall be provided externally. The overvoltage threshold is set with VMON_EXT_OVTH_OTP[3:0] bitfield and the undervoltage threshold is set with VMON_EXT_UVTH_OTP[3:0] bitfield.

To allow flexibility in the application, reactions to both overvoltage and undervoltage faults are configurable with the VMON_EXT_OV_FS_REACTION[1:0] and VMON_EXT_UV_FS_REACTION[1:0] bits during the *initialization phase*. If a 'short to high' type of fault on VMON_EXT should not impact RSTB, NXP recommends configuring VMON_EXT_OV_FS_REACTION[1:0] = 1 before turning ON the external regulator.

The monitoring is able to report UV/OV flags as soon as the power-up sequence is completed and the *enable monitoring* state is reached.

Table 228. VMON_EXT overvoltage reaction configuration

VMON_EXT_OV_FS_REACTION[1:0]	Overvoltage faults reaction
0	No action on Safety Output(s) and RSTB
1	An overvoltage detection asserts safety output(s) only
2 (default) 3	**An overvoltage detection asserts safety output(s) and RSTB**

Table 229. VMON_EXT undervoltage reaction configuration

VMON_EXT_UV_FS_REACTION[1:0]	Undervoltage faults reaction
0	No action on Safety Output(s) and RSTB
1 (default)	**An undervoltage detection asserts safety output(s) only**
2 3	An undervoltage detection asserts Safety output(s) and RSTB

Table 230. VMON_EXT monitoring electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. $V_{SUP\_UVH} < V_{SUP} < 36$ V, $V_{PRE\_PWM} + V_{PRE\_HDR} < V_{SUP\_PWR} < 36$ V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
	Static electrical characteristics				
$VMON_{EXT\_CFG}$	VMON_EXT monitoring target voltage setting (voltage between VMONEXT pin and ground)	—	0.8	—	V
$VMON_{EXT\_OVTH\_RANGE}$	VMON_EXT overvoltage monitoring threshold range setting with VMON_EXT_OVTH_OTP[3:0] bitfield	104.5	—	112	%
$VMON_{EXT\_OVTH\_STEP}$	VMON_EXT overvoltage monitoring OTP threshold setting step	—	0.5	—	%
$VMON_{EXT\_OVTH\_ACC}$	VMON_EXT overvoltage detection accuracy	-1.2	—	1.2	%
$VMON_{EXT\_UVTH\_RANGE}$	VMON_EXT undervoltage monitoring threshold range setting with VMON_EXT_UVTH_OTP[3:0] bitfield	88	—	95.5	%
$VMON_{EXT\_UVTH\_STEP}$	VMON_EXT undervoltage monitoring OTP threshold setting step	—	0.5	—	%
$VMON_{EXT\_UVTH\_ACC}$	VMON_EXT undervoltage detection accuracy	-1.2	—	1.2	%
R_{MONEXT_PD}	Internal pull-down resistor on VMONEXT pin	1	2	4	MΩ

Table 230. VMON_EXT monitoring electrical characteristics*...continued*

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < V_{SUP} < 36 V, V_{PRE_PWM} + V_{PRE_HDR} < V_{SUP_PWR} < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Dynamic electrical characteristics					
$t_{VMON\_EXT\_OV\_DGLT}$	VMON_EXT overvoltage deglitch time VMON_EXT_OVDGLT_OTP = 0 VMON_EXT_OVDGLT_OTP = 1	 20 40	 25 45	 30 50	µs
$t_{VMON\_EXT\_UV\_DGLT}$	VMON_EXT undervoltage deglitch time VMON_EXT_UVDGLT_OTP[1:0] = 0 VMON_EXT_UVDGLT_OTP[1:0] = 1 VMON_EXT_UVDGLT_OTP[1:0] = 2 VMON_EXT_UVDGLT_OTP[1:0] = 3	 2.5 10 20 35	 5 15 25 40	 7.5 20 30 45	µs

22.9 ERRMON: external IC monitoring

To monitor another device (on top of the microcontroller) in the application, the WAKE2 pin can be configured as a digital input. This external IC monitoring feature is enabled by the OTP bit ERRMON_DIS_VOTP. When this feature is activated, the WAKE2 pin is used to monitor an external IC.

This monitoring is active as soon as the *initialization phase* is closed by the first good watchdog refresh. A transition detected at the WAKE2 pin indicates an error from the external IC.

The following parameters can be configured during FS2630 *initialization phase* to facilitate monitoring of an external IC in the application:

- The polarity of the fault signal is configurable with the ERRMON_FLT_POLARITY bit.
- The desired reaction on RSTB and safety output(s).
- The time allowed to the microcontroller for receiving error acknowledgment.

When an error is detected, the microcontroller should acknowledge the FS2630 device. If the acknowledgment is not received by the FS2630 within the predefined time, the FS2630 will assert its safety output(s) and the RSTB pin will react as defined during the *initialization phase*.

The following tables show the various SPI bits used by this external IC monitoring function:

Table 231. Signal polarity to detect an error on WAKE2 pin

ERRMON_FLT_POLARITY	Condition to detect a fault
0 (default)	**High to low level**
1	Low to high level

Table 232. Reaction when an error is detected WAKE2 pin

ERRMON_FS_REACTION	Reaction
0	Error on WAKE2 pin asserts safety output(s) only
1 (default)	**Error on WAKE2 pin asserts safety output(s) and RSTB**

Table 233. Allowed time to receive microcontroller acknowledge when an external IC error is detected

ERRMON_ACK_TIME[1:0]	Time allowed for acknowledgment
0	1 ms
1 (default)	**8 ms**
2	16 ms
3	32 ms

Table 234. Error flag for external IC monitoring

ERRMON bit	Error flag on WAKE 2
0	No error
1	Error detected. FS2630 is waiting for the MCU to acknowledge the error within the allowed time.

Table 235. Acknowledge error detection from MCU

ERRMON_ACK	Error flag on WAKE 2
0	No error
1	MCU acknowledgment timeout expired

The acknowledgment by the MCU is done through SPI communication according to Figure 60.

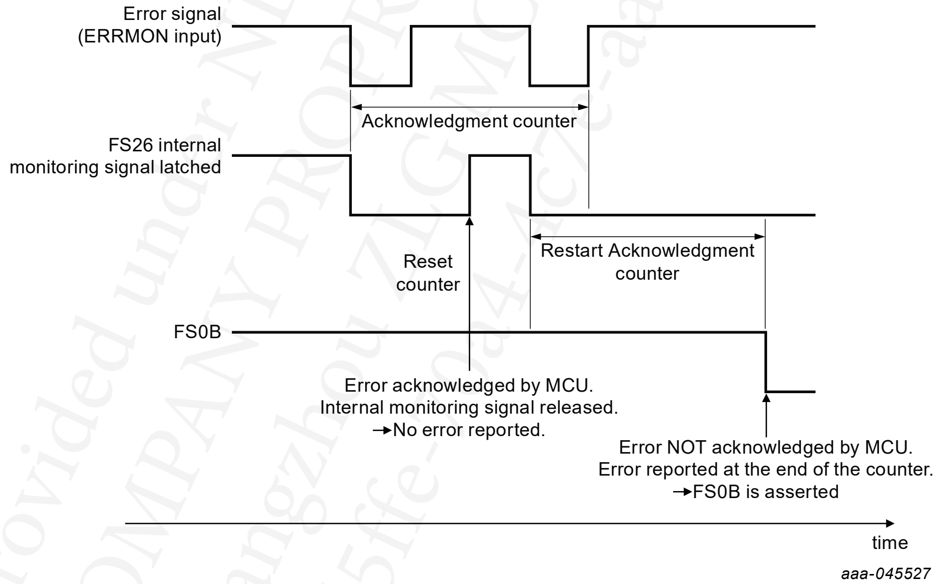

Figure 60. External IC monitoring timing diagram

Table 236. External IC monitoring electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < V_{SUP} < 36 V, V_{PRE_PWM} + V_{PRE_HDR} < V_{SUP_PWR} < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
	Electrical characteristics				
V_{IH_ERRMON}	High-level input voltage threshold	—	—	1.4	V
V_{IL_ERRMON}	Low-level input voltage threshold	0.5	—	—	V
$V_{IN\_HYS\_ERRMON}$	Threshold hysteresis	50	190	500	mV
t_{ERRMON_ERR}	Filtering time	4	—	8	µs
$t_{ERRMON\_ACK\_ACC}$	acknowledgment counter accuracy	-10	—	10	%
R_{PD_ERRMON}	ERRMON pull-down resistor value	100	200	320	kΩ

22.10 Fault management

22.10.1 Fault error counter

The FS26 integrates a configurable fault error counter which counts the number of faults related to the device itself, and also those caused by external events. The fault error counter starts at level "1" after a POR or when resuming from Low Power modes. The final value of the fault error counter is used to transition to DFS mode. The maximum value of this counter is configurable with the FLT_ERR_CNT_LIMIT[1:0] bits during the initialization phase.

Table 237. Fault error counter configuration

FLT_ERR_CNT_LIMIT[1:0]	Error counter maximum value	Error counter intermediate value
00	2	1
01 (default)	**6**	**3**
10	8	4
11	12	6

The fault error counter has two output values: intermediate and final. The intermediate value can be used to force the FS0B activation or to generate an RSTB pulse according to the FLT_ERR_REACTION[1:0] bits configuration.

Table 238. Fault error counter reaction configuration

FLT_ERR_REACTION[1:0]	Reaction
00	No effect on RSTB and FS0B
01	FS0B is asserted low if FLT_ERR_CNT[3:0] ≥ intermediate value
10 (default)	**RSTB and FS0B are asserted low if FLT_ERR_CNT[3:0] ≥ intermediate value**
11	RSTB and FS0B are asserted low if FLT_ERR_CNT[3:0] ≥ intermediate value

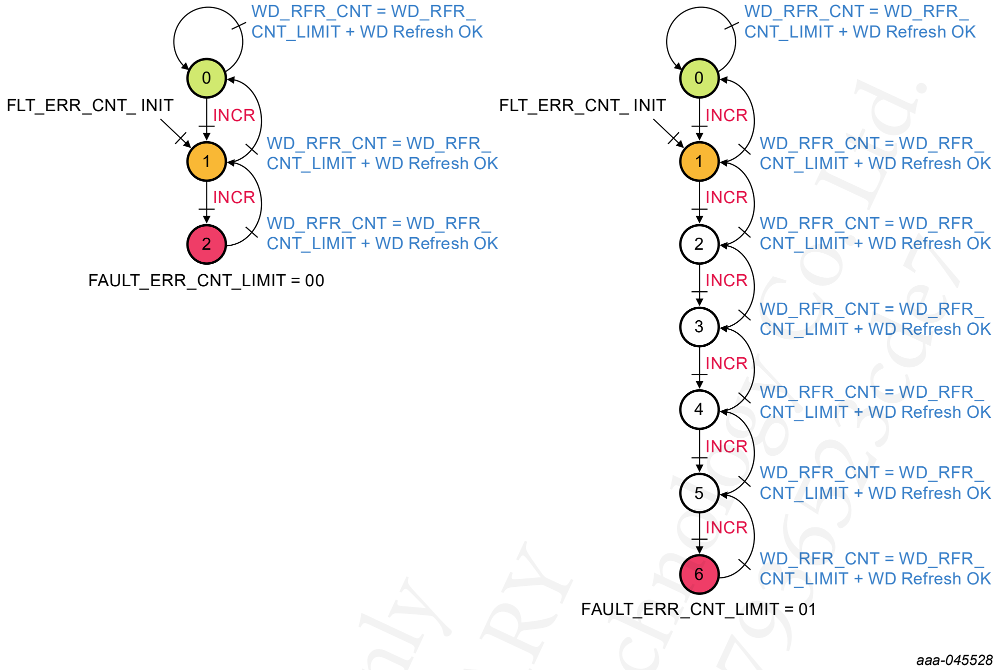

Figure 61. Fault error counter (FLT_ERR_CNT_LIMIT[1:0] = 00 or 01)

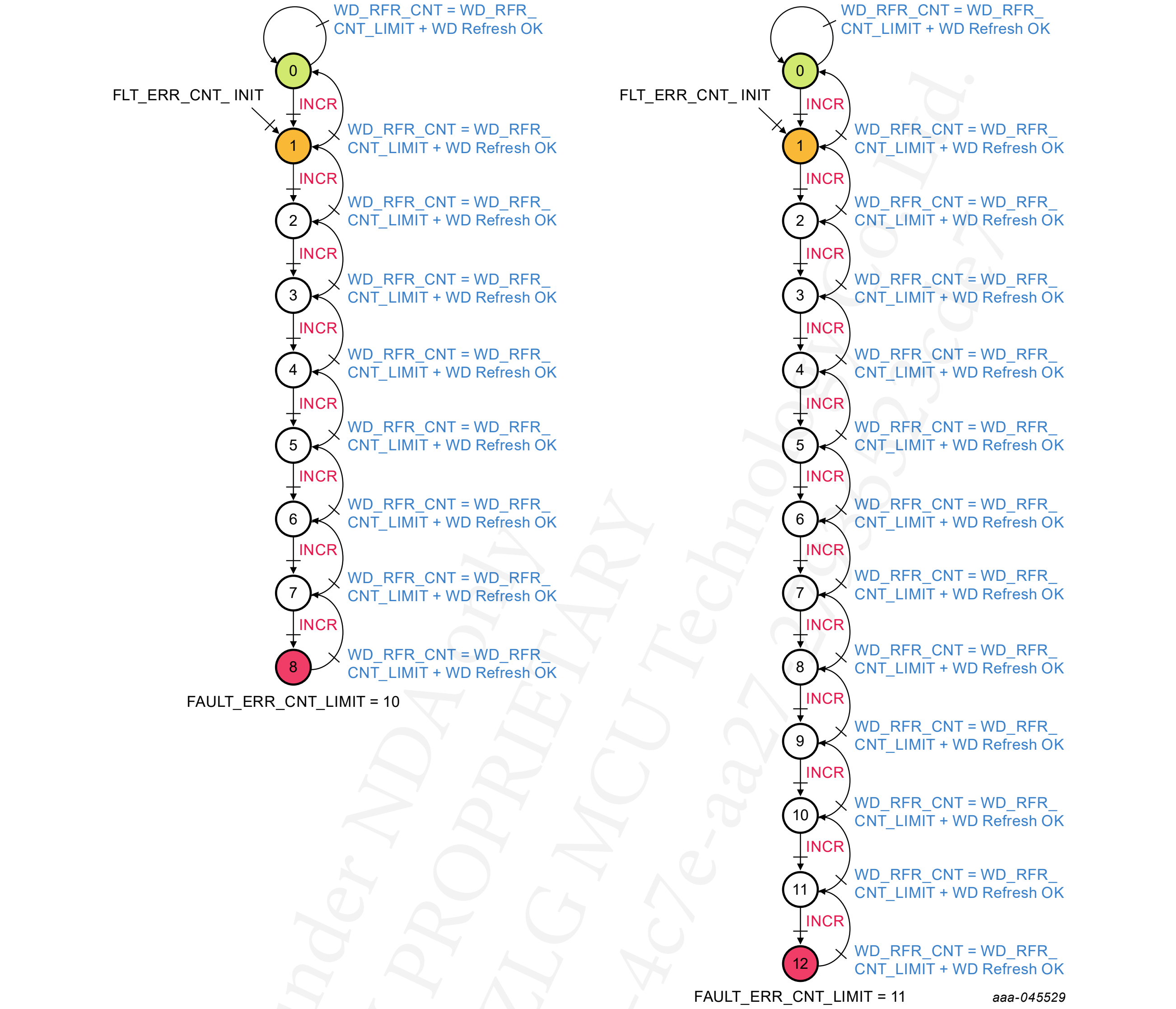

Figure 62. Fault error counter (FLT_ERR_CNT_LIMIT[1:0] = 10 or 11)

22.10.2 Fault sources and reactions

In *normal mode*, when FS0B and RSTB (and FS1B if used) are released, the fault error counter is incremented when a fault is detected by the FS2630 fail-safe state machine. Table 239 lists the faults and their impact on RSTB, FS0B and FS1B pins according to the device configuration. The faults that are configured to not assert RSTB and FS0B (and FS1B if used) will not increment the fault error counter. In that case, only the flags are available for MCU diagnostics. When FS0B is asserted, the fault error counter continues to be incremented by +1 each time the WD error counter reaches its maximum value. With default configuration, when FS0B is asserted, the fault error counter is not incremented by 1 in case of UV detection on a regulator. When a RSTB failure occurs, the fault error counter is increased by 1 and a new 256 ms watchdog window is opened.

Table 239. Application related fail-safe fault list and reaction

In orange, the reaction is not configurable.
In green, the reaction is configurable by SPI during the initialization phase.

Application related fail-safe faults	Fault error counter increment	FS0B assertion	RSTB assertion
VMON_PRE overvoltage	+1	VMON_PRE_OV_FS_REACTION[0]	VMON_PRE_OV_FS_REACTION[1]
VMON_CORE overvoltage	+1	VMON_CORE_OV_FS_REACTION[0]	VMON_CORE_OV_FS_REACTION[1]
VMON_LDO1 overvoltage	+1	VMON_LDO1_OV_FS_REACTION[0]	VMON_LDO1_OV_FS_REACTION[1]
VMON_LDO2 overvoltage	+1	VMON_LDO2_OV_FS_REACTION[0]	VMON_LDO2_OV_FS_REACTION[1]
VMON_TRK1 overvoltage	+1	VMON_TRK1_OV_FS_REACTION[0]	VMON_TRK1_OV_FS_REACTION[1]
VMON_TRK2 overvoltage	+1	VMON_TRK2_OV_FS_REACTION[0]	VMON_TRK2_OV_FS_REACTION[1]
VMON_REF overvoltage	+1	VMON_REF_OV_FS_REACTION[0]	VMON_REF_OV_FS_REACTION[1]
VMON_EXT overvoltage	+1	VMON_EXT_OV_FS_REACTION[0]	VMON_EXT_OV_FS_REACTION[1]
VMON_PRE undervoltage	+1	VMON_PRE_UV_FS_REACTION[0]	VMON_PRE_UV_FS_REACTION[1]
VMON_CORE undervoltage	+1	VMON_CORE_UV_FS_REACTION[0]	VMON_CORE_UV_FS_REACTION[1]
VMON_LDO1 undervoltage	+1	VMON_LDO1_UV_FS_REACTION[0]	VMON_LDO1_UV_FS_REACTION[1]
VMON_LDO2 undervoltage	+1	VMON_LDO2_UV_FS_REACTION[0]	VMON_LDO2_UV_FS_REACTION[1]
VMON_TRK1 undervoltage	+1	VMON_TRK1_UV_FS_REACTION[0]	VMON_TRK1_UV_FS_REACTION[1]
VMON_TRK2 undervoltage	+1	VMON_TRK2_UV_FS_REACTION[0]	VMON_TRK2_UV_FS_REACTION[1]
VMON_REF undervoltage	+1	VMON_REF_UV_FS_REACTION[0]	VMON_REF_UV_FS_REACTION[1]
VMON_EXT undervoltage	+1	VMON_EXT_UV_FS_REACTION[0]	VMON_EXT_UV_FS_REACTION[1]
An error is sent by the MCU on FCCU1 and FCCU2 pins (dual wire protocol)	+1	Yes	FCCU12_FS_REACTION
An error is sent by the MCU on FCCU1 pin (single wire protocol)	+1	Yes	FCCU1_FS_REACTION
An error is sent by the MCU on FCCU2 pin (single wire protocol)	+1	Yes	FCCU2_FS_REACTION
An external IC is driving to the error state the signal connected on ERRMON	+1	Yes	ERRMON_FS_REACTION
Watchdog error counter reaches its maximum value (WD_ERR_CNT[3:0] = @WD_ERR_ LIMIT[1:0])	+1	WD_FS_REACTION[0]	WD_FS_REACTION[1]
The fault error counter reaches its intermediate value: (@WD_ERR_LIMIT[1:0])/2	No	FLT_ERR_REACTION[0]	FLT_ERR_REACTION[1]
Wrong watchdog refresh in *initialization phase* state	+1	Yes	Yes
No watchdog refresh in *initialization phase*	+1	Yes	Yes
RSTB pin asserted externally	+1	No[1]	Yes (low externally)
RSTB pulse request by MCU	No	No[1]	Yes
RSTB short to high	+1	Yes	No (high externally)
FS0B short to high	+1	No (high externally)	BACKUP_SAFETY_PATH_FS0B
FS0B request by the MCU	No	Yes	No
FS1B short to high	+1	No	BACKUP_SAFETY_PATH_FS1B
FS1B request by the MCU	No	Yes	No
REG_CORRUPT = 1	+1	Yes	No
OTP_CORRUPT = 1	+1	Yes	No
GOTO_INIT request by MCU	No	No[1]	No

[1] By cascaded effect, the FS0B is asserted low in *initialization phase*.

22.11 Safety outputs (RSTB, FS0B, FS1B)

These two or three (depending on the product part number) safety output pins are meant to set the ECU in a protected and known safe state. All these safety outputs are active low, and the internal implementation is an open drain topology.

22.11.1 RSTB: output for MCU reset

RSTB is an open-drain output that can be connected in the application to the RESET of the MCU. RSTB requires an external pull-up resistor to VDDIO and a filtering capacitor to ground for immunity.

An internal pull-down R_{RSTB_PD} ensures an RSTB low level in *LPOFF mode*. RSTB remains high in *standby mode*.

An internal pull-up on the gate of the low-side MOS ensures an RSTB low level in case of logic failure. When RSTB is stuck low for more than t_{RSTB_8S}, the device transitions into *Deep Fail Safe* mode.

RSTB is asserted accordingly with [fault sources and reactions] configuration set during the *initialization phase*. When RSTB is asserted low, FS0B is also asserted low and remain asserted until [release conditions] are met.

RSTB is asserted low during t_{RSTB_PULSE} configured with RSTB_DUR bit.

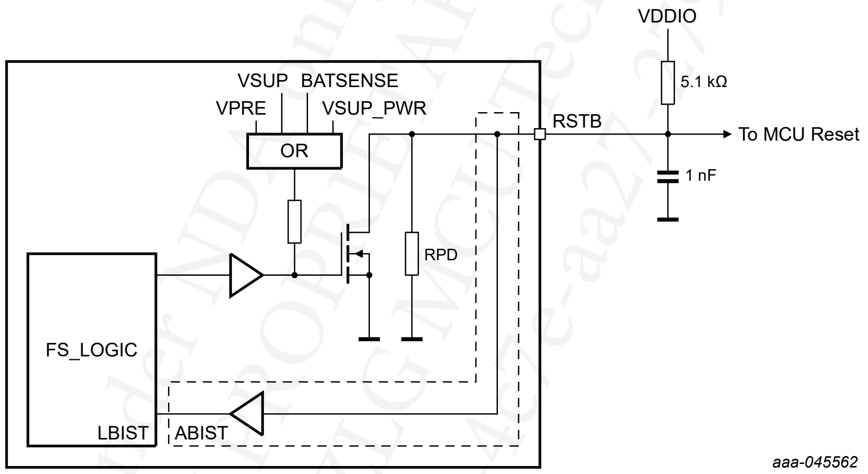

Figure 63. RSTB implementation

Table 240. RSTB electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. $V_{SUP\_UVH} < V_{SUP} < 36$ V, $V_{PRE\_PWM} + V_{PRE\_HDR} < V_{SUP\_PWR} < 36$ V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Static electrical characteristics					
V_{RSTB_IL}	RSTB low detection threshold	0	—	0.7	V
V_{RSTB_IH}	RSTB high detection threshold	1.5	—	—	V
V_{RSTB_HYS}	RSTB level detection hysteresis	100	—	300	mV
V_{RSTB_VOL}	RSTB low level output voltage (with I_{RSTB} = 2.0 mA)	—	—	0.4	V
R_{RSTB_PD}	RSTB internal pull-down resistor	200	400	800	kΩ
I_{RSTB_ILIM}	RSTB current limitation	4	—	22	mA
Dynamic electrical characteristics					

Table 240. RSTB electrical characteristics...*continued*

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < V_{SUP} < 36 V, V_{PRE_PWM} + V_{PRE_HDR} < V_{SUP_PWR} < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
t_{RSTB_FB}	RSTB sensing filtering time	8	—	15	µs
t_{RSTB_SHORT}	RSTB short to high detection timer	500	650	800	µs
t_{RSTB_PULSE}	RSTB pulse RSTB_DUR = 0 (long) RSTB_DUR = 1 (short)	 9 0.9	 — —	 11 1.1	ms
t_{RSTB_8S}	8 second timer to detect RSTB shorted to ground	7	8	9	s
$t_{RSTB\_RELEASE}$	Minimum time to release RSTB from POR - with all regulators started in Slot 0 - with TSLOT_OTP[1:0] = 0 - with SLOT_BYP_OTP[2:0] = 1 - with VPRE_SS_OTP[1:0] = 0 - with VBST_CFG_OTP = 1	—	5.5	7	ms

22.11.2 FS0B: safety output #0 pin

The purpose of this pin is to drive safe electrical circuitry independent from the MCU to deactivate the whole system and set the ECU in a protected and known state.

After each power-on reset or after each wake-up event (either from *standby mode* or *LPOFF mode*) the FS0B pin is asserted low. The MCU can release the FS0B pin when the application is ready to start. External pull-up circuitry must be connected to VDDIO or VSUP.

- If the pull-up is connected to VDDIO, the value recommended is 5.1 kΩ. There is no current in LPOFF, because VDDIO is off in *LPOFF mode*;
- If the pull-up is connected to VSUP, the value must be above 10 kΩ. There is a current in the pull-up resistor to consider at the application level in *LPOFF mode*.

The safety pins are asserted accordingly with fault sources and reactions configuration and remain asserted until release conditions are met.

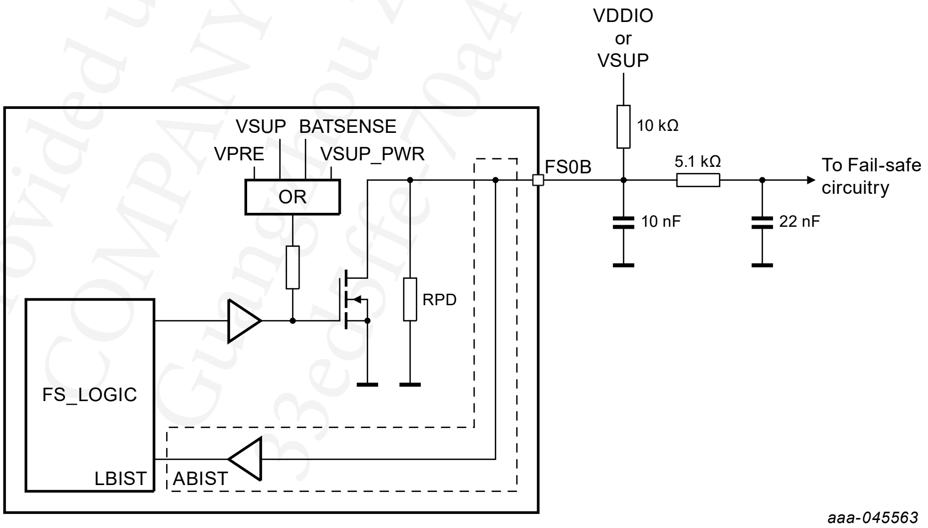

Figure 64. FS0B implementation

Table 241. FS0B electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. $V_{SUP\_UVH} < V_{SUP} <$ 36 V, $V_{PRE\_PWM} + V_{PRE\_HDR} < V_{SUP\_PWR} <$ 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Static electrical characteristics					
V_{FS0B_IL}	FS0B low detection threshold	0	—	0.7	V
V_{FS0B_IH}	FS0B high detection threshold	1.5	—	—	V
V_{FS0B_HYS}	FS0B level detection Hysteresis	100	—	300	mV
V_{FS0B_VOL}	FS0B low level output voltage (with I_{FS0B} = 2.0 mA)	—	—	0.4	V
R_{FS0B_PD}	FS0B internal pull-down resistor	1	2	4	MΩ
I_{FS0B_ILIM}	FS0B current limitation	4	—	22	mA
Dynamic electrical characteristics					
t_{FS0B_FB}	FS0B sensing filtering time	8	10	15	µs
t_{FS0B_SHORT}	FS0B short to high detection timer	500	650	800	µs

22.11.3 FS1B: safety output #1 pin

The FS1B pin is the secondary safety output pin. FS1B can either be asserted low with a configurable delay t_{DELAY} or duration t_{DUR} when FS0B is asserted low, or can behave exactly like FS0B. This pin can be used to:

- Open the phases of a motor after a configurable delay, starting when FS0B is asserted, to demagnetize the motor coils and reduce the inductive effect when the switch opens.
- Disable an external physical layer during a configurable duration, starting when FS0B is asserted, to avoid miscommunication when the module is in fail mode.
- Be a redundant safety output pin to FS0B when t_{DELAY} = 0. In this case, FS1B is asserted at the same time as FS0B.
- Any other use case where a second safety pin is needed.

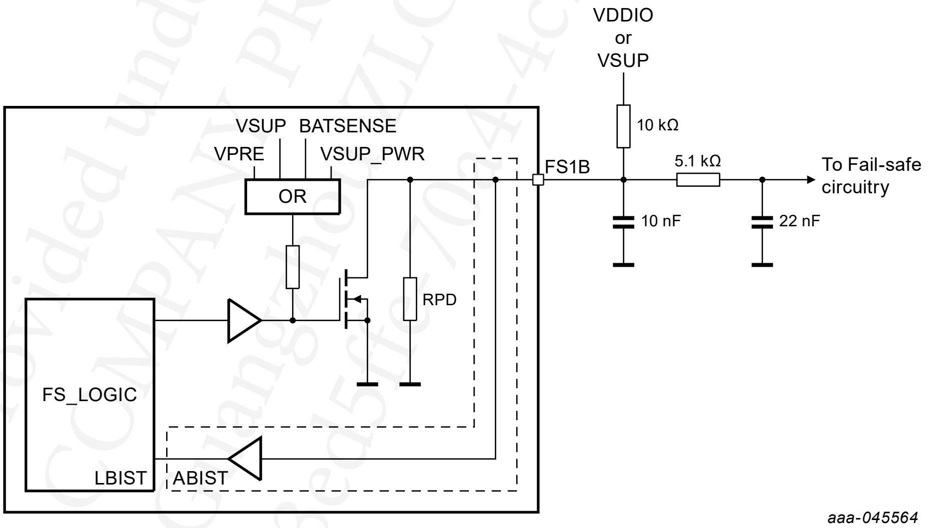

Figure 65. FS1B implementation

After each power-on reset or after each wake-up event (from *standby mode* or *LPOFF mode*) the FS1B pin is asserted low. Then the MCU can decide to release the FS1B pin when the application is ready to start. External pull-up circuitry connected to VSUP or VDDIO is mandatory.

To offer full flexibility to the system implementation, both t_{DELAY} and t_{DUR} are configurable through the FS_SAFE_IOS_2 register.

The FS1B_FS0B_EN_OTP bit impacts directly the FS1B pin assertion but also its release conditions.

If FS1B_FS0B_EN_OTP = 0:

- FS1B can be released when the FLT_ERR_CNT[3:0] ≠ 0.
- FS1B can be set low by a FS1B_REQ command and can be released without having FS0B asserted.

If FS1B_FS0B_EN_OTP = 1:

- FS1B cannot be released when FLT_ERR_CNT[3:0] ≠ 0.
- FS1B cannot be released before FS0B when FLT_ERR_CNT[3:0] = 0.
- FS0B has to be released at first but, when FS0B release command is executed, FS1B is released at the same time. It is not possible to release FS1B after FS0B.
- FS1B cannot be set low by a FS1B_REQ command, it will only be set low in case of a FS0B_REQ command.

Because of this flexibility, five use cases can be supported to fit perfectly with system requirements, as described below:

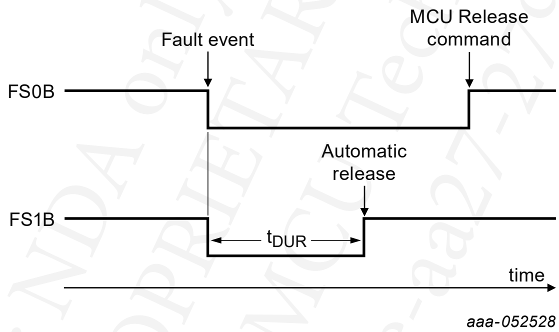

Figure 66. Use case 1: FS1B asserted when FS0B is asserted and released after t_{DUR} elapsed (FS1B_FS0B_EN_OTP = 0, FS1B_TDELAY[4:0] = 00h and FS1B_TDUR[4:0] ≠ 00h and 1Fh)

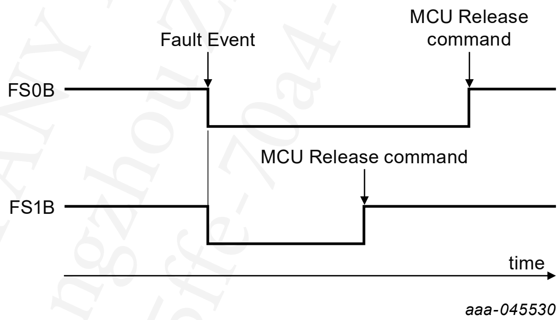

Figure 67. Use case 2: FS1B asserted when FS0B is asserted and released with MCU request (FS1B_FS0B_EN_OTP = 1, no impact from FS1B_TDELAY[4:0] and FS1B_TDUR[4:0] settings)

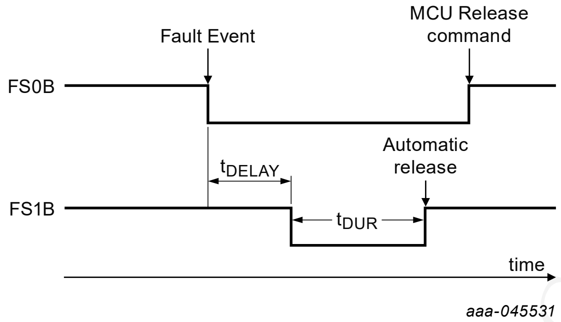

Figure 68. Use case 3: FS1B asserted with a delay after FS0B and released after t_{DUR} elapsed (FS1B_FS0B_EN_OTP = 0, FS1B_TDELAY[4:0] ≠ 00h and FS1B_TDUR[4:0] ≠ 00h and 1Fh)

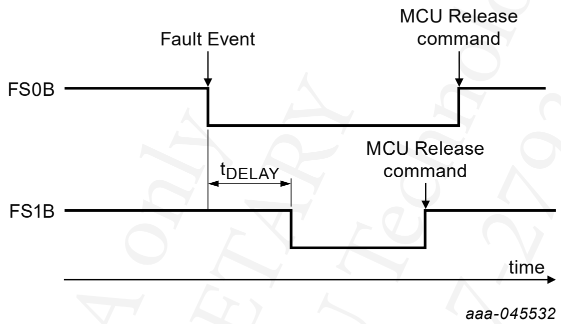

Figure 69. Use case 4: FS1B asserted with a delay after FS0B and released with MCU request (FS1B_FS0B_EN_OTP = 0, FS1B_TDELAY[4:0] ≠ 00h and FS1B_TDUR[4:0] = 1Fh)

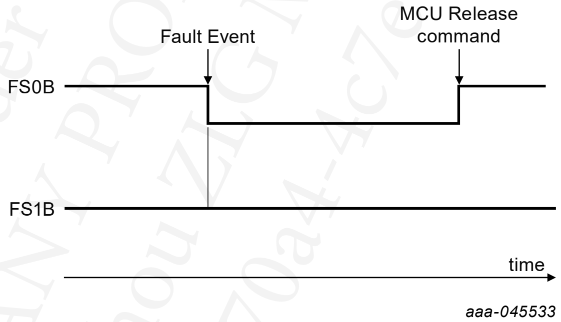

Figure 70. Use case 5: FS1B never asserted (FS1B_FS0B_EN_OTP = 0, FS1B_TDUR[4:0] = 00h)

When sending a GOTO_INIT SPI command (in the FS_SAFE_IOS_1 register), FS1B assertion and release will depend on FS1B_TDUR[4:0] and FS1B_TDELAY[4:0] settings. To avoid unexpected FS1B release during *initialization phase*, FS1B_TDUR[4:0] and FS1B_TDELAY[4:0] must be updated accordingly. When the FS2630 is requested to go into *LPOFF mode* or *standby mode*, transition timing and FS1B assertion will depend on the FS1B_TDUR[4:0] and FS1B_TDELAY[4:0] settings.

Going into *LPOFF mode*:

- If t_{DUR} = 0 s, FS1B_TDELAY[4:0] will not be taken into account, and the device will assert FS1B and go into *LPOFF mode* as soon as the 2nd SPI command is received and acknowledged.

- If 0 s < t_{DUR} < infinite, the transition into LPOFF will be delayed by t_{DELAY} + t_{DUR}, and FS1B will be asserted after t_{DELAY}. Regardless of the FS1B_TDUR[4:0] setting, FS1B will not be released.
- If t_{DUR} = infinite, the transition into LPOFF will be delayed only by t_{DELAY}, and FS1B will be asserted after t_{DELAY}.

Going into *standby mode*:

- If t_{DUR} = 0 s, FS1B_TDELAY[4:0] will not be taken into account, and the device will either assert FS1B or not (if pulled up to an active regulator in *standby mode*) and go into Standby as soon as the 2nd SPI command is received and acknowledged.
- If 0 s < t_{DUR} < infinite, the transition into *standby mode* will be delayed by t_{DELAY} + t_{DUR}, and FS1B will be asserted after t_{DELAY}. FS1B will then be released after t_{DUR}.
- If t_{DUR} = Infinite, transition into *standby mode* will be delayed by t_{DELAY} only and FS1B will be asserted after t_{DELAY}.

Figure 71, Figure 72, and Figure 73 describe the different behaviors possible when going into *standby mode* or *LPOFF mode*.

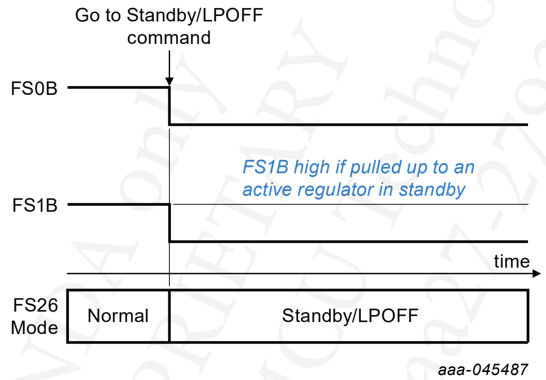

Figure 71. FS1B behavior: transition to *LPOFF mode* / *standby mode* when t_{DUR} = 0 s

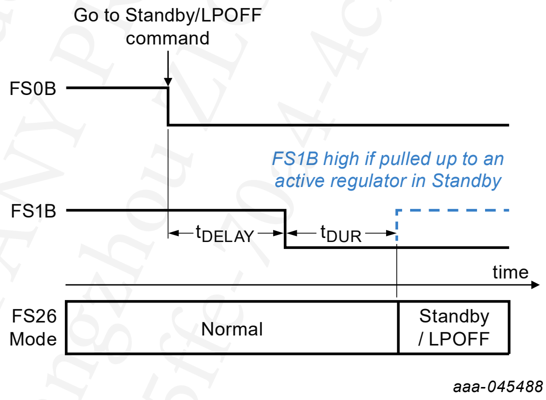

Figure 72. FS1B behavior: transition to *LPOFF mode* / *standby mode* when 0 s < t_{DUR} < infinite

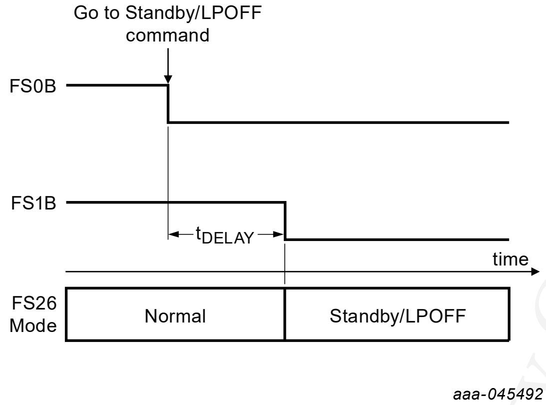

Figure 73. FS1B behavior: transition to *LPOFF mode* / *standby mode* when t_{DUR} = infinite

Table 242. FS1B electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. $V_{SUP\_UVH} < V_{SUP} < 36$ V, $V_{PRE\_PWM} + V_{PRE\_HDR} < V_{SUP\_PWR} < 36$ V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Static electrical characteristics					
V_{FS1B_IL}	FS1B low detection threshold	0	—	0.7	V
V_{FS1B_IH}	FS1B high detection threshold	1.5	—	—	V
V_{FS1B_HYS}	FS1B level detection Hysteresis	100	—	300	mV
V_{FS1B_VOL}	FS1B low level output voltage (with I_{FS1B} = 2.0 mA)	—	—	0.4	V
R_{FS1B_PD}	FS1B internal pull-down resistor	1	2	4	MΩ
I_{FS1B_ILIM}	FS1B current limitation	4	—	22	mA
Dynamic electrical characteristics					
t_{DELAY}	FS1B configurable assertion delay after FS0B assertion Typical value set on FS1B_TDELAY[4:0] bitfield	0	—	10.5	s
t_{DUR}	FS1B configurable assertion duration Typical value set on FS1B_TDUR[4:0] bitfield	0	—	—	s
t_{FS1B_FB}	FS1B sensing filtering time	8	10	15	µs
t_{FS1B_SHORT}	FS1B short to high detection timer	500	650	800	µs

22.11.4 Safety outputs release

When the safety output FS0B is asserted low by the device, the exit conditions must be validated before it allows this pin to be released. These conditions are:

- LBIST OK
- ABIST OK
- Fault is removed.
- Fault Error Counter = 0
- SPI write to RELEASE_FS0B_FS1B [15:0] register

When the safety output FS1B is asserted low by the device, the exit conditions must be validated before it allows this pin to be released. These conditions are:

- Fault is removed (only if FS1B_FS0B_EN_OTP = 1)
- SPI write to RELEASE_FS0B_FS1B [15:0] register

The procedure to compute the RELEASE_FS0B_FS1B [15:0] value to release the safety outputs is described below, with Table 243 illustrating all these steps with an example:

1. Get the FS_WD_TOKEN value.
2. Swap MSB/LSB of the value get in step No. 1.
3. Invert all computed bits at step No. 2.
4. Write bits 12 to 0 computed in step No. 3 into RELEASE_FS0B_FS1B [12:0] register. Bits 15 to 13 are used to select the safety output(s) to release as shown in Table 244.

Table 243. RELEASE_FS0B_FS1B bits code to release safety outputs

Step #1	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Read FS_WD_ TOKEN register	1	1	1	0	0	1	0	0	1	1	1	1	0	0	0	0
Step #2	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Reverse LSB/MSB	0	0	0	0	1	1	1	1	0	0	1	0	0	1	1	1
Step #3	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Complement bits	1	1	1	1	0	0	0	0	1	1	0	1	1	0	0	0
Step #4	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Write to RELEASE_ FS0B_FS1B[12:0]	**1**	**0**	**1**	1	0	0	0	0	1	1	0	1	1	0	0	0

Table 244. Bits 15 to 13 RELEASE_FS0B_FS1B register bit description

Bit	Symbol	Description	
15 to 13	RELEASE_FS0B_FS1B[15:13]	**Bits to select the desired safety output to release**	
		011	Release FS0B only
		110	Release FS1B only
		101	Release FS0B and FS1B

22.12 Built-in self-tests

To reduce latent faults, built-in self-tests are implemented in the functional safety circuitry. Both logical and analog areas can be checked when the device is powering up, or when it goes back to Normal mode from Low Power modes.

22.12.1 LBIST: logic built-in self-test

The fail-safe state machine includes a logic built-in self-test (LBIST) to verify the correct functionality of the safety logic circuitry. It is performed after each start-up of the device or after each wake-up from Low Power modes. In the case of an LBIST failure, RSTB is released, but FS0B remains low and cannot be released. The flag LBIST_OK is available through SPI for microcontroller diagnostics. The maximum LBIST duration is 3 ms. LBIST availability is dependent on part number. The microcontroller can check the LBIST status, using the LBIST_STATUS[1:0] SPI bits.

Table 245. LBIST SPI Flags bits

LBIST_STATUS[1:0]	LBIST Status
0	Reserved (Not used)
1	LBIST bypassed
2	LBIST fail
3	LBIST passed

22.12.2 ABIST1: analog built-in self-test

The fail-safe state machine includes one built-in self-test (BIST) to verify the correct functionality of the safety analog circuitry. The analog BIST (ABIST) is executed automatically when the device is powered on, or after each transition from Low Power modes to *normal mode*. This self-test checks all the voltage comparators that are used to detect undervoltage and overvoltage faults. It also checks, via a dedicated sense path, the voltage level of the safety output(s) pin(s) and compares it (or them) to the logic control. This self-test between logic control and voltage on the pin is also done for the RSTB pin.

In the case of ABIST failure, RSTB is released, but FS0B remains low and cannot be released. To support various system configurations, ABIST can be activated or deactivated via OTP bits. The ABIST coverage is detailed in the safety manual.

22.12.3 ABIST2: analog built-in self-test on demand

On top of the ABIST launched when the device is starting up, self-test of voltage monitoring comparators can be requested by the microcontroller. This request is accessible via a SPI request as soon as the FS2630 is in *normal mode*. ABIST on demand allows checking of the latent fault time interval during Normal operation, and not only at power-up sequence. This feature is available for specific part numbers. To launch this check, the microcontroller must select which monitoring has to be checked. Then, with a single SPI access, the check sequence launches. The result of this self-test is available via SPI on one bit.

Table 246. ABIST on demand for VMON_PRE monitoring SPI enable bits

ABIST2_VPRE	ABIST on demand request
0	Not requested
1	Requested

Table 247. ABIST on demand for VMON_CORE monitoring SPI enable bits

ABIST2_CORE	ABIST on demand request
0	Not requested
1	Requested

Table 248. ABIST on demand for VMON_LDO1 monitoring SPI enable bits

ABIST2_LDO1	ABIST on demand request
0	Not requested
1	Requested

Table 249. ABIST on demand for VMON_LDO2 monitoring SPI enable bits

ABIST2_LDO2	ABIST on demand request
0	Not requested
1	Requested

Table 250. ABIST on demand for VMON_TRK1 monitoring SPI enable bits

ABIST2_TRK1	ABIST on demand request
0	Not requested
1	Requested

Table 251. ABIST on demand for VMON_TRK2 monitoring SPI enable bits

ABIST2_TRK2	ABIST on demand request
0	Not requested
1	Requested

Table 252. ABIST on demand for VMON_REF monitoring SPI enable bits

ABIST2_REF	ABIST on demand request
0	Not requested
1	Requested

Table 253. ABIST on demand for VMON_EXT monitoring SPI enable bits

ABIST2_EXT	ABIST on demand request
0	Not requested
1	Requested

Table 254. ABIST on demand launch SPI enable bits

LAUNCH_ABIST2	ABIST on demand sequence launch
0	No action
1	Start ABIST on demand sequence

Table 255. ABIST on demand status SPI status bits

ABIST2_DONE	ABIST status
0	Self-test on going
1	Self-test sequence completed

Table 256. ABIST on demand result SPI status bits

ABIST2_PASS	ABIST result
0	Self-test failed or not executed
1	Self-test passed

Table 257. ABIST coverage

Monitoring	Overvoltage	Undervoltage	Short to high	ABIST1	ABIST2
VMON_PRE	X[1]	X		OTP[2]	SPI request[3]
VMON_CORE	X	X		OTP	SPI request
VMON_TRK1	X	X		OTP	SPI request
VMON_TRK2	X	X		OTP	SPI request
VMON_LDO1	X	X		OTP	SPI request
VMON_LDO2	X	X		OTP	SPI request
VMON_REF	X	X		OTP	SPI request
VMON_EXT	X	X		OTP	SPI request
VANA_FS and VDIG_FS	X			X	
RSTB			X	X	
FS0B			X	X	
FS1B			X	X	

[1] Means the check of the monitoring is done
[2] Means the check of the monitoring can be configured by OTP
[3] Means the check of the monitoring can be requested by SPI

Table 258. ABIST1 and ABIST2 electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. $V_{SUP\_UVH} < V_{SUP} <$ 36 V, $V_{PRE\_PWM} + V_{PRE\_HDR} < V_{SUP\_PWR} <$ 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Electrical characteristics					
t_{ABIST1_DUR}	ABIST1 duration • MIN with no voltage monitoring assigned by OTP • MAX with all voltage monitoring assigned by OTP	50	—	300	µs
t_{ABIST2_DUR}	ABIST2 duration • MIN with no voltage monitoring assigned by SPI • MAX with all voltage monitoring assigned by SPI	50	—	300	µs

23 OTP and Debug mode

OTP mode and Debug mode are intended for use during the development process, not in production applications or vehicles. OTP mode is intended for OTP emulation and OTP programming.

When an OTP configuration is emulated, the configuration remains available until the POR_M / POR_FS of the digital circuitry. The fail-safe configuration is lost in low power mode (*LPOFF mode* and *standby mode*) since the fail-safe digital is OFF in these modes.

The main digital configuration is lost when VSUP is removed, which means $V_{BOS} < V_{BOS\_POR}$. When an OTP configuration is programmed, the device will start with the programmed OTP configuration by default. A programmed part cannot be re-programmed, but can be emulated. To enter OTP mode, the voltage at the DEBUG pin must be set to V_{OTP} prior to applying VSUP voltage.

During the power-up sequence, the main and the fail-safe state machines will stop prior to starting the regulators, waiting for SPI communication to send an OTP configuration to the device. When the OTP configuration is complete, the fail-safe state machine will start in Debug mode when the voltage at the DEBUG pin is below V_{NORM_MAX} (NXP recommends applying 0 V or ground).

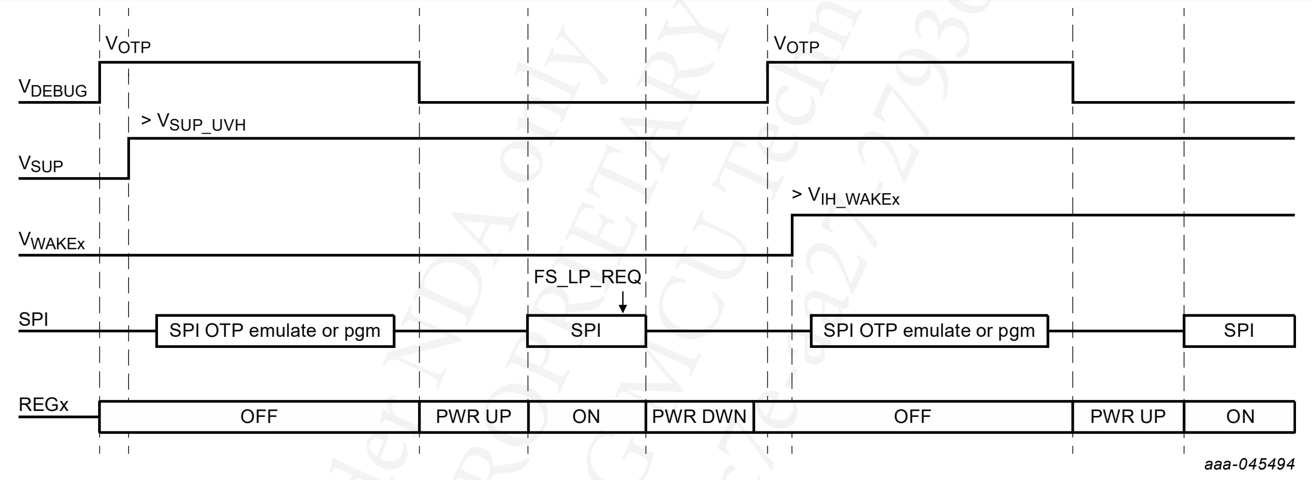

Figure 74. OTP mode time chart

Debug mode is intended for software debugging or first MCU programming during ECU assembly. To enter Debug mode without first entering OTP mode, the voltage at the DEBUG pin must be set to V_{DBG} prior to applying the VSUP voltage. During the power-up sequence, the fail-safe state machine will start in Debug mode and reach the *initialization phase*.

In Debug mode, the watchdog window is infinite opened, the RSTB 8 s counter is disabled, FS0B is maintained low and cannot be released. The *Deep Fail Safe* is deactivated. The Debug mode status is reported by the DBG_MODE bit in FS_STATES register (latched information) or by VDBG_VOLT_S in M_STATUS (real time information). To exit Debug mode, write to the EXIT_DBG_MODE bit in the FS_STATES register.

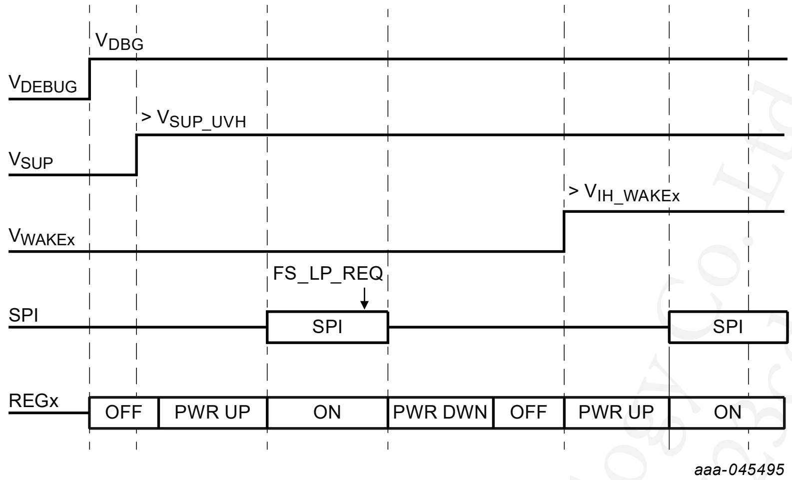

Figure 75. Debug mode time chart

Table 259. Electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. $V_{SUP\_UVH} < V_{SUP} < 36$ V, $V_{PRE\_PWM} + V_{PRE\_HDR} < V_{SUP\_PWR} < 36$ V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Electrical characteristics					
V_{NORM}	Voltage to apply at DEBUG pin to exit OTP mode and to start in *normal mode*	0	—	1.8	V
V_{OTP}	Voltage to apply at DEBUG pin to enter OTP mode (State machines stopped for OTP emulation/ programming)	7.4	—	8.4	V
V_{DBG}	Voltage to apply at DEBUG pin to enter *debug mode* (Automatic start in Debug mode with watchdog disabled)	2.5	—	6	V
t_{OTP_DBG}	DEBUG pin filtering time to enter OTP mode or *debug mode*	4	6	8	µs

23.1 OTP mode flowchart

The diagram in Figure 76 explains the steps to enter OTP mode, emulate or program an OTP configuration, start the Fail-safe machine in Debug mode, exit Debug mode with the watchdog disabled, and release the safety outputs.

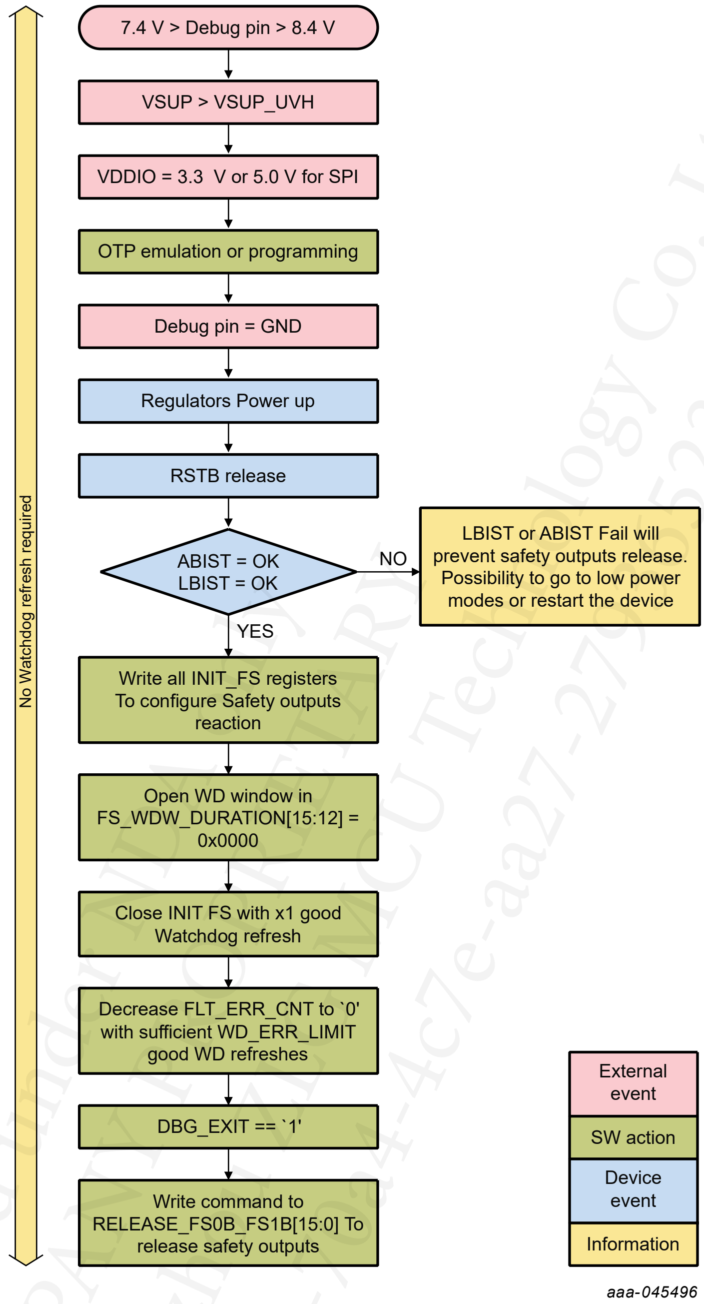

Figure 76. OTP mode flowchart until safety outputs release

23.2 Debug mode flowchart

The diagram in Figure 77 explains the steps to enter Debug mode without first entering OTP mode, start the fail-safe machine in Debug mode, exit Debug mode with the watchdog disabled, and release the safety outputs.

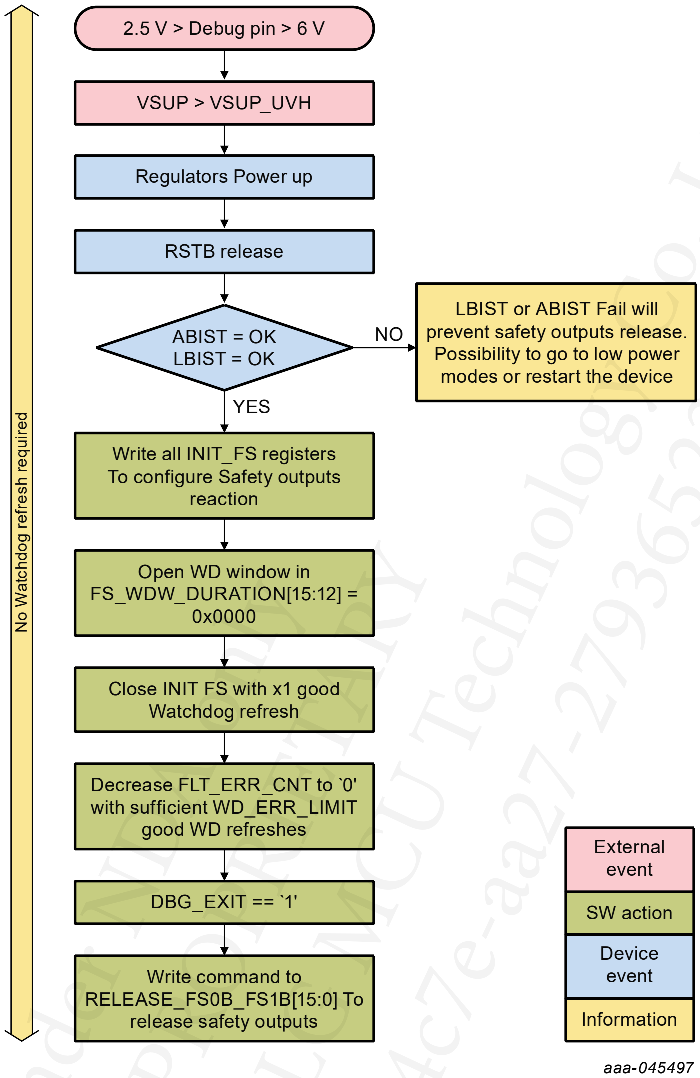

Figure 77. Debug mode flowchart till safety outputs release

24 Application schematics

Refer to AN12995 for further information.

24.1 Front-end configuration

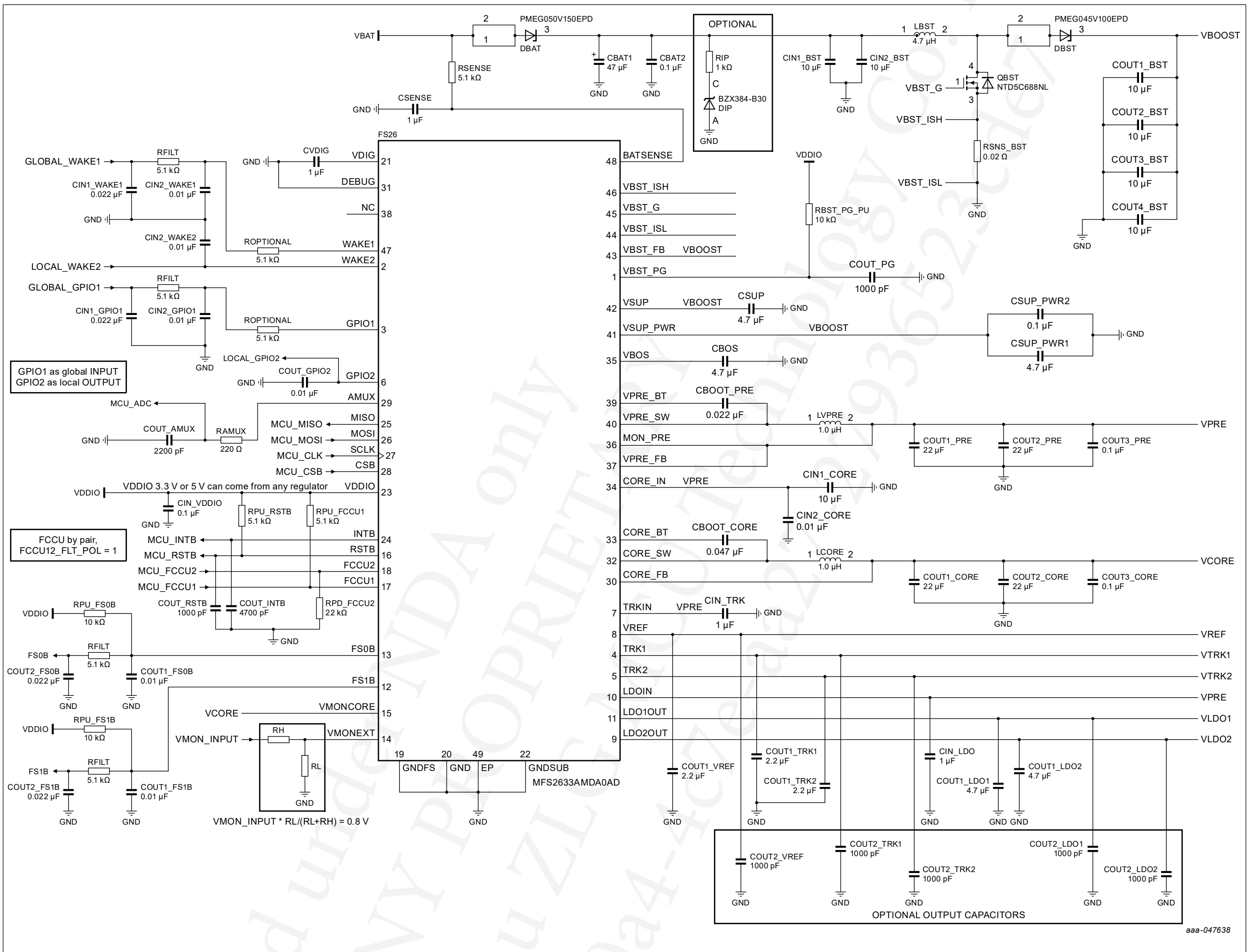

Figure 78. Application schematic in front-end configuration for F_{PRE} = 450 kHz

24.2 Back-end configuration

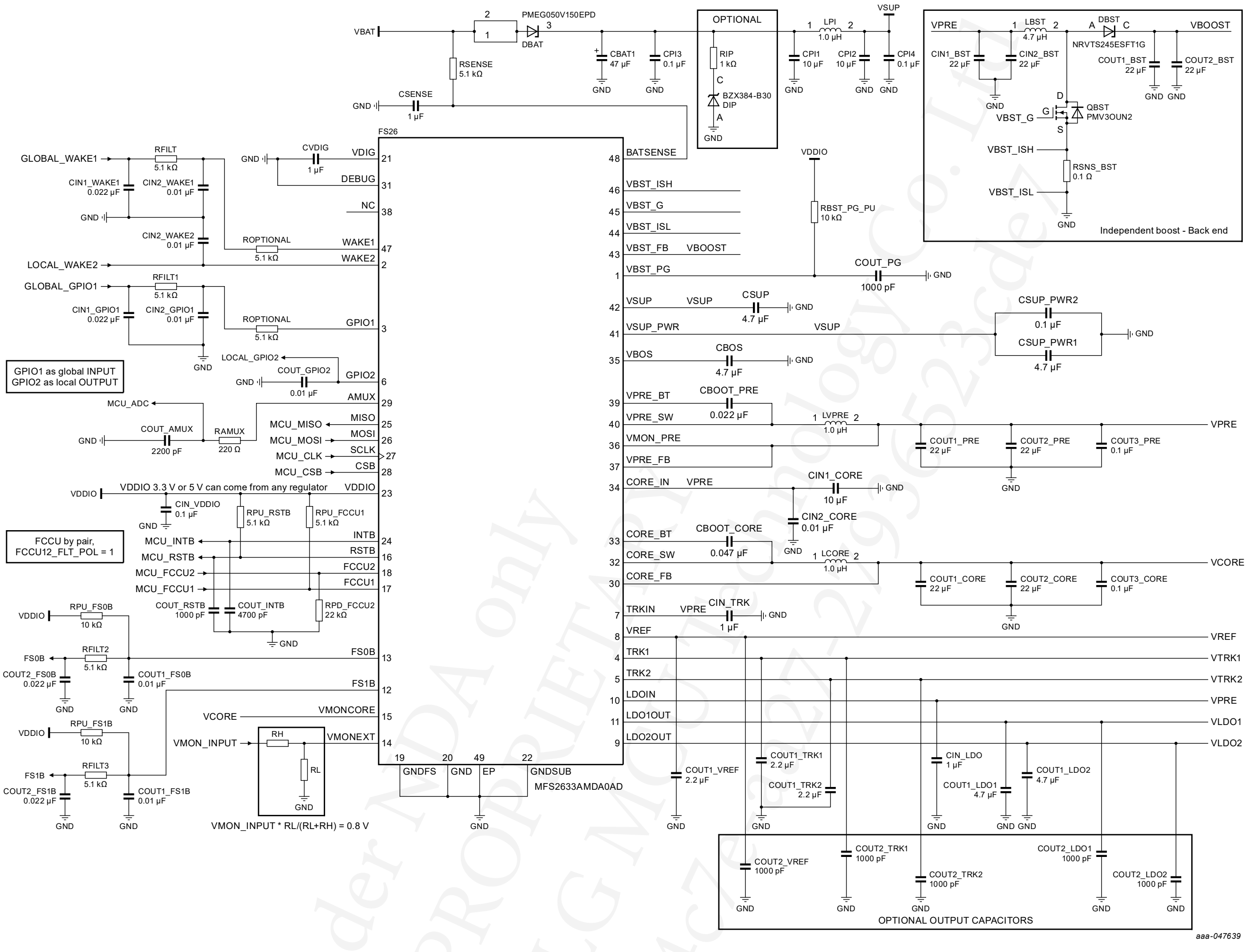

Figure 79. Application schematic in back-end configuration for F_{PRE} = 450 kHz

25 OTP configurations

Table 260. OTP configurations

	Register bitfield	Register description	MFS2613AMDA2AD	MFS2613AMDA3AD	MFS2613AMDA4AD	MFS2613AMDA6AD	MFS2621AMDABAD	MFS2613AMDDCAD
System configuration	VSUP_UVTH_OTP	VSUP UV threshold	4.8 V / 4.3 V	4.8 V / 4.3 V	4.8 V / 4.3 V	4.8 V / 4.3 V	4.8 V / 4.3 V	4.8 V / 4.3 V
	WK1DFS_DIS_OTP	Exit DFS on WAKE1 event	DFS exit on WAKE1 event enabled	DFS exit on WAKE1 event enabled	DFS exit on WAKE1 event enabled	DFS exit on WAKE1 event enabled	DFS exit on WAKE1 event enabled	DFS exit on WAKE1 event enabled
	RETRY_DIS_OTP	Auto-retry power-up from DFS	Auto-retry enabled	Auto-retry enabled	Auto-retry enabled	Auto-retry enabled	Auto-retry enabled	Auto-retry enabled
	RETRY_MODE_OTP	Auto-retry mode	Infinite retry	Infinite retry	Limited retry	Limited retry	Infinite retry	Limited retry
	RETRY_MSK_OTP[3:0]	Auto-retry timer limit	800 ms	800 ms	800 ms	800 ms	1600 ms	800 ms
	CLK_FREQ_OTP[1:0]	Clock frequency selection	18 MHz	18 MHz	18 MHz	18 MHz	18 MHz	18 MHz
	BOS_IN_OTP[1:0]	VBOS input selection	Auto Transition on V_{PRE_UVH}	Auto Transition on V_{PRE_UVH}	Auto Transition on V_{PRE_UVH}	Auto Transition on V_{PRE_UVH}	Auto Transition on V_{PRE_UVH}	Auto Transition on V_{PRE_UVH}
Power-up sequence	TSLOT_OTP[1:0]	Power-up slot time	250 µs	250 µs	250 µs	250 µs	1000 µs	250 µs
	SLOT_BYP_OTP[2:0]	Power-up slot bypass	Bypass disabled	Bypass disabled	Bypass disabled	Bypass disabled	Bypass disabled	Bypass disabled
	CORE_SLOT_OTP[2:0]	VCORE power-up slot	Slot 0	Slot 0	Slot 0	Slot 0	Slot 6	Slot 0
	LDO1_SLOT_OTP[2:0]	LDO1 power-up slot	Slot 0	Slot 0	Slot 0	Slot 0	Slot 0	Slot 0
	LDO2_SLOT_OTP[2:0]	LDO2 power-up slot	Slot 0	Slot 1	Slot 0	Slot 0	Slot 0	Slot 0
	TRK1_SLOT_OTP[2:0]	TRK1 power-up slot	Slot 2	Slot 2	Slot 2	Slot 0	Slot 0	Slot 2
	TRK2_SLOT_OTP[2:0]	TRK2 power-up slot	Slot 3	Slot 3	Slot 3	Slot 0	OFF	Slot 3
	VREF_SLOT_OTP[2:0]	VREF power-up slot	Slot 1	Slot 0	Slot 1	Slot 0	Slot 0	Slot 1
	GPIO1_SLOT_OTP[2:0]	GPIO1 power-up slot	OFF	Slot 4	OFF	OFF	Slot 1	OFF
	GPIO2_SLOT_OTP[2:0]	GPIO2 power-up slot	OFF	Slot 4	OFF	OFF	Slot 1	OFF
I/O configuration	GPIO1STAGE_OTP[1:0]	GPIO configuration	GPIO configured as an input	Push-pull driver	GPIO configured as an input	GPIO configured as an input	Low-side Driver	GPIO configured as an input
	GPIO1_MODE_OTP	GPIO low-side polarity	GPIO LS active high	GPIO LS active high	GPIO LS active high	GPIO LS active high	GPIO LS active high	GPIO LS active high
	GPIO1PU_OTP	GPIO1 pull-up	Pull-up disabled	Pull-up disabled	Pull-up disabled	Pull-up disabled	Pull-up disabled	Pull-up disabled
	GPIO1PD_OTP	GPIO1 pull-down	Pull-down enabled	Pull-down disabled	Pull-down disabled	Pull-down enabled	Pull-down enabled	Pull-down disabled
	GPIO1TH_OTP	GPIO1 detection threshold	Low-voltage threshold	Low-voltage threshold	Low-voltage threshold	Low-voltage threshold	High-voltage threshold	Low-voltage threshold
	GPIO1TSD_PD_OTP	GPIO1 TSD pull-down	Pull-down enabled in TSD	Pull-down enabled in TSD	Pull-down enabled in TSD	Pull-down enabled in TSD	Pull-down enabled in TSD	Pull-down enabled in TSD
	GPIO2STAGE_OTP[1:0]	GPIO configuration	Low-side driver	Push-pull driver	GPIO configured as an input	GPIO configured as an input	Low-side driver	GPIO configured as an input
	GPIO2_MODE_OTP	GPIO low-side polarity	GPIO LS active high	GPIO LS active high	GPIO LS active high	GPIO LS active high	GPIO LS active high	GPIO LS active high
	GPIO2_VCORE_PGOOD_OTP	GPIO2 VCORE PGOOD	GPIO is not driven by VCORE PGOOD	GPIO is not driven by VCORE PGOOD	GPIO is not driven by VCORE PGOOD	GPIO is not driven by VCORE PGOOD	GPIO is not driven by VCORE PGOOD	GPIO is not driven by VCORE PGOOD
	GPIO2PU_OTP	GPIO2 pull-up	Pull-up disabled	Pull-up disabled	Pull-up disabled	Pull-up disabled	Pull-up disabled	Pull-up disabled
	GPIO2PD_OTP	GPIO2 pull-down	Pull-down disabled	Pull-down disabled	Pull-down disabled	Pull-down enabled	Pull-down enabled	Pull-down disabled
	GPIO2TH_OTP	GPIO2 detection threshold	Low-voltage threshold	Low-voltage threshold	Low-voltage threshold	Low-voltage threshold	High-voltage threshold	Low-voltage threshold
	WK1TH_OTP	WAKE1 detection threshold	High-voltage threshold	Low-voltage threshold	High-voltage threshold	Low-voltage threshold	High-voltage threshold	High-voltage threshold
	WK2TH_OTP	WAKE2 detection threshold	High-voltage threshold	High-voltage threshold	High-voltage threshold	Low-voltage threshold	High-voltage threshold	High-voltage threshold

Table 260. OTP configurations*...continued*

	WK1PD_OTP	WAKE1 pull-down	Pull-down enabled	Pull-down enabled	Pull-down enabled	Pull-down enabled	Pull-down enabled	Pull-down enabled
	WK2PD_OTP	WAKE2 pull-down	Pull-down enabled	Pull-down enabled	Pull-down enabled	Pull-down enabled	Pull-down enabled	Pull-down enabled
	WK1PD_SEL_OTP	WAKE1 pull-down selection	200 kΩ	200 kΩ	200 kΩ	10 kΩ	200 kΩ	200 kΩ
	WK2PD_SEL_OTP	WAKE2 pull-down selection	200 kΩ	200 kΩ	200 kΩ	200 kΩ	200 kΩ	200 kΩ
VPRE configuration	VPRE_OTP[5:0]	VPRE in *normal mode*	6.00 V	5.40 V	6.00 V	6.00 V	6.00 V	6.00 V
	VPRE_LP_OTP[5:0]	VPRE in *standby mode*	5.35 V	5.35 V	5.35 V	5.35 V	5.35 V	5.35 V
	VPRE_LP_DVS_OTP[1:0]	DVS ramp rate	22 mV/µs	22 mV/µs	22 mV/µs	22 mV/µs	22 mV/µs	22 mV/µs
	VPRE_OC_OTP[2:0]	VPRE overcurrent flag	2.2 A	1.54 A	2.2 A	1.54 A	2.2 A	2.2 A
	VPRE_OC_DGLT_OTP[1:0]	Overcurrent deglitch	2000 µs	250 µs	2000 µs	250 µs	2000 µs	2000 µs
	VPRE_SS_OTP[1:0]	Soft-start ramp	2150 µs	538 µs	2150 µs	269 µs	2150 µs	2150 µs
	VPRE_PDWN_DLY_OTP[1:0]	VPRE power-down delay	100 µs	100 µs	100 µs	100 µs	100 µs	100 µs
	VPRE_BOS_OTP[5:0]	VPRE transition voltage	5.35 V	5.35 V	5.35 V	5.35 V	5.35 V	5.35 V
	VPRE_PH_OTP[1:0]	VPRE phase delay	No delay	No delay	No delay	No delay	No delay	No delay
	VPRE_SR_OTP	VPRE SW slew rate	Fast mode	Fast mode	Slow mode	Fast mode	Fast mode	Slow mode
	VPRE_GM_OTP[1:0]	Transconductance amp	15 µS	15 µS	15 µS	15 µS	15 µS	15 µS
	VPRE_CCOMP_OTP[1:0]	Comp capacitance	12.0 pF	23.0 pF	12.0 pF	12.0 pF	12.0 pF	12.0 pF
	VPRE_RCOMP_OTP[2:0]	Comp resistance	1300 kΩ	1137 kΩ	1300 kΩ	1300 kΩ	1300 kΩ	1300 kΩ
	VPRE_SC_OTP[5:0]	Slope compensation	266 mV/µs	266 mV/µs	266 mV/µs	266 mV/µs	266 mV/µs	266 mV/µs
	VPRE_PFM_TON_OTP[1:0]	HS minimum ON in PFM mode	1125 ns	1125 ns	1125 ns	1125 ns	1125 ns	1125 ns
	VPRE_PFM_TOFF_OTP[1:0]	HS minimum OFF in PFM mode	720 ns	720 ns	720 ns	720 ns	720 ns	720 ns
	VPRE_CLK_OTP	VPRE clock selection	FSW/40	FSW/40	FSW/40	FSW/40	FSW/40	FSW/40
	VPRETDFS_OTP	TSD behavior	Go to DFS	VPRE disabled only	Go to DFS	VPRE disabled only	Go to DFS	Go to DFS
	VPRETSD_PD_OTP	TSD pull-down	Pull-down enabled in TSD	Pull-down enabled in TSD	Pull-down enabled in TSD	Pull-down enabled in TSD	Pull-down enabled in TSD	Pull-down enabled in TSD
VBST configuration	VBST_OTP[4:0]	VBST voltage	8.00 V	7.00 V	8.00 V	8.00 V	8.00 V	8.00 V
	VBST_CFG_OTP	VBST configuration	Front-end boost	Front-end boost	Front-end boost	Front-end boost	Front-end boost	Front-end boost
	VBST_OV_OTP	VBST_FB overvoltage monitor mode	Auto-enable mode	Auto-enable mode	Auto-enable mode	Auto-enable mode	Auto-enable mode	Auto-enable mode
	VBST_PH_OTP[1:0]	Phase delay	1 Clock Cycle	1 Clock Cycle	1 Clock Cycle	1 Clock Cycle	1 Clock Cycle	1 Clock Cycle
	VBSTLS_SR_OTP	Low-side slew rate	PU = 1.5 Ω / PD = 1.0 Ω	PU = 1.5 Ω / PD = 1.0 Ω	PU = 1.5 Ω / PD = 1.0 Ω	PU = 2 Ω / PD = 1.7 Ω	PU = 1.5 Ω / PD = 1.0 Ω	PU = 1.5 Ω / PD = 1.0 Ω
	VBST_TON_MIN_OTP[1:0]	Minimum ON time	200 ns	200 ns	200 ns	200 ns	200 ns	200 ns
	VBST_SS_OTP[1:0]	VBST soft-start	425 µs	850 µs	425 µs	425 µs	425 µs	425 µs
	VBST_MAX_DC_OTP[1:0]	Max duty cycle	87.50 %	87.50 %	87.50 %	87.50 %	87.50 %	87.50 %
	VBST_CCOMP_OTP[1:0]	Comp capacitance	200 pF	200 pF	200 pF	200 pF	200 pF	200 pF
	VBST_GMCOMP_OTP[1:0]	Comp transconductance	3.9 µS	5.1 µS	3.9 µS	3.9 µS	3.9 µS	3.9 µS
	VBST_RCOMP_OTP[1:0]	Comp resistance	740 kΩ	500 kΩ	500 kΩ	740 kΩ	740 kΩ	500 kΩ
	VBST_ILIM_OTP[1:0]	Current limit	180 mV/RSNS	120 mV/RSNS	150 mV/RSNS	120 mV/RSNS	180 mV/RSNS	150 mV/RSNS
	VBST_SC_OTP[5:0]	Slope compensation	155 mV/µs	127 mV/µs	169 mV/µs	155 mV/µs	155 mV/µs	169 mV/µs

Table 260. OTP configurations*...continued*

VCORE configuration	VCORE_OTP[7:0]	VCORE voltage	1.50 V	1.50 V	1.50 V	1.50 V	1.25 V	1.50 V
	CORE_CTRL_OTP	Control type	Valley mode control	Valley mode control	Valley mode control	Valley mode control	Valley mode control	Valley mode control
	-	VCORE operating mode	CCM only	CCM only	CCM only	CCM only	CCM only	CCM only
	CORE_SS_OTP[1:0]	Soft-start	5 mV/µs	10 mV/µs	10 mV/µs	5 mV/µs	5 mV/µs	20 mV/µs
	CORE_ILIM_OTP[1:0]	VCORE current limit	2.7 A	2.7 A	1.7 A	1.7 A	2.7 A	1.7 A
	CORE_PH_OTP[1:0]	Phase delay	2 Clock Cycles	3 Clock Cycles	2 Clock Cycles	2 Clock Cycles	2 Clock Cycles	2 Clock Cycles
	COREHS_SR_OTP[1:0]	High-side slew rate	Rise = 4.5 V/ns Fall = 1.2 V/ns	Rise = 4.0 V/ns Fall = 0.6 V/ns	Rise = 4.5 V/ns Fall = 1.2 V/ns	Rise = 4.5 V/ns Fall = 1.2 V/ns	Rise = 4.5 V/ns Fall = 1.2 V/ns	Rise = 4.5 V/ns Fall = 1.2 V/ns
	CORE_GM_OTP[1:0]	Transconductance amp	53 µS	53 µS	26 µS	26 µS	53 µS	26 µS
	CORE_CCOMP_OTP[1:0]	Comp capacitance	50 pF	50 pF	50 pF	50 pF	50 pF	50 pF
	CORE_RCOMP_OTP[1:0]	Comp resistance	200 kΩ	150 kΩ	200 kΩ	200 kΩ	150 kΩ	200 kΩ
	CORE_LSEL_OTP[1:0]	VCORE inductor	1 µH	1 µH	1 µH	1 µH	1 µH	1 µH
	CORETDFS_OTP	TSD behavior	Go to DFS	Go to DFS	Go to DFS	Go to DFS	Go to DFS	Go to DFS
	CORETSD_PD_OTP	TSD pull-down	Pull-down enabled in TSD	Pull-down enabled in TSD	Pull-down enabled in TSD	Pull-down enabled in TSD	Pull-down enabled in TSD	Pull-down enabled in TSD
LDO1 configuration	VLDO1_OTP	LDO1 voltage in *normal mode*	5.0 V	3.3 V	5.0 V	5.0 V	5.0 V	5.0 V
	VLDO1_LP_OTP	LDO1 voltage in *standby mode*	5.0 V	3.3 V	5.0 V	5.0 V	5.0 V	5.0 V
	LDO1_LP_EN_OTP	LDO1 in *standby mode*	LDO1 enabled	LDO1 disabled	LDO1 enabled	LDO1 enabled	LDO1 enabled	LDO1 enabled
	LDO1TDFS_OTP	TSD behavior	LDO1 disabled only	LDO1 disabled only	LDO1 disabled only	LDO1 disabled only	LDO1 disabled only	LDO1 disabled only
	LDO1TSD_PD_OTP	TSD pull-down	Pull-down enabled in TSD	Pull-down enabled in TSD	Pull-down enabled in TSD	Pull-down enabled in TSD	Pull-down enabled in TSD	Pull-down enabled in TSD
LDO2 configuration	VLDO2_OTP	LDO2 voltage in *normal mode*	3.3 V	5.0 V	3.3 V	3.3 V	3.3 V	3.3 V
	VLDO2_LP_OTP	LDO2 voltage in *standby mode*	3.3 V	5.0 V	3.3 V	3.3 V	3.3 V	3.3 V
	LDO2_LP_EN_OTP	LDO2 in *standby mode*	LDO2 enabled	LDO2 enabled	LDO2 enabled	LDO2 enabled	LDO2 enabled	LDO2 enabled
	LDO2TDFS_OTP	TSD behavior	LDO2 disabled only	LDO2 disabled only	LDO2 disabled only	LDO2 disabled only	LDO2 disabled only	LDO2 disabled only
	LDO2TSD_PD_OTP	TSD pull-down	Pull-down enabled in TSD	Pull-down enabled in TSD	Pull-down enabled in TSD	Pull-down enabled in TSD	Pull-down enabled in TSD	Pull-down enabled in TSD
TRK1 configuration	TRK1_SEL_OTP[1:0]	TRK1 input selection	VREF	LDO2	Internal LDO_REF	VREF	VREF	Internal LDO_REF
	TRK1TDFS_OTP	TSD behavior	TRK1 disabled only	TRK1 disabled only	TRK1 disabled only	TRK1 disabled only	TRK1 disabled only	TRK1 disabled only
	TRK1TSD_PD_OTP	TSD pull-down	Pull-down enabled in TSD	Pull-down enabled in TSD	Pull-down enabled in TSD	Pull-down enabled in TSD	Pull-down enabled in TSD	Pull-down enabled in TSD
TRK2 configuration	TRK2_SEL_OTP[1:0]	TRK2 input selection	LDO2	LDO2	Internal LDO_REF	LDO2	VREF	Internal LDO_REF
	TRK2TDFS_OTP	TSD behavior	TRK2 disabled only	TRK2 disabled only	TRK2 disabled only	TRK2 disabled only	TRK2 disabled only	TRK2 disabled only
	TRK2TSD_PD_OTP	TSD pull-down	Pull-down enabled in TSD	Pull-down enabled in TSD	Pull-down enabled in TSD	Pull-down enabled in TSD	Pull-down enabled in TSD	Pull-down enabled in TSD
VREF configuration	VREF_OTP	VREF voltage	5.0 V	3.3 V	5.0 V	5.0 V	3.3 V	3.3 V
	VLDO_REF_OTP[1:0]	Internal LDO reference	1.2 V	3.3 V	5.0 V	3.3 V	1.2 V	3.3 V
VMON_PRE configuration	VPRE_V_OTP[5:0]	VMON_PRE monitoring voltage	6.00 V	5.40 V	6.00 V	6.00 V	6.00 V	6.00 V
	VMON_PRE_OVTH_OTP[3:0]	VMON_PRE overvoltage threshold	110.5 %	110.5 %	110 %	110 %	110 %	110 %
	VMON_PRE_UVTH_OTP[3:0]	VMON_PRE undervoltage threshold	90 %	94 %	90 %	90 %	90 %	90 %

Table 260. OTP configurations*...continued*

	VMON_PRE_OVDGLT_OTP	VMON_PRE overvoltage deglitch	45 µs	45 µs	45 µs	45 µs	45 µs	45 µs
	VMON_PRE_UVDGLT_OTP[1:0]	VMON_PRE undervoltage deglitch	40 µs	40 µs	40 µs	25 µs	40 µs	40 µs
VMON_CORE configuration	VCORE_V_OTP[7:0]	VMON_CORE monitoring voltage	1.50 V	1.50 V	1.50 V	1.50 V	1.25 V	1.50 V
	VMON_CORE_OVTH_OTP[3:0]	VMON_CORE overvoltage threshold	104.5 %	108.00 %	106 %	106 %	106 %	106 %
	VMON_CORE_UVTH_OTP[3:0]	VMON_CORE undervoltage threshold	95.5 %	95.5 %	94.00 %	94.00 %	94.00%	94.00 %
	VMON_CORE_OVDGLT_OTP	VMON_CORE overvoltage deglitch	45 µs	45 µs	45 µs	45 µs	45 µs	45 µs
	VMON_CORE_UVDGLT_OTP[1:0]	VMON_CORE undervoltage deglitch	40 µs	40 µs	40 µs	25 µs	40 µs	40 µs
VMON_LDO1 configuration	LDO1_V_OTP	VMON_LDO1 monitoring voltage	5.0 V	3.3 V	5.0 V	5.0 V	5.0 V	5.0 V
	VMON_LDO1_OVTH_OTP[3:0]	VMON_LDO1 overvoltage threshold	106.00 %	108.00 %	107.50 %	107.50 %	106.00 %	107.50 %
	VMON_LDO1_UVTH_OTP[3:0]	VMON_LDO1 undervoltage threshold	94.00 %	91.00 %	92.50 %	93.00 %	94.00 %	92.50 %
	VMON_LDO1_UVDTH_OTP	VMON_LDO1 Degraded UV Monitoring	Normal UV	Normal UV	Normal UV	Normal UV	Normal UV	Normal UV
	VMON_LDO1_OVDGLT_OTP	VMON_LDO1 overvoltage deglitch	45 µs	45 µs	45 µs	45 µs	45 µs	45 µs
	VMON_LDO1_UVDGLT_OTP[1:0]	VMON_LDO1 undervoltage deglitch	40 µs	40 µs	40 µs	25 µs	40 µs	40 µs
	LDO1_PLIFT_DIS_OTP	LDO1 pin lift detection	LDO1 pin lift detection enabled	LDO1 pin lift detection enabled	LDO1 pin lift detection enabled	LDO1 pin lift detection enabled	LDO1 pin lift detection enabled	LDO1 pin lift detection enabled
VMON_LDO2 configuration	LDO2_V_OTP	VMON_LDO2 monitoring voltage	3.3 V	5.0 V	3.3 V	3.3 V	3.3 V	3.3 V
	VMON_LDO2_OVTH_OTP[3:0]	VMON_LDO2 overvoltage threshold	106.00 %	104.5 %	106.00 %	106.00 %	106.00 %	106.00 %
	VMON_LDO2_UVTH_OTP[3:0]	VMON_LDO2 undervoltage threshold	94.00 %	95.5 %	94.00 %	94.00 %	94.00 %	94.00 %
	VMON_LDO2_UVDTH_OTP	VMON_LDO2 Degraded UV Monitoring	Normal UV	Normal UV	Normal UV	Normal UV	Normal UV	Normal UV
	VMON_LDO2_OVDGLT_OTP	VMON_LDO2 overvoltage deglitch	45 µs	45 µs	45 µs	45 µs	45 µs	45 µs
	VMON_LDO2_UVDGLT_OTP[1:0]	VMON_LDO2 undervoltage deglitch	40 µs	40 µs	40 µs	25 µs	40 µs	40 µs
	LDO2_PLIFT_DIS_OTP	LDO2 pin lift detection	LDO2 pin lift detection enabled	LDO2 pin lift detection enabled	LDO2 pin lift detection enabled	LDO2 pin lift detection enabled	LDO2 pin lift detection enabled	LDO2 pin lift detection enabled
VMON_TRK1 configuration	TRK1_V_OTP[1:0]	VMON_TRK1 monitoring voltage	5.0 V	5.0 V	5.0 V	5.0 V	3.3 V	3.3 V
	VMON_TRK1_OVTH_OTP[3:0]	VMON_TRK1 overvoltage threshold	104.5 %	108.00 %	106 %	107.50 %	106.00 %	106 %
	VMON_TRK1_UVTH_OTP[3:0]	VMON_TRK1 undervoltage threshold	95.5 %	92.00 %	94 %	93.00 %	94 %	94 %
	VMON_TRK1_OVDGLT_OTP	VMON_TRK1 overvoltage deglitch	45 µs	45 µs	45 µs	45 µs	45 µs	45 µs
	VMON_TRK1_UVDGLT_OTP[1:0]	VMON_TRK1 undervoltage deglitch	40 µs	40 µs	40 µs	25 µs	40 µs	40 µs
VMON_TRK2 configuration	TRK2_V_OTP[1:0]	VMON_TRK2 monitoring voltage	3.3 V	5.0 V	5.0 V	3.3 V	3.3 V	3.3 V
	VMON_TRK2_OVTH_OTP[3:0]	VMON_TRK2 overvoltage threshold	104.5 %	108.00 %	106 %	106 %	104.50 %	106 %
	VMON_TRK2_UVTH_OTP[3:0]	VMON_TRK2 undervoltage threshold	95.5 %	92.00 %	94.00 %	94.00 %	95.50 %	94.00 %
	VMON_TRK2_OVDGLT_OTP	VMON_TRK2 overvoltage deglitch	45 µs	45 µs	45 µs	45 µs	45 µs	45 µs
	VMON_TRK2_UVDGLT_OTP[1:0]	VMON_TRK2 undervoltage deglitch	40 µs	40 µs	40 µs	25 µs	40 µs	40 µs
VMON_REF configuration	VREF_V_OTP	VMON_VREF monitoring voltage	5.0 V	3.3 V	5.0 V	5.0 V	3.3 V	3.3 V
	VMON_VREF_OVTH_OTP[3:0]	VMON_VREF overvoltage threshold	104.50 %	105.00 %	104.50 %	105.00 %	105.00 %	104.50 %
	VMON_VREF_UVTH_OTP[3:0]	VMON_VREF undervoltage threshold	95.50 %	95.00 %	95.50 %	95.00 %	95.00 %	95.50 %
	VMON_VREF_OVDGLT_OTP	VMON_REF overvoltage deglitch	45 µs	45 µs	45 µs	45 µs	45 µs	45 µs
	VMON_VREF_UVDGLT_OTP[1:0]	VMON_REF undervoltage deglitch	40 µs	40 µs	40 µs	25 µs	40 µs	40 µs

Table 260. OTP configurations*...continued*

	VREF_PLIFT_DIS_OTP	VREF pin lift detection	VREF pin lift detection enabled	VREF pin lift detection enabled	VREF pin lift detection enabled	VREF pin lift detection enabled	VREF pin lift detection enabled	VREF pin lift detection enabled
VMON_EXT configuration	VMON_EXT_OVTH_OTP[3:0]	VMON_EXT overvoltage threshold	104.50 %	110.00 %	110.00 %	105.00 %	105.00 %	110.00 %
	VMON_EXT_UVTH_OTP[3:0]	VMON_EXT undervoltage threshold	95.50 %	95.00 %	90 %	95.00 %	95.00 %	90 %
	VMON_EXT_OVDGLT_OTP	VMON_EXT overvoltage deglitch	45 µs	45 µs	45 µs	45 µs	45 µs	45 µs
	VMON_EXT_UVDGLT_OTP[1:0]	VMON_EXT undervoltage deglitch	40 µs	40 µs	40 µs	25 µs	40 µs	40 µs
ABIST1 configuration	ABIST1_VPRE_EN_OTP	ABIST1 on VMON_PRE	ABIST1 enabled	ABIST1 enabled	ABIST1 enabled	ABIST1 enabled	ABIST1 enabled	ABIST1 enabled
	ABIST1_VCORE_EN_OTP	ABIST1 on VMON_CORE	ABIST1 enabled	ABIST1 enabled	ABIST1 enabled	ABIST1 enabled	ABIST1 enabled	ABIST1 enabled
	ABIST1_LDO1_EN_OTP	ABIST1 on VMON_LDO1	ABIST1 enabled	ABIST1 enabled	ABIST1 enabled	ABIST1 enabled	ABIST1 enabled	ABIST1 enabled
	ABIST1_LDO2_EN_OTP	ABIST1 on VMON_LDO2	ABIST1 enabled	ABIST1 enabled	ABIST1 enabled	ABIST1 enabled	ABIST1 enabled	ABIST1 enabled
	ABIST1_TRK1_EN_OTP	ABIST1 on VMON_TRK1	ABIST1 enabled	ABIST1 enabled	ABIST1 enabled	ABIST1 enabled	ABIST1 enabled	ABIST1 enabled
	ABIST1_TRK2_EN_OTP	ABIST1 on VMON_TRK2	ABIST1 enabled	ABIST1 enabled	ABIST1 enabled	ABIST1 enabled	ABIST1 disabled	ABIST1 enabled
	ABIST1_VREF_EN_OTP	ABIST1 on VMON_REF	ABIST1 enabled	ABIST1 enabled	ABIST1 enabled	ABIST1 enabled	ABIST1 enabled	ABIST1 enabled
	ABIST1_EXT_EN_OTP	ABIST1 on VMON_EXT	ABIST1 disabled	ABIST1 enabled	ABIST1 enabled	ABIST1 enabled	ABIST1 disabled	ABIST1 enabled
System safety configuration	FAULT_DFS_EN_OTP	DFS entry mode	Go to DFS when FLT_ ERR_CNT = max	Go to DFS when FLT_ ERR_CNT = max	Go to DFS when FLT_ ERR_CNT = max	Go to DFS when FLT_ ERR_CNT = max	Go to DFS when FLT_ ERR_CNT = max	Go to DFS when FLT_ ERR_CNT = max
	FS1B_FS0B_EN_OTP	FS1B assertion mode	Delayed assertion disabled	Delayed assertion enabled	Delayed assertion enabled	Delayed assertion enabled	Delayed assertion disabled	Delayed assertion enabled
	PRE_RSTB_DLY_EN_OTP	RSTB delay from FS0B	0 µs	100 µs	0 µs	100 µs	0 µs	0 µs
	DIS8S_DIS_OTP	RSTB low detection timer	Timer disabled	8 second timer enabled	8 second timer enabled	8 second timer enabled	8 second timer enabled	8 second timer enabled
	WD_DIS_OTP	Watchdog timer	Watchdog timer enabled	Watchdog timer enabled	Watchdog timer enabled	Watchdog timer enabled	Watchdog timer enabled	Watchdog timer enabled
	LBIST_STDBY_OTP[7:0]	Bypass LBIST from *standby mode*	Always perform LBIST	Always perform LBIST	Always perform LBIST	Always perform LBIST	Always perform LBIST	Always perform LBIST
	MDFS_DIS_OTP	Main DFS availability	Deep Fail Safe available	Deep Fail Safe available	Deep Fail Safe available	Deep Fail Safe available	Deep Fail Safe available	Deep Fail Safe available
	DFS_DIS_OTP	Deep Fail Safe state availability	Deep Fail Safe available	Deep Fail Safe available	Deep Fail Safe available	Deep Fail Safe available	Deep Fail Safe available	Deep Fail Safe available
OTP ID	PROG_IDH_OTP[7:0]	Program ID high	A	A	A	A	A	D
	PROG_IDL_OTP[7:0]	Program ID low	2	3	4	6	B	C
FS versioning bits	VMON_EXT_DIS_VOTP	External monitor	VMON disabled	VMON enabled	VMON enabled	VMON enabled	VMON enabled	VMON enabled
	FCCU_DIS_VOTP	FCCU function	FCCU available	FCCU available	FCCU available	FCCU available	FCCU available	FCCU available
	ERRMON_DIS_VOTP	ERRMON function	ERRMON not available	ERRMON available	ERRMON not available	ERRMON available	ERRMON not available	ERRMON not available

26 Packaging

26.1 Package mechanical dimensions

Package dimensions are provided in package drawings. To find the most current package outline drawing, go to http://www.nxp.com and perform a keyword search for the drawing's document number.

Table 261. Package mechanical dimensions

Package	Suffix	Package outline drawing number
7.0 × 7.0, 48–Pin LQFP exposed pad, with 0.5 mm pitch, and a 4.5 × 4.5 exposed pad	AE	98ASA00945D

26.2 Package outline

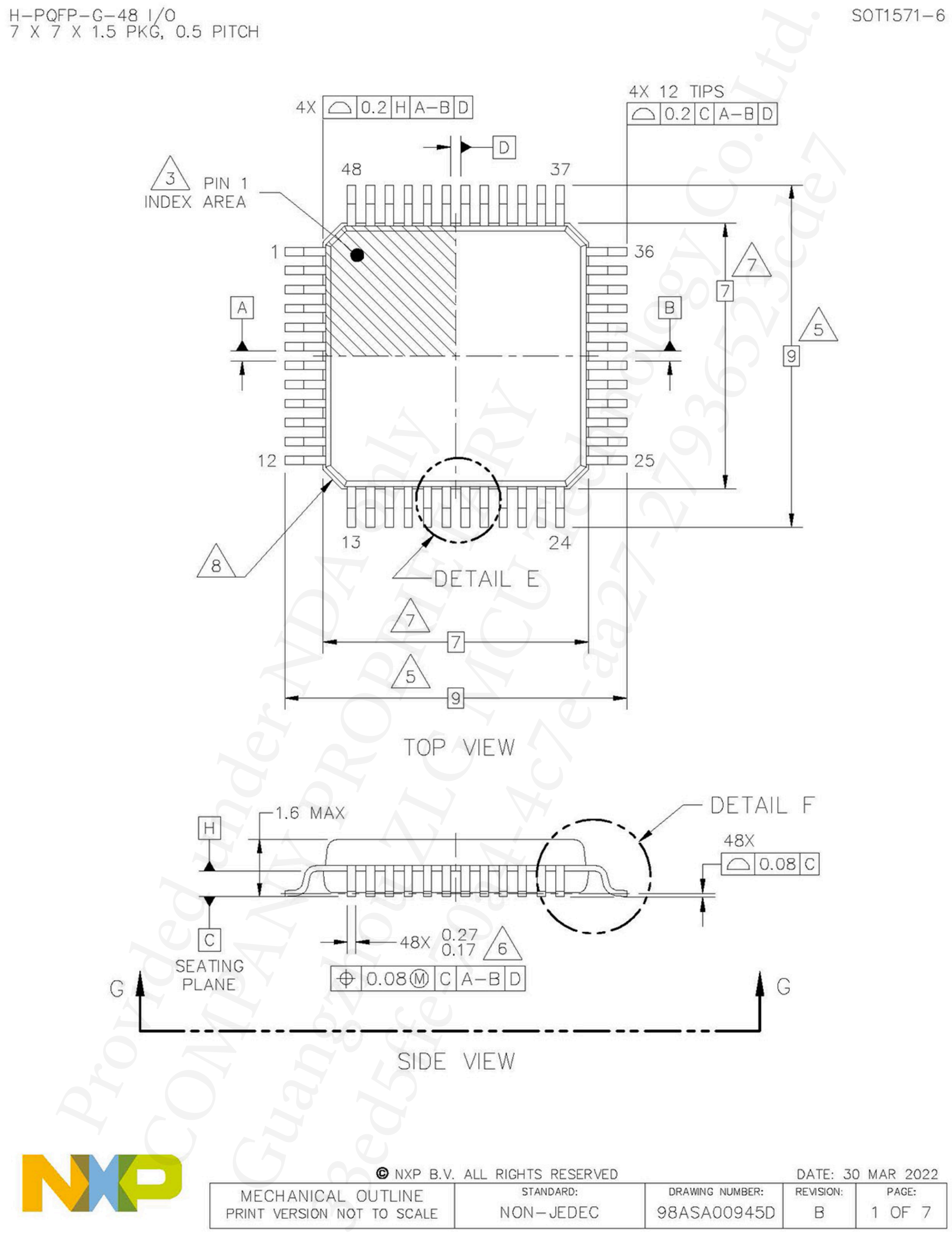

Figure 80. SOT1571-6

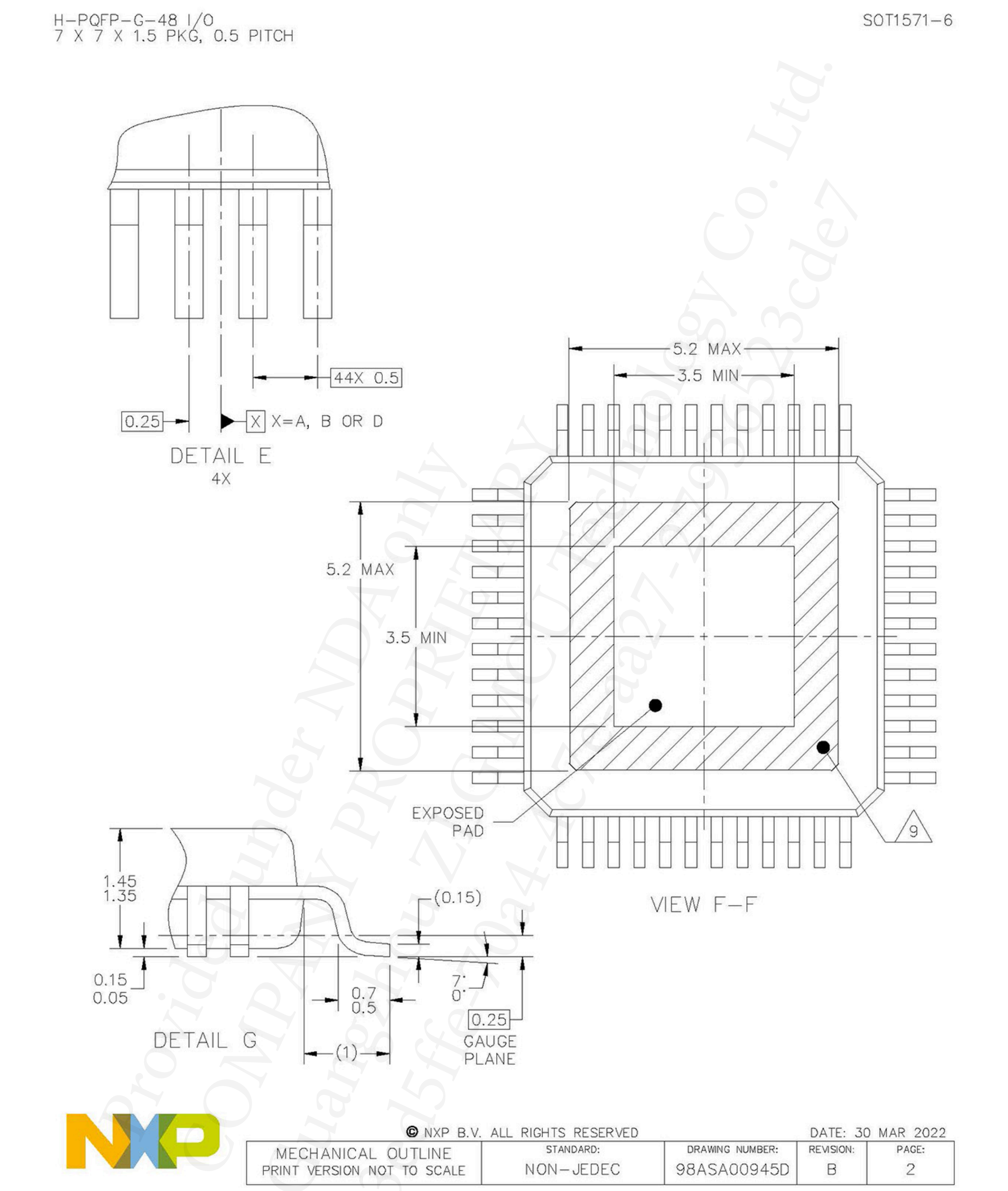

Figure 81. Package outline details (SOT1571-6)

H–PQFP–G–48 I/O
7 X 7 X 1.5 PKG, 0.5 PITCH

SOT1571–6

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. PIN 1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
5. DIMENSION TO BE DETERMINED AT SEATING PLANE C.
6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT BY MORE THAN 0.08MM AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07MM.
7. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25MM PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
8. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
9. HATCHED AREA REPRESENTS POSSIBLE MOLD FLASH ON EXPOSED PAD.
10. KEEP OUT ZONE REPRESENTS AREA ON PCB THAT MUST NOT HAVE ANY EXPOSED METAL (TRACE/VIA) FOR PCB ROUTING DUE TO THE POSSIBILITY OF SHORTING TO TIE BAR/EXPOSED PAD.

DATE: 30 MAR 2022

MECHANICAL OUTLINE	STANDARD:	DRAWING NUMBER:	REVISION:	PAGE:
PRINT VERSION NOT TO SCALE	NON–JEDEC	98ASA00945D	B	6

Figure 82. Package outline notes (SOT1571-6)

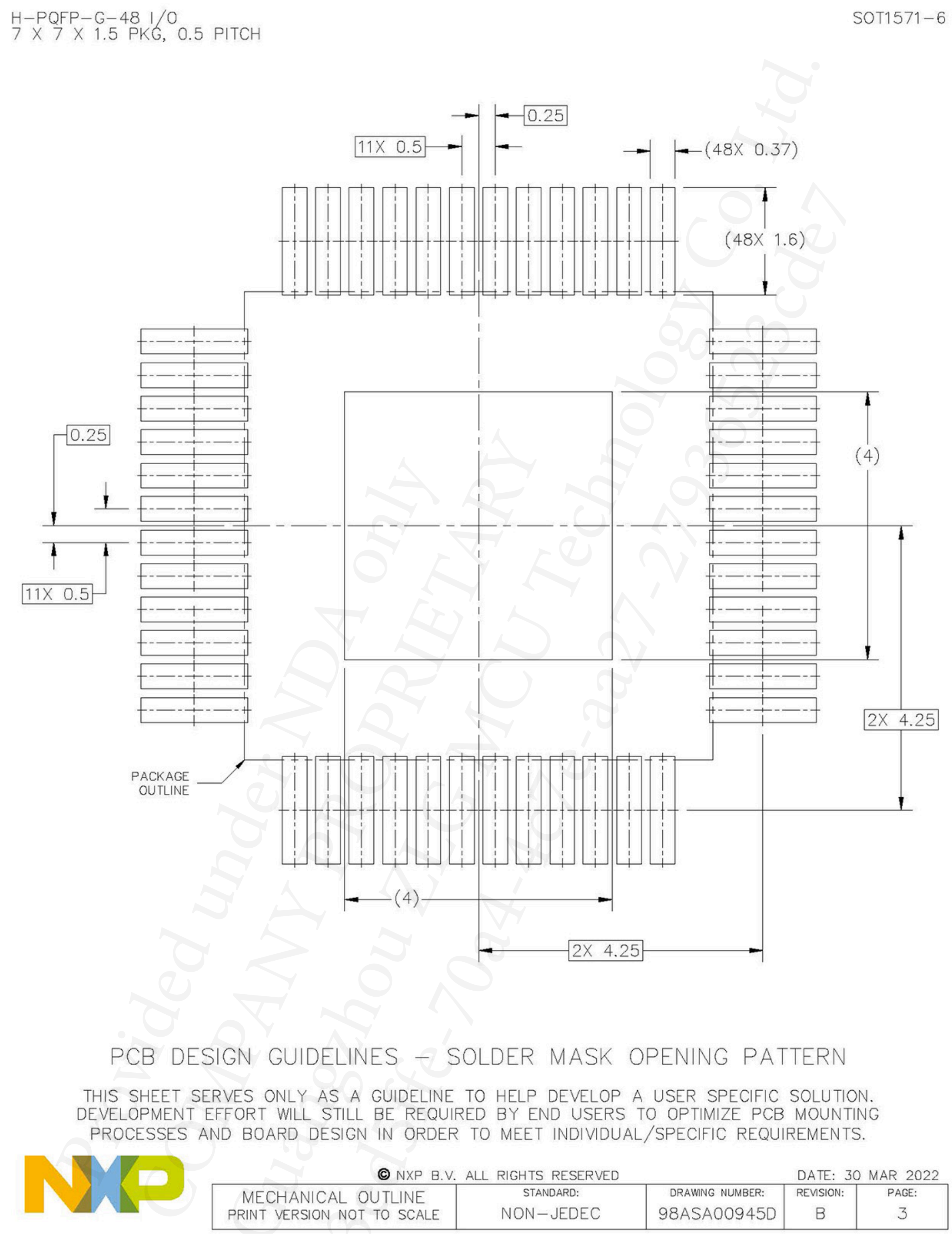

Figure 83. PCB design guidelines - solder mask opening pattern (SOT1571-6)

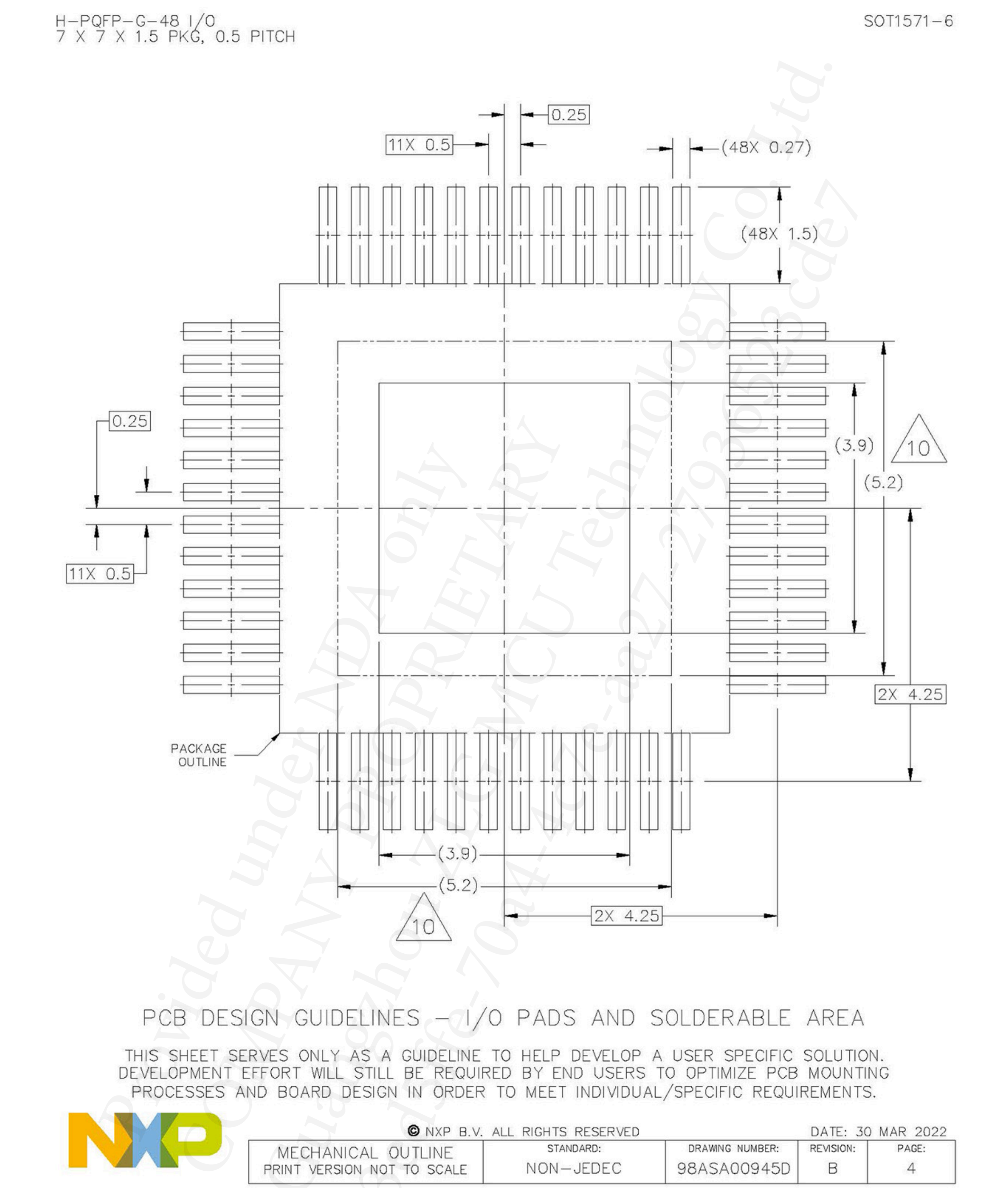

Figure 84. PCB design guidelines - I/O pads and solderable area (SOT1571-6)

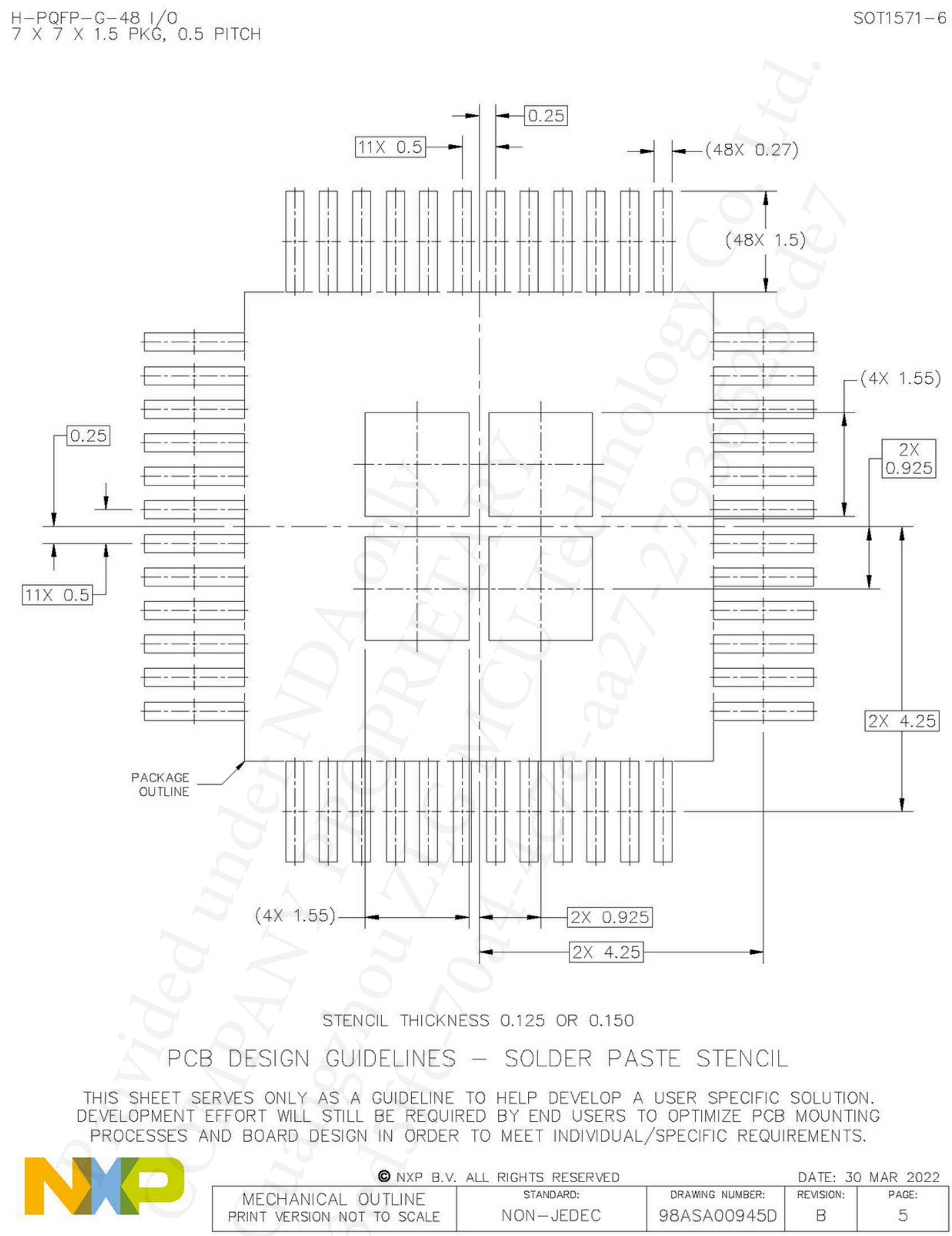

Figure 85. PCB design guidelines - solder paste stencil (SOT1571-6)

27 References

Table 262. References

Documents, Tools, Enablement	URL
FS26 Functional Safety Manual	https://www.nxp.com/products/power-management/pmics-and-sbcs/safety-sbcs/safety-system-basis-chip-sbc-with-low-power-fit-for-asil-d:FS26
FS26 Dynamic FMEDA	https://www.nxp.com/products/power-management/pmics-and-sbcs/safety-sbcs/safety-system-basis-chip-sbc-with-low-power-fit-for-asil-d:FS26
AN12995 - FS26 Product Guidelines	https://www.nxp.com/products/power-management/pmics-and-sbcs/safety-sbcs/safety-system-basis-chip-sbc-with-low-power-fit-for-asil-d:FS26
FS26_SMPS_Calculator.xls	https://www.nxp.com/products/power-management/pmics-and-sbcs/safety-sbcs/safety-system-basis-chip-sbc-with-low-power-fit-for-asil-d:FS26
FS26 SMPS Simplis models	https://www.nxp.com/products/power-management/pmics-and-sbcs/safety-sbcs/safety-system-basis-chip-sbc-with-low-power-fit-for-asil-d:FS26
FS26 Graphical User Interface • To create an OTP configuration • To interface an EVB KIT with a computer	https://www.nxp.com/products/power-management/pmics-and-sbcs/safety-sbcs/safety-system-basis-chip-sbc-with-low-power-fit-for-asil-d:FS26
FS26 Power Dissipation Tool Calculator	https://www.nxp.com/products/power-management/pmics-andsbcs/safety-sbcs/safety-system-basis-chip-sbc-with-low-powerfit-for-asil-d:FS26
FS26 Product Overview	https://www.nxp.com/products/power-management/pmics-and-sbcs/safety-sbcs/safety-system-basis-chip-sbc-with-low-power-fit-for-asil-d:FS26
KITFS26AEEVM: FS26 Evaluation Board	https://www.nxp.com/products/power-management/pmics-and-sbcs/safety-sbcs/fs26-safety-sbc-evaluation-board:KITFS26AEEVM
KITFS26SKTEVM: FS26 Socket Board	https://www.nxp.com/products/power-management/pmics-and-sbcs/safety-sbcs/fs26-safety-sbc-programming-socket-board:KITFS26SKTEVM

28 Revision history

Table 263. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
FS26 v.4	20231031	Product data sheet	202310014I	FS26 v.3
Modifications:	• Global: corrected many parameter names by inserting underscores, formatting using subscript, or changing subscript to regular text • Updated Figure 45: corrected NMOS symbol • UpdatedFigure 66: updated format • Updated Table 1: updated hyperlinks • Updated Table 2: corrected package name • Updated Table 258: changed $ABIST1_{TDUR}$ to t_{ABIST1_DUR} and $ABIST2_{TDUR}$ to t_{ABIST2_DUR} and corrected t_{ABIST2_DUR} description • Updated Section 22.9: clarified ERRMON functionality • Updated Section 20.3: changed V_{BST_OTP} to V_{BST} • Updated Section 22.7.1: added Figure 54 • Updated Section 22.7: reordered Table 195 rows • Updated Section 22.7.3: changed *FCCU1_FS_REACT* to *FCCU1_FS_REACTION* • Updated Section 22.11.3: added detailed description of FS1B behavior depending on FS1 B_FS0B_EN_OTP bit, changed *If FS1B_FS0B_EN_OTP = 0* to *If FS1B_FS0B_EN_OTP = 1*; reordered figures and re-added use case 1 figure • Updated Section 20.2: fixed typos in bit field references • Updated Table 183: changed RPU_{INTB} to R_{INTB_PU}; changed VOL_{INTB} to V_{INTB_VOL}; changed ILK_{INTB} to I_{INTB_LEAK} • Updated Section 15.5: changed *VBST_OTP* to *VBST*; changed V_{PRE} to V_{PRE_PWM} • Updated Section 18.20: removed extra table title • Updated Section 20.1 • Updated Section 22.12.1: corrected sentence "In the case of an LBIST failure, RSTB is released, but FS0B remains low and cannot be released." • Updated Section 20.5 • Updated Table 168: changed *LDOxOC* to *LDOxOC_I* and R_{LDOx_DCHG} to R_{LDOx_DIS}; removed a typo to reveal C_{OUT_LDOx} in the last row • Updated Section 21.4: clarified the different available functionalities and behaviors throughout the section. • Updated Section 20.4 • Updated Section 17.20: in AMUX[4:0], for bit values 00111 through 01110, changed *voltage* to *feedback voltage*; added *(voltage reference)* to descriptions of bit vaiues 00001 through 00011 • Updated Section 19.1: corrected bit field ranges in OTP_VBST_CFG3 register • Updated Section 22.6.6: detailed the device settings to have the MCU fault recovery feature operating as described • Updated Section 13.2.2: removed application use case above 18 V • Updated Table 260: changed Wake1 to WAKE1 multiple times in the second body row • Updated Table 262: added FS26 Power Dissipation Tool Calculator; under FS26 Graphical User Interface, struck first bullet • Updated Section 22.11.4: removed FS1B release conditions LBIST OK and added FS1B_ FS0B_EN_OTP condition for releasing FS1B safety output • Updated Section 21.1.3: aligned deviation range in the text with the specification in Table 173 • Updated Section 21.4.4: changed *LONG_DURATION_TIMER* to *M_LDT_CFG1, M_LDT_ CFG2, M_LDT_CFG3 and M_LDT_CTRL*; changed *LDT_ENABLE* to *LDT_EN* • Updated Section 14.1			

Table 263. Revision history*...continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
	• Updated Table 170; changing R_{TRKx_DCHG} to R_{TRKx_DIS} • Updated Section 22.8.5: added recommendation on the ABIST1 setting when using TRK1 to supply off-board loads • Updated Section 22.8.6: added recommendation on the ABIST1 setting when using TRK2 to supply off-board loads • Updated Section 20.4: changed I_{PEAK_CORE} to I_{CORE_PEAK} • Updated Section 20.4.1: corrected tool name from *GUI POWER tool* to *power dissipation tool calculator* • Updated Table 166: changed $I_{PEAK\_CORE\_08}$ to $I_{CORE\_PEAK\_08}$; changed $I_{PEAK\_CORE\_165}$ to $I_{CORE\_PEAK\_165}$; changed η_{PEAK_VCORE} to η_{CORE_PEAK} • Updated Section 21.3.2.4: added sentence explaining VCORE_PGOOD signal behavior at startup and when powering down • Updated Section 20.6 • Updated Section 20.2.2: corrected tool name from *GUI POWER tool* to *power dissipation tool calculator* • Updated Section 20.2.1: changed VOL_{BST_PG} to $V_{BST\_PG\_VOL}$ and ILK_{BST_PG} to I_{BSTPG_LEAK} • Updated Table 158: added $V_{DIG\_FS\_POR}$ parameter, updated footnote [2] adding temperature parameter impacti, and updated V_{PRE_PFM} minimum value from 3.3 V to 3.7 V in V_{BOS_STBY} • Updated Table 10: added Deep Fail-safe current consumption (equivalent to LPOFF) • Updated Figure 14: updated naming for consistency; corrected *Pre-Standby mode* and *Pre-LPOFF mode* states • Updated Table 210 added $VMON_{CORE\_UVTH\_ACC}$ parameter • Updated Table 181: details added on LDT_I event description *Function 1 only* • Updated Table 160: updated C_{BOOT_PRE} nominal value ranges and effective value range • Updated Table 65: removed LDT_FNCT[2:0] = 5, 6 and 7 (unnecessary values) • Updated Section 22.7.2: added Figure 56 and Figure 57 • Updated Section 22.4: details added for the GOTO_INIT request impacti on the different counters and the RSTB pin • Added disclaimer *NXP B.V. is not an operating company and it does not distribute or sell products.*			
FS26 v.3	20221117	Product data sheet	—	FS26 v.2.2
Modifications	• Global corrections to grammar and style throughout • Updated Table 2 • Updated Table 10 • Updated Section 14.1: – Added list item "L_{PRE} = 10 µH", updated footnotes – Changed list item "FS0B asserted, FS1B pulled up to a disabled supply in Standby mode" to "FS0B = 0 and FS1B = 0, pulled up to a disabled supply in Standby mode." • Updated Section 14.2: – Added list item "L_{PRE} = 10 µH – Updated list item "LDO1 = 3.3 V, LDO2 = 5 V and VPRE = 5.35 V" to read "V_{LDO1} = 3.3 V, V_{LDO2} = 5 V and V_{PRE} = 5.35 V" – Inserted text after Figure 12 – Changed list item "FS0B asserted, FS1B pulled up to a disabled supply in Standby mode." to "FS0B = 0 and FS1B = 0, pulled up to a disabled supply in Standby mode." – Changed list item "FS0B asserted, FS1B pulled up to a disabled supply in Standby mode." to "FS0B = 0 and FS1B = 0, pulled up to a disabled supply in Standby mode." • Updated Section 18.7			

Table 263. Revision history...*continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes

	• Updated Table 111
	• Updated Table 160
	• Updated Section 20.3: "In Back-end mode (VBST_CFG_OTP = ‘1’):" now reads "In Back-end mode or boost not used (VBST_CFG_OTP = ‘1’):"; inserted text
	• Updated Table 170
	• Updated Section 21.4.1: Changed "448 μs resolution" to "488 μs resolution"
	• Updated Section 22.4: Inserted text
	• Updated Table 10: Inserted "L_{PRE} = 10 μH" in first I_{Q_STBY} entry Description, removed "L_{PRE} = 10 μH" from second I_{Q_STBY} Description
	• Updated Table 189
	• Updated Table 194
	• Updated Table 207
	• Updated Table 71: Changed "Flags Reporting: FCCU12, FCCU1, FCCU2, ERRMON to "Flags Reporting: RSTB_DIAG, FS0B_DIAG, FS1B_DIAG" in Bit 13; changed "Source register: FS_DIAG_SAFETY2" to "Source register: FS_SAFE_IOS_1"
	• Updated Table 109: Changed table title from "FS_LP_REQ register bit description" to "FS_LDT_LPSEL register bit description"
	• Updated Table 160
	  – Changed Description of F_{PRE} from "VPRE_FREQ_OTP = 0" and "VPRE_FREQ_OTP = 1" to "VPRE_CLK_OTP = 0" and "VPRE_CLK_OTP = 1", respectively
	  – Changed Description of $t_{PRE\_ON\_MIN\_450K}$ from "VPRE_FREQ_OTP = 0" to "VPRE_CLK_OTP = 0"
	  – Changed Description of $t_{PRE\_OFF\_MIN}$, VPRE_PFM_TOFF_OTP[1:0] = 10 and V_{PREIN} = 12 V switched positions
	• Updated Table 168
	  – Removed Symbol I_{Q_LDOx25}
	  – Changed Symbol I_{Q_LDOx85} to I_{Q_LDOx}
	    – Changed I_{Q_LDOx} Description from "$V_{LDOx\_HDR\_STBY}$ = 50mV" to "$V_{LDOx\_HDR\_STBY}$ = 50mV or 350 mV"
	    – Changed Typ value from 21 to 7
	• Updated Section 22.10.2: Inserted text
	• Updated Section 22.11.3: Inserted text
	• Updated text in Section 23
	• Updated Table 260
	• Updated: Figure 2, Figure 3, Figure 6, Figure 59, Figure 10, Figure 11, Figure 12, Figure 8, Figure 26, Figure 27
	• Updated links in Table 262			

FS26 v.2.2	20221004	Product data sheet	—	FS26 v.2.1
Modifications	• Global corrections to grammar and style throughout • Corrected footnotes throughout • In Section 2, updated VCORE entry under Power Supplies to read: VCORE: synchronous buck converter with integrated FETs. VCORE is dedicated for microcontroller core supply. Output DC current up to 0.8 A or 1.65 A (depending on part number), output voltage range setting from 0.8 V to 3.35 V. • In Table 1, changed values in column labeled "Core Current Capability" from 1.6 to 1.65 • In Table 3, updated information in "RSTB" row. • In Section 12, updated text. • Corrected Section 14: I_{Q_STBY} Typ values changes from 25, 27 30 to 28, 31, 34 respectively • Updated third paragraph in Section 21.3.2			

Table 263. Revision history*...continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
	• Corrected Table 181 • Added Figure 63 to Section 22.11.1 • Added Figure 64 to Section 22.11.2 • Repositioned and replaced Figure 65 in Section 22.11.3 • Updated "LBIST Status" for entry 00 in Table 245 in Section 22.12.1 • Updated "Min" values for V_{OTP} and V_{DBG} in Table 259 • Updated Figure 78Section 24.1 • Updated Figure 79Section 24.2 • Corrected Figure 10, Figure 11 and text of Section 14.1, added footnotes • Section 14.2: Corrected Figure 12 • Section 19.4: Removed first three values under 0x12, CFG_OVUV_4_OTP, VMON_PRE_UVTH_OTP[3:0], VPRE UV threshold • Corrected Table 159 • In Table 111: Removed first entry for Hexidecimal Value and Settings, under 0x2A, OTP_VPRE_CFG4, VPRE_PFM_TON_OTP[1:0], VPRE highside minimum on time in PFM (450 kHz / 2.25 MHz) • Corrected Table 158, Table 160, Table 164, Table 166, Table 168, Table 170, Table 175, Table 180 • In Table 160, changed description of $\eta_{PEAK\_VPRE\_PWM}$ from L_{PRE} = 10 µH with DCR = 60 mΩ to L_{PRE} = 10 µH with RDCR_LPRE = 60 mΩ; changed description of $\eta_{PEAK\_VPRE\_PFM}$ from C_{OUT_PRE} = 22 µF with ESR = 2 mΩ, L_{PRE} = 10 µH with DCR = 60 mΩ, F_{PRE} = 450 kHz to C_{OUT_PRE} = 22 µF with ESR = 2 mΩ, L_{PRE} = 10 µH with RDCR_LPRE = 60 mΩ, F_{PRE} = 450 kHz; corrected Typ and Max values for TSD_{VPRE}; corrected Max value for TSD_{VPRE_HYST} • Table 168: Corrected Typ and Max values for $TSDL_{DOx}$; corrected Typ value for TSD_{LDOx_HYS} • Table 170: Corrected Typ and Max values for TSD_{TRKx}; corrected Typ value for TSD_{TRKx_HYS}; updated "Description" of the following entries, V_{TRKx_OFF}, $PSRR_{TRKx\_450KHz}$, and $PSRR_{TRKx\_2.2MHz}$ • Table 180: Corrected Typ and Max values for TSD_{GPIO1}; corrected Typ value for TSD_{GPIO1_HYS} • Corrected text of Section 14.2 • Corrected Section 15.1 • Corrected text of Section 15.2 • Updated text of Section 15.8 • Added text to Table 13 • Replaced image titled "CRC encoder example" in Section 15.8.1 • Corrected text in Table 13 under row for Bit 27 to read "Flags Reporting: WUEVENT, LDT_I, GPIO2_I, GPIO1_I, WK2_I, WK1_I • Corrected text in Section 16 • Added row to Table 52 in Section 17.18 • Updated text in Table 99 in Section 18.15 • Corrected Hexadecimal Value entries in Section 19.4 in rows for 0x1A and 0x1C • Updated, added text in Section 20.2 and Table 160 • Updated "Min" value of $C_{IN\_BST\_BE}$ entry in Table 164 in Section 20.3 • Updated "µF" value of $C_{IN\_BST\_BE}$ entry in Table 165 in Section 20.3.2 • Updated text in Table 166 in Section 20.4 • Updated Table 168 in Section 20.5 • Updated third paragraph in Section 21.3.2 • Corrected Table 181 • Added Figure 63 to Section 22.11.1 • Added Figure 64 to Section 22.11.2			

Table 263. Revision history*...continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
	• Repositioned and replaced Figure 65 in Section 22.11.3 • Updated "LBIST Status" for entry 00 in Table 245 in Section 22.12.1 • Updated "Min" values for V_{OTP} and V_{DBG} in Table 259 • Updated Figure 78Section 24.1 • Updated Figure 79Section 24.2			
FS26 v.2.1	20220517	Product data sheet	—	FS26 v.2
Modifications	• For Table 1, change title from *Orderable parts example* to *Device segmentation* • Correct content of Table 2 • Correct the package outline drawing number in Table 261 • Correct Figure 20 • Add footnotes to Table 166 and change four instances of *VCORE_SS_OTP* to *CORE_SS_OTP* • Correct descriptions in Table 21 • Change approximately 140 bit names from IO* to GPIO*, including instances in Figure 39, Figure 40, Figure 41, Figure 42, Figure 43, and Figure 44 • In Table 174, add tolerance of +/- 0.5 % for AMUX[4:0] = 00001, 0010, and 00011 • In Table 174, add tolerance of +/- 50 mV for AMUX[4:0] = 00100, 00101, and 00110 • In Section 21.3.2, add information about thermal shutdown protection • Correct title of Table 233 by adding *error* • Correct table title from *Error flag for external IC monitoring* to *Acknowledge error detection from MCU* for Table 235 • Add *Quick reference data* disclaimer to *Legal information* section.			
FS26 v.2	20220414	Product data sheet	—	FS26 v.1
Modifications	• Update Mechanical outline data to 98ASA00945D rev. B • Correct figure titles in Section 26.2			
FS26 v.1	20220329	Product data sheet	—	—
Modificaitons	Initial release			

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL https://www.nxp.com.

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