FS23 data sheet

Safety system basis chip (SBC) with power management, CAN FD and LIN transceivers

Rev. 4 — 15 September 2023

Product data sheet

CONFIDENTIAL

Document information

Information	Content
Keywords	FS23, system basis chip (SBC), pin-to-pin, software compatible, low dropout (LDO), DC-DC, quality management (QM), automotive safety integrity level (ASIL) B
Abstract	The FS23 SBC offers an expandable family of devices that is pin-to-pin and software compatible. It is scalable from the LDO version to the DC-DC version, as well as from QM to ASIL B.

1 General description

The FS23 SBC offers an expandable family of devices that is pin-to-pin and software compatible. The FS23 SBC is scalable from the linear voltage regulator version to the DC-DC regulator version, as well as from QM to ASIL B. The FS23 SBC includes CAN and LIN transceivers, along with a number of system and safety features for the latest generation of automotive electronic control units (ECU).

The FS23 SBC provides a high level of integration in order to optimize the bill of material (BOM) cost for the body and comfort market.

The FS23 device is highly flexible. It is suitable for S32K processor-based applications, as well as multi-vendor processors because of its high level of flexibility.

Several device versions are available, offering choice in output-voltage settings, operating frequency, power-up sequencing, and inputs/outputs configuration to address multiple applications.

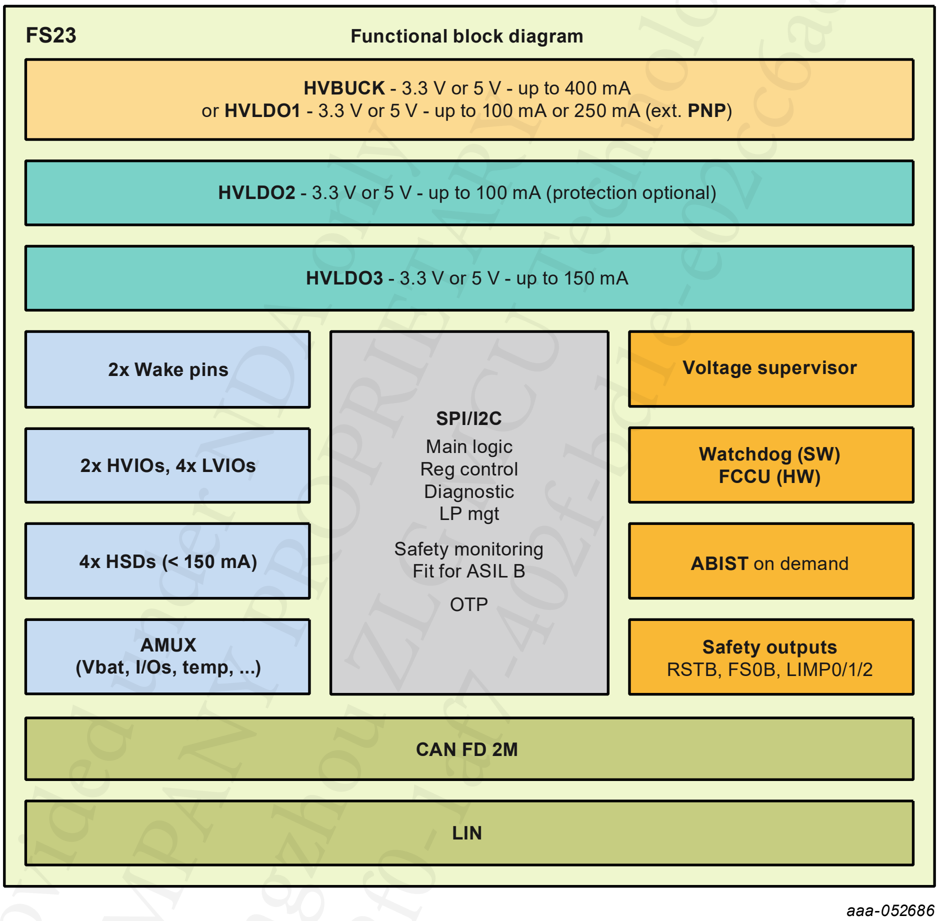


Figure 1. Functional block diagram 400 mA alternative

2 Features and benefits

Operating modes

- Normal mode with all power management and functional safety features available
- Stop mode: Low-power OFF mode with multiple wake-up sources (LPOFF)
- Standby mode: Low-power ON mode with HVBUCK or HVLDO1 active and multiple wake-up sources (LPON)

Power management

- HVBUCK: Synchronous buck converter with integrated FETs. Configurable Normal mode output voltage and LPON mode output voltage (3.3 V or 5.5 V). Output DC current capability of 400 mA in Normal mode, and 100 mA current capability in Low-power ON mode
- HVLDO1: High-voltage LDO instead of the HVBUCK for MCU supply with selectable output voltage (3.3 V or 5.5 V) and up to 100 mA DC current capability with internal PMOS and 250 mA with external PNP
- HVLDO2: High-voltage LDO regulator for system loads, with optional external protection for off-board sensors, selectable output voltage (3.3 V or 5.0 V) and up to 100 mA DC current capability
- HVLDO3: High-voltage LDO regulator for CAN FD block supply or other with selectable output voltage (3.3 V or 5.0 V) and up to 150 mA current capability

System features

- One CAN FD supporting up to 2 Mbps communication following ISO 11898-2:2016 and SAE J2284 standards
- One LIN following LIN 2.2, ISO 17987-4 and SAE-J2602-2 standards
- Two wake-up inputs (40 V capable)
- Two high-voltage I/Os with wake-up capability (40 V capable)
- Up to four low-voltage I/Os with wake-up capability
- Four configurable high-side drivers with 150 mA drive capability, to supply LEDs or enable external devices (INH), and cyclic-sense capability
- Multiple wake-up sources: WAKE pins, HVIO pins, LVIO pins, CAN FD, LIN or dedicated SPI / I^{2}C command
- Device control via 32 bits SPI interface or via I^{2}C interface, with CRC
- Integrated long duration timer (LDT) for system shutdown and wake-up control, programmable up to 194 days
- 16-channel analog multiplexer (AMUX) for system monitoring (temperature, battery voltage, internal voltages)

Functional safety

- Developed following ISO 26262:2018 standard to fit for ASIL B applications
- Internal monitoring circuitry with its own reference
- Additional input for external voltage monitoring
- Window or timeout watchdog function to monitor the MCU failures by software
- FCCU inputs to monitor MCU failures by hardware
- Analog built-in self-test (ABIST) on demand
- Safety outputs (RSTB, FS0B, LIMP0 and LIMP1/2 with 1.25 Hz or 100 Hz PWM capability)

EMC compliance

- The FS23 EMC tests are performed according to ZVEI Generic IC EMC Test Specification version 2.1 (2017) and FMC1278 Electromagnetic Compatibility Specification for Electrical/Electronic Components and subsystems version 3.0 (2018).

Configuration and enablement

- QFN48EP: QFN 48 pins with exposed pad for optimized thermal management, wettable flanks, 7 x 7 x 0.85 mm, 0.5 mm pitch, 48 pins
- One-time programmable (OTP) memory for scalability, expandability and device customization
- OTP emulation mode for system development and evaluation

3 Simplified application diagram

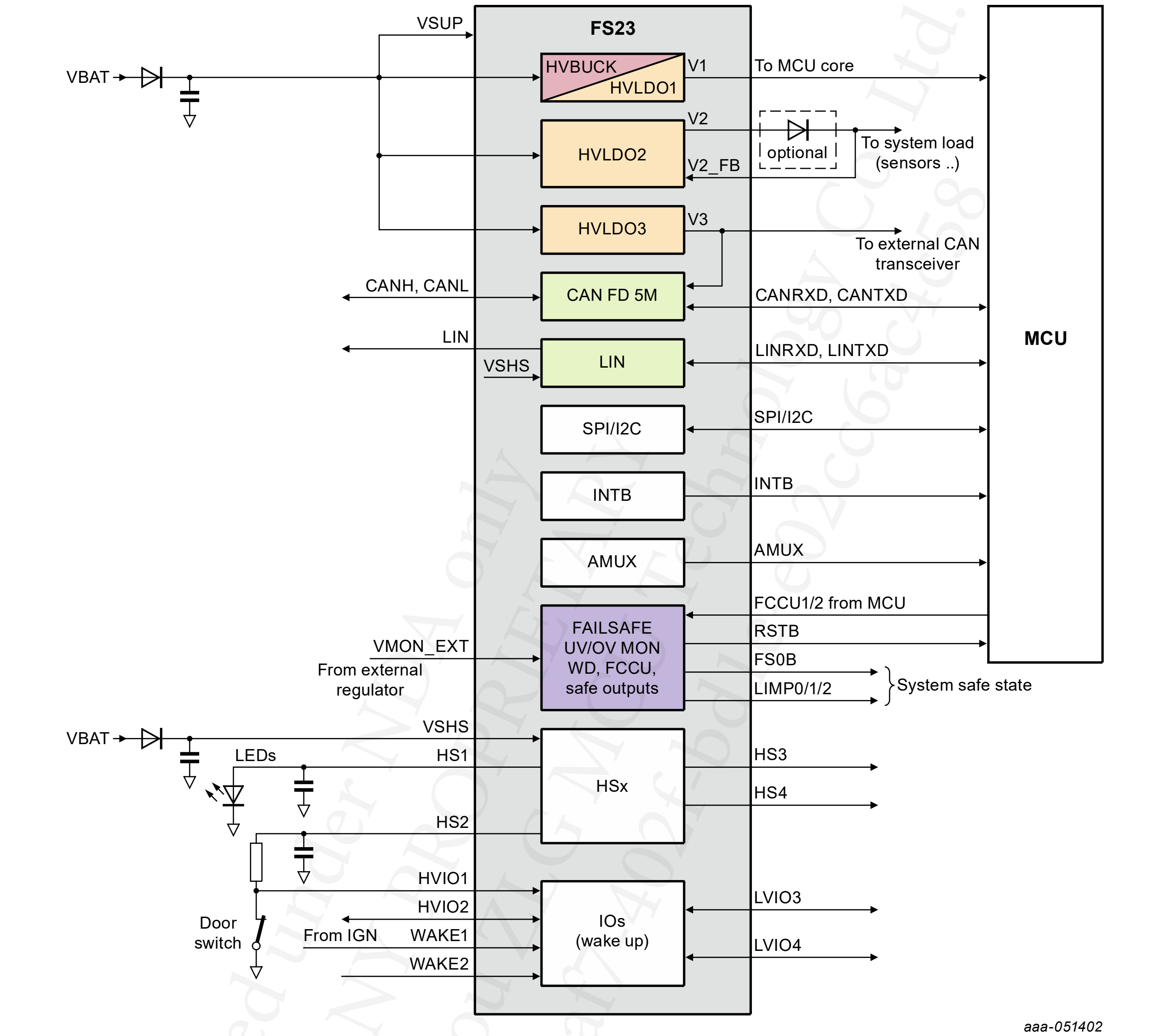


Figure 2. Typical application diagram

4 Ordering information

This section describes the part numbers available to be purchased, along with their main differences. It also describes how the part number reference is built.

4.1 Part numbers definition

Two FS23 part numbering types can be found: a full part number reference and a simplified part number.

Figure 3 and Figure 4 describe how the FS23 part numbers are built.

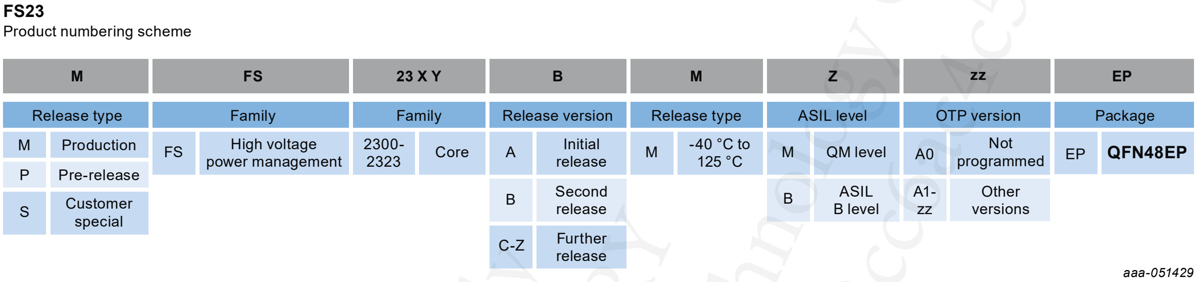
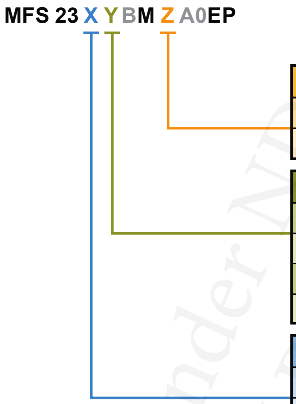


Figure 3. Full FS23 part numbers breakdown



Z	ASIL level
M	QM level (timeout WD, OV/UV, VMON)
B	Fit for ASIL B (window WD, OV/UV, ABIST, VMON, FCCU)

Y	CAN	LIN	LDT	Use case
0	Yes	No	No	Base
1	Yes	Yes	No	LIN
2	Yes	No	Yes	LDT
3	Yes	Yes	Yes	LIN and LDT

X	Power management solution
0	3 x HVLDOs
2	1 HVBUCK, 2 HVLDOs

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Figure 4. Simplified FS23 part numbers breakdown

Figure 5 maps FS23 part numbers versus the selectable product features.

V1 regulator	HVLDO		HVBUCK	
ASIL level	QM	ASIL B	QM	ASIL B
Base	FS2300M	FS2300B	FS2320M	FS2320B
LIN	FS2301M	FS2301B	FS2321M	FS2321B
LDT	FS2302M	FS2302B	FS2322M	FS2322B
LIN + LDT	FS2303M	FS2303B	FS2323M	FS2323B

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Figure 5. Part numbers mapping versus base feature sets

4.2 Part numbers list

Table 1. Device segmentation

Generic part number	V1 type	HV LDO2	HV LDO3	CAN	LIN	LDT	SPI/ I^2C	AMUX	HVIOs	LVIOs	Wake pins	High-side drivers	Fit for ASIL	FS0B	LIMPx	VMON_EXT	FCCU	Watchdog	Cyclic CRC check	RSTB 8 s timer	ABIST on demand
FS2300M	HVLDO	Yes	Yes	Yes	No	No	Yes	Yes	Yes	Yes	Yes	Yes	QM	No	Yes	No	No	Opt.	Opt.	No	No
FS2301M	HVLDO	Yes	Yes	Yes	Yes	No	Yes	Yes	Yes	Yes	Yes	Yes	QM	No	Yes	No	No	Opt.	Opt.	No	No
FS2302M	HVLDO	Yes	Yes	Yes	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes	QM	No	Yes	No	No	Opt.	Opt.	No	No
FS2303M	HVLDO	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	QM	No	Yes	No	No	Opt.	Opt.	No	No
FS2300B	HVLDO	Yes	Yes	Yes	No	No	Yes	Yes	Yes	Yes	Yes	Yes	ASIL B	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
FS2301B	HVLDO	Yes	Yes	Yes	Yes	No	Yes	Yes	Yes	Yes	Yes	Yes	ASIL B	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
FS2302B	HVLDO	Yes	Yes	Yes	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes	ASIL B	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
FS2303B	HVLDO	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	ASIL B	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
FS2320M	HVBUCK	Yes	Yes	Yes	No	No	Yes	Yes	Yes	Yes	Yes	Yes	QM	No	Yes	No	No	Opt.	Opt.	No	No
FS2321M	HVBUCK	Yes	Yes	Yes	Yes	No	Yes	Yes	Yes	Yes	Yes	Yes	QM	No	Yes	No	No	Opt.	Opt.	No	No
FS2322M	HVBUCK	Yes	Yes	Yes	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes	QM	No	Yes	No	No	Opt.	Opt.	No	No
FS2323M	HVBUCK	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	QM	No	Yes	No	No	Opt.	Opt.	No	No
FS2320B	HVBUCK	Yes	Yes	Yes	No	No	Yes	Yes	Yes	Yes	Yes	Yes	ASIL B	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
FS2321B	HVBUCK	Yes	Yes	Yes	Yes	No	Yes	Yes	Yes	Yes	Yes	Yes	ASIL B	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
FS2322B	HVBUCK	Yes	Yes	Yes	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes	ASIL B	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
FS2323B	HVBUCK	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	ASIL B	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

Note: *Additional part numbers will exist with different features and parametric settings. The device segmentation is also available on nxp.com.*

Table 2 is an example of orderable part number list.

Table 2. Orderable parts numbers

Part number[1]	Description	Package
MFS2300BMBA0EP	Superset covering FS2300B devices.	QFN48EP
MFS2303BMBA3EP	BASIC OTP configuration given as example for FS2303B devices.	
MFS2320BMBB1EP	Configuration given as example for S32K312 MCU, CAN enabled, LIN and LDT disabled.	
MFS2321BMBB2EP	Configuration given as example for S32K324 MCU, CAN and LIN enabled, LDT disabled.	
MFS2323BMBA5EP	S32K311 + FS23 EVB ASIL B, S32K31 X-Q100	
MFS2323BMMA0EP[2]	Superset covering FS2323M devices.	

[1] To order parts in tape and reel, add the R2 suffix to the full part number reference.
[2] A0 parts are non-programmed OTP configurations. Preprogrammed OTP configurations are managed through part number extension. For a custom OTP configuration, please contact a local NXP sales representative.

5 Applications

- Body control module
- HVAC
- Lighting
- Steering column lock
- Seat module
- Roof module
- Door control module
- Car access
- Gearshift
- Seat belt pre-tension
- Tail gate
- Alarm

6 Internal block diagram

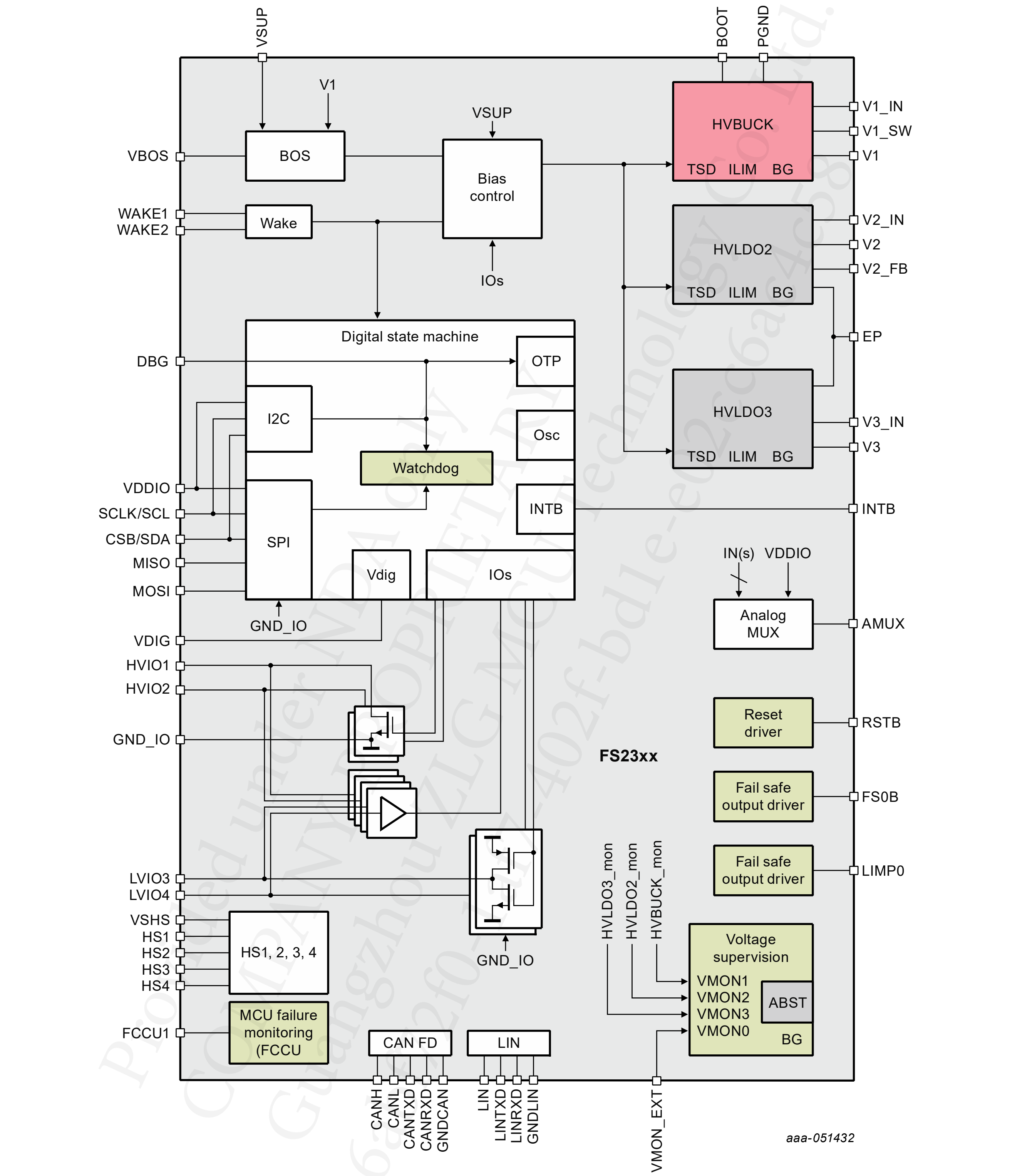


Figure 6. FS2320 Block diagram (HVBUCK)

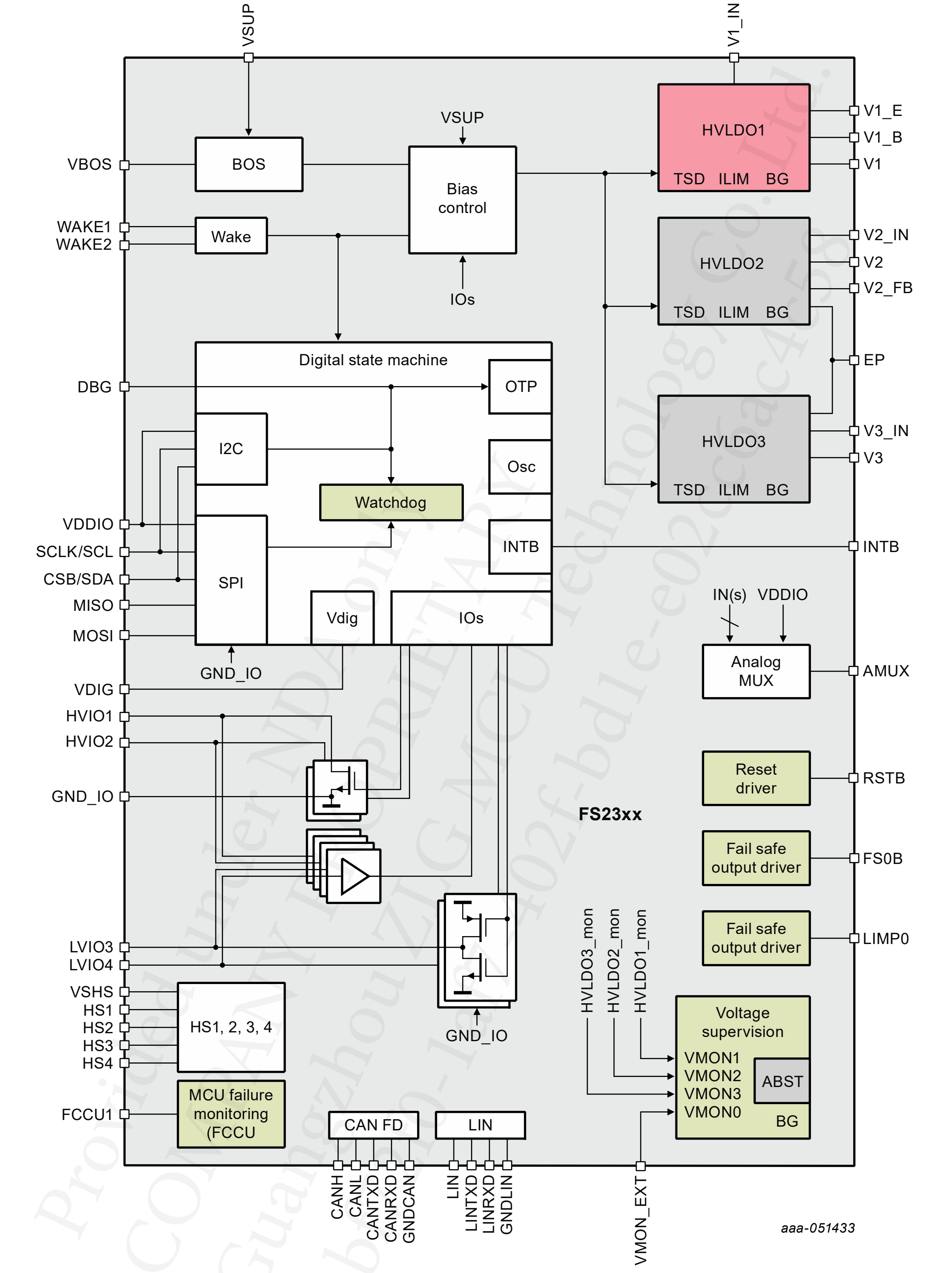


Figure 7. FS2300 Block diagram (HVLDO1)

7 Pinout information

7.1 Pinout

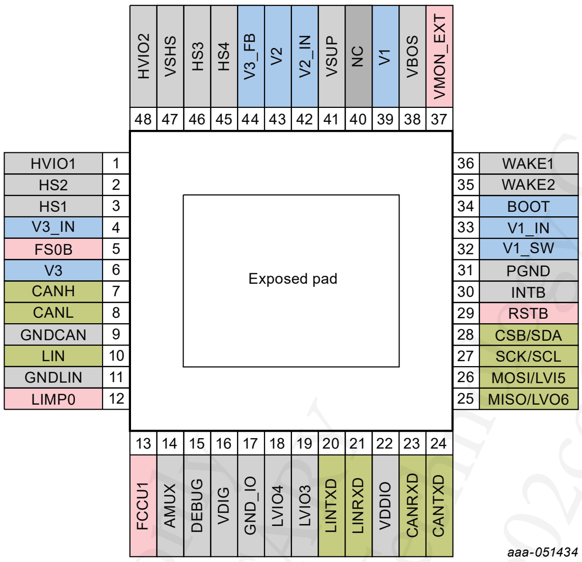
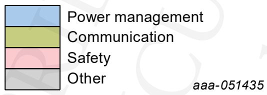


Figure 8. FS2320 Pin configuration (HVBUCK)



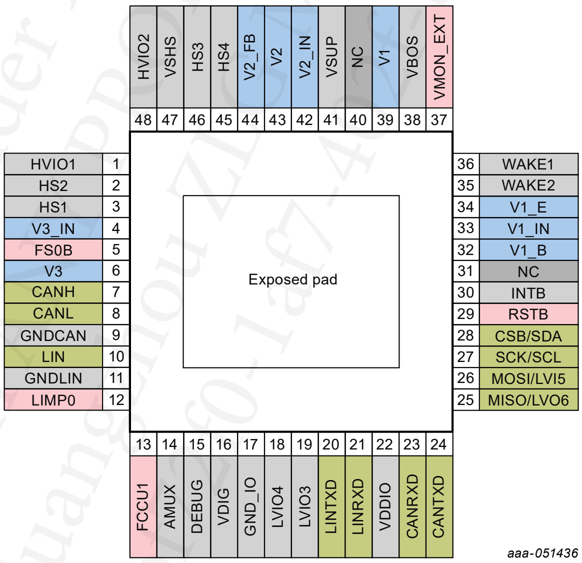


Figure 9. FS2300 Pin configuration (HVLDO1)

7.2 Pin description

Table 3. Pin description

Pin	Pin name	Type	Description
1	HVIO1	Digital input/output	High-voltage I/O 1, with wake-up capability
2	HS2	Analog output	High-side driver 2
3	HS1	Analog output	High-side driver 1
4	V3_IN	Analog input	V3 regulator input voltage
5	FS0B	Digital output	Fail-safe output 0 - Active low (low by default)
6	V3	Analog output	V3 regulator output voltage
7	CANH	Analog input/output	CAN bus - CAN high
8	CANL	Analog input/output	CAN bus - CAN low
9	GNDCAN	Ground	CAN bus - ground
10	LIN	Analog input/output	LIN single-wire bus transmitter and receiver
11	GNDLIN	Ground	LIN bus - ground
12	LIMP0	Digital output	LIMP Home mode output 0 - Active low (high by default)
13	FCCU1	Digital Input	MCU error monitoring input 1
14	AMUX	Analog output	Multiplexed output to be connected to an MCU ADC with selection of the analog parameter through I2C/SPI.
15	DEBUG	Analog input	Debug mode entry and OTP input supply (development only)
16	VDIG	Analog output	Internal supply decoupling capacitor
17	GND_IO	Ground	I/Os ground connection
18	LVIO4	Digital input/output	Low-voltage IO 4, with wake-up capability
19	LVIO3	Digital input/output	Low-voltage IO 3, with wake-up capability
20	LINTXD	Digital input	Transmitter input from the MCU, which controls the state of the LIN bus
21	LINRXD	Digital output	Receiver output, which reports the state of the LIN bus to the MCU
22	VDDIO	Analog input	Input voltage for SPI, I2C, LVIOs and AMUX
23	CANRXD	Digital output	Receiver output, which reports the state of the CAN bus to the MCU
24	CANTXD	Digital input	Transmitter input from the MCU, which controls the state of the CAN bus
25	MISO/LVO6	Digital output	SPI bus - Master input slave output(MISO)/Low-voltage output 6
26	MOSI/LVI5	Digital input	SPI bus - Master output slave input(MOSI)/Low-voltage input 5
27	SCK/SCL	Digital input/output	SPI bus - Clock input / I2C bus - clock input
28	CSB/SDA	Digital input/output	SPI bus - Chip select (active low) / I2C bus - bidirectional data line
29	RSTB	Digital input/output	Reset input/output. Active low. The main function is to reset the MCU. Reset input voltage is monitored in order to detect external reset and fault condition.
30	INTB	Digital output	Interrupt output
31	PGND	Ground	(FS2320) Power ground connection
	NC	NC	(FS2300) Not connected. This pin must be left open.
32	V1_SW	Analog input/output	(FS2320) Switching node
	V1_B	Analog output	(FS2300) V1 external PNP base signal. This pin must be left open if no PNP.
33	V1_IN	Analog input	V1 regulator input voltage
34	BOOT	Analog input/output	(FS2320) V1 bootstrap capacitor
	V1_E	Analog output	(FS2300) V1 external PNP emitter signal. This pin must be left open if no PNP.

Table 3. Pin description*...continued*

Pin	Pin name	Type	Description
35	WAKE2	Analog input	Wake up input 2
36	WAKE1	Analog input	Wake up input 1
37	VMON_EXT	Analog input	External-voltage monitoring input
38	VBOS	Analog output	Best of supply output voltage
39	V1	Analog output	V1 regulator output voltage
40	NC	NC	Not connected. This pin must be left open.
41	VSUP	Analog input	Power supply of the device
42	V2_IN	Analog input	V2 regulator input voltage
43	V2	Analog output	V2 regulator output voltage
44	V2_FB	Analog input	V2 regulator voltage feedback
45	HS4	Analog output	High-side driver 4
46	HS3	Analog output	High-side driver 3
47	VSHS	Analog input	High-side drivers and LIN supply
48	HVIO2	Digital input/output	High-voltage I/O 2, with wake-up capability

7.3 Connection of unused pins

Table 4. Connection of unused pins

Pin	Pin name	Type	Description
1	HVIO1	Digital input/output	Open (HVIO1PUPD_OTP = 01)
2	HS2	Analog output	Open
3	HS1	Analog output	Open
4	V3_IN	Analog input	VSUP
5	FS0B	Digital output	Open
6	V3	Analog output	Open
7	CANH	Analog input/output	Open
8	CANL	Analog input/output	Open
9	GNDCAN	Ground	Connection mandatory
10	LIN	Analog input/output	Open
11	GNDLIN	Ground	Connection mandatory
12	LIMP0	Digital output	Open
13	FCCU1	Digital Input	GND
14	AMUX	Analog output	Open
15	DEBUG	Analog input	Connection mandatory to GND in production (5 V or 8 V authorized for development only)
16	VDIG	Analog output	Connection mandatory
17	GND_IO	Ground	Connection mandatory
18	LVIO4	Digital input/output	Open (LVIO4PUPD_OTP = 01)
19	LVIO3	Digital input/output	Open (LVIO3PUPD_OTP = 01)
20	LINTXD	Digital input	Open (200 kΩ internal pull up to VDDIO)
21	LINRXD	Digital output	Open (push-pull structure)

Table 4. Connection of unused pins...*continued*

Pin	Pin name	Type	Description
22	VDDIO	Analog input	Connection mandatory
23	CANRXD	Digital output	Open (push-pull structure)
24	CANTXD	Digital input	Open (200 kΩ internal pull up to VDDIO)
25	MISO/LVO6	Digital output	Open
26	MOSI/LVI5	Digital input	Open (200 kΩ internal pull up to VDDIO)
27	SCK/SCL	Digital input/output	Connection mandatory
28	CSB/SDA	Digital input/output	Connection mandatory
29	RSTB	Digital input/output	Connection mandatory
30	INTB	Digital output	Open
31	PGND	Ground	Connection mandatory
	NC	NC	Open
32	V1_SW	Analog input/output	Connection mandatory
	V1_B	Analog output	Open
33	V1_IN	Analog input	Connection mandatory
34	BOOT	Analog input/output	Connection mandatory
	V1_E	Analog output	Open
35	WAKE2	Analog input	Open (WK2PUPD_OTP = 01)
36	WAKE1	Analog input	Open (WK1PUPD_OTP = 01)
37	VMON_EXT	Analog input	GND
38	VBOS	Analog output	Connection mandatory
39	V1	Analog output	Connection mandatory
40	NC	NC	Open
41	VSUP	Analog input	Connection mandatory
42	V2_IN	Analog input	Open
43	V2	Analog output	Open
44	V2_FB	Analog input	Open (internal pull down)
45	HS4	Analog output	Open
46	HS3	Analog output	Open
47	VSHS	Analog input	Connection mandatory
48	HVIO2	Digital input/output	Open (HVIO2PUPD_OTP = 01)

8 Limiting values

Table 5. Limiting values

T_A = −40 °C to 125 °C, unless otherwise specified. All voltages referenced to ground, unless otherwise specified. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Description (Rating)	Min	Max	Unit
		Voltage ratings		
WAKE2, LIMP0, WAKE1, HVIO2, HVIO1, FS0B	Global pins	–0.3	40	V
V1_IN, VSUP, V2_IN, VSHS, V3_IN	Global supply input pins	–1	40	V
V2_FB, HS4, HS3, HS2, HS1	Global pins	–2	40	V
CANH, CANL[1]	Global CAN bus pins	–33	40	V
LIN	Global LIN bus pins	–40	40	V
BOOT	High-voltage pin/Local pin	–0.3	45.5	V
V1_SW, V1_B, VMON_EXT	High-voltage pins/Local pins	–0.3	40	V
V2	High-voltage pin/Local pin	–0.3	V2_IN + 0.3	V
V1_E	High-voltage PNP pin/Local pin	V1_IN – 0.075	V1_IN + 0.075	V
DEBUG	Debug pin to enter in Debug mode. Should be grounded in the application.	–0.3	10	V
V1, V3	Local regulator outputs	–0.3	5.6	V
VDDIO, VBOS	Local pins	–0.3	5.5	V
FCCU1, LVIO4, LVIO3, LINTXD, LINRXD, CANRXD, CANTXD, MISO/ LVO6, MOSI/LVI5, SCK/SCL, CSB/ SDA, RSTB, INTB, AMUX	Local pins	–0.3	VDDIO + 0.3	V
VDIG	Local pin	–0.3	2	V
GND_IO, PGND, GDNCAN, GNDLIN	Ground pins	–0.3	0.3	V

[1] Min value is the worst case value at cold temperature (T_A = –40 °C).

9 Electrostatic discharge

All voltages referenced to ground, unless otherwise specified. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Table 6. ESD ratings

Symbol	Description (Rating)	Min	Max	Unit
ESD ratings				
Human body model: AEC-Q100 Rev H.				
V_{ESD_HBM}	All pins	–2	2	kV
$V_{ESD\_GLOBAL\_HBM}$	Global pins (VSUP, VSHS, Vx_IN, V2_FB, LIMP0, FS0B, WAKEx, HVIOx, HSx)	–4	4	kV
$V_{ESD\_CAN\_HBM}$	CAN bus interface pins (CANH, CANL)	–8	8	kV
$V_{ESD\_LIN\_HBM}$	LIN bus interface pin (LIN)	–8	8	kV
Charged device model: AEC-Q100 Rev H				
V_{ESD_CDM}	All pins	–500	500	V
Gun discharged contact Test				
V_{ESD_GUN1}	330 Ω/150 pF unpowered according to IEC 61000-4-2 Global pins and bus interface pins	–8	8	kV
V_{ESD_GUN2}	2 kΩ/150 pF unpowered according to ISO 10605.2008 Global pins and bus interface pins	–8	8	kV
V_{ESD_GUN3}	2 kΩ/330 pF powered, GND connected, according to ISO 10605.2008 Global pins and bus interface pins	–8	8	kV
V_{ESD_GUN4}	330 Ω/150 pF unpowered, GND connected, according to ISO 10605.2008 Global pins and bus interface pins	–8	8	kV

10 Thermal characteristics

Table 7. Thermal characteristics

Symbol	Description (Rating)	Min	Max	Unit
Thermal ratings				
T_A	Ambient temperature (Grade 1)	–40	125	°C
T_J	Junction temperature (Grade 1)	–40	150	°C
T_{STG}	Storage temperature	–55	150	°C
Thermal resistance (per JEDEC JESD51-2 and JESD51-8)				
$R_{\theta JA}$	Thermal resistance junction to ambient (2s2p)	-	32	°C/W
$R_{\theta JC\_BOT}$	Thermal resistance junction to case bottom (between the die and the solder pad on the bottom of the package)	-	7	°C/W
$R_{\theta JC\_TOP}$	Thermal resistance junction to case top (between package top and the junction temperature)	-	14	°C/W

11 Operating range and current consumption

11.1 Supply voltage

Table 8. Supply voltage

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = 5.5 V to 40 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
Device power supply					
V_{SUP}	Device input supply voltage	V_{SUP_UV}	-	36	V
V_{SUP_OV}[1]	VSUP overvoltage threshold	20	-	22	V
V_{SUP_UV}[2]	VSUP undervoltage threshold	4.8	5.0	5.2	V
T_{SUP_OV}	V_{SUP_OV} filtering time	6	10	20	us
T_{SUP_UV}	V_{SUP_UV} filtering time	6	10	20	us
V_{SHS}	LIN and high-side drivers input supply voltage	V_{SHS_UV}	-	36	V
V_{SHS_OV}	VSHS overvoltage threshold	20	-	22	V
V_{SHS_UV}	VSHS undervoltage threshold	4.8	5.0	5.2	V
T_{SHS_OV}	V_{SHS_OV} filtering time	10	15	25	us
T_{SHS_UV}	V_{SHS_UV} filtering time	10	15	25	us
Internal digital supply					
V_{DIG}	Device digital supply voltage	-	1.6	-	V
V_{DIG_OV}	VDIG overvoltage threshold	1.85	2.00	2.15	V
T_{DIG_OV}	V_{DIG_OV} filtering time	0.13	1.00	3.10	us
V_{DIG_POR}	VDIG power-on reset (POR) threshold	1.35	1.44	1.55	V
T_{DIG_POR}	V_{DIG_POR} filtering time	0.13	1.00	3.10	us
Interface supply pins					
V_{DDIO}	VDDIO supply voltage range	3.0	-	5.5	V

[1] The V_{SUP_OV} comparator will trigger a flag in the SPI / I^2C mapping for MCU diagnostic to indicate a load dump happened, but will have no direct action to the safety pins (FS0B, RSTB, LIMP0).

[2] The V_{SUP_UV} comparator will trigger a flag in the SPI / I^2C mapping for MCU diagnostic to indicate a cranking event happened, but will have no direct action to the safety pins (FS0B, RSTB, LIMP0). It is also used at power up to start the device.

11.2 Current consumption

Table 9. Current consumption

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = 5.5 V to 40 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
Quiescent current					
I_{NORMAL}	Current in Normal mode, all regulators ON, no load (I_{OUT} = 0) all high side switched ON (I_{OUT} = 0)	-	8	15	mA
I_{LPON_25}[1]	Current in Low-power ON mode, V1 = HVBUCK = 3.3 V, V1 ON (I_{OUT} = 0), T_A = 25 °C	-	20	36	µA
I_{LPON_85}[1]	Current in Low-power ON mode, V1 = HVBUCK = 3.3 V, V1 ON (I_{OUT} = 0), T_A = 85 °C	-	30	40	µA
I_{LPON_25}	Current in Low-power ON mode, V1 = HVLDO1 = 3.3 V, V1 ON (I_{OUT} = 0), T_A = 25 °C	-	40	60	µA
I_{LPON_85}	Current in Low-power ON mode, V1 = HVLDO1 = 3.3 V, V1 ON (I_{OUT} = 0), T_A = 85 °C	-	50	70	µA
I_{LPOFF_25}	Current in Low-power OFF mode, all regulators OFF, T_A = 25 °C	-	30	50	µA
I_{LPOFF_85}	Current in Low-power OFF mode, all regulators OFF, T_A = 85 °C	-	40	60	µA

[1] In LPON mode, when V1 is a HVBUCK, the quiescent current can be reduced by supplying VBOS from V1 (closing VBOS2V1 switch, if configured by OTP). This way, the current consumption beneficiates from the ratio between VBAT and V1 output.

12 Functional description

The FS23 device has one main state machine. The main state machine manages the power management, the Low-Power modes, and the wake-up sources. The main state machine also manages the monitoring of the power management, the monitoring of the MCU, and the monitoring of an external IC.

In parallel, an INIT state machine is implemented to manage the INIT state of the device. This state is used for the configuration of the device per SPI/I^{2}C.

The safety pins RSTB, FS0B, and LIMP0 are managed independently from each other, in parallel of the main state machine.

12.1 Simplified state machine

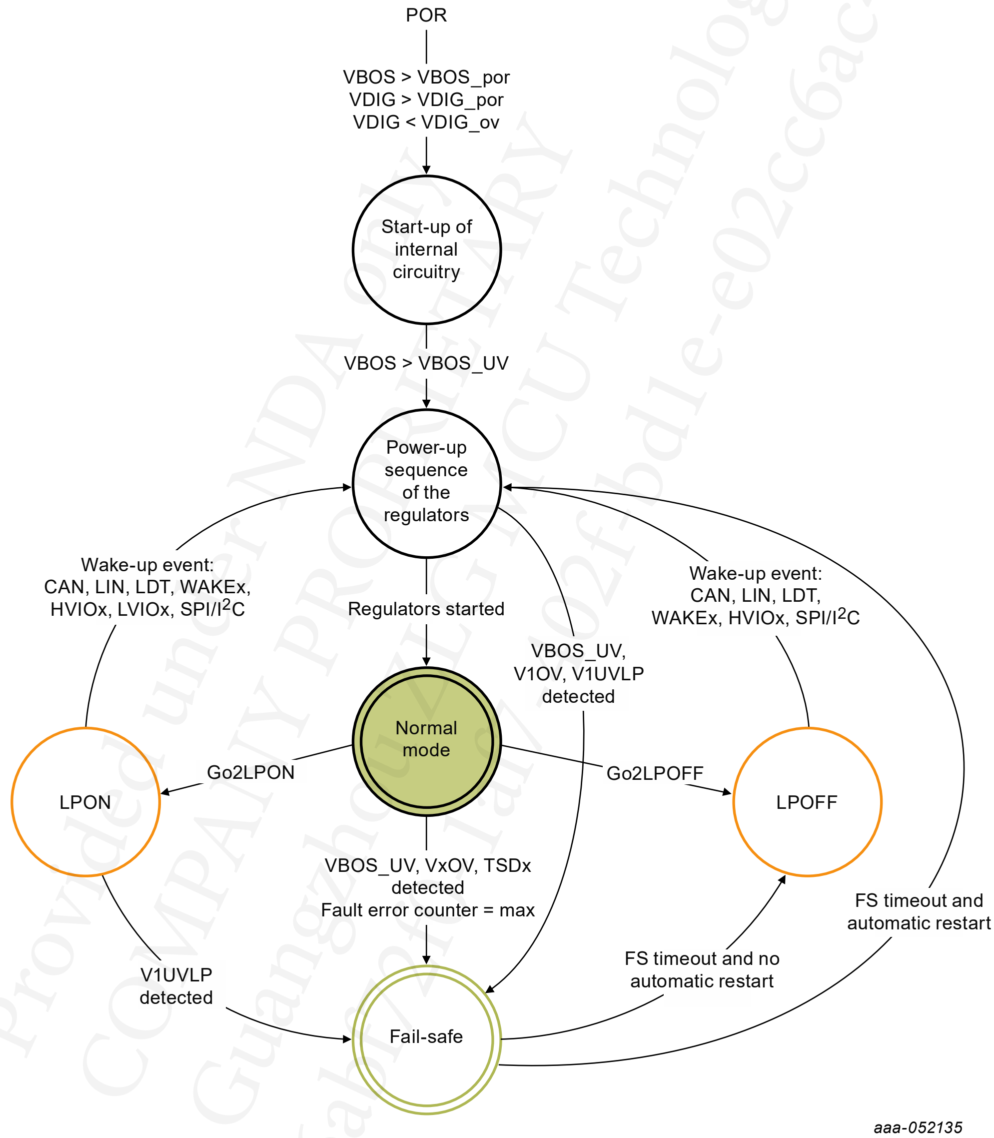


Figure 10. Simplified state machine

12.2 Operation and power modes

The FS23 provides three main operating modes:

- **Normal mode** is intended to be the fully functional mode. All power supplies are enabled as required by the system, and all system functionalities provided by the FS23 are available. In Normal mode, the monitoring is available and all safety features operate in the device.
- **LPON mode** is the Low-power ON mode, providing support to the minimum system requirements with low current consumption from the battery. During the LPON mode, only V1 regulator (HVBUCK or HVLDO1) remains enabled, by default, to supply the microcontroller rail. For V1 HVBUCK configuration, an LPON-specific output voltage can be configured by OTP, and the regulator operates in PFM mode. For V1 HVLDO1 configuration, only the internal PMOS can be used in LPON mode, and the external PNP is turned OFF. HVLDO2 and HVLDO3 can remain in the same state as in Normal mode, depending on the SPI / I^2C configuration. HVIOx and LVIOx only stay active in LPON mode when used as wake-up sources. LPON mode is assumed to be a safe state with no critical activity. Therefore, only monitoring of undervoltage on V1 power rail and MCU watchdog are active to achieve minimum current consumption by the system and FS0B is asserted low.
- **LPOFF mode** is the Low-power OFF mode, with no active system supplies. Logic circuitry is internally supplied to allow proper wake up from any of the available wake-up mechanisms, with the minimum current consumption possible.

The system can wake up from any of the Low-power modes via any of the following wake-up mechanisms available in the device:

- WAKE1 and WAKE2 pins
- HVIOx pins
- LVIOx pins (from LPON only)
- Long duration timer (LDT) expiration
- CAN via wake-up pattern
- LIN via wake-up pattern
- GO2NORMAL SPI or I^2C command via M_SYS_CFG register (from LPON only)

The FS23 will also wake up from LPON ...

- … in case of repeated watchdog error (WD_ERR_CNT = max)
- … in case of pending interrupt for more than T_{INTB_TO}
- … in case of external reset event.

- **Fail-safe mode** is intended to be the safe state of the device. It is used to bring the application in a safe state and to protect the FS23, the MCU and the full system in case of failure of the FS23 or the MCU itself. In this mode, all regulators, safety features and systems features are disabled and the safety pins are asserted.

Table 10 summarizes the operating modes and available features:

Green: Not configurable functions. Orange: Configurable functions

Table 10. Operating modes summary

Function	Operating mode			Fail-safe
	Normal	LPON	LPOFF	
Power management				
HVBUCK	ON, PWM mode	ON, PFM mode	OFF	OFF
or HVLDO1	ON	ON	OFF	OFF
HVLDO2	ON (opt.)[1]	OFF (opt.)[2]	OFF	OFF
HVLDO3	ON (opt.)[1]	OFF (opt.)[2]	OFF	OFF
System features				OFF
CAN transceiver	Full functionality	Wake-up capable	Wake-up capable	OFF
LIN transceiver	Full functionality	Wake-up capable	Wake-up capable	OFF
WAKEx pins	Full functionality	Wake-up capable	Wake-up capable	OFF
HVIOx pins	Full functionality	Wake-up capable	Wake-up capable	OFF
LVIOx pins	Full functionality	Wake-up capable	OFF	OFF
High-side drivers	Full functionality	Cyclic-sense capable	Cyclic-sense capable	OFF
SPI/I^{2}C interface	Full functionality	Wake-up capable	OFF	OFF
Long duration timer (LDT)	Full functionality	Wake-up capable	Wake-up capable	OFF
AMUX	Full functionality	OFF	OFF	OFF
Functional safety				OFF
Voltage monitoring	Full functionality	V1UVLP only	OFF	OFF
Watchdog monitoring	Full functionality	Timeout (opt.)[2]	OFF	OFF
FCCU monitoring	Full functionality	OFF	OFF	OFF
ABIST on demand	Full functionality	OFF	OFF	OFF
INIT CRC check	Full functionality	OFF	OFF	OFF
Clock monitoring	Full functionality	OFF	OFF	OFF
RSTB pin	Full functionality	Released by default	Asserted	Asserted
FS0B pin	Full functionality	Asserted	Asserted	Asserted
LIMP0 pin (and LIMP1/2)	Full functionality	Released by default	Released by default	Asserted

[1] In Normal mode, V2 and V3 regulators can be enabled and disabled by SPI / I^{2}C

[2] In LPON mode, V2 and V3 regulators are considered OFF by default but can be kept ON if previously configured by SPI/I^{2}C. The watchdog can also be kept active (timeout) in LPON, if previously configured by SPI / I^{2}C.

12.3 Main state machine description

Power-on reset and power-up sequence

The FS23 starts when VBOS > V_{BOS_POR} and VDIG > V_{DIG_POR}. VBOS is the first supply to start. The internal 1.6 V supply of the digital circuitry, VDIG, is generated from VBOS. When VBOS > V_{BOS_UV}, the high-power (HP) analog circuitry is enabled and the OTP registers content is loaded into mirror registers. When VSUP > V_{SUP_UV} , the power-up sequence starts in Slot 0, with at least V1 regulator. The remaining regulators start according to the power-up sequencing configured by OTP.

Transition to fail-safe during the power up

During the power-up sequence, if VBOS < V_{BOS_UV}, the device goes to Fail-Safe mode and all regulators are disabled. If an overvoltage or an overtemperature is detected, the device goes to fail-safe, depending on the OTP configuration.

Normal mode

When the power up is finished, the main state machine is in Normal mode, which is the application running mode. If VSUP < VSUP_UV, an interrupt is generated but it has no effect on the state machine. If VBOS < V_{BOS_UV}, the device goes to Fail-Safe mode.

Transitions to low-power modes

The device can go to Low-power modes via an SPI/I^{2}C command from the MCU. A GO2LPOFF command will start the power-down sequence to go in LPOFF mode, and a GO2LPON command will start the power-down sequence to go in LPON mode. The device goes into Low-power mode after the power-down sequence to stop all the regulators in the reverse order of the power-up sequence. In case the device goes in LPON, V1 regulator is not shut down and is kept ON.

Transition to Fail-Safe from Normal mode

In case of loss of VBOS (VBOS < V_{BOS_UV}), the device goes directly to Fail-Safe mode without power-down sequence.

In case of overvoltage detection, or TSD detection on a regulator, depending on OTP configuration, or when the fault error counter reaches its maximum value, the device stops and goes directly to Fail-Safe mode without power-down sequence.

Fail-Safe state exit

Three behaviors are configurable by OTP to exit the Fail-Safe state :

- Automatic restart after T_{FS_DUR} (autoretry feature, configurable by OTP at 100 ms or 4 s)
- Semi-automatic restart after T_{FS_DUR}, the device exits Fail-Safe state and enters LPOFF states, then waits for a wake-up source to transition to M2 and restart (FS_LPOFF = 1 and KEY_OFFON_EN_OTP = 0).
- Restart on Key OFF – Key ON event: Key OFF – Key ON feature is meant to be used when the ignition signal is connected to WAKE1. When enabled, the car driver must turn OFF then ON the ignition signal to restart the device from fail-safe. In this case, the device will only exit fail-safe when WAKE1 = 0 and KEY_OFFON_EN_OTP = 1, and will transition to LPOFF. There, the device will wait for a wake-up event (that is, WAKE1 = 1) to transition to M2 and restart.
- This feature requires WAKE1 to be configured as a direct wake-up source.

Waking up from Low-power modes

When waking up from Low-power modes, it is possible to reduce the startup time by bypassing the M3 state (OTP content loaded in the mirror register) using LOAD_OTP_BYP SPI/I²C bit. This is also valid when exiting fail-safe.

When waking up from LPON only, it is possible to bypass slots 1 and 2 if all of the regulators are configured to start in Slot 0. This can be configured by OTP (SLOT_BYP_OTP) or later by SPI/I²C (SLOT_BYP).

12.4 Detailed functional state diagram

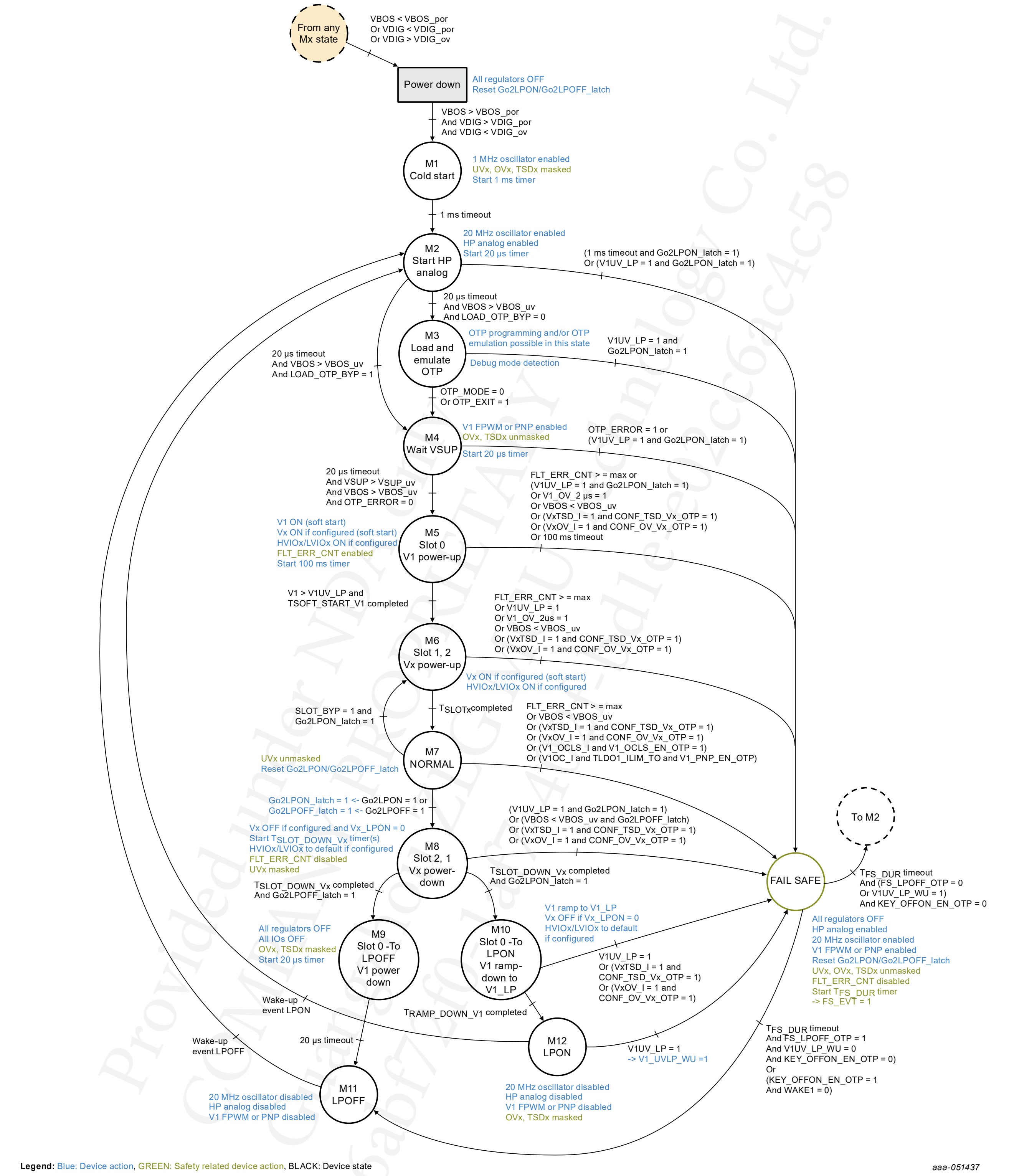


Figure 11. Detailed functional state diagram

12.5 INIT state machine

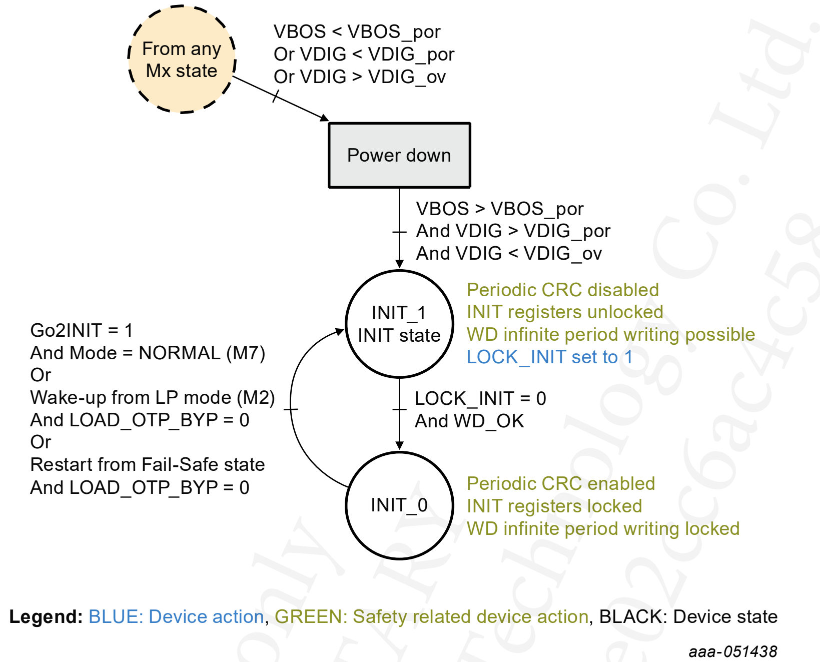


Figure 12. Simplified INIT state diagram

At power-on reset, the device is automatically in INIT state. In this mode, the INIT registers (FS_I_xxxxx) are available for writing and configure the device safety features and reactions. When the device enters INIT state, LOCK_INIT bit is set to 1. The cyclic CRC check that protects these registers is disabled. Also in this mode, the watchdog period can be configured as infinite, which is equivalent to disabling the watchdog. For an MCU programming example, see Section 12.8.

To exit the INIT state, LOCK_INIT is cleared by writing 1, and then a good watchdog refresh must be sent. The INIT registers, as well as the possibility to select infinite watchdog period configuration, are then protected against write access. The cyclic CRC check on the INIT registers is activated, and occurs every 5 ms.

At power-on reset, the first good watchdog refresh must be sent in less than 256 ms, which is the default watchdog period. If not, the watchdog error counter will be incremented, see Section 19.2.2.

In Normal mode, the INIT state can be accessed again by sending a GO2INIT request by SPI / I^{2}C. In this case, if the watchdog is enabled, it must be refreshed every watchdog period.

The device will also enter the INIT state when waking up from LPON or LPOFF states, or when restarting from Fail-Safe state, in case the OTP register loading is not bypassed. This allows the MCU to reconfigure the safety features if needed.

Note: *If the device goes into LPON, LPOFF, or Fail-Safe mode while in INIT state, it stays in INIT state, which can lead to misconfiguration of the device. Therefore, it is recommended to read the INIT_S status bit in M_STATUS register before going to LPON or LPOFF mode, and to go only if the device is no longer in INIT state.*

12.6 Power sequencing

V1 is the first regulator to start automatically in Slot 0, then the other regulators start following the OTP power sequencing configuration. Three slots are available, from SLOT_0 to SLOT_2, to program the start-up sequence of V2 and V3 regulators, as well as I/Os release or assertion.

The power-up sequence starts at SLOT_0 towards SLOT_2. The power-down sequence is executed in reverse order, starting at SLOT_2 toward SLOT_0.

All regulators not assigned in any slot are not started during the power-up sequence. These regulators can be started (or not) later when the main state machine is in NORMAL mode with an SPI/I²C command to write in M_REG_CTRL register if they were enabled by OTP.

Slot 0 duration depends on the device version. In the HVBUCK version (FS232x), Slot 0 lasts at least 500 μs and until the soft start of the DC-DC is done, which depends on the OTP configuration. In the HVLDO1 version (FS230x), it lasts 500 μs (fixed duration).

Slot 1 and Slot 2 always last 500 μs.

When waking up from LPON, it is possible to reduce the start-up time by bypassing Slot 1 and Slot 2. In this case, the V2 and V3 regulators must be configured to start in Slot 0, or later by SPI/I²C, as their correct soft start will not be guaranteed otherwise. Bypassing Slot 1 and Slot 2 is enabled by SPI/I²C with SLOT_BYP bit. It can also be preconfigured by OTP using SLOT_BYP_OTP bit.

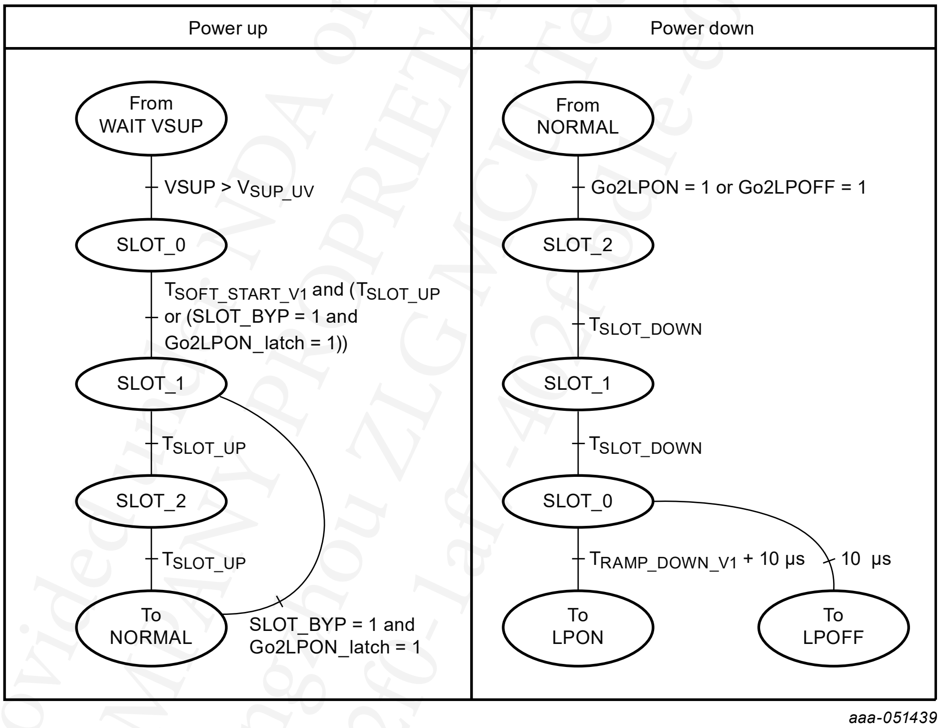


Figure 13. Power sequencing

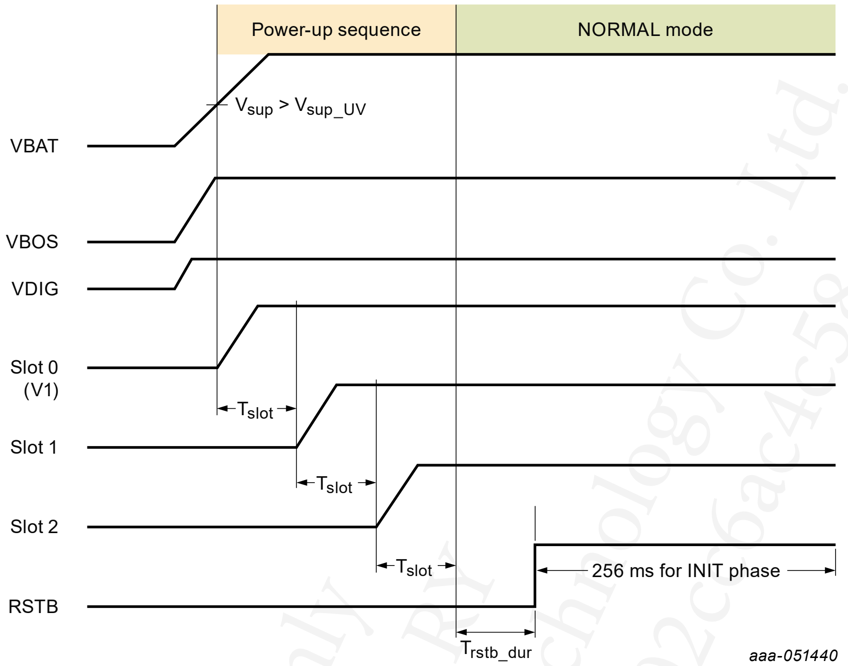


Figure 14. Power-up sequence example

12.7 Debug and OTP modes

OTP mode and Debug mode are intended for use during the development process, not in production applications or vehicles. OTP mode is intended for OTP emulation and OTP programming.

The FS23 enters Debug mode in M3 state of the main state machine when V_{DBG} (DBG pin voltage) > V_{DBG_MODE}. NXP recommend's connecting the DBG pin to the VBOS pin through a diode ($V_{DBG} = V_{BOS} – Vd ≈$ 4.1 V). The Debug mode disables the watchdog (period configured as infinite), the RSTB 8 s timer, the Fail-Safe mode entry via the fault error counter, and locks FS0B low. In Debug mode, CAN and LIN transceivers are set in Active mode by default. The Debug mode status is reported by the DBG_MODE bit in M_SYS1_CFG. To exit Debug mode, write 1 in the DBG_EXIT bit in the M_SYS1_CFG register.

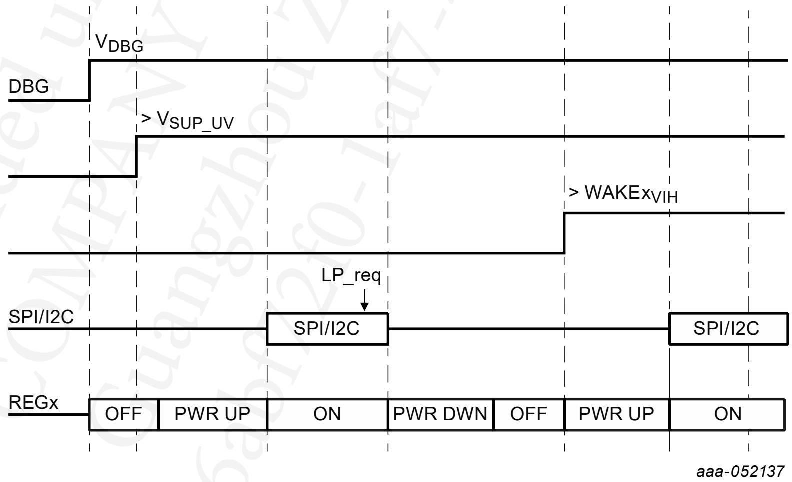


Figure 15. Debug mode

The FS23 enters OTP mode in M3 state of the main state machine, when $V_{DBG} > V_{OTP\_MODE}$. NXP recommends applying V_{OTP_MODE} with an external power supply at DBG pin before applying V_{SUP}. In this case, the diode protects VBOS pin. For OTP programming process, VDBG shall be equal to V_{OTP_MODE}.

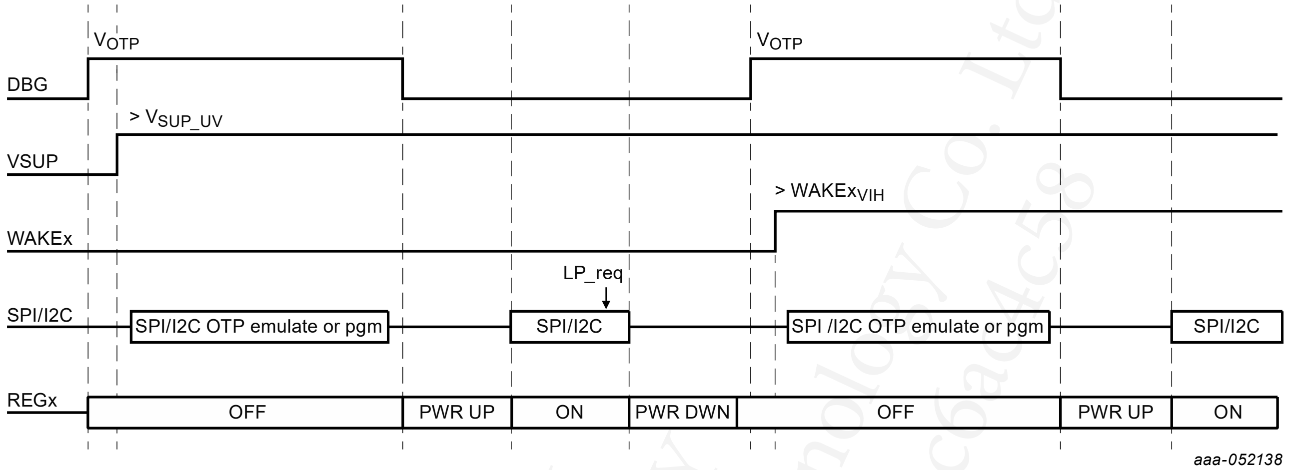


Figure 16. OTP mode time chart

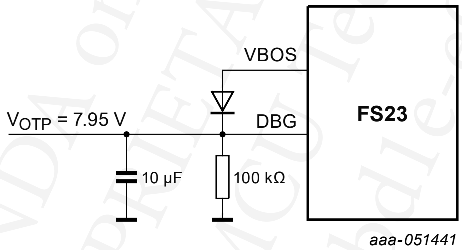


Figure 17. Debug pin (DBG) circuitry

12.7.1 Electrical characteristics

Table 11. Electrical characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = 5.5 V to 40 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
Debug mode					
V_{DBG_MODE}	Voltage to apply at DBG pin to enter Debug mode	3.5	4.5	5.5	V
T_{DBG_MODE}	Debug mode entry filtering time	4	6	15	us
V_{OTP_MODE}	Voltage to apply at DBG pin to program the OTP	7.75	7.95	8.15	V
T_{OTP_MODE}	OTP mode entry filtering time	4.0	5.5	7.0	us
I_{DBG}	DBG pin input current consumption	-	-	60	µA

12.8 MCU programming

MCU programming can be done at any time. When the watchdog functionality is enabled by OTP (WD_INF_OTP = 0), NXP recommends extending the watchdog period (up to 1024 ms) or to set it as infinite (window is fully opened) during INIT phase. This will prevent any watchdog error detection and RSTB pin assertion while programming. If the watchdog is not “disabled” (window set as infinite), the user will have to refresh it during the MCU programming.

The advised procedure to change the watchdog period to infinite is the following:

1. Make sure the FS23 is in Normal mode by reading M_STATUS register.
2. Send a GO2INIT request by writing in M_SYS_CFG register.
3. Make sure the FS23 is in INIT mode by reading M_STATUS register.
4. Set the infinite watchdog period by writing 4b’0000 in the WDW_PERIOD and WDW_RECOVERY fields in FS_WDW register.
5. Exit INIT mode by clearing the LOCK_INIT bit, then sending a good WD refresh.

12.9 Best of supply

12.9.1 Functional description

The VBOS regulator manages the best of supply from VSUP or V1 (in case V1 is an HVBUCK) to efficiently generate the internal biasing of the device, in every Device mode. VBOS is also the supply of V1 high-side and low-side gate drivers in HVBUCK use case.

VBOS undervoltage may not guarantee the full functionality of the device. Consequently, VBOS_UV detection powers down the device by going into Fail-Safe state.

VBOS is composed of two regulators implemented in parallel: VBOS_HP used to supply the HP analog internal biasing, and VBOS_LP used to supply the internal biasing in Low-Power modes. Both VBOS_LP and VBOS_HP are generated from VSUP.

At power up, VBOS_LP is automatically enabled, and VBOS_HP is enabled later when the HP analog circuitry is enabled.

In HVBUCK use case only:

- In Normal mode, VBOS can be connected to V1 if V1 = 5 V (configurable by OTP + SPI/I^{2}C, using VBOS2V1_SW_ALWAYS_EN bit). In this case, VBOS will stay connected to V1 in LPON mode.
- In LPON mode, VBOS can be connected to V1 using VBOS2V1_SW_LP_EN _OTP bit. This feature allows the user to optimize the efficiency, as the current consumption benefits from the VBAT to V1 ratio.
- When waking-up from LPON mode, VBOS will stay connected to V1 if VBOS2V1_SW_ALWAYS_EN = 1.

In HVLDO1 use case, VBOS is always supplied from VSUP.

In LPOFF mode, only VBOS_LP is enabled.

The behavior of VBOS regulator is summarized in Figure 18.

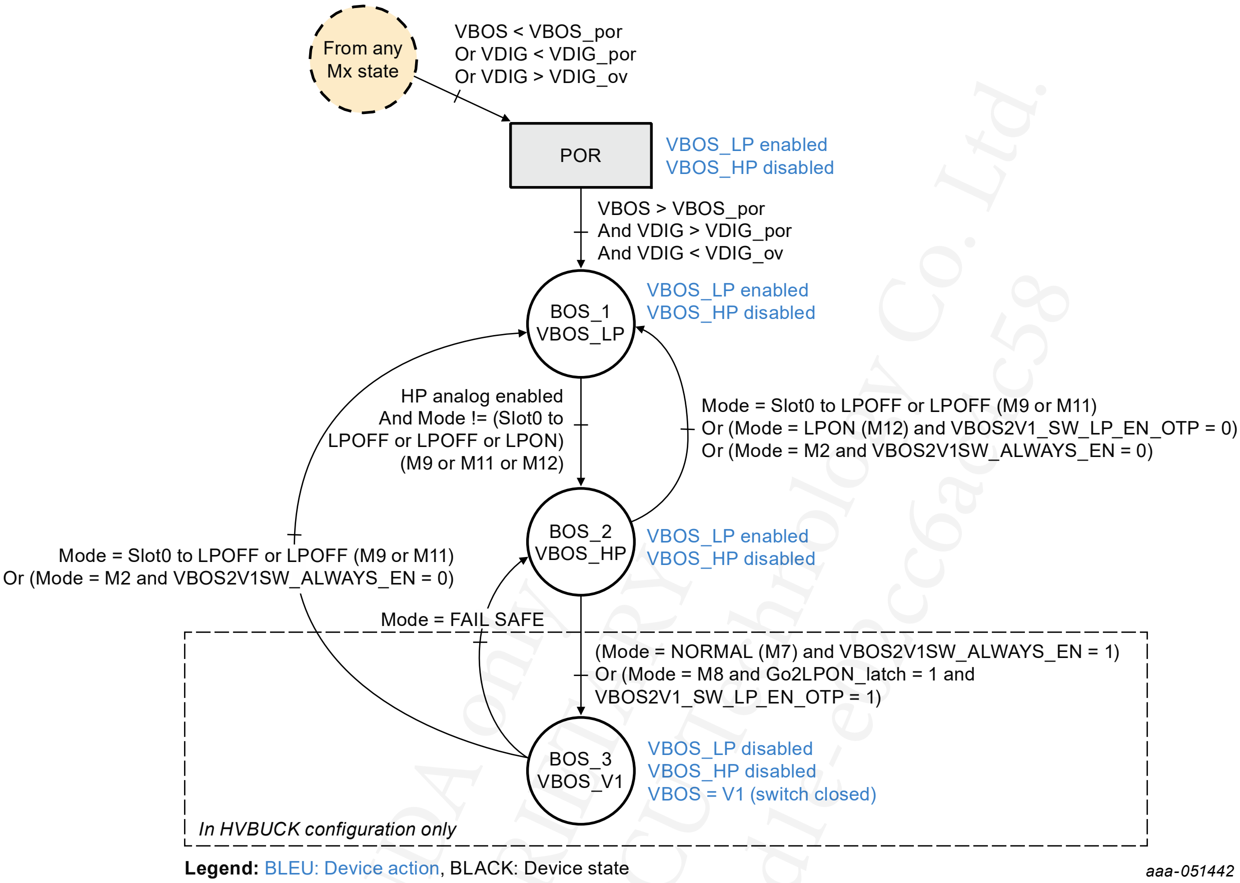


Figure 18. Simplified VBOS state diagram

12.9.2 BOS electrical characteristics

Table 12. Best of supply electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. VSUP = 4 V to 40 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
Static electrical characteristics					
V_{BOS_HP}	Best of supply high-power output voltage	3.4	4.7	5.2	V
V_{BOS_LP}	Best of supply low-power output voltage	3.4	4.3	5.2	V
V_{BOS_UV}	V_{BOS} undervoltage threshold	2.95	3.04	3.13	V
V_{BOS_POR}	V_{BOS} power on reset threshold	2.45	2.6	2.7	V
$V_{BOS\_HP\_DROP}$	Maximum V_{BOS_HP} dropout voltage (VSUP = 4 V, I_{BOS} = 5 mA, VBOS = 3.3 V)	-	-	650	mV
$V_{BOS\_SW\_V1}$	V_{BOS} to V1 switch dropout voltage (V1 = 3.3 V, I_{BOS} = 5 mA)	-	-	50	mV
$I_{BOS\_HP\_LIM}$	Best of supply high-power current limitation	-	-	50	mA
$I_{BOS\_LP\_LIM}$	Best of supply low-power current limitation	-	-	35	mA
Dynamic electrical characteristics					
T_{BOS_UV}	V_{BOS_UVH} and V_{BOS_UVL} filtering time	6	10	20	μs
T_{BOS_POR}	V_{BOS_POR} filtering time	0.13	1.00	3.10	μs
T_{BOS_START}	V_{BOS} low-power starting time (VSUP = 5.2V, C_{OUT_BOS} = 1 μF, VBOS = 2.6V)	-	-	500	μs
External components					
C_{OUT_BOS}	Effective output capacitor	-	1	-	μF

13 Power management

Table 13. FS23 regulators list (400 mA)

Regulator	Type	Input Supply	Output Range	Max DC current
V1	HV Buck regulator	V1_IN (V_{BUCK} / DC_{max_drop} + ((R_{HS_BUCK} + R_{DCR_LBUCK}) x I_{BUCK} x DC_{max_drop}) to 36 V)	3.3 V or 5.0 V	400 mA
	HV Linear regulator	V1_IN (4 V or V1 + 500 mV to 40 V)		100 mA/250 mA
V2	HV Linear regulator	V2_IN (4 V or V2 + 500 mV to 40 V)	3.3 V or 5.0 V	100 mA
V3	HV Linear regulator	V3_IN (4 V or V3 + 500 mV to 40 V)	3.3 V or 5.0 V	150 mA

The FS23 includes three regulators, all supplied in parallel from the battery line. Depending on the part number, the V1 regulator can be a BUCK regulator or a linear regulator.

The FS23 starts when VSUP > V_{SUP_UV}, with VBOS first, followed by V1, then the power-up sequencing configured by OTP for the remaining regulators (LDO2, LDO3).

13.1 HVBUCK: High-voltage buck regulator

13.1.1 Functional description

HVBUCK block is a high-voltage integrated synchronous buck. It can be used to supply the ECU MCU and other local loads inside the ECU.

General operation

The HVBUCK operates in force PWM or PFM modes and uses internal N-type FETs. The output voltage is configurable by OTP. Compensation is ensured by internal circuitry.

The current in the inductor is sensed via the internal FETs. This information is used to compute an average value reflecting the output DC current.

Mode-specific operation

HVBUCK operates in force PWM (pulse width modulation) when the FS23 is in Normal mode and in PFM (pulsed frequency modulation) when the FS23 is in Low-Power ON mode (LPON). HVBUCK output voltage can be different in Normal mode and in LPON mode. The voltage ramp-up/down between the normal and the LPON voltages is done in PWM mode.

Switching frequency

HVBUCK switching frequency in force PWM mode is configurable at 450 kHz or 2.25 MHz by OTP, using BUCK_CLK_OTP bit.

Current limitation

HVBUCK has current limitation protection features. In PWM mode, HVBUCK has both peak and average current limitations, configurable by OTP. In PFM mode, HVBUCK has a peak current limitation, as well configurable by OTP.

When HVBUCK current reaches one of these current limitations, V1OC_I flag is set. The regulator stays enabled, but it induces a duty cycle reduction and therefore an output voltage drop, which could lead to an undervoltage detection (V1UV_I flag generated).

An overcurrent detection is also implemented on the low-side MOSFET, to detect high negative current in case of output short to the battery. In this case, both V1OC_I flag and V1_OCLS_I flag are set and the device transitions to fail-safe depending on OTP configuration using V1_OCLS_EN_OTP.

Input voltage range

HVBUCK output voltage regulation is guaranteed for a minimum V1_IN, which depends on I_{BUCK} current load. To ensure HVBUCK output voltage regulation, V1_IN should be above V_{BUCK} / DC_{max_drop} + ((R_{HS_BUCK} + R_{DCR_LBUCK}) x I_{BUCK} x DC_{max_drop}) with DC_{max_drop} the maximum duty cycle in Dropout mode.

For example, with R_{DCR_LBUCK} = 200 mΩ at I_{BUCK} = 400 mA with V_{BUCK} = 3.3 V, the minimal V1_IN is V_{BUCK} + 527 mV.

Thermal shutdown

When a thermal shutdown is detected, the regulator is disabled and V1TSD_I flag is generated.

13.1.2 Application schematic

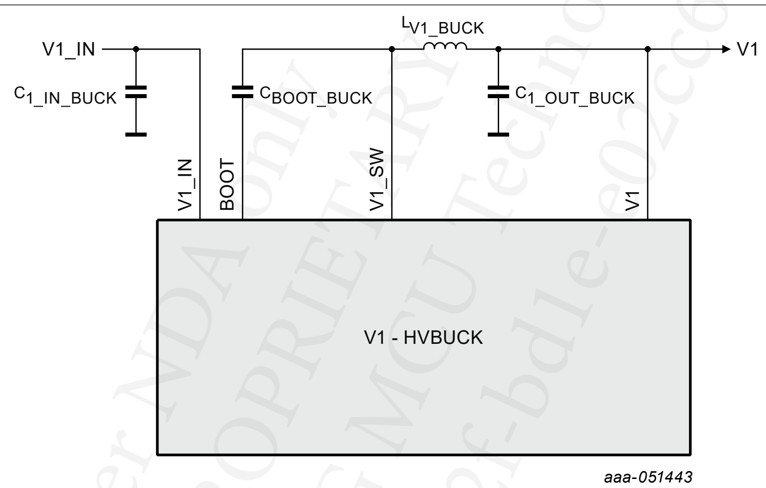


Figure 19. HVBUCK schematic with connection to V_{1_IN}

13.1.3 Electrical characteristics

Table 14. Electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. V1_IN = V_{BUCK_IN} (min) to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Static electrical characteristics					
$V_{BUCK\_IN\_STUP}$	Input-voltage range during startup and softstart time	4.6	-	36	V
V_{BUCK_IN}	Input-voltage range (after start-up)	V_{BUCK} / DC_{max_drop} + ((R_{HS_BUCK} + R_{DCR_LBUCK}) x I_{BUCK} x DC_{max_drop}	-	36	V
V_{BUCK_PWM}	Output-voltage in Normal mode (VV1_BUCK_OTP configuration, 3.3 V or 5 V)	3.3	-	5.0	V
V_{BUCK_PFM}	Output-voltage in Low-Power ON mode (VV1_LP_BUCK_OTP configuration, 3.3 V or 5 V)	3.3	-	5.0	V
V_{BUCK_ACCPWM}	Output-voltage accuracy in PWM mode	-2	-	2	%
V_{BUCK_ACCPFM}	Output-voltage accuracy in PFM mode	-4	-	4	%
I_{BUCK}	Output DC current capability	-	-	400	mA

Table 14. Electrical characteristics*...continued*

T_A = –40 °C to 125 °C, unless otherwise specified. V1_IN = V_{BUCK_IN} (min) to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
I_{BUCK_PFM}	Current capability in PFM mode (Standby mode only)	-	-	100	mA
$\eta_{PEAK\_BUCK\_450k\_3V3}$	Efficiency in PWM mode F_{SW} = 450 kHz L_{V1_BUCK} = 22 µH with DRC = 500 mΩ VSUP = 14 V V_{BUCK} = 3.3 V with I_{BUCK} = 400 mA	-	89	-	%
$\eta_{PEAK\_BUCK\_450k\_5V}$	Efficiency in PWM mode F_{SW} = 450 kHz L_{V1_BUCK} = 22 µH with DRC = 500 mΩ VSUP = 14 V V_{BUCK} = 5 V with I_{BUCK} = 400 mA	-	92.2	-	%
$\eta_{PEAK\_BUCK\_2M2\_3V3}$	Efficiency in PWM mode F_{SW} = 2.25 MHz L_{V1_BUCK} = 4.7 µH with DRC = 500 mΩ VSUP = 14 V V_{BUCK} = 3.3 V with I_{BUCK} = 400 mA	-	83.4	-	%
$\eta_{PEAK\_BUCK\_2M2\_5V}$	Efficiency in PWM mode F_{SW} = 2.2 MHz L_{V1_BUCK} = 4.7 µH with DRC = 500 mΩ VSUP = 14 V V_{BUCK} = 5 V with I_{BUCK} = 400 mA	-	88	-	%
R_{HS_BUCK}	High-side MOSFET RDSON (VBOS = 5 V, including bonding)	150	330	735	mΩ
R_{LS_BUCK}	Low-side MOSFET RDSON (VBOS = 5 V, including bonding)	150	330	735	mΩ
R_{BUCK_DIS}	Discharge resistor (when HVBUCK is disabled – LPOFF)	-	60	100	Ω
$TWARN_{V1}$	Temperature prewarning	125	145	160	°C
TSD_{V1}	Thermal shutdown threshold	175	190	215	°C
TSD_{V1_HYST}	Thermal shutdown threshold hysteresis	6	9	16	°C
$I_{OC\_AVG\_PWM}$ [1]	Average overcurrent threshold in PWM mode BUCK_AVG_OC_PWM_OTP[2:0] = 000 BUCK_AVG_OC_PWM_OTP[2:0] = 001 BUCK_AVG_OC_PWM_OTP[2:0] = 010 BUCK_AVG_OC_PWM_OTP[2:0] = 011 BUCK_AVG_OC_PWM_OTP[2:0] = 100 BUCK_AVG_OC_PWM_OTP[2:0] = 101	130 210 300 390 468 546	200 300 400 500 600 700	290 400 505 630 735 854	mA
$I_{OC\_PK\_PWM/PFM}$ [1]	Peak overcurrent threshold in PWM/PFM mode BUCK_PK_OC_[PWM/PFM]_OTP[2:0] = 010 BUCK_PK_OC_[PWM/PFM]_OTP[2:0] = 011 BUCK_PK_OC_[PWM/PFM]_OTP[2:0] = 100 BUCK_PK_OC_[PWM/PFM]_OTP[2:0] = 101 BUCK_PK_OC_[PWM/PFM]_OTP[2:0] = 110 BUCK_PK_OC_[PWM/PFM]_OTP[2:0] = 111	300 375 468 546 624 702	400 500 600 700 800 900	500 635 732 950 1100 1200	mA
I_{OC_LS}	Low-side FET overcurrent threshold	0.3	0.8	1.1	A
Dynamic electrical characteristics					
F_{SW_BUCK}	Operating frequency in PWM mode: HVBUCK @ 450kHz HVBUCK @ 2.2MHz	405 2.025	450 2.250	495 2.475	kHz MHz
DC_{max_drop}	Maximum duty cycle in Dropout mode	-	90.5	-	%
$t_{V1OV\_DGLT\_STUP}$	Overvoltage deglitch time at startup	1	2	3	µs
t_{V1OV_DGLT}	Overvoltage deglitch time V1MON_OVDGLT_OTP[0] = 0 V1MON_OVDGLT_OTP[0] = 1	20 40	25 45	30 50	µs
t_{V1OC_DGLT}	Overcurrent deglitch time	16	20	24	µs

Table 14. Electrical characteristics*...continued*

T_A = –40 °C to 125 °C, unless otherwise specified. V1_IN = V_{BUCK_IN} (min) to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
t_{V1OCOV_DGLT}	Low-side overcurrent deglitch time	380	-	920	ns
$T_{TSD\_V1\_FILT}$	Thermal shutdown filtering time	6	10	20	µs
t_{BUCK_SS}	Soft-start from 10 % to 90 % BUCK_SS_OTP[1:0] = 00 BUCK _SS_OTP[1:0] = 01 BUCK _SS_OTP[1:0] = 10 BUCK _SS_OTP[1:0] = 11	200 431 873 1753	269 538 1077 2150	410 645 1281 2547	µs
$V_{BUCK\_LINE\_REG\_PWM}$	Transient line in PWM mode @ 450 kHz and 2.2 MHz VSUP = 6 V - 18 V - 6 V and 14 V - 35 V - 14 V I_{BUCK} = 1 mA and 300 mA V_{BUCK} = 3.3V and 5.0 V dv/dt = 100 mV/µs	-3	-	3	%
$V_{BUCK\_LINE\_REG\_DO}$	Transient line after dropout exit @ 450 kHz and 2.2 MHz VSUP = V_{BUCK} - 0.4 V to 14 V I_{BUCK} = 1 mA and 300 mA V_{BUCK} = 3.3V and 5.0 V dv/dt = 200 mV/µs	-3	-	3	%
$V_{BUCK\_LOTR\_PWM}$	Transient load response in PWM mode @ 450 kHz and 2.2 MHz 50 mA to 350 mA step 1 mA to 150 mA step di/dt = 300 mA/µs	-3	-	3	%
$V_{BUCK\_LOTR\_PFM}$	Transient load response in PFM mode mA to 100 mA step di/dt = 100 mA/µs	-3	-	3	%
t_{BUCKHS_SLR}	High-side FET rising slew rate BUCK_SRHSON_OTP[2:0] = 000 BUCK_SRHSON_OTP[2:0] = 001 BUCK_SRHSON_OTP[2:0] = 010 BUCK_SRHSON_OTP[2:0] = 011 BUCK_SRHSON_OTP[2:0] = 100 BUCK_SRHSON_OTP[2:0] = 101 BUCK_SRHSON_OTP[2:0] = 110 BUCK_SRHSON_OTP[2:0] = 111	10 10 7 4.1 3 2.5 1.5 0.5	20 20 15 10 6.3 5 3 2	32 32 23.7 15 12 10 6 4	ns
t_{BUCKHS_SLF}	High-side FET rising slew rate BUCK_SRHSOFF_OTP[1:0] = 00 BUCK_SRHSOFF_OTP[1:0] = 01 BUCK_SRHSOFF_OTP[1:0] = 10 BUCK_SRHSOFF_OTP[1:0] = 11	13 10 6.5 2.5	20 15 10 5	29 21.5 14 9	ns
$t_{BUCKHS\_ON\_450k\_5V}$	High-side FET ON time in PFM mode, V_{BUCK} = 5 V, V_{BUCK_IN} = 12 V, F_{SW} = 450 kHz BUCK_PFM_TON_OTP[1:0] = 00 BUCK_PFM_TON_OTP[1:0] = 01 BUCK_PFM_TON_OTP[1:0] = 10 BUCK_PFM_TON_OTP[1:0] = 11	842 1050 1255 1465	1021 1272.5 1632.5 1772.5	1200 1495 2010 2080	ns
$t_{BUCKHS\_ON\_450k\_3V3}$	High-side FET ON time in PFM mode, V_{BUCK} = 3.3 V, V_{BUCK_IN} = 12 V, F_{SW} = 450 kHz BUCK_PFM_TON_OTP[1:0] = 00 BUCK_PFM_TON_OTP[1:0] = 01 BUCK_PFM_TON_OTP[1:0] = 10 BUCK_PFM_TON_OTP[1:0] = 11	687 858 1026 1195	820 1023 1221 1422.5	953 1188 1426 1650	ns
$t_{BUCKHS\_ON\_2M2\_5V}$	High-side FET ON time in PFM mode, V_{BUCK} = 5 V, V_{BUCK_IN} = 12 V, F_{SW} = 2.2 MHz BUCK_PFM_TON_OTP[1:0] = 00 BUCK_PFM_TON_OTP[1:0] = 01 BUCK_PFM_TON_OTP[1:0] = 10 BUCK_PFM_TON_OTP[1:0] = 11	160 205 254 303	205 263.5 324.5 386	250 322 395 469	ns

Table 14. Electrical characteristics*...continued*

T_A = –40 °C to 125 °C, unless otherwise specified. V1_IN = V_{BUCK_IN} (min) to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
$t_{BUCKHS\_ON\_2M2\_3V3}$	High-side FET ON time in PFM mode, V_{BUCK} = 3.3 V, V_{BUCK_IN} = 12 V, F_{SW} = 2.2 MHz BUCK_PFM_TON_OTP[1:0] = 00 BUCK_PFM_TON_OTP[1:0] = 01 BUCK_PFM_TON_OTP[1:0] = 10 BUCK_PFM_TON_OTP[1:0] = 11	129 165 204 243	162.5 209 57 305	196 253 310 367	ns
$t_{BUCKHS\_OFF\_450k}$	High-side FET OFF time in PFM mode, V_{BUCK_IN} = 12 V, F_{SW} = 450 kHz BUCK_PFM_TOFF_OTP[1:0] = 00 BUCK_PFM_TOFF_OTP[1:0] = 01 BUCK_PFM_TOFF_OTP[1:0] = 10 BUCK_PFM_TOFF_OTP[1:0] = 11	380 730 1070 1420	605 1170 1725 2285	890 1700 2520 3340	ns
$t_{BUCKHS\_OFF\_2M2}$	High-side FET OFF time in PFM mode, V_{BUCK_IN} = 12 V, F_{SW} = 2.2 MHz BUCK_PFM_TOFF_OTP[1:0] = 00 BUCK_PFM_TOFF_OTP[1:0] = 01 BUCK_PFM_TOFF_OTP[1:0] = 10 BUCK_PFM_TOFF_OTP[1:0] = 11	85 160 230 300	130 250 360 475	195 360 525 695	ns
External components					
$C_{1\_IN\_BUCK}$	Nominal[2] input capacitor F_{SW_BUCK} = 450 kHz	4.7	10	-	µF
C_{BOOT_BUCK}	Effective[3] bootstrap capacitor	10	22	33	nF
$L_{V1\_BUCK\_450k}$	Nominal inductor for F_{SW_BUCK} = 450 kHz (±30 % tolerance)	15	22	29	µH
$L_{V1\_BUCK\_2M2}$	Nominal inductor for F_{SW_BUCK} = 2.2 MHz (±30 % tolerance)	3.3	4.7	5.5	µH
$C_{1\_OUT\_BUCK\_450k\_3V3}$	Effective[3] output capacitor for F_{SW_BUCK} = 450 kHz, V_{BUCK} = 3.3 V	25	50	100	µF
$C_{1\_OUT\_BUCK\_450k\_5V}$	Effective[3] output capacitor for F_{SW_BUCK} = 450 kHz, V_{BUCK} = 5 V	25	40	100	µF
$C_{1\_OUT\_BUCK\_2M2\_3V3}$	Effective[3] output capacitor for F_{SW_BUCK} = 2.2 MHz, V_{BUCK} = 3.3 V	6.5	10	30	µF
$C_{1\_OUT\_BUCK\_2M2\_5V}$	Effective[3] output capacitor for F_{SW_BUCK} = 2.2 MHz, V_{BUCK} = 5 V	13	20	40	µF

[1] Average and peak current limits shall be set dependently, taking into account the inductor value.
[2] For all regulators, the nominal capacitor value is the capacitor value normalized.
[3] For all regulators, the effective capacitor value is the capacitor value after Tolerance, DC bias and Aging removal.

13.2 HVBUCK clock management

13.2.1 Description

The HVBUCK 450 kHz or 2.2 MHz clock is generated from a 20 MHz internal oscillator.

A triangular and a pseudo-random spread spectrum feature can be activated and configured by OTP and SPI/ I^2C to reduce the emission of the oscillator fundamental frequency.

13.2.2 Spread spectrum

The internal oscillator can be modulated around the oscillator frequency. The spread spectrum feature can be activated by SPI/I^2C with the MOD_EN bit and the carrier frequency can be selected by SPI/I^2C with the MOD_CONF bit. By default, the spread spectrum is disabled, unless configured differently by OTP.

The main purpose of the spread spectrum is to improve the EMC performance by spreading the energy of the internal oscillator and HVBUCK frequency on VBAT frequency spectrum.

It is recommended to select the triangular spread spectrum for the best performance.

Table 15. Spread spectrum configuration

MOD_EN	MOD_CONF	Spread spectrum
0	X	Disabled
1	0	Triangular (19 kHz)
1	1	Pseudo-random triangular

13.2.2.1 Triangular spread spectrum

The triangular spread spectrum is activated in M_SYS_CFG SPI/I^2C register by setting MOD_EN bit high and MOD_CONF bit low. In this configuration, the internal oscillator is modulated with a triangular carrier frequency of 19 kHz with -10 %/0 % deviation range of the nominal oscillator frequency.

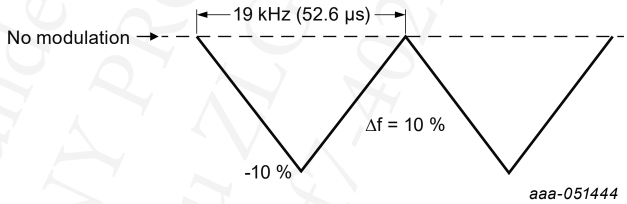


Figure 20. Triangular spread spectrum

13.2.2.2 Pseudo-random triangular spread spectrum

The pseudo-random triangular spread spectrum is activated in M_SYS_CFG SPI / I^2C register by setting MOD_EN bit high and MOD_CONF bit high. In this configuration, the internal oscillator is modulated with a triangular carrier frequency of 19 kHz with -10 %/0 % deviation range of the nominal oscillator frequency, but two random commutations on the carrier slope are added in each half period to increase the spectrum content.

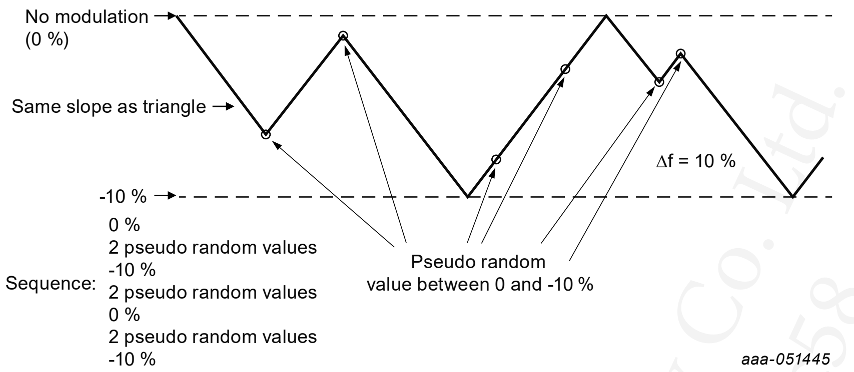


Figure 21. Pseudo-random triangular spread spectrum

13.2.3 Electrical characteristics

Table 16. Clock management electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. V1_IN = VBUCK_IN (min) to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
Internal oscillator					
F_{20MHz}	HVBUCK oscillator nominal frequency	19	20	21	MHz
F_{20MHz_ACC}	HVBUCK oscillator accuracy	-10	-	+10	%
Spread spectrum					
FSS_{MOD}	Spread spectrum frequency modulation	-	19	-	kHz
FSS_{RANGE}	Spread spectrum Range	-	-10	0	%

13.3 HVLDO1: High-voltage linear regulator 1

13.3.1 Functional description

The HVLDO1 is a high-voltage linear-voltage regulator. The HVLDO1 is supplied from the battery. The HVLDO1 is meant to supply the MCU and other loads on the ECU, as an alternative to the HVBUCK (only one of the two options is available by part number). The HVLDO1 is low-power capable and stays enabled in LPON mode.

General operation

The output voltage is configurable by OTP at 3.3 V or 5.0 V.

The HVLDO1 can be used without an external power device (internal PMOS only) or with an external PNP transistor for current sharing. The ratio between the current flowing through the internal PMOS and the external PNP is a fixed ratio of 4. The HVLDO1 maximum output DC current is 100 mA with internal PMOS only.

Mode-specific operation

In LPON mode, only the internal PMOS can be used, and external PNP is turned OFF.

Current limitation and thermal shutdown

An overcurrent detection and a thermal shutdown are implemented on LDO1 to protect the internal pass device. The overcurrent detection limits the current in the internal PMOS and by extension in the external PNP, if used.

The overcurrent threshold is configurable by OTP (CONF_OC_V1_OTP). An additional current limitation is implemented on the PNP base control pin, V1_B, to protect it.

When the overcurrent is reached on the internal PMOS, the regulator stays enabled and V1OC_I flag is generated.

In case an external PNP is used, a timeout (configurable by OTP) is implemented and disables the regulator when an overcurrent is detected for more than $T_{LDO1\_ILIM\_TO}$. In this case, the device transitions to Fail-Safe state and the regulator only restarts when the device restarts.

When a thermal shutdown is detected, the regulator is disabled and V1TSD_I flag is generated. Additionally, the device can transition to Fail-Safe state if configured by OTP.

13.3.2 Application schematic

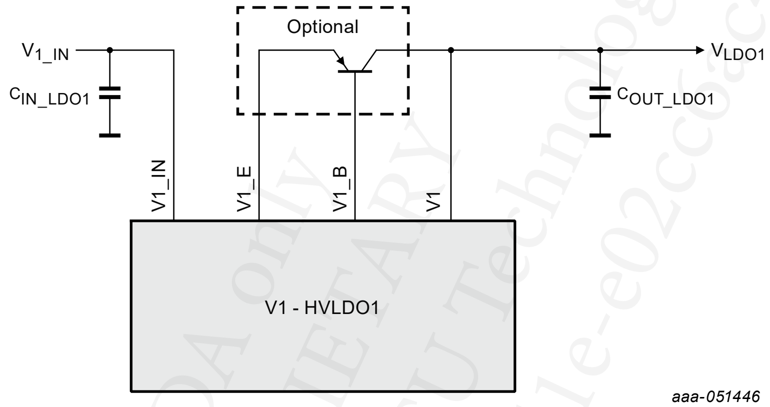


Figure 22. HVLDO1 application schematic, with optional external PNP

13.3.3 Electrical characteristics

Table 17. LDO1 electrical characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. V1_IN = VSUP = 5.5 V to 40 V if V1 = 5 V, or V1_IN = VSUP = 4 V to 40 V if V1 = 3.3 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
Static electrical characteristics					
V_{LDO1_IN}	Input voltage range	4	-	40	V
V_{LDO1}	Output voltage (OTP configurable) VV1_LDO_OTP = 0 VV1_LDO_OTP = 1	3.234 4.9	3.3 5.0	3.366 5.1	V
V_{LDO1_ACC}	Output voltage accuracy	-2	-	2	%
V_{LDO1_DROP}	Maximum output voltage drop in drop out mode (V_{LDO1} = 5 V, V_{LDO1_IN} = 4.5 V, I_{LDO1} = 100 mA)	-	-	500	mV
$I_{LDO1\_PNP\_RATIO}$	Current ratio between int. PMOS and ext. PNP	3.4	4.0	4.6	-
$I_{LDO1\_NORMAL\_PMOS}$	DC current capability in Normal mode (int. PMOS only)	-	-	100	mA
$I_{LDO1\_NORMAL\_PNP}$	DC current capability in Normal mode (with ext. PNP)	-	-	250	mA
I_{LDO1_LPON}	DC current capability in LPON mode (int. PMOS only)	-	-	100	mA
$I_{LDO1\_ILIM\_PMOS}$	Internal PMOS current limitation CONF_OC_V1_OTP = 0 CONF_OC_V1_OTP = 1	150 75	- -	300 160	mA

Table 17. LDO1 electrical characteristics*...continued*

T_A = −40 °C to 125 °C, unless otherwise specified. V1_IN = VSUP = 5.5 V to 40 V if V1 = 5 V, or V1_IN = VSUP = 4 V to 40 V if V1 = 3.3 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
$I_{LDO1\_ILIM\_BASE}$	External PNP base current limitation	10	-	20	mA
TSD_{V1}	Thermal shutdown threshold	175	190	215	°C
TSD_{V1_HYST}	Thermal shutdown threshold hysteresis	6	9	16	°C
Dynamic electrical characteristics					
$T_{LDO1\_SOFT\_START}$	Soft start (from 10 % to 90 %), with and without ext. PNP	150	300	500	µs
T_{LDO1_PDWN}	Discharge time when disabled	-	-	2	ms
T_{LDO1_ILIM}	Current limit filtering time	16	20	36	µs
$T_{TSD\_V1\_FILT}$	Thermal shutdown filtering time	6	10	20	µs
$T_{LDO1\_ILIM\_TO}$	Current limit timeout (ext. PNP) CONF_OC_TO_V1_OTP = 0 CONF_OC_TO_V1_OTP = 1	8 0.8	10 1.0	12 1.2	ms
$V_{LDO1\_LINE\_REG\_NORMAL\_PMOS}$	Transient line response in Normal mode, int. PMOS only VSUP = 6 V - 18 V - 6 V and 14 V - 35 V - 14 V I_{LDO1} = 0.1 mA and 100 mA V_{LDO1} = 3.3V and 5.0 V dv/dt = 100 mV/µs, C_{OUT_LDO1} = 4.7 µF	-3	-	3	%
$V_{LDO1\_LINE\_REG\_NORMAL\_PNP}$	Transient line response in Normal mode, with ext. PNP VSUP = 6 V - 18 V - 6 V and 14 V - 35 V - 14 V I_{LDO1} = 10 mA and 200 mA V_{LDO1} = 3.3V and 5.0 V dv/dt = 100 mV/µs, C_{OUT_LDO1} = 4.7 µF	-3	-	3	%
$V_{LDO1\_LTR\_NORMAL\_PMOS}$	Transient load regulation in Normal mode with int. PMOS only I_{LDO1} = 10m A to 100 mA in 10 us, and from 100 mA to 10 mA in 2us, V_{LDO1} = 3.3 V and 5.0 V, C_{OUT_LDO1} = 4.7 µF	-2	-	2	%
$V_{LDO1\_LTR\_NORMAL\_PNP}$	Transient load regulation in Normal mode with ext. PNP I_{LDO1} = 10 mA to 200 mA in 10 µs, and from 200 mA to 10 mA in 2 µs, V_{LDO1} = 3.3 V and 5.0 V, C_{OUT_LDO1} = 4.7 µF	-2	-	2	%
$V_{LDO1\_LTR\_LPON}$	Transient load regulation in LPON mode I_{LDO1} = 1 mA to 50 mA in 1 µs, and from 50 mA to 1 mA in 10 us. V_{LDO1} = 3.3 V and 5.0 V, C_{OUT_LDO1} = 4.7 µF	-2	-	2	%
V_{LDO1_PSRR}	DC PSRR I_{LDO1} = 0.1 mA to 100 mA, V_{LDO1} = 3.3 V or 5.0V, V_{DROP} = 500 mV (min), 20 Hz to 500 kHz	-	-40	-20	dB
External Components					
C_{IN_LDO1}	Input capacitor (close to V1_IN pin)	-	1.0	-	µF
C_{OUT_LDO1}	Effective output capacitor	2.2	-	4.7	µF
$C_{OUT\_LDO1\_PNP}$	Effective output capacitor, with external PNP	10	-	22	µF

13.4 HVLDO2: High-voltage linear regulator 2

13.4.1 Functional description

General operation

The HVLDO2 is a high-voltage linear-voltage regulator. The HVLDO2 is supplied from the battery. The output voltage is configurable by OTP at 3.3 V or 5.0 V.

The HVLDO2 is low-power capable and can stay enabled in LPON mode. However, if disabled in LPON mode, it cannot be enabled again by SPI/I^{2}C in this mode.

This regulator is meant to supply load on the ECU or outside of the module: a dedicated feedback pin is implemented so a diode can be added between V2_FB pin and V2 pin in order to protect the regulator against short to the battery. If V2 is used as a local supply, V2_FB is shorted to V2 pin.

Open-feedback detection

A comparator is implemented to detect an open between V2_FB and V2 pins. When the difference between the two voltages is higher than $V_{DELTA\_V2\_to\_V2\_FB}$ threshold, the regulator is turned OFF. It can be enabled again by SPI/I^{2}C command.

Current limitation and thermal shutdown

An overcurrent detection and a thermal shutdown are implemented on HVLDO2 to protect the internal pass device. The overcurrent threshold is configurable by OTP (CONF_OC_V2_OTP). When an overcurrent is detected, V2OC_I flag is generated and the regulator remains enabled. It is the MCU's responsibility to disable the regulator by SPI/I^{2}C using the V2DIS bit, and to decide when to enable the regulator using the V2EN bit. When a thermal shutdown is detected, the regulator is disabled and V2TSD_I flag is generated.

13.4.2 Application schematic

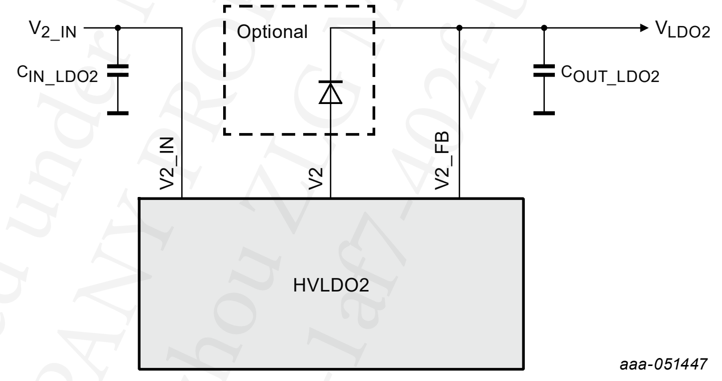


Figure 23. HVLDO2 application schematic

13.4.3 Electrical characteristics

Table 18. HVLDO2 electrical characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. V2_IN = VSUP = 5.5 V to 40 V if V2 = 5 V, or V2_IN = VSUP = 4 V to 40 V if V2 = 3.3 V, unless otherwise specified. I_{LDO2} = 0 to 100 mA unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
Static electrical characteristics					
V_{LDO2_IN}	Input voltage range	4	-	40	V
V_{LDO2}	Output voltage (OTP configurable) VV2_OTP = 0 VV2_OTP = 1	3.234 4.9	3.3 5.0	3.366 5.1	V
V_{LDO2_ACC}	Output voltage accuracy	-2	-	2	%
V_{LDO2_DROP}	Maximum output voltage Drop-in/Drop-out mode (V_{LDO2} = 5 V, V_{LDO2_IN} = 4.5 V, I_{LDO2} = 100 mA)	-	-	500	mV
$V_{DELTA\_V2\_to\_V2\_FB}$	Maximum delta voltage between V2 and V2_FB pin	-	-	2.1	V
I_{LDO2_NORMAL}	DC current capability in Normal mode	-	-	100	mA
I_{LDO2_LPON}	DC current capability in LPON mode	-	-	100	mA
I_{LDO2_ILIM}	Internal PMOS current limitation CONF_OC_V2_OTP = 0 CONF_OC_V2_OTP = 1	150 75	- -	300 160	mA
I_{QLDO2}	Quiescent current, no load (typ @25 °C, max @85°C)	-	15	20	µA
	Quiescent current, I_{LDO2} = 50 µA (typ @25 °C, max @85 °C)	-	20	25	µA
TSD_{V2}	Thermal shutdown threshold	175	190	215	°C
TSD_{V2_HYST}	Thermal shutdown threshold hysteresis	6	9	16	°C
Dynamic electrical characteristics					
$T_{LDO2\_SOFT\_START}$	Soft start (from 10 % to 90 %)	150	300	500	µs
T_{LDO2_PDWN}	Discharge time when disabled	-	-	2	ms
$T_{DELTA\_V2\_to\_V2\_FB}$	Delta voltage between V2 and V2_FB filtering time	3	5	10	µs
T_{LDO2_ILIM}	Current limit filtering time	16	20	36	µs
$T_{TSD\_V2\_FILT}$	Thermal shutdown filtering time	6	10	20	µs
$V_{LDO2\_LINE\_REG\_NORMAL}$	Transient line response in Normal mode VSUP = 6 V - 18 V - 6 V and 14 V - 35 V - 14 V I_{LDO2} = 0.1 mA and 70 mA V_{LDO2} = 3.3 V and 5.0 V dv/dt = 100 mV/µs, C_{OUT_LDO2} = 2.2 µF	-3	-	3	%
$V_{LDO2\_LTR\_NORMAL}$	Transient Load Regulation in Normal mode I_{LDO2} = 10 mA to 50 mA in 10us, and from 50 mA to 10 mA in 10us, V_{LDO2} = 5.0 V, C_{OUT_LDO2} = 2.2 µF	-2	-	2	%
V_{LDO2_PSRR}	DC PSRR I_{LDO2} = 0.1 mA to 100mA, V_{LDO2} = 3.3 V or 5.0 V, V_{DROP} = 500 mV (min), 20 Hz to 500kHz	-	-40	-20	dB
External Components					
C_{IN_LDO2}	Input capacitor (close to V2_IN pin)	-	1.0	-	µF
C_{OUT_LDO2}	Effective output capacitor	2.2	-	4.7	µF

13.5 HVLDO3: High-voltage linear regulator 3

13.5.1 Functional description

General operation

The HVLDO3 is a high-voltage linear-voltage regulator. The HVLDO3 is supplied from the battery. The output voltage is configurable by OTP at 3.3 V or 5.0 V.

The HVLDO3 is low-power capable and can stay enabled in LPON mode. However, if disabled in LPON mode, it cannot be enabled again by SPI/I^2C in this mode.

This regulator is meant to supply the integrated CAN transceiver. The connection is made internally. The HVLDO3 can also supply an additional external transceiver on the module.

Current limitation and thermal shutdown

An overcurrent detection and a thermal shutdown are implemented on the HVLDO3 to protect the internal pass device. The overcurrent threshold is configurable by OTP (CONF_OC_V3_OTP). When an overcurrent is detected, V3OC_I flag is generated and the regulator remains enabled. It is the MCU's responsibility to disable the regulator by SPI/I^2C using V3DIS bit, and to decide when to enable it using V3EN bit. When a thermal shutdown is detected, the regulator is disabled and V3TSD_I flag is generated.

13.5.2 Application schematic

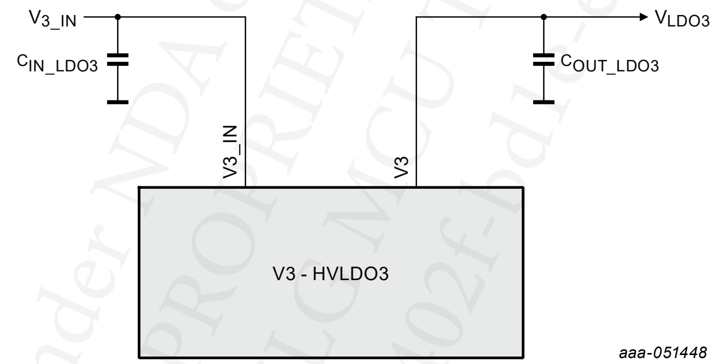


Figure 24. HVLDO3 application schematic.

13.5.3 Electrical characteristics

Table 19. HVLDO3 electrical characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. V3_IN = VSUP = 5.5 V to 40 V if V3 = 5 V, or V3_IN = VSUP = 4 V to 40 V if V3 = 3.3V, unless otherwise specified. I_{LDO3} = 0 to 100 mA unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
Static electrical characteristics					
V_{LDO3_IN}	Input voltage range	4	-	40	V
V_{LDO3}	Output voltage (OTP configurable) VV3_OTP = 0 VV3_OTP = 1	3.234 4.9	3.3 5.0	3.366 5.1	V
V_{LDO3_ACC}	Output voltage accuracy	-2	-	2	%
V_{LDO3_DROP}	Maximum output voltage Drop-in/Drop-out mode (V_{LDO3} = 5 V, V_{LDO3_IN} = 4.5 V, I_{LDO3} = 100 mA)	-	-	500	mV
I_{LDO3_NORMAL}	DC current capability in Normal mode	-	-	I_{LDO3_ILIM}	mA

Table 19. HVLDO3 electrical characteristics*...continued*

T_A = −40 °C to 125 °C, unless otherwise specified. V3_IN = VSUP = 5.5 V to 40 V if V3 = 5 V, or V3_IN = VSUP = 4 V to 40 V if V3 = 3.3V, unless otherwise specified. I_{LDO3} = 0 to 100 mA unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
I_{LDO3_LPON}	DC current capability in LPON mode	-	-	100	mA
I_{LDO3_ILIM}	Internal PMOS current limitation CONF_OC_V3_OTP = 0 CONF_OC_V3_OTP = 1	150 75	- -	300 160	mA
I_{QLDO3}	Quiescent current, no load (typ @25 °C, max @85 °C)	-	15	20	µA
	Quiescent current, I_{LDO3} = 50 µA (typ @25 °C, max @85 °C)	-	20	25	µA
TSD_{V3}	Thermal shutdown threshold	175	190	215	°C
TSD_{V3_HYST}	Thermal shutdown threshold hysteresis	6	9	16	°C
Dynamic electrical characteristics					
$T_{LDO3\_SOFT\_START}$	Soft start (from 10 % to 90 %)	150	300	500	µs
T_{LDO3_PDWN}	Discharge time when disabled	-	-	2	ms
T_{LDO3_ILIM}	Current limit filtering time	16	20	36	µs
$T_{TSD\_V3\_FILT}$	Thermal shutdown filtering time	6	10	20	µs
$V_{LDO3\_LINE\_REG\_NORMAL}$	Transient Line Response in Normal mode VSUP = 6 V - 18 V - 6 V and 14 V - 35 V - 14 V I_{LDO3} = 0.1 mA and 70 mA V_{LDO3} = 3.3 V and 5.0 V dv/dt = 100 mV/µs, C_{OUT_LDO3} = 2.2 µF	-3	-	3	%
$V_{LDO3\_LTR\_NORMAL}$	Transient load regulation in Normal mode I_{LDO3} = 10 mA to 50 mA in 10 us, and from 50 mA to 10 mA in 10 us, V_{LDO3} = 5.0 V, C_{OUT_LDO3} = 2.2 µF	-2	-	2	%
V_{LDO3_PSRR}	DC PSRR I_{LDO3} = 0.1 mA to 100 mA, V_{LDO3} = 3.3 V or 5.0 V, V_{DROP} = 500 mV (min), 20 Hz to 500 kHz	-	-40	-20	dB
External Components					
C_{IN_LDO3}	Input capacitor (close to V3_IN pin)	-	1.0	-	µF
C_{OUT_LDO3}	Effective output capacitor	2.2	-	4.7	µF

14 AMUX: Analog multiplexer

14.1 Functional description

The AMUX pin delivers 32 analog voltage channels to the MCU ADC input. The voltage channels delivered to the AMUX pin can be selected by SPI/I²C. The maximum AMUX output voltage range is VDDIO (3.3 V or 5.0 V). An external output capacitor, C_{AMUX_OUT}, is required for the buffer stability.

14.2 Block diagram

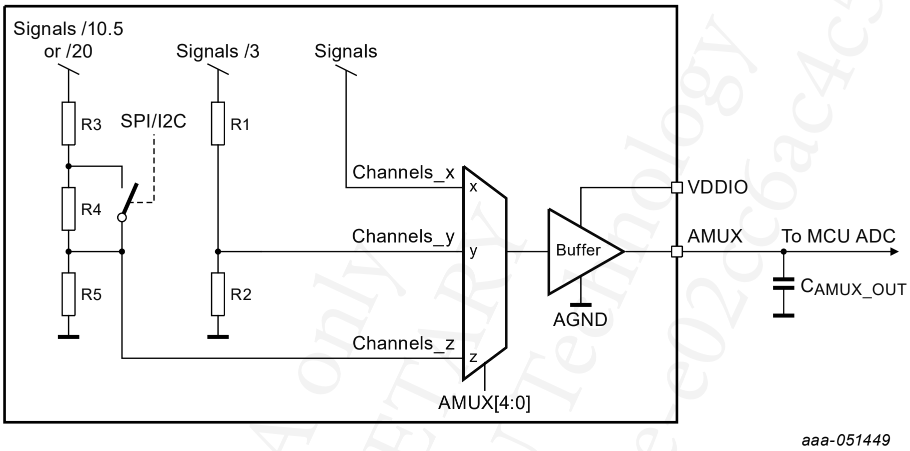


Figure 25. AMUX block diagram.

14.3 Channel selection

Table 20. AMUX output selection

Channel	AMUX[4:0]	Signal selection for AMUX output	AMUX_DIV = 0	AMUX_DIV = 1
0	00000	AGND	1	1
1	00001	VDIG: Internal voltage supply (1.6 V)	1	1
2	00010	V1 voltage	3	3
3	00011	V2 voltage	3	3
4	00100	V3 voltage	3	3
5	00101	VBOS internal voltage	3	3
6	00110	VSUP voltage (Divider ratio configurable by SPI/I²C)	10.5	20
7	00111	VSHS voltage (Divider ratio configurable by SPI/I²C)	10.5	20
8	01000	WAKE1 voltage (Divider ratio configurable by SPI/I²C)	10.5	20
9	01001	WAKE2 voltage (Divider ratio configurable by SPI/I²C)	10.5	20
10	01010	HVIO1 voltage (Divider ratio configurable by SPI/I²C)	10.5	20
11	01011	HVIO2 voltage (Divider ratio configurable by SPI/I²C)	10.5	20
12	01100	Die temperature sensor	1	1
13	01101	V1 temperature sensor	1	1
14	01110	V2 temperature sensor	1	1

Table 20. AMUX output selection*...continued*

Channel	AMUX[4:0]	Signal selection for AMUX output	AMUX_DIV = 0	AMUX_DIV = 1
15	01111	V3 temperature sensor	1	1
16	10000	VDDIO voltage	3	3
> 16	1xxxx	Reserved	N/A	N/A

For temperature sensors, the temperature must be calculated from the AMUX output voltage as per the following formula: $T(°C) = (V_{AMUX} – V_{TEMP25}) / V_{TEMP\_COEFF} + 25$.

14.4 Electrical characteristics

Table 21. AMUX electrical characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = 5.5 V to 40 V, unless otherwise specified. VDDIO = 3.0 V to 5.5 V, unless otherwise specified. I_{AMUX} = -1 mA to 1 mA, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
AMUX					
V_{AMUX_IN}	Input-voltage range for VSUP, VSHS, WAKE1, WAKE2, HVIO1, HVIO2 • AMUX_DIV = 0 • AMUX_DIV = 1	2.5 4.2	- -	22 40	V
V_{AMUX_OUT}	AMUX output-voltage range	0.3	-	VDDIO – 0.2	V
R_{PD_AMUX}	Output pulldown resistance	100	1000	3000	kΩ
V_{AMUX_OFF}	Offset voltage	-7	-	+7	mV
R_{AMUX_ACC}	AMUX ratio accuracy • Ratio 1 • Ratio 3 • Ratio 10.5 (AMUX_DIV = 0) • Ratio 20 (AMUX_DIV = 1)	-0.5 -1.7 -1.9 -1.5	- - - -	0.5 1.7 1.9 1.5	%
V_{TEMP25}	Temperature sensor voltage at 25 °C	1.31	1.38	1.45	V
V_{TEMP_COEFF}	Temperature sensor coefficient	-4.074	-3.880	-3.686	mV/°C
T_{AMUX_SET}	Settling time (from 10 % to 90 % of VDDIO, Rs = 220 Ω, Cout = 10 nF)	-	-	10	us
C_{AMUX_OUT}	Output capacitor	-	-	2	nF
R_{AMUX_OUT}	Output resistor	-	220	-	Ohm

15 I/O interface pins

15.1 WAKE1, WAKE2

WAKE pins are high-voltage inputs used as wake-up sources for the device. WAKE inputs can be used alone or in combination with an high-side driver (HSx) for cyclic sensing.

WAKE1 and WAKE2 are wake-up input signals with analog measurement capability through AMUX. For example, WAKE1 can be connected to a switched VBAT (KL15 line) and WAKE2 to the wake-up output of a CAN or FlexRay transceiver. When a WAKE pin is used as a global pin, a capacitor-resistor-capacitor filter is required. See Section 25.

In Normal mode, any event on WAKE1 pin or WAKE2 pin generates a flag (WKx_I), when not masked (WKx_M). In Low-Power modes, a wake-up event can be generated on level (high or low) or on a cyclic sense event, depending on WKx_WUCFG[1:0] bits.

Wake-up filtering time is configurable by SPI/I^{2}C using WKx_DGLT bits. Internal pulldown and pullup resistors can be enabled, disabled, or configured as cell repeater as per WKxPUPD_OTP[1:0] bits.

Note: *Cell-repeater configuration is used to reduce the current consumption. In this configuration, the pullup or pulldown selection follows the state of the internal buffer output after filtering. If the buffer output is low, pulldown resistor is selected. If the buffer output is high, the pullup resistor is selected.*

15.1.1 WAKE1 as input for Key OFF – Key ON feature

WAKE1 pin can be connected to the ignition signal of the vehicle to implement the Key OFF – Key ON feature. The Key OFF – Key ON feature is enabled via OTP using KEY_OFFON_EN_OTP = 1. When this feature is enabled, the car driver must turn the ignition signal OFF, then ON, to restart the device from fail-safe. As the ignition signal is connected to WAKE1 pin, the device will only exit fail-safe to transition to LPOFF when WAKE1 = 0. In LPOFF, the device will wait for any wake-up event to restart.

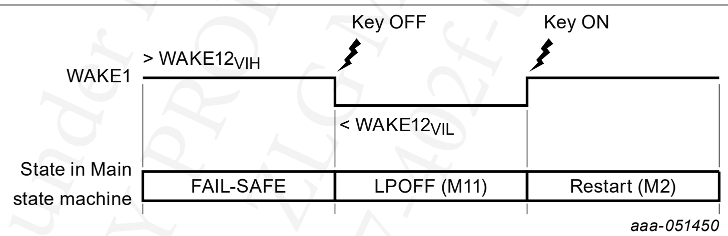


Figure 26. Key OFF – Key ON feature description.

15.1.2 Electrical characteristics

Table 22. WAKE12 electrical characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = 5.5 V to 40 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
WAKE1, WAKE2					
$WAKE12_{VIL}$	Digital low-input voltage threshold (falling)	-	-	2.0	V
$WAKE12_{VIH}$	Digital high-input voltage threshold (rising)	2.97	-	-	V
$WAKE12_{HYST}$	Hysteresis	50	100	400	mV
R_{PD_WAKE12}	Pulldown resistance	100	200	400	kΩ
R_{PU_WAKE12}	Pullup resistance	100	200	400	kΩ
T_{WAKE12_FLT}[1]	Wake-up filtering time • WKx_DGLT = 0 • WKx_DGLT = 1	12 50	15 65	25 80	µs

[1] There is no digital filtering when WAKEx input pin is used as a source to control an high-side driver.

15.2 HVIO1, HVIO2

HVIO pins are high-voltage input/output. When these pins are used as input, they can be used as wake-up sources for the device, alone or in combination with a high-side driver (HSx) for cyclic sense. When configured as output, the pins provide an open-drain output structure.

15.2.1 HVIO1, HVIO2 used as input

HVIOx pins can be used as simple wake-capable inputs. In this case, when the device is in Normal mode, any event on the HVIO1 or HVIO2 pins generates a flag (HVIOx_I), when not masked (HVIOx_M). In Low-Power modes, a wake-up event can be generated on level (high or low) or on a cyclic sense event, depending on HVIOx_WUCFG[1:0] bits.

When used as a wake-up source, wake-up filtering time is configurable by SPI/I^{2}C using HVIOx_DGLT bits. Internal pulldown and pullup resistors can be enabled, disabled, or configured as cell repeater as per HVIOxPUPD_OTP[1:0] bits.

Note: *Cell repeater configuration is used to reduce the current consumption. In this configuration, the pullup or pulldown selection follows the state of the internal buffer output after filtering. If the buffer output is low, pulldown resistor is selected. If the buffer output is high, the pullup resistor is selected.*

When a HVIO pin is used as a global input pin, a a capacitor-resistor-capacitor protection is required. See Section 25.

HVIO1 or HVIO2 can also be configured as FCCU2 input, to provide MCU or external device error detection in combination or independently of FCCU1 pin. This mechanism is detailed in Section 19.3.

15.2.2 HVIO1, HVIO2 used as output

HVIO1 and HVIO2 can be configured as open drain outputs by OTP via HVIOx_OUT_EN_OTP bits. In this case, the output state can be controlled by SPI/I^{2}C using HVIOxHI and HVIOxLO control bits.

HVIO1 and HVIO2 default output state can be configured by OTP using HVIOx_OUT_DFLT_OTP. HVIOx can also be assigned to one of the slots (SLOT_0/1/2) by OTP using HVIOx_SLOT_OTP. In this case, during power up, the pin follows the default state as soon as the OTP configuration is loaded in the mirror registers. The pin state is inverted when the configured slot starts. At power down, the pin goes back to its default value when the configured slot starts. See Figure 27 as an example of HVIO pins configuration, with HVIO1 default state low and assigned to power sequence slot 1, and HVIO2 default state high assigned to power sequence slot 2.

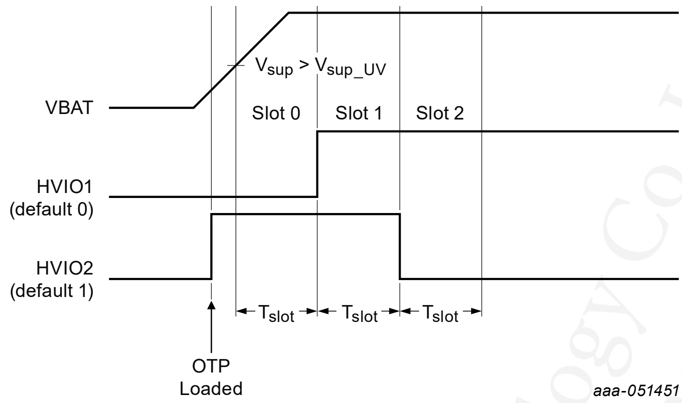


Figure 27. Example of HVIO pins configuration in the slots, at power up

HVIO1 and HVIO2 pins can also be configured respectively as LIMP1 and LIMP2 pseudo-safety outputs. These functions come in addition to LIMP0 safety output pin, and are described in detail in Section 19.6.6.

15.2.3 Electrical characteristics

Table 23. HVIO12 electrical characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = 5.5 V to 40 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
HVIO1, HVIO2					
$HVIO12_{VIL}$	Digital low-input voltage threshold (falling)	-	-	2.0	V
$HVIO12_{VIH}$	Digital high-input voltage threshold (rising)	2.97	-	-	V
$HVIO12_{HYST}$	Hysteresis	50	100	400	mV
$HVIO12_{VOL}$	Low-output level (I_{OUT} = 2 mA)	-	-	0.4	V
$HVIO12_{ILIM}$	Current limitation	4	-	22	mA
R_{PD_HVIO12}	Pulldown resistance	100	200	400	kΩ
R_{PU_HVIO12}	Pullup resistance	100	200	400	kΩ
T_{HVIO12_FLT}[1]	Wake-up filtering time HVIOx_DGLT = 0 HVIOx_DGLT = 1	 12 50	 15 65	 25 80	µs
T_{HVIO12_FALL}	Fall time (external pull up at VUP = 14 V, C_{OUT_HVIO12} = 10 nF)	-	-	35	µs
$T_{HVIO12\_FALL\_nocap}$	Fall time (external pull up at VUP = 14 V, no capacitor)	-	-	10	µs

[1] There is no digital filtering when HVIOx input pin is used as a source to control an high-side driver.

15.3 LVIO3, LVIO4, LVI5, LVO6

The LVIO3 and LVIO4 pins are low-voltage digital input/output. They can be used as digital input as wake-up sources for the device, or as digital outputs.

The MOSI/LVI5 pin can only be used as digital input, and MISO/LVO6 can only be used as digital output.

15.3.1 LVIO3, LVIO4, LVI5 used as input

The LVIO3, LVIO4, and LVI5 pins can be used as simple wake-capable digital inputs. In this case, when the device is in Normal mode, any event on the LVIO3, LVIO4, or LVI5 pins generates a flag (LVIOx_I), when not masked (LVIOx_M). In Low-power ON mode, wake-up events are generated on level (high or low), depending on LVIOx_WUCFG bits.

When used as a wake-up source, internal pulldown and pullup resistors can be enabled or disabled as per LVIOxPUPD_OTP[1:0] bits.

The LVIO3, LVIO4, or LVI5 pins can also be configured as FCCU2 input, to provide MCU or external device error detection in combination or independently of FCCU1 pin. This mechanism is detailed in Section 19.3.

When the SPI communication interface is used, the MOSI/LVI5 pin, is used a MOSI function. See Section 20.2.

15.3.2 LVIO3, LVIO4, LVO6 used as output

The LVIO3 and LVIO4 pins can be configured as digital outputs by OTP via LVIOx_XX_EN_OTP bits. The LVIO3 and LVIO4 pins can then be used as high-side driver, low-side driver, push-pull driver or in 3-state, depending on LVIOx_HS_EN_OTP and LVIOx_LS_EN_OTP bits. The LVIO3 and LVIO4 pins' output states can be controlled by SPI/I^2C using LVIOxHI and LVIOxLO control bits.

The LVIO3 and LVIO4 default output states can be configured by OTP using LVIOx_OUT_DFLT_OTP. They can also be assigned to one of the power sequence slots (SLOT_0/1/2) by OTP using LVIOx_SLOT_OTP. In this case, during power up, the pin follows the default state as soon as the OTP configuration is loaded in the mirror registers and the pin state is inverted when the configured slot starts. At power down, the pin goes back to its default value when the configured slot starts. See Figure 28 as an example of LVIO pins configuration, with LVIO3 default state low and assigned to SLOT_1, and LVIO4 default state high assigned to SLOT_2.

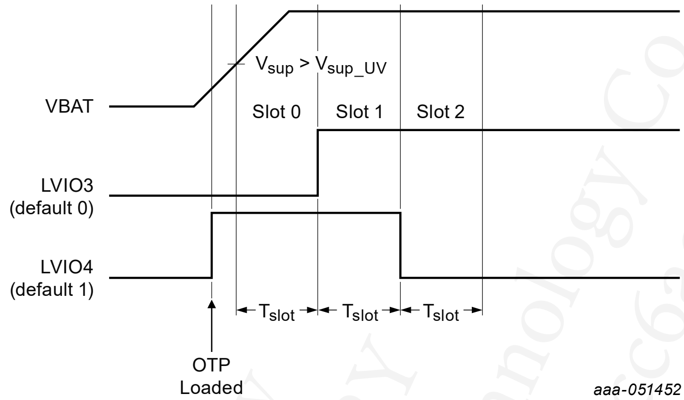


Figure 28. Example of LVIO pins configuration in the slots, at power-up.

The LVIO3 and LVIO4 pins can also be configured respectively as LIMP1 and LIMP2 pseudo-safety outputs, for a local use case. These functions come in addition to the LIMP0 safety output pin, and are described in detail in Section 19.6.6.

LVO6 can be used as push-pull driver, with 3-state default condition, when the I^2C communication interface is used. In this case, it can be controlled by I^2C using LVO6HI and LVO6LO bits.

When SPI communication interface is used, MOSI/LVO6 pin is used as MISO function. See Section 20.2.

15.3.3 Electrical characteristics

Table 24. LVIOx electrical characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = 5.5 V to 40 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
LVIOx					
$LVIO_{VIL}$	Digital low-input voltage threshold (falling)	-	-	0.3 x VDDIO	V
$LVIO_{VIH}$	Digital high-input voltage threshold (rising)	0.7 x VDDIO	-	-	V
$LVIO_{HYST}$	Hysteresis	100	-	600	mV
$LVIO_{VOL}$	Low-output level (I_{OUT} = 2 mA)	-	-	0.4	V
$LVIO_{VOH}$	High-output level (I_{OUT} = -2 mA)	VDDIO – 0.4V	-	-	V
$LVIO_{IQ}$	3-state leakage current	-5	-	5	µA
R_{PD_LVIO}	Pulldown resistance	100	200	400	kΩ
R_{PU_LVIO}	Pullup resistance	100	200	400	kΩ
T_{LVIO_FLT} [1]	Wake-up filtering time	12	15	25	µs

[1] There is no digital filtering when LVIOx input pin is used as a source to control an high-side driver.

15.4 I/Os configuration summary

The following table summarizes the available I/Os configurations.

Table 25. I/Os configurations

Pin	Input function				Output function		
	Simple input	Cyclic sense input	FCCU2 input	MOSI input	Simple output	LIMPx output	MISO output
WAKEx	Yes	Yes	No	No	No	No	No
HVIO1	Yes	Yes	Yes	No	Yes	Yes (LIMP1)	No
HVIO2	Yes	Yes	Yes	No	Yes	Yes (LIMP2)	No
LVIO3	Yes	No	Yes	No	Yes	Yes (LIMP1)	No
LVIO4	Yes	No	Yes	No	Yes	Yes (LIMP2)	No
LVI5	Yes	No	Yes	Yes	No	No	No
LVO6	No	No	No	No	Yes	No	Yes

15.5 INTB

INTB is an open-drain output pin with internal pullup to VDDIO. This pin generates a pulse when an internal interrupt occurs to inform the MCU. Each interrupt can be masked by setting the corresponding inhibit interrupt.

An INTB pulse can be required for diagnosis by the MCU setting the SPI/I^{2}C INTB_REQ bit in M_SYS_CFG register.

15.5.1 Interrupts and wake-up events management

Two types of interruptions must be dissociated:

- The “classic” interrupts used to diagnose the device state and to report events
- The wake-up interrupts used to manage the wake-up from the Low-Power modes

The list of all the interrupts is given in Table 26.

The “classic” interrupts are maskable. If the interrupts are not masked, a pulse will be generated on the INTB pin. Out of Normal mode, most of these interrupt flags will not be generated, because the monitoring functions associated will be disabled. In addition, the WKx_I, HVIOx_I, LVIOx_I, and LVI5_I flags are not generated out of Normal mode.

The I/Os are considered as wake-up sources, with the CAN, LIN, and LDT. A wake-up event on these functions will generate a non-maskable wake-up flag (xxxx_WU_I). An interrupt pulse will be generated on INTB if the wake-up source is enabled following SPI/I^{2}C configuration (xxxx_WUEN[1:0] bits). Each wake-up source can be configured to generate an interrupt, a transition to Normal mode, or both.

In LPON mode, if a wake-up event occurs and the wake-up source is enabled, an interrupt is generated, and/or the device transitions to Normal mode. If only the interrupt generation is enabled, it is the MCU's decision to request a transition to Normal mode or not, via GO2NORMAL SPI/I^{2}C bit.

In LPOFF mode, if a wake-up event occurs and the wake-up source is enabled, the device transitions to Normal mode.

15.5.2 Electrical characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = 5.5 V to 40 V, unless otherwise specified. All voltages referenced to ground.

Table 26. INTB electrical characteristics

Symbol	Parameter	Min	Typ	Max	Unit
Interrupt pin					
$INTB_{PULL-up}$	Internal pullup resistor to VDDIO	5	10	20	kΩ
$INTB_{VOL}$	Low-output level (I_{OUT} = 2 mA)	-	-	0.4	V
$INTB_{VOH}$	High-output level	VDDIO – 0.5V	-	-	V
$INTB_{ILIM}$	INTB current limitation	4.0	-	20	mA
T_{INTB_PULSE}	Pulse duration INTB_DUR = 0 (short) INTB_DUR = 1 (long)	17.5 70	25.0 100	32.5 130	µs
T_{INTB_TO}	INTB timeout for wake-up event	8	10	12	ms
T_{INTB_DLY}	Delay between INTB_REQ command reception and INTB pulse start	36	40	44	µs

Table 27. List of interrupts from main logic

Interrupt	Description	Mask/Enable
Event interrupt		
VSUP_UV_I	VSUP undervoltage	VSUP_UV_M
VSUP_OV_I	VSUP overvoltage	VSUP_OV_M
VSHS_UV_I	VSHS undervoltage	VSHS_UV_M
VSHS_OV_I	VSHS overvoltage	VSHS_OV_M
V1TWARN_I	V1 high-temperature warning	V1TWARN_M
VxTSD_I	Vx overtemperature (x = 1, 2, 3)	VxTSD_M
VxOC_I	Vx overcurrent (x = 1, 2, 3)	VxOC_M
VxOV_I	Vx overvoltage (x = 0,1, 2, 3)	VxOV_M
VxUV_I	Vx undervoltage (x = 0,1, 2, 3)	VxUV_M
WKx_I	WAKEx state change in Normal mode (x = 1, 2)	WKx_M
HVIOx_I	HVIOx state change in Normal mode (x = 1, 2)	HVIOx_M
LVIOx_I	LVIOx state change in Normal mode (x = 3, 4)	LVIOx_M
LVI5	MOSI/LVI5 state change in Normal mode	LVI5_M
LDT_I	Long duration timer event	LDT_M
WAKEx_OL_I	WAKEx open load when used for cyclic sense (x = 1, 2)	WAKEx_OL_M
HVIOx_OL_I	HVIOx open load when used for cyclic sense (x = 1, 2)	HVIOx_OL_M
HS12_TSD_I	HS1 or HS2 overtemperature	HS12_TSD_M
HS34_TSD_I	HS3 or HS4 overtemperature	HS34_TSD_M
HSx_OC_I	HSx overcurrent (x = 1, 2, 3, 4)	HSx_OC_M
HSx_OL_I	HSx open load (x = 1, 2, 3, 4)	HSx_OL_M
CAN_TSD_I	CAN overtemperature	CAN_TSD_M

Table 27. List of interrupts from main logic*...continued*

CAN_TXD_TO_I	CAN dominant timeout	CAN_TXD_TO_M
LIN_TSD_I	LIN overtemperature	LIN_TSD_M
LIN_TXD_TO_I	LIN dominant timeout	LIN_TXD_TO_M
LIN_SC_I	LIN short circuit timeout	LIN_SC_M
FCCU12_I	FCCU1 and FCCU2 error in bi-stable protocol	FCCU12_M
FCCUx_I	FCCUx error when used independently (x = 1, 2)	FCCUx_M
WD_NOK_I	Watchdog refresh error	WD_NOK_M
INIT_CRC_NOK_I	INIT registers CRC error	INIT_CRC_NOK_M
Configurable wake-up event interrupt		
WKx_WU_I	WAKEx wake-up event (x = 1, 2)	WKx_WUEN[1:0]
HVIOx_WU_I	HVIOx wake-up event (x = 1, 2)	HVIOx_WUEN[1:0]
LVIOx_WU_I	LVIOx wake-up event (x = 3, 4)	LVIOx_WUEN[1:0]
LVI5_WU_I	MOSI/LVI5 wake-up event (when I2C is used)	LVI5_WUEN[1:0]
CAN_WU_I	CAN wake-up event	CAN_WUEN[1:0]
LIN_WU_I	LIN wake-up event	LIN_WUEN[1:0]
LDT_WU_I	Long duration timer wake-up event	LDT_WUEN[1:0]
Non-configurable wake-up event interrupt		
GO2NORMAL_WU	SPI/I^2C GO2NORMAL wake-up event	None
INT_TO_WU	Interrupt timeout wake-up event	None
V1_UVLP_WU	V1 undervoltage wake-up event in LPON	None
WD_OFL_WU	Watchdog error counter overflow wake-up event	None
EXT_RSTB_WU	External reset wake-up event	None

16 High-side drivers

16.1 Functional description

The FS23 provides four high-side drivers, supplied by VSHS supply voltage. Each high-side driver (HSx) can be used to drive loads, such as LEDs, or to perform cyclic sense in combination with a high-voltage input (WAKEx, HVIOx).

Each HSx can be controlled by different sources, configurable by SPI/I^{2}C (HSx_SRC_SEL):

- HSx_EN and HSx_DIS SPI/I^{2}C control bits
- Any input (WAKEx, HVIOx, LVIOx, LVI5)
- One of the TIMERx (x = 1, 2, 3) for cyclic sense
- One of the PWMx (x = 1, 2, 3) for LED driving

Undervoltage and overvoltage is implemented on the HSx supply VSHS. In case of under/overvoltage detection, all the HSx are kept enabled or disabled depending on SPI/I^{2}C configuration via HS_VSHSUV_DIS and HS_VSHSOV_DIS bits. When the HSx are disabled because of a UV/OV on VSHS, an automatic recovery of the HSx functions is possible if enabled via HS_VSHSUVOV_REC bit. If not, the MCU will enable the HSx again.

The HSx are monitored by pair for overtemperature. If the temperature of HS1 or HS2 rises above the overtemperature threshold, HS12_TSD_I flag is generated. If the temperature of HS3 or HS4 rises above the overtemperature threshold, HS34_TSD_I flag is generated.

All four HSx are also monitored individually for overcurrent (short-circuit detection) and open load. When an overcurrent is detected, a flag is generated (HSx_OC_I) and the concerned high-side driver is disabled. When an open load is detected, a flag is generated (HSx_OL_I).

16.2 LED driving

The high-side drivers can be used to drive LEDs, with one of the three PWMs configured as source. The frequency of each PWM is configurable between 200 Hz and 400 Hz (PWMx_F), and the duty cycle is configurable on 10 bits from 0 % to 100 % (PWMx_DC[9:0]). A configurable delay (PWMx_DLY) can be applied to both the rising and falling edges of each PWMx in order to limit the inrush current on VSHS supply if multiple HSx are used with a PWM at the same time. LED driving is controlled by SPI/I^{2}C using PWMx_EN bits.

16.3 Cyclic sense

The high-side drivers can be used for cyclic sense, with one of the three TIMERs configured as source and one of the high-voltage inputs among WAKE1, WAKE2, HVIO1, and HVIO2 configured as a sensing input.

Cyclic sense is enabled by SPI/I^{2}C using TIMx_EN bits. Both the period and the ON time of each TIMER are configurable by SPI/I^{2}C using TIMERx_PER[2:0] and TIMERx_ON[3:0] bits. The period is configurable from 10.24 ms to 2048 ms and the ON time is configurable from 0.128 ms to 204.8 ms. A configurable delay (TIMERx_DLY) can be added to both the rising and falling edges of each TIMERx in order to limit the inrush current on the VSHS supply if multiple HSx are used with a TIMER at the same time.

When used for cyclic sense, an HSx is turned ON following the ON time of the associated TIMERx. At the end of each ON time, at each falling edge, the state of the high-voltage input pin is sampled and stored for one period. If two successive samples show different states, a flag is generated. See Figure 29.

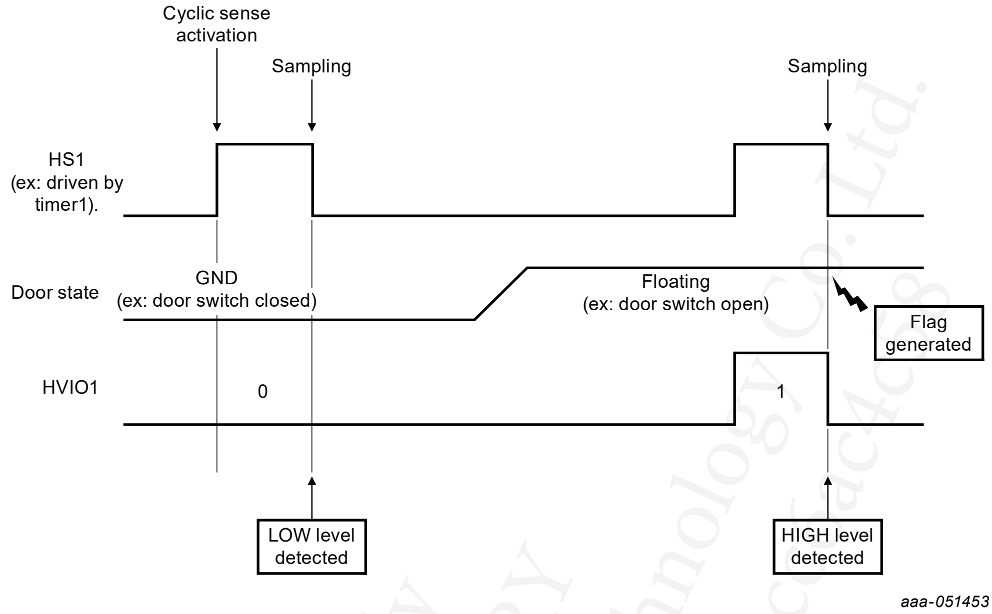


Figure 29. Cyclic sense example with HS1 and HVIO1

External components, a serial resistor, and a capacitor-resistor-capacitor filter, are necessary to limit the current delivered by the high-side driver and protect the high-voltage input pin, used as a global input. See Section 25 for more details.

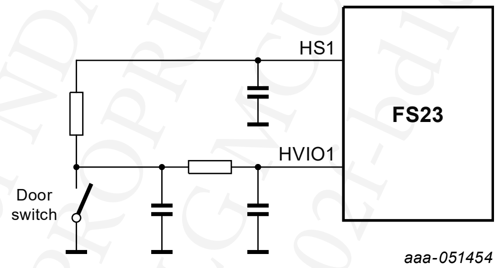


Figure 30. Cyclic sense schematic example with HS1 and HVIO1

A dedicated open-load detection is implemented to detect hardware disconnection between the HSx and the associated input pin when cyclic sense is enabled. The overtemperature and overcurrent monitoring features are also active in Cyclic Sense mode. If any of these faults occurs, the functionality is disabled, and depending on HS_FLT_WU_FORCE bit, the device can be forced to wake up.

16.4 Electrical characteristics

Table 28. High-Side drivers electrical characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. VSHS = 5.5 V to 40 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
HSx static characteristic					
R_{DSON_HSx}	Static drain source ON resistance	-	-	9	Ω
ΔR_{DSON_HSx}	Static drain source ON resistance matching between two HSx	-	3	10	%
I_{ON_HSx}	Incremental current consumption when powering each HS driver (Tj = 85 °C)	-	-	60	µA
I_{Q_HSx}	High-side leakage current, Tj < 85 °C, VSHS<18V	-	-	2	µA
I_{OC_HSx}	Overcurrent shutdown threshold	150	-	380	mA
I_{OL_HSx}	Open-load detection threshold	0.4	-	3.0	mA
$I_{MAX\_REV\_HSx}$	Maximum allowable reverse current	-450	-	-	mA
I_{HSx_CYS}	Cyclic sense current consumption (Tj = 85 °C), HS1 used for cyclic sense, 20ms period, 0.1ms on-time, no load on HS1	-	-	30	µA
HSx dynamic characteristic					
T_{SRON_HSx}	Slew rate rising (from HSx = 2 V to VSHS - 2V), VSHS = 9 V to 18 V, I_{OUT} = 60 mA	0.8	-	2.5	V/µs
T_{SROFF_HSx}	Slew rate falling (from HSx = 2 V to VSHS - 2 V), VSHS = 9 V to 18 V, I_{OUT} = 60 mA	-2.5	-	-0.8	V/µs
T_{SWON_HSx}	Switch ON time (from SPI/I^2C command to HSx = VSHS - 1V), VSHS = 9V to 18V, I_{OUT} = 60 mA	3	-	30	µs
T_{SWOFF_HSx}	Switch OFF time (from SPI / I²C command to HSx = 1V), VSHS = 9 V to 18 V, I_{OUT} = 60 mA	3	-	30	µs
$T_{OC\_FILT\_HSx}$ [1]	Overcurrent filtering time	8	12	25	µs
$T_{OC\_BLK\_HSx}$	Overcurrent blanking time	25	30	35	µs
$T_{OL\_FILT\_HSx}$	Open-load filtering time	50	70	105	µs
$T_{OL\_BLK\_HSx}$	Open-load blanking time	25	30	35	µs
HSx external component					
C_{OUT_HSx}	Output capacitor for one HSx	10	-	47	nF
TIMERx					
T_{START_TIMER}	TIMERx activation delay	-	-	5	ms
$TIMER_{PER\_ACC}$	TIMERx period accuracy	-10	-	10	%
$TIMER_{TON\_ACC}$	TIMERx ON time accuracy (TIMERx_ON = 0001)	-10	-	35	%
	TIMERx ON time accuracy (TIMERx_ON = 0010)	-10	-	24	%
	TIMERx ON time accuracy (TIMERx_ON = 0011)	-10	-	15	%

Table 28. High-Side drivers electrical characteristics*...continued*

T_A = −40 °C to 125 °C, unless otherwise specified. VSHS = 5.5 V to 40 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
	TIMERx ON time accuracy (TIMERx_ON > 0001)	-10	-	12	%
$TIMER_{DLY\_ACC}$	TIMERx delay accuracy	-10	-	10	%
PWMx					
F_{PWM}	PWMx frequency PWMx_F = 0 PWMx_F = 1	180 360	200 400	220 440	Hz
D_{PWM}	PWMx duty cycle (accuracy valid for duty cycles above 5 %)	90*(PWMx_DC/1000)	100*(PWMx_DC/1000)	110*(PWMx_DC/1000)	%
PWM_{DLY_ACC}	PWMx delay accuracy	-10	-	10	%

[1] On resistive short-circuit.

17 Long duration timer

The FS23 features a long duration timer (LDT). The timer is configurable by SPI/I^{2}C and can operate in Normal and in Low-Power modes.

The FS23 provides several functions and offers a wide range of configurable counting periods, as well as a calibration mechanism for oscillator compensation.

The timer can be activated in Normal mode and all prescaler options can be selected to allow timer circuitry verification.

The timer is based on a 24-bit counter, with a 1 MHz/64-input clock, allowing a 1.0 second time base.

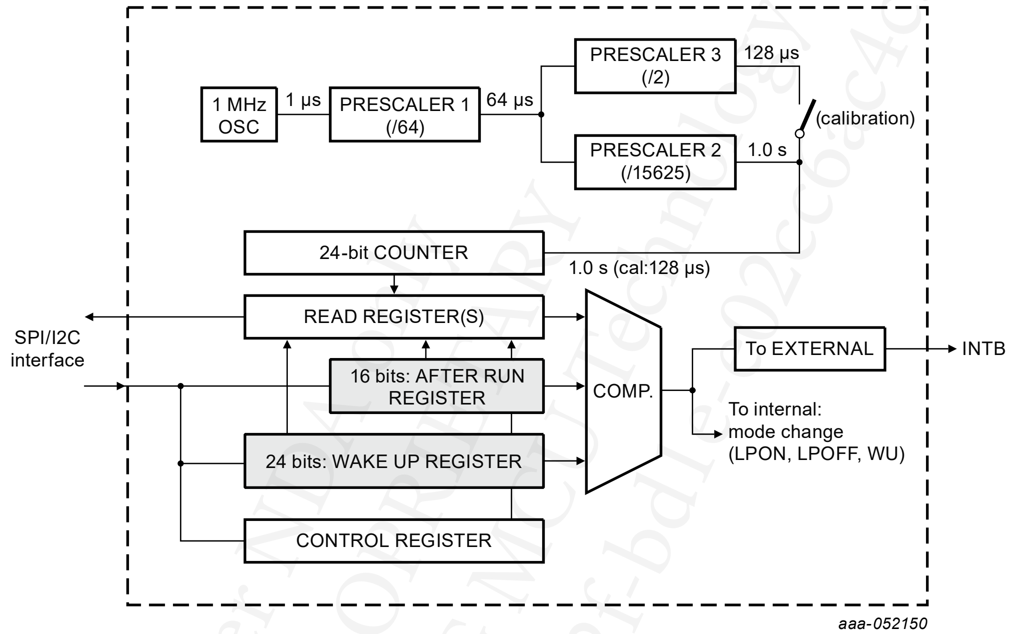


Figure 31. Long duration timer block diagram

In Normal mode operation, the timer can count up to 194 days, with 1 second resolution. In Calibration mode, the prescaler 2 is bypassed and the timer can count up to 36 minutes, with 128 µs resolution.

Table 29. Long duration timer characteristics

Mode	Input clock frequency	Input clock period	Prescaler	Counter resolution	Max count	
Operation	1 MHz	1 µs	64 x 15625	1.0 s	4660 Hrs	194 days
Calibration	1 MHz	1 µs	64 x 2	128 µs	2160 s	36 min

The LDT has two modes of operation based on the prescaler used during the count.

- When LDT_MODE = 0, the LDT is set in long count mode.
- When LDT_MODE = 1, the LDT is set in short count mode.

The LDT_AFTER_RUN[15:0] bits are used to set or to read the after-run target value in Normal mode.

The LDT_WUP_H[7:0] and the LDT_WUP_L[15:0] bits is used to set or to read the wakeup target value, in combination with the LDT_SEL bit:

- LDT_WUP_H[7:0] contains the eight most significant bits of the wake-up target value.
- LDT_WUP_L[15:0] contains the 16 least significant bits of the wake-up target value.

The LDT_SEL bit allows the MCU to either set/read the wake-up target value or to read the current value of the 24 bit LDT counter in the LDT_WUP_H[7:0] and the LDT_WUP_L[15:0] bits.

- When LDT_SEL = 0, the MCU can read or write the wake-up target value in the LDT_WUP_H[7:0] and the LDT_WUP_L[15:0] bits.
- When LDT_SEL = 1, the MCU can read the counter current value (running or not).

The LDT_EN bit is provided to start the LDT timer operation:

- When LDT_EN = 0, the LDT is disabled.
- When LDT_EN = 1, the LDT starts counting as defined in the M_LDT_CTRL and M_LDT_CFGx registers.

The LDT2LP bit selects which Low-power mode (LPON or LPOFF) it needs to go once the after-run timer is expired, when timer function 2 or 3 is selected.

- When LDT2LP = 0, the device goes into LPOFF mode when the after-run timer expires.
- When LDT2LP = 1, the device goes into LPON mode when the after-run timer expires.
- When timer function 4 or 5 is selected and the LDT_EN = 1, the LDT does not start any count until the device enters the corresponding Low-Power mode.

17.1 Calibration procedure

The calibration principle consists of activating the counter for a specific duration and comparing the timing given by the LDT with the MCU's accurate clock and timing. Once the timer expires, the MCU reads back the final timer value and compares it that value with its own accurate time of activation to calculate a time offset. It is recommended to perform the calibration between -20 °C and 85 °C.

Calibration example:

1. Set the Timer mode to short count. Select the timer function 1. Set the after-run value at 65535 (~8.4 s).
2. Start the counter.
3. Read the counter when the MCU RTC reaches 7 s (must be less than 7.5 s with ±10.0 % oscillator accuracy).
4. If the oscillator period is at the exact typical value (absolutely no deviation error), the expected reading is 54688.
5. The exact reading is used to compute the error correction factor ECF = exact_reading/expected_reading.

- ECF < 1 if the oscillator is faster than the exact typical value.
- ECF > 1 if the oscillator is slower than the exact typical value.

After calibration, the new after-run or wake-up values to set the counter are “after run x ECF” and “wake-up x ECF”.

17.2 Timer functions

Table 30. LDT functions

LDT_FNCT[2:0]	LDT Function
000	**Function 1:** In Normal mode, count and generate a flag or an interrupt when the counter reaches the after-run value.
001	**Function 2:** In Normal mode, count until the counter reaches the after-run value and enters Low-Power mode.
010	**Function 3:** In Normal mode, count until the counter reaches the after-run value and enters Low-Power mode. Once in Low-Power mode, count until the counter reaches the wake-up value and wakes up.

Table 30. LDT functions*...continued*

LDT_FNCT[2:0]	LDT Function
011	**Function 4:** In Low-Power mode, count until the counter reaches the wake-up value and wakes up.
100	**Function 5:** In Low-Power mode, count and do not wake up unless the counter overflow occurs or if the device wakes up by wake-up input source.

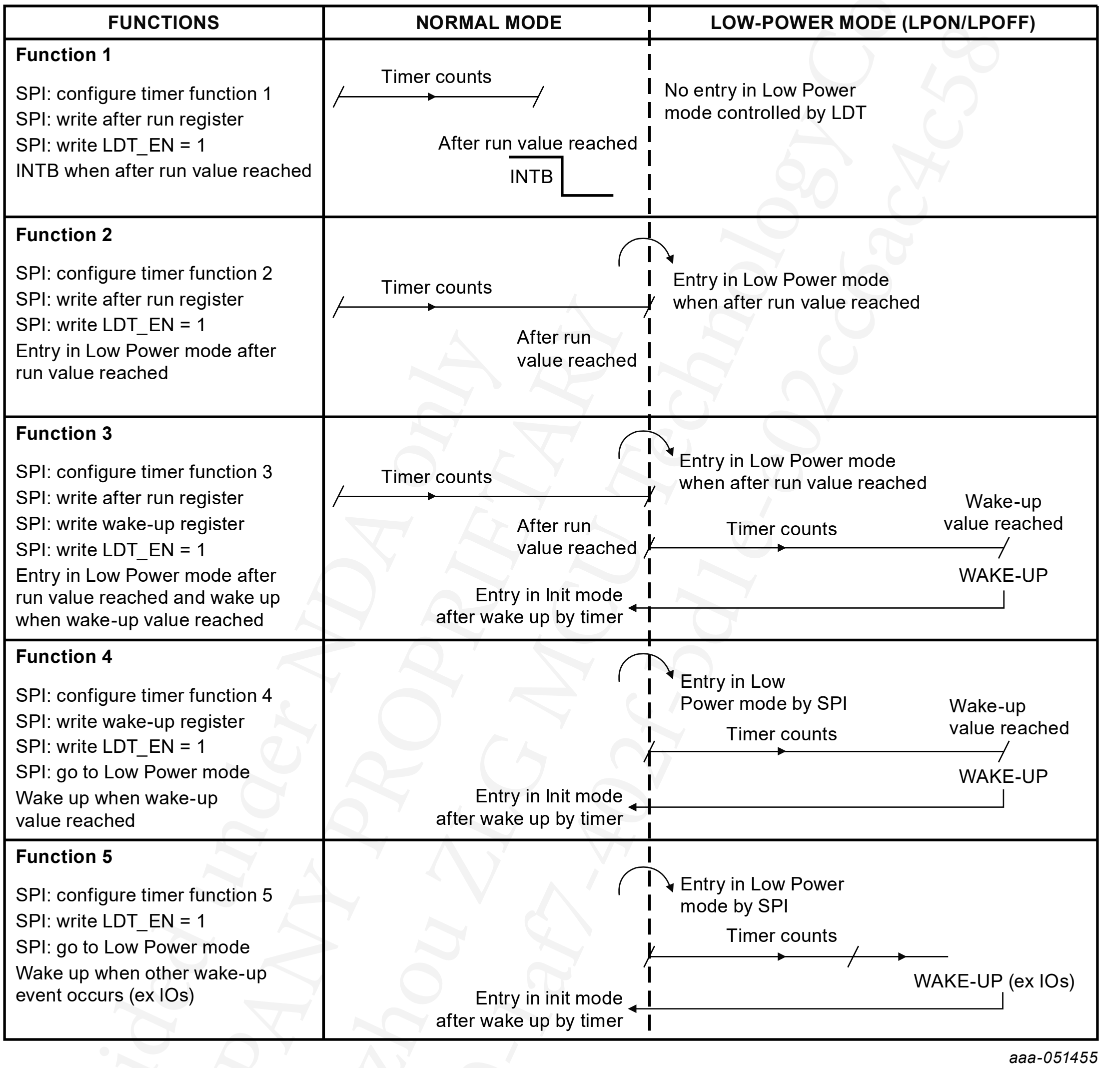


Figure 32. Long Duration Timer functions

17.3 Electrical characteristics

Table 31. Long duration timer characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = 5.5 V to 18.0 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Electrical characteristics					
$F_{IN\_CLK\_LDT}$	Long duration timer source clock (1 MHz/64)	-	15.625	-	kHz
T_{BASE_LDT}	Long duration timer time base LDT_MODE = 0 (long) LDT_MODE = 1 (short)	0.909 116.4	1 128	1.11 142.1	s µs
$I_{Q\_LDT\_85}$	Long duration timer quiescent current consumption (Tj = 85 °C)	-	2	5	µA
$I_{Q\_LDT\_125}$	Long duration timer quiescent current consumption (Ta = 125 °C)	-	5	10	µA
LDT_{ACC1}	Long duration timer accuracy without calibration	-10	-	10	%
LDT_{ACC2}	Long duration timer accuracy with calibration In LPOFF or LPON states Including one month aging drift (max) Including temperature drift 0 °C < ∆Tj < 85 °C	-5	-	5	%
LDT_{DRIFT}	Long duration timer maximum drift per hour after calibration In LPOFF or LPON states Within 20 °C temperature variation.	-1	-	1	%

18 Physical layers

18.1 CAN FD transceiver

The FS23 device includes a 2 Mbps capable, integrated CAN FD transceiver, developed in compliance with the ISO 11898-2:2016 and SAE J2284 standards and SAE J2962-2 (2019) and IEC 62228-3 (2019) for EMC performance. The CAN transceiver is 5 Mbps compatible from electrical point of view. It provides the physical interface between the CAN protocol controller of an MCU and the physical CAN bus.

The CAN FD transceiver bus driver is supplied internally by the V3 regulator.

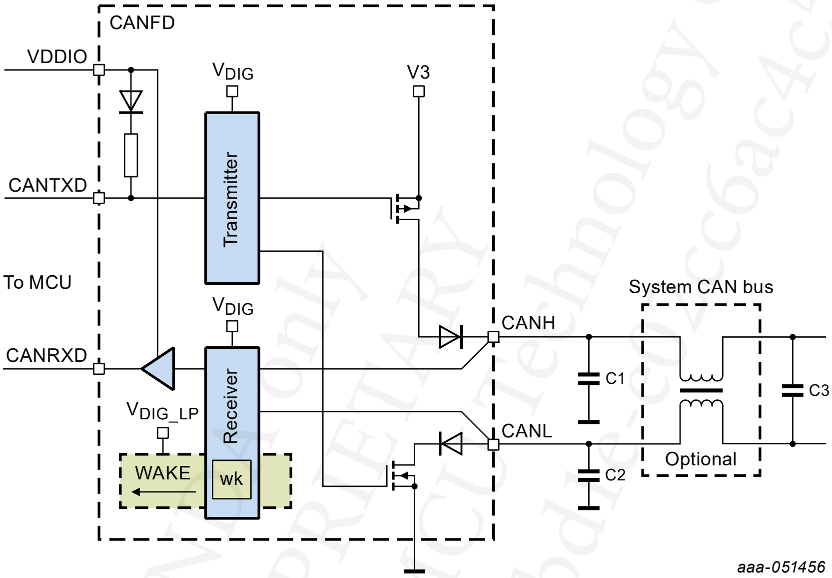


Figure 33. CAN FD transceiver internal diagram, with external components

18.1.1 CAN operating modes

The CAN transceiver has four modes: Off, Wake Capable, Listen Only, and Active. The Listen Only and Active modes are only available when the device is in Normal mode. In Low-Power modes, the transceiver can be in kept in Wake Capable mode in order to be used as a wake-up source for the device and the module.

By default, the CAN FD transceiver is disabled (set to Offline mode) when one of the safety outputs RSTB, FS0B, or LIMP0 is asserted in Normal mode. This can be configured by SPI/I^{2}C using CAN_FS_DIS bit.

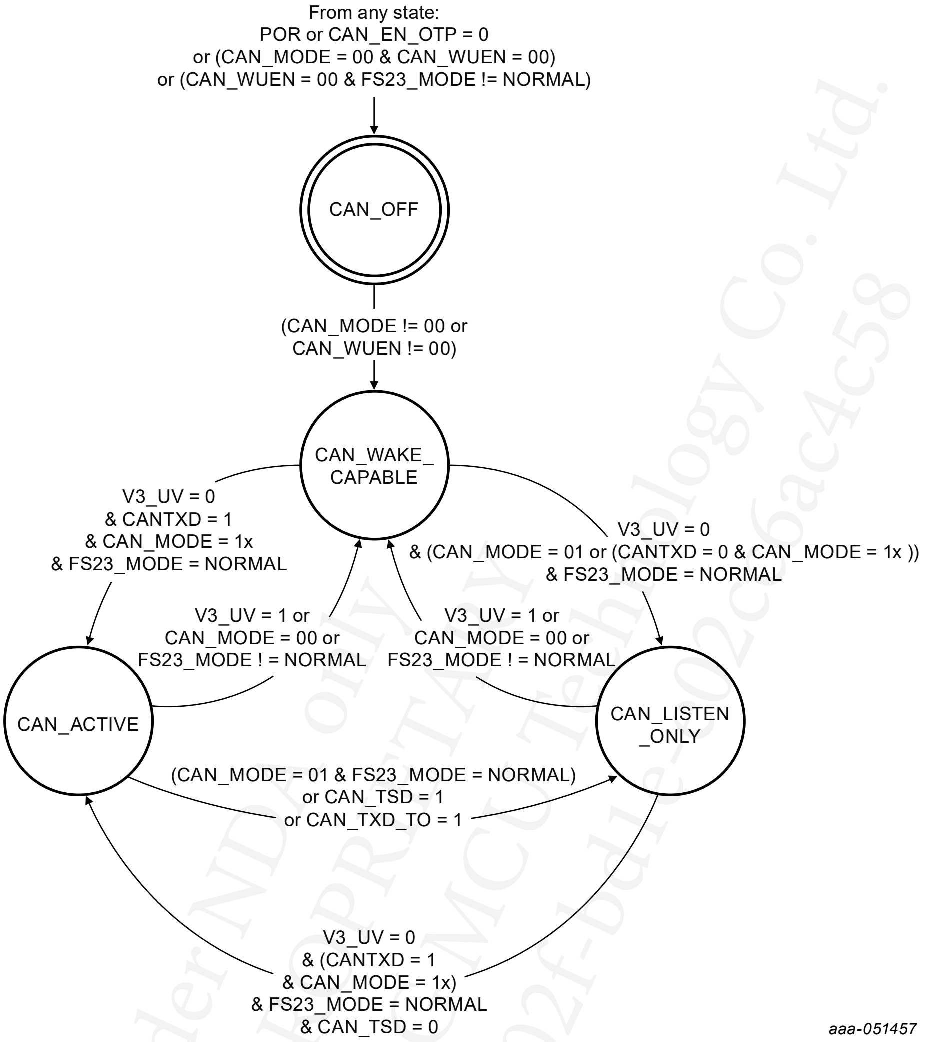


Figure 34. CAN transceiver state machine

18.1.1.1 CAN Off mode

When the CAN mode is set to 2b’00 and the CAN wake-up capability is disabled, or if the device is not in Normal mode (that is, in LPON or LPOFF modes) and the wake-up capability is disabled, the CAN transceiver is in Off mode.

In this mode, the normal and low-power receivers and the transmitter of the CAN transceiver are disabled, the CANH and CANL pins are set high ohmic, and the CANRXD pin is driven high.

18.1.1.2 CAN Wake Capable mode

The CAN transceiver is in Wake Capable mode as soon as the CAN mode is different from 2b’00 or as soon as the wake-up capability of the CAN is enabled, regardless of the device state once powered-up.

In this mode, the CAN transmitter and the CAN normal receiver are disabled, only the low-power wake-capable receiver is enabled to allow wake-up pattern detection and device wake-up. The CANH and CANL pins are biased to ground via the Common mode input resistor $R_{CAN\_IN\_CM}$ and the CANRXD pin is driven high.

18.1.1.3 CAN wake up

When the CAN transceiver is in Wake Capable mode, a valid CAN wake up is detected when a dominant – recessive – dominant pattern is observed on the CAN bus, where the dominant and recessive phases are longer than $T_{CAN\_WU\_FILT}$. The total pattern is valid only if it is shorter than the wake-up timeout time $T_{CAN\_WU\_TO}$.

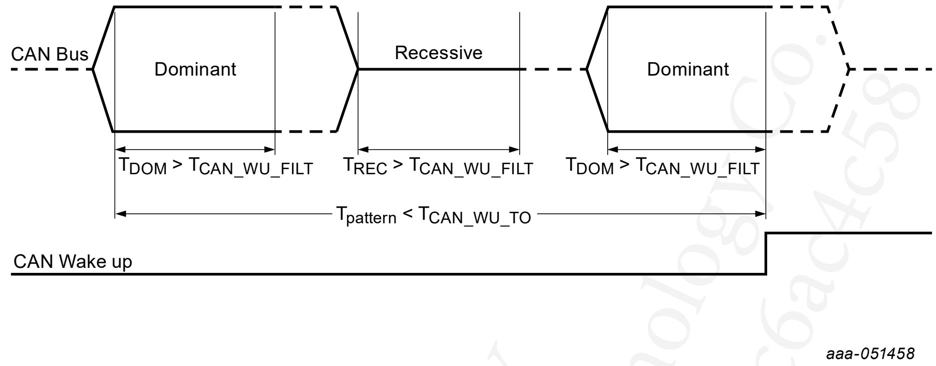


Figure 35. CAN Wake-up timing diagram

18.1.1.4 CAN Listen Only mode

The CAN transceiver Listen Only mode is entered from Wake Capable mode when CAN mode is set to 2b'01 or when CAN mode is set to 2b'10 or 2b'11 and CANTXD is low (bus dominant) for more than $T_{CAN\_DOM\_TO}$. The device must be in Normal mode and no undervoltage on V3 can be detected.

In this mode, CANH and CANL pins are biased to 0.5 x V3 and CANTXD is maintained high by an internal pullup resistor R_{CANTXD_PU} connected to VDDIO.

The low-power wake-up receiver and the transmitter are disabled. Only the normal receiver is enabled. The device is only able to report the bus level to the CANRXD pin. The device is not able to transmit information from TXD to the bus.

18.1.1.5 CAN Active mode

The CAN transceiver Active mode is entered from Wake Capable or Listen Only mode when CAN mode is set to 2b'10 or 2b'11 and CANTXD is high (bus recessive). The device must be in Normal mode and no undervoltage on V3 must be detected. When a TSD or a CAN dominant timeout is detected, the transceiver goes back to Listen Only mode and the transmitter is disabled.

In this mode, the normal receiver and the transmitter are enabled, and the low-power receiver is disabled. The device can transmit information from CANTXD to the CAN bus and report the bus level to the CANRXD pin.

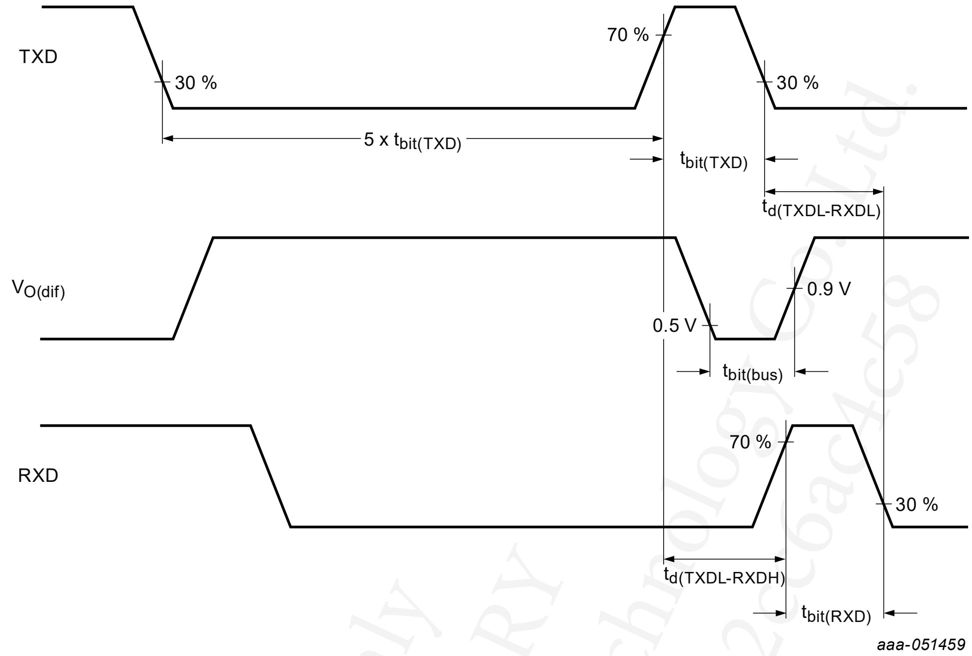


Figure 36. CAN timing definition according to ISO 11898-2:2016

18.1.2 Electrical characteristics

Table 32. CAN FD transceiver characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = 5.5 V to 40 V, unless otherwise specified. V3 = V3UV to 5 V, unless otherwise specified. VDDIO = 3 V to 5.5V, unless otherwise specified. All voltages referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
CANTXD					
Static characteristics					
V_{CANTXD_IH}	CANTXD input threshold high	-	-	0.7 x VDDIO	V
V_{CANTXD_IL}	CANTXD input threshold low	0.3 x VDDIO	-	-	V
R_{CANTXD_PU}	CANTXD pullup resistance	100	200	400	kΩ
CANRXD					
V_{CANRXD_OH}	CANRXD output high level relative to VDDIO, I_{OUT} = -2 mA	0.8 x VDDIO	-	-	V
V_{CANRXD_OL}	CANRXD output low level relative to VDDIO, I_{OUT} = 2 mA	-	-	0.2 x VDDIO	V
CAN Bus					
$V_{CAN\_DIFF\_MAX}$	CAN maximum rating for V_{DIFF}	-5	-	10	V
$V_{CANH\_OUT\_DOM}$	CAN dominant output voltage on pin CANH, Active mode R_L = 50 Ω to 65 Ω	2.75	3.50	4.50	V
$V_{CANL\_OUT\_DOM}$	CAN dominant output voltage on pin CANL, Active mode R_L = 50 Ω to 65 Ω	0.50	1.50	2.25	V

Table 32. CAN FD transceiver characteristics*...continued*

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = 5.5 V to 40 V, unless otherwise specified. V3 = V3UV to 5 V, unless otherwise specified. VDDIO = 3 V to 5.5V, unless otherwise specified. All voltages referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
$V_{CAN\_OUT\_SYM}$	CAN output voltage symmetry (V_{CANH} + V_{CANL}), Active mode, F_{CANTXD} = 1 MHz (2 Mbps), R_L = 60 Ω, C1 = 4.7 nF	0.9 x V3	1 x V3	1.1 x V3	V
$V_{CAN\_OUT\_CM\_PK}$	CAN Common mode peak-to-peak voltage, Active mode	-	-	300	mV
$V_{CAN\_OUT\_DIFF\_DOM}$	CAN bus differential output voltage, Active mode, dominant state, V3 = 4.75 V to 5.5 V, R_L = 50 Ω to 65 Ω	1.5	2.0	3.0	V
	CAN bus differential output voltage, Active mode, dominant state, V3 = 4.75 V to 5.5 V, R_L = 45 Ω to 75 Ω	1.4	2.0	3.3	V
	CAN bus differential output voltage, Active mode, dominant state, V3 = 4.75 V to 5.5 V, R_L = 2240 Ω	1.5	-	5.0	V
$V_{CAN\_OUT\_DIFF\_REC}$	CAN bus differential output voltage, Active mode and Recessive state, or Listen Only mode, or Wake Capable mode, V3 = 4.75 V to 5.5 V, no load, C1 = C2 = CCANRXD = 0 pF	-50	-	50	mV
$V_{CAN\_OUT\_REC\_ACT}$	CAN recessive output voltage, Active mode, no load	2	-	3	V
$V_{CAN\_OUT\_REC\_WC}$	CAN recessive output voltage, Wake Capable mode, no load	-0.1	0	0.1	V
$V_{CAN\_OUT\_DIFF\_REC}$	CAN bus differential output voltage, Wake Capable mode, Recessive state, no load	-0.2	0	0.2	V
$V_{CAN\_OUT\_REC\_LO}$	CAN recessive output voltage, Listen Only mode, no load, V3 = 0 V	2.0	2.5	3.0	V
$V_{CAN\_IN\_DIFF}$	CAN differential receiver threshold voltage, Active or Listen Only mode	0.5	0.7	0.9	V
$V_{CAN\_IN\_DIFF\_LP}$	CAN differential low-power receiver threshold voltage, Wake Capable mode	0.4	0.7	1.15	V
$V_{CAN\_IN\_DIFF\_HYST}$	CAN differential receiver hysteresis voltage, Active or Listen Only mode	50	200	400	mV
$V_{CAN\_IN\_DIFF\_REC}$	CAN Recessive state differential input voltage range, Active or Listen Only mode, V_{CANH} = -12 V to 12 V, V_{CANL} = -12 V to 12 V	-4	-	0.5	V
	CAN recessive state differential input voltage range, no biasing, V_{CANH} = -12 V to 12 V, V_{CANL} = -12 V to 12 V	-4	-	0.4	V
$V_{CAN\_IN\_DIFF\_DOM}$	CAN Dominant state differential input voltage range, Active or Listen Only mode, V_{CANH} = -12 V to 12 V, V_{CANL} = -12 V to 12 V	0.9	-	9.0	V
	CAN dominant state differential input voltage range, no biasing, V_{CANH} = -12 V to 12 V, V_{CANL} = -12 V to 12 V	1.1	-	9.0	V
$R_{CAN\_IN\_CM}$	CAN Common mode input resistance, Active mode, V_{CANH} = -2 V to 7 V, V_{CANL} = -2 V to 7 V	6	-	50	kΩ
$R_{CAN\_IN\_DIFF}$	CAN differential input resistance, V_{CANH} = -2 V to 7 V, V_{CANL} = -2 V to 7 V	12		100	kΩ
ΔR_{CAN_IN}	CAN input resistance deviation, V_{CANH} = V_{CANL} = 5 V	-3	-	3	%
$C_{CAN\_IN\_CM}$	CAN Common mode input capacitance	-	-	20	pF
$C_{CAN\_IN\_DIFF}$	CAN differential input capacitance	-	-	10	pF

Table 32. CAN FD transceiver characteristics*...continued*

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = 5.5 V to 40 V, unless otherwise specified. V3 = V3UV to 5 V, unless otherwise specified. VDDIO = 3 V to 5.5V, unless otherwise specified. All voltages referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
$I_{CANH\_OUT\_SC}$	CANH short circuit output current, Active mode, Dominant state, V3 = 5 V, V_{CANH} = -15 V to 27 V	-115	-	-	mA
$I_{CANL\_OUT\_SC}$	CANL short circuit output current, Active mode, Dominant state, V3 = 5 V, V_{CANL} = -15 V to 27 V	-	-	115	mA
$I_{CAN\_OUT\_REC}$	CAN recessive output current, Recessive state, V_{CANH} = V_{CANL} = -27 V to 32 V	-3	-	3	mA
$I_{CAN\_ACT\_DOM}$	CAN current consumption, Active mode, Dominant state, Tj = 150 °C, V3 = 5 V	23	39	60	mA
$I_{CAN\_ACT\_REC}$	CAN current consumption, Active mode, Recessive state, Tj = 150 °C, V3 = 5 V	1	4	7	mA
I_{CAN_WU}	CAN current consumption, wake-up capability, Tj = 85 °C, VBOS = 5 V	1.5	3	7	µA
I_{QCANH}	CAN input leakage current, V_{CANH} = 5 V, all supply inputs connected to GND	-10	-	10	µA
I_{QCANL}	CAN input leakage current, V_{CANL} = 5 V, all supply inputs connected to GND	-10	-	10	µA
Dynamic characteristics					
T_{CAN_EN}	Setup time needed when going to Active mode of the transceiver before sending data.	15	17	19	µs
$T_{CAN\_DOM\_TO}$	CAN CANTXD dominant timeout time	0.8	-	9.0	ms
T_{CAN_LOOP}	CAN loop delay time from CANTXD to CANRXD, C_{CANRXD} = 15 pF, R_{CAN} = 45 Ω to 70 Ω, C_{CAN} = 100 pF, F_{CANTXD} < 2.5 MHz	-	-	255	ns
$T_{CAN\_TX2BUS\_DOM}$	CAN delay time from CANTXD to bus dominant	-	-	127.5	ns
$T_{CAN\_TX2BUS\_REC}$	CAN delay time from CANTXD to bus recessive	-	-	127.5	ns
$T_{CAN\_BUS2RX\_DOM}$	CAN delay time from bus dominant to CANRXD	-	-	127.5	ns
$T_{CAN\_BUS2RX\_REC}$	CAN delay time from bus recessive to CANRXD	-	-	127.5	ns
$T_{CAN\_BIT\_RX\_2M}$	CAN received recessive bit width @ 2 Mbps, R_L = 60 Ω, C_{CANRXD} = 15 pF, C_1 = 0 nF , C_2 = 100 pF	400	500	550	ns
$T_{CAN\_BIT\_RX\_5M}$	CAN received recessive bit width @ 5 Mbps, R_L = 60 Ω, C_{CANRXD} = 15 pF, C_1 = 0 nF , C_2 = 100 pF	120	200	220	ns
$T_{CAN\_BIT\_BUS\_2M}$	CAN transmitted recessive bit width @ 2 Mbps, R_L = 60 Ω, C_{CANRXD} = 15 pF, C_1 = 0 nF , C_2 = 100 pF	435	500	530	ns
$T_{CAN\_BIT\_BUS\_5M}$	CAN transmitted recessive bit width @ 5 Mbps, R_L = 60 Ω, C_{CANRXD} = 15 pF, C_1 = 0 nF , C_2 = 100 pF	155	200	210	ns
$\Delta T_{CAN\_BIT\_RXBUS\_2M}$	CAN receiver timing symmetry @ 2 Mbps, R_L = 60 Ω, C_{CANRXD} = 15 pF, C_1 = 0 nF , C_2 = 100 pF	-65	-	40	ns
$\Delta T_{CAN\_BIT\_RXBUS\_5M}$	CAN receiver timing symmetry @ 5 Mbps, R_L = 60 Ω, C_{CANRXD} = 15 pF, C_1 = 0 nF , C_2 = 100 pF	-45	-	15	ns

Table 32. CAN FD transceiver characteristics...*continued*

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = 5.5 V to 40 V, unless otherwise specified. V3 = V3UV to 5 V, unless otherwise specified. VDDIO = 3 V to 5.5V, unless otherwise specified. All voltages referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
$T_{CAN\_WU\_FILT}$	CAN recessive/dominant filter time for wake-up	0.5	1.4	1.8	us
$T_{CAN\_WU\_TO}$	CAN wake-up timeout time	0.8	-	10.0	ms

18.2 LIN transceiver

The FS23 device includes an integrated LIN transceiver, developed in compliance with the LIN 2.2a (ISO 17987-4) and SAE-J2602-2 standards, SAE J2962-1 (2019), and IEC 62228-2 (2016) for EMC performance. It provides the physical interface between the LIN controller of an MCU and the physical LIN bus.

The LIN transceiver bus driver is supplied by VSHS supply input. Depending on the OTP configuration via VSHS_UV_DIS_OTP bit, the transceiver is deactivated or kept on in case of VSHS_UV (5 V). It can operate up to VSHS = 28 V.

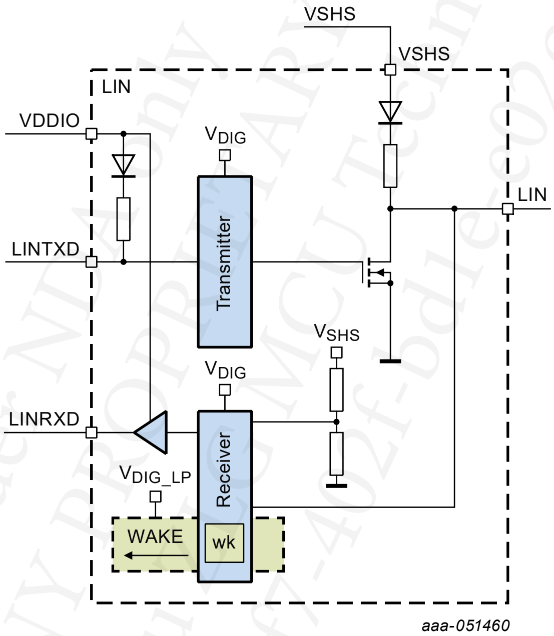


Figure 37. LIN transceiver internal diagram

18.2.1 LIN operating modes

The LIN transceiver has four modes: Off, Wake Capable, Listen Only, and Active. The Listen Only and Active modes are only available when the device is in Normal mode. In Low-Power modes, the transceiver can be in kept in Wake Capable mode in order to be used as a wake-up source for the device and the module.

By default, the LIN transceiver is disabled (set to Offline mode) when one of the safety outputs RSTB, FS0B, or LIMP0 is asserted. This can be configured by SPI/I^{2}C using LIN_FS_DIS bit.

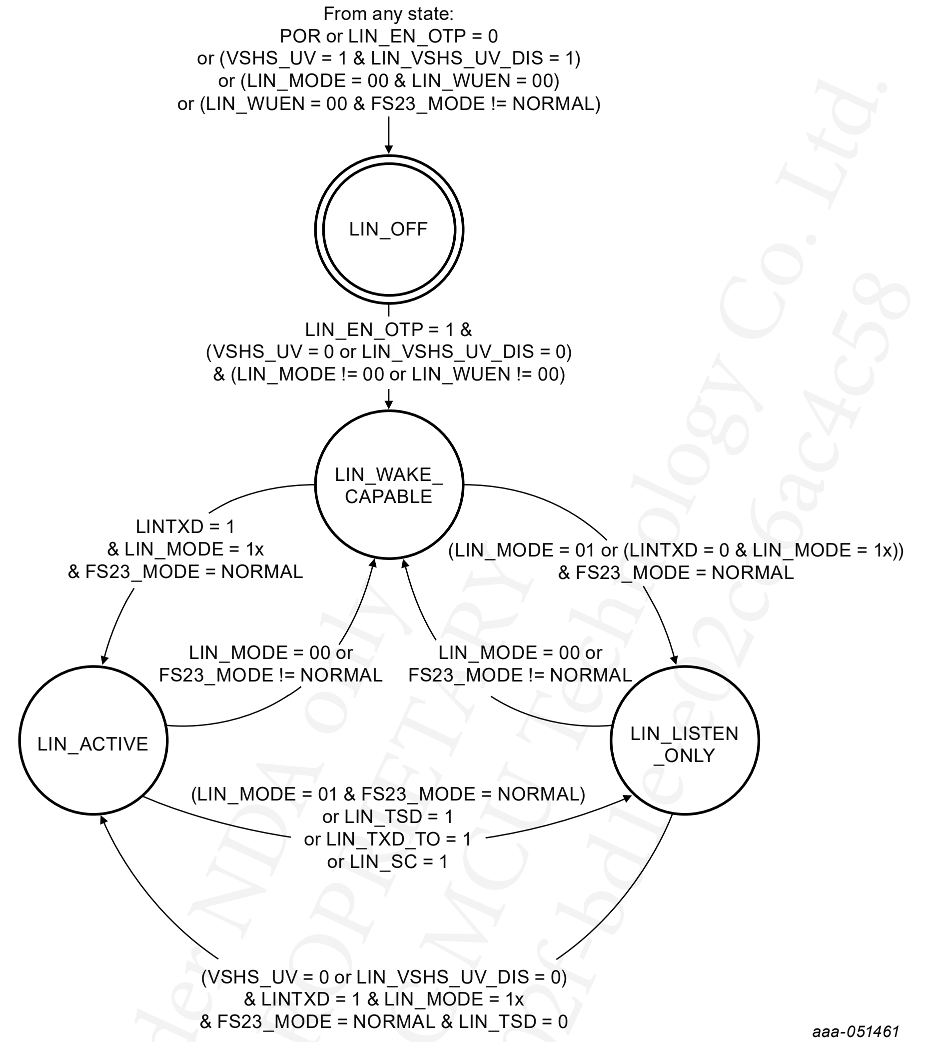


Figure 38. LIN transceiver state machine

18.2.1.1 LIN Off mode

When the LIN mode is set to 2b’00 and the LIN wake-up capability is disabled, or if the device is not in Normal mode (that is, in LPON or LPOFF modes) and the wake-up capability is disabled, the LIN transceiver is in Off mode.

In this mode, the normal and low-power receivers and the transmitter of the LIN transceiver are disabled, the LIN pin is set high ohmic, and the LINRXD pin is driven high.

18.2.1.2 LIN Wake Capable mode

The LIN transceiver is in Wake Capable mode as soon as the LIN mode is different from 2b’00 or as soon as the wake-up capability of the LIN is enabled, regardless of the device state once powered up.

In this mode, the LIN transmitter and the LIN normal receiver are disabled. Only the low-power wake-capable receiver is enabled to allow wake-up pattern detection and device wake-up. The LINRXD pin is driven high (to VDDIO).

18.2.1.3 LIN wake up

A LIN wake-up event is detected when a low level on LIN bus is detected for at least $T_{LIN\_DOM\_WU}$ and is followed by a rising edge.

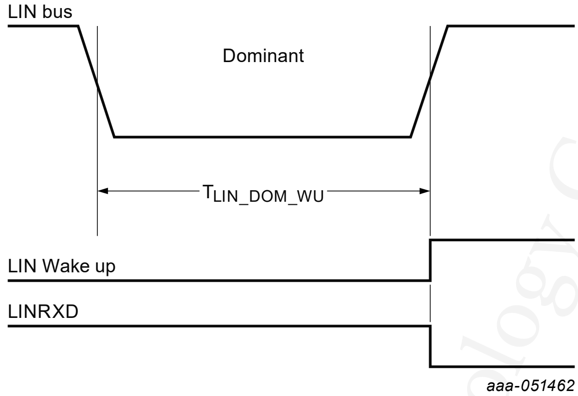


Figure 39. LIN wake-up timing diagram

18.2.1.4 LIN Listen Only mode

The LIN transceiver Listen Only mode is entered from Wake Capable mode when LIN mode is set to 2b’01 or when LIN mode is set to 2b’10 or 2b’11 and LINTXD is low (bus dominant). The device must be in Normal mode.

The low-power wake-up receiver and the transmitter are disabled. Only the normal receiver is enabled. The device is only able to report the bus level to the LINRXD pin. The device is not able to transmit information from LINTXD to the bus.

18.2.1.5 LIN Active mode

The LIN transceiver Active mode is entered from Wake Capable or Listen Only mode when LIN mode is set to 2b’10 or 2b’11 and LINTXD is high. The device must be in Normal mode.

In Active mode, the normal receiver and the transmitter are enabled, and the low-power receiver is disabled. The device can transmit information from LINTXD to the LIN bus and report the bus level to the LINRXD pin.

In this mode, the slope control feature is available by setting LIN_SLOPE to 2b’10, in order to reduce electromagnetic emissions.

When a TSD or a LIN dominant timeout or a short circuit is detected, the transceiver goes back to Listen Only mode and the transmitter is disabled. After a short circuit or a dominant timeout, the transmitter is enabled again by a rising edge on LINTXD pin.

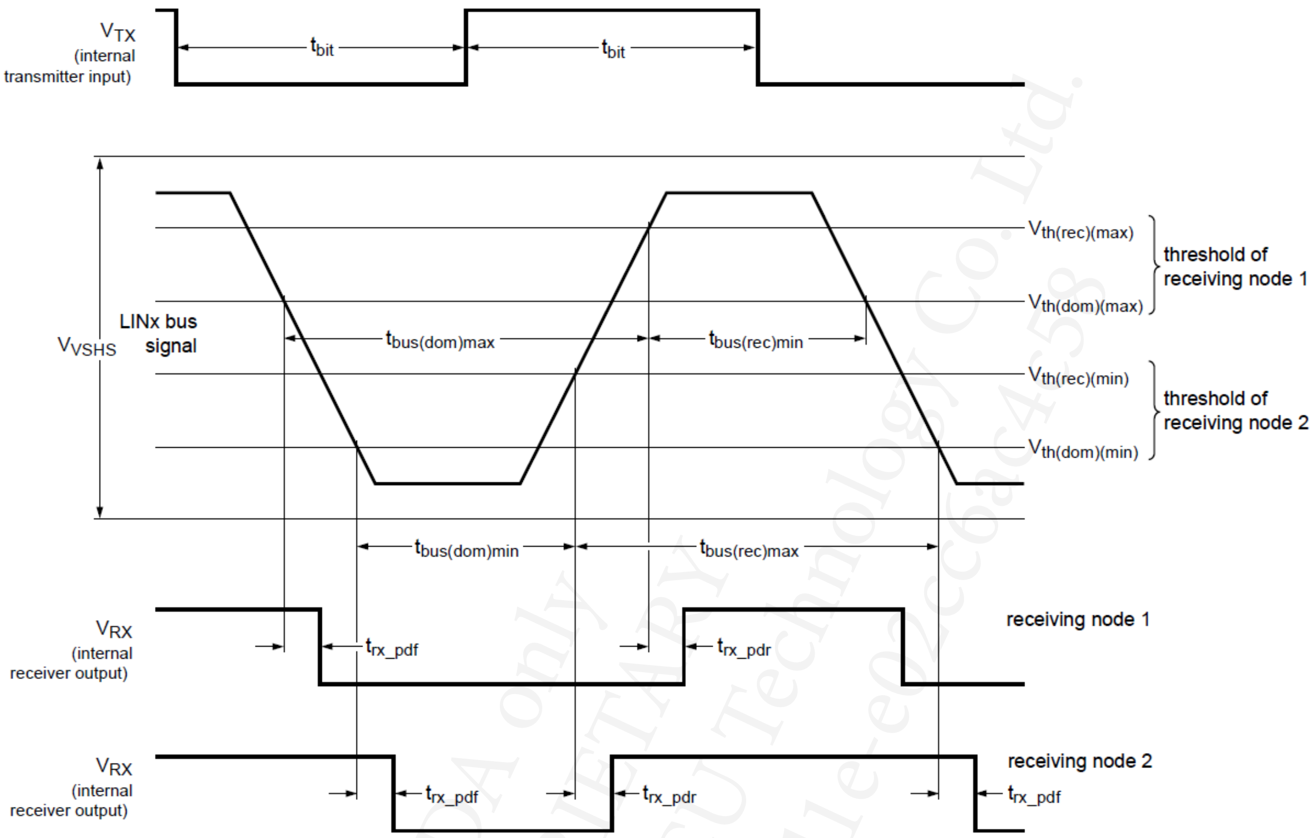


Figure 40. Timing diagram of LIN duty cycle

18.2.2 Electrical characteristics

Table 33. LIN transceiver characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. VSHS = VSHS_UV to 28V, unless otherwise specified. VDDIO = 3V to 5.5V, unless otherwise specified. All voltages referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
LINTXD					
Static characteristics					
V_{LINTXD_IH}	LINTXD input threshold high	-	-	0.7 x VDDIO	V
V_{LINTXD_IL}	LINTXD input threshold low	0.3 x VDDIO	-	-	V
R_{LINTXD_PU}	LINTXD pullup resistance	100	200	400	kΩ
LINRXD					
V_{LINRXD_OH}	LINRXD output high level relative to VDDIO, I_{OUT} = -2 mA	0.8 x VDDIO	-	-	V
V_{LINRXD_OL}	LINRXD output low level relative to VDDIO, I_{OUT} = 2 mA	-	-	0.2 x VDDIO	V

Table 33. LIN transceiver characteristics*...continued*

T_A = −40 °C to 125 °C, unless otherwise specified. VSHS = VSHS_UV to 28V, unless otherwise specified. VDDIO = 3V to 5.5V, unless otherwise specified. All voltages referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
LIN Bus					
V_{LIN_REC}	LIN receiver Recessive state, Active mode	0.6 x V_{SHS}	-	-	V
$V_{LIN\_IN\_DOM}$	LIN receiver Dominant state, Active mode	-	-	0.4 x V_{SHS}	V
$V_{LIN\_ CENTER}$	LIN receiver center voltage (V_{LIN_REC} + $V_{LIN\_IN\_DOM}$)/2, Active mode	0.475 x V_{SHS}	0.5 x V_{SHS}	5.25 x V_{SHS}	V
$V_{LIN\_ HYST}$	LIN receiver hysteresis voltage (V_{LIN_REC} - $V_{LIN\_IN\_DOM}$), Active mode	-	-	0.175 x V_{SHS}	V
$V_{LIN\_ DIODE}$	LIN voltage drop at serial diode in pullup path, with R_{LIN_SLAVE} and I_{DIODE} = 0.9 mA	0.4	0.7	1.0	V
R_{LIN_SLAVE}	LIN responder resistance	20	30	60	kΩ
$I_{LIM\_LIN\_ACT\_DOM}$	LIN current limitation Dominant state, Active mode	40	-	200	mA
$I_{QLIN\_IN\_REC}$	LIN receiver recessive input leakage current	-	-	20	uA
$I_{QLIN\_IN\_DOM}$	LIN receiver dominant input leakage current including pullup resistor	-1	-	-	mA
$I_{LIN\_ACT\_DOM}$	LIN current consumption, LIN Active mode, Dominant state, Tj = 150 °C. Measured via VSHS pin	-	-	2.70	mA
$I_{LIN\_ACT\_REC}$	LIN current consumption, LIN Active mode, Recessive state, Tj = 150 °C. Measured via VSHS pin	-	-	1.35	mA
$I_{LIN\_NO\_GND}$	LIN current consumption, control unit disconnected from ground (GND_{Device} = V_{SHS}), V_{BAT} = 12 V, V_{LIN} = 0 V to 18 V	-1	-	1	uA
$I_{LIN\_NO\_BAT}$	LIN current consumption, V_{BAT} disconnected (V_{SHS} = GND), V_{LIN} = 0 V to 18 V	-	-	100	uA
I_{LIN_WU}	LIN current consumption, wake capability, Tj = 85 °C, VBOS = 5 V. Measured via VSHS pin	-	-	3	uA
C_{LIN}	LIN pin capacitance	-	-	2	pF
Dynamic characteristics					
T_{LIN_EN}	Setup time needed when going to Active mode of the transceiver before sending data.	30	40	50	µs
D_{LIN1}	Duty cycle 1, $TH_{Rec(max)}$ = 0.744 x VSHS, $TH_{Dom(max)}$ = 0.581 x V_{SHS}, V_{SHS} = 7.0 V to 18 V, T_{LIN_BIT} = 50 µs, D1 = $T_{Bus\_rec(min)}$/(2 x T_{LIN_BIT})	39.6	-	-	%
D_{LIN2}	Duty cycle 2, $TH_{Rec(min)}$ = 0.422 x V_{SHS}, $TH_{Dom(min)}$ = 0.284 x V_{SHS}, V_{SHS} = 7.6 V to 18 V, T_{LIN_BIT} = 50 µs, D2 = $T_{Bus\_rec(max)}$/(2 x T_{LIN_BIT})	-	-	58.1	%
D_{LIN3}	Duty cycle 3, $TH_{Rec(max)}$ = 0.778 x V_{SHS}, $TH_{Dom(max)}$ = 0.616 x V_{SHS}, V_{SHS} = 7.0 V to 18 V, T_{LIN_BIT} = 96 µs, D3 = $T_{Bus\_rec(min)}$/(2 x T_{LIN_BIT})	41.7	-	-	%

Table 33. LIN transceiver characteristics*...continued*

T_A = −40 °C to 125 °C, unless otherwise specified. VSHS = VSHS_UV to 28V, unless otherwise specified. VDDIO = 3V to 5.5V, unless otherwise specified. All voltages referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
D_{LIN4}	Duty cycle 4, $TH_{Rec(min)}$ = 0.389 x V_{SHS}, $TH_{Dom(min)}$ = 0.251 x V_{SHS}, V_{SHS} = 7.6 V to 18 V, T_{LIN_BIT} = 96 µs, D4 = $T_{Bus\_rec(max)}$/(2 x T_{LIN_BIT})	-	-	59	%
T_{LIN_BUS2RX}	LIN receiver propagation delay, V_{SHS} = 7 V to 28 V, C_{LINRXD} = 20 pF, R_{LINRXD} = 2.4 kΩ	-	-	6	µs
$T_{LIN\_BUS2RX\_SYM}$	LIN receiver propagation delay symmetry, C_{LINRXD} = 20 pF, R_{LINRXD} = 2.4 kΩ	-2	-	2	µs
$T_{LIN\_DOM\_WU}$	LIN dominant wake-up time	30	80	150	us
$T_{LIN\_DOM\_TO}$	LINTXD dominant timeout time, Active mode	5.0	7.2	8.6	ms
T_{LIN_SC}	LIN short-circuit detection time, Active mode	20	25	30	us

19 Safety

19.1 Functional description

The FS23 includes multiple safety mechanisms to guarantee the functional safety of the system, and reach up to ASIL B level. Safety features are configurable, either by OTP or by SPI/I^{2}C, allowing scalability depending on the application needs. The FS23 also provides an on-demand ABIST to cover latent faults.

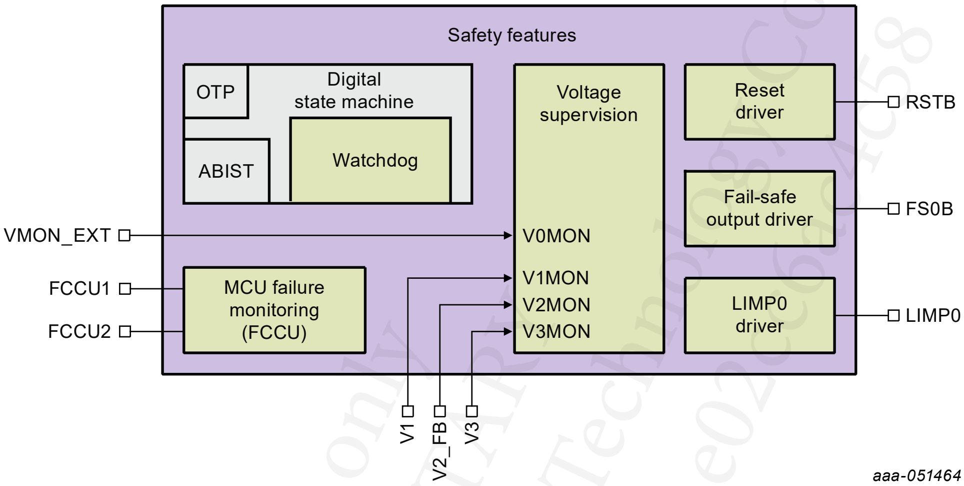


Figure 41. Fail-Safe features block diagram

19.2 Watchdog

The FS23 provides a watchdog monitoring, as a software monitoring of the MCU. The watchdog functionality can be disabled by OTP using WD_INF_OTP bit. When WD_INF_OTP bit is equal to 1, the watchdog period is always considered as infinite. There is no need to refresh the watchdog, except to release the safety pins.

In LPON mode, the watchdog stays enabled or is disabled depending on WD_DIS_LPON bit (configurable during INIT phase). When enabled in LPON, the watchdog operates in Timeout mode.

The watchdog uses two keys, 0x5AB2 (default value after POR) and 0xD564, to validate the answer. The key is stored in the WD_TOKEN register, and is changed alternatively after each good WD refresh.

The MCU reads the WD_TOKEN register and writes the correct answer (WD_TOKEN register value) through the SPI/I^{2}C in WD_ANSWER register, in the right timing. The WD error counter is incremented when the answer is wrong or not given at the right moment, or not given at all at the end of the watchdog period.

The first good watchdog refresh closes the INIT phase if LOCK_INIT = 0. The first good watchdog refresh is sent by the MCU in less than 256 ms (default period duration). Then the watchdog window is running and the MCU must refresh the watchdog every period.

The duration of the watchdog period is configurable from 1 ms to 1024 ms during operation using WDW_PERIOD[3:0] bits. The new watchdog window is effective after the next good watchdog refresh. The watchdog window can be disabled (during INIT phase only) by setting the WDW_PERIOD[3:0] to 4b'0000. The watchdog disable is effective when the INIT phase is closed.

Table 34. Watchdog window period configuration

WDW_PERIOD[3:0]	Watchdog window period
0000	Disable (infinite open window)
0001	1 ms
0010	2 ms
0011	3 ms
0100	4 ms
0101	6 ms
0110	8 ms
0111	12 ms
1000	16 ms
1001	24 ms
1010	32 ms
0011	64 ms
1100	128 ms
1101 (default)	**256 ms**
1110	512 ms
1111	1024 ms

19.2.1 Watchdog selection

Two types of watchdog monitoring, timeout and window watchdog, are implemented and can be selected and changed during operation by SPI/I^{2}C using WDW_EN bit.

Table 35. Watchdog type configuration

WDW_EN	Watchdog type selection
0	**Timeout watchdog (default)**
1	Window watchdog

19.2.1.1 Timeout watchdog

The timeout watchdog is the default configuration at startup. In this mode, the watchdog period is considered as fully open, and the MCU writes the correct value in the WD_ANSWER register before the period ends. If the answer is wrong, or if the answer is not sent before the watchdog timer overflows, the WD error counter is incremented and WD_NOK_I flag is set to 1.

19.2.1.2 Window watchdog

The window watchdog can be enabled by SPI/I^{2}C by setting WDW_EN bit at 1. In this mode, the watchdog period is divided in two. The first half is said to be “closed” and the second is said “open”. The MCU writes the correct value in the WD_ANSWER register during the "open "window. If the answer is wrong, or if the answer is sent during the "closed" window, or if the answer is not sent before the watchdog timer overflows, the WD error counter is incremented and WD_NOK_I flag is set to 1.

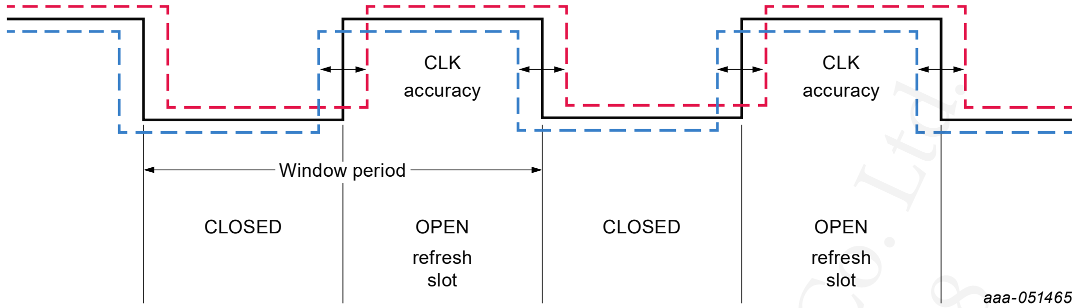


Figure 42. Window watchdog time diagram

Table 36. Watchdog answer and refresh validation

SPI/I²C	Window WD		Timeout WD
	Closed	Open	(Always open)
BAD key	WD_NOK	WD_NOK	WD_NOK
GOOD key	WD_NOK	**WD_OK**	**WD_OK**
None (timeout)	N/A	WD_NOK	WD_NOK

19.2.2 Watchdog error counter

A watchdog error counter is implemented in the device to filter the incorrect watchdog refresh. Each time a watchdog failure occurs, the device increments this counter by 2. The watchdog error counter is decremented by 1 each time the watchdog is properly refreshed. This principle ensures a cyclic 'OK/NOK' behavior converges to a failure detection.

To allow flexibility in the application, the maximum value of this counter is configurable with the WD_ERR_LIMIT[1:0] bits during the INIT phase.

Table 37. Watchdog error counter limit configuration

WD_ERR_LIMIT[1:0]	Watchdog error counter value
00	8
01 (default)	**6**
10	4
11	2
Reset condition	POR

The watchdog error counter value can be read by the MCU for diagnostic with the WD_ERR_CNT[3:0] bits.

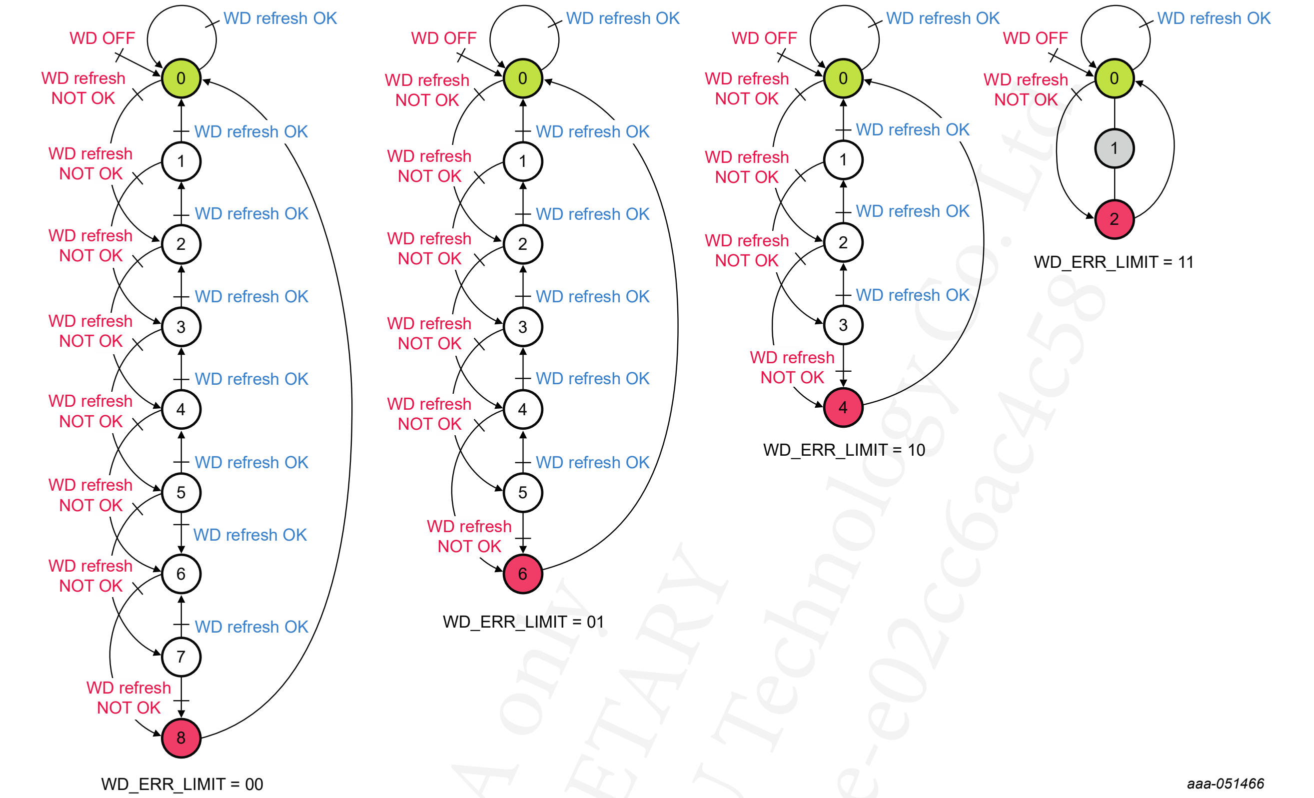


Figure 43. Watchdog error counter configurations

19.2.3 Watchdog refresh counter

The watchdog refresh counter is used to decrement the fault error counter. Each time the watchdog is properly refreshed, the watchdog refresh counter is incremented by ’1’. Each time the watchdog refresh counter reaches its maximum value (‘6’ by default). If the next WD refresh is also good, the fault error counter is decremented by ’1’. Whatever the position the watchdog refresh counter is in, each time there is a wrong refresh watchdog, the watchdog refresh counter is reset to ’0’.

To allow flexibility in the application, the maximum value of this watchdog refresh counter is configurable with the WD_RFR_LIMIT[1:0] bits during the INIT_FS phase.

Table 38. Watchdog refresh counter limit configuration

WD_RFR_LIMIT[1:0]	Watchdog refresh counter value
00 (default)	**6**
01	4
10	2
11	1
Reset condition	POR

The watchdog refresh counter value can be read by the MCU for diagnostic with the WD_RFR_CNT[2:0] bits.

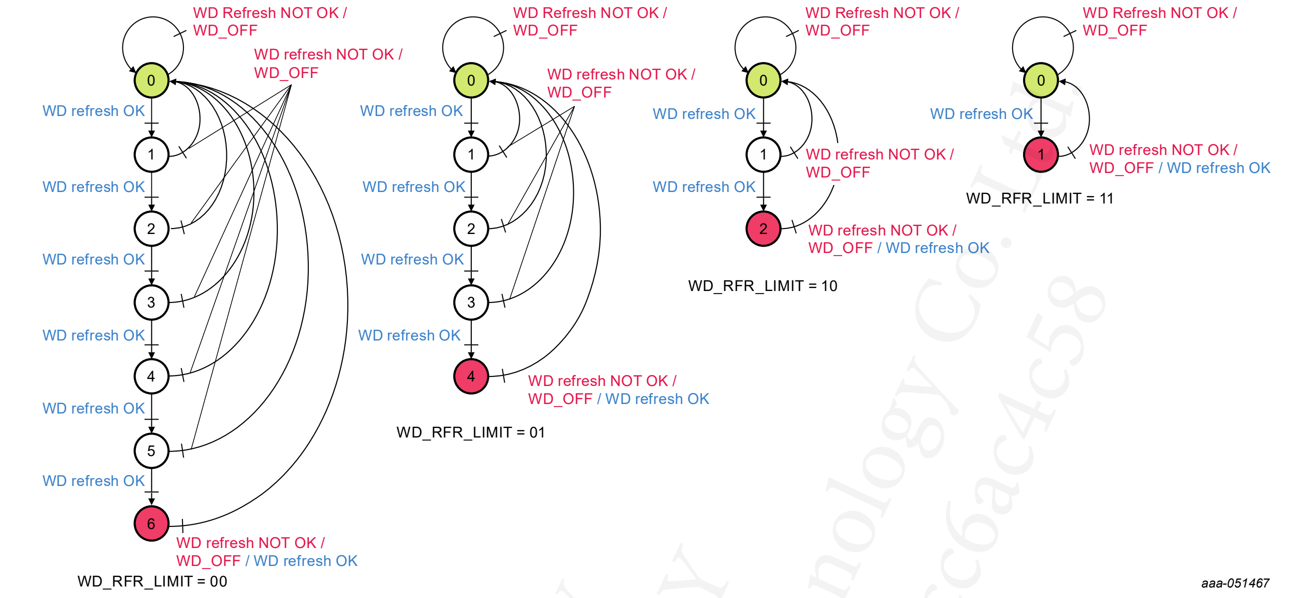


Figure 44. Watchdog refresh counter configurations

19.2.4 Watchdog error impact

When the watchdog error counter reaches its maximum value, in Normal mode or in LPON mode, the fail-safe reaction on RSTB, FS0B, or LIMP0 is configurable with the WD_RSTB/FS0B/LIMP0_IMPACT bits during the INIT phase. If it happens in LPON mode, the device also wakes up.

Table 39. Watchdog error impact configuration

WD_RSTB/FS0B/LIMP0_IMPACT	WD impact on RSTB/FS0B/LIMP0
0	No effect on the pin
1 (default)	**The pin RSTB/FS0B/LIMP0 is asserted**
Reset condition	POR

19.2.5 MCU fault recovery strategy

The fault recovery strategy feature is enabled by SPI/I^{2}C using WDW_REC_EN bit. This function extends the watchdog window to allow the MCU to perform a fault recovery strategy. The goal is to not reset the MCU while it is trying to recover the application after a failure event. When a fault is triggered by the MCU via its FCCU pins, the FS0B and LIMP0 pins are asserted by the device depending on the FCCU error impact configuration. The RSTB pin is not asserted to keep the MCU availability and the watchdog window duration becomes automatically an open window (no more duty cycle). This open window duration is configurable with the WDW_RECOVERY[3:0] bits.

Table 40. Watchdog window in fault recovery configuration

WDW_RECOV[3:0]	Watchdog window duration when the device is in fault recovery strategy
0000	DISABLE (Infinite window, fully open)
0001	1.0 ms
0010	2.0 ms
0011	3.0 ms
0100	4.0 ms
0101	6.0 ms
0110	8.0 ms
0111	12 ms
1000	16 ms
1001	24 ms
1010	32 ms
1011(default)	**64 ms**
1100	128 ms
1101	256 ms
1110	512 ms
1111	1024 ms
Reset condition	POR

The transition from WDW_PERIOD to WDW_RECOVERY happens when the FCCU pin indicates an error and FS0B or LIMP0 is asserted. If the MCU sends a good watchdog refresh before the end of the WDW_RECOVERY duration, the device switches back to the WDW_PERIOD duration and associated duty cycle if the FCCU pins do not indicate an error anymore. Otherwise, a new WDW_RECOVERY period is started. If the MCU does not send a good watchdog refresh before the end of the WDW_RECOVERY duration, then a reset pulse is generated and the device goes to Fail-Safe state.

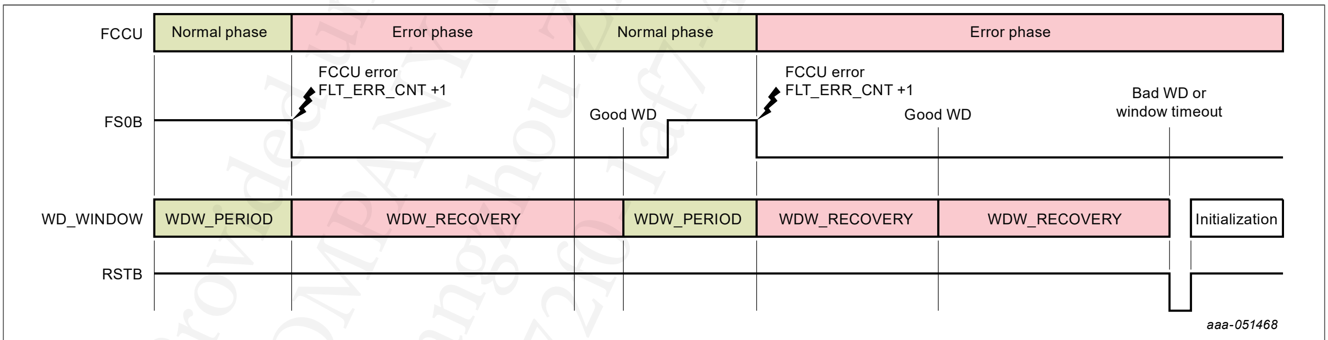


Figure 45. Fault recovery strategy principle

19.2.6 Watchdog electrical characteristics

Table 41. Watchdog electrical characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = 5.5 V to 40 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
Watchdog					
WD_{PER_ACC}	Watchdog period accuracy	-10	-	10	%
WD_{DUTY_CYCLE}	Window watchdog duty cycle	47.5	50	52.5	%

19.3 FCCU monitoring

The FS23 provides an FCCU monitoring feature, which is a hardware monitoring mechanism of the MCU failure. This feature is enabled by OTP using FCCU_EN_OTP bit. The FCCU input pins of the FS23 are in charge of monitoring the error signals of the MCU fault collection and control unit.

The FS23 provides one dedicated FCCU1 pin. Another input among HVIO1, HVIO2, LVIO3, LVIO4, and LVI5 can be configured as FCCU2 pin, via FCCU2_ASSIGN[2:0] bits, in INIT phase.

The FCCU input pins can be configured by pair, or single independent inputs using FCCU_CFG[2:0] bits. The FCCU monitoring is active as soon as the INIT phase is closed. It is deactivated when the device goes to LPON or LPOFF modes.

Table 42. FCCU monitoring configuration

FCCU_CFG[2:0]	FCCU pins configuration
000	No monitoring
001 (default)	**FCCU1 and FCCU2 inputs monitoring activated by pair (bi-stable protocol)**
010	FCCU1 or FCCU2 single input level monitoring activated
011	FCCU1 input level monitoring only, FCCU2 input not used
100	FCCU2 input level monitoring only, FCCU1 input not used
101	FCCU1 or FCCU2 single input PWM monitoring activated
110	FCCU1 input PWM monitoring only, FCCU2 input level monitoring
111	FCCU2 input PWM monitoring only, FCCU1 input level monitoring
Reset condition	POR

19.3.1 FCCU12 monitoring by pair

When FCCU12 are used by pair, the bi-stable protocol is supported according to Figure 46:

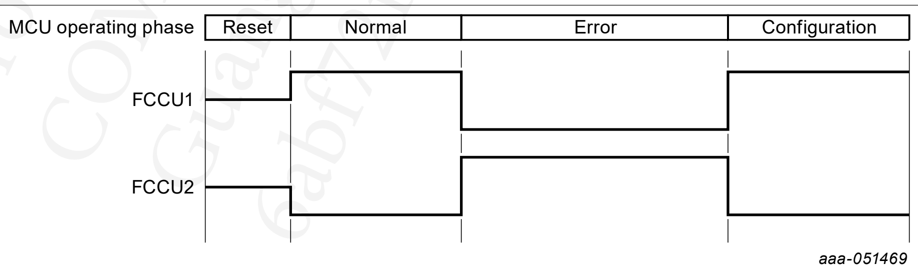


Figure 46. FCCU bi-stable protocol

The polarity of the FCCU fault signals is configurable with FCCU12_FLT_POL bit during the INIT_FS phase.

Table 43. FCCU12 polarity configuration

FCCU12_FLT_POL	FCCU12 polarity
0 (default)	**FCCU1 = 0 or FCCU2 = 1 level is a fault**
1	FCCU1 = 1 or FCCU2 = 0 level is a fault
Reset condition	POR

When FCCU fault is detected in bi-stable protocol, the fail-safe reaction on RSTB, FS0B, or LIMP0 pins is configurable with the FCCU1_RSTB/FS0B/LIMP0_IMPACT bits during the INIT phase.

Table 44. FCCU12 error impact configuration

FCCU1_RSTB/FS0B/LIMP0_IMPACT	FCCU12 impact on RSTB/FS0B/LIMP0
0	No effect on the pin
1 (default)	**The pin RSTB/FS0B/LIMP0 is asserted**
Reset condition	POR

19.3.2 FCCU1, FCCU2 independent monitoring

When FCCU1 and/or FCCU2 are used independently, the FCCU inputs can monitor two different and independent error signals. These error signals can be either steady-state level signals or PWM signals.

When the error signal(s) is/are steady-state level signal(s), the polarity of each FCCU fault signal is configurable with FCCUx_FLT_POL bits during the INIT phase.

Table 45. FCCUx polarity configuration

FCCU1_FLT_POL	FCCU1 polarity
0 (default)	**FCCU1 low level is a fault**
1	FCCU1 high level is a fault
Reset condition	POR
FCCU2_FLT_POL	**FCCU2 polarity**
0 (default)	**FCCU2 low level is a fault**
1	FCCU2 high level is a fault
Reset condition	POR

When the error signal(s) is/are PWM signal(s), the error state is reported when the high-level signal duration is < $FCCU12_{HFDET}$ or when the low-level signal duration is > $FCCU12_{LFDET}$

The fail-safe reaction on RSTB, FS0B, or LIMP0 to an FCCU fault detection is configurable with the FCCUx_RSTB/FS0B/LIMP0_IMPACT bits during the INIT phase.

Table 46. FCCUx error impact configuration

FCCU1_RSTB/FS0B/LIMP0_IMPACT	FCCU1 impact on RSTB/FS0B/LIMP0
0	No effect on the pin
1 (default)	**The pin RSTB/FS0B/LIMP0 is asserted**
Reset condition	POR
FCCU2_RSTB/FS0B/LIMP0_IMPACT	**FCCU2 impact on RSTB/FS0B/LIMP0**

Table 46. FCCUx error impact configuration*...continued*

0	No effect on the pin
1 (default)	**The pin RSTB/FS0B/LIMP0 is asserted**
Reset condition	POR

19.3.3 FCCU12 electrical characteristics

Table 47. FCCU12 electrical characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = 5.5 V to 40 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
FCCU1 static characteristics					
$FCCU1_{VIH}$	FCCU1 high-level input voltage	-	-	0.7 x VDDIO	V
$FCCU1_{VIL}$	FCCU1 low-level input voltage	0.3 x VDDIO	-	-	V
$FCCU1_{HYST}$	FCCU1 input voltage hysteresis	0.1	-	0.6	V
$FCCU1_{RPD}$	FCCU1 internal pulldown resistor	400	800	1300	kΩ
FCCU1,2 dynamic characteristics					
$FCCU12_{TERR}$	FCCU1, 2 filter time when PWM monitoring is activated	0.47	-	0.79	µs
	FCCU1, 2 filter time when level monitoring is activated	4.0	6.0	9.0	µs
$FCCU12_{GF}$	FCCU1, 2 good frequency range (PWM detection)	10.0	22.5	45.0	kHz
$FCCU12_{GTHL}$	FCCU1, 2 good T_{HIGH} and T_{LOW} range (half period)	11.1	25.0	50.0	µs
$FCCU12_{BLF}$	FCCU1, 2 bad-low frequency range (PWM detection)	-	-	5	kHz
$FCCU12_{BHF}$	FCCU1, 2 bad-high frequency range (PWM detection)	90	-	-	kHz
$FCCU12_{HFDET}$	FCCU1, 2 high-level detection time (PWM HF detection)	6.0	8.0	10.0	µs
$FCCU12_{LFDET}$	FCCU1, 2 low-level detection time (PWM LF detection)	51	64	80	µs

19.4 Voltage supervisor

The voltage supervisor is in charge of overvoltage and undervoltage monitoring of all the supply generated by the FS23, Vx (x from 1 to 3), and of VMON_EXT input pin. When an overvoltage occurs on a FS23 regulator, the regulator is switched off until the fault is removed. The overvoltage monitoring is activated before the power-up slots start, and the undervoltage monitoring is activated once the device is in Normal mode. UV/OV flags are then reported accordingly. V0MON monitoring on VMON_EXT pin is enabled by OTP (V0MON_EN_OTP).

19.4.1 V0MON (VMON_EXT) monitoring

The VMON_EXT input pin can be connected to an external regulator. The regulator connected to VMON_EXT must be at least 1 V to be compatible with overvoltage and undervoltage monitoring thresholds. An external resistor bridge must be used to divide the regulator voltage if higher than 1 V, and set the middle point to 1 V. The external resistors accuracy must be at least ±1 %, to ensure a total accuracy of ±2.5 % with the internal thresholds accuracy (±1.5 %).

19.4.2 VxMON monitoring (x from 1 to 3)

V1 and V3 regulators are monitored via the corresponding V1 and V3 pins, which also serve as feedback pins. V2 is monitored via its dedicated V2_FB feedback pin. The expected voltage for each regulators, 3.3 V or 5 V, is configured by OTP (VxMON_OTP), separately from the output voltage and must be configured the same.

Each voltage monitoring channel is connected to a pulldown resistor to detect an undervoltage in case of disconnection.

The VxMON threshold have ±1.5 % UV/OV accuracy (trimmed at 5 V setting, 5.0 % VxMON threshold).

19.4.3 VxMON UV/OV threshold

The OV and UV thresholds are configured independently for each VxMON (x from 0 to 3) by OTP at VxMON_UVTH_OTP[3:0] and VxMON_OVTH_OTP[3:0]. UV thresholds are configurable from 96.5 % to 91.5 % and OV thresholds are configurable from 102.5 % to 110 %. When a regulator is configured at 5 V, five additional UV thresholds are available at 61 %, 62 %, 62.5 %, 63 %, and 64 %.

Table 48. VxMON UV/OV threshold configuration

VxMON_UVTH_OTP[3:0] VxMON_OVTH_OTP[3:0]	VxMON undervoltage threshold configuration	VxMON overvoltage threshold configuration
0000	64 % (for 5 V only)	102.5 %
0001	63 % (for 5 V only)	103.0 %
0010	96.5 %	103.5 %
0011	96.0 %	104.0 %
0100	95.5 %	104.5 %
0101	95.0 %	105.0 %
0110	94.5 %	105.5 %
0111	94.0 %	106.0 %
1000	93.5 %	106.5 %
1001	93.0 %	107.0 %
1010	92.5 %	107.5 %
1011	92.0 %	108.0 %
1100	91.5 %	108.5 %
1101	62.5 % (for 5 V only)	109.0 %
1110	62 % (for 5 V only)	109.5 %
1111	61 % (for 5 V only)	110.0 %

19.4.4 VxMON deglitch time

The OV and UV deglitch times are configured independently by OTP at VxMON_UVDGLT_OTP[1:0] and VxMON_OVDGLT_OTP.

Table 49. VxMON deglitch time

VxMON_UVDGLT_OTP[1:0]	UV detection time	VxMON_OVDGLT_OTP	OV detection time
00	5 µs	0	25 µs
01	15 µs	1	45 µs
10	25 µs		
11	40 µs		

19.4.5 VxMON safety reaction (impact)

When an overvoltage or undervoltage fault is detected, the fail-safe reaction on RSTB, FS0B, or LIMP0 is configurable with VxMON_OV/UV_RSTB/FS0B/LIMP0_IMPACT bits during the INIT phase, for each monitoring input. The reactions of RSTB pin can be pre-selected by OTP.

19.4.6 V1UVLP monitoring

In LPON mode, all the VxMON monitoring are disabled. Only V1 is monitored for undervoltages at V_{1UVLP} = 3.065 V. In case the V1 voltage goes lower than this threshold, the device goes into Fail-Safe state (not configurable), and V1_UVLP_WU bit is set to 1.

V1 is also monitored for V1UVLP when the device powers up after a wake up from LPON, and during a cold start after $T_{SOFT\_START\_V1}$. If, at the end of the softstart, V1 is still under V_{1UVLP} threshold, then the device goes into Fail-Safe state.

19.4.7 Electrical characteristics

Table 50. VxMON electrical characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = 5.5 V to 40 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
VxMON (x from 0 to 3)					
VxMON_OVTH	VxMON overvoltage threshold	-	102.5+0.5*code_ov	-	%
VxMON_UVTH	VxMON undervoltage thresholds at 5 V and 3.3 V output voltage (code_uv = 0010 to 1100)	-	97.5-0.5*code_uv	-	%
	VxMON undervoltage threshold at 5 V output voltage (code_uv = 0000)	-	64	-	%
	VxMON undervoltage threshold at 5 V output voltage (code_uv = 0001)	-	63	-	%
	VxMON undervoltage threshold at 5 V output voltage (code_uv = 1101)	-	62.5	-	%
	VxMON undervoltage threshold at 5 V output voltage (code_uv = 1110)	-	62	-	%
	VxMON undervoltage threshold at 5 V output voltage (code_uv = 1111)	-	61	-	%
$VxMON_{OV\_ACC}$	V0MON OV threshold maximum accuracy	-1.5	-	1.5	%
$VxMON_{UV\_ACC}$	V0MON UV threshold maximum accuracy	-1.5	-	1.5	%
T_{OV_DGLT}	VxMON overvoltage deglitch time	20	25	30	µs

Table 50. VxMON electrical characteristics*...continued*

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = 5.5 V to 40 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
	VxMON_OVDGLT_OTP = 0				
	VxMON overvoltage deglitch time VxMON_OVDGLT_OTP = 1	40	45	60	µs
T_{UV_DGLT}	VxMON undervoltage deglitch time VxMON_UVDGLT_OTP[1:0] = 00	2.5	5.0	13	µs
	VxMON undervoltage deglitch time VxMON_UVDGLT_OTP[1:0] = 01	10	15	23	µs
	VxMON undervoltage deglitch time VxMON_UVDGLT_OTP[1:0] = 10	20	25	23	µs
	VxMON undervoltage deglitch time VxMON_UVDGLT_OTP[1:0] = 11	35	40	53	µs
VxMON (x from 1 to 3)					
$VxMON_{RPD}$	VxMON internal passive pulldown	100	250	400	kΩ
$T_{OV\_DGLT\_START\_UP}$	V1MON OV deglitcher time when V1MON_OVTH_ OTP[3:0] is forced at startup	1.5	2	12	µs
V0MON					
$V0MON_{RPD}$	V0MON internal passive pulldown	1	2	4	MΩ
V1UVLP					
V_{1UVLP}	V1UVLP detection threshold	3.000	3.065	3.130	V
T_{V1UVLP_FILT}	V1UVLP filtering time	0.26	2	7	µs
$T_{V1UVLP\_TO\_FS}$	Time to transition to fail-safe after V1UVLP	-	-	10	µs

19.5 Fault management

19.5.1 Fault error counter

The FS23 integrates a configurable fault error counter, which is counting the number of faults related to the device itself and also caused by external events. The fault error counter starts at 1 after a POR or resuming from LPON or LPOFF. The final value of the fault error counter is used to transition in Fail-Safe state (all safety pins asserted). The maximum value of this counter is configurable with the FLT_ERR_LIMIT[1:0] bits during the INIT phase.

Table 51. Fault error counter configuration

FLT_ERR_LIMIT[1:0]	Fault error counter max value configuration	Fault error counter intermediate value
00	2	1
01 (default)	**6**	**3**
10	8	4
11	12	6
Reset condition	POR	

The fault error counter has two output values: intermediate and final. The intermediate value can be used to force the FS0B or LIMP0 activation or generate a RSTB pulse according to the FLT_MID_RSTB/FS0B/LIMP0_IMPACT bits configuration (INIT phase).

Table 52. Fault error counter fail-safe impact

FLT_MID_RSTB/FS0B/LIMP0_IMPACT	Intermediate value impact on RSTB/FS0B/LIMP0
0	No effect on the pin
1 (default)	**The pin RSTB/FS0B/LIMP0 is asserted**
Reset condition	POR

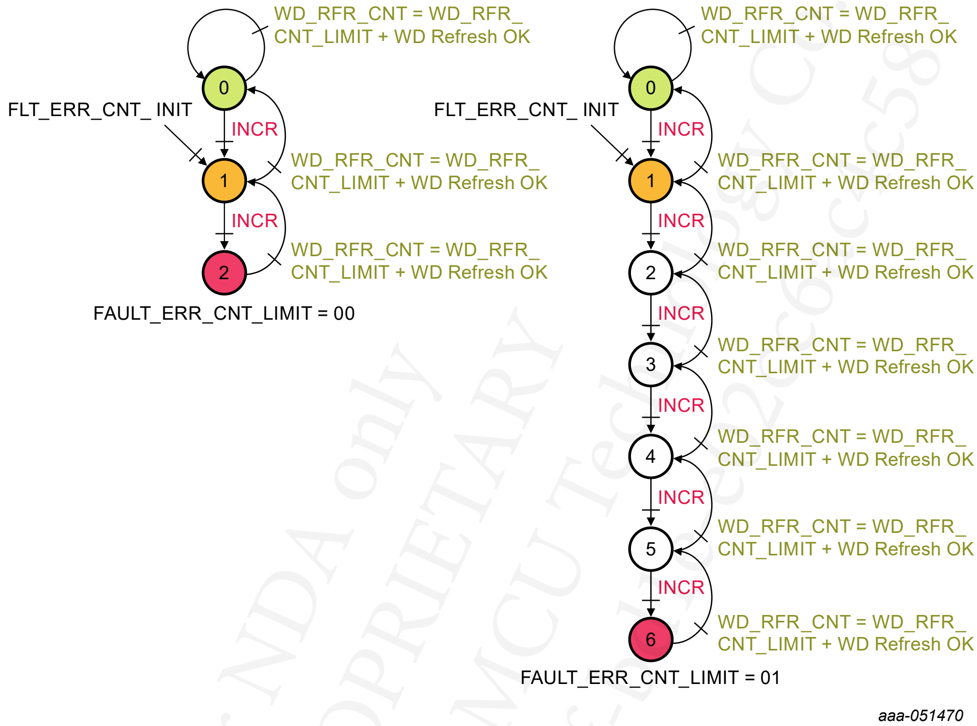


Figure 47. Fault Error Counter diagram with maximum value = 2 or 6

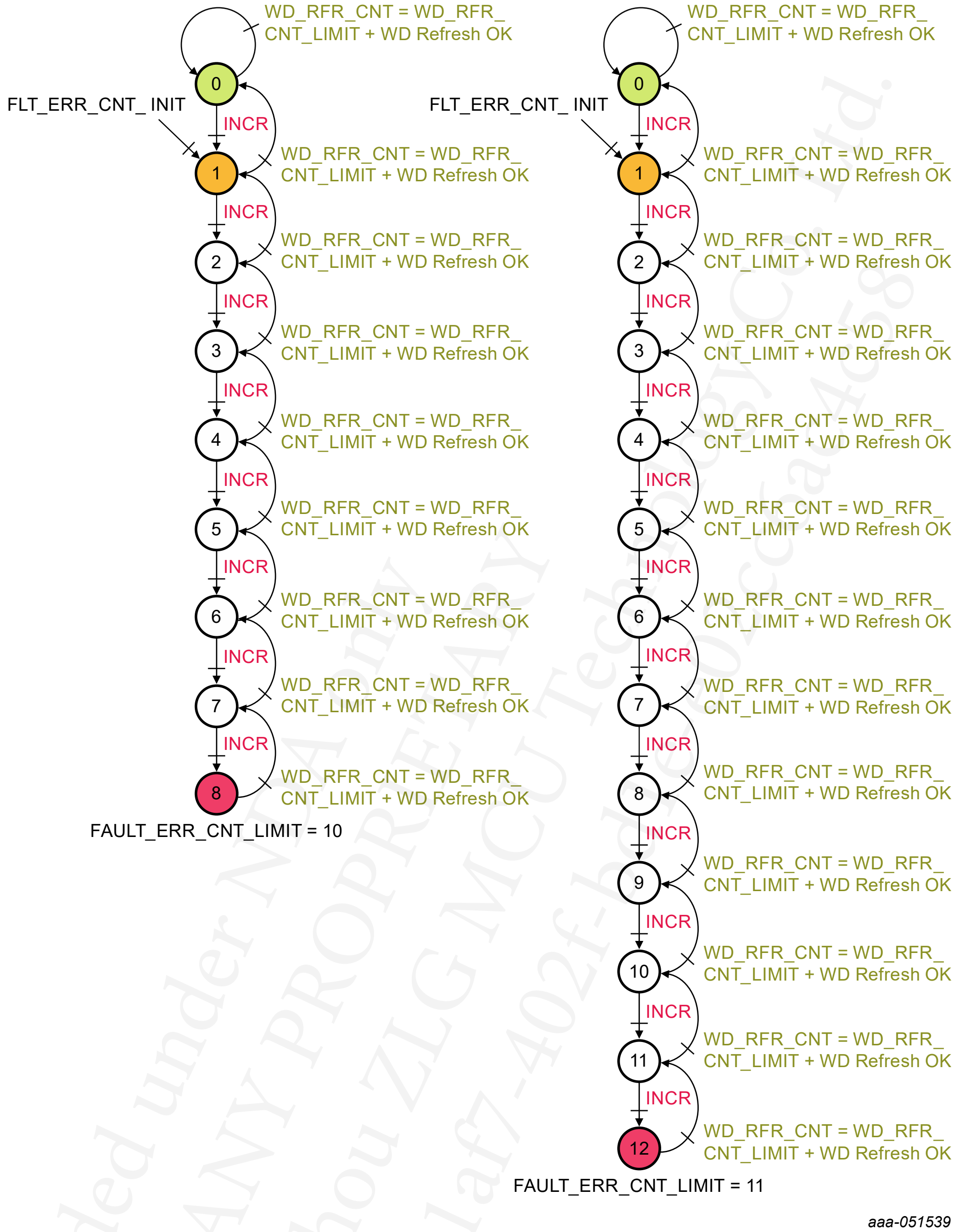


Figure 48. Fault Error Counter diagram with maximum value = 8 or 12

19.5.2 Fault source and reaction

In normal operation when FS0B, LIMP0, and RSTB are released, the fault error counter is incremented when a fault is detected by the FS23 state machine. Table 53 lists all the faults and their impacts on RSTB, FS0B, and LIMP0 pins according to the device configuration. The faults that are configured to not assert RSTB, FS0B, and LIMP0 will not increment the fault error counter. In that case, only the flags are available for MCU diagnostic. The fault error counter is incremented by 1, each time the RSTB and/or FS0B and/or LIMP0 pin is asserted.

Table 53. Application related fail-safe fault list and reaction

In Orange, the reaction is not configurable. In Green, the reaction is configurable by OTP and SPI / I²C for RSTB and by SPI / I²C for FS0B/LIMP0 in INIT mode.

Mode	Fault source	FLT_ERR _CNT	RSTB assertion	FS0B assertion	LIMP0 assertion
Slot 0 to Normal state	VxTSD and CONF_ TSD_Vx_OTP	= Max	Yes	Yes	Yes
	VxMON OV	+1	VxMON_OV_ RSTB_ IMPACT	VxMON_OV_ FS0B_ IMPACT	VxMON_OV_ LIMP0_ IMPACT
	VxMON UV	+1	VxMON_UV_ RSTB_ IMPACT	VxMON_UV_ FS0B_ IMPACT	VxMON_UV_ LIMP0_ IMPACT
	FLT_ERR_CNT = MID VALUE	No change	FLT_MID_ RSTB_ IMPACT	FLT_MID_FS0 B_ IMPACT	FLT_MID_ LIMP0_ IMPACT
	WD_ERR_CNT = WD_ERR_LIMIT	+1	WD_RSTB_IMPACT	WD_FS0B_IMPACT	WD_LIMP0_IMPACT
	FCCU1 single	+1	FCCU1_ RSTB_IMPACT	FCCU1_FS0 B_IMPACT	FCCU1_LIMP0_IMPACT
	FCCU2 single	+1	FCCU2_ RSTB_IMPACT	FCCU2_FS0 B_IMPACT	FCCU2_LIMP0_IMPACT
	FCCU12 pair	+1	FCCU1_ RSTB_IMPACT	FCCU1_FS0 B_IMPACT	FCCU1_LIMP0_IMPACT
	External reset (out of extended RSTB)	+1	No	EXTRSTB_FS0 B_ IMPACT	No
	RSTB short to high	No change	No	Yes	Yes
	RSTB short 8 s	= Max	Yes	Yes	Yes
	FS0B short to high	No change	FS0B_SC_RSTB_ IMPACT	No	No
	LIMP0 short to high	No change	LIMP0_SC_RSTB_ IMPACT	No	No
	INIT_CRC_NOK	+1	No	INIT_CRC_FS0 B_ IMPACT	INIT_CRC_ LIMP0_ IMPACT
	WD_NOK_ RECOVERY	+1	Yes	No	No
	1MHz_STUCK_AT	No change	Yes	Yes	Yes
LPON state	V1UVLP	No change	Yes	Yes by default	Yes
	WD_ERR_CNT = WD_ERR_LIMIT	No change	WD_RSTB_IMPACT	Yes by default	WD_LIMP0_IMPACT
	No fault	= 1	No	Yes by default	No
LPOFF state	No fault	= 1	Yes by default	Yes by default	No
Fail-Safe state	State machine in fail-safe	= 1	Yes by default	Yes by default	Yes by default

19.5.3 Fail-Safe mode

FS23 enters in Fail-Safe (FS) mode when:

- The fault error counter reaches its maximum value (not configurable)
- VBOS UV is detected
- RSTB is asserted low for 8 s (if enabled by OTP)
- VxOV is detected (if configured by OTP)
- VxTSD is detected (if configured by OTP)
- Negative overcurrent (V1_OC_LS) is detected in HVBUCK version (if enabled by OTP)
- OC timeout is detected in HVLDO1 version used with external PNP
- V1UVLP is detected in LPON mode or during transition from LPON mode to Normal mode
- When the first fault is detected (if configured by OTP)

In Fail-Safe mode, all the regulators are turned off, the high-power analog circuitry in enabled, the 20 MHz oscillator is enabled, the OV/UV monitoring is turned on, and the FS_EVT bit is set to 1.

The fault error counter is reset to 1.

The device exits the Fail-Safe state after T_{FS_DUR} time. If FS_LPOFF_OTP bit is set to 1 or if KEY_OFFON_EN_OTP bit is set to 1, the device exits FS state and goes to LPOFF. Otherwise, the device goes back automatically to the power-up sequence.

Table 54. Fail-Safe state electrical characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = 5.5 V to 40 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
Fail-Safe					
T_{FS_DUR}	Fail-Safe state duration • FS_DUR_CFG_OTP = 0 • FS_DUR_CFG_OTP = 1	90 3.6	100 4.0	110 4.4	ms s

19.6 RSTB, FS0B, LIMP0/1/2

Three safety output pins, RSTB, FS0B, and LIMP0, are implemented in order to guarantee the safe state of the system. All those safety outputs are active low.

RSTB and FS0B are activated during power up and can only be released when the device is in Normal mode. LIMP0, on the contrary, will be released at startup and will only be asserted when a fault occurs.

The three pins are managed independently in parallel of the main state machine.

19.6.1 RSTB

RSTB is an open-drain output that can be connected in the application to the reset of the MCU. RSTB requires an external pullup resistor to VDDIO and a filtering capacitor to GND for immunity. An internal pulldown $RSTB_{RPD}$ ensures RSTB low level in LPOFF mode and in Power-Up/Down mode. Redundant supplies of the RSTB driver ensures the pin will be driven low when VSUP is lost. When RSTB is stuck low for more than $RSTB_{T8S}$, the device transitions in Fail-Safe mode. RSTB assertion depends on the device configuration during INIT phase. The configurations can be pre-selected by OTP. RSTB can also be asserted at MCU request by SPI/I^2C, to check the correct hardware connection.

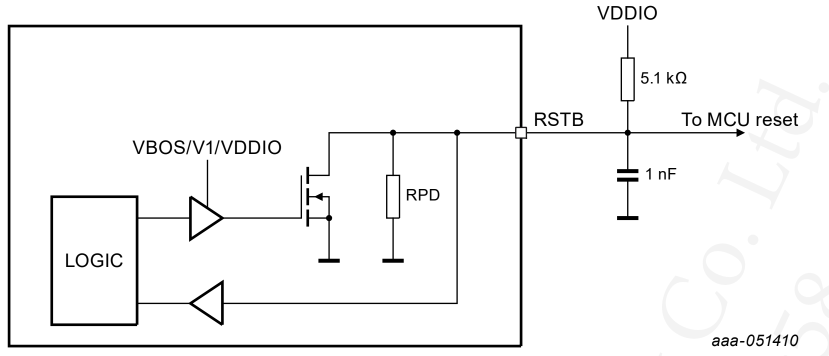


Figure 49. RSTB pin implementation

A 1 ms or 10 ms delay is added before RSTB is released, depending on RSTB_DUR bit (pre-selectable by OTP) to accommodate specific MCU requirement asking for voltage supply stabilization before RSTB is released.

Table 55. RSTB electrical characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = 5.5 V to 40 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
Static electrical characteristics					
$RSTB_{VIL}$	Low-level input voltage	0	-	0.7	V
$RSTB_{VIH}$	High-level input voltage	1.5	-	-	V
$RSTB_{VOL}$	Low-level output voltage (I = 2.0 mA)	-	-	0.4	V
$RSTB_{RPD}$	Internal pulldown resistor	1	2	4	MΩ
$RSTB_{ILIM}$	Current limitation	4.0	-	22.0	mA
Dynamic electrical characteristics					
$RSTB_{TFB}$	Feedback filtering time	8	10	16	us
$RSTB_{TSC}$	Short- to high-detection timer	500	650	800	us
$RSTB_{EXT}$	External reset detection time	20	30	40	μs
$RSTB_{TLG}$	Long pulse (configurable with RSTB_DUR bit)	8.5	-	11.5	ms
$RSTB_{TST}$	Short pulse (configurable with RSTB_DUR bit)	0.85	-	1.15	ms
$RSTB_{T8S}$	8 second timer	7.0	8.0	9.0	s
$RSTB_{TFALL}$	Fall time (pull up to VDDIO = 5 V, 1 nF output capacitor)	-	-	8	us
$RSTB_{TRELEASE}$	Time to release RSTB from POR or LPOFF - With all slots used - With RSTB_DUR = 1 (1 ms)	-	4	6	ms
External components					
$RSTB_{RPU}$	External pullup resistor to VDDIO (nominal)	-	5.1	-	kΩ
$RSTB_{COUT}$	External filtering capacitor	-	1	-	nF

19.6.2 FS0B

FS0B is an open-drain output that can be used to transition the system in safe state. It is asserted low by default, and must be released by the MCU in Normal mode. Once released, it is asserted low in case of fault and depending on the fault impact configuration. In Low-Power modes (LPON and LPOFF), FS0B is asserted low.

FS0B requires an external pullup resistor to VDDIO or VSUP, a 10 nF filtering capacitor to GND for immunity when FS0B is a local pin, and an additional RC network when FS0B is a global pin to be robust against ESD GUN and ISO 7637 transient pulses. An internal pulldown RPD ensures FS0B low level in LPON AND LPOFF and Power-Up/Down mode. Redundant supplies of the FS0B driver ensure the pin will be driven low when VSUP is lost. FS0B assertion depends on the device configuration during INIT phase. FS0B can also be asserted at MCU request by SPI/I^{2}C, to check the correct hardware connection.

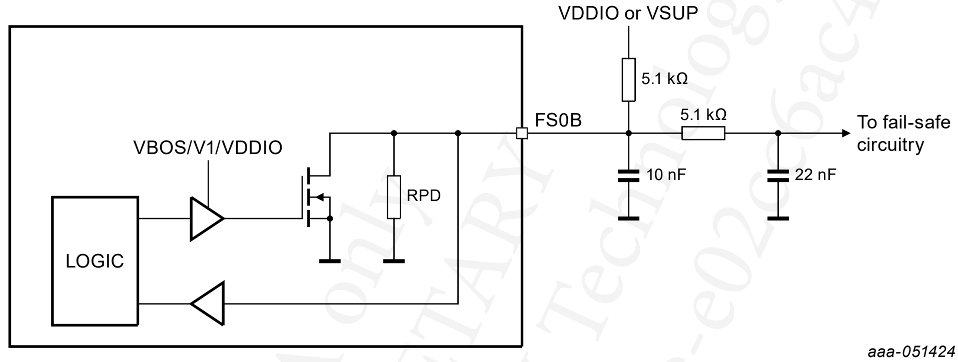


Figure 50. FS0B pin implementation

Table 56. FS0B electrical characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = 5.5 V to 40 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
Static electrical characteristics					
$FS0B_{VIL}$	Low-level input voltage	0	-	0.7	V
$FS0B_{VIH}$	High-level input voltage	1.5	-	-	V
$FS0B_{VOL}$	Low-level output voltage (I = 2.0mA)	-	-	0.5	V
$FS0B_{RPD}$	Internal pulldown resistor	1	2	4	MΩ
$FS0B_{ILIM}$	Current limitation	4.0	-	22.0	mA
Dynamic electrical characteristics					
$FS0B_{TFB}$	Feedback filtering time	8	10	16	µs
$FS0B_{TSC}$	Short- to high-detection timer	500	650	800	µs
$FS0B_{TFALL}$	Fall time (pull up to VDDIO = 5 V, 10 nF output capacitor)	-	-	10	µs
External components					
$FS0B_{RPU}$	External pullup resistor to VDDIO (nominal)	-	5.1	-	kΩ
$FS0B_{RSER}$	External serial resistor (optional, 0805 package size)	-	5.1	-	kΩ
$FS0B_{COUT1}$	External output capacitor (close to the pin)	-	10	-	nF
$FS0B_{COUT2}$	External output capacitor (optional, after the serial resistor)	-	22	-	nF

19.6.3 FS0B release

When the fail-safe output FS0B is asserted low by the device because of a fault, or after a power up, some conditions must be validated before allowing the FS0B pin to be released by the device. These conditions are:

- No fault affecting FS0B reported
- Fault error counter = 0
- Device in Normal mode
- Device not in Debug mode and not in INIT mode
- FS_FS0B_LIMP0_REL register filled with the correct value, depending on current WD_TOKEN[15:0] value as Table 57:

Table 57. FS0B and/or LIMP0 release commands

FS_FS0B_ LIMP0_REL[15:0]	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Release FS0B	**0**	**1**	**1**	NOT(WD_TOKEN[**0:12**])												
Release LIMP0	**1**	**1**	**0**	NOT(WD_TOKEN[**3:15**])												
Release both FS0B and LIMP0	**1**	**0**	**1**	NOT(WD_TOKEN[**0:6**])							NOT(WD_TOKEN[**10:15**])					

19.6.4 LIMP0

LIMP0 is an open-drain output that can be used to transition the system in safe state. It is released high by default. It is asserted low in case of fault and depending on the fault impact configuration. In Low-Power modes (LPON and LPOFF), LIMP0 works like in Normal mode.

LIMP0 requires an external pullup resistor to VSUP or VDDIO, a 10 nF filtering capacitor to GND for immunity when LIMP0 is a local pin, and an additional RC network, when LIMP0 is a global pin, to be robust against ESD GUN and ISO 7637 transient pulses. A weak internal pulldown RPD ensures LIMP0 low level in case of pin lift. An internal pulldown RPD_STUP ensures LIMP0 is released at startup.

LIMP0 assertion depends on the device configuration during INIT phase. LIMP0 can also be asserted at MCU request by SPI/I^{2}C, to check the correct HW connection.

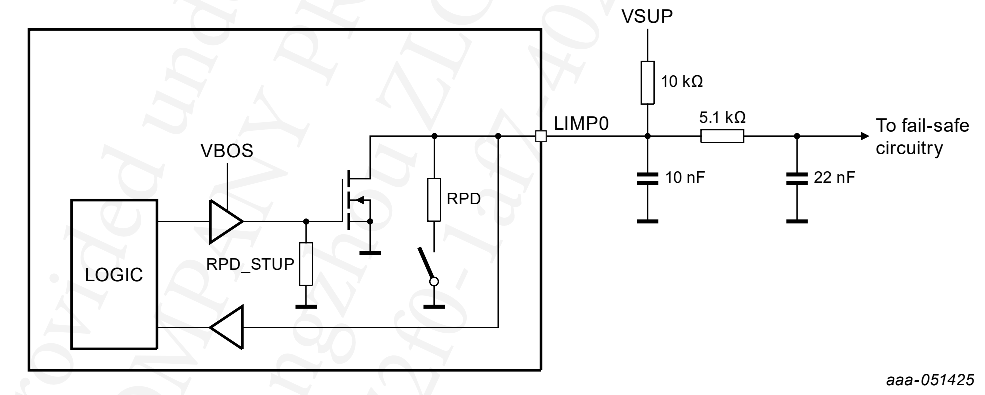


Figure 51. LIMP0 pin implementation

Table 58. LIMP0 electrical characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = 5.5 V to 40 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
Static electrical characteristics					

Table 58. LIMP0 electrical characteristics*...continued*

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = 5.5 V to 40 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
$LIMP0_{VIL}$	Low-level input voltage	0	-	0.7	V
$LIMP0_{VIH}$	High-level input voltage	1.5	-	-	V
$LIMP0_{VOL}$	Low-level output voltage (I = 2.0mA)	-	-	0.5	V
$LIMP0_{RPD}$	Internal pulldown resistor	1	2	4	MΩ
$LIMP0_{ILIM}$	Current limitation	4.0	-	22.0	mA
Dynamic electrical characteristics					
$LIMP0_{TFB}$	Feedback filtering time	8	10	16	µs
$LIMP0_{TSC}$	Short- to high-detection timer	500	650	800	µs
$LIMP0_{TFALL}$	Fall time (pull up to VSUP = 14 V, 10 nF output capacitor)	-	-	35	µs
	Fall time (pull up to VSUP = 14 V, no output capacitor)	-	-	10	µs
External components					
$LIMP0_{RPU}$	External pullup resistor to VDDIO (nominal)	-	5.1	-	kΩ
	External pullup resistor to VSUP (nominal)	-	10	-	kΩ
$LIMP0_{RSER}$	External serial resistor (optional, 0805 package size)	-	5.1	-	kΩ
$LIMP0_{COUT1}$	External output capacitor (close to the pin)	-	10	-	nF
$LIMP0_{COUT2}$	External output capacitor (optional, after the serial resistor)	-	22	-	nF

19.6.5 LIMP0 release

When the fail-safe outputs LIMP0 is asserted low by the device because of a fault, some conditions must be validated before allowing LIMP0 pin to be released by the device. These conditions are:

- No fault affecting LIMP0 reported
- Fault error counter = 0
- Device in Normal mode
- Device not in INIT mode
- FS_FS0B_LIMP0_REL register filled with the correct value, depending on current WD_TOKEN[15:0] value as per Table 57.

19.6.6 LIMP1, LIMP2

Two additional pseudo-safety output can be used when configuring general purpose I/Os as LIMP1 or LIMP2 functions. HVIO1 or LVIO3 can be configured as LIMP1 function and HVIO2 or LVIO4 can be configured as LIMP2 function.

When used, LIMP1 and LIMP2 are following LIMP0 assertion, except when requested from the MCU. LIMP1 and LIMP2 paths can also be checked by the MCU by requesting their assertion by SPI/I^2C.

When asserted, LIMP1 and/or LIMP2 will be released when LIMP0 is released. If LIMP0 is already released (that is, LIMP1 or LIMP2 was asserted after MCU request), a LIMP0 release request must be sent by the SPI to release them.

LIMP1 and LIMP2 can work as asserted to a static level (high or low), or as PWM (configurable polarity) when asserted, depending on LIMPx_CFG[1:0] bit.

When configured as PWM, LIMP1 is static when no fault is reported and toggles at 1.25 Hz with a 50 % duty cycle when asserted.

When configured as PWM, LIMP2 is static when no fault is reported and toggles at 100 Hz when asserted. Its duty cycle is configurable between 2.5 %/5 %/10 %/20 % using LIMP2_DC_CFG[1:0] bit.

Table 59. LIMP1, LIMP2 electrical characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = 5.5 V to 40 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
Dynamic electrical characteristics					
$LIMP1_{PWM\_FREQ}$	LIMP1 PWM frequency	1.13	1.25	1.38	Hz
$LIMP1_{PWM\_DLY}$	LIMP1 PWM assertion delay	-	-	500	µs
$LIMP2_{PWM\_FREQ}$	LIMP2 PWM frequency	80	100	120	Hz
$LIMP2_{PWM\_DLY}$	LIMP2 PWM assertion delay	-	-	500	µs

19.7 Analog built-in self-test (ABIST)

The FS23 provides an analog built-in self-test (ABIST) to verify the correct functionality of the voltage monitoring functions. The ABIST is executed on demand, after a SPI/I^{2}C request from the MCU. ABIST can only be launched from Normal mode. A status bit ABIST_READY is provided to notify that ABIST is available and ready to be launched.

ABIST can be launched for all the voltage-monitoring channels at the same time (via LAUNCH_ABIST bit), or individually (via ABIST_VxMON or ABIST_V1UVLP individual bits). An individual diagnostic bit is available for each channel once the ABIST is done (ABIST_DONE = 1). The diagnostics flags have no impact on the safety pins.

The diagnostic flags must be cleared before launching the next ABIST, using the CLEAR_ABIST bit.

If one of the concerned monitored voltages is out of range (OV or UV), the ABIST on-demand command is ignored. While the ABIST is running, the other monitoring functions are kept available.

Table 60. ABIST electrical characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = 5.5 V to 40 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
ABIST					
T_{ABIST}	ABIST duration for one monitoring channel	-	-	70	us

19.8 Periodic CRC check

The FS23 provides an 8-bit periodic CRC check to verify the integrity of the INIT registers (FS_I_xxxx) containing the safety configuration information (configurable in INIT mode only). This mechanism allows the detection of a misconfiguration from the MCU or a bit flip in the INIT registers.

The 8-bit CRC is computed on the result of the concatenation of the following 58 register bits:

- FS_I_OVUV_CFG1[12:7], FS_I_OVUV_CFG1[5:0]
- FS_I_OVUV_CFG2[12:7], FS_I_OVUV_CFG2[5:0]
- FS_I_FCCU_CFG[14:0]
- FS_I_FSSM_CFG[14:4]

- FS_I_WD_CFG[14:7]

The calculation to apply on the result of the concatenation is the same as the SPI/I^2C CRC, using x^8+x^4+x^3+x^2+1 polynomial. The MCU must write the obtained CRC in the FS_CRC register before closing the INIT phase, after the modification of the INIT registers.

Once the INIT phase closes and the device is in Normal mode, the periodic CRC check is launched automatically each 5 ms (T_{CRC}) (<FTTI).

Each 5 ms, the device logic recalculates the CRC and compares it to the value stored in FS_CRC register. If a mismatch is reported, the INIT_CRC_NOK_I bit is set and the safety outputs FS0B or LIMP0 are asserted depending on their impact configuration (INIT_CRC_FS0B_IMPACT and INIT_CRC_LIMP0_IMPACT).

Table 61. Cyclic CRC check characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = 5.5 V to 40 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
Cyclic CRC check					
T_{CRC}	CRC check timing interval	-	-	5.5	ms
T_{CRC_RUN}	CRC maximum computation time	-	-	80	µs

19.9 Clock monitoring

The 1 MHz is monitored for stuck-at faults in Normal mode. In case a stuck-at is detected, the three safety pins — RSTB, FS0B, and LIMP0 — are asserted.

20 MCU communication

The FS23 provides both I²C and SPI interfaces with shared pins, for device configuration, control and diagnostic, in Normal and LPON modes. The choice of the interface is done by OTP.

By default and when SPI_EN_OTP = 0, the I²C interface is selected. In this case, pins 27 and 28 are used respectively as SCL and SDA signals, and pins 25 and 26 are available as LVO6 and LVI5 digital I/Os.

When SPI_EN_OTP = 1, the SPI interface is selected. In this case, pins 25 to 28 are used respectively as MISO, MOSI, SCK, and CSB pins.

20.1 I²C communication interface

20.1.1 I²C interface overview

The FS23 I²C interface follows the Fast mode-plus definition up to 1 Mbit/s. High-speed mode (3.4 Mbit/s) is not supported by the device. I²C interface protocol requires a device address for addressing the target IC on a multidevice bus. The FS23 has one device address to access the logic. This I²C addresses is set by OTP (I2CDEVADDR_OTP).

The I²C interface uses the VDDIO pin as power input and it is compatible with 3.3 V and 5.0 V input supply. Timing, diagrams, and further details can be found in the NXP I²C specification. Refer to UM10204 Rev. 7.

An I²C message has the following arrangement:

Table 62. I²C message construction

								B39	**B38**	**B37**	**B36**	**B35**	**B34**	**B33**	**B32**
								ID[6:0]							**R/W**
								Device address							R/W
B31	**B30**	**B29**	**B28**	**B27**	**B26**	**B25**	**B24**	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
0	**ADR[6:0]**							**DATA[15:8]**							
0	Register address							Data MSB							
B15	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
DATA[7:0]								**CRC[7:0]**							
Data LSB								CRC							

Bit B32 must be set to 0 to execute a write command, and to 1 to execute a read command.

A read command is composed of two I²C accesses:

- The first access is the request with the device address and the register address.
- The second access is the answer with the data contained in the register and the CRC.

Table 63. Read command example

First access			Second access		
Device address + R/W	**0b0 + Register address**		**Device address + R/W**	**Data**	**8-bit CRC**
0 1 0 0 0 0 0 0	0 0 0 0 0 1 1 0		0 1 0 0 0 0 0 1	0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 1	**0x5F**
0x40	0x06		0x41	0x0009	

An 8-bit CRC is required for each write and read I²C command. Computation of a CRC is derived from the mathematics of polynomial division, modulo two. The CRC polynomial used is x^8+x^4+x^3+x^2+1 defined by SAE-J1850 (identified by 0x1D) with a SEED value of hexadecimal '0xFF'.

20.1.2 Device address

The I²C address has the following arrangement:

- Bit 39: 0
- Bit 38: 1
- Bit 37 to 34: OTP value
- Bit 33: 0

Table 64. Device address

B39	B38	B37	B36	B35	B34	B33
0	**1**	**I2CDEVADDR_OTP[3:0]**				**0**

20.1.3 I²C CRC calculation and results

CRC calculation using XOR:

CRC_7 = XOR (B38, B35, B32, B31, B24, B23, B22, B20, B17, B13, B12, B11, 1, 1, 1)

CRC_6 = XOR (B37, B34, B23, B22, B21, B19, B16, B12, B11, B10, 1, 1)

CRC_5 = XOR (B39, B36, B33, B30, B29, B22, B21, B20, B18, B15, B11, B10, B9, 1, 1, 1)

CRC_4 = XOR (B39, B38, B35, B32, B29, B28, B21, B20, B19, B17, B14, B10, B9, B8, 1, 1, 1, 1)

CRC_3 = XOR (B37, B35, B34, B32, B28, B27, B24, B23, B22, B19, B18, B17, B16, B12, B11, B9, B8, 1, 1, 1, 1)

CRC_2 = XOR (B39, B38, B36, B35, B34, B33, B32, B27, B26, B24, B21, B20, B18, B16, B15, B13, B12, B10, B8, 1, 1, 1, 1, 1, 1, 1)

CRC_1 = XOR (B37, B34, B33, B26, B25, B24, B22, B19, B15, B14, B13, B9, 1, 1, 1)

CRC_0 = XOR (B39, B36, B33, B32, B25, B24, B23, B21, B18, B14, B13, B12, B8, 1, 1, 1, 1)

Table 65. CRC result examples

Device address + R/W								0b0 + Register address								Data																8-bit CRC
0	1	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0xAC**
0x41								0x02								0x0000																**0xAC**
0	1	0	0	0	1	0	0	0	1	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	1	**0x38**
0x44								0x7F								0xD001																**0x38**

20.1.4 Electrical characteristics

Table 66. Electrical characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = 5.5 V to 40 V, unless otherwise specified. VDDIO = 3.0 V to 5.5 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
I2C					
VDDIO	I^2C interface supply input	3.135	3.300	3.465	V
		4.75	5.00	5.25	
F_{SCL}	SCL clock frequency (max load cap = 100 pF)	-	-	1	MHz
$I2C_{VIL}$	SCL, SDA low-level input voltage	0.3 x VDDIO	-	-	V
$I2C_{VIH}$	SCL, SDA high-level input voltage	-	-	0.7 x VDDIO	V
$I2C_{HYST}$	Input hysteresis	170	-	-	mV
SDA_{VOL}	Low-level output voltage at SDA pin (I = 20 mA)	-	-	0.4	V
C_{I2C}	Input capacitance at SCL/SDA	-	-	10	pF
t_{SPSCL}	SCL pulse width filtering time	18	-	-	ns
t_{SPSDA}	SDA pulse width filtering time	28	-	-	ns

20.2 SPI communication

The FS23 provides a 32-bit SPI interface, as alternative to the I^2C interface (SPI_EN_OTP = 1).

20.2.1 SPI interface overview

The SPI has the following arrangement:

MOSI bits

- Bits 31 to 25: register address
- Bit 24: Read/Write (for reading Bit 24 = 0; For writing Bit 24 = 1)
- Bits 23 to 8: control bits
- Bits 7 to 0: CRC

MISO bits

- Bits 31 to 24: general device status
- Bits 23 to 8: device internal control register content
- Bits 7 to 0: CRC

The digital SPI pins (CSB, SCLK, MOSI, MISO) are referenced to VDDIO.

The MCU is the master driving MOSI and FS23 is the slave driving MISO. The MISO data is latched at the SCLK rising edge and MOSI data is latched at the SCLK falling edge. MSB first.

- In write command, MISO [31:24] bits are the general status flags, [23:8] bits are register’s content before Write access and MISO [7:0] is the CRC of the message sent by the FS23.
- In read command, MOSI [23:8] bits are all 0 and MOSI [7:0] is the CRC of the message sent by the MCU.

Table 67 and Table 68 describe SPI communication protocol for writing data into the FS23 or reading data from the FS23.

Table 67. SPI write command message construction

	B31	B30	B29	B28	B27	B26	B25	B24	B23	B22	B21	B20	B19	B18	B17	B16
MOSI	**Register address [6:0]**							**R/W**	**Write data [15:8]**							
MISO	**General status flags**								**Register content before write**							
	B15	**B14**	**B13**	**B12**	**B11**	**B10**	**B09**	**B08**	**B07**	**B06**	**B05**	**B04**	**B03**	**B02**	**B01**	**B00**
MOSI	**Write data [7:0]**								**CRC [7:0]**							
MISO	**Register content before write**								**CRC [7:0] - response**							

Table 68. SPI read command message construction

	B31	B30	B29	B28	B27	B26	B25	B24	B23	B22	B21	B20	B19	B18	B17	B16
MOSI	**Register address [6:0]**							**R/W**	**0x00**							
MISO	**General status flags**								**Read data [15:8]**							
	B15	**B14**	**B13**	**B12**	**B11**	**B10**	**B09**	**B08**	**B07**	**B06**	**B05**	**B04**	**B03**	**B02**	**B01**	**B00**
MOSI	**0x00**								**CRC [7:0]**							
MISO	**Read data [7:0]**								**CRC [7:0] - response**							

20.2.2 SPI status bits

Table 69. MISO general device status bits descriptions

Bit	Symbol	Description
31	HSxG	**Interrupt notification from M_HSx_FLG or M_CS_FLG_MSK registers**
		0 No event reported in M_HSx_FLG or M_CS_FLG_MSK registers
		1 An interrupt or flag is present in M_HSx_FLG or M_CS_FLG_MSK registers
		Reset on power-on reset (POR), cleared when all individual bits are cleared
		Flags reported: HS1_OL_I, HS1_OC_I, HS12_TSD_I, HS2_OL_I, HS2_OC_I, HS3_OL_I, HS3_OC_I, HS34_TSD_I, HS4_OL_I, HS4_OC_I, WAKE1_OL_I, WAKE2_OL_I, HVIO1_OL_I, HVIO2_OL_I
30	SAFETYG	**Interrupt notification from FS_SAFETY_FLG register (safety related errors)**
		0 No event reported in FS_SAFETY_FLG register
		1 Safety-related interrupt or flag present in FS_SAFETY_FLG register
		Reset on power-on reset (POR), cleared when all individual bits are cleared
		Flags reported: WD_NOK_I, FCCU12_I, FCCU1_I, FCCU2_I, INIT_CRC_NOK_I
29	PHYG	**Interrupt notification from M_CAN or M_LIN registers**
		0 No event present reported in M_CAN or M_LIN registers
		1 An interrupt or flag is present in M_CAN or M_LIN registers
		Reset on power-on reset (POR), cleared when all individual bits are cleared
		Flags reported: CAN_TSD_I, CAN_TXD_TO_I, LIN_TSD_I, LIN_TXD_TO_I, LIN_SC_I
28	WUG	**Interrupt notification from M_IOWU_FLG or M_WU1_FLG registers**
		0 No event reported in M_IOWU_FLG or M_WU1_FLG registers
		1 An interrupt or flag is present in M_IOWU_FLG or M_WU1_FLG registers

Table 69. MISO general device status bits descriptions*...continued*

Bit	Symbol	Description
		Reset on power-on reset (POR), cleared when all individual bits are cleared
		Flags reported: WK1_WU_I, WK2_WU_I, HVIO1_WU_I, HVIO2_WU_I, LVIO3_WU_I, LVIO4_WU_I, LVI5_WU_I, CAN_WU_I, LIN_WU_I, LDT_WU_I, INT_TO_WU, WD_OFL_WU, V1_UVLP_WU, GO2NORMAL_WU, EXT_RSTB_WU
27	IOTIMG	**Interrupt notification from M_IO_TIMER_G register**
		0 No event reported in M_IO_TIMER_G register
		1 An interrupt or flag is present in M_IO_TIMER_G register
		Reset on power-on reset (POR), cleared when all individual bits are cleared
		Flags reported: WK1_I, WK2_I, HVIO1_I, HVIO2_I, LVIO3_I, LVIO4_I, LVI5_I, LDT_I
26	COMG	**Interrupt notification from M_VSUP_COM_FLG register**
		0 No event reported into M_VSUP_COM_FLG register
		1 An interrupt or flag is present in the M_VSUP_COM_FLG register
		Reset on power-on reset (POR), cleared when all individual bits are cleared
		Flags reported: SPI_REQ_I, SPI_CLK_I, SPI_CRC_I, I2C_REQ_I, I2C_CRC_I
25	VSUPG	**Interrupt notification from M_VSUP_COM_FLG register**
		0 No event reported into M_VSUP_COM_FLG register
		1 An interrupt or flag is present in the M_VSUP_COM_FLG register
		Reset on power-on reset (POR), cleared when all individual bits are cleared
		Flags reported: VSUP_UV_I, VSUP_OV_I, VSHS_UV_I, VSHS_OV_I
24	VxG	**Interrupt notification from M_REG_FLG register**
		0 No event reported into M_REG_FLG and M_REG1_FLG registers
		1 An interrupt or flag is present in M_REG_FLG or M_REG1_FLG register
		Reset on power-on reset (POR), cleared when all individual bits are cleared
		Flags reported: V0UV_I, V0OV_I, V1OC_I, V1UV_I, V1OV_I, V1TSD_I, V1TWARN_I, V1_OCLS_I, V2OC_I, V2UV_I, V2OV_I, V2TSD_I, V3OC_I, V3UV_I, V3OV_I, V3TSD_I

20.2.3 Cyclic redundant check

An 8-bit CRC is required for each write and read SPI command. Computation of a CRC is derived from the mathematics of polynomial division, modulo two. The CRC polynomial used is x^8+x^4+x^3+x^2+1 (identified by 0x1D) with a SEED value of hexadecimal '0xFF'.

Figure 52 is an example of CRC encoding HW implementation:

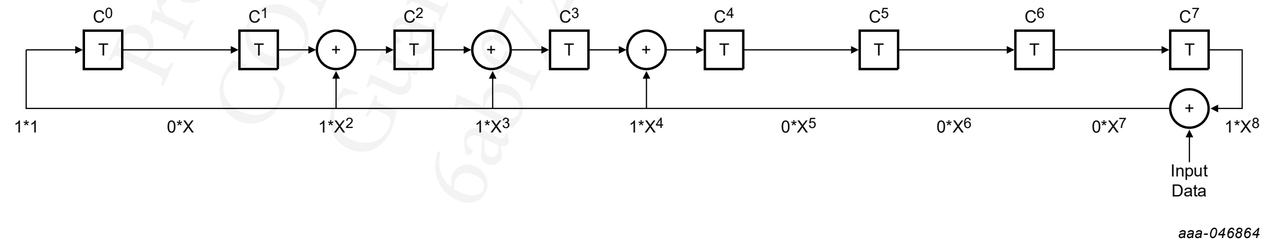


Figure 52. CRC encoder example

20.2.3.1 CRC encoding procedure

The effect of the CRC encoding procedure is shown in Table 70. The seed value is appended into the most significant bits of the shift register.

Table 70. Data preparation for CRC encoding

Seed	Register address	Read/write	Data_MSB	Data_LSB	
0xFF	Bits[31:25]	Bit[24]	Bits[23:16]	Bits[15:8]	
Seed…	… padded with the message to encode				… padded with 8 zeros

1. Using a serial CRC calculation method, the transmitter rotates the seed and data into the least significant bits of the shift register.
2. During the serial CRC calculation, the seed and the data bits are XOR compared with the polynomial data bits. When the MSB is logic 1, the comparison result is loaded in the register, otherwise the data bits are simply shifted. It must be noted the 32-bit message to be processed must have the bits corresponding to the CRC byte all equal to zero (00000000).
3. Once the CRC is calculated, it replaces the CRC byte initially set to all zeros and is transmitted.

20.2.3.2 CRC decoding procedure

1. The seed value is loaded into the most significant bits of the receive register.
2. Using a serial CRC calculation method, the receiver rotates the received message and CRC into the least significant bits of the shift register in the order received (MSB first).
3. When the calculation on the last bit of the CRC is rotated into the shift register, the shift register contains the CRC check result.
   - If the shift register contains all zeros, the CRC is correct.
   - If the shift register contains a value other than zero, the CRC is incorrect.

20.2.4 Electrical characteristics

Table 71. SPI electrical characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = 5.5 V to 40 V, unless otherwise specified. VDDIO = 3.0 V to 5.5 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Interface I/O input supply					
V_{DDIO}	VDDIO supply voltage range	3.0	-	5.5	V
Static electrical characteristics					
SPI_{VIL}	CSB, SCLK, MOSI low-level input voltage	0.3 x VDDIO	-	-	V
SPI_{VIH}	CSB, SCLK, MOSI high-level input voltage	-	-	0.7 x VDDIO	V
SPI_{HYST}	CSB, SCLK, MOSI input-voltage hysteresis	0.1	-	0.6	V
$SCLK_{Pull\text{-}Down}$	SCLK internal pulldown	100	200	400	kΩ
$MISO_{VOH}$	MISO high-output voltage (I = 2.0 mA)	VDDIO - 0.4	-	-	V
$MISO_{VOL}$	MISO low-output voltage (I = 2.0 mA)	-	-	0.4	V
I_{MISO}	Tristate leakage current (VDDIO = 5.0 V)	-5.0	-	5.0	µA

Table 71. SPI electrical characteristics*...continued*

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = 5.5 V to 40 V, unless otherwise specified. VDDIO = 3.0 V to 5.5 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
$SPI_{Pull-up}$	CSB, MOSI internal pullup (pullup to VDDIO)	100	200	400	kΩ
C_{SPI}	Input capacitor at CSB, SCLK, MOSI	-	-	10	pF
Dynamic electrical characteristics					
F_{SPI}	SPI operation frequency (50 % DC)	0.5	-	4.0	MHz
t_{CLH}	Minimum time SCLK = HIGH	125	-	-	ns
t_{CLL}	Minimum time SCLK = LOW	125	-	-	ns
t_{PCLD}	Propagation delay (SCLK to data at 10 % of MISO rising edge), Cout = 100 pF max	-	-	50	ns
t_{CSDV}	CSB = low to data at MISO active	-	-	100	ns
t_{SCLCH}	SCLK low before CSB low (setup time SCLK to CSB change H/L)	125	-	-	ns
t_{HCLCL}	SCLK change L/H after CSB = low	125	-	-	ns
t_{SCLD}	MOSI input setup time (SCLK change H/L after MOSI data valid)	100	-	-	ns
t_{HCLD}	MOSI input hold time (MOSI data hold after SCLK change H/L)	50	-	-	ns
t_{SCLCL}	SCLK low before CSB high	125	-	-	ns
t_{HCLCH}	SCLK high after CSB high	125	-	-	ns
t_{PCHD}	CSB L/H to MISO at high-impedance	-	-	100	ns
t_{ONCSB}	CSB minimum high time	5	-	-	µs
t_{CSB_MIN}	CSB filter time	10	-	40	ns

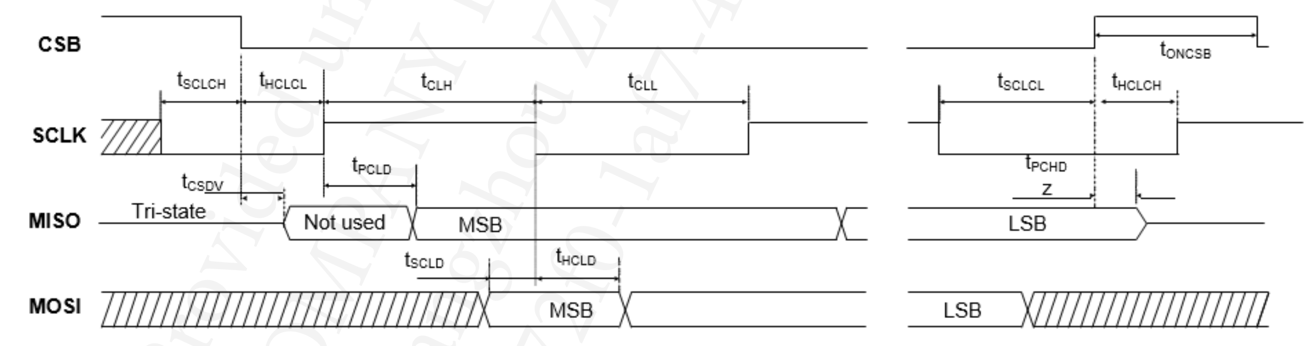


Figure 53. SPI timing diagram

21 SPI/I²C register mapping

Table 72. Main register mapping

Register	#	Address							Read/Write	Reference
		Adr_6	Adr_5	Adr_4	Adr_3	Adr_2	Adr_1	Adr_0		
M_DEV_CFG	0	0	0	0	0	0	0	0	Read only	Section 22.1
M_DEV_PROG_ID	1	0	0	0	0	0	0	1	Read only	Section 22.2
M_GEN_FLAG	2	0	0	0	0	0	1	0	Read only	Section 22.3
M_STATUS	3	0	0	0	0	0	1	1	Read only	Section 22.4
Reserved	4	0	0	0	0	1	0	0	Reserved	-
M_SYS_CFG	5	0	0	0	0	1	0	1	Read/Write	Section 22.5
M_SYS1_CFG	6	0	0	0	0	1	1	0	Read/Write	Section 22.6
M_REG_CTRL	7	0	0	0	0	1	1	1	Read/Write	Section 22.7
Reserved	8	0	0	0	1	0	0	0	Reserved	-
Reserved	9	0	0	0	1	0	0	1	Reserved	-
M_REG_FLG	10	0	0	0	1	0	1	0	Read/Write	Section 22.8
M_REG_MSK	11	0	0	0	1	0	1	1	Read/Write	Section 22.9
M_REG1_FLG	12	0	0	0	1	1	0	0	Read/Write	Section 22.10
M_REG1_MSK	13	0	0	0	1	1	0	1	Read/Write	Section 22.11
M_IO_CTRL	14	0	0	0	1	1	1	0	Write only	Section 22.12
M_IO_TIMER_FLG	15	0	0	0	1	1	1	1	Read/Write	Section 22.13
M_IO_TIMER_MSK	16	0	0	1	0	0	0	0	Read/Write	Section 22.14
M_VSUP_COM_FLG	17	0	0	1	0	0	0	1	Read/Write	Section 22.15
M_VSUP_COM_MSK	18	0	0	1	0	0	1	0	Read/Write	Section 22.16
M_IOWU_CFG	19	0	0	1	0	0	1	1	Read/Write	Section 22.17
M_IOWU_EN	20	0	0	1	0	1	0	0	Read/Write	Section 22.18
M_IOWU_FLG	21	0	0	1	0	1	0	1	Read/Write	Section 22.19
M_WU1_EN	22	0	0	1	0	1	1	0	Read/Write	Section 22.20
M_WU1_FLG	23	0	0	1	0	1	1	1	Read/Write	Section 22.21
M_TIMER1_CFG	24	0	0	1	1	0	0	0	Read/Write	Section 22.22
M_TIMER2_CFG	25	0	0	1	1	0	0	1	Read/Write	Section 22.23
M_TIMER3_CFG	26	0	0	1	1	0	1	0	Read/Write	Section 22.24
M_PWM1_CFG	27	0	0	1	1	0	1	1	Read/Write	Section 22.25
M_PWM2_CFG	28	0	0	1	1	1	0	0	Read/Write	Section 22.26
M_PWM3_CFG	29	0	0	1	1	1	0	1	Read/Write	Section 22.27
M_TIMER_PWM_CTRL	30	0	0	1	1	1	1	0	Read/Write	Section 22.28
M_CS_CFG	31	0	0	1	1	1	1	1	Read/Write	Section 22.29
M_CS_FLG_MSK	32	0	1	0	0	0	0	0	Read/Write	Section 22.30

Table 72. Main register mapping*...continued*

Register	#	Address							Read/Write	Reference
		Adr_6	Adr_5	Adr_4	Adr_3	Adr_2	Adr_1	Adr_0		
M_HSx_SRC_CFG	33	0	1	0	0	0	0	1	Read/Write	Section 22.31
M_HSx_CTRL	34	0	1	0	0	0	1	0	Read/Write	Section 22.32
M_HSx_FLG	35	0	1	0	0	0	1	1	Read/Write	Section 22.33
M_HSx_MSK	36	0	1	0	0	1	0	0	Read/Write	Section 22.34
M_AMUX_CTRL	37	0	1	0	0	1	0	1	Read/Write	Section 22.35
M_LDT_CFG1	38	0	1	0	0	1	1	0	Read/Write	Section 22.36
M_LDT_CFG2	39	0	1	0	0	1	1	1	Read/Write	Section 22.37
M_LDT_CFG3	40	0	1	0	1	0	0	0	Read/Write	Section 22.38
M_LDT_CTRL	41	0	1	0	1	0	0	1	Read/Write	Section 22.39
M_CAN	42	0	1	0	1	0	1	0	Read/Write	Section 22.40
M_LIN	43	0	1	0	1	0	1	1	Read/Write	Section 22.41
M_CAN_LIN_MSK	44	0	1	0	1	1	0	0	Read/Write	Section 22.42
M_MEMORY0	45	0	1	0	1	1	0	1	Read/Write	Section 22.43
M_MEMORY1	46	0	1	0	1	1	1	0	Read/Write	Section 22.44

Table 73. Safety-related register mapping

Register	#	Address							Read/Write	Reference
		Adr_6	Adr_5	Adr_4	Adr_3	Adr_2	Adr_1	Adr_0		
FS_I_OVUV_CFG1	50	0	1	1	0	0	1	0	Write during INIT then Read only	Section 22.45
FS_I_OVUV_CFG2	51	0	1	1	0	0	1	1	Write during INIT then Read only	Section 22.46
FS_I_FCCU_CFG	52	0	1	1	0	1	0	0	Write during INIT then Read only	Section 22.47
Reserved	53	0	1	1	0	1	0	1	Reserved	-
FS_I_FSSM_CFG	54	0	1	1	0	1	1	0	Write during INIT then Read only	Section 22.48
FS_I_WD_CFG	55	0	1	1	0	1	1	1	Write during INIT then Read only	Section 22.49
FS_WDW_CFG	56	0	1	1	1	0	0	0	Read/Write	Section 22.50
FS_WD_TOKEN	57	0	1	1	1	0	0	1	Read only	Section 22.51
FS_WD_ANSWER	58	0	1	1	1	0	1	0	Write only	Section 22.52
FS_LIMP12_CFG	59	0	1	1	1	0	1	1	Read/Write	Section 22.53
FS_FS0B_LIMP0_REL	60	0	1	1	1	1	0	0	Read/Write	Section 22.54
FS_ABIST	61	0	1	1	1	1	0	1	Read/Write	Section 22.55
Reserved	62	0	1	1	1	1	1	0	Reserved	-
FS_SAFETY_OUTPUTS	63	0	1	1	1	1	1	1	Read/Write	Section 22.56
FS_SAFETY_FLG	64	1	0	0	0	0	0	0	Read/Write	Section 22.57
FS_CRC	65	1	0	0	0	0	0	1	Read/Write	Section 22.58

21.1 Readable registers

Logic	Register name	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Main	M_DEV_ CFG	0	0	CAN_EN	LIN_EN	LDTIM_EN	HSD13_EN	HSD24_EN	V2_EN	V1_PNP_EN	ABIST_EN	FCCU_EN	FS0B_EN	LIMP0_EN	V0MON_EN	0	0
	M_DEV_ PROG_ID	FULL_LAYER_REV				METAL_LAYER_REV				PROG_IDH				PROG_IDL			
	M_GEN_ FLAG	0	0	0	0	0	0	0	0	HSxG	SAFETYG	PHYG	WUG	IOTIMG	COMG	VSUPG	VxG
	M_STATUS	V1 TWARN_S	LPON_S	NORMAL_S	INIT_S	0	WK2_S	WK1_S	HVIO2_S	HVIO1_S	LVI5_S	LVIO4_S	LVIO3_S	V1_MODE	V1_S	V2_S	V3_S
	M_SYS_ CFG	0	BAT_FAIL	0	POR	0	LOCK_INIT	0	0	0	0	INT_TO_ WUEN	0	INTB_DUR	0	MOD_CONF	MOD_EN
	M_SYS1_ CFG	0	0	0	VBOS2 V1_SW_ ALWAYS_EN	0	LOAD_ OTP_BYP	SLOT_BYP	TSLOT_ DOWN_CFG	0	0	0	0	DBG_MODE	0	0	OTP_MODE
	M_REG_ CTRL	0	0	0	BUCK_SRHSOFF		BUCK_SRHSON			0	0	V2ON_ LPON	0	0	V3ON_ LPON	0	0
	M_REG_ FLG	V0UV_I	V0OV_I	V1TWARN_I	V1TSD_I	V2TSD_I	V3TSD_I	V2OL_I	V1UV_I	V2UV_I	V3UV_I	V1OV_I	V2OV_I	V3OV_I	V1OC_I	V2OC_I	V3OC_I
	M_REG_ MSK	V0UV_M	V0OV_M	V1 TWARN_M	V1TSD_M	V2TSD_M	V3TSD_M	V2OL_M	V1UV_M	V2UV_M	V3UV_M	V1OV_M	V2OV_M	V3OV_M	V1OC_M	V2OC_M	V3OC_M
	M_REG1_ FLG	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	V1_OCLS_I
	M_REG1_ MSK	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	V1_OCLS_M
	M_IO_ TIMER_FLG	0	0	0	0	0	0	0	LDT_I	LVI5_I	LVIO4_I	LVIO3_I	HVIO2_I	HVIO1_I	0	WK2_I	WK1_I
	M_IO_ TIMER_MSK	0	0	0	0	0	0	0	LDT_M	LVI5_M	LVIO4_M	LVIO3_M	HVIO2_M	HVIO1_M	0	WK2_M	WK1_M
	M_VSUP_ COM_FLG	0	0	0	VBOS2 V1SW_S	VBOS_UV	0	I2C_CRC_I	I2C_REQ_I	SPI_CRC_I	SPI_CLK_I	SPI_REQ_I	0	VSHS_OV_I	VSHS_UV_I	VSUPOV_I	VSUPUV_I
	M_VSUP_ COM_MSK	0	0	0	0	0	0	I2C_CRC_M	I2C_REQ_M	SPI_CRC_M	SPI_CLK_M	SPI_REQ_M	0	VSHS_ OV_M	VSHS_ UV_M	VSUPOV_M	VSUPUV_M
	M_IOWU_ CFG	LVI5_ WUCFG	LVIO4_ WUCFG	LVIO3_ WUCFG	0	HVIO2_ DGLT	HVIO1_ DGLT	WK2_DGLT	WK1_DGLT	HVIO2_WUCFG		HVIO1_WUCFG		WK2_WUCFG		WK1_WUCFG	
	M_ IOWU_EN	0	0	LVI5_WUEN		LVIO4_WUEN		LVIO3_WUEN		HVIO2_WUEN		HVIO1_WUEN		WK2_WUEN		WK1_WUEN	
	M_IOWU_ FLG	LVI5_WU_I	LVIO4_WU_I	LVIO3_WU_I	0	HVIO2_ CYS_RDY	HVIO1_ CYS_RDY	HVIO2_ CYC_S	HVIO1_ CYC_S	HVIO2_ WU_I	HVIO1_ WU_I	WK2_ CYS_RDY	WK1_ CYS_RDY	WK2_ CYC_S	WK1_ CYC_S	WK2_WU_I	WK1_WU_I
	M_WU1_EN	0	0	0	0	0	0	0	0	0	0	LDT_WUEN		LIN_WUEN		CAN_WUEN	
	M_WU1_ FLG	0	0	0	0	0	0	FS_EVT	EXT_ RSTB_WU	WD_ OFL_WU	V1_ UVLP_WU	INT_TO_WU	GO2 NORMAL_ WU	0	LDT_WU_I	LIN_WU_I	CAN_WU_I
	M_TIMER1_ CFG	0	0	0	0	0	0	0	TIMER1_DLY		TIMER1_ON				TIMER1_PER		

Logic	Register name	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	M_TIMER2_CFG	0	0	0	0	0	0	0	TIMER2_DLY		TIMER2_ON				TIMER2_PER		
	M_TIMER3_CFG	0	0	0	0	0	0	0	TIMER3_DLY		TIMER3_ON				TIMER3_PER		
	M_PWM1_CFG	0	0	0	PWM1_DLY		PWM1_F	PWM1_DC									
	M_PWM2_CFG	0	0	0	PWM2_DLY		PWM2_F	PWM2_DC									
	M_PWM3_CFG	0	0	0	PWM3_DLY		PWM3_F	PWM3_DC									
	M_TIMER_PWM_CTRL	0	0	0	0	0	0	0	0	0	TIM1_EN	TIM2_EN	TIM3_EN	0	PWM1_EN	PWM2_EN	PWM3_EN
	M_CS_CFG	0	0	0	0	0	0	HS_FLT_WU_FORCE	0	HVIO2_HS_SEL		HVIO1_HS_SEL		WK2_HS_SEL		WK1_HS_SEL	
	M_CS_FLG_MSK	0	0	0	0	0	0	0	HVIO2_OL_M	HVIO1_OL_M	WAKE2_OL_M	WAKE1_OL_M	0	HVIO2_OL_I	HVIO1_OL_I	WAKE2_OL_I	WAKE1_OL_I
	M_HSx_SRC_CFG	HS4_SRC_SEL				HS3_SRC_SEL				HS2_SRC_SEL				HS1_SRC_SEL			
	M_HSx_CTRL	0	HS_VSHSUVOV_REC	HS_VSHSUV_DIS	HS_VSHSOV_DIS	0	0	0	0	0	HS4_EN	0	HS3_EN	0	HS2_EN	0	HS1_EN
	M_HSx_FLG	0	0	0	HS4_OL_I	HS4_OC_I	0	HS3_OL_I	HS3_OC_I	HS34_TSD_I	0	HS2_OL_I	HS2_OC_I	0	HS1_OL_I	HS1_OC_I	HS12_TSD_I
	M_HSx_MSK	0	0	0	HS4_OL_M	HS4_OC_M	0	HS3_OL_M	HS3_OC_M	HS34_TSD_M	0	HS2_OL_M	HS2_OC_M	0	HS1_OL_M	HS1_OC_M	HS12_TSD_M
	M_AMUX_CTRL	0	0	0	0	0	0	AMUX_EN	AMUX_DIV	0	0	0	AMUX				
	M_LDT_CFG1	LDT_AFTER_RUN															
	M_LDT_CFG2	LDT_WUP_L															
	M_LDT_CFG3	0	0	0	0	0	0	0	0	LDT_WUP_H							
	M_LDT_CTRL	0	0	0	0	0	0	0	0	LDT2LP	LDT_FNCT			LDT_SEL	LDT_MODE	LDT_EN	LDT_RUN
	M_CAN	0	0	0	0	0	0	CAN_MODE		CAN_ACTIVE_MODE_S	0	CAN_FS_DIS	0	0	0	CAN_TXD_TO_I	CAN_TSD_I
	M_LIN	0	LIN_MODE		LIN_SLOPE		LIN_FS_DIS	LIN_VSHSUV_DIS	LIN_SC	LIN_TXD_TO	0	0	0	0	LIN_SC_I	LIN_TXD_TO_I	LIN_TSD_I
	M_CAN_LIN_MSK	0	0	LIN_FSM_STATE_S					LIN_SC_M	LIN_TXD_TO_M	LIN_TSD_M	0	CAN_FSM_STATE_S			CAN_TXD_TO_M	CAN_TSD_M
	M_MEMORY0	MEMORY0[15]	MEMORY0[14]	MEMORY0[13]	MEMORY0[12]	MEMORY0[11]	MEMORY0[10]	MEMORY0[9]	MEMORY0[8]	MEMORY0[7]	MEMORY0[6]	MEMORY0[5]	MEMORY0[4]	MEMORY0[3]	MEMORY0[2]	MEMORY0[1]	MEMORY0[0]
	M_MEMORY1	MEMORY1[15]	MEMORY1[14]	MEMORY1[13]	MEMORY1[12]	MEMORY1[11]	MEMORY1[10]	MEMORY1[9]	MEMORY1[8]	MEMORY1[7]	MEMORY1[6]	MEMORY1[5]	MEMORY1[4]	MEMORY1[3]	MEMORY1[2]	MEMORY1[1]	MEMORY1[0]

Logic	Register name	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Fail-safe	FS_I_OVUV_CFG1	0	0	0	V1MON_OV_RSTB_IMPACT	V1MON_OV_FS0B_IMPACT	V1MON_OV_LIMP0_IMPACT	V1MON_UV_RSTB_IMPACT	V1MON_UV_FS0B_IMPACT	V1MON_UV_LIMP0_IMPACT	0	V2MON_OV_RSTB_IMPACT	V2MON_OV_FS0B_IMPACT	V2MON_OV_LIMP0_IMPACT	V2MON_UV_RSTB_IMPACT	V2MON_UV_FS0B_IMPACT	V2MON_UV_LIMP0_IMPACT
	FS_I_OVUV_CFG2	0	0	0	V3MON_OV_RSTB_IMPACT	V3MON_OV_FS0B_IMPACT	V3MON_OV_LIMP0_IMPACT	V3MON_UV_RSTB_IMPACT	V3MON_UV_FS0B_IMPACT	V3MON_UV_LIMP0_IMPACT	0	V0MON_OV_RSTB_IMPACT	V0MON_OV_FS0B_IMPACT	V0MON_OV_LIMP0_IMPACT	V0MON_UV_RSTB_IMPACT	V0MON_UV_FS0B_IMPACT	V0MON_UV_LIMP0_IMPACT
	FS_I_FCCU_CFG	0	FCCU_CFG			FCCU2_ASSIGN			FCCU12_FLT_POL	FCCU2_FLT_POL	FCCU1_FLT_POL	FCCU2_RSTB_IMPACT	FCCU2_FS0B_IMPACT	FCCU2_LIMP0_IMPACT	FCCU1_RSTB_IMPACT	FCCU1_FS0B_IMPACT	FCCU1_LIMP0_IMPACT
	FS_I_FSSM_CFG	0	EXT_RSTB_DIS	RSTB8S_DIS	RSTB_DUR	LIMP0_SC_RSTB_IMPACT	EXTRSTB_FS0B_IMPACT	FS0B_SC_RSTB_IMPACT	FLT_ERR_LIMIT		FLT_MID_RSTB_IMPACT	FLT_MID_FS0B_IMPACT	FLT_MID_LIMP0_IMPACT	FLT_ERR_CNT			
	FS_I_WD_CFG	0	WD_RSTB_IMPACT	WD_FS0B_IMPACT	WD_LIMP0_IMPACT	WD_DIS_LPON	WD_RFR_LIMIT		WD_ERR_LIMIT		WD_RFR_CNT			WD_ERR_CNT			
	FS_WDW_CFG	0	0	0	0	WDW_REC_EN	WDW_EN	0	WDW_PERIOD				0	WDW_RECOVERY			
	FS_WD_TOKEN	WD_TOKEN															
	FS_LIMP12_CFG	0	0	0	0	0	0	0	LIMP2_DC_CFG		LIMP2_CFG		0	0	LIMP1_CFG		0
	FS_FS0B_LIMP0_REL	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	FS_ABIST	ABIST_READY	0	0	ABIST_DONE	ABIST_ONGOING	ABIST_V0MON_DIAG	ABIST_V1UVLP_DIAG	ABIST_V1MON_DIAG	ABIST_V2MON_DIAG	ABIST_V3MON_DIAG	0	ABIST_V0MON	ABIST_V1UVLP	ABIST_V1MON	ABIST_V2MON	ABIST_V3MON
	FS_SAFETY_OUTPUTS	0	RSTB_EXT	RSTB_EVT	RSTB_DRV	RSTB_SNS	RSTB_DIAG	0	FS0B_DRV	FS0B_SNS	FS0B_DIAG	0	0	LIMP0_DRV	LIMP0_SNS	LIMP0_DIAG	0
	FS_SAFETY_FLG	FCCU12_ERR_S	FCCU1_ERR_S	FCCU2_ERR_S	INIT_CRC_NOK_M	INIT_CRC_NOK_I	WD_NOK_M	WD_NOK_I	0	FCCU12_M	FCCU1_M	FCCU2_M	FCCU12_I	FCCU1_I	FCCU2_I	FCCU1_S	FCCU2_S
	FS_CRC	0	0	0	0	0	INIT_CRC_FS0B_IMPACT	INIT_CRC_LIMP0_IMPACT	0	CRC_VALUE							

21.2 Writable registers

Logic	Register name	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default value
Main	M_SYS_CFG	-	-	-	-	-	LOCK_INIT	GO2INIT	GO2 NORMAL	GO2LPON	GO2LPOFF	INT_TO_WUEN	INTB_REQ	INTB_DUR	-	MOD_CONF	MOD_EN	OTP fuse
	M_SYS1_CFG	-	-	-	VBOS2_V1_SW_ALWAYS_EN	-	LOAD_OTP_BYP	SLOT_BYP	TSLOT_DOWN_CFG	-	SOFTPOR_REQ	-	DBG_EXIT	-	-	OTP_EXIT	-	OTP fuse
	M_REG_CTRL	-	-	-	BUCK_SRHSOFF		BUCK_SRHSON			-	-	V2ON_LPON	V2EN	V2DIS	V3ON_LPON	V3EN	V3DIS	OTP fuse
	M_REG_MSK	V0UV_M	V0OV_M	V1 TWARN_M	V1TSD_M	V2TSD_M	V3TSD_M	V2OL_M	V1UV_M	V2UV_M	V3UV_M	V1OV_M	V2OV_M	V3OV_M	V1OC_M	V2OC_M	V3OC_M	0x0000
	M_REG1_MSK	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	V1_OCLS_M	0x0000
	M_IO_CTRL	-	-	-	-	-	-	HVIO1HI	HVIO1LO	HVIO2HI	HVIO2LO	LVIO3HI	LVIO3LO	LVIO4HI	LVIO4LO	LVO6HI	LVO6LO	0x0000
	M_IO_TIMER_MSK	-	-	-	-	-	-	-	LDT_M	LVI5_M	LVIO4_M	LVIO3_M	HVIO2_M	HVIO1_M	-	WK2_M	WK1_M	0x0000
	M_VSUP_COM_MSK	-	-	-	-	-	-	I2C_CRC_M	I2C_REQ_M	SPI_CRC_M	SPI_CLK_M	SPI_REQ_M	-	VSHS_OV_M	VSHS_UV_M	VSUPOV_M	VSUPUV_M	0x0000
	M_IOWU_CFG	LVI5_WUCFG	LVIO4_WUCFG	LVIO3_WUCFG	Reserved	HVIO2_DGLT	HVIO1_DGLT	WK2_DGLT	WK1_DGLT	HVIO2_WUCFG		HVIO1_WUCFG		WK2_WUCFG		WK1_WUCFG		0x0005
	M_IOWU_EN	-	-	LVI5_WUEN		LVIO4_WUEN		LVIO3_WUEN		HVIO2_WUEN		HVIO1_WUEN		WK2_WUEN		WK1_WUEN		0x00FF
	M_WU1_EN	-	-	-	-	-	-	-	-	-	-	LDT_WUEN		LIN_WUEN		CAN_WUEN		0x000F
	M_TIMER1_CFG	-	-	-	-	-	-	-	TIMER1_DLY		TIMER1_ON				TIMER1_PER			0x0000
	M_TIMER2_CFG	-	-	-	-	-	-	-	TIMER2_DLY		TIMER2_ON				TIMER2_PER			0x0000
	M_TIMER3_CFG	-	-	-	-	-	-	-	TIMER3_DLY		TIMER3_ON				TIMER3_PER			0x0000
	M_PWM1_CFG	-	-	-	PWM1_DLY		PWM1_F	PWM1_DC										0x0000
	M_PWM2_CFG	-	-	-	PWM2_DLY		PWM2_F	PWM2_DC										0x0000
	M_PWM3_CFG	-	-	-	PWM3_DLY		PWM3_F	PWM3_DC										0x0000
	M_TIMER_PWM_CTRL	-	-	-	-	-	-	-	-	-	TIM1_EN	TIM2_EN	TIM3_EN	-	PWM1_EN	PWM2_EN	PWM3_EN	0x0000
	M_CS_CFG	-	-	-	-	-	-	HS_FLT_WU_FORCE	-	HVIO2_HS_SEL		HVIO1_HS_SEL		WK2_HS_SEL		WK1_HS_SEL		0x0000

Logic	Register name	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default value
	M_CS_FLG_MSK	-	-	-	-	-	-	-	HVIO2_OL_M	HVIO1_OL_M	WAKE2_OL_M	WAKE1_OL_M	-	-	-	-	-	0x0000
	M_HSx_SRC_CFG	HS4_SRC_SEL				HS3_SRC_SEL				HS2_SRC_SEL				HS1_SRC_SEL				0x0000
	M_HSx_CTRL	-	HS_VSHSUVOV_REC	HS_VSHSUV_DIS	HS_VSHSOV_DIS	-	-	-	-	-	HS4_EN	-	HS3_EN	-	HS2_EN	-	HS1_EN	0x0000
	M_HSx_MSK	-	-	-	HS4_OL_M	HS4_OC_M	-	HS3_OL_M	HS3_OC_M	HS34_TSD_M	-	HS2_OL_M	HS2_OC_M	-	HS1_OL_M	HS1_OC_M	HS12_TSD_M	0x0000
	M_AMUX_CTRL	-	-	-	-	-	-	AMUX_EN	AMUX_DIV	-	-	-	AMUX					0x0000
	M_LDT_CFG1	LDT_AFTER_RUN																0x0000
	M_LDT_CFG2	LDT_WUP_L																0x0000
	M_LDT_CFG3	-	-	-	-	-	-	-	-	LDT_WUP_H								0x0000
	M_LDT_CTRL	-	-	-	-	-	-	-	-	LDT2LP	LDT_FNCT			LDT_SEL	LDT_MODE	LDT_EN	-	0x0000
	M_CAN	-	-	-	-	-	-	CAN_MODE		-	-	CAN_FS_DIS	-	-	-	CAN_TXD_TO_I	CAN_TSD_I	0x0000
	M_LIN	-	LIN_MODE		LIN_SLOPE		LIN_FS_DIS	LIN_VSHSUV_DIS	LIN_SC	LIN_TXD_TO	-	-	-	-	LIN_SC_I	LIN_TXD_TO_I	LIN_TSD_I	0x0000
	M_CAN_LIN_MSK	-	-	LIN_FSM_STATE_S					LIN_SC_M	LIN_TXD_TO_M	LIN_TSD_M	-	CAN_FSM_STATE_S			CAN_TXD_TO_M	CAN_TSD_M	0x0000
	M_MEMORY0	MEMORY0																0x0000
	M_MEMORY1	MEMORY1																0x0000
Fail-safe	FS_I_OVUV_CFG1	-	-	-	V1MON_OV_RSTB_IMPACT	V1MON_OV_FS0B_IMPACT	V1MON_OV_LIMP0_IMPACT	V1MON_UV_RSTB_IMPACT	V1MON_UV_FS0B_IMPACT	V1MON_UV_LIMP0_IMPACT	-	V2MON_OV_RSTB_IMPACT	V2MON_OV_FS0B_IMPACT	V2MON_OV_LIMP0_IMPACT	V2MON_UV_RSTB_IMPACT	V2MON_UV_FS0B_IMPACT	V2MON_UV_LIMP0_IMPACT	OTP fuse
	FS_I_OVUV_CFG2	-	-	-	V3MON_OV_RSTB_IMPACT	V3MON_OV_FS0B_IMPACT	V3MON_OV_LIMP0_IMPACT	V3MON_UV_RSTB_IMPACT	V3MON_UV_FS0B_IMPACT	V3MON_UV_LIMP0_IMPACT	-	V0MON_OV_RSTB_IMPACT	V0MON_OV_FS0B_IMPACT	V0MON_OV_LIMP0_IMPACT	V0MON_UV_RSTB_IMPACT	V0MON_UV_FS0B_IMPACT	V0MON_UV_LIMP0_IMPACT	OTP fuse
	FS_I_FCCU_CFG	-	FCCU_CFG			FCCU2_ASSIGN			FCCU12_FLT_POL	FCCU2_FLT_POL	FCCU1_FLT_POL	FCCU2_RSTB_IMPACT	FCCU2_FS0B_IMPACT	FCCU2_LIMP0_IMPACT	FCCU1_RSTB_IMPACT	FCCU1_FS0B_IMPACT	FCCU1_LIMP0_IMPACT	0X103F
	FS_I_FSSM_CFG	-	EXT_RSTB_DIS	RSTB8S_DIS	RSTB_DUR	LIMP0_SC_RSTB_IMPACT	EXTRSTB_FS0B_IMPACT	FS0B_SC_RSTB_IMPACT	FLT_ERR_LIMIT		FLT_MID_RSTB_IMPACT	FLT_MID_FS0B_IMPACT	FLT_MID_LIMP0_IMPACT	FLT_ERR_CNT				OTP fuse
	FS_I_WD_CFG	-	WD_RSTB_IMPACT	WD_FS0B_IMPACT	WD_LIMP0_IMPACT	WD_DIS_LPON	WD_RFR_LIMIT		WD_ERR_LIMIT		-	-	-	-	-	-	-	0x7080
	FS_WDW_CFG	-	-	-	-	WDW_REC_EN	WDW_EN	-	WDW_PERIOD				-	WDW_RECOVERY				0x01AB

Logic	Register name	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default value
	FS_WD_ANSWER	WD_ANSWER																0x0000
	FS_LIMP12_CFG	-	-	-	-	-	-	-	LIMP2_DC_CFG		LIMP2_CFG		LIMP2_REQ	-	LIMP1_CFG		LIMP1_REQ	OTP fuse
	FS_FS0B_LIMP0_REL	RELEASE_FS0B_LIMP0																0x0000
	FS_ABIST	-	LAUNCH_ABIST	CLEAR_ABIST	-	-	-	-	-	-	-	-	ABIST_V0MON	ABIST_V1UVLP	ABIST_V1MON	ABIST_V2MON	ABIST_V3MON	0x0000
	FS_SAFETY_OUTPUTS	-	-	-	-	-	-	RSTB_REQ	-	-	-	FS0B_REQ	-	-	-	-	LIMP0_REQ	0x0000
	FS_SAFETY_FLG	-	-	-	INIT_CRC_NOK_M	-	WD_NOK_M	-	-	FCCU12_M	FCCU1_M	FCCU2_M	-	-	-	-	-	0x0000
	FS_CRC	-	INIT_CRC_REQ	-	-	-	INIT_CRC_FS0B_IMPACT	INIT_CRC_LIMP0_IMPACT	-	CRC_VALUE								0x0000

22 SPI/I²C register description

22.1 M_DEV_CFG

Table 74. M_DEV_CFG register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	-	-	-	-	-	-	-	-
Read	0	0	CAN_EN	LIN_EN	LDTIM_EN	HSD13_EN	HSD24_EN	V2_EN
Reset	0	0	OTP fuse	OTP fuse	OTP fuse	OTP fuse	OTP fuse	OTP fuse
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	-	-	-	-	-	-	-	-
Read	V1_PNP_EN	ABIST_EN	FCCU_EN	FS0B_EN	LIMP0_EN	V0MON_EN	0	0
Reset	OTP fuse	OTP fuse	OTP fuse	OTP fuse	OTP fuse	OTP fuse	0	0

Table 75. M_DEV_CFG register bit description

Bit	Symbol	Description
2	V0MON_EN	**Report the enable of VMON_EXT**
		0 VMON_EXT is disabled
		1 VMON_EXT is enabled
		OTP Fuse load
3	LIMP0_EN	**Report the enable of LIMP0**
		0 LIMP0 is disabled
		1 LIMP0 is enabled
		OTP Fuse load
4	FS0B_EN	**Report the enable of FS0B**
		0 FS0B is disabled
		1 FS0B is enabled
		OTP Fuse load
5	FCCU_EN	**Report the enable of FCCU**
		0 FCCU is disabled
		1 FCCU is enabled
		OTP Fuse load
6	ABIST_EN	**Report the enable of ABIST on demand**
		0 ABIST on demand is disabled
		1 ABIST on demand is enabled
		OTP Fuse load
7	V1_PNP_EN	**Report the enable of V1 PNP mode**
		0 V1 PNP mode is disabled
		1 V1 PNP mode is enabled
		OTP Fuse load
8	V2_EN	**Report the enable of V2 regulator by OTP**
		0 V2 regulator is disabled by OTP
		1 V2 regulator is enabled by OTP
		OTP Fuse load
9	HSD24_EN	**Report the enable of HS2 and HS4**
		0 HS2 and HS4 are disabled

Table 75. M_DEV_CFG register bit description*...continued*

Bit	Symbol	Description
		1 HS2 and HS4 are enabled
		OTP Fuse load
10	HSD13_EN	**Report the enable of HS1 and HS3**
		0 HS1 and HS3 are disabled
		1 HS1 and HS3 are enabled
		OTP Fuse load
11	LDTIM_EN	**Report the enable of the Long Duration Timer (LDT)**
		0 LDT is disabled
		1 LDT is enabled
		OTP Fuse load
12	LIN_EN	**Report the enable of the LIN**
		0 The LIN is disabled
		1 The LIN is enabled
		OTP Fuse load
13	CAN_EN	**Report the enable of the CAN**
		0 The CAN is disabled
		1 The CAN is enabled
		OTP Fuse load

22.2 M_DEV_PROG_ID

Table 76. M_DEV_PROG_ID register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	-	-	-	-	-	-	-	-
Read	FULL_LAYER_REV				METAL_LAYER_REV			
Reset	0	0	0	1	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	-	-	-	-	-	-	-	-
Read	PROG_IDH				PROG_IDL			
Reset	OTP fuse				OTP fuse			

Table 77. M_DEV_PROG_ID register bit description

Bit	Symbol	Description
0 to 3	PROG_IDL	**Report the first digit of the OTP code (0-F)**
		Program ID dependent
		OTP Fuse load
4 to 7	PROG_IDH	**Report the second digit of the OTP code (A-R)**
		Program ID dependent
		OTP Fuse load
8 to 11	METAL_ LAYER_REV	**Report the Metal Mask revision**
		0000 Rev A0 (Default full Layer revision)
		0001 Rev X1
		0010 Rev X2
		0011 Rev X3
		0100 Rev X4
		0101 Rev X5
		0110 Rev X6
		0111 Rev X7
		1000 Rev X8
		1001 Rev X9
		1010 Rev X10
		1011 Rev X11
		1100 Rev X12
		1101 Rev X13
		1110 Rev X14
		1111 Rev X15
		N/A
12 to 15	FULL_LAYER_REV	**Report the Full Layer Mask revision (X)**
		0000 Unused
		0001 Pass A silicon
		0010 Pass B silicon
		0011 Pass C silicon
		0100 Pass D silicon
		0101 Pass E silicon
		0110 Pass F silicon

Table 77. M_DEV_PROG_ID register bit description...*continued*

Bit	Symbol	Description
		0111 Pass G silicon
		1000 Pass H silicon
		1001 Pass I silicon
		1010 Pass J silicon
		1011 Pass K silicon
		1100 Pass L silicon
		1101 Pass M silicon
		1110 Pass N silicon
		1111 Pass O silicon
		N/A

22.3 M_GEN_FLAG

Table 78. M_GEN_FLAG register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	-	-	-	-	-	-	-	-
Read	-	-	-	-	-	-	-	-
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	-	-	-	-	-	-	-	-
Read	HSxG	SAFETYG	PHYG	WUG	IOTIMG	COMG	VSUPG	VxG
Reset	0	0	0	0	0	0	0	0

Table 79. M_GEN_FLAG register bit description

Bit	Symbol	Description
0	VxG	**Report an event on a regulator VxG = V3OC_I or V3OV_I or V3UV_I or V3TSD_I or V2OC_I or V2OV_I or V2UV_I or V2TSD_I or V2OL_I or V1OC_I or V1OV_I or V1UV_I or V1TSD_I or V1TWARN_I or V1_OCLS_I or V0UV_I or V0OV_I**
		0 No event
		1 Vx event occurred
		POR, cleared when all Vx flags are cleared
1	VSUPG	**Report a VSUP error VSUPG = VSUP_UV_I or VSUP_OV_I or VSHS_OV_I or VSHS_UV_I**
		0 No error
		1 VSUP error reported
		POR, cleared when all VSUP flags are cleared
2	COMG	**Report an error on the communication (SPI or I2C) COMG = SPI_REQ_I or SPI_CLK_I or SPI_CRC_I or I2C_REQ_I or I2C_CRC_I**
		0 No error
		1 Communication error reported
		POR, cleared when all COM flags are cleared
3	IOTIMG	**Report an IO or LDT event IOTIMG = WK1_I or WK2_I or HVIO1_I or HVIO2_I or LVIO3_I or LVIO4_I or LVI5_I or LDT_I**
		0 No event
		1 event occurred
		POR, cleared when all IO and LDT flags are cleared

Table 79. M_GEN_FLAG register bit description*...continued*

Bit	Symbol	Description
4	WUG	**Report a wake up event WUG = LVI5_WU_I or LVIO4_WU_I or LVIO3_WU_I or HVIO2_WU_I or HVIO1_WU_I or WK2_WU_I or WK1_WU_I or CAN_WU_I or LIN_WU_I or LDT_WU_I or INT_TO_WU or WD_OFL_WU or V1_UVLP_WU or GO2NORMAL_WU or EXT_RSTB_WU**
		0 No event
		1 Wake up event occurred
		POR, cleared when all WU flags are cleared
5	PHYG	**Report a Physical Layer error PHYG = LIN_TSD_I or LIN_TXD_TO_I or LIN_SC_I or CAN_TSD_I or CAN_TXD_TO_I**
		0 No error
		1 CAN or LIN error reported
		POR, cleared when all CAN and LIN flags are cleared
6	SAFETYG	Report a safety related error SAFETYG = WD_NOK_I or FCCU12_I or FCCU1_I or FCCU2_I or INIT_CRC_NOK_I
		0 No error
		1 Watchdog Refresh error reported
		POR, cleared when all WD flags are cleared
7	HSxG	**Report a High Side event or a Cyclic Sense event HSxG = HS1_OL_I or HS1_OC_I or HS12_TSD_I or HS2_OL_I or HS2_OC_I or HS3_OL_I or HS3_OC_I or HS34_TSD_I or HS4_OL_I or HS4_OC_I or WAKE1_OL_I or WAKE2_OL_I or HVIO1_OL_I or HVIO2_OL_I**
		0 No error
		1 event reported
		POR, cleared when all HSx and cyclic sense flags are cleared

22.4 M_STATUS

Table 80. M_STATUS register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	-	-	-	-	-	-	-	-
Read	V1TWARN_S	LPON_S	NORMAL_S	INIT_S	0	WK2_S	WK1_S	HVIO2_S
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	-	-	-	-	-	-	-	-
Read	HVIO1_S	LVI5_S	LVIO4_S	LVIO3_S	V1_MODE	V1_S	V2_S	V3_S
Reset	0	0	0	0	0	0	0	0

Table 81. M_STATUS register bit description

Bit	Symbol	Description
0	V3_S	**Real-time Status of V1 Regulator**
		0 V3 is Disabled
		1 V3 is Enabled
		Real-time information
1	V2_S	**Real-time status of V2 Regulator**
		0 V2 is Disabled
		1 V2 is Enabled
		Real-time information
2	V1_S	**Real-time status of V1 Regulator**
		0 V1 is Disabled

Table 81. M_STATUS register bit description*...continued*

Bit	Symbol	Description
		1 V1 is Enabled
		Real-time information
3	V1_MODE	**Real-time status of the HVBUCK mode or HVLDO1 mode when used with ext PNP**
		0 BUCK is in PWM mode or HVLDO1 PNP is enabled
		1 BUCK is in PFM mode or HVLDO1 PNP is disabled
		Real-time information
4	LVIO3_S	**Real-time status of LVIO3 input**
		0 LVIO3 is Low
		1 LVIO3 is High
		Real-time information
5	LVIO4_S	**Real-time status of LVIO4 input**
		0 LVIO4 is Low
		1 LVIO4 is High
		Real-time information
6	LVI5_S	**Real-time status of LVI5 input**
		0 LVI5 is Low
		1 LVI5 is High
		Real-time information
7	HVIO1_S	**Real-time status of HVIO1 input**
		0 HVIO1 is Low
		1 HVIO1 is High
		Real-time information
8	HVIO2_S	**Real-time status of HVIO2 input**
		0 HVIO2 is Low
		1 HVIO2 is High
		Real-time information
9	WK1_S	**Real-time status of WAKE1 input**
		0 WAKE1 is Low
		1 WAKE1 is High
		Real-time information
10	WK2_S	**Real-time status of WAKE2 input**
		0 WAKE2 is Low
		1 WAKE2 is High
		Real-time information
12	INIT_S	**Real-time status of INIT mode**
		0 Device is Not in INIT mode
		1 Device is in INIT mode
		Real-time information
13	NORMAL_S	**Real-time status of Normal mode**
		0 Device is Not in Normal mode
		1 Device is in Normal mode
		Real-time information
14	LPON_S	**Real-time status of LPON mode**
		0 Device is Not in LPON mode
		1 Device is in LPON mode

Table 81. M_STATUS register bit description*...continued*

Bit	Symbol	Description
		Real-time information
15	V1TWARN_S	**Real-time status of V1 temperature**
		0 V1 temperature is < TWARNV1
		1 V1 temperature is > TWARNV1
		Real-time information

22.5 M_SYS_CFG

Table 82. M_SYS_CFG register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	-	-	-	-	-	LOCK_INIT	GO2INIT	GO2NORMAL
Read	0	BAT_FAIL	0	POR	0	LOCK_INIT	0	0
Reset	0	1	0	1	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	GO2LPON	GO2LPOFF	INT_TO_WUEN	INTB_REQ	INTB_DUR	-	MOD_CONF	MOD_EN
Read	0	0	INT_TO_WUEN	0	INTB_DUR	0	MOD_CONF	MOD_EN
Reset	0	0	0	0	0	0	OTP fuse	OTP fuse

Table 83. M_SYS_CFG register bit description

Bit	Symbol	Description
0	MOD_EN	**Enable the Frequency Spread Spectrum**
		0 Spread spectrum is disabled
		1 Spread spectrum is enabled
		OTP Fuse load
1	MOD_CONF	**Select the Spread Spectrum Modulation type**
		0 Triangular modulation is selected
		1 Pseudo random modulation is selected
		OTP Fuse load
3	INTB_DUR	**Select INTB pulse duration**
		0 INTB pulse = 25us
		1 INTB pulse = 100us
		POR
4	INTB_REQ	**Request INTB pulse**
		0 No effect
		1 INTB pulse is requested
		POR, or Self-clear
5	INT_TO_WUEN	**Enable Interrupt Time Out wake-up capability**
		0 Interrupt Time Out wake up capability is disabled
		1 Interrupt Time Out wake up capability is enabled
		POR
6	GO2LPOFF	**Request to go in LPOFF mode from Normal mode**
		0 No action
		1 Go to LPOFF mode
		POR, Self-clear

Table 83. M_SYS_CFG register bit description*...continued*

Bit	Symbol	Description
7	GO2LPON	**Request to go in LPON mode from Normal mode**
		0 No action
		1 Go to LPON mode
		POR, Self-clear
8	GO2NORMAL	**Request to go in Normal mode from LPON mode**
		0 No action
		1 Go to Normal mode
		POR, Self-clear
9	GO2INIT	**Request to go in INIT phase**
		0 No action
		1 Go to INIT phase
		POR, Self-clear
10	LOCK_INIT	**Lock the device in INIT phase**
		0 Exit INIT phase is possible
		1 Device locked in INIT phase
		POR
12	POR	**Report a POR of the digital POR = VBOS_POR or VDIG_UV_POR or VDIG_OV_POR or SOFTPOR_REQ**
		0 No POR event
		1 Digital POR event occurred
		POR
14	BAT_FAIL	**Report battery failure event (not reset by SOFTPOR_REQ) BAT_FAIL = VBOS_POR or VDIG_UV_POR or VDIG_OV_POR**
		0 No battery failure event
		1 Battery failure event occurred
		HARD_POR

22.6 M_SYS1_CFG

Table 84. M_SYS1_CFG register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	-	-	-	VBOS2 V1_SW_ ALWAYS_EN	-	LOAD_ OTP_BYP	SLOT_BYP	TSLOT_ DOWN_ CFG
Read	0	0	0	VBOS2 V1_SW_ ALWAYS_EN	0	LOAD_ OTP_BYP	SLOT_BYP	TSLOT_ DOWN_ CFG
Reset	0	0	0	OTP fuse	0	0	OTP fuse	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	-	SOFTPOR_ REQ	-	DBG_EXIT	-	-	OTP_EXIT	-
Read	0	0	0	0	DBG_ MODE	0	0	OTP_ MODE
Reset	0	0	0	0	0	0	0	0

Table 85. M_SYS1_CFG register bit description

Bit	Symbol	Description
0	OTP_MODE	**Real-time status of OTP mode**
		0 Device is not in OTP mode
		1 Device is in OTP mode
		Real-time information
1	OTP_EXIT	**Exit OTP mode**
		0 No action
		1 Exit OTP mode
		POR, Self-clear
3	DBG_MODE	**Real-time status of Debug mode**
		0 Device is not in Debug mode
		1 Device is in Debug mode
		Real-time information
4	DBG_EXIT	**Exit DEBUG mode**
		0 No action
		1 Exit DEBUG mode
		POR, Self-clear
6	SOFTPOR_REQ	**Request a Software POR of FS23 (reset the digital and restart from POR)**
		0 No action
		1 Software POR is requested
		POR, Self-clear

Table 85. M_SYS1_CFG register bit description...*continued*

Bit	Symbol	Description
8	TSLOT_DOWN_CFG	**Select the power down Time Slot**
		0 TSLOT = 2ms
		1 TSLOT = 0ms
		POR
9	SLOT_BYP	**Bypass the power sequence Slot 1 and Slot 2 after wake-up from LPON**
		0 Slot 1 and Slot 2 are not bypassed
		1 Slot 1 and Slot 2 are bypassed during power up
		OTP Fuse load
10	LOAD_OTP_BYP	**Bypass the OTP loading during power up**
		0 OTP loading is not bypassed
		1 OTP loading is bypassed
		POR or in main FSM M4 state
12	VBOS2V1_SW_ ALWAYS_EN	**Control VBOS to V1 switch in Normal and LPON modes when V1 = BUCK (the switch is kept open when V1 = LDO)**
		0 VBOS to V1 switch is open in Normal mode
		1 VBOS to V1 switch is closed in Normal and LPON mode (possible only when V1 = 5V in Normal mode)
		OTP Fuse load

22.7 M_REG_CTRL

Table 86. M_REG_CTRL register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	-	-	-	BUCK_SRHSOFF		BUCK_SRHSON		
Read	0	0	0	BUCK_SRHSOFF		BUCK_SRHSON		
Reset	0	0	0	OTP fuse		OTP fuse		
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	-	-	V2ON_LPON	V2EN	V2DIS	V3ON_LPON	V3EN	V3DIS
Read	0	0	V2ON_LPON	0	0	V3ON_LPON	0	0
Reset	0	0	0	0	0	0	0	0

Table 87. M_REG_CTRL register bit description

Bit	Symbol	Description
0	V3DIS	**Request to disable V3**
		0 No effect (Regulator remain in its current state)
		1 Request to disable V3
		POR, Self-clear
1	V3EN	**Request to enable V3**
		0 No effect (Regulator remain in its current state)
		1 Request to enable V3

Table 87. M_REG_CTRL register bit description...*continued*

Bit	Symbol	Description
		POR, Self-clear
2	V3ON_LPON	**Configure V3 state in LPON mode**
		0 Follow the power down slot configuration
		1 Keep V3 ON in LPON if V3 was already ON in NORMAL mode
		POR
3	V2DIS	**Request to disable V2**
		0 No effect (Regulator remain in its current state)
		1 Request to disable V2
		POR, Self-clear
4	V2EN	**Request to enable V2**
		0 No effect (Regulator remain in its current state)
		1 Request to enable V2
		POR, Self-clear
5	V2ON_LPON	**Configure V2 state in LPON mode**
		0 Follow the power down slot configuration
		1 Keep V2 ON in LPON if V2 was already ON in NORMAL mode
		POR
8 to 10	BUCK_SRHSON	**Select BUCK slew rate when the High Side turns ON**
		000 HS rising slew rate is 20 ns
		001 HS rising slew rate is 20 ns
		010 HS rising slew rate is 15 ns
		011 HS rising slew rate is 10 ns
		100 HS rising slew rate is 6.3 ns
		101 HS rising slew rate is 5 ns
		110 HS rising slew rate is 3 ns
		111 HS rising slew rate is 2 ns
		OTP Fuse load
11 to 12	BUCK_SRHSOFF	**Select BUCK slew rate when the High Side turns OFF**
		00 HS falling slew rate is 20 ns
		01 HS falling slew rate is 15 ns
		10 HS falling slew rate is 10 ns
		11 HS falling slew rate is 5 ns
		OTP Fuse load

22.8 M_REG_FLG

Table 88. M_REG_FLG register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	-	-	-	-	-	-	-	-
Read	V0UV_I	V0OV_I	V1TWARN_I	V1TSD_I	V2TSD_I	V3TSD_I	V2OL_I	V1UV_I
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	-	-	-	-	-	-	-	-
Read	V2UV_I	V3UV_I	V1OV_I	V2OV_I	V3OV_I	V1OC_I	V2OC_I	V3OC_I
Reset	0	0	0	0	0	0	0	0

Table 89. M_REG_FLG register bit description

Bit	Symbol	Description
0	V3OC_I	**Report V3 overcurrent event**
		0 No event detected
		1 V3 OC occurred
		POR, or Clear on Write (write '1')
1	V2OC_I	**Report V2 overcurrent event**
		0 No event detected
		1 V2 OC occurred
		POR, or Clear on Write (write '1')
2	V1OC_I	**Report V1 overcurrent event**
		0 No event detected
		1 V1 OC occurred
		POR, or Clear on Write (write '1')
3	V3OV_I	**Report V3 overvoltage event**
		0 No event detected
		1 V3 OV occurred
		POR, or Clear on Write (write '1')
4	V2OV_I	**Report V2 overvoltage event**
		0 No event detected
		1 V2 OV occurred
		POR, or Clear on Write (write '1')
5	V1OV_I	**Report V1 overvoltage event**
		0 No event detected
		1 V1 OV occurred
		POR, or Clear on Write (write '1')
6	V3UV_I	**Report V3 undervoltage event**
		0 No event detected
		1 V3 UV occurred
		POR, or Clear on Write (write '1')
7	V2UV_I	**Report V2 undervoltage event**
		0 No event detected
		1 V2 UV occurred
		POR, or Clear on Write (write '1')
8	V1UV_I	**Report V1 undervoltage event**
		0 No event detected
		1 V1 UV occurred
		POR, or Clear on Write (write '1')
9	V2OL_I	**Report V2 open loop event**
		0 No event detected
		1 V2 OL occurred
		POR, or Clear on Write (write '1')
10	V3TSD_I	**Report V3 Thermal Shutdown event**
		0 No event detected
		1 V3 TSD occurred
		POR, or clear on Write(write '1')
11	V2TSD_I	**Report V2 Thermal Shutdown event**

Table 89. M_REG_FLG register bit description*...continued*

Bit	Symbol	Description
		0 No event detected
		1 V2 TSD occurred
		POR, or clear on Write(write '1')
12	V1TSD_I	**Report V1 Thermal Shutdown event**
		0 No event detected
		1 V1 TSD occurred
		POR, or clear on Write(write '1')
13	V1TWARN_I	**Report V1 Temperature Warning event**
		0 No event detected
		1 die V1 TWARN occurred
		POR, or clear on Write(write '1')
14	V0OV_I	**Report VMON_EXT overvoltage event**
		0 No event detected
		1 VMON_EXT OV occurred
		POR, or Clear on Write (write '1')
15	V0UV_I	**Report VMON_EXT undervoltage event**
		0 No event detected
		1 VMON_EXT UV occurred
		POR, or Clear on Write (write '1')

22.9 M_REG_MSK

Table 90. M_REG_MSK register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	V0UV_M	V0OV_M	V1TWARN_M	V1TSD_M	V2TSD_M	V3TSD_M	V2OL_M	V1UV_M
Read	V0UV_M	V0OV_M	V1TWARN_M	V1TSD_M	V2TSD_M	V3TSD_M	V2OL_M	V1UV_M
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	V2UV_M	V3UV_M	V1OV_M	V2OV_M	V3OV_M	V1OC_M	V2OC_M	V3OC_M
Read	V2UV_M	V3UV_M	V1OV_M	V2OV_M	V3OV_M	V1OC_M	V2OC_M	V3OC_M
Reset	0	0	0	0	0	0	0	0

Table 91. M_REG_MSK register bit description

Bit	Symbol	Description
0	V3OC_M	**Inhibit V3 overcurrent interrupt**
		0 Interrupt is Not Inhibited
		1 Interrupt is Inhibited
		POR
1	V2OC_M	**Inhibit V2 overcurrent interrupt**
		0 Interrupt is Not Inhibited
		1 Interrupt is Inhibited
		POR
2	V1OC_M	**Inhibit V1 overcurrent interrupt**
		0 Interrupt is Not Inhibited

Table 91. M_REG_MSK register bit description*...continued*

Bit	Symbol	Description
		1 Interrupt is Inhibited
		POR
3	V3OV_M	**Inhibit V3 overvoltage interrupt**
		0 Interrupt is Not Inhibited
		1 Interrupt is Inhibited
		POR
4	V2OV_M	**Inhibit V2 overvoltage interrupt**
		0 Interrupt is Not Inhibited
		1 Interrupt is Inhibited
		POR
5	V1OV_M	**Inhibit V1 overvoltage interrupt**
		0 Interrupt is Not Inhibited
		1 Interrupt is Inhibited
		POR
6	V3UV_M	**Inhibit V3 undervoltage interrupt**
		0 Interrupt is Not Inhibited
		1 Interrupt is Inhibited
		POR
7	V2UV_M	**Inhibit V2 undervoltage interrupt**
		0 Interrupt is Not Inhibited
		1 Interrupt is Inhibited
		POR
8	V1UV_M	**Inhibit V1 undervoltage interrupt**
		0 Interrupt is Not Inhibited
		1 Interrupt is Inhibited
		POR
9	V2OL_M	**Inhibit V2 Open Load interrupt**
		0 Interrupt is Not Inhibited
		1 Interrupt is Inhibited
		POR
10	V3TSD_M	**Inhibit V3 Thermal Shutdown interrupt**
		0 Interrupt is Not Inhibited
		1 Interrupt is Inhibited
		POR
11	V2TSD_M	**Inhibit V2 Thermal Shutdown interrupt**
		0 Interrupt is Not Inhibited
		1 Interrupt is Inhibited
		POR
12	V1TSD_M	**Inhibit V1 Thermal Shutdown interrupt**
		0 Interrupt is Not Inhibited
		1 Interrupt is Inhibited
		POR
13	V1TWARN_M	**Inhibit V1 Thermal Warning interrupt**
		0 Interrupt is Not Inhibited
		1 Interrupt is Inhibited

Table 91. M_REG_MSK register bit description*...continued*

Bit	Symbol	Description
		POR
14	V0OV_M	**Inhibit VMON_EXT overvoltage interrupt**
		0 Interrupt is Not Inhibited
		1 Interrupt is Inhibited
		POR
15	V0UV_M	**Inhibit VMON_EXT undervoltage interrupt**
		0 Interrupt is Not Inhibited
		1 Interrupt is Inhibited
		POR

22.10 M_REG1_FLG

Table 92. M_REG1_FLG register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	-	-	-	-	-	-	-	-
Read	-	-	-	-	-	-	-	-
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	-	-	-	-	-	-	-	-
Read	-	-	-	-	-	-	-	V1_OCLS_I
Reset	0	0	0	0	0	0	0	0

Table 93. M_REG1_FLG register bit description

Bit	Symbol	Description
0	V1_OCLS_I	**Report V1 low side FET Over Current event (HVBUCK)**
		0 No event detected
		1 V1 low side OC occurred
		POR, or Clear on Write (write '1')

22.11 M_REG1_MSK

Table 94. M_REG1_MSK register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	-	-	-	-	-	-	-	-
Read	-	-	-	-	-	-	-	-
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	-	-	-	-	-	-	-	V1_OCLS_M
Read	-	-	-	-	-	-	-	V1_OCLS_M
Reset	0	0	0	0	0	0	0	0

Table 95. M_REG1_MSK register bit description

Bit	Symbol	Description
0	V1_OCLS_M	**Inhibit V1 low side Over Current interrupt**
		0 Interrupt is Not Inhibited
		1 Interrupt is Inhibited
		POR

22.12 M_IO_CTRL

Table 96. M_IO_CTRL register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	-	-	-	-	-	-	HVIO1HI	HVIO1LO
Read	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	HVIO2HI	HVIO2LO	LVIO3HI	LVIO3LO	LVIO4HI	LVIO4LO	LVO6HI	LVO6LO
Read	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0

Table 97. M_IO_CTRL register bit description

Bit	Symbol	Description
0	LVO6LO	**Request to assert LVO6 when configured as an output**
		0 No effect (IO remain in its current state)
		1 Request to assert LVO6 low
		POR, Self-clear
1	LVO6HI	**Request to release LVO6 when configured as an output**
		0 No effect (IO remain in its current state)
		1 Request to release LVO6 high
		POR, Self-clear
2	LVIO4LO	**Request to assert LVIO4 when configured as an output**
		0 No effect (IO remain in its current state)
		1 Request to assert LVIO4 low
		POR, Self-clear
3	LVIO4HI	**Request to release LVIO4 when configured as an output**
		0 No effect (IO remain in its current state)
		1 Request to release LVIO4 high
		POR, Self-clear
4	LVIO3LO	**Request to assert LVIO3 when configured as an output**
		0 No effect (IO remain in its current state)
		1 Request to assert LVIO3 low
		POR, Self-clear
5	LVIO3HI	**Request to release LVIO3 when configured as an output**
		0 No effect (IO remain in its current state)
		1 Request to release LVIO3 high
		POR, Self-clear
6	HVIO2LO	**Request to assert HVIO2 when configured as an output**

Table 97. M_IO_CTRL register bit description...*continued*

Bit	Symbol	Description
		0 No effect (IO remain in its current state)
		1 Request to assert HVIO2 low
		POR, Self-clear
7	HVIO2HI	**Request to release HVIO2 when configured as an output**
		0 No effect (IO remain in its current state)
		1 Request to release HVIO2 high
		POR, Self-clear
8	HVIO1LO	**Request to assert HVIO1 when configured as an output**
		0 No effect (IO remain in its current state)
		1 Request to assert HVIO1 low
		POR, Self-clear
9	HVIO1HI	**Request to release HVIO1 when configured as an output**
		0 No effect (IO remain in its current state)
		1 Request to release HVIO1 high
		POR, Self-clear

22.13 M_IO_TIMER_FLG

Table 98. M_IO_TIMER_FLG register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	-	-	-	-	-	-	-	-
Read	0	0	0	0	0	0	0	LDT_I
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	-	-	-	-	-	-	-	-
Read	LVI5_I	LVIO4_I	LVIO3_I	HVIO2_I	HVIO1_I	0	WK2_I	WK1_I
Reset	0	0	0	0	0	0	0	0

Table 99. M_IO_TIMER_FLG register bit description

Bit	Symbol	Description
0	WK1_I	**Report WAKE1 input state change event if not masked**
		0 No event on WAKE1
		1 Event on WAKE1 occurred
		POR, or Clear on Write (write '1')
1	WK2_I	**Report WAKE2 input state change event if not masked**
		0 No event on WAKE2
		1 Event on WAKE2 occurred
		POR, or Clear on Write (write '1')
3	HVIO1_I	**Report HVIO1 input state change event if not masked**
		0 No event on HVIO1
		1 Event on HVIO1 occurred
		POR, or Clear on Write (write '1')
4	HVIO2_I	**Report HVIO2 input state change event if not masked**
		0 No event on HVIO2

Table 99. M_IO_TIMER_FLG register bit description*...continued*

Bit	Symbol	Description
		1 Event on HVIO2 occurred
		POR, or Clear on Write (write '1')
5	LVIO3_I	**Report LVIO3 input state change event if not masked**
		0 No event on LVIO3
		1 Event on LVIO3 occurred
		POR, or Clear on Write (write '1')
6	LVIO4_I	**Report LVIO4 input state change event if not masked**
		0 No event on LVIO4
		1 Event on LVIO4 occurred
		POR, or Clear on Write (write '1')
7	LVI5_I	**Report LVI5 input state change event if not masked**
		0 No event on LVI5
		1 Event on LVI5 occurred
		POR, or Clear on Write (write '1')
8	LDT_I	**Report LDT event**
		0 No event on LDT
		1 Event on LDT occurred
		POR, or Clear on Write (write '1')

22.14 M_IO_TIMER_MSK

Table 100. M_IO_TIMER_MSK register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	-	-	-	-	-	-	-	LDT_M
Read	0	0	0	0	0	0	0	LDT_M
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	LVI5_M	LVIO4_M	LVIO3_M	HVIO2_M	HVIO1_M	-	WK2_M	WK1_M
Read	LVI5_M	LVIO4_M	LVIO3_M	HVIO2_M	HVIO1_M	0	WK2_M	WK1_M
Reset	0	0	0	0	0	0	0	0

Table 101. M_IO_TIMER_MSK register bit description

Bit	Symbol	Description
0	WK1_M	**Inhibit WAKE1 input state change interrupt**
		0 Interrupt is Not Inhibited in Normal mode
		1 Interrupt is always Inhibited
		POR
1	WK2_M	**Inhibit WAKE2 input state change interrupt**
		0 Interrupt is Not Inhibited in Normal mode
		1 Interrupt is always Inhibited
		POR
3	HVIO1_M	**Inhibit HVIO1 input state change interrupt**
		0 Interrupt is Not Inhibited in Normal mode
		1 Interrupt is always Inhibited

Table 101. M_IO_TIMER_MSK register bit description *...continued*

Bit	Symbol	Description
		POR
4	HVIO2_M	**Inhibit HVIO2 input state change interrupt**
		0 Interrupt is Not Inhibited in Normal mode
		1 Interrupt is always Inhibited
		POR
5	LVIO3_M	**Inhibit LVIO3 input state change interrupt**
		0 Interrupt is Not Inhibited in Normal mode
		1 Interrupt is always Inhibited
		POR
6	LVIO4_M	**Inhibit LVIO4 input state change interrupt**
		0 Interrupt is Not Inhibited in Normal mode
		1 Interrupt is always Inhibited
		POR
7	LVI5_M	**Inhibit LVI5 input state change interrupt**
		0 Interrupt is Not Inhibited in Normal mode
		1 Interrupt is always Inhibited
		POR
8	LDT_M	**Inhibit LDT event interrupt**
		0 Interrupt is Not Inhibited
		1 Interrupt is always Inhibited
		POR

22.15 M_VSUP_COM_FLG

Table 102. M_VSUP_COM_FLG register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	-	-	-	-	-	-	-	-
Read	0	0	0	VBOS2V1SW_S	VBOS_UV	0	I2C_CRC_I	I2C_REQ_I
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	-	-	-	-	-	-	-	-
Read	SPI_CRC_I	SPI_CLK_I	SPI_REQ_I	0	VSHS_OV_I	VSHS_UV_I	VSUP_OV_I	VSUP_UV_I
Reset	0	0	0	0	0	0	0	0

Table 103. M_VSUP_COM_FLG register bit description

Bit	Symbol	Description
0	VSUP_UV_I	**Report VSUP UV event**
		0 No VSUP undervoltage event
		1 VSUP undervoltage event occurred
		POR, or clear on Write(write '1')
1	VSUP_OV_I	**Report VSUP OV event**
		0 No VSUP overvoltage event
		1 VSUP overvoltage event occurred
		POR, or clear on Write(write '1')

Table 103. M_VSUP_COM_FLG register bit description*...continued*

Bit	Symbol	Description
2	VSHS_UV_I	**Report VSHS undervoltage event**
		0 No VSHS undervoltage event
		1 VSHS undervoltage event occurred
		POR, or clear on Write(write '1')
3	VSHS_OV_I	**Report VSHS overvoltage event**
		0 No VSHS overvoltage event
		1 VSHS undervoltage event occurred
		POR, or clear on Write(write '1')
5	SPI_REQ_I	**Report SPI request error due to writing or reading in an invalid register**
		0 No error
		1 SPI request error reported
		POR, or Clear on Write(write'1)
6	SPI_CLK_I	**Report SPI clock error due to wrong number of clock pulses**
		0 No error
		1 SPI clock error reported
		POR, or Clear on Write(write'1)
7	SPI_CRC_I	**Report SPI CRC error due to incorrect CRC calculation**
		0 No error
		1 SPI CRC error reported
		POR, or Clear on Write(write'1)
8	I2C_REQ_I	**Report I2C request error due to writing or reading in an invalid register**
		0 No error
		1 I2C request error reported
		POR, or Clear on Write(write'1)
9	I2C_CRC_I	**Report I2C CRC error due to incorrect CRC calculation**
		0 No error
		1 I2C CRC error reported
		POR, or Clear on Write(write'1)
11	VBOS_UV	**Report VBOS undervoltage event**
		0 No event detected
		1 VBOS UV occurred
		POR, or Clear on Write(write'1)
12	VBOS2V1SW_S	**Real-time status of the switch between VBOS and V1**
		0 The switch is opened
		1 The switch is closed
		Real-time information

22.16 M_VSUP_COM_MSK

Table 104. M_VSUP_COM_MSK register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	-	-	-	-	-	-	I2C_CRC_M	I2C_REQ_M
Read	0	0	0	0	0	0	I2C_CRC_M	I2C_REQ_M
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**

Table 104. M_VSUP_COM_MSK register bit allocation*...continued*

Bit	15	14	13	12	11	10	9	8
Write	SPI_CRC_M	SPI_CLK_M	SPI_REQ_M	-	VSHS_OV_M	VSHS_UV_M	VSUP_OV_M	VSUP_UV_M
Read	SPI_CRC_M	SPI_CLK_M	SPI_REQ_M	0	VSHS_OV_M	VSHS_UV_M	VSUP_OV_M	VSUP_UV_M
Reset	0	0	0	0	0	0	0	0

Table 105. M_VSUP_COM_MSK register bit description

Bit	Symbol	Description
0	VSUP_UV_M	**Inhibit VSUP_UV Interrupt**
		0 Interrupt is Not Inhibited
		1 Interrupt is Inhibited
		POR
1	VSUP_OV_M	**Inhibit VSUP_OV Interrupt**
		0 Interrupt is Not Inhibited
		1 Interrupt is Inhibited
		POR
2	VSHS_UV_M	**Inhibit VSHS_UV Interrupt**
		0 Interrupt is Not Inhibited
		1 Interrupt is Inhibited
		POR
3	VSHS_OV_M	**Inhibit VSHS_OV Interrupt**
		0 Interrupt is Not Inhibited
		1 Interrupt is Inhibited
		POR
5	SPI_REQ_M	**Inhibit SPI request error Interrupt**
		0 Interrupt is Not Inhibited
		1 Interrupt is Inhibited
		POR
6	SPI_CLK_M	**Inhibit SPI clock error Interrupt**
		0 Interrupt is Not Inhibited
		1 Interrupt is Inhibited
		POR
7	SPI_CRC_M	**Inhibit SPI CRC error Interrupt**
		0 Interrupt is Not Inhibited
		1 Interrupt is Inhibited
		POR
8	I2C_REQ_M	**Inhibit I2C request error Interrupt**
		0 Interrupt is Not Inhibited
		1 Interrupt is Inhibited
		POR
9	I2C_CRC_M	**Inhibit I2C CRC error Interrupt**
		0 Interrupt is Not Inhibited
		1 Interrupt is Inhibited
		POR

22.17 M_IOWU_CFG

Table 106. M_IOWU_CFG register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	LVI5_WUCFG	LVIO4_WUCFG	LVIO3_WUCFG	-	HVIO2_DGLT	HVIO1_DGLT	WK2_DGLT	WK1_DGLT
Read	LVI5_WUCFG	LVIO4_WUCFG	LVIO3_WUCFG	0	HVIO2_DGLT	HVIO1_DGLT	WK2_DGLT	WK1_DGLT
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	HVIO2_WUCFG		HVIO1_WUCFG		WK2_WUCFG		WK1_WUCFG	
Read	HVIO2_WUCFG		HVIO1_WUCFG		WK2_WUCFG		WK1_WUCFG	
Reset	0	0	0	0	0	1	0	1

Table 107. M_IOWU_CFG register bit description

Bit	Symbol	Description
0 to 1	WK1_WUCFG	**Configure WAKE1 wake-up polarity**
		00 Input comparator disabled in LP modes only (no consumption)
		01 High level wake up is configured
		10 Low level wake up is configured
		11 Cyclic sense wake up is configured
		POR
2 to 3	WK2_WUCFG	**Configure WAKE2 wake-up polarity**
		00 Input comparator disabled in LP modes only (no consumption)
		01 High level wake up is configured
		10 Low level wake up is configured
		11 Cyclic sense wake up is configured
		POR
4 to 5	HVIO1_WUCFG	**Configure HVIO1 wake-up polarity**
		00 Input comparator disabled in LP modes only (no consumption)
		01 High level wake up is configured
		10 Low level wake up is configured
		11 Cyclic sense wake up is configured
		POR
6 to 7	HVIO2_WUCFG	**Configure HVIO2 wake-up polarity**
		00 Input comparator disabled in LP modes only (no consumption)
		01 High level wake up is configured
		10 Low level wake up is configured
		11 Cyclic sense wake up is configured
		POR
8	WK1_DGLT	**Configure WAKE1 deglitcher time**
		0 WAKE1 deglitcher = 15 us
		1 WAKE1 deglitcher = 65 us
		POR, Write
9	WK2_DGLT	**Configure WAKE2 deglitcher time**
		0 WAKE2 deglitcher = 15 us
		1 WAKE2 deglitcher = 65 us
		POR, Write

Table 107. M_IOWU_CFG register bit description...*continued*

Bit	Symbol	Description
10	HVIO1_DGLT	**Configure HVIO1 deglitcher time**
		0 HVIO1 deglitcher = 15 us
		1 HVIO1 deglitcher = 65 us
		POR, Write
11	HVIO2_DGLT	**Configure HVIO2 deglitcher time**
		0 HVIO2 deglitcher = 15 us
		1 HVIO2 deglitcher = 65 us
		POR, Write
13	LVIO3_WUCFG	**Configure LVIO3 wake-up polarity**
		0 High level wake up is configured
		1 Low level wake up is configured
		POR
14	LVIO4_WUCFG	**Configure LVIO4 wake-up polarity**
		0 High level wake up is configured
		1 Low level wake up is configured
		POR
15	LVI5_WUCFG	**Configure LVI5 wake-up polarity**
		0 High level wake up is configured
		1 Low level wake up is configured
		POR

22.18 M_IOWU_EN

Table 108. M_IOWU_EN register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	-	-	LVI5_WUEN		LVIO4_WUEN		LVIO3_WUEN	
Read	0	0	LVI5_WUEN		LVIO4_WUEN		LVIO3_WUEN	
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	HVIO2_WUEN		HVIO1_WUEN		WK2_WUEN		WK1_WUEN	
Read	HVIO2_WUEN		HVIO1_WUEN		WK2_WUEN		WK1_WUEN	
Reset	1	1	1	1	1	1	1	1

Table 109. M_IOWU_EN register bit description

Bit	Symbol	Description
0 to 1	WK1_WUEN	**Configure WAKE1 wake up and interrupt capability**
		00 No wake up and no interrupt
		01 Wake up only
		10 Interrupt only
		11 Wake up and interrupt
		POR or Fail-Safe state
2 to 3	WK2_WUEN	**Configure WAKE2 wake up and interrupt capability**
		00 No wake up and no interrupt
		01 Wake up only

Table 109. M_IOWU_EN register bit description*...continued*

Bit	Symbol	Description
		10 Interrupt only
		11 Wake up and interrupt
		POR or Fail-Safe state
4 to 5	HVIO1_WUEN	**Configure HVIO1 wake up and interrupt capability**
		00 No wake up and no interrupt
		01 Wake up only
		10 Interrupt only
		11 Wake up and interrupt
		POR or Fail-Safe state
6 to 7	HVIO2_WUEN	**Configure HVIO2 wake up and interrupt capability**
		00 No wake up and no interrupt
		01 Wake up only
		10 Interrupt only
		11 Wake up and interrupt
		POR or Fail-Safe state
8 to 9	LVIO3_WUEN	**Configure LVIO3 wake up and interrupt capability**
		00 No wake up and no interrupt
		01 Wake up only
		10 Interrupt only
		11 Wake up and interrupt
		POR
10 to 11	LVIO4_WUEN	**Configure LVIO4 wake up and interrupt capability**
		00 No wake up and no interrupt
		01 Wake up only
		10 Interrupt only
		11 Wake up and interrupt
		POR
12 to 13	LVI5_WUEN	**Configure LVI5 wake up and interrupt capability**
		00 No wake up and no interrupt
		01 Wake up only
		10 Interrupt only
		11 Wake up and interrupt
		POR

22.19 M_IOWU_FLG

Table 110. M_IOWU_FLG register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	-	-	-	-	-	-	-	-
Read	LVI5_WU_I	LVIO4_WU_I	LVIO3_WU_I	0	HVIO2_ CYS_RDY	HVIO1_ CYS_RDY	HVIO2_CYC_S	HVIO1_CYC_S
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	-	-	-	-	-	-	-	-
Read	HVIO2_WU_I	HVIO1_WU_I	WK2_ CYS_RDY	WK1_ CYS_RDY	WK2_CYC_S	WK1_CYC_S	WK2_WU_I	WK1_WU_I

Table 110. M_IOWU_FLG register bit allocation*...continued*

Bit	15	14	13	12	11	10	9	8
Reset	0	0	0	0	0	0	0	0

Table 111. M_IOWU_FLG register bit description

Bit	Symbol	Description
0	WK1_WU_I	**Report WAKE1 wake-up event**
		0 No wake up by WAKE1 (level) or WAKE1 pin state did not change between two trigger event (cyclic sense)
		1 Wake up by WAKE1 occurred (level) or WAKE1 pin state changed between two trigger event (cyclic sense)
		POR or Fail-safe or Clear on Write (write '1)
1	WK2_WU_I	**Report WAKE2 wake-up event**
		0 No wake up by WAKE2 (level) or WAKE2 pin state did not change between two trigger event (cyclic sense)
		1 Wake up by WAKE2 occurred (level) or WAKE2 pin state changed between two trigger event (cyclic sense)
		POR or Fail-safe or Clear on Write (write '1)
2	WK1_CYC_S	**Report WAKE1 state at trigger point**
		0 State at trigger point captured at 0
		1 State at trigger point captured at 1
		POR, or each trigger point
3	WK2_CYC_S	**Report WAKE2 state at trigger point**
		0 State at trigger point captured at 0
		1 State at trigger point captured at 1
		POR, or each trigger point
4	WK1_CYS_RDY	**Report WAKE1 readiness for cyclic sense**
		0 Cyclic sense not ready
		1 Cyclic sense ready
		POR
5	WK2_CYS_RDY	**Report WAKE2 readiness for cyclic sense**
		0 Cyclic sense not ready
		1 Cyclic sense ready
		POR
6	HVIO1_WU_I	**Report HVIO1 wake up event**
		0 No wake up by HVIO1 (level) or HVIO1 pin state did not change between two trigger event (cyclic sense)
		1 Wake up by HVIO1 occurred (level) or HVIO1 pin state changed between two trigger event (cyclic sense)
		POR or Fail-safe or Clear on Write (write '1)
7	HVIO2_WU_I	**Report HVIO2 wake up event**
		0 No wake up by HVIO2 (level) or HVIO2 pin state did not change between two trigger event (cyclic sense)
		1 Wake up by HVIO2 occurred (level) or HVIO2 pin state changed between two trigger event (cyclic sense)
		POR or Fail-safe or Clear on Write (write '1)
8	HVIO1_CYC_S	**Report HVIO1 state at trigger point**
		0 State at trigger point captured at 0
		1 State at trigger point captured at 1
		POR, or each trigger point
9	HVIO2_CYC_S	**Report HVIO2 state at trigger point**
		0 State at trigger point captured at 0
		1 State at trigger point captured at 1
		POR, or each trigger point

Table 111. M_IOWU_FLG register bit description*...continued*

Bit	Symbol	Description
10	HVIO1_CYS_RDY	**Report HVIO1 readiness for cyclic sense**
		0 Cyclic sense not ready
		1 Cyclic sense ready
		POR
11	HVIO2_CYS_RDY	**Report HVIO2 readiness for cyclic sense**
		0 Cyclic sense not ready
		1 Cyclic sense ready
		POR
13	LVIO3_WU_I	**Report LVIO3 wake up event (outside NORMAL mode)**
		0 no wake up by LVIO3
		1 wake up by LVIO3 occurred
		POR or Fail-safe or Clear on Write (write '1)
14	LVIO4_WU_I	**Report LVIO4 wake up event (outside NORMAL mode)**
		0 no wake up by LVIO4
		1 wake up by LVIO4 occurred
		POR or Fail-safe or Clear on Write (write '1)
15	LVI5_WU_I	**Report LVI5 wake up event (outside NORMAL mode)**
		0 no wake up by LVI5
		1 wake up by LVI5 occurred
		POR or Fail-safe or Clear on Write (write '1)

22.20 M_WU1_EN

Table 112. M_WU1_EN register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	-	-	-	-	-	-	-	-
Read	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	-	-	LDT_WUEN		LIN_WUEN		CAN_WUEN	
Read	0	0	LDT_WUEN		LIN_WUEN		CAN_WUEN	
Reset	0	0	0	0	1	1	1	1

Table 113. M_WU1_EN register bit description

Bit	Symbol	Description
0 to 1	CAN_WUEN	**Configure CAN wake up and interrupt capability**
		00 No wake up and no interrupt
		01 Wake up only
		10 Interrupt only
		11 Wake up and interrupt
		POR or Fail-Safe state
2 to 3	LIN_WUEN	**Configure LIN wake up and interrupt capability**
		00 No wake up and no interrupt
		01 Wake up only

Table 113. M_WU1_EN register bit description*...continued*

Bit	Symbol	Description
		10 Interrupt only
		11 Wake up and interrupt
		POR or Fail-Safe state
4 to 5	LDT_WUEN	**Configure LDT wake up and interrupt capability**
		00 No wake up and no interrupt
		01 Wake up only
		10 Interrupt only
		11 Wake up and interrupt
		POR

22.21 M_WU1_FLG

Table 114. M_WU1_FLG register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	-	-	-	-	-	-	-	-
Read	0	0	0	0	0	0	FS_EVT	EXT_ RSTB_WU
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	-	-	-	-	-	-	-	-
Read	WD_OFL_WU	V1_UVLP_WU	INT_TO_WU	GO2 NORMAL_WU	0	LDT_WU_I	LIN_WU_I	CAN_WU_I
Reset	0	0	0	0	0	0	0	0

Table 115. M_WU1_FLG register bit description

Bit	Symbol	Description
0	CAN_WU_I	**Report CAN wake up event**
		0 No wake up by CAN
		1 Wake up by CAN occurred
		POR or Fail-safe or Clear on Write (write '1)
1	LIN_WU_I	**Report LIN wake up event**
		0 No wake up by LIN
		1 Wake up by LIN occurred
		POR or Fail-safe or Clear on Write (write '1)
2	LDT_WU_I	**Report LDT wake up event**
		0 No wake up by LDT
		1 Wake up by LDT occurred
		POR or Fail-safe or Clear on Write (write '1)
4	GO2NORMAL_WU	**Report GO2NORMAL request from MCU wake up event**
		0 No wake up by MCU GO2NORMAL request
		1 Wake up by MCU GO2NORMAL request occurred
		POR or Fail-safe or Clear on Write (write '1)
5	INT_TO_WU	**Report Interrupt Time Out wake up event**
		0 No wake up by Interrupt Time Out
		1 Wake up by Interrupt Time Out occurred

Table 115. M_WU1_FLG register bit description*...continued*

Bit	Symbol	Description
		POR or Fail-safe or Clear on Write (write '1)
6	V1_UVLP_WU	**Report V1 LPON under voltage wake up event**
		0 No wake up by V1 LPON under voltage
		1 Wake up by V1 LPON under voltage occurred
		POR or Fail-safe or Clear on Write (write '1)
7	WD_OFL_WU	**Report Watchdog Max Error Failure wake up event**
		0 No wake up by Max Error Failure
		1 Wake up by Watchdog Max Error Failure occurred
		POR or Fail-safe or Clear on Write (write '1)
8	EXT_RSTB_WU	**Report RSTB assertion wake up event**
		0 No wake up by to RSTB assertion
		1 Wake up by to RSTB assertion occurred
		POR or Fail-safe or Clear on Write (write '1)
9	FS_EVT	**Report a Fail-Safe event**
		0 No Fail-Safe event
		1 Fail-Safe event occurred (FSM went to Fail-Safe state)
		POR or Fail-safe or Clear on Write (write '1)

22.22 M_TIMER1_CFG

Table 116. M_TIMER1_CFG register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	-	-	-	-	-	-	-	TIMER1_DLY
Read	0	0	0	0	0	0	0	TIMER1_DLY
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	TIMER1_DLY	TIMER1_ON				TIMER1_PER		
Read	TIMER1_DLY	TIMER1_ON				TIMER1_PER		
Reset	0	0	0	0	0	0	0	0

Table 117. M_TIMER1_CFG register bit description

Bit	Symbol	Description
0 to 2	TIMER1_PER	**Configure the TIMER1 period**
		000 TIMER1 period = 10.24 ms
		001 TIMER1 period = 20.48 ms
		010 TIMER1 period = 51.2 ms
		011 TIMER1 period = 102.4 ms
		100 TIMER1 period = 204.8 ms
		101 TIMER1 period = 512 ms
		110 TIMER1 period = 1024 ms
		111 TIMER1 period = 2048 ms
		POR
3 to 6	TIMER1_ON	**Configure the TIMER1 ON time**
		0000 TIMER1 ON time = 0 ms

Table 117. M_TIMER1_CFG register bit description*...continued*

Bit	Symbol	Description
		0001 TIMER1 ON time = 0.128 ms
		0010 TIMER1 ON time = 0.256 ms
		0011 TIMER1 ON time = 1.024 ms
		0100 TIMER1 ON time = 10.24 ms
		0101 TIMER1 ON time = 20.48 ms
		0110 TIMER1 ON time = 30.72 ms
		0111 TIMER1 ON time = 40.96 ms
		1000 TIMER1 ON time = 51.2 ms
		1001 TIMER1 ON time = 61.44 ms
		1010 TIMER1 ON time = 81.92 ms
		1011 TIMER1 ON time = 102.4 ms
		1100 TIMER1 ON time = 122.88 ms
		1101 TIMER1 ON time = 153.6 ms
		1110 TIMER1 ON time = 204.8 ms
		1111 TIMER1 ON time = Infinite
		POR
7 to 8	TIMER1_DLY	**Configure the TIMER1 delay time (apply on rising edge only)**
		00 TIMER1 delay = 0 us
		01 TIMER1 delay = 5 us
		10 TIMER1 delay = 10 us
		11 TIMER1 delay = 15 us
		POR

22.23 M_TIMER2_CFG

Table 118. M_TIMER2_CFG register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	-	-	-	-	-	-	-	TIMER2_DLY
Read	0	0	0	0	0	0	0	TIMER2_DLY
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	TIMER2_DLY	TIMER2_ON				TIMER2_PER		
Read	TIMER2_DLY	TIMER2_ON				TIMER2_PER		
Reset	0	0	0	0	0	0	0	0

Table 119. M_TIMER2_CFG register bit description

Bit	Symbol	Description
0 to 2	TIMER2_PER	**Configure the TIMER2 period**
		000 TIMER2 period = 10.24 ms
		001 TIMER2 period = 20.48 ms
		010 TIMER2 period = 51.2 ms
		011 TIMER2 period = 102.4 ms
		100 TIMER2 period = 204.8 ms
		101 TIMER2 period = 512 ms

Table 119. M_TIMER2_CFG register bit description*...continued*

Bit	Symbol	Description
		110 TIMER2 period = 1024 ms
		111 TIMER2 period = 2048 ms
		POR
3 to 6	TIMER2_ON	**Configure the TIMER2 ON time**
		0000 TIMER2 ON time = 0 ms
		0001 TIMER2 ON time = 0.128 ms
		0010 TIMER2 ON time = 0.256 ms
		0011 TIMER2 ON time = 1.024 ms
		0100 TIMER2 ON time = 10.24 ms
		0101 TIMER2 ON time = 20.48 ms
		0110 TIMER2 ON time = 30.72 ms
		0111 TIMER2 ON time = 40.96 ms
		1000 TIMER2 ON time = 51.2 ms
		1001 TIMER2 ON time = 61.44 ms
		1010 TIMER2 ON time = 81.92 ms
		1011 TIMER2 ON time = 102.4 ms
		1100 TIMER2 ON time = 122.88 ms
		1101 TIMER2 ON time = 153.6 ms
		1110 TIMER2 ON time = 204.8 ms
		1111 TIMER2 ON time = Infinite
		POR
7 to 8	TIMER2_DLY	**Configure the TIMER2 delay time (apply on rising edge only)**
		00 TIMER2 delay = 0 us
		01 TIMER2 delay = 5 us
		10 TIMER2 delay = 10 us
		11 TIMER2 delay = 15 us
		POR

22.24 M_TIMER3_CFG

Table 120. M_TIMER3_CFG register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	-	-	-	-	-	-	-	TIMER3_DLY
Read	0	0	0	0	0	0	0	TIMER3_DLY
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	TIMER3_DLY	TIMER3_ON				TIMER3_PER		
Read	TIMER3_DLY	TIMER3_ON				TIMER3_PER		
Reset	0	0	0	0	0	0	0	0

Table 121. M_TIMER3_CFG register bit description

Bit	Symbol	Description
0 to 2	TIMER3_PER	**Configure the TIMER3 period**
		000 TIMER3 period = 10.24 ms

Table 121. M_TIMER3_CFG register bit description...*continued*

Bit	Symbol	Description
		001 TIMER3 period = 20.48 ms
		010 TIMER3 period = 51.2 ms
		011 TIMER3 period = 102.4 ms
		100 TIMER3 period = 204.8 ms
		101 TIMER3 period = 512 ms
		110 TIMER3 period = 1024 ms
		111 TIMER3 period = 2048 ms
		POR
3 to 6	TIMER3_ON	**Configure the TIMER3 ON time**
		0000 TIMER3 ON time = 0 ms
		0001 TIMER3 ON time = 0.128 ms
		0010 TIMER3 ON time = 0.256 ms
		0011 TIMER3 ON time = 1.024 ms
		0100 TIMER3 ON time = 10.24 ms
		0101 TIMER3 ON time = 20.48 ms
		0110 TIMER3 ON time = 30.72 ms
		0111 TIMER3 ON time = 40.96 ms
		1000 TIMER3 ON time = 51.2 ms
		1001 TIMER3 ON time = 61.44 ms
		1010 TIMER3 ON time = 81.92 ms
		1011 TIMER3 ON time = 102.4 ms
		1100 TIMER3 ON time = 122.88 ms
		1101 TIMER3 ON time = 153.6 ms
		1110 TIMER3 ON time = 204.8 ms
		1111 TIMER3 ON time = Infinite
		POR
7 to 8	TIMER3_DLY	**Configure the TIMER3 delay time (apply on rising edge only)**
		00 TIMER3 delay = 0 us
		01 TIMER3 delay = 5 us
		10 TIMER3 delay = 10 us
		11 TIMER3 delay = 15 us
		POR

22.25 M_PWM1_CFG

Table 122. M_PWM1_CFG register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	-	-	-	PWM1_DLY		PWM1_F	PWM1_DC	
Read	0	0	0	PWM1_DLY		PWM1_F	PWM1_DC	
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	PWM1_DC							
Read	PWM1_DC							
Reset	0	0	0	0	0	0	0	0

Table 123. M_PWM1_CFG register bit description

Bit	Symbol	Description
0 to 9	PWM1_DC	**Configure the PWM1 duty cycle**
		PWM1 duty cycle = 100 * PWM1_DC / 1000
		POR
10	PWM1_F	**Configure the PWM1 frequency**
		0 PWM1 frequency = 200 Hz
		1 PWM1 frequency = 400 Hz
		POR
11 to 12	PWM1_DLY	**Configure the PWM1 delay time (applies on both edges)**
		00 PWM1 delay = 0 us
		01 PWM1 delay = 5 us
		10 PWM1 delay = 10 us
		11 PWM1 delay = 15 us
		POR

22.26 M_PWM2_CFG

Table 124. M_PWM2_CFG register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	-	-	-	PWM2_DLY		PWM2_F	PWM2_DC	
Read	0	0	0	PWM2_DLY		PWM2_F	PWM2_DC	
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	PWM2_DC							
Read	PWM2_DC							
Reset	0	0	0	0	0	0	0	0

Table 125. M_PWM2_CFG register bit description

Bit	Symbol	Description
0 to 9	PWM2_DC	**Configure the PWM2 duty cycle**
		PWM2 duty cycle = 100 * PWM2_DC / 1000
		POR
10	PWM2_F	**Configure the PWM2 frequency**
		0 PWM2 frequency = 200 Hz
		1 PWM2 frequency = 400 Hz
		POR
11 to 12	PWM2_DLY	**Configure the PWM2 delay time (applies on both edges)**
		00 PWM2 delay = 0 us
		01 PWM2 delay = 5 us
		10 PWM2 delay = 10 us
		11 PWM2 delay = 15 us
		POR

22.27 M_PWM3_CFG

Table 126. M_PWM3_CFG register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	-	-	-	PWM3_DLY		PWM3_F	PWM3_DC	
Read	0	0	0	PWM3_DLY		PWM3_F	PWM3_DC	
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	PWM3_DC							
Read	PWM3_DC							
Reset	0	0	0	0	0	0	0	0

Table 127. M_PWM3_CFG register bit description

Bit	Symbol	Description
0 to 9	PWM3_DC	**Configure the PWM3 duty cycle**
		PWM3 duty cycle = 100 * PWM3_DC / 1000
		POR
10	PWM3_F	**Configure the PWM3 frequency**
		0 PWM3 frequency = 200 Hz
		1 PWM3 frequency = 400 Hz
		POR
11 to 12	PWM3_DLY	**Configure the PWM3 delay time (applies on both edges)**
		00 PWM3 delay = 0 us
		01 PWM3 delay = 5 us
		10 PWM3 delay = 10 us
		11 PWM3 delay = 15 us
		POR

22.28 M_TIMER_PWM_CTRL

Table 128. M_TIMER_PWM_CTRL register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	-	-	-	-	-	-	-	-
Read	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	-	TIM1_EN	TIM2_EN	TIM3_EN	-	PWM1_EN	PWM2_EN	PWM3_EN
Read	0	TIM1_EN	TIM2_EN	TIM3_EN	0	PWM1_EN	PWM2_EN	PWM3_EN
Reset	0	0	0	0	0	0	0	0

Table 129. M_TIMER_PWM_CTRL register bit description

Bit	Symbol	Description
0	PWM3_EN	**Enable the PWM3**
		0 PWM3 is disabled
		1 PWM3 is enabled

Table 129. M_TIMER_PWM_CTRL register bit description...*continued*

Bit	Symbol	Description
		POR, or clear on Write(write '1')
1	PWM2_EN	**Enable the PWM2**
		0 PWM2 is disabled
		1 PWM2 is enabled
		POR, or clear on Write(write '1')
2	PWM1_EN	**Enable the PWM1**
		0 PWM1 is disabled
		1 PWM1 is enabled
		POR, or clear on Write(write '1')
4	TIM3_EN	**Enable the TIMER3**
		0 TIMER3 is disabled
		1 TIMER3 is enabled
		POR, or clear on Write(write '1')
5	TIM2_EN	**Enable the TIMER2**
		0 TIMER2 is disabled
		1 TIMER2 is enabled
		POR, or clear on Write(write '1')
6	TIM1_EN	**Enable the TIMER1**
		0 TIMER1 is disabled
		1 TIMER1 is enabled
		POR, or clear on Write(write '1')

22.29 M_CS_CFG

Table 130. M_CS_CFG register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	-	-	-	-	-	-	HS_FLT_ WU_FORCE	-
Read	0	0	0	0	0	0	HS_FLT_ WU_FORCE	0
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	HVIO2_HS_SEL		HVIO1_HS_SEL		WK2_HS_SEL		WK1_HS_SEL	
Read	HVIO2_HS_SEL		HVIO1_HS_SEL		WK2_HS_SEL		WK1_HS_SEL	
Reset	0	0	0	0	0	0	0	0

Table 131. M_CS_CFG register bit description

Bit	Symbol	Description
0 to 1	WK1_HS_SEL	**Select the High Side connected to WAKE1 for cyclic sensing**
		00 HS1 is connected to WAKE1
		01 HS2 is connected to WAKE1
		10 HS3 is connected to WAKE1
		11 HS4 is connected to WAKE1
		POR
2 to 3	WK2_HS_SEL	**Select the High Side connected to WAKE2 for cyclic sensing**

Table 131. M_CS_CFG register bit description*...continued*

Bit	Symbol	Description
		00 HS1 is connected to WAKE2
		01 HS2 is connected to WAKE2
		10 HS3 is connected to WAKE2
		11 HS4 is connected to WAKE2
		POR
4 to 5	HVIO1_HS_SEL	**Select the High Side connected to HVIO1 for cyclic sensing**
		00 HS1 is connected to HVIO1
		01 HS2 is connected to HVIO1
		10 HS3 is connected to HVIO1
		11 HS4 is connected to HVIO1
		POR
6 to 7	HVIO2_HS_SEL	**Select the High Side connected to HVIO2 for cyclic sensing**
		00 HS1 is connected to HVIO2
		01 HS2 is connected to HVIO2
		10 HS3 is connected to HVIO2
		11 HS4 is connected to HVIO2
		POR
9	HS_FLT_WU_FORCE	**Select the reaction when a fault is detected on a High Side**
		0 Disable the cyclic sense engine when the fault is present
		1 Force the wake up of the device when the fault is detected
		POR

22.30 M_CS_FLG_MSK

Table 132. M_CS_FLG_MSK register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	-	-	-	-	-	-	-	HVIO2_OL_M
Read	0	0	0	0	0	0	0	HVIO2_OL_M
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	HVIO1_OL_M	WAKE2_OL_M	WAKE1_OL_M	-	-	-	-	-
Read	HVIO1_OL_M	WAKE2_OL_M	WAKE1_OL_M	0	HVIO2_OL_I	HVIO1_OL_I	WAKE2_OL_I	WAKE1_OL_I
Reset	0	0	0	0	0	0	0	0

Table 133. M_CS_FLG_MSK register bit description

Bit	Symbol	Description
0	WAKE1_OL_I	**Report WAKE1 Open Load event**
		0 No event detected
		1 WAKE1 OL occurred
		POR, or clear on Write(write '1')
1	WAKE2_OL_I	**Report WAKE2 Open Load event**
		0 No event detected
		1 WAKE2 OL occurred
		POR, or clear on Write(write '1')

Table 133. M_CS_FLG_MSK register bit description*...continued*

Bit	Symbol	Description
2	HVIO1_OL_I	**Report HVIO1 Open Load event**
		0 No event detected
		1 HVIO1 OL occurred
		POR, or clear on Write(write '1')
3	HVIO2_OL_I	**Report HVIO2 Open Load event**
		0 No event detected
		1 HVIO2 OL occurred
		POR, or clear on Write(write '1')
5	WAKE1_OL_M	**Inhibit WAKE1 Open Load Interrupt**
		0 Interrupt is Not Inhibited
		1 Interrupt is Inhibited
		POR
6	WAKE2_OL_M	**Inhibit WAKE2 Open Load Interrupt**
		0 Interrupt is Not Inhibited
		1 Interrupt is Inhibited
		POR
7	HVIO1_OL_M	**Inhibit HVIO1 Open Load Interrupt**
		0 Interrupt is Not Inhibited
		1 Interrupt is Inhibited
		POR
8	HVIO2_OL_M	**Inhibit HVIO2 Open Load Interrupt**
		0 Interrupt is Not Inhibited
		1 Interrupt is Inhibited
		POR

22.31 M_HSx_SRC_CFG

Table 134. M_HSx_SRC_CFG register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	HS4_SRC_SEL				HS3_SRC_SEL			
Read	HS4_SRC_SEL				HS3_SRC_SEL			
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	HS2_SRC_SEL				HS1_SRC_SEL			
Read	HS2_SRC_SEL				HS1_SRC_SEL			
Reset	0	0	0	0	0	0	0	0

Table 135. M_HSx_SRC_CFG register bit description

Bit	Symbol	Description
0 to 3	HS1_SRC_SEL	**Select HS1 source**
		0000 High side is driven by HS1_EN and HS1_DIS register bits
		0001 HVIO1 is selected as direct drive pin
		0010 HVIO2 is selected as direct drive pin.
		0011 WAKE1 is selected as direct drive pin.

Table 135. M_HSx_SRC_CFG register bit description*...continued*

Bit	Symbol	Description
		0100 WAKE2 is selected as direct drive pin.
		0101 LVIO3 is selected as direct drive pin.
		0110 LVIO4 is selected as direct drive pin.
		0111 LVI5 is selected as direct drive pin.
		1000 High side is driven by TIMER1
		1001 High side is driven by TIMER2
		1010 High side is driven by TIMER3
		1011 High side is driven by PWM1
		1100 High side is driven by PWM2
		1101 High side is driven by PWM3
		1110 Not used
		1111 Not used
		POR or HS1 FSM in HS2 state
4 to 7	HS2_SRC_SEL	**Select HS2 source**
		0000 High side is driven by HS2_EN and HS2_DIS register bits
		0001 HVIO1 is selected as direct drive pin
		0010 HVIO2 is selected as direct drive pin.
		0011 WAKE1 is selected as direct drive pin.
		0100 WAKE2 is selected as direct drive pin.
		0101 LVIO3 is selected as direct drive pin.
		0110 LVIO4 is selected as direct drive pin.
		0111 LVI5 is selected as direct drive pin.
		1000 High side is driven by TIMER1
		1001 High side is driven by TIMER2
		1010 High side is driven by TIMER3
		1011 High side is driven by PWM1
		1100 High side is driven by PWM2
		1101 High side is driven by PWM3
		1110 Not used
		1111 Not used
		POR or HS2 FSM in HS2 state
8 to 11	HS3_SRC_SEL	**Select HS3 source**
		0000 High side is driven by HS3_EN and HS3_DIS register bits
		0001 HVIO1 is selected as direct drive pin
		0010 HVIO2 is selected as direct drive pin.
		0011 WAKE1 is selected as direct drive pin.
		0100 WAKE2 is selected as direct drive pin.
		0101 LVIO3 is selected as direct drive pin.
		0110 LVIO4 is selected as direct drive pin.
		0111 LVI5 is selected as direct drive pin.
		1000 High side is driven by TIMER1
		1001 High side is driven by TIMER2
		1010 High side is driven by TIMER3
		1011 High side is driven by PWM1
		1100 High side is driven by PWM2

Table 135. M_HSx_SRC_CFG register bit description...*continued*

Bit	Symbol	Description
		1101 High side is driven by PWM3
		1110 Not used
		1111 Not used
		POR or HS3 FSM in HS2 state
12 to 15	HS4_SRC_SEL	**Select HS4 source**
		0000 High side is driven by HS4_EN and HS4_DIS register bits
		0001 HVIO1 is selected as direct drive pin
		0010 HVIO2 is selected as direct drive pin.
		0011 WAKE1 is selected as direct drive pin.
		0100 WAKE2 is selected as direct drive pin.
		0101 LVIO3 is selected as direct drive pin.
		0110 LVIO4 is selected as direct drive pin.
		0111 LVI5 is selected as direct drive pin.
		1000 High side is driven by TIMER1
		1001 High side is driven by TIMER2
		1010 High side is driven by TIMER3
		1011 High side is driven by PWM1
		1100 High side is driven by PWM2
		1101 High side is driven by PWM3
		1110 Not used
		1111 Not used
		POR or HS4 FSM in HS2 state

22.32 M_HSx_CTRL

Table 136. M_HSx_CTRL register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	-	HS_ VSHSUVOV_ REC	HS_ VSHSUV_DIS	HS_ VSHSOV_DIS	-	-	-	-
Read	0	HS_ VSHSUVOV_ REC	HS_ VSHSUV_DIS	HS_ VSHSOV_DIS	0	0	0	0
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	-	HS4_EN	-	HS3_EN	-	HS2_EN	-	HS1_EN
Read	0	HS4_EN	0	HS3_EN	0	HS2_EN	0	HS1_EN
Reset	0	0	0	0	0	0	0	0

Table 137. M_HSx_CTRL register bit description

Bit	Symbol	Description
0	HS1_EN	**Enable the HS1**
		0 HS1 is disabled
		1 HS1 is enabled
		POR or HS1 FSM in HS2 state
2	HS2_EN	**Enable the HS2**

Table 137. M_HSx_CTRL register bit description*...continued*

Bit	Symbol	Description
		0 HS2 is disabled
		1 HS2 is enabled
		POR or HS2 FSM in HS2 state
4	HS3_EN	**Enable the HS3**
		0 HS3 is disabled
		1 HS3 is enabled
		POR or HS3 FSM in HS2 state
6	HS4_EN	**Enable the HS4**
		0 HS4 is disabled
		1 HS4 is enabled
		POR or HS4 FSM in HS2 state
12	HS_VSHSOV_DIS	**Disable HSx in case of VSHS overvoltage**
		0 HSx remains enable in case of VSHS overvoltage
		1 HSx are disabled in case of VSHS overvoltage
		POR
13	HS_VSHSUV_DIS	**Disable HSx in case of VSHS undervoltage**
		0 HSx remains enable in case of VSHS undervoltage
		1 HSx are disabled in case of VSHS undervoltage
		POR
14	HS_VSHSUVOV_REC	**Configure the automatic recovery when HSx is disabled due to VSHS UV/OV**
		0 No recovery
		1 Automatic recovery when VSHS UV or OV is removed
		POR

22.33 M_HSx_FLG

Table 138. M_HSx_FLG register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	-	-	-	-	-	-	-	-
Read	0	0	0	HS4_OL_I	HS4_OC_I	0	HS3_OL_I	HS3_OC_I
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	-	-	-	-	-	-	-	-
Read	HS34_TSD_I	0	HS2_OL_I	HS2_OC_I	0	HS1_OL_I	HS1_OC_I	HS12_TSD_I
Reset	0	0	0	0	0	0	0	0

Table 139. M_HSx_FLG register bit description

Bit	Symbol	Description
0	HS12_TSD_I	**Report HS1 or HS2 Thermal Shutdown event**
		0 No event detected
		1 HS1 or HS2 TSD occurred
		POR, or clear on Write(write '1')
1	HS1_OC_I	**Report HS1 overcurrent event**
		0 No event detected

Table 139. M_HSx_FLG register bit description*...continued*

Bit	Symbol	Description
		1 HS1 OC occurred
		POR, or clear on Write(write '1')
2	HS1_OL_I	**Report HS1 Open Load event**
		0 No event detected
		1 HS1 OL occurred
		POR, or clear on Write(write '1')
4	HS2_OC_I	**Report HS2 overcurrent event**
		0 No event detected
		1 HS2 OC occurred
		POR, or clear on Write(write '1')
5	HS2_OL_I	**Report HS2 Open Load event**
		0 No event detected
		1 HS2 OL occurred
		POR, or clear on Write(write '1')
7	HS34_TSD_I	**Report HS3 or HS4 Thermal Shutdown event**
		0 No event detected
		1 HS3 or HS4 TSD occurred
		POR, or clear on Write(write '1')
8	HS3_OC_I	**Report HS3 overcurrent event**
		0 No event detected
		1 HS3 OC occurred
		POR, or clear on Write(write '1')
9	HS3_OL_I	**Report HS3 Open Load event**
		0 No event detected
		1 HS3 OL occurred
		POR, or clear on Write(write '1')
11	HS4_OC_I	**Report HS4 overcurrent event**
		0 No event detected
		1 HS4 OC occurred
		POR, or clear on Write(write '1')
12	HS4_OL_I	**Report HS4 Open Load event**
		0 No event detected
		1 HS4 OL occurred
		POR, or clear on Write(write '1')

22.34 M_HSx_MSK

Table 140. M_HSx_MSK register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	-	-	-	HS4_OL_M	HS4_OC_M	-	HS3_OL_M	HS3_OC_M
Read	0	0	0	HS4_OL_M	HS4_OC_M	0	HS3_OL_M	HS3_OC_M
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	HS34_TSD_M	-	HS2_OL_M	HS2_OC_M	-	HS1_OL_M	HS1_OC_M	HS12_TSD_M
Read	HS34_TSD_M	0	HS2_OL_M	HS2_OC_M	0	HS1_OL_M	HS1_OC_M	HS12_TSD_M

Table 140. M_HSx_MSK register bit allocation*...continued*

Bit	15	14	13	12	11	10	9	8
Reset	0	0	0	0	0	0	0	0

Table 141. M_HSx_MSK register bit description

Bit	Symbol	Description
0	HS12_TSD_M	**Inhibit HS1 and HS2 Thermal Shutdown Interrupt**
		0 Interrupt is Not Inhibited
		1 Interrupt is Inhibited
		POR
1	HS1_OC_M	**Inhibit HS1 overcurrent Interrupt**
		0 Interrupt is Not Inhibited
		1 Interrupt is Inhibited
		POR
2	HS1_OL_M	**Inhibit HS1 Open Load Interrupt**
		0 Interrupt is Not Inhibited
		1 Interrupt is Inhibited
		POR
4	HS2_OC_M	**Inhibit HS2 overcurrent Interrupt**
		0 Interrupt is Not Inhibited
		1 Interrupt is Inhibited
		POR
5	HS2_OL_M	**Inhibit HS2 Open Load Interrupt**
		0 Interrupt is Not Inhibited
		1 Interrupt is Inhibited
		POR
7	HS34_TSD_M	**Inhibit HS3 and HS4 Thermal Shutdown Interrupt**
		0 Interrupt is Not Inhibited
		1 Interrupt is Inhibited
		POR
8	HS3_OC_M	**Inhibit HS3 overcurrent Interrupt**
		0 Interrupt is Not Inhibited
		1 Interrupt is Inhibited
		POR
9	HS3_OL_M	**Inhibit HS3 Open Load Interrupt**
		0 Interrupt is Not Inhibited
		1 Interrupt is Inhibited
		POR
11	HS4_OC_M	**Inhibit HS4 overcurrent Interrupt**
		0 Interrupt is Not Inhibited
		1 Interrupt is Inhibited
		POR
12	HS4_OL_M	**Inhibit HS4 Open Load Interrupt**
		0 Interrupt is Not Inhibited
		1 Interrupt is Inhibited
		POR

22.35 M_AMUX_CTRL

Table 142. M_AMUX_CTRL register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	-	-	-	-	-	-	AMUX_EN	AMUX_DIV
Read	0	0	0	0	0	0	AMUX_EN	AMUX_DIV
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	-	-	-	AMUX				
Read	0	0	0	AMUX				
Reset	0	0	0	0	0	0	0	0

Table 143. M_AMUX_CTRL register bit description

Bit	Symbol	Description
0 to 4	AMUX	**Select AMUX Input Channel**
		00000 AGND is selected
		00001 V1p6 internal voltage (VDIG) is selected
		00010 V1 voltage is selected
		00011 V2 voltage is selected
		00100 V3 voltage is selected
		00101 VBOS internal voltage is selected
		00110 VSUP voltage is selected (divider ratio configurable by SPI / I²C)
		00111 VSHS voltage is selected (divider ratio configurable by SPI / I²C)
		01000 WAKE1 voltage is selected (divider ratio configurable by SPI / I²C)
		01001 WAKE2 voltage is selected (divider ratio configurable by SPI / I²C)
		01010 HVIO1 voltage is selected (divider ratio configurable by SPI / I²C)
		01011 HVIO2 voltage is selected (divider ratio configurable by SPI / I²C)
		01100 Die Temperature Sensor is selected : T(°C) = (V_{AMUX} – V_{TEMP25}) / V_{TEMP_COEFF} + 25
		01101 V1 Temperature sensor is selected
		01110 V2 Temperature sensor is selected
		01111 V3 Temperature sensor is selected
		10000 VDDIO not divided is selected
		>10000 Reserved
		POR
8	AMUX_DIV	**Select AMUX divider ratio for high voltage channels**
		0 Low divider ratio is selected (div by 10.5)
		1 High divider ratio is selected (div by 20)
		POR
9	AMUX_EN	**Enable AMUX block**
		0 AMUX is disabled (HIZ, int pull down)
		1 AMUX is enabled in Normal mode only
		POR

22.36 M_LDT_CFG1

Table 144. M_LDT_CFG1 register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	LDT_AFTER_RUN							
Read	LDT_AFTER_RUN							
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
Write	LDT_AFTER_RUN							
Read	LDT_AFTER_RUN							
Reset	0	0	0	0	0	0	0	0

Table 145. M_LDT_CFG1 register bit description

Bit	Symbol	Description
0 to 15	LDT_AFTER_RUN	**Configure and read the After run LDT Timer**
		LDT timer value in NORMAL mode
		POR, LDT Count started

22.37 M_LDT_CFG2

Table 146. M_LDT_CFG2 register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	LDT_WUP_L							
Read	LDT_WUP_L							
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
Write	LDT_WUP_L							
Read	LDT_WUP_L							
Reset	0	0	0	0	0	0	0	0

Table 147. M_LDT_CFG2 register bit description

Bit	Symbol	Description
0 to 15	LDT_WUP_L	**Configure and read the 16 less significant bits of Wake-up LDT Timer**
		LDT timer value in LP Mode (LSB)
		POR, LDT Count started

22.38 M_LDT_CFG3

Table 148. M_LDT_CFG3 register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	-	-	-	-	-	-	-	-
Read	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
Write	LDT_WUP_H							

Table 148. M_LDT_CFG3 register bit allocation*...continued*

Bit	15	14	13	12	11	10	9	8
Read	LDT_WUP_H							
Reset	0	0	0	0	0	0	0	0

Table 149. M_LDT_CFG3 register bit description

Bit	Symbol	Description
0 to 7	LDT_WUP_H	**Configure and read the 8 more significant bits of LDT Wake-up Timer**
		LDT timer value in LP Mode (MSB)
		POR, LDT Count started

22.39 M_LDT_CTRL

Table 150. M_LDT_CTRL register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	-	-	-	-	-	-	-	-
Read	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	LDT2LP	LDT_FNCT			LDT_SEL	LDT_MODE	LDT_EN	-
Read	LDT2LP	LDT_FNCT			LDT_SEL	LDT_MODE	LDT_EN	LDT_RUN
Reset	0	0	0	0	0	0	0	0

Table 151. M_LDT_CTRL register bit description

Bit	Symbol	Description
0	LDT_RUN	**LDT Status**
		0 LDT is idle
		1 LDT is busy
		POR, LDT stopped
1	LDT_EN	**Start LDT Timer operation**
		0 LDT is disabled
		1 LDT starts counting
		POR
2	LDT_MODE	**Set LDT operation mode**
		0 LDT is set to long count (1s)
		1 LDT is set to short count (128us)
		POR
3	LDT_SEL	**Configure and read LDT timer selection**
		0 Target value of Wake-up LDT timer can be read or write
		1 Real time value of 24 bit Timer is reported (once LDT stopped)
		POR
4 to 6	LDT_FNCT[2:0]	**Select LDT function**
		000 Function1 is selected
		001 Function2 is selected
		010 Function3 is selected

Table 151. M_LDT_CTRL register bit description...*continued*

Bit	Symbol	Description
		011 Function4 is selected
		100 Function5 is selected
		101 Not used
		110 Not used
		111 Not used
		POR
7	LDT2LP	**Select LP mode transition from LDT F2 and F3**
		0 Go to LPOFF
		1 Go to LPON
		POR

22.40 M_CAN

Table 152. M_CAN register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	-	-	-	-	-	-	CAN_MODE	
Read	0	0	0	0	0	0	CAN_MODE	
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	-	-	CAN_FS_DIS	-	-	-	CAN_TXD_TO_I	CAN_TSD_I
Read	CAN_ACTIVE_MODE_S	0	CAN_FS_DIS	0	0	0	CAN_TXD_TO_I	CAN_TSD_I
Reset	0	0	0	0	0	0	0	0

Table 153. M_CAN register bit description

Bit	Symbol	Description
0	CAN_TSD_I	**Report CAN overtemperature event**
		0 No event detected
		1 CAN Thermal Shutdown occurred
		POR, or clear on Write(write '1')
1	CAN_TXD_TO_I	**Report CAN TXD Dominant timeout event**
		0 No event detected
		1 Dominant timeout occurred
		POR, or clear on Write(write '1')
5	CAN_FS_DIS	**Disable the CAN when RSTB or LIMP0 or FS0B is activated**
		0 CAN transceiver is offline
		1 CAN transceiver keeps the current state
		POR
7	CAN_ACTIVE_MODE_S	**Real-time status of CAN mode**
		0 CAN is neither in LISTEN ONLY mode nor in NORMAL mode
		1 CAN is either in LISTEN ONLY mode or in NORMAL mode
		Real-time information
8 to 9	CAN_MODE	**Select the CAN mode control**
		00 Transceiver offline (TX and RX disabled)
		01 Transceiver receive only mode (TX disabled and RX enabled)

Table 153. M_CAN register bit description*...continued*

Bit	Symbol	Description
		10 Transceiver active mode (TX and RX enabled) reacting on V3UV
		11 Transceiver active mode (TX and RX enabled) reacting on V3UV
		POR

22.41 M_LIN

Table 154. M_LIN register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	-	LIN_MODE		LIN_SLOPE		LIN_FS_DIS	LIN_VSHSUV_DIS	LIN_SC
Read	0	LIN_MODE		LIN_SLOPE		LIN_FS_DIS	LIN_VSHSUV_DIS	LIN_SC
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	LIN_TXD_TO	-	-	-	-	LIN_SC_I	LIN_TXD_TO_I	LIN_TSD_I
Read	LIN_TXD_TO	0	0	0	0	LIN_SC_I	LIN_TXD_TO_I	LIN_TSD_I
Reset	0	0	0	0	0	0	0	0

Table 155. M_LIN register bit description

Bit	Symbol	Description
0	LIN_TSD_I	**Report LIN overtemperature event**
		0 No event detected
		1 LIN Thermal Shutdown occurred
		POR, or clear on Write (write '1')
1	LIN_TXD_TO_I	**Report LIN TXD Dominant timeout event**
		0 No event detected
		1 Dominant timeout occurred
		POR, or clear on Write (write '1')
2	LIN_SC_I	**Report LIN short-circuit event**
		0 No event detected
		1 Short-circuit timeout occurred
		POR, or clear on Write (write '1')
7	LIN_TXD_TO	**Enable the TXD dominant timeout detection**
		0 TXD dominant timeout detection is disabled
		1 TXD dominant timeout detection is enabled
		POR
8	LIN_SC	**Disable the LIN short circuit detection**
		0 LIN short circuit protection is enabled
		1 LIN short circuit protection is disabled
		POR
9	LIN_VSHSUV_DIS	**Disable VSHS_UV impact on the LIN transceiver**
		0 The LIN transceiver is OFF in case of VSHS undervoltage
		1 The LIN transceiver remains in active mode in case of VSHS undervoltage
		POR
10	LIN_FS_DIS	**Disable the LIN when RSTB or LIMP0 or FS0B is activated**
		0 LIN transceiver is offline

Table 155. M_LIN register bit description*...continued*

Bit	Symbol	Description
		1 LIN transceiver keeps the current state
		POR
11 to 12	LIN_SLOPE	**Select the LIN slope control**
		00 LIN normal slope is enabled
		01 Not used
		10 LIN slow slope is enabled
		11 Not used
		POR
13 to 14	LIN_MODE	**Select the LIN mode control**
		00 Transceiver offline
		01 Transceiver receive only mode
		10 Transceiver active mode
		11 Transceiver active mode
		POR

22.42 M_CAN_LIN_MSK

Table 156. M_CAN_LIN_MSK register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	-	-	LIN_FSM_STATE_S					LIN_SC_M
Read	0	0	LIN_FSM_STATE_S					LIN_SC_M
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	LIN_TXD_TO_M	LIN_TSD_M	-	CAN_FSM_STATE_S			CAN_TXD_TO_M	CAN_TSD_M
Read	LIN_TXD_TO_M	LIN_TSD_M	0	CAN_FSM_STATE_S			CAN_TXD_TO_M	CAN_TSD_M
Reset	0	0	0	0	0	0	0	0

Table 157. M_CAN_LIN_MSK register bit description

Bit	Symbol	Description
0	CAN_TSD_M	**Inhibit CAN temperature shutdown Interrupt**
		0 Interrupt is Not Inhibited
		1 Interrupt is Inhibited
		POR
1	CAN_TXD_TO_M	**Inhibit CAN TXD Dominant timeout Interrupt**
		0 Interrupt is Not Inhibited
		1 Interrupt is Inhibited
		POR
2 to 4	CAN_FSM_STATE_S[2:0]	**Report the CAN state machine state**
		000 OFF
		001 OFFLINE
		010 Invalid state
		011 OFFLINEVCCNOK
		100 GOACTIVE
		101 LISTEN

Table 157. M_CAN_LIN_MSK register bit description...*continued*

Bit	Symbol	Description
		110 Invalid state
		111 NORMAL
		Real-time information
6	LIN_TSD_M	**Inhibit LIN temperature shutdown Interrupt**
		0 Interrupt is Not Inhibited
		1 Interrupt is Inhibited
		POR
7	LIN_TXD_TO_M	**Inhibit LIN TXD Dominant timeout Interrupt**
		0 Interrupt is Not Inhibited
		1 Interrupt is Inhibited
		POR
8	LIN_SC_M	**Inhibit LIN short-circuit Interrupt**
		0 Interrupt is Not Inhibited
		1 Interrupt is Inhibited
		POR
9 to 13	LIN_FSM_STATE_S	**Report the LIN state machine state**
		00011 TRX_ON
		00110 TRX_RXONLY
		00111 TRX_PROTECT
		01100 TRX_DISABLE
		01111 TRX_POWERON
		10011 TRX_MONITOR
		10111 TX_POWERON
		Any other value Invalid state
		Real-time information

22.43 M_MEMORY0

Table 158. M_MEMORY0 register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	MEMORY0							
Read	MEMORY0							
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	MEMORY0							
Read	MEMORY0							
Reset	0	0	0	0	0	0	0	0

Table 159. M_MEMORY0 register bit description

Bit	Symbol	Description
0 to 15	MEMORY0	**Provide 16 memory bits**
		Read or write MEMORY0 memory bits
		Reset on Power On Reset (POR)

22.44 M_MEMORY1

Table 160. M_MEMORY1 register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	MEMORY1							
Read	MEMORY1							
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	MEMORY1							
Read	MEMORY1							
Reset	0	0	0	0	0	0	0	0

Table 161. M_MEMORY1 register bit description

Bit	Symbol	Description
0 to 15	MEMORY1	**Provide 16 memory bits**
		Read or write MEMORY1 memory bits
		Reset on Power On Reset (POR)

22.45 FS_I_OVUV_CFG1

Table 162. FS_I_OVUV_CFG1 register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	-	-	-	V1MON_OV_ RSTB_IMPACT	V1MON_OV_ FS0B_IMPACT	V1MON_OV_ LIMP0_IMPACT	V1MON_UV_ RSTB_IMPACT	V1MON_UV_ FS0B_IMPACT
Read	0	0	0	V1MON_OV_ RSTB_IMPACT	V1MON_OV_ FS0B_IMPACT	V1MON_OV_ LIMP0_IMPACT	V1MON_UV_ RSTB_IMPACT	V1MON_UV_ FS0B_IMPACT
Reset	0	0	0	OTP fuse	1	1	OTP fuse	1
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	V1MON_UV_ LIMP0_IMPACT	-	V2MON_OV_ RSTB_IMPACT	V2MON_OV_ FS0B_IMPACT	V2MON_OV_ LIMP0_IMPACT	V2MON_UV_ RSTB_IMPACT	V2MON_UV_ FS0B_IMPACT	V2MON_UV_ LIMP0_IMPACT
Read	V1MON_UV_ LIMP0_IMPACT	0	V2MON_OV_ RSTB_IMPACT	V2MON_OV_ FS0B_IMPACT	V2MON_OV_ LIMP0_IMPACT	V2MON_UV_ RSTB_IMPACT	V2MON_UV_ FS0B_IMPACT	V2MON_UV_ LIMP0_IMPACT
Reset	1	0	OTP fuse	1	1	OTP fuse	0	0

Table 163. FS_I_OVUV_CFG1 register bit description

Bit	Symbol	Description
0	V2MON_UV_LIMP0_IMPACT	**Configure V2MON UV impact on LIMP0**
		0 No Effect
		1 LIMP0 Assertion
		POR
1	V2MON_UV_FS0B_IMPACT	**Configure V2MON UV impact on FS0B**
		0 No Effect
		1 FS0B Assertion
		POR
2	V2MON_UV_RSTB_IMPACT	**Configure V2MON UV impact on RSTB**
		0 No Effect
		1 RSTB Assertion

Table 163. FS_I_OVUV_CFG1 register bit description*...continued*

Bit	Symbol	Description
		OTP Fuse load
3	V2MON_OV_LIMP0_IMPACT	**Configure V2MON OV impact on LIMP0**
		0 No Effect
		1 LIMP0 Assertion
		POR
4	V2MON_OV_FS0B_IMPACT	**Configure V2MON OV impact on FS0B**
		0 No Effect
		1 FS0B Assertion
		POR
5	V2MON_OV_RSTB_IMPACT	**Configure V2MON OV impact on RSTB**
		0 No Effect
		1 RSTB Assertion
		OTP Fuse load
7	V1MON_UV_LIMP0_IMPACT	**Configure V1MON UV impact on LIMP0**
		0 No Effect
		1 LIMP0 Assertion
		POR
8	V1MON_UV_FS0B_IMPACT	**Configure V1MON UV impact on FS0B**
		0 No Effect
		1 FS0B Assertion
		POR
9	V1MON_UV_RSTB_IMPACT	**Configure V1MON UV impact on RSTB**
		0 No Effect
		1 RSTB Assertion
		OTP Fuse load
10	V1MON_OV_LIMP0_IMPACT	**Configure V1MON OV impact on LIMP0**
		0 No Effect
		1 LIMP0 Assertion
		POR
11	V1MON_OV_FS0B_IMPACT	**Configure V1MON OV impact on FS0B**
		0 No Effect
		1 FS0B Assertion
		POR
12	V1MON_OV_RSTB_IMPACT	**Configure V1MON OV impact on RSTB**
		0 No Effect
		1 RSTB Assertion
		OTP Fuse load

22.46 FS_I_OVUV_CFG2

Table 164. FS_I_OVUV_CFG2 register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	-	-	-	V3MON_ OV_RSTB_ IMPACT	V3MON_ OV_FS0 B_IMPACT	V3MON_ OV_LIMP0_ IMPACT	V3MON_ UV_RSTB_ IMPACT	V3MON_ UV_FS0 B_IMPACT

Table 164. FS_I_OVUV_CFG2 register bit allocation...*continued*

Bit	15	14	13	12	11	10	9	8
Read	0	0	0	V3MON_OV_RSTB_IMPACT	V3MON_OV_FS0B_IMPACT	V3MON_OV_LIMP0_IMPACT	V3MON_UV_RSTB_IMPACT	V3MON_UV_FS0B_IMPACT
Reset	0	0	0	OTP fuse	1	1	OTP fuse	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	V3MON_UV_LIMP0_IMPACT	-	V0MON_OV_RSTB_IMPACT	V0MON_OV_FS0B_IMPACT	V0MON_OV_LIMP0_IMPACT	V0MON_UV_RSTB_IMPACT	V0MON_UV_FS0B_IMPACT	V0MON_UV_LIMP0_IMPACT
Read	V3MON_UV_LIMP0_IMPACT	0	V0MON_OV_RSTB_IMPACT	V0MON_OV_FS0B_IMPACT	V0MON_OV_LIMP0_IMPACT	V0MON_UV_RSTB_IMPACT	V0MON_UV_FS0B_IMPACT	V0MON_UV_LIMP0_IMPACT
Reset	0	0	OTP fuse	1	1	OTP fuse	0	0

Table 165. FS_I_OVUV_CFG2 register bit description

Bit	Symbol	Description
0	V0MON_UV_LIMP0_IMPACT	**Configure VMON_EXT UV impact on LIMP0**
		0 No Effect
		1 LIMP0 Assertion
		POR
1	V0MON_UV_FS0B_IMPACT	**Configure VMON_EXT UV impact on FS0B**
		0 No Effect
		1 FS0B Assertion
		POR
2	V0MON_UV_RSTB_IMPACT	**Configure VMON_EXT UV impact on RSTB**
		0 No Effect
		1 RSTB Assertion
		OTP Fuse load
3	V0MON_OV_LIMP0_IMPACT	**Configure VMON_EXT OV impact on LIMP0**
		0 No Effect
		1 LIMP0 Assertion
		POR
4	V0MON_OV_FS0B_IMPACT	**Configure VMON_EXT OV impact on FS0B**
		0 No Effect
		1 FS0B Assertion
		POR
5	V0MON_OV_RSTB_IMPACT	**Configure VMON_EXT OV impact on RSTB**
		0 No Effect
		1 RSTB Assertion

Table 165. FS_I_OVUV_CFG2 register bit description*...continued*

Bit	Symbol	Description
		OTP Fuse load
7	V3MON_UV_LIMP0_IMPACT	**Configure V3MON UV impact on LIMP0**
		0 No Effect
		1 LIMP0 Assertion
		POR
8	V3MON_UV_FS0B_IMPACT	**Configure V3MON UV impact on FS0B**
		0 No Effect
		1 FS0B Assertion
		POR
9	V3MON_UV_RSTB_IMPACT	**Configure V3MON UV impact on RSTB**
		0 No Effect
		1 RSTB Assertion
		OTP Fuse load
10	V3MON_OV_LIMP0_IMPACT	**Configure V3MON OV impact on LIMP0**
		0 No Effect
		1 LIMP0 Assertion
		POR
11	V3MON_OV_FS0B_IMPACT	**Configure V3MON OV impact on FS0B**
		0 No Effect
		1 FS0B Assertion
		POR
12	V3MON_OV_RSTB_IMPACT	**Configure V3MON OV impact on RSTB**
		0 No Effect
		1 RSTB Assertion
		OTP Fuse load

22.47 FS_I_FCCU_CFG

Table 166. FS_I_FCCU_CFG register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	-	FCCU_CFG			FCCU2_ASSIGN			FCCU12_FLT_POL
Read	0	FCCU_CFG			FCCU2_ASSIGN			FCCU12_FLT_POL
Reset	0	0	0	1	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	FCCU2_FLT_POL	FCCU1_FLT_POL	FCCU2_RSTB_IMPACT	FCCU2_FS0B_IMPACT	FCCU2_LIMP0_IMPACT	FCCU1_RSTB_IMPACT	FCCU1_FS0B_IMPACT	FCCU1_LIMP0_IMPACT

Table 166. FS_I_FCCU_CFG register bit allocation*...continued*

Bit	15	14	13	12	11	10	9	8
Read	FCCU2_FLT_POL	FCCU1_FLT_POL	FCCU2_RSTB_IMPACT	FCCU2_FS0B_IMPACT	FCCU2_LIMP0_IMPACT	FCCU1_RSTB_IMPACT	FCCU1_FS0B_IMPACT	FCCU1_LIMP0_IMPACT
Reset	0	0	1	1	1	1	1	1

Table 167. FS_I_FCCU_CFG register bit description

Bit	Symbol	Description
0	FCCU1_LIMP0_IMPACT	**Configure FCCU1 impact on LIMP0**
		0 No Effect
		1 LIMP0 Assertion
		POR
1	FCCU1_FS0B_IMPACT	**Configure FCCU1 impact on FS0B**
		0 No Effect
		1 FS0B Assertion
		POR
2	FCCU1_RSTB_IMPACT	**Configure FCCU1 impact on RSTB**
		0 No Effect
		1 RSTB Assertion
		POR
3	FCCU2_LIMP0_IMPACT	**Configure FCCU2 impact on LIMP0**
		0 No Effect
		1 LIMP0 Assertion
		POR
4	FCCU2_FS0B_IMPACT	**Configure FCCU2 impact on FS0B**
		0 No Effect
		1 FS0B Assertion
		POR
5	FCCU2_RSTB_IMPACT	**Configure FCCU2 impact on RSTB**
		0 No Effect
		1 RSTB Assertion
		POR
6	FCCU1_FLT_POL	**Configure FCCU1 Fault Polarity**
		0 Low Level is a Fault
		1 High Level is a Fault
		POR
7	FCCU2_FLT_POL	**Configure FCCU2 Fault Polarity**
		0 Low Level is a Fault
		1 High Level is a Fault
		POR
8	FCCU12_FLT_POL	**Configure FCCU12 Fault Polarity**
		0 FCCU1=0 or FCCU2=1 level is a fault
		1 FCCU1=1 or FCCU2=0 level is a fault
		POR
9 to 11	FCCU2_ASSIGN	**Assign FCCU2 function to an input pin**
		000 FCCU2 is disabled

Table 167. FS_I_FCCU_CFG register bit description*...continued*

Bit	Symbol	Description
		001 FCCU2 is assigned to HVIO1
		010 FCCU2 is assigned to HVIO2
		011 FCCU2 is assigned to LVIO3
		100 FCCU2 is assigned to LVIO4
		101 FCCU2 is assigned to LVI5
		110 not used
		111 not used
		POR
12 to 14	FCCU_CFG	**Configure FCCU Monitoring**
		000 No monitoring
		001 FCCU1 and FCCU2 inputs monitoring activated by pair (bi-stable protocol)
		010 FCCU1 or FCCU2 single input monitoring activated
		011 FCCU1 input monitoring only, FCCU2 input not used
		100 FCCU2 input monitoring only, FCCU1 input not used
		101 FCCU1 or FCCU2 single input PWM monitoring activated
		110 FCCU1 input PWM monitoring only, FCCU2 input level monitoring
		111 FCCU2 input PWM monitoring only, FCCU1 input level monitoring
		POR

22.48 FS_I_FSSM_CFG

Table 168. FS_I_FSSM_CFG register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	-	EXT_RSTB_DIS	RSTB8S_DIS	RSTB_DUR	LIMP0_SC_ RSTB_IMPACT	EXTRSTB_ FS0B_IMPACT	FS0B_SC_ RSTB_IMPACT	FLT_ERR_ LIMIT
Read	0	EXT_RSTB_DIS	RSTB8S_DIS	RSTB_DUR	LIMP0_SC_ RSTB_IMPACT	EXTRSTB_ FS0B_IMPACT	FS0B_SC_ RSTB_IMPACT	FLT_ERR_ LIMIT
Reset	0	0	OTP fuse	OTP fuse	1	0	1	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	FLT_ERR_ LIMIT	FLT_MID_ RSTB_IMPACT	FLT_MID_FS0 B_IMPACT	FLT_MID_ LIMP0_IMPACT	FLT_ERR_CNT			
Read	FLT_ERR_ LIMIT	FLT_MID_ RSTB_IMPACT	FLT_MID_FS0 B_IMPACT	FLT_MID_ LIMP0_IMPACT	FLT_ERR_CNT			
Reset	1	1	1	1	0	0	0	1

Table 169. FS_I_FSSM_CFG register bit description

Bit	Symbol	Description
0 to 3	FLT_ERR_CNT	**Reflect the value of the Fault Error Counter**
		0000 0
		0001 1
		0010 2
		0011 3
		0100 4
		0101 5
		0110 6
		0111 7

Table 169. FS_I_FSSM_CFG register bit description*...continued*

Bit	Symbol	Description
		1000 8
		1001 9
		1010 10
		1011 11
		1100 12
		1101 12
		1110 12
		1111 12
		POR
4	FLT_MID_LIMP0_IMPACT	**Configure LIMP0 reaction when Fault Error Counter ≥ intermediate value**
		0 No action
		1 LIMP0 assertion
		POR
5	FLT_MID_FS0B_IMPACT	**Configure FS0B reaction when Fault Error Counter ≥ intermediate value**
		0 No action
		1 FS0B assertion
		POR
6	FLT_MID_RSTB_IMPACT	**Configure RSTB reaction when Fault Error Counter ≥ intermediate value**
		0 No action
		1 RSTB assertion
		POR
7 to 8	FLT_ERR_LIMIT	**Configure the Fault Error Counter max value**
		00 Max Value = 2
		01 Max Value = 6
		10 Max Value = 8
		11 Max Value = 12
		POR
9	FS0B_SC_RSTB_IMPACT	**Configure RSTB reaction when FS0B is detected shorted to high**
		0 No action
		1 RSTB assertion
		POR
10	EXTRSTB_FS0B_IMPACT	**Configure FS0B reaction when external reset is detected**
		0 No action
		1 FS0B assertion
		POR
11	LIMP0_SC_RSTB_IMPACT	**Configure RSTB reaction when LIMP0 is detected shorted to high**
		0 No action
		1 LIMP0 assertion
		POR
12	RSTB_DUR	**Configure RSTB pulse duration**
		0 10 ms
		1 1 ms
		OTP Fuse load
13	RSTB8S_DIS	**Disable the RSTB low 8s timer**
		0 RSTB low 8s timer is enabled

Table 169. FS_I_FSSM_CFG register bit description *...continued*

Bit	Symbol	Description
		1 RSTB low 8s time is disabled
		OTP Fuse load
14	EXT_RSTB_DIS	**Disable the external RSTB monitoring in Normal mode (except RSTB8s time out)**
		0 External RSTB monitoring is enabled
		1 External RSTB monitoring is disabled
		POR

22.49 FS_I_WD_CFG

Table 170. FS_I_WD_CFG register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	-	WD_RSTB_ IMPACT	WD_FS0 B_IMPACT	WD_LIMP0_ IMPACT	WD_DIS_ LPON	WD_RFR_LIMIT		WD_ERR_ LIMIT
Read	0	WD_RSTB_ IMPACT	WD_FS0 B_IMPACT	WD_LIMP0_ IMPACT	WD_DIS_ LPON	WD_RFR_LIMIT		WD_ERR_ LIMIT
Reset	0	1	1	1	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	WD_ERR_LIMIT	-	-	-	-	-	-	-
Read	WD_ERR_LIMIT	WD_RFR_CNT			WD_ERR_CNT			
Reset	1	0	0	0	0	0	0	0

Table 171. FS_I_WD_CFG register bit description

Bit	Symbol	Description
0 to 3	WD_ERR_CNT	**Reflect the value of the Watchdog Error Counter**
		0000 0
		0001 1
		0010 2
		0011 3
		0100 4
		0101 5
		0110 6
		0111 7
		1000 8
		POR
4 to 6	WD_RFR_CNT	**Reflect the value of the Watchdog Refresh Counter**
		000 0
		001 1
		010 2
		011 3
		100 4
		101 5
		110 6
		111 6
		POR
7 to 8	WD_ERR_LIMIT	**Configure the Watchdog Error Counter Limit**

Table 171. FS_I_WD_CFG register bit description*...continued*

Bit	Symbol	Description
		00 8
		01 6
		10 4
		11 2
		POR
9 to 10	WD_RFR_LIMIT	**Configure the Watchdog Refresh Counter Limit**
		00 6
		01 4
		10 2
		11 1
		POR
11	WD_DIS_LPON	**Automatically disable the Watchdog in LPON mode (when GO2LPON)**
		0 WD stays enabled in LPON
		1 WD is disabled in LPON
		POR
12	WD_LIMP0_IMPACT	**Configure Watchdog error impact on LIMP0**
		0 No Effect
		1 LIMP0 Assertion
		POR
13	WD_FS0B_IMPACT	**Configure Watchdog error impact on FS0B**
		0 No Effect
		1 FS0B Assertion
		POR
14	WD_RSTB_IMPACT	**Configure Watchdog error impact on RSTB**
		0 No Effect
		1 RSTB Assertion
		POR

22.50 FS_WDW_CFG

Table 172. FS_WDW_CFG register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	-	-	-	-	WDW_ REC_EN	WDW_EN	-	WDW_ PERIOD
Read	0	0	0	0	WDW_ REC_EN	WDW_EN	0	WDW_ PERIOD
Reset	0	0	0	0	0	0	0	1
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	WDW_PERIOD			-	WDW_RECOVERY			
Read	WDW_PERIOD			0	WDW_RECOVERY			
Reset	1	0	1	0	1	0	1	1

Table 173. FS_WDW_CFG register bit description

Bit	Symbol	Description
0 to 3	WDW_RECOVERY	**Configure the Watchdog Window Recovery period**
		0000 INFINITE Time Out, Window fully opened
		0001 1 ms
		0010 2 ms
		0011 3 ms
		0100 4 ms
		0101 6 ms
		0110 8 ms
		0111 12 ms
		1000 16 ms
		1001 24 ms
		1010 32 ms
		1011 64 ms (default value)
		1100 128 ms
		1101 256 ms
		1110 512 ms
		1111 1024 ms
		POR
5 to 8	WDW_PERIOD	**Configure the Watchdog Window period**
		0000 INFINITE Time Out, Window fully opened
		0001 1 ms
		0010 2 ms
		0011 3 ms
		0100 4 ms
		0101 6 ms
		0110 8 ms
		0111 12 ms
		1000 16 ms
		1001 24 ms
		1010 32 ms
		1011 256 ms (default value)
		1100 128 ms
		1101 256 ms
		1110 512 ms
		1111 1024 ms
		POR, WD_DISABLE

Table 173. FS_WDW_CFG register bit description...*continued*

Bit	Symbol	Description
10	WDW_EN	**Enable the Watchdog Window**
		0 Watchdog Window is disabled (Watchdog Time out)
		1 Watchdog Window is enabled (Watchdog Window 50%)
		POR, WD_2 to WD_1 FSM transition, WD_0
11	WDW_REC_EN	**Enable the Watchdog Recovery when FCCU fault is detected**
		0 Watchdog recovery is disabled
		1 Watchdog recovery is enabled
		POR

22.51 FS_WD_TOKEN

Table 174. FS_WD_TOKEN register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	WD_TOKEN							
Read	WD_TOKEN							
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	WD_TOKEN							
Read	WD_TOKEN							
Reset	0	0	0	0	0	0	0	0

Table 175. FS_WD_TOKEN register bit description

Bit	Symbol	Description
0 to 15	WD_TOKEN	**Read Watchdog Token code**
		0x5AB2 (default value) or 0xD564
		Reset on Power on Reset (POR)

22.52 FS_WD_ANSWER

Table 176. FS_WD_ANSWER register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	WD_ANSWER							
Read	WD_ANSWER							
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	WD_ANSWER							
Read	WD_ANSWER							
Reset	0	0	0	0	0	0	0	0

Table 177. FS_WD_ANSWER register bit description

Bit	Symbol	Description
0 to 15	WD_ANSWER	**Read or Write WD Answer**
		WD_TOKEN[15:0]
		Reset on Power on Reset (POR)

22.53 FS_LIMP12_CFG

Table 178. FS_LIMP12_CFG register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	-	-	-	-	-	-	-	LIMP2_DC_CFG
Read	0	0	0	0	0	0	0	LIMP2_DC_CFG
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	LIMP2_DC_CFG	LIMP2_CFG		LIMP2_REQ	-	LIMP1_CFG		LIMP1_REQ
Read	LIMP2_DC_CFG	LIMP2_CFG		0	0	LIMP1_CFG		0
Reset	0	OTP fuse		0	0	OTP fuse		0

Table 179. FS_LIMP12_CFG register bit description

Bit	Symbol	Description
0	LIMP1_REQ	**Request an assertion of LIMP1**
		0 No action
		1 LIMP1 assertion
		POR, Self-clear
1 to 2	LIMP1_CFG	**Select LIMP1 polarity or PWM frequency**
		00 PWM frequency = 1.25 Hz with 50 % duty cycle (Default high)
		01 Default High (Active low)
		10 PWM frequency = 1.25 Hz with 50 % duty cycle (Default low)
		11 Default Low (Active high)
		OTP Fuse Load
4	LIMP2_REQ	**Request an assertion of LIMP2**
		0 No action
		1 LIMP2 assertion
		POR, Self-clear
5 to 6	LIMP2_CFG	**Select LIMP2 polarity or PWM frequency**
		00 PWM frequency = 100 Hz (Default high)
		01 Default High (Active low)
		10 PWM frequency = 100 Hz (Default low)
		11 Default Low (Active high)
		OTP Fuse Load
7 to 8	LIMP2_DC_CFG	**Select LIMP2 PWM duty cycle**
		00 PWM duty cycle = 20 %
		01 PWM duty cycle = 10 %
		10 PWM duty cycle = 5 %
		11 PWM duty cycle = 2.5 %
		POR

22.54 FS_FS0B_LIMP0_REL

Table 180. FS_FS0B_LIMP0_REL register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	RELEASE_FS0B_LIMP0							
Read	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	RELEASE_FS0B_LIMP0							
Read	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0

Table 181. FS_FS0B_LIMP0_REL register bit description

Bit	Symbol	Description
0 to 15	RELEASE_FS0B_LIMP0	**Write secured 16 bits word to release FS0B and/or LIMP0**
		Write 3'b011,~WD_TOKEN[0:12] to release FS0B
		Write 3'b110,~WD_TOKEN[3:15] to release LIMP0
		Write 3'b101,~WD_TOKEN[0:6],~WD_TOKEN[10:15] to release both FS0B and LIMP0
		Reset on Power on Reset (POR)

22.55 FS_ABIST

Table 182. FS_ABIST register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	-	LAUNCH_ABIST	CLEAR_ABIST	-	-	-	-	-
Read	ABIST_READY	0	0	ABIST_DONE	ABIST_ ONGOING	ABIST_V0 MON_DIAG	ABIST_V1 UVLP_DIAG	ABIST_V1 MON_DIAG
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	-	-	-	ABIST_V0MON	ABIST_ V1UVLP	ABIST_V1MON	ABIST_V2MON	ABIST_V3MON
Read	ABIST_V2 MON_DIAG	ABIST_V3 MON_DIAG	0	ABIST_V0MON	ABIST_ V1UVLP	ABIST_V1MON	ABIST_V2MON	ABIST_V3MON
Reset	0	0	0	0	0	0	0	0

Table 183. FS_ABIST register bit description

Bit	Symbol	Description
0	ABIST_V3MON	**Request ABIST on V3MON**
		0 No ABIST
		1 ABIST on V3MON Requested
		POR
1	ABIST_V2MON	**Request ABIST on V2MON**
		0 No ABIST
		1 ABIST on V2MON Requested
		POR
2	ABIST_V1MON	**Request ABIST on V1MON**

Table 183. FS_ABIST register bit description*...continued*

Bit	Symbol	Description
		0 No ABIST
		1 ABIST on V1MON Requested
		POR
3	ABIST_V1UVLP	**Request ABIST on V1UVLP**
		0 No ABIST
		1 ABIST on V1UVLP Requested
		POR
4	ABIST_V0MON	**Request ABIST on VMON_EXT**
		0 No ABIST
		1 ABIST on VMON_EXT Requested
		POR
6	ABIST_V3MON_DIAG	**Report ABIST status on V3MON**
		0 ABIST not executed on V3MON or fail on V3MON
		1 V3MON ABIST PASS
		POR / Clear on Write / LAUNCH_ABIST
7	ABIST_V2MON_DIAG	**Report ABIST status on V2MON**
		0 ABIST not executed on V2MON or fail on V2MON
		1 V2MON ABIST PASS
		POR / CLEAR_ABIST
8	ABIST_V1MON_DIAG	**Report ABIST status on V1MON**
		0 ABIST not executed on V1MON or fail on V1MON
		1 V1MON ABIST PASS
		POR / CLEAR_ABIST
9	ABIST_V1UVLP_DIAG	**Report ABIST status on V1UVLP**
		0 ABIST not executed on V1UVLP or fail on V1UVLP
		1 V1UVLP ABIST PASS
		POR / CLEAR_ABIST
10	ABIST_V0MON_DIAG	**Report ABIST status on V0MON**
		0 ABIST not executed on V0MON or fail on V0MON
		1 V0MON ABIST PASS
		POR / CLEAR_ABIST
11	ABIST_ONGOING	**Report ABIST On going status**
		0 No ABIST on going
		1 ABIST on going
		POR
12	ABIST_DONE	**Diagnostic of ABIST on Demand**
		0 ABIST not executed
		1 ABIST executed
		POR / CLEAR_ABIST
13	CLEAR_ABIST	**Clear ABIST flags**
		0 No action
		1 Clear ABIST flags (ABIST_DONE, ABIST_VxMON_DIAG, ABIST_V1UVLP_DIAG)
		POR
14	LAUNCH_ABIST	**Launch ABIST on selected VMON**
		0 No action

Table 183. FS_ABIST register bit description *...continued*

Bit	Symbol	Description
		1 Launch ABIST
		POR
15	ABIST_READY	**Report ABIST Ready for launch**
		0 ABIST not ready for launch
		1 ABIST ready for launch
		POR

22.56 FS_SAFETY_OUTPUTS

Table 184. FS_SAFETY_OUTPUTS register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	-	-	-	-	-	-	RSTB_REQ	-
Read	0	RSTB_EXT	RSTB_EVT	RSTB_DRV	RSTB_SNS	RSTB_DIAG	0	FS0B_DRV
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	-	-	FS0B_REQ	-	-	-	-	LIMP0_REQ
Read	FS0B_SNS	FS0B_DIAG	0	0	LIMP0_DRV	LIMP0_SNS	LIMP0_DIAG	0
Reset	0	0	0	0	0	0	0	0

Table 185. FS_SAFETY_OUTPUTS register bit description

Bit	Symbol	Description
0	LIMP0_REQ	**Request an assertion of LIMP0**
		0 No action
		1 LIMP0 assertion
		POR, Self-clear
1	LIMP0_DIAG	**Report a LIMP0 short to HIGH**
		0 No Failure
		1 Short to High detected
		POR, or clear on Write(write '1')
2	LIMP0_SNS	**Sense LIMP0 pad**
		0 LIMP0 pad is sensed low
		1 LIMP0 pad is sensed High
		Real-time information
3	LIMP0_DRV	**Report the digital command of LIMP0 driver**
		0 LIMP0 Driver command sensed Low
		1 LIMP0 Driver command sensed High
		Real-time information
5	FS0B_REQ	**Request an assertion of FS0B**
		0 No action
		1 FS0B assertion
		POR, Self-clear
6	FS0B_DIAG	**Report a FS0B short to HIGH**
		0 No Failure
		1 FS0B short to High detected

Table 185. FS_SAFETY_OUTPUTS register bit description*...continued*

Bit	Symbol	Description
		POR, or clear on Write(write '1')
7	FS0B_SNS	**Sense FS0B pad**
		0 FS0B pad sensed low
		1 FS0B pad sensed High
		Real-time information
8	FS0B_DRV	**Report the digital command of FS0B driver**
		0 FS0B Driver command sensed Low
		1 FS0B Driver command sensed High
		Real-time information
9	RSTB_REQ	**Request an assertion of Reset**
		0 No action
		1 RSTB assertion (pulse)
		POR, Self-clear
10	RSTB_DIAG	**Report a Reset short to HIGH**
		0 No Failure
		1 Short to High detected
		POR, or clear on Write(write '1')
11	RSTB_SNS	**Sense RSTB pad**
		0 RSTB pad is sensed low
		1 RSTB pad is sensed High
		Real-time information
12	RSTB_DRV	**Report the digital command of RSTB driver**
		0 RSTB Driver command sensed Low
		1 RSTB Driver command sensed High
		Real-time information
13	RSTB_EVT	**Report a RSTB Event generated by FS23**
		0 No RSTB event
		1 RSTB event Occurred
		POR, or clear on Write(write '1')
14	RSTB_EXT	**Report a RSTB pin assertion**
		0 No RSTB pin assertion
		1 RSTB pin assertion Occurred
		POR, or clear on Write(write '1')

22.57 FS_SAFETY_FLG

Table 186. FS_SAFETY_FLG register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	-	-	-	INIT_CRC_NOK_M	-	WD_NOK_M	-	-
Read	FCCU12_ERR_S	FCCU1_ERR_S	FCCU2_ERR_S	INIT_CRC_NOK_M	INIT_CRC_NOK_I	WD_NOK_M	WD_NOK_I	0
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	FCCU12_M	FCCU1_M	FCCU2_M	-	-	-	-	-
Read	FCCU12_M	FCCU1_M	FCCU2_M	FCCU12_I	FCCU1_I	FCCU2_I	FCCU1_S	FCCU2_S

Table 186. FS_SAFETY_FLG register bit allocation*...continued*

Bit	15	14	13	12	11	10	9	8
Reset	0	0	0	0	0	0	0	0

Table 187. FS_SAFETY_FLG register bit description

Bit	Symbol	Description
0	FCCU2_S	**Sense FCCU2 pin state**
		0 FCCU2 is Low
		1 FCCU2 is High
		Real-time information
1	FCCU1_S	**Sense FCCU1 pin state**
		0 FCCU1 is Low
		1 FCCU1 is High
		Real-time information
2	FCCU2_I	**Report FCCU2 input error**
		0 No error
		1 FCCU2 error reported
		POR, or clear on Write(write '1')
3	FCCU1_I	**Report FCCU1 input error**
		0 No error
		1 FCCU1 error reported
		POR, or clear on Write(write '1')
4	FCCU12_I	**Report FCCU12 input error**
		0 No error
		1 FCCU12 error reported
		POR, or clear on Write(write '1')
5	FCCU2_M	**Inhibit FCCU2 Interrupt**
		0 Interrupt is Not Inhibited
		1 Interrupt is Inhibited
		POR
6	FCCU1_M	**Inhibit FCCU1 Interrupt**
		0 Interrupt is Not Inhibited
		1 Interrupt is Inhibited
		POR
7	FCCU12_M	**Inhibit FCCU12 Interrupt**
		0 Interrupt is Not Inhibited
		1 Interrupt is Inhibited
		POR
9	WD_NOK_I	**Report a Watchdog Refresh error**
		0 WD refresh OK
		1 WD refresh not OK
		POR, or clear on Write (write '1')
10	WD_NOK_M	**Mask Watchdog Not OK Refresh Interrupt**
		0 Interrupt is Not Inhibited
		1 Interrupt is Inhibited
		POR

Table 187. FS_SAFETY_FLG register bit description*...continued*

Bit	Symbol	Description
11	INIT_CRC_NOK_I	**Report an INIT Register CRC error**
		0 No error detected
		1 INIT registers CRC error detected
		POR, or clear on Write(write '1')
12	INIT_CRC_NOK_M	**Mask CRC Not OK Interrupt**
		0 Interrupt is Not Inhibited
		1 Interrupt is Inhibited
		POR
13	FCCU2_ERR_S	**Report real-time FCCU2 error (generated by MCU)**
		0 No error
		1 Real-time error detected
		Real-time information
14	FCCU1_ERR_S	**Report real-time FCCU1 error (generated by MCU)**
		0 No error
		1 Real-time error detected
		Real-time information
15	FCCU12_ERR_S	**Report real-time FCCU12 error (generated by MCU)**
		0 No error
		1 Real-time error detected
		Real-time information

22.58 FS_CRC

Table 188. FS_CRC register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	-	INIT_ CRC_REQ	-	-	-	INIT_CRC_ FS0B_IMPACT	INIT_CRC_ LIMP0_IMPACT	-
Read	0	0	0	0	0	INIT_CRC_ FS0B_IMPACT	INIT_CRC_ LIMP0_IMPACT	0
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	CRC_VALUE							
Read	CRC_VALUE							
Reset	0	0	0	0	0	0	0	0

Table 189. FS_CRC register bit description

Bit	Symbol	Description
0 to 7	CRC_VALUE	**INIT registers CRC value calculated by the MCU (CRC check every 5 ms in NORMAL mode only)**
		CRC_VALUE[7:0]
		Reset on Power on Reset (POR)
9	INIT_CRC_LIMP0_IMPACT	**Configure CRC impact on LIMP0**
		0 No Effect
		1 LIMP0 Assertion
		Reset on Power on Reset (POR)
10	INIT_CRC_FS0B_IMPACT	**Configure CRC impact on FS0B**

Table 189. FS_CRC register bit description*...continued*

Bit	Symbol	Description
		0 No Effect
		1 FS0B Assertion
		Reset on Power on Reset (POR)
14	INIT_CRC_REQ	**Request INIT CRC computation in INIT phase**
		0 No Effect
		1 Computation of the INIT CRC starts
		Reset on Power on Reset (POR)

23 OTP register mapping

Table 190. OTP Register mapping

Register	#	Address							Reference
		Adr_6	Adr_5	Adr_4	Adr_3	Adr_2	Adr_1	Adr_0	
OTP_DEVICE_VER	0	0	0	1	1	1	0	0	Section 24.1
OTP_DEVICE_VER1	1	0	0	1	1	1	0	1	Section 24.2
OTP_PROG_ID	2	0	0	1	1	1	1	0	Section 24.3
OTP_V1_CFG1	3	0	0	1	1	1	1	1	Section 24.4
OTP_V1_CFG2	4	0	1	0	0	0	0	0	Section 24.5
OTP_V1_CFG3	5	0	1	0	0	0	0	1	Section 24.6
OTP_V1_CFG4	6	0	1	0	0	0	1	0	Section 24.7
OTP_V1_CFG5	7	0	1	0	0	0	1	1	Section 24.8
OTP_V1_CFG6	8	0	1	0	0	1	0	0	Section 24.9
OTP_V1_CFG7	9	0	1	0	0	1	0	1	Section 24.10
OTP_V1_CFG8	10	0	1	0	0	1	1	0	Section 24.11
OTP_V1_CFG9	11	0	1	0	0	1	1	1	Section 24.12
OTP_V2_CFG	12	0	1	0	1	0	0	0	Section 24.13
OTP_V3_CFG	13	0	1	0	1	0	0	1	Section 24.14
OTP_HVIO_CFG1	14	0	1	0	1	0	1	0	Section 24.15
OTP_HVIO_CFG2	15	0	1	0	1	0	1	1	Section 24.16
OTP_LVIO_CFG1	16	0	1	0	1	1	0	0	Section 24.17
OTP_LVIO_CFG2	17	0	1	0	1	1	0	1	Section 24.18
OTP_IO_OUT_SEL_CFG	18	0	1	0	1	1	1	0	Section 24.19
OTP_MAIN_SYS_I2C_CFG	19	0	1	0	1	1	1	1	Section 24.20
OTP_FS_SYS_CFG	20	0	1	1	0	0	0	0	Section 24.21
OTP_OVUV_CFG1	21	0	1	1	0	0	0	1	Section 24.22
OTP_OVUV_CFG2	22	0	1	1	0	0	1	0	Section 24.23
OTP_OVUV_CFG3	23	0	1	1	0	0	1	1	Section 24.24
OTP_OVUV_CFG4	24	0	1	1	0	1	0	0	Section 24.25
OTP_UV_DGLT_CFG	25	0	1	1	0	1	0	1	Section 24.26
OTP_LIMP_OV_DGLT_CFG	26	0	1	1	0	1	1	0	Section 24.27
OTP_RSTB_IMPACT_CFG	27	0	1	1	0	1	1	1	Section 24.28

Table 191. OTP register map content

Orange = HVBUCK version only. Green = HVLDO version only

Register	Address	Default	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
OTP_DEVICE_VER	0x1C	0x00	KEY_OFFON_EN_OTP	CAN_EN_OTP	LIN_EN_OTP	LDTIM_EN_OTP	HSD13_EN_OTP	HSD24_EN_OTP	V2_EN_OTP	V1_PNP_EN_OTP
OTP_DEVICE_VER1	0x1D	0x00	RSTB_DUR_OTP	ABIST_EN_OTP	FCCU_EN_OTP	FS0B_EN_OTP	LIMP0_EN_OTP	V0MON_EN_OTP	Reserved	Reserved
OTP_PROG_ID	0x1E	0x00	PROG_IDH_OTP[3]	PROG_IDH_OTP[2]	PROG_IDH_OTP[1]	PROG_IDH_OTP[0]	PROG_IDL_OTP[3]	PROG_IDL_OTP[2]	PROG_IDL_OTP[1]	PROG_IDL_OTP[0]
OTP_V1_CFG1	0X1F	0x00	Reserved	BUCK_ SRHSON_OTP[2]	BUCK_ SRHSON_OTP[1]	BUCK_ SRHSON_OTP[0]	BUCK_ SRHSOFF_OTP[1]	BUCK_ SRHSOFF_OTP[0]	BUCK_SS_OTP[1]	BUCK_SS_OTP[0]
OTP_V1_CFG2	0x20	0x00	Reserved	Reserved	BUCK_CLK_OTP	BUCK_RCOMP_OTP[2]	BUCK_RCOMP_OTP[1]	BUCK_RCOMP_OTP[0]	BUCK_CCOMP_OTP[1]	BUCK_CCOMP_OTP[0]
OTP_V1_CFG3	0x21	0x00	Reserved	V1_OCLS_EN_OTP	BUCK_SC_OTP[5]	BUCK_SC_OTP[4]	BUCK_SC_OTP[3]	BUCK_SC_OTP[2]	BUCK_SC_OTP[1]	BUCK_SC_OTP[0]
OTP_V1_CFG4	0x22	0x00	Reserved	BUCK_PK_OC_ PFM_OTP[2]	BUCK_PK_OC_ PFM_OTP[1]	BUCK_PK_OC_ PFM_OTP[0]	BUCK_PFM_ TOFF_OTP[1]	BUCK_PFM_ TOFF_OTP[0]	BUCK_PFM_ TON_OTP[1]	BUCK_PFM_ TON_OTP[0]
OTP_V1_CFG5	0x23	0x00	BUCK_LP_ DVS_OTP{1]	BUCK_LP_ DVS_OTP[0]	BUCK_PK_OC_ PWM_OTP[2]	BUCK_PK_OC_ PWM_OTP[1]	BUCK_PK_OC_ PWM_OTP[0]	BUCK_AVG_OC_ PWM_OTP[2]	BUCK_AVG_OC_ PWM_OTP[1]	BUCK_AVG_OC_ PWM_OTP[0]
OTP_V1_CFG6	0x24	0x00	Reserved	Reserved	BUCK_LDO_ SET_OTP[1]	BUCK_LDO_ SET_OTP[0]	Reserved	Reserved	Reserved	Reserved
OTP_V1_CFG7	0x25	0x00	VV1_BUCK_ RANGE_OTP	VV1_BUCK_OTP[6]	VV1_BUCK_OTP[5]	VV1_BUCK_OTP[4]	VV1_BUCK_OTP[3]	VV1_BUCK_OTP[2]	VV1_BUCK_OTP[1]	VV1_BUCK_OTP[0]
OTP_V1_CFG8	0x26	0x00	Reserved	VV1_LP_BUCK_OTP[6]	VV1_LP_BUCK_OTP[5]	VV1_LP_BUCK_OTP[4]	VV1_LP_BUCK_OTP[3]	VV1_LP_BUCK_OTP[2]	VV1_LP_BUCK_OTP[1]	VV1_LP_BUCK_OTP[0]
OTP_V1_CFG9	0x27	0x00	VBOS2V1_SW_ ALWAYS_EN_OTP	V1MON_OTP	CONF_OV_V1_OTP	CONF_TSD_V1_OTP	CONF_OC_V1_OTP	VV1_LDO_OTP	CONF_OC_ TO_V1_OTP	VBOS2V1_SW_ LP_EN_OTP
OTP_V2_CFG	0x28	0x00	Reserved	V2MON_OTP	CONF_OV_V2_OTP	CONF_TSD_V2_OTP	CONF_OC_V2_OTP	VV2_OTP	V2_SLOT_OTP[1]	V2_SLOT_OTP[0]
OTP_V3_CFG	0x29	0x00	Reserved	V3MON_OTP	CONF_OV_V3_OTP	CONF_TSD_V3_OTP	CONF_OC_V3_OTP	VV3_OTP	V3_SLOT_OTP[1]	V3_SLOT_OTP[0]
OTP_HVIO_CFG1	0X2A	0x00	WK1PUPD_OTP[1]	WK1PUPD_OTP[0]	WK2PUPD_OTP[1]	WK2PUPD_OTP[0]	HVIO1_SLOT_OTP[1]	HVIO1_SLOT_OTP[0]	HVIO2_SLOT_OTP[1]	HVIO2_SLOT_OTP[0]
OTP_HVIO_CFG2	0X2B	0x00	HVIO1_OUT_EN_OTP	HVIO1_OUT_ DFLT_OTP	HVIO1PUPD_OTP[1]	HVIO1PUPD_OTP[0]	HVIO2_OUT_EN_OTP	HVIO2_OUT_ DFLT_OTP	HVIO2PUPD_OTP[1]	HVIO2PUPD_OTP[0]
OTP_LVIO_CFG1	0X2C	0x00	LVIO4_OUT_DFT_OTP	LVIO3_OUT_DFT_OTP	LVIO3PUPD_OTP[1]	LVIO3PUPD_OTP[0]	LVIO3_LS_EN_OTP	LVIO3_HS_EN_OTP	LVIO3_SLOT_OTP[1]	LVIO3_SLOT_OTP[0]
OTP_LVIO_CFG2	0X2D	0x00	LVI5PUPD_OTP[1]	LVI5PUPD_OTP[0]	LVIO4PUPD_OTP[1]	LVIO4PUPD_OTP[0]	LVIO4_LS_EN_OTP	LVIO4_HS_EN_OTP	LVIO4_SLOT_OTP[1]	LVIO4_SLOT_OTP[0]
OTP_IO_OUT_SEL_CFG	0X2E	0x00	Reserved	Reserved	HS3_SEL_OTP	HS1_SEL_OTP	LVO4_SEL_OTP	LVO3_SEL_OTP	HVO2_SEL_OTP	HVO1_SEL_OTP
OTP_MAIN_SYS_I2C_CFG	0X2F	0x00	MOD_CONF_OTP	MOD_EN_OTP	SLOT_BYP_OTP	SPI_EN_OTP	I2CDEVADDR_OTP[3]	I2CDEVADDR_OTP[2]	I2CDEVADDR_OTP[1]	I2CDEVADDR_OTP[0]
OTP_FS_SYS_CFG	0x30	0x00	Reserved	Reserved	INIT_CRC_DIS_OTP	FS_LPOFF_OTP	FS_DUR_CFG_OTP	WD_INF_OTP	RSTB8S_DIS_OTP	FIRST_FAULT_ EN_OTP
OTP_OVUV_CFG1	0x31	0x00	V1MON_UVTH_OTP[3]	V1MON_UVTH_OTP[2]	V1MON_UVTH_OTP[1]	V1MON_UVTH_OTP[0]	V1MON_OVTH_OTP[3]	V1MON_OVTH_OTP[2]	V1MON_OVTH_OTP[1]	V1MON_OVTH_OTP[0]
OTP_OVUV_CFG2	0x32	0x00	V2MON_UVTH_OTP[3]	V2MON_UVTH_OTP[2]	V2MON_UVTH_OTP[1]	V2MON_UVTH_OTP[0]	V2MON_OVTH_OTP[3]	V2MON_OVTH_OTP[2]	V2MON_OVTH_OTP[1]	V2MON_OVTH_OTP[0]
OTP_OVUV_CFG3	0x33	0x00	V3MON_UVTH_OTP[3]	V3MON_UVTH_OTP[2]	V3MON_UVTH_OTP[1]	V3MON_UVTH_OTP[0]	V3MON_OVTH_OTP[3]	V3MON_OVTH_OTP[2]	V3MON_OVTH_OTP[1]	V3MON_OVTH_OTP[0]
OTP_OVUV_CFG4	0x34	0x00	V0MON_UVTH_OTP[3]	V0MON_UVTH_OTP[2]	V0MON_UVTH_OTP[1]	V0MON_UVTH_OTP[0]	V0MON_OVTH_OTP[3]	V0MON_OVTH_OTP[2]	V0MON_OVTH_OTP[1]	V0MON_OVTH_OTP[0]
OTP_UV_DGLT_CFG	0x35	0x00	V0MON_ UVDGLT_OTP[1]	V0MON_ UVDGLT_OTP[0]	V1MON_ UVDGLT_OTP[1]	V1MON_ UVDGLT_OTP[0]	V2MON_ UVDGLT_OTP[1]	V2MON_ UVDGLT_OTP[0]	V3MON_ UVDGLT_OTP[1]	V3MON_ UVDGLT_OTP[0]
OTP_LIMP_OV_DGLT_CFG	0x36	0x00	LIMP2_CFG_OTP[1]	LIMP2_CFG_OTP[0]	LIMP1_CFG_OTP[1]	LIMP1_CFG_OTP[0]	V0MON_OVDGLT_OTP	V1MON_OVDGLT_OTP	V2MON_OVDGLT_OTP	V3MON_OVDGLT_OTP
OTP_RSTB_IMPACT_CFG	0x37	0x00	V0UV_RSTB_ IMPACT_OTP	V0OV_RSTB_ IMPACT_OTP	V1UV_RSTB_ IMPACT_OTP	V1OV_RSTB_ IMPACT_OTP	V2UV_RSTB_ IMPACT_OTP	V2OV_RSTB_ IMPACT_OTP	V3UV_RSTB_ IMPACT_OTP	V3OV_RSTB_ IMPACT_OTP

24 OTP register description

24.1 OTP_DEVICE_VER

Table 192. OTP_DEVICE_VER register bit allocation

Bit	7	6	5	4	3	2	1	0
Write **Read**	KEY_ OFFON_ EN_OTP	CAN_EN_ OTP	LIN_EN_ OTP	LDTIM_ EN_OTP	HSD13_ EN_OTP	HSD24_ EN_OTP	V2_EN_ OTP	V1_PNP_ EN_OTP
Reset	0	0	0	0	0	0	0	0

Table 193. OTP_DEVICE_VER register bit description

Bit	Symbol	Description
0	V1_PNP_EN_OTP	**Enable V1 PNP mode**
		0 V1 PNP mode is disabled
		1 V1 PNP mode is enabled
		Reset on power-on reset
1	V2_EN_OTP	**Enable V2 regulator**
		0 V2 is disabled
		1 V2 is enabled
		Reset on power-on reset
2	HSD24_EN_OTP	**Enable HS2 and HS4**
		0 HS2 and HS4 are disabled
		1 HS2 and HS4 are enabled
		Reset on power-on reset
3	HSD13_EN_OTP	**Enable HS1 and HS3**
		0 HS1 and HS3 are disabled
		1 HS1 and HS3 are enabled
		Reset on power-on reset
4	LDTIM_EN_OTP	**Enable the Long Duration Timer**
		0 LDT is disabled
		1 LDT is enabled
		Reset on power-on reset
5	LIN_EN_OTP	**Enable LIN transceiver**
		0 LIN is disabled
		1 LIN is enabled
		Reset on power-on reset

Table 193. OTP_DEVICE_VER register bit description*...continued*

Bit	Symbol	Description
6	CAN_EN_OTP	**Enable CAN transceiver**
		0 CAN is disabled by OTP
		1 CAN is enabled by OTP
		Reset on power-on reset
7	KEY_OFF_ ON_EN_OTP	**Enable KEY OFF – KEY ON feature**
		0 Key OFF – Key ON feature is disabled by OTP
		1 Key OFF – Key ON feature is enabled by OTP
		Reset on power-on reset

24.2 OTP_DEVICE_VER1

Table 194. OTP_DEVICE_VER1 register bit allocation

Bit	7	6	5	4	3	2	1	0
Write / **Read**	RSTB_ DUR_OTP	ABIST_ EN_OTP	FCCU_ EN_OTP	FS0B_ EN_ OTP	LIMP0_ EN_OTP	V0MON_ EN_OTP	Reserved	Reserved
Reset	0	0	0	0	0	0	0	0

Table 195. OTP_DEVICE_VER1 register bit description

Bit	Symbol	Description
2	V0MON_EN_OTP	**Enable VMON_EXT pin for V0MON monitoring**
		0 VMON_EXT pin is disabled
		1 VMON_EXT pin is enabled
		Reset on power-on reset
3	LIMP0_EN_OTP	**Enable LIMP0 safety output**
		0 LIMP0 is disabled
		1 LIMP0 is enabled
		Reset on power-on reset
4	FS0B_EN_OTP	**Enable FS0B safety output**
		0 FS0B is disabled
		1 FS0B is enabled
		Reset on power-on reset
5	FCCU_EN_OTP	**Enable FCCU monitoring**
		0 FCCU monitoring is disabled
		1 FCCU monitoring is enabled
		Reset on power-on reset

Table 195. OTP_DEVICE_VER1 register bit description*...continued*

Bit	Symbol	Description
6	ABIST_EN_OTP	**Enable ABIST checks**
		0 ABIST is disabled
		1 ABIST is enabled
		Reset on power-on reset
7	RSTB_DUR_OTP	**Configure RSTB pulse duration**
		0 10 ms
		1 1 ms
		Reset on power-on reset

24.3 OTP_PROG_ID

Table 196. OTP_PROG_ID register bit allocation

Bit	7	6	5	4	3	2	1	0
Write	PROG_IDH_OTP				PROG_IDL_OTP			
Read								
Reset	0	0	0	0	0	0	0	0

Table 197. OTP_PROG_ID register bit description

Bit	Symbol	Description
0 to 3	PROG_IDL_OTP	**Report the OTP code**
		0000 0
		0001 1
		0010 2
		0011 3
		0100 4
		0101 5
		0110 6
		0111 7
		1000 8
		1001 9
		1010 A
		1011 B
		1100 C
		1101 D
		1110 E
		1111 F
		Reset on power-on reset

Table 197. OTP_PROG_ID register bit description*...continued*

Bit	Symbol	Description
4 to 7	PROG_ IDH_OTP	**Report the OTP code**
		0000 A
		0001 B
		0010 C
		0011 D
		0100 E
		0101 F
		0110 G
		0111 H
		1000 J
		1001 K
		1010 L
		1011 M
		1100 N
		1101 P
		1110 Q
		1111 R
		Reset on power-on reset

24.4 OTP_V1_CFG1

Table 198. OTP_V1_CFG1 register bit allocation

Bit	7	6	5	4	3	2	1	0
Write	Reserved	BUCK_SRHSON_OTP			BUCK_SRHSOFF_OTP		BUCK_SS_OTP	
Read								
Reset	0	0	0	0	0	0	0	0

Table 199. OTP_V1_CFG1 register bit description

Bit	Symbol	Description
0 to 1	BUCK_SS_OTP	**Select BUCK soft start ramp**
		00 Soft start is 269 µs
		01 Soft start is 538 µs
		10 Soft start is 1077 µs
		11 Soft start is 2150 µs
		Reset on power-on reset
2 to 3	BUCK_ SRHSOFF_OTP	**Select BUCK slew rate when the High Side turns OFF**
		00 HS falling slew rate is 20 ns
		01 HS falling slew rate is 15 ns
		10 HS falling slew rate is 10 ns
		11 HS falling slew rate is 5 ns
		Reset on power-on reset
4 to 6	BUCK_ SRHSON_OTP	**Select BUCK slew rate when the High Side turns ON**
		000 HS rising slew rate is 20 ns
		001 HS rising slew rate is 20 ns
		010 HS rising slew rate is 15 ns
		011 HS rising slew rate is 10 ns
		100 HS rising slew rate is 6.3 ns
		101 HS rising slew rate is 5 ns
		110 HS rising slew rate is 3 ns
		111 HS rising slew rate is 2 ns
		Reset on power-on reset

24.5 OTP_V1_CFG2

Table 200. OTP_V1_CFG2 register bit allocation

Bit	7	6	5	4	3	2	1	0
Write / Read	Reserved	Reserved	BUCK_ CLK_OTP	BUCK_RCOMP_OTP			BUCK_CCOMP_OTP	
Reset	0	0	0	0	0	0	0	0

Table 201. OTP_V1_CFG2 register bit description

Bit	Symbol	Description
0 to 1	BUCK_CCOMP_OTP	**Select BUCK compensation network capacitor**
		00 12 pF
		01 23 pF
		10 33.5 pF
		11 44.5 pF
		Reset on power-on reset
2 to 4	BUCK_RCOMP_OTP	**Select BUCK compensation network resistor**
		000 1300 kOhms
		001 1137 kOhms
		010 975 kOhms
		011 812 kOhms
		100 650 kOhms
		101 512 kOhms
		110 325 kOhms
		111 162 kOhms
		Reset on power-on reset
5	BUCK_CLK_OTP	**Select BUCK switching frequency**
		0 Switching frequency is 450 kHz
		1 Switching frequency is 2.25 MHz
		Reset on power-on reset

24.6 OTP_V1_CFG3

Table 202. OTP_V1_CFG3 register bit allocation

Bit	7	6	5	4	3	2	1	0
Write	Reserved	V1_OCLS_EN_OTP	BUCK_SC_OTP					
Read								
Reset	0	0	0	0	0	0	0	0

Table 203. OTP_V1_CFG3 register bit description

Bit	Symbol	Description
0 to 5	BUCK_SC_OTP[1][2]	**Select BUCK slope compensation**
		010111 SC = 3690 mV/µs (recommended when Fsw = 2.25 MHz, LV1_buck = 4.7 µH and Vbuck = 3.3 V)
		011100 SC = 3229 mV/µs (recommended when Fsw = 2.25 MHz, LV1_buck = 4.7 µH and Vbuck = 5 V)
		100101 SC = 480 mV/µs (recommended when Fsw = 450 kHz, LV1_buck = 22 µH and Vbuck = 3.3 V)
		101001 SC = 406 mV/µs (recommended when Fsw = 450 kHz, LV1_buck = 22 µH and Vbuck = 5 V)
		Reset on power-on reset
6	V1_OCLS_EN_OTP	**Enable BUCK low side over current protection**
		0 Low side over current protection is disabled
		1 Low side over current protection is enabled
		Reset on power-on reset

[1] These codes are suggested as best fit for the described use cases. In case other values are needed, contact local support.
[2] The slope compensation values are given for a typical V1_IN at 13.5 V.

24.7 OTP_V1_CFG4

Table 204. OTP_V1_CFG4 register bit allocation

Bit	7	6	5	4	3	2	1	0
Write	Reserved	BUCK_PK_OC_PFM_OTP			BUCK_PFM_TOFF_OTP		BUCK_PFM_TON_OTP	
Read								
Reset	0	0	0	0	0	0	0	0

Table 205. OTP_V1_CFG4 register bit description

Bit	Symbol	Description
0 to 1	BUCK_PFM_TON_OTP[1]	**Select BUCK TON time in PFM**
		00 TON time in PFM is 1021 ns (V1 = 5 V, freq = 450 kHz, V1_IN = 12 V)
		01 TON time in PFM is 1272.5 ns (V1 = 5 V, freq = 450 kHz, V1_IN = 12 V)
		10 TON time in PFM is 1632.5 ns (V1 = 5 V, freq = 450 kHz, V1_IN = 12 V)
		11 TON time in PFM is 1772.5 ns (V1 = 5 V, freq = 450 kHz, V1_IN = 12 V)
		Reset on power-on reset
2 to 3	BUCK_PFM_TOFF_OTP[1]	**Select BUCK TOFF time in PFM**
		00 TOFF time in PFM is 605 ns (freq = 450 kHz)
		01 TOFF time in PFM is 1170 ns (freq = 450 kHz)
		10 TOFF time in PFM is 1725 ns (freq = 450 kHz)
		11 TOFF time in PFM is 2285 ns (freq = 450 kHz)
		Reset on power-on reset
4 to 6	BUCK_PK_OC_PFM_OTP	**Select BUCK peak over current detection threshold in PFM mode**
		000 Not used
		001 Not used
		010 Overcurrent (peak) threshold is 400 mA
		011 Overcurrent (peak) threshold is 500 mA
		100 Overcurrent (peak) threshold is 600 mA
		101 Overcurrent (peak) threshold is 700 mA
		110 Overcurrent (peak) threshold is 800 mA
		111 Overcurrent (peak) threshold is 900 mA
		Reset on power-on reset

[1] Values given for indication only. Refer to Application note for detailed description of these parameters.

24.8 OTP_V1_CFG5

Table 206. OTP_V1_CFG5 register bit allocation

Bit	7	6	5	4	3	2	1	0
Write	BUCK_LP_DVS_OTP		BUCK_PK_OC_PWM_OTP			BUCK_AVG_OC_PWM_OTP		
Read								
Reset	0	0	0	0	0	0	0	0

Table 207. OTP_V1_CFG5 register bit description

Bit	Symbol	Description
0 to 2	BUCK_AVG_ OC_PWM_OTP	**Select BUCK average over current detection threshold in PWM mode**
		000 Average overcurrent threshold is 200 mA
		001 Average overcurrent threshold is 300 mA
		010 Average overcurrent threshold is 400 mA
		011 Average overcurrent threshold is 500 mA
		100 Average overcurrent threshold is 600 mA
		101 Average overcurrent threshold is 700 mA
		110 Not used
		111 Not used
		Reset on power-on reset
3 to 5	BUCK_PK_ OC_PWM_OTP	**Select BUCK peak over current detection threshold in PWM mode**
		000 Not used
		001 Not used
		010 Overcurrent (peak) threshold is 400 mA
		011 Overcurrent (peak) threshold is 500 mA
		100 Overcurrent (peak) threshold is 600 mA
		101 Overcurrent (peak) threshold is 700 mA
		110 Overcurrent (peak) threshold is 800 mA
		111 Overcurrent (peak) threshold is 900 mA
		Reset on power-on reset
6 to 7	BUCK_LP_DVS_OTP	**Select BUCK DVS ramp rate**
		00 22.5 mV/µs
		01 11.25 mV/µs
		10 5.625 mV/µs
		11 2.8125 mV/µs
		Reset on power-on reset

24.9 OTP_V1_CFG6

Table 208. OTP_V1_CFG6 register bit allocation

Bit	7	6	5	4	3	2	1	0
Write / **Read**	Reserved	Reserved	BUCK_LDO_SET_OTP		Reserved	Reserved	Reserved	Reserved
Reset	0	0	0	0	0	0	0	0

Table 209. OTP_V1_CFG6 register bit description

Bit	Symbol	Description
4 to 5	BUCK_LDO_SET_OTP	**Select LDO mode detect comparator threshold**
		00 LDO mode detect falling threshold is 5.2 V
		01 LDO mode detect falling threshold is 6.2 V
		10 LDO mode detect falling threshold is 7.2 V
		11 LDO mode detect falling threshold is 8.2 V
		Reset on power-on reset

24.10 OTP_V1_CFG7

Table 210. OTP_V1_CFG7 register bit allocation

Bit	7	6	5	4	3	2	1	0
Write / **Read**	Reserved	VV1_BUCK_OTP						
Reset	0	0	0	0	0	0	0	0

Table 211. OTP_V1_CFG7 register bit description

Bit	Symbol	Description
0 to 6	VV1_BUCK_OTP	**Select V1 BUCK regulator output voltage in Normal mode**
		011 0010 3.3 V
		101 0100 5 V
		Reset on power-on reset

24.11 OTP_V1_CFG8

Table 212. OTP_V1_CFG8 register bit allocation

Bit	7	6	5	4	3	2	1	0
Write / **Read**	Reserved	VV1_LP_BUCK_OTP						
Reset	0	0	0	0	0	0	0	0

Table 213. OTP_V1_CFG8 register bit description

Bit	Symbol	Description
0 to 6	VV1_LP_BUCK_OTP	**Select V1 BUCK regulator output voltage in LPON mode**
		011 0010 3.3 V
		101 0100 5 V
		Reset on power-on reset

24.12 OTP_V1_CFG9

Table 214. OTP_V1_CFG9 register bit allocation

Bit	7	6	5	4	3	2	1	0
Write / **Read**	VBOS2V1_SW_ALWAYS_EN_OTP	V1MON_OTP	CONF_OV_V1_OTP	CONF_TSD_V1_OTP	CONF_OC_V1_OTP	VV1_LDO_OTP	CONF_OC_TO_V1_OTP	VBOS2V1_SW_LP_EN_OTP
Reset	0	0	0	0	0	0	0	0

Table 215. OTP_V1_CFG9 register bit description

Bit	Symbol	Description
0	VBOS2V1_SW_LP_EN_OTP	**Control VBOS to V1 switch in LPON mode when V1 = BUCK (the switch is kept open when V1 = LDO)**
		0 VBOS to V1 switch is open in LPON mode
		1 VBOS to V1 switch is closed in LPON mode
		Reset on power-on reset
1	CONF_OC_TO_V1_OTP	**Select V1 LDO overcurrent time out to protect the external PNP**
		0 V1 PNP OC time out = 10 ms
		1 V1 PNP OC time out = 1 ms
		Reset on power-on reset
2	VV1_LDO_OTP	**Select V1 LDO regulator output voltage**
		0 V1 = 3.3 V
		1 V1 = 5.0 V
		Reset on power-on reset
3	CONF_OC_V1_OTP	**Select V1 LDO overcurrent threshold**
		0 V1 LDO OC = 150 mA
		1 V1 LDO OC = 75 mA
		Reset on power-on reset

Table 215. OTP_V1_CFG9 register bit description...*continued*

Bit	Symbol	Description
4	CONF_TSD_V1_OTP	**Select the device reaction in case of V1 thermal shutdown detection**
		0 V1 regulator is disabled in case of TSD
		1 V1 regulator is disabled and the device transitions to Fail-Safe state (M30) in case of TSD
		Reset on power-on reset
5	CONF_OV_V1_OTP	**Select the device reaction in case of V1 overvoltage detection**
		0 V1 regulator is disabled in case of OV
		1 V1 regulator is disabled and the device transitions to Fail-Safe state (M30) in case of OV
		Reset on power-on reset
6	V1MON_OTP	**Select V1 VMON input voltage**
		0 V1MON = 3.3 V
		1 V1MON = 5.0 V
		Reset on power-on reset
7	VBOS2V1_SW_ ALWAYS_EN_OTP	**Control VBOS to V1 switch in Normal and LPON modes when V1 = BUCK (the switch is kept open when V1 = LDO)**
		0 VBOS to V1 switch is open in Normal mode
		1 VBOS to V1 switch is closed in Normal and LPON mode (possible only when V1 = 5 V in Normal mode)
		Reset on power-on reset

24.13 OTP_V2_CFG

Table 216. OTP_V2_CFG register bit allocation

Bit	7	6	5	4	3	2	1	0
Write	Reserved	V2MON_ OTP	CONF_OV_ V2_OTP	CONF_TSD_ V2_OTP	CONF_OC_ V2_OTP	VV2_OTP	V2_SLOT_OTP	
Read								
Reset	0	0	0	0	0	0	0	0

Table 217. OTP_V2_CFG register bit description

Bit	Symbol	Description
0 to 1	V2_SLOT_OTP	**Select the power sequence slot for V2**
		00 V2 starts and stops in slot 0
		01 V2 starts and stops in slot 1
		10 V2 starts and stops in slot 2
		11 V2 does not start in a slot (enabled by SPI / I²C)
		Reset on power-on reset

Table 217. OTP_V2_CFG register bit description*...continued*

Bit	Symbol	Description
2	VV2_OTP	**Select V2 LDO regulator output voltage**
		0 V2 = 3.3 V
		1 V2 = 5.0 V
		Reset on power-on reset
3	CONF_OC_V2_OTP	**Select V2 LDO overcurrent threshold**
		0 V2 LDO OC = 150 mA
		1 V2 LDO OC = 75 mA
		Reset on power-on reset
4	CONF_TSD_ V2_OTP	**Select the device reaction in case of V2 thermal shutdown detection**
		0 V2 regulator is disabled in case of TSD
		1 V2 regulator is disabled and the device transitions to Fail-Safe state (M30) in case of TSD
		Reset on power-on reset
5	CONF_OV_V2_OTP	**Select the device reaction in case of V2 overvoltage detection**
		0 V2 regulator is disabled in case of OV
		1 V2 regulator is disabled and the device transitions to Fail-Safe state (M30) in case of OV
		Reset on power-on reset
6	V2MON_OTP	**Select V2 VMON input voltage**
		0 V2MON = 3.3 V
		1 V2MON = 5.0 V
		Reset on power-on reset

24.14 OTP_V3_CFG

Table 218. OTP_V3_CFG register bit allocation

Bit	7	6	5	4	3	2	1	0
Write	Reserved	V3MON_ OTP	CONF_OV_ V3_OTP	CONF_ TSD_ V3_OTP	CONF_OC_ V3_OTP	VV3_OTP	V3_SLOT_OTP	
Read								
Reset	0	0	0	0	0	0	0	0

Table 219. OTP_V3_CFG register bit description

Bit	Symbol	Description
0 to 1	V3_SLOT_OTP	**Select the power sequence slot for V3**
		00 V3 starts and stops in slot 0
		01 V3 starts and stops in slot 1
		10 V3 starts and stops in slot 2
		11 V3 does not start in a slot (enabled by SPI / I²C)
		Reset on power-on reset
2	VV3_OTP	**Select V3 LDO regulator output voltage**
		0 V3 = 3.3 V
		1 V3 = 5.0 V
		Reset on power-on reset
3	CONF_OC_ V3_OTP	**Select V3 LDO overcurrent threshold**
		0 V3 LDO OC = 150 mA
		1 V3 LDO OC = 75 mA
		Reset on power-on reset
4	CONF_TSD_ V3_OTP	**Select the device reaction in case of V3 thermal shutdown detection**
		0 V3 regulator is disabled in case of TSD
		1 V3 regulator is disabled and the device transitions to Fail-Safe state (M30) in case of TSD
		Reset on power-on reset
5	CONF_OV_ V3_OTP	**Select the device reaction in case of V3 overvoltage detection**
		0 V3 regulator is disabled in case of OV
		1 V3 regulator is disabled and the device transitions to Fail-Safe state (M30) in case of OV
		Reset on power-on reset
6	V3MON_OTP	**Select V3 VMON input voltage**
		0 V3MON = 3.3 V
		1 V3MON = 5.0 V
		Reset on power-on reset

24.15 OTP_HVIO_CFG1

Table 220. OTP_HVIO_CFG1 register bit allocation

Bit	7	6	5	4	3	2	1	0
Write	WK1PUPD_OTP		WK2PUPD_OTP		HVIO1_SLOT_OTP		HVIO2_SLOT_OTP	
Read								
Reset	0	0	0	0	0	0	0	0

Table 221. OTP_HVIO_CFG1 register bit description

Bit	Symbol	Description
0 to 1	HVIO2_SLOT_OTP	**Select the power sequence slot for HVIO2**
		00 HVIO2 polarity is changed in slot 0
		01 HVIO2 polarity is changed in slot 1
		10 HVIO2 polarity is changed in slot 2
		11 HVIO2 is not released in a slot (enabled by SPI / I²C)
		Reset on power-on reset
2 to 3	HVIO1_SLOT_OTP	**Select the power sequence slot for HVIO1**
		00 HVIO1 polarity is changed in slot 0
		01 HVIO1 polarity is changed in slot 1
		10 HVIO1 polarity is changed in slot 2
		11 HVIO1 is not released in a slot (enabled by SPI/I^{2}C)
		Reset on power-on reset
4 to 5	WK2PUPD_OTP	**Select the pull down on WAKE2 pin**
		00 WAKE2 internal pull down and pull up are configured as cell repeater
		01 WAKE2 internal pull down is enabled and pull up is disabled
		10 WAKE2 internal pull down is disabled and pull up is enabled
		11 WAKE2 internal pull down and pull up are disabled
		Reset on power-on reset
6 to 7	WK1PUPD_OTP	**Select the pull down on WAKE1 pin**
		00 WAKE1 internal pull down and pull up are configured as cell repeater
		01 WAKE1 internal pull down is enabled and pull up is disabled
		10 WAKE1 internal pull down is disabled and pull up is enabled
		11 WAKE1 internal pull down and pull up are disabled
		Reset on power-on reset

24.16 OTP_HVIO_CFG2

Table 222. OTP_HVIO_CFG2 register bit allocation

Bit	7	6	5	4	3	2	1	0
Write / Read	HVIO1_ OUT_ EN_OTP	HVIO1_ OUT_ DFLT_OTP	HVIO1PUPD_OTP		HVIO2_ OUT_ EN_OTP	HVIO2_ OUT_ DFLT_OTP	HVIO2PUPD_OTP	
Reset	0	0	0	0	0	0	0	0

Table 223. OTP_HVIO_CFG2 register bit description

Bit	Symbol	Description
0 to 1	HVIO2PUPD_OTP	**Select the pull down on HVIO2 pin**
		00 HVIO2 internal pull down and pull up are configured as cell repeater
		01 HVIO2 internal pull down is enabled and pull up is disabled
		10 HVIO2 internal pull down is disabled and pull up is enabled
		11 HVIO2 internal pull down and pull up are disabled
		Reset on power-on reset
2	HVIO2_OUT_DFLT_OTP	**Configure the HVIO2 pin default state when HVIO2 is an output**
		0 HVIO2 default state is low (asserted)
		1 HVIO2 default state is high (HIZ)
		Reset on power-on reset
3	HVIO2_OUT_EN_OTP	**Configure the HVIO2 pin as an output**
		0 HVIO2 is configured as an input
		1 HVIO2 is configured as an output
		Reset on power-on reset
4 to 5	HVIO1PUPD_OTP	**Select the pull down on HVIO1 pin**
		00 HVIO1 internal pull down and pull up are configured as cell repeater
		01 HVIO1 internal pull down is enabled and pull up is disabled
		10 HVIO1 internal pull down is disabled and pull up is enabled
		11 HVIO1 internal pull down and pull up are disabled
		Reset on power-on reset
6	HVIO1_OUT_DFLT_OTP	**Configure the HVIO1 pin default state when HVIO1 is an output**
		0 HVIO1 default state is low (asserted)
		1 HVIO1 default state is high (HIZ)
		Reset on power-on reset
7	HVIO1_OUT_EN_OTP	**Configure the HVIO1 pin as an output**
		0 HVIO1 is configured as an input
		1 HVIO1 is configured as an output
		Reset on power-on reset

24.17 OTP_LVIO_CFG1

Table 224. OTP_LVIO_CFG1 register bit allocation

Bit	7	6	5	4	3	2	1	0
Write / Read	LVIO4_OUT_DFT_OTP	LVIO3_OUT_DFT_OTP	LVIO3PUPD_OTP		LVIO3_LS_EN_OTP	LVIO3_HS_EN_OTP	LVIO3_SLOT_OTP	
Reset	0	0	0	0	0	0	0	0

Table 225. OTP_LVIO_CFG1 register bit description

Bit	Symbol	Description
0 to 1	LVIO3_SLOT_OTP	**Select the power sequence slot for LVIO3**
		00 LVIO3 polarity is changed in slot 0
		01 LVIO3 polarity is changed in slot 1
		10 LVIO3 polarity is changed in slot 2
		11 LVIO3 is not released in a slot (enabled by SPI / I²C)
		Reset on power-on reset
2	LVIO3_HS_EN_OTP	**Enable the HS of LVIO3**
		0 LVIO3 HS is disabled
		1 LVIO3 HS is enabled
		Reset on power-on reset
3	LVIO3_LS_EN_OTP	**Enable the LS of LVIO3**
		0 LVIO3 LS is disabled
		1 LVIO3 LS is enabled
		Reset on power-on reset
4 to 5	LVIO3PUPD_OTP	**Select the pull down on LVIO3 pin**
		00 LVIO3 internal pull down and pull up are configured as cell repeater
		01 LVIO3 internal pull down is enabled and pull up is disabled
		10 LVIO3 internal pull down is disabled and pull up is enabled
		11 LVIO3 internal pull down and pull up are disabled
		Reset on power-on reset
6	LVIO3_OUT_DFT_OTP	**Configure the LVIO3 pin default state when LVIO3 is an output**
		0 LVIO3 default state is low (LS ON or LS OFF with ext. PD)
		1 LVIO3 default state is high (HS ON or HS OFF with ext. PU)
		Reset on power-on reset
7	LVIO4_OUT_DFT_OTP	**Configure the LVIO4 pin default state when LVIO4 is an output**
		0 LVIO4 default state is low (LS ON or LS OFF with ext. PD)
		1 LVIO4 default state is high (HS ON or HS OFF with ext. PU)
		Reset on power-on reset

24.18 OTP_LVIO_CFG2

Table 226. OTP_LVIO_CFG2 register bit allocation

Bit	7	6	5	4	3	2	1	0
Write	LVI5PUPD_OTP		LVIO4PUPD_OTP		LVIO4_LS_EN_OTP	LVIO4_HS_EN_OTP	LVIO4_SLOT_OTP	
Read								
Reset	0	0	0	0	0	0	0	0

Table 227. OTP_LVIO_CFG2 register bit description

Bit	Symbol	Description
0 to 1	LVIO4_SLOT_OTP	**Select the power sequence slot for LVIO4**
		00 LVIO4 polarity is changed in slot 0
		01 LVIO4 polarity is changed in slot 1
		10 LVIO4 polarity is changed in slot 2
		11 LVIO4 is not released in a slot (enabled by SPI / I²C)
		Reset on power-on reset
2	LVIO4_HS_EN_OTP	**Enable the HS of LVIO4**
		0 LVIO4 HS is disabled
		1 LVIO4 HS is enabled
		Reset on power-on reset
3	LVIO4_LS_EN_OTP	**Enable the LS of LVIO4**
		0 LVIO4 LS is disabled
		1 LVIO4 LS is enabled
		Reset on power-on reset
4 to 5	LVIO4PUPD_OTP	**Select the pull down on LVIO4 pin**
		00 LVIO4 internal pull down and pull up are configured as cell repeater
		01 LVIO4 internal pull down is enabled and pull up is disabled
		10 LVIO4 internal pull down is disabled and pull up is enabled
		11 LVIO4 internal pull down and pull up are disabled
		Reset on power-on reset
6 to 7	LVI5PUPD_OTP	**Select the pull down on LVI5 pin**
		00 LVI5 internal pull down and pull up are configured as cell repeater
		01 LVI5 internal pull down is enabled and pull up is disabled (possible config when LVI5 is used as MOSI pin)
		10 LVI5 internal pull down is disabled and pull up is enabled (default config when LVI5 is used as MOSI pin)
		11 LVI5 internal pull down and pull up are disabled
		Reset on power-on reset

24.19 OTP_IO_OUT_SEL_CFG

Table 228. OTP_IO_OUT_SEL_CFG register bit allocation

Bit	7	6	5	4	3	2	1	0
Write	Reserved	Reserved	HS3_ SEL_ OTP	HS1_ SEL_ OTP	LVO4_ SEL_OTP	LVO3_ SEL_OTP	HVO2_ SEL_OTP	HVO1_ SEL_OTP
Read								
Reset	0	0	0	0	0	0	0	0

Table 229. OTP_IO_OUT_SEL_CFG register bit description

Bit	Symbol	Description
0	HVO1_SEL_OTP	**Select the function assigned to HVIO1 when configured as output**
		0 HVO1 is connected to alternate function (SLOT by OTP or control by SPI / I^2C)
		1 HVO1 is connected to LIMP1 function
		Reset on power-on reset
1	HVO2_SEL_OTP	**Select the function assigned to HVIO2 when configured as output**
		0 HVO2 is connected to alternate function (SLOT by OTP or control by SPI / I^2C)
		1 HVO2 is connected to LIMP2 function
		Reset on power-on reset
2	LVO3_SEL_OTP	**Select the function assigned to LVIO3 when configured as output**
		0 LVO3 is connected to alternate function (SLOT by OTP or control by SPI / I^2C)
		1 LVO3 is connected to LIMP1 function
		Reset on power-on reset
3	LVO4_SEL_OTP	**Select the function assigned to LVIO4 when configured as output**
		0 LVO4 is connected to alternate function (SLOT by OTP or control by SPI/I^2C)
		1 LVO4 is connected to LIMP2 function
		Reset on power-on reset
4	HS1_SEL_OTP	**Select the function assigned to HS1**
		0 HS1 is connected to HS1 driver
		1 HS1 is connected to LIMP1 function
		Reset on power-on reset
5	HS3_SEL_OTP	**Select the function assigned to HS3**
		0 HS3 is connected to HS3 driver
		1 HS3 is connected to LIMP2 function
		Reset on power-on reset

24.20 OTP_MAIN_SYS_I2C_CFG

Table 230. OTP_MAIN_SYS_I2C_CFG register bit allocation

Bit	7	6	5	4	3	2	1	0
Write / Read	MOD_CONF_OTP	MOD_EN_OTP	SLOT_BYP_OTP	SPI_EN_OTP	I2CDEVADDR_OTP			
Reset	0	0	0	0	0	0	0	0

Table 231. OTP_MAIN_SYS_I2C_CFG register bit description

Bit	Symbol	Description
0 to 3	I2CDEVADDR_ OTP[3:0]	**Configure the I2C address**
		0000 I2C address is 0x20
		0001 I2C address is 0x22
		0010 I2C address is 0x24
		0011 I2C address is 0x26
		0100 I2C address is 0x28
		0101 I2C address is 0x2A
		0110 I2C address is 0x2C
		0111 I2C address is 0x2E
		1000 I2C address is 0x30
		1001 I2C address is 0x32
		1010 I2C address is 0x34
		1011 I2C address is 0x36
		1100 I2C address is 0x38
		1101 I2C address is 0x3A
		1110 I2C address is 0x3C
		1111 I2C address is 0x3E
		Reset on power-on reset
4	SPI_EN_OTP	**Enable the SPI or I2C hardware pins**
		0 I2C pins are enabled
		1 SPI pins are enabled
		Reset on power-on reset
5	SLOT_BYP_OTP	**Bypass the power sequence Slot 1 and Slot 2 after wake-up from LPON**
		0 Slot 1 and Slot 2 are not bypassed
		1 Slot 1 and Slot 2 are bypassed when waking up from LPON
		Reset on power-on reset
6	MOD_EN_OTP	**Enable clock modulation on 20 MHz clock**
		0 Modulation is disabled
		1 Modulation is enabled
		Reset on power-on reset
7	MOD_CONF_OTP	**Select clock modulation configuration**
		0 Triangular modulation is selected
		1 Pseudo-random modulation is selected
		Reset on power-on reset

24.21 OTP_FS_SYS_CFG

Table 232. OTP_FS_SYS_CFG register bit allocation

Bit	7	6	5	4	3	2	1	0
Write / Read	Reserved	Reserved	INIT_CRC_DIS_OTP	FS_LPOFF_OTP	FS_DUR_CFG_OTP	WD_INF_OTP	RSTB8S_DIS_OTP	FIRST_FAULT_EN_OTP
Reset	0	0	0	0	0	0	0	0

Table 233. OTP_FS_SYS_CFG register bit description

Bit	Symbol	Description
0	FIRST_FAULT_EN_OTP	**Configure the first fault to send the device in Fail-Safe mode**
		0 Do not go to FS at first fault
		1 Go to FS at first fault
		Reset on power-on reset
1	RSTB8S_DIS_OTP	**Disable the RSTB 8s timer**
		0 RSTB 8 s timer is enabled
		1 RSTB 8 s timer is disabled
		Reset on power-on reset
2	WD_INF_OTP	**Set the watchdog period as infinite**
		0 Watchdog period is configurable by SPI/I^2C
		1 Watchdog period is infinite
		Reset on power-on reset
3	FS_DUR_CFG_OTP	**Configure FS state duration**
		0 FS state duration is 100 ms
		1 FS state duration is 4 s
		Reset on power-on reset
4	FS_LPOFF_OTP	**Configure FS state exit**
		0 Automatic restart after FS state
		1 Go to LPOFF after FS state
		Reset on power-on reset
5	INIT_CRC_DIS_OTP	**Disable the INIT registers CRC protection**
		0 CRC is enabled
		1 CRC is disabled
		Reset on power-on reset

24.22 OTP_OVUV_CFG1

Table 234. OTP_OVUV_CFG1 register bit allocation

Bit	7	6	5	4	3	2	1	0
Write	V1MON_UVTH_OTP				V1MON_OVTH_OTP			
Read								
Reset	0	0	0	0	0	0	0	0

Table 235. OTP_OVUV_CFG1 register bit description

Bit	Symbol	Description
0 to 3	V1MON_OVTH_OTP	**Select V1MON OV threshold**
		0000 V1MON OV = 102.5 %
		0001 V1MON OV = 103 %
		0010 V1MON OV = 103.5 %
		0011 V1MON OV = 104 %
		0100 V1MON OV = 104.5 %
		0101 V1MON OV = 105 %
		0110 V1MON OV = 105.5 %
		0111 V1MON OV = 106 %
		1000 V1MON OV = 106.5 %
		1001 V1MON OV = 107 %
		1010 V1MON OV = 107.5 %
		1011 V1MON OV = 108 %
		1100 V1MON OV = 108.5 %
		1101 V1MON OV = 109 %
		1110 V1MON OV = 109.5 %
		1111 V1MON OV = 110 %
		Reset on power-on reset
4 to 7	V1MON_UVTH_OTP	**Select V1MON UV threshold**
		0000 V1MON UV = 64 %
		0001 V1MON UV = 63 %
		0010 V1MON UV = 96.5 %
		0011 V1MON UV = 96 %
		0100 V1MON UV = 95.5 %
		0101 V1MON UV = 95 %
		0110 V1MON UV = 94.5 %
		0111 V1MON UV = 94 %
		1000 V1MON UV = 93.5 %

Table 235. OTP_OVUV_CFG1 register bit description*...continued*

Bit	Symbol	Description
		1001 V1MON UV = 93 %
		1010 V1MON UV = 92.5 %
		1011 V1MON UV = 92 %
		1100 V1MON UV = 91.5 %
		1101 V1MON UV = 62.5 %
		1110 V1MON UV = 62 %
		1111 V1MON UV = 61 %
		Reset on power-on reset

24.23 OTP_OVUV_CFG2

Table 236. OTP_OVUV_CFG2 register bit allocation

Bit	7	6	5	4	3	2	1	0
Write	V2MON_UVTH_OTP				V2MON_OVTH_OTP			
Read								
Reset	0	0	0	0	0	0	0	0

Table 237. OTP_OVUV_CFG2 register bit description

Bit	Symbol	Description
0 to 3	V2MON_ OVTH_OTP	**Select V2MON OV threshold**
		0000 V2MON OV = 102.5 %
		0001 V2MON OV = 103 %
		0010 V2MON OV = 103.5 %
		0011 V2MON OV = 104 %
		0100 V2MON OV = 104.5 %
		0101 V2MON OV = 105 %
		0110 V2MON OV = 105.5 %
		0111 V2MON OV = 106 %
		1000 V2MON OV = 106.5 %
		1001 V2MON OV = 107 %
		1010 V2MON OV = 107.5 %
		1011 V2MON OV = 108 %
		1100 V2MON OV = 108.5 %
		1101 V2MON OV = 109 %
		1110 V2MON OV = 109.5 %
		1111 V2MON OV = 110 %
		Reset on power-on reset

Table 237. OTP_OVUV_CFG2 register bit description*...continued*

Bit	Symbol	Description
4 to 7	V2MON_ UVTH_OTP	**Select V2MON UV threshold**
		0000 V2MON UV = 64 %
		0001 V2MON UV = 63 %
		0010 V2MON UV = 96.5 %
		0011 V2MON UV = 96 %
		0100 V2MON UV = 95.5 %
		0101 V2MON UV = 95 %
		0110 V2MON UV = 94.5 %
		0111 V2MON UV = 94 %
		1000 V2MON UV = 93.5 %
		1001 V2MON UV = 93 %
		1010 V2MON UV = 92.5 %
		1011 V2MON UV = 92 %
		1100 V2MON UV = 91.5 %
		1101 V2MON UV = 62.5 %
		1110 V2MON UV = 62 %
		1111 V2MON UV = 61 %
		Reset on power-on reset

24.24 OTP_OVUV_CFG3

Table 238. OTP_OVUV_CFG3 register bit allocation

Bit	7	6	5	4	3	2	1	0
Write	V3MON_UVTH_OTP				V3MON_OVTH_OTP			
Read								
Reset	0	0	0	0	0	0	0	0

Table 239. OTP_OVUV_CFG3 register bit description

Bit	Symbol	Description
0 to 3	V3MON_ OVTH_OTP	**Select V3MON OV threshold**
		0000 V3MON OV = 102.5 %
		0001 V3MON OV = 103 %
		0010 V3MON OV = 103.5 %
		0011 V3MON OV = 104 %
		0100 V3MON OV = 104.5 %
		0101 V3MON OV = 105 %
		0110 V3MON OV = 105.5 %

Table 239. OTP_OVUV_CFG3 register bit description...*continued*

Bit	Symbol	Description
		0111 V3MON OV = 106 %
		1000 V3MON OV = 106.5 %
		1001 V3MON OV = 107 %
		1010 V3MON OV = 107.5 %
		1011 V3MON OV = 108 %
		1100 V3MON OV = 108.5 %
		1101 V3MON OV = 109 %
		1110 V3MON OV = 109.5 %
		1111 V3MON OV = 110 %
		Reset on power-on reset
4 to 7	V3MON_ UVTH_OTP	**Select V3MON UV threshold**
		0000 V3MON UV = 64 %
		0001 V3MON UV = 63 %
		0010 V3MON UV = 96.5 %
		0011 V3MON UV = 96 %
		0100 V3MON UV = 95.5 %
		0101 V3MON UV = 95 %
		0110 V3MON UV = 94.5 %
		0111 V3MON UV = 94 %
		1000 V3MON UV = 93.5 %
		1001 V3MON UV = 93 %
		1010 V3MON UV = 92.5 %
		1011 V3MON UV = 92 %
		1100 V3MON UV = 91.5 %
		1101 V3MON UV = 62.5 %
		1110 V3MON UV = 62 %
		1111 V3MON UV = 61 %
		Reset on power-on reset

24.25 OTP_OVUV_CFG4

Table 240. OTP_OVUV_CFG4 register bit allocation

Bit	7	6	5	4	3	2	1	0
Write	V0MON_UVTH_OTP				V0MON_OVTH_OTP			
Read								
Reset	0	0	0	0	0	0	0	0

Table 241. OTP_OVUV_CFG4 register bit description

Bit	Symbol	Description
0 to 3	V0MON_ OVTH_OTP	**Select V0MON OV threshold**
		0000 V0MON OV = 102.5 %
		0001 V0MON OV = 103 %
		0010 V0MON OV = 103.5 %
		0011 V0MON OV = 104 %
		0100 V0MON OV = 104.5 %
		0101 V0MON OV = 105 %
		0110 V0MON OV = 105.5 %
		0111 V0MON OV = 106 %
		1000 V0MON OV = 106.5 %
		1001 V0MON OV = 107 %
		1010 V0MON OV = 107.5 %
		1011 V0MON OV = 108 %
		1100 V0MON OV = 108.5 %
		1101 V0MON OV = 109 %
		1110 V0MON OV = 109.5 %
		1111 V0MON OV = 110 %
		Reset on power-on reset
4 to 7	V0MON_ UVTH_OTP	**Select V0MON UV threshold**
		0000 V0MON UV = 64 %
		0001 V0MON UV = 63 %
		0010 V0MON UV = 96.5 %
		0011 V0MON UV = 96 %
		0100 V0MON UV = 95.5 %
		0101 V0MON UV = 95 %
		0110 V0MON UV = 94.5 %
		0111 V0MON UV = 94 %
		1000 V0MON UV = 93.5 %
		1001 V0MON UV = 93 %
		1010 V0MON UV = 92.5 %
		1011 V0MON UV = 92 %
		1100 V0MON UV = 91.5 %
		1101 V0MON UV = 62.5 %
		1110 V0MON UV = 62 %
		1111 V0MON UV = 61 %
		Reset on power-on reset

24.26 OTP_UV_DGLT_CFG

Table 242. OTP_UV_DGLT_CFG register bit allocation

Bit	7	6	5	4	3	2	1	0
Write	V0MON_UVDGLT_OTP		V1MON_UVDGLT_OTP		V2MON_UVDGLT_OTP		V3MON_UVDGLT_OTP	
Read								
Reset	0	0	0	0	0	0	0	0

Table 243. OTP_UV_DGLT_CFG register bit description

Bit	Symbol	Description
0 to 1	V3MON_ UVDGLT_OTP	**Select V3MON UV deglitcher time**
		00 V3MON UV deglitcher = 5 µs
		01 V3MON UV deglitcher = 15 µs
		10 V3MON UV deglitcher = 25 µs
		11 V3MON UV deglitcher = 40 µs
		Reset on power-on reset
2 to 3	V2MON_ UVDGLT_OTP	**Select V2MON UV deglitcher time**
		00 V2MON UV deglitcher = 5 µs
		01 V2MON UV deglitcher = 15 µs
		10 V2MON UV deglitcher = 25 µs
		11 V2MON UV deglitcher = 40 µs
		Reset on power-on reset
4 to 5	V1MON_ UVDGLT_OTP	**Select V1MON UV deglitcher time**
		00 V1MON UV deglitcher = 5 µs
		01 V1MON UV deglitcher = 15 µs
		10 V1MON UV deglitcher = 25 µs
		11 V1MON UV deglitcher = 40 µs
		Reset on power-on reset
6 to 7	V0MON_ UVDGLT_OTP	**Select V0MON UV deglitcher time (VMON_EXT)**
		00 V0MON UV deglitcher = 5 µs
		01 V0MON UV deglitcher = 15 µs
		10 V0MON UV deglitcher = 25 µs
		11 V0MON UV deglitcher = 40 µs
		Reset on power-on reset

24.27 OTP_LIMP_OV_DGLT_CFG

Table 244. OTP_LIMP_OV_DGLT_CFG register bit allocation

Bit	7	6	5	4	3	2	1	0
Write	LIMP2_CFG_OTP		LIMP1_CFG_OTP		V0MON_ OVDGLT_OTP	V1MON_ OVDGLT_OTP	V2MON_ OVDGLT_OTP	V3MON_ OVDGLT_OTP
Read								
Reset	0	0	0	0	0	0	0	0

Table 245. OTP_LIMP_OV_DGLT_CFG register bit description

Bit	Symbol	Description
0	V3MON_OVDGLT_OTP	**Select V3MON OV deglitcher time**
		0 V3MON OV deglitcher = 25 µs
		1 V3MON OV deglitcher = 45 µs
		Reset on power-on reset
1	V2MON_OVDGLT_OTP	**Select V2MON OV deglitcher time**
		0 V2MON OV deglitcher = 25 µs
		1 V2MON OV deglitcher = 45 µs
		Reset on power-on reset
2	V1MON_OVDGLT_OTP	**Select V1MON OV deglitcher time**
		0 V1MON OV deglitcher = 25 µs
		1 V1MON OV deglitcher = 45 µs
		RESET ON POWER ON RESET
3	V0MON_OVDGLT_OTP	**Select V0MON OV deglitcher time (VMON_EXT)**
		0 V0MON OV deglitcher = 25 µs
		1 V0MON OV deglitcher = 45 µs
		Reset on power-on reset
4 to 5	LIMP1_CFG_OTP	**Select LIMP1 polarity or PWM frequency**
		00 PWM frequency = 1.25 Hz with 50 % duty cycle (default high)
		01 Default high (Active low)
		10 PWM frequency = 1.25 Hz with 50 % duty cycle (default low)
		11 Default low (Active high)
		Reset on power-on reset
6 to 7	LIMP2_CFG_OTP	**Select LIMP2 polarity or PWM frequency**
		00 PWM frequency = 100 Hz (default high)
		01 Default high (Active low)
		10 PWM frequency = 100 Hz (default low)
		11 Default low (Active high)
		Reset on power-on reset

24.28 OTP_RSTB_IMPACT_CFG

Table 246. OTP_RSTB_IMPACT_CFG register bit allocation

Bit	7	6	5	4	3	2	1	0
Write	V0UV_RSTB_ IMPACT_ OTP	V0OV_RSTB_ IMPACT_ OTP	V1UV_RSTB_ IMPACT_ OTP	V1OV_RSTB_ IMPACT_ OTP	V2UV_RSTB_ IMPACT_ OTP	V2OV_RSTB_ IMPACT_ OTP	V3UV_RSTB_ IMPACT_ OTP	V3OV_RSTB_ IMPACT_ OTP
Read								
Reset	0	0	0	0	0	0	0	0

Table 247. OTP_RSTB_IMPACT_CFG register bit description

Bit	Symbol	Description
0	V3OV_RSTB_IMPACT_OTP	**Configure V3 OV impact on RSTB**
		0 V3 OV does not assert RSTB
		1 V3 OV asserts RSTB
		Reset on power-on reset
1	V3UV_RSTB_IMPACT_OTP	**Configure V3 UV impact on RSTB**
		0 V3 UV does not assert RSTB
		1 V3 UV asserts RSTB
		Reset on power-on reset
2	V2OV_RSTB_IMPACT_OTP	**Configure V2 OV impact on RSTB**
		0 V2 OV does not assert RSTB
		1 V2 OV asserts RSTB
		Reset on power-on reset
3	V2UV_RSTB_IMPACT_OTP	**Configure V2 UV impact on RSTB**
		0 V2 UV does not assert RSTB
		1 V2 UV asserts RSTB
		Reset on power-on reset
4	V1OV_RSTB_IMPACT_OTP	**Configure V1 OV impact on RSTB**
		0 V1 OV does not assert RSTB
		1 V1 OV asserts RSTB
		Reset on power-on reset
5	V1UV_RSTB_IMPACT_OTP	**Configure V1 UV impact on RSTB**
		0 V1 UV does not assert RSTB
		1 V1 UV asserts RSTB
		Reset on power-on reset
6	V0OV_RSTB_IMPACT_OTP	**Configure VMON_EXT OV impact on RSTB**
		0 VMON_EXT OV does not assert RSTB
		1 VMON_EXT OV asserts RSTB
		Reset on power-on reset
7	V0UV_RSTB_IMPACT_OTP	**Configure VMON_EXT UV impact on RSTB**
		0 VMON_EXT UV does not assert RSTB
		1 VMON_EXT UV asserts RSTB
		Reset on power-on reset

25 Application information

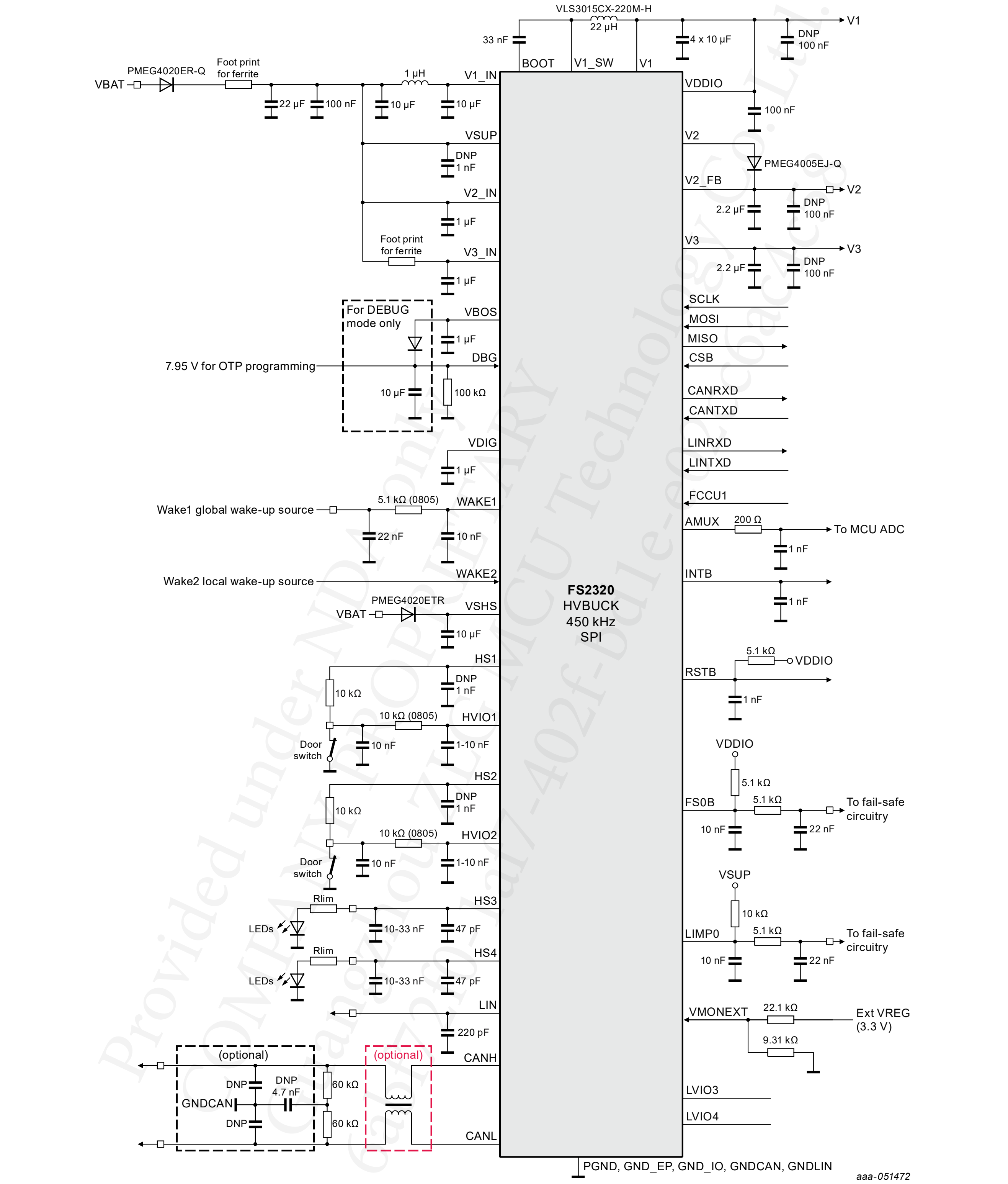


Figure 54. Example of application schematic with 450 kHz HVBUCK version, SPI interface

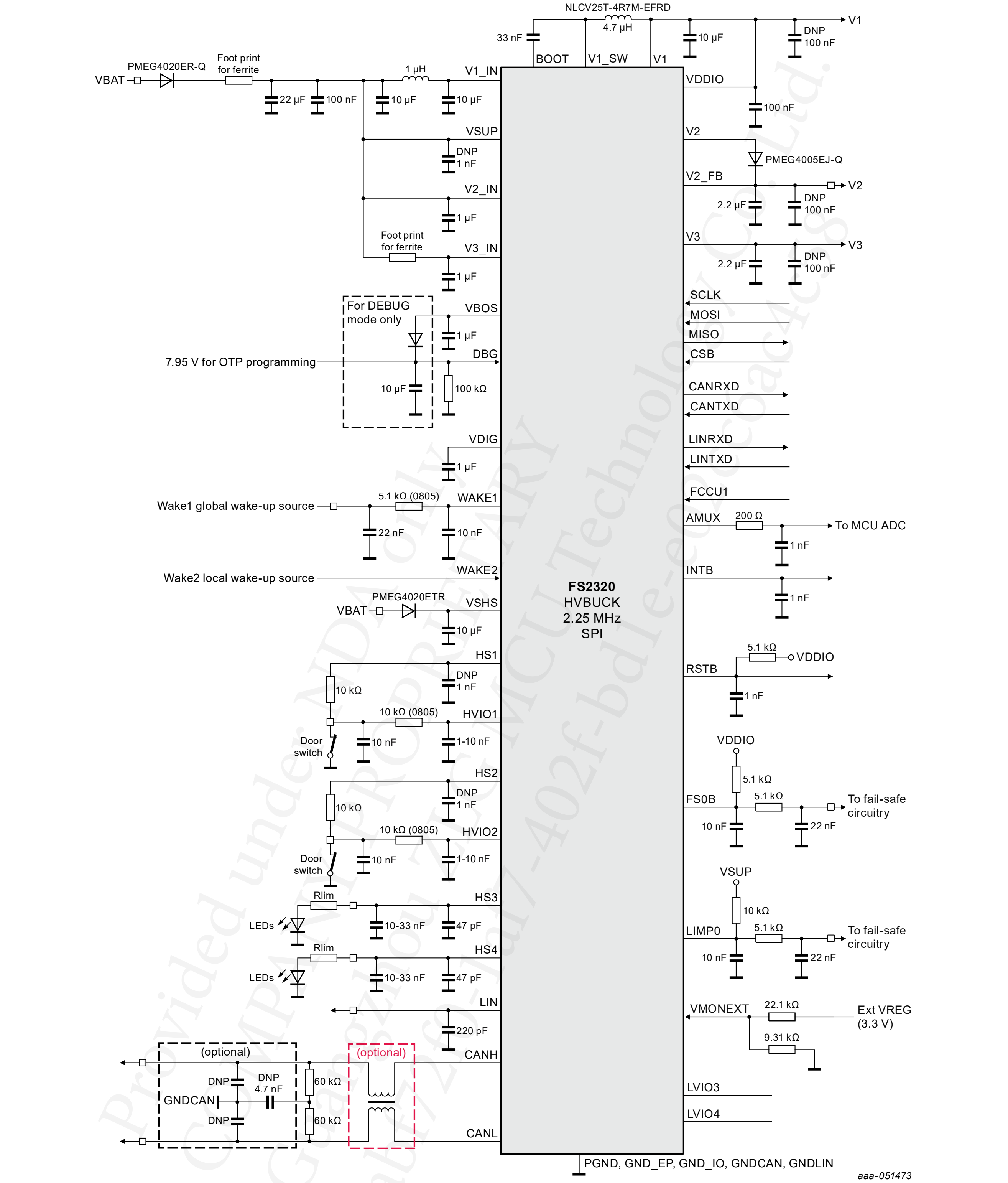


Figure 55. Example of application schematic with 2.25 MHz HVBUCK version, SPI interface

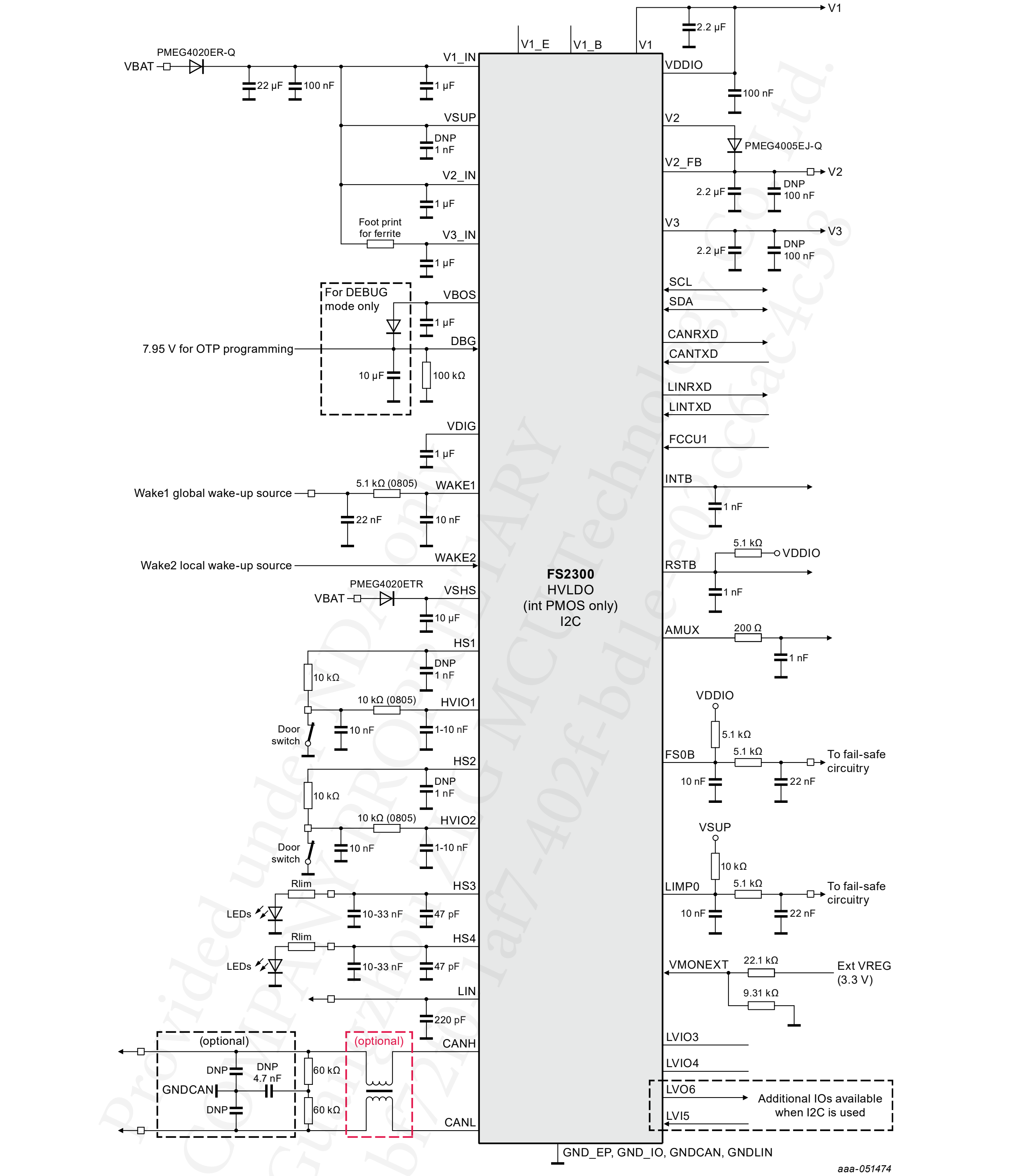


Figure 56. Example of application schematic, HVLDO1 version with internal PMOS only, I2C interface

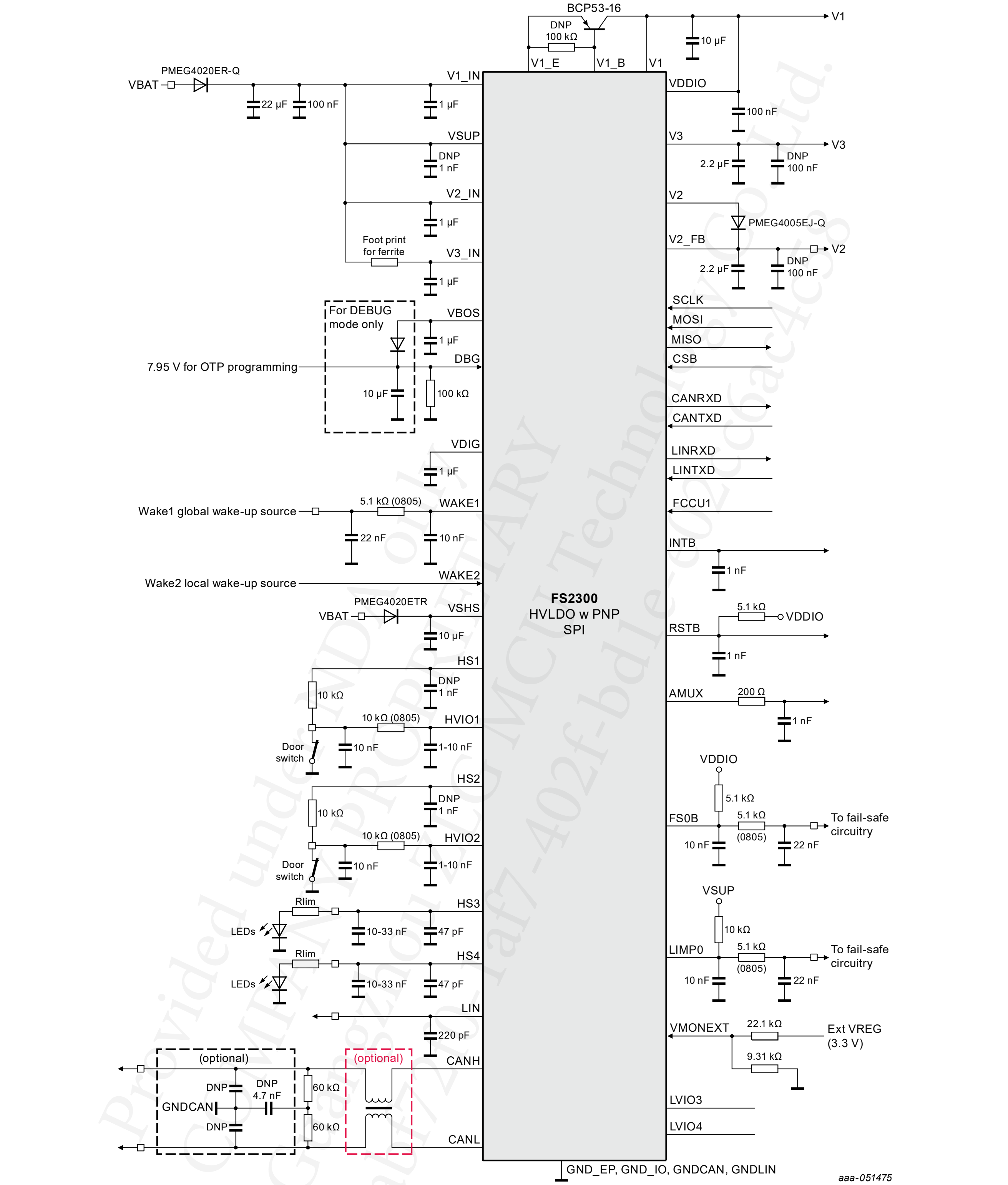
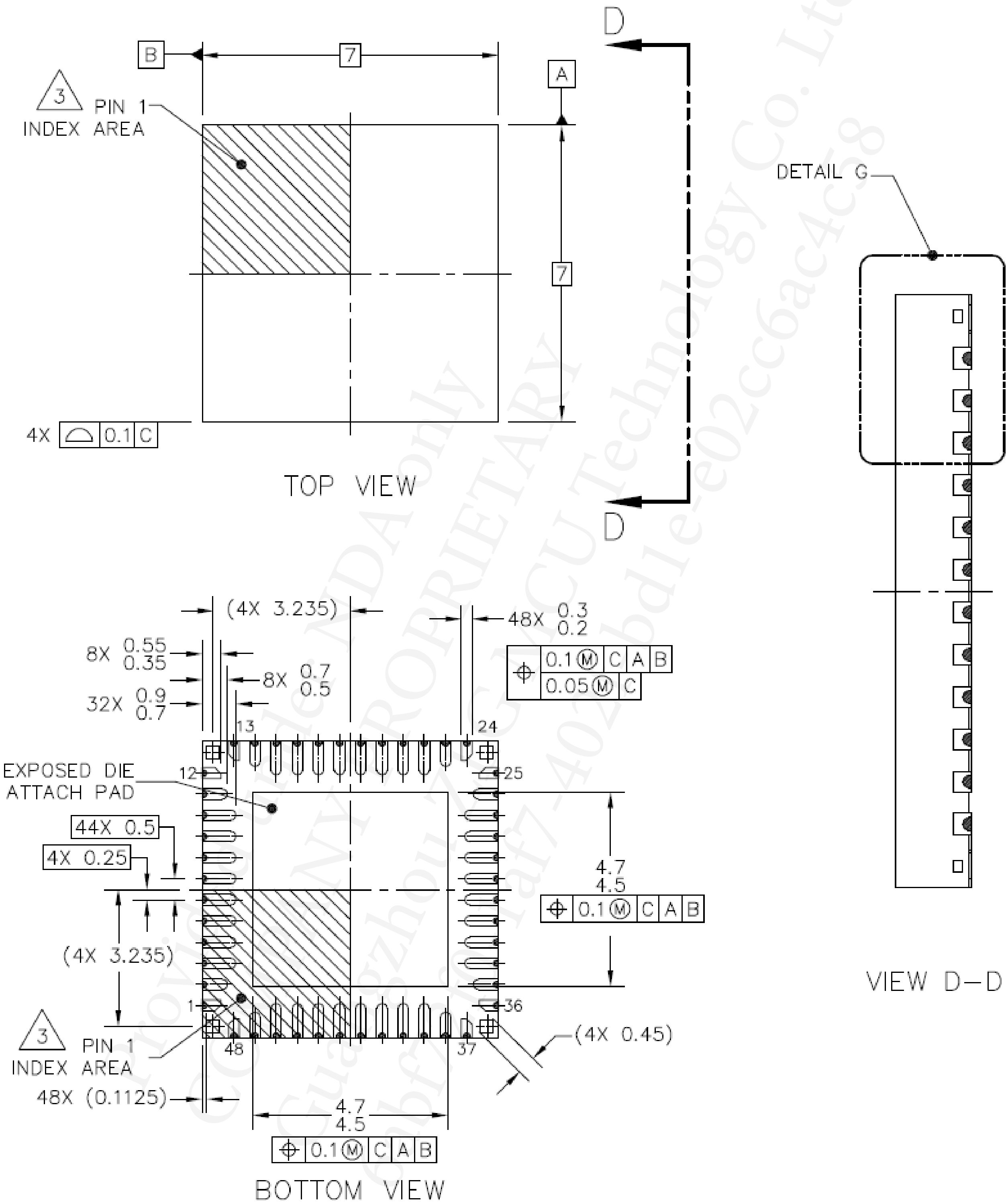
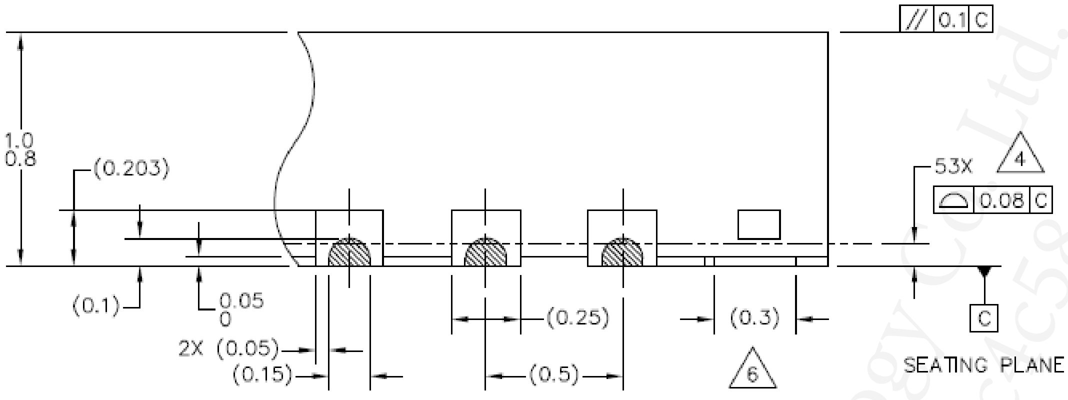


Figure 57. Example of application schematic, HVLDO1 version with external PNP, SPI interface

26 Package drawing

FS23 package is a QFN, thermally enhanced, wettable flanks, 7 x 7 x 0.85 mm, 0.5 mm pitch, 48 pins.

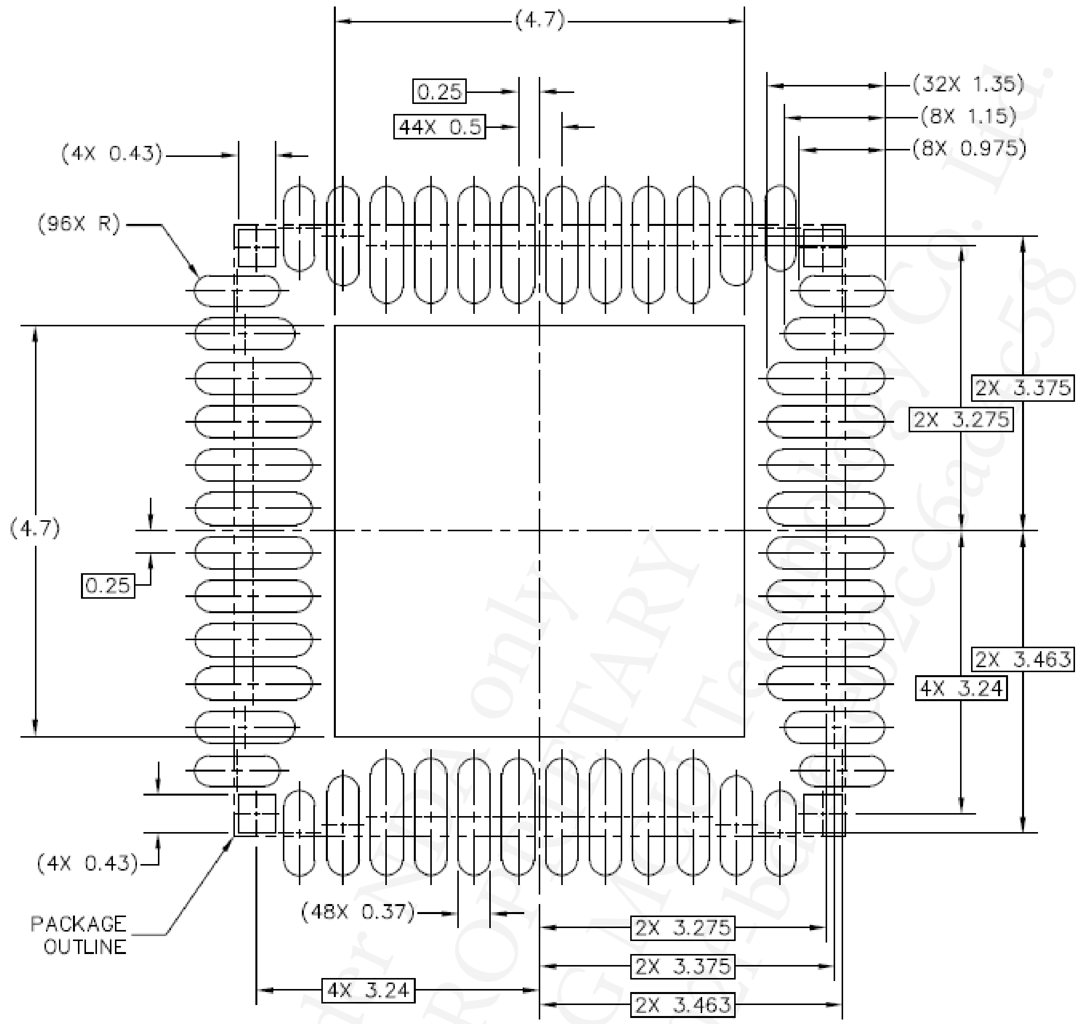




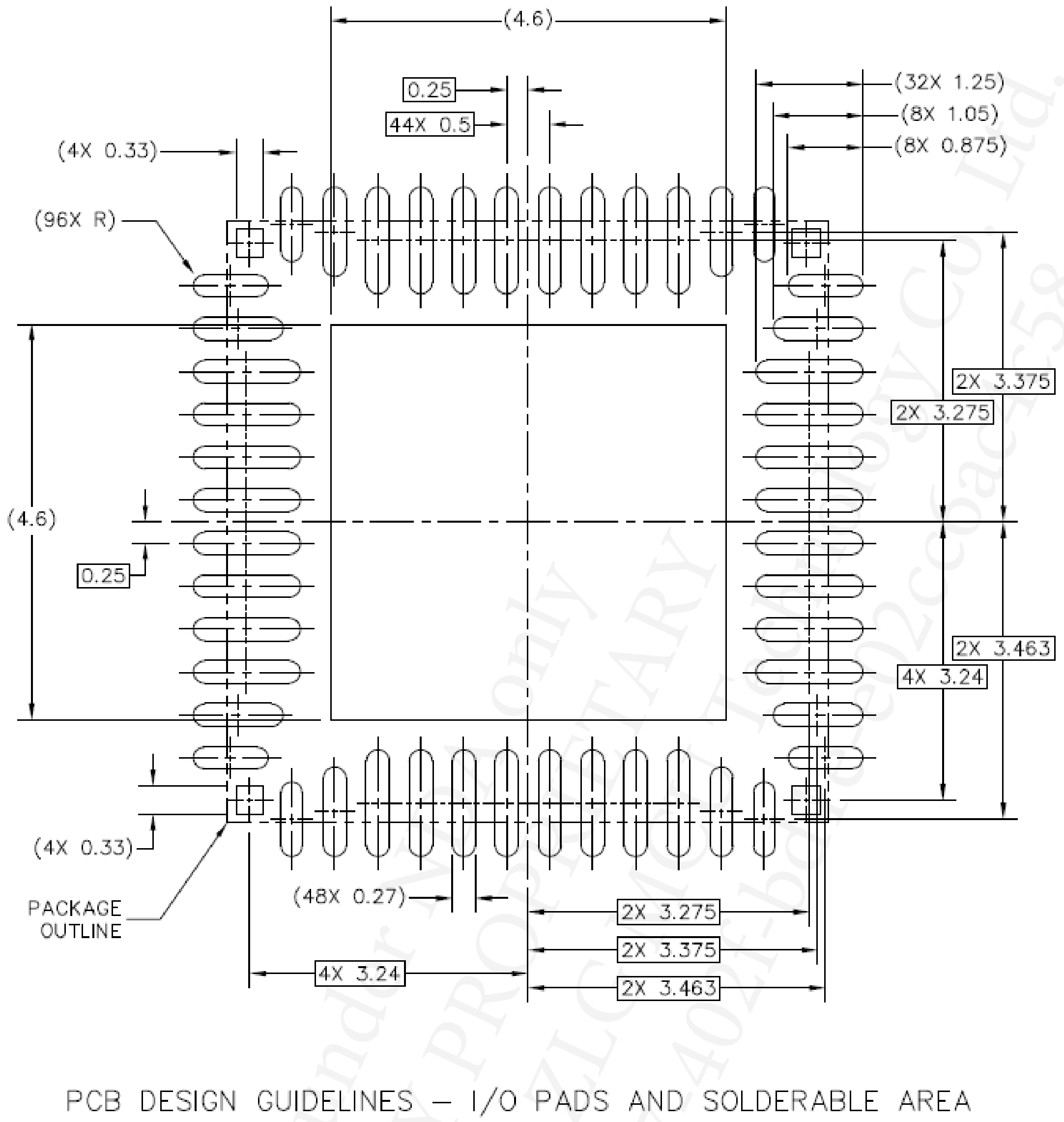
DETAIL G
VIEW ROTATED 90° CW

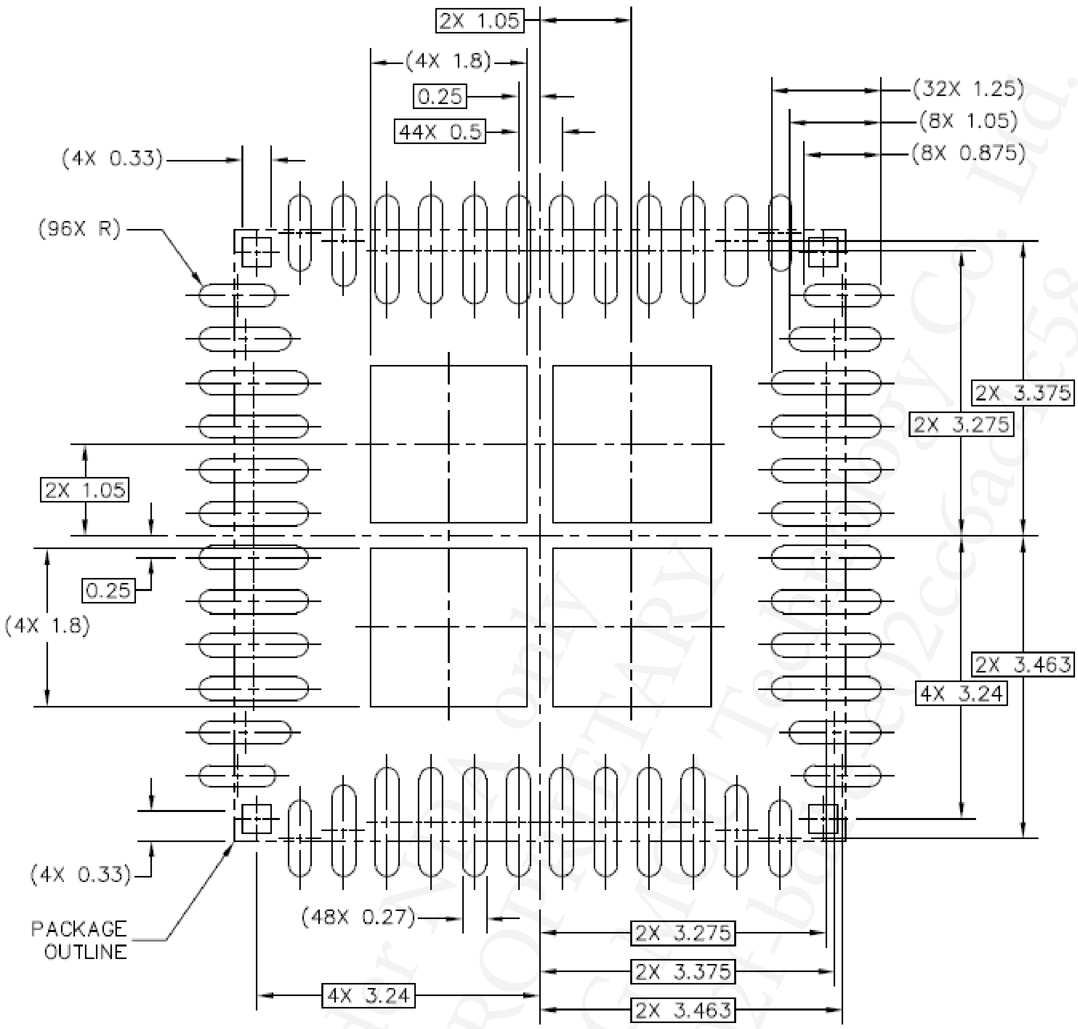
NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M−1994.
3. PIN 1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. COPLANARITY APPLIES TO LEADS AND DIE ATTACH PAD.
5. MIN. METAL GAP FOR LEAD TO EXPORED PAD SHALL BE 0.2 MM.
6. ANCHORING PADS.



PCB DESIGN GUIDELINES — SOLDER MASK OPENING PATTERN


(4.6)
0.25
44X 0.5
(4X 0.33)
(96X R)
(32X 1.25)
(8X 1.05)
(8X 0.875)
2X 3.375
2X 3.275
(4.6)
0.25
2X 3.463
4X 3.24
(4X 0.33)
PACKAGE
OUTLINE
(48X 0.27)
2X 3.275
2X 3.375
4X 3.24
2X 3.463
PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA



RECOMMENDED STENCIL THICKNESS 0.125

PCB DESIGN GUIDELINES — SOLDER PASTE STENCIL

Revision history

Table 248.

Document ID	Release date	Data sheet status	Change notice	Supercedes
FS23 v.4	20230915	Product		FS23 v.3

Modifications:

- Updated status to "Product"
- Global updates for style and grammar
- Updated Figure 1, Figure 3, Figure 4, Figure 7, Figure 11, Figure 13, Figure 14, Figure 54, Figure 55, Figure 56, Figure 57
- Section 12.3; Section 12.6; Section 13.3.1; Section 15.3.1; Section 15.3.2; Section 17; Section 18.1.1; Section 18.1.1.4; Section 18.2: Updated text
- Features and benefits: Added "EMC compliance" section
- Updated Table 2; Table 32; Table 33; Table 247
- Table 9: Changed I_{LPOFF_25} Max value from "40" to "50".
- Added Section 12.1
- Updated section title from "Simplified functional state diagram" to Detailed functional state diagram.
- Updated appearance of Table 10.
- Removed section titled "EMC compliance"
- Adjusted position of Section 12.2.
  - Added bullet item after "The FS23 will also wake up from LPON ..." beginning "Fail-safe mode ..."
  - Table 10: Added column titled "Fail-safe".
- Section 12.7: Inserted Figure 15, Figure 16.
- Section 12.8: Updated item 5.
- Section 12.9.1: Updated first bullet item under "In HVBUCK use case only:"
- Table 12: Updated V_{BOS_POR} Min value from "2.5" to "2.45", updated "$I_{BOS\_HP\_LIM}$" to "$I_{BOS\_LP\_LIM}$".
- Section 13: Updated "The FS23 starts when VSUP > V_{SUP_UVH}, " to "The FS23 starts when VSUP > V_{SUP_UV}, … "
- Table 14: Removed "With VBOS = 5 V" from Description of "V_{BUCK_IN}"; updated Descriptions and Min/Typ/Max values for "$I_{OC\_AVG\_PWM}$" and "$I_{OC\_PK\_PWM/PFM}$"
- Section 18.1.2: Updated Description of "$V_{CAN\_OUT\_DIFF\_REC}$" from "RL = 2240 Ω" to "no load, C1 = C2 = CCANRXD = 0 pF"
- Table 28: Updated I_{OC_HSx} Max value from "350" to "380".
- Table 49: Updated title of third column from "VxMON_OVDGLT_OTP[1:0]" to "VxMON_OVDGLT_OTP".
- Table 50
  - Added "VxMON_OVDGLT_OTP = 0" and "VxMON_OVDGLT_OTP = 1" to Parameters for Symbol "T_{OV_DGLT}".
  - Added "VxMON_UVDGLT_OTP[1:0] = 00", "VxMON_UVDGLT_OTP[1:0] = 01", "VxMON_UVDGLT_OTP[1:0] = 10", and "VxMON_UVDGLT_OTP[1:0] = 11" to Parameters for Symbol "T_{UV_DGLT}"
- Section 19.5.3: Added two bullets starting "Negative overcurrent ..." and "OC timeout ..."
- Updated appearance of Table 53.
- Table 80: Updated Bit 3 Description from "0 BUCK" and "1 BUCK" to "0 HVBUCK" and "1 HBUCK".
- Table 85: Updated four instances of "Leave" to "Exit".
- Table 143: Updated Bit 8 Descriptions values from "7.5" and "14" to "10.5" and "20", respectively.
- Table 173: Updated Bit 5 to 8 Description from "1011 64 ms (default value)" to "1101 256 ms (default value)".
- Table 191: Updated OTP_DEVICE_VER Bit 7 from "Reserved" to "KEY_OFFON_EN_OTP".
- Table 203: Updated Description for Bit 0 to 5.
- Table 231: Updated Description for Bit 5 from "1 Slot 1 and Slot 2 are bypassed" to "1 Slot 1 and Slot 2 are bypassed when waking up from LPON".
- Updated .
- Added "Reference" column to Table 72, Table 73, Table 190,

Table 248. *...continued*

Document ID	Release date	Data sheet status	Change notice	Supercedes
FS23 v.3	2023/03			FS23 v.2
Modifications:	• Global updates for style and grammar • Updated structure of Revision history • Updated section titled "Maximum Ratings" to Limiting values			
FS23 v.2	2023/03			FS23 v.1.1
Modifications:	• Update Table 1, Table 2, Table 7, Table 9, Table 12, Table 13, Table 14, Table 17, Table 18, Table 19, Table 20, Table 21. Add Table 10, Table 62, Table 63. • Update Figure 2, Figure 3, Figure 9, Figure 10, Figure 28, Figure 47. Add Figure 51. • Add section 13.3 “Operation and power modes” • Update section 13.4 “INIT state machine” • Update section 13.6 “Debug and OTP modes” • Update section 14 “Power management” • Update section 18.1 “Calibration procedure” • Update section 21 “MCU communication” • Add section 22.1 “Readable registers” • Add section 22.2 “Writable registers” • Update section 24 “OTP Register mapping” • Update section 25 “OTP Register description” • Update SPI / I²C register map and description (paragraphs 22 and 23). • Correct typos.			
FS23 v.1.1	2022/05			FS23 v.1
Modifications:	• Update Table 1, Table 2, Table 4, Table 6, Table 8, Table 9, Table 11, Table 25, Table 51, Table 52, Table 54, Table 80, Table 187. • Update Figure 2, Figure 3, Figure 4, Figure 5, Figure 9, Figure 11, Figure 12, Figure 24, Figure 49, Figure 50, Figure 51. • Add “HVBUCK clock management” paragraph (14.2) • Add SPI / I²C register map and description (paragraphs 22 and 23). • Add OTP register map and description (paragraphs 24 and 25). • Correct typos.			
FS23 v.1	2022/01			
Modifications:	• Initial release			

27 Legal information

27.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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[2] The term 'short data sheet' is explained in section "Definitions".
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